ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

DESIGN OF A CONFIGURABLE BANDWIDTH PLL USING ADAPTIVE APPROACH

M.Sc. THESIS

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

ADAPTİF YAKLAŞIM KULLANILARAK BAND GENİŞLİĞİ PROGRAMLANABİLİR BİR FKÇ SİSTEMİ TASARIMI

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Umut YILMAZER, a **M.Sc** student of ITU **Graduate School of Science, Engineering and Technology** student ID **504091261**, successfully defended the **thesis** entitled **"Design of a Configurable Bandwidth PLL Using Adaptive Approach"**, which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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FOREWORD

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May 2012

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ABBREVIATIONS

PLL : Phase locked loop
FKÇ : Faz Kilitlemeli Çevrim
VCO : Voltage Controlled Oscillator
CCO : Current Controlled Oscillator
Q : Quality Factor
DDR : Double-Date Rate
SERDES : Serializer and Deserializer
SIP : System Packet Interface
SONET : Synchronous Optical Networking
PFD : Phase-Frequency Detector
PD : Phase Detector
TVC : Time to Voltage Converter
DPFD : Digital Phase-Frequency Detector
SAR : Successive Approximation Register
DAC : Digital to Analog Converter
V2I : Voltage to Current Converter
SRLF : Sample-Reset Loop Filter
CML : Current Mode Logic
EMI : Electromagnetic Interference

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DESIGN OF A CONFIGURABLE BANDWIDTH PLL USING ADAPTIVE APPROACH

SUMMARY

The recent advances in communication and multimedia technologies have increased the desire in high performance systems. In most of these high performance systems, critical timing goals of the systems are achieved using PLL circuits.

There are many application areas for PLLs and each of these applications may need different requirements. Design of one type of PLL is simple, but as the number of designs increases it will be very time consuming and expensive to design and test different PLLs for different applications. Therefore, design of one configurable PLL is a better and time saving strategy.

In many applications, the VCO must cover a wide frequency range in order to accommodate process, voltage and temperature variations. The wide frequency range with today's scaled supply voltage technology leads to a large VCO gain. A large VCO gain makes PLL more susceptible to noise. Therefore, a VCO needs to be calibrated before use in PLL closed loop. For that purpose, an extensive review of VCO calibration methods in literature is given. Most of the calibration methods are based on frequency comparison techniques. In this work, a new frequency comparison technique is proposed. This auto calibration technique nearly eliminates the process and temperature dependency of the comparison and it is suitable for the frequency comparison in a wide frequency range. According to corner simulations, after calibrating in one sub-range, re-calibration is not needed even if the temperature changes marginally.

Adaptive PLLs have the capability of adjusting the loop dynamics adaptively and they have wide operating frequency range, wide multiplication range, low process and low temperature dependent loop dynamics. In this work, a new tracking mechanism between the natural frequency, stabilizing zero and the update frequency is proposed. The proposed PLL adaptively adjusts the loop dynamics using the update rate information. Thus, the PLL bandwidth can be adjusted to the desired value just by changing the loop update rate with a reference divider. Design and implementation of the system are given step by step with their theoretical analysis. The system is designed in 0.18µm CMOS technology.

The designed system can operate between 1 MHz-50 MHz update rate without threatening the stability and VCO covers 500 MHz-2500 MHz frequency range. The loop dynamics of the system have low process and temperature dependency. According to the simulations, bandwidth of the system changes less than ±10 percent with the process and temperature corners.

ADAPTİF YAKLAŞIM KULLANILARAK BAND GENİŞLİĞİ PROGRAMLANABİLİR BİR FKÇ SİSTEMİ TASARIMI

ÖZET

Günümüzde haberleşme ve multimedya uygulamalarının yaygınlaşması yüksek performansa sahip sistemlere ilgiyi artmıştır. Fiber optik sistemleri, radyo frekansı haberleşme devreleri ve yüksek hızlarda işaret işleme uygulamalarını sağlayan mikroişlemciler bu sistemlere örnek olarak verilebilir. Tüm bu uygulamalarda sistemin performansı saat işaretinin kalitesi tarafından sınırlanabilir. Bu yüzden yüksek performansa sahip bu sistemlerin birçoğu kritik zamanlama ihtiyaçlarından dolayı faz kilitlemeli çevrim (FKÇ) sistemlerini kullanır.

Bir sistemde PLL'in kullanım amacı sistemin kritik zamanlama ihtiyaçlarını karşılamak dışında sistem içerisindeki bir sinyalin sistem dışından uygulanan işarete senkron hale getirilmesi, saat işareti dağıtımı sırasında kaynaklanan gecikme ve kaymaların engellenmesi veya saat işaretlerinin frekanslarının kırmık üzerinde hassas bir şekilde çarpılması olabilir.

FKÇ sistemlerinin bir çok uygulama alanı vardır ve bu uygulamalar farklı PLL özellikleri gerektirebilir. Gereksinimlere göre düşük band genişliğine, yüksek band genişliğine ya da adaptif band genişliğine sahip bir PLL'e ihtiyaç duyulabilir.

Düşük band genişliğine sahip bir PLL referans işaretindeki yüksek frekanslı seğirmeleri (jitter) filtreleyebilir. Fakat bu PLL'lerin kilitlenme süreleri yüksek band genişliğine sahip PLL'lere göre oldukça uzundur. Bununla birlikte düşük band genişliğine sahip bir PLL'i kullanmak saat işaretinin seğirme bakımından temiz olması durumunda avantajlı olmayabilir. Bu durumda VCO'nun faz gürültüsünden kaynaklı gürültünün PLL'in çıkış işaretine etkisi artar. Eğer tasarımın düşük band genişliğine sahip bir PLL ile düşük gürültüye sahip çıkış işareti elde etme ihtiyacı varsa yüksek kalite faktörüne sahip VCO'lar PLL sistemi içerisinde kullanılabilir. Böylece sistem hem referans işaretindeki yüksek frekans bileşenlerine sahip seğirmeyi filtrelerken hem de VCO'nun faz gürültüsünün çıkış işaretine etkisi de filtrelenmiş olur. Yüksek kalite faktörüne sahip VCO'ların dezavantajı kırmık üzerinde oldukça fazla yer kaplamaları ve dar bir çalışma bölgesine sahip olmalarıdır.

Yüksek band genişliğine sahip PLL'lerin avantajı VCO faz gürültüsünü iyi bir şekilde filtrelemelerinden dolayı uzun zamanlı seğirmelerinin (long term jitter) düşük olmasıdır. Yüksek band genişliğine sahip PLL'ler ayrıca VCO faz gürültüsünü iyi bir şekilde filtrelemelerinden dolayı düşük kalite faktörüne sahip VCO'ların kullanılmasına olanak sağlamaktadır. Bu VCO'lar kırmık üzerinde az yer kaplamaları, geniş çalışma bölgelerine sahip olma gibi özellikleri sayesinde günümüz tasarımlarında kendilerine oldukça fazla yer bulmaktadır.

Yukarıda bahsedilen PLL'ler dışında çevrim dinamiklerini adaptif bir şekilde ayarlayan PLL'ler de vardır. Bu PLL'ler geniş frekans aralığında çalışabilip, düşük üretim ve sıcaklık duyarlılığına sahip çevrim dinamiklerine sahiplerdir. Sistem yenilenme frekansının değişimiyle bu PLL'lerin band genişliği yenilenme frekansını takip etmektedir. Yüksek yenilenme frekanslarında PLL'in band genişliği artarak VCO faz gürültüsünden kaynaklı seğirmeyi de iyi bir şekilde filtrelemektedir.

Literatürde birçok adaptif PLL tanıtılmıştır. Bu PLL'lerden bazısı sistemin doğal frekansı, kararlılığı sağlayan sıfırı arasında bir takip mekanizması kurarak adaptif band genişliği elde eder. Bu sistemlerin birçoğu örneklemeli-resetlemeli çevrim filtresi yapısı kullanır. Bu filtreler anahtarlamalı kapasite yapısındadır ve eşdeğer dirençleri anahtarlama frekansı değerine gore değişmektedir. Bu özellik kararlılığı sağlayan sıfırın çevrim yenilenme frekansını takip etmesini sağlamaktadır. Anahtar sayısının artması sistemin anahtarlama gürültüsüne olan duyarlılığını arttırdığı için anahtar sayısının arttırılması istenilmeyen bir durumdur. Literatürdeki başka bir PLL 3. dereceden çevrimle adaptif band genişliğini sağlamaktadır. Ancak kararlılık için büyük miktarda kapasiteye gereksinim duyma ve fazla miktarda anahtar içerme gibi dezavantajlara sahiptir. Literatürdeki en popüler PLL, Maneatis tarafından tasarlanmıştır. Bu PLL, düşük üretim ve sıcaklık duyarlıklı çevrim dinamiklerine sahiptir. Bununla birlikte yük pompasının akım referans değerinin VCO tarafından sağlanması, sistemde başlama sorunlarına ya da lineer olmayan kilitlenme davranışlarına sebep olabilmektedir. Ayrıca bu PLL herhangi bir VCO kalibrasyon yöntemini kullanmadığı için ileride değinileceği gibi PLL'in gürültü performansını kötü yönde etkileyebilir.

Birçok uygulamada VCO'nun üretim ve sıcaklık değişimleri gibi faktörlerden etkilenmemesi için geniş bir aralığı kapsamasına gereksinim vardır. Günümüzün düşük besleme gerilimleri ve artan yüksek çalışma hızları düşünüldüğünde VCO kazançlarının yüksek olması gerekir. Yüksek VCO kazancı PLL'in gürültüden daha fazla etkilenmesine neden olur. Yüksek VCO kazancını azaltıp, yine aynı çalışma bölgesinin kapsanması için birçok teknik vardır. Bu teknikler VCO frekans gerilim eğrisini birçok alt banda böler. Bu alt bandların seçimi VCO kapalı çevrimdeyken ya da açık çevrimdeyken gerçekleştirilebilir. Kapalı çevrim tekniklerinde VCO kontrol gerilimi, sistem tarafından önceden belirlenen gerilim değerleri arasında kalacak şekilde VCO kilitlenene kadar VCO alt bandları değiştirilir. Böylece uygun bir band bulunur. Bu yöntemin dezavantajı sistem her alt bandda kilitlenmeye çalıştığı için kalibrasyon süresi oldukça artmaktadır. Açık çevrim teknikleri genel olarak frekans karşılaştırma teknikleri üzerine dayanır. Açık çevrim yöntemlerinde PLL klasik faz karşılaştırmaya dayalı kitlenme çevrimine bırakılmaz. Bu yöntemlerde, VCO'nun bölünmüş geribesleme işaretinin frekansı ile referans işareti frekansları karşılaştırılarak, VCO'nun bandı karşılaştırma sonucuna göre değiştirilir ve uygun bir alt band bulunur.

Frekans karşılaştırma işlemi analog ve sayısal devreler yardımıyla yapılabilir. Analog yöntemlerde karşılaştırılacak olan işaretlerin periyodu gerilime çevrilerek analog karşılaştırıcı yardımıyla hangi işaretin daha yüksek ya da düşük frekansa sahip olduğu bulunur. Analog yöntemler hızlı kalibrasyon sürelerine karşın, eşleştirme, gürültü, offset, besleme gerilimi gibi faktörlerden oldukça fazla etkilenmektedir. Sayısal yöntemlerin az önce bahsedilen etkilerden oldukça az etkilenmesi bu yöntemlere olan ilgiyi arttırmıştır.

Literatürde birkaç sayısal frekans karşılaştırma tekniği tanıtılmıştır. Bunlardan birisi referans ve geribesleme işaretinin yükselen ya da düşen kenarlarını bir sayıcı ile sayarak, sayılan değerlerin sayısal bir karşılaşırıcı tarafından karşılaştırılması üzerine kuruludur. Bu yöntemin dezavantajı yüksek doğruluk için uzun süre sayma ihtiyacına gereksinim duyulmasıdır.

Yukarıda bahsedilen dezavantaj referans ve geribesleme işaretlerinin periyotlarının yüksek hızlı bir saat işareti tarafından sayılması ve sayısal bir karşılaştırıcı ile karşılaştırılması ile çözülmüştür. Bu yöntemin dezavantajı referans ve geribesleme işaretlerinin frekansının geniş bir aralıkta değişmesi durumunda karşılaştırma doğruluğunun azalmasıdır. Bu çalışmada bu eksiklik referans ve geribesleme işaretlerinin frekansının istenilen doğruluğu sağlayan sayıya bölündükten sonra karşılaştırılması yöntemiyle giderilmiştir. Bunun için önce referans işareti istenilen doğruluk elde edilene kadar 2'nin katlarına bölünür. Bu çalışmada istenilen doğruluk, sayıcının 255 değerini aşmasıdır. Bölünecek değer bulunduktan sonra referans ve geribesleme işaretleri aynı sayıya bölünerek karşılaştırılır. Bu yöntem ile yüksek doğruluklu bir karşılaştırma elde edilmiş olur. Bu yöntem ayrıca kalibrasyon süresini kapalı çevrim yöntemleri ve birçok sayısal karşılaştırma yöntemlerine göre hızlandırmaktadır. Kalibrasyon süresinin daha da kısalması istenilirse karşılaştırma doğruluğundan ödün verilerek 255 olarak belirlenen sınır değeri aşağıya çekilebilir. Simülasyon sonuçlarına göre VCO bir alt bandda kalibre olduktan sonra sıcaklık oldukça fazla değişse bile tekrar kalibrasyon gerekmemektedir.

Daha önce bahsedildiği gibi tek tip bir FKÇ sisteminin tasarımı basittir, ancak değişik uygulamalara yönelik sistemlerin sayısı arttıkça tasarım, test süresi ve maliyeti de oldukça artar. Bunun yerine programlanabilir bir sistem tasarımı yapmak daha iyi ve zaman tasarrufu sağlayan bir yaklaşımdır.

Adaptif FKÇ sistemleri tanıtımı kısmında bu sistemlerin çevrim dinamiklerini otomatik olarak ayarladığından bahsedilmiştir. Bu yöntem sistemin geniş çevrim yenilenme frekans aralığında üretim ve sıcaklık gibi faktörlerden fazla etkilenmeden çalışabilmesini sağlar. Bu çalışmada, sistemin doğal frekansı, kararlılığı sağlayan sıfırı ve çevrim yenilenme frekansı arasında yeni bir takip mekanizması kurulmuştur. Bu yöntem sistemin yenilenme frekansını kullanarak çevrim dinamiklerini değiştirir. Böylece istenilen band genişliği sadece referans bölücü devresini programlayarak elde edilebilir. Bu yöntem kısaca yük pompası devresinin akımının yenilenme frekansı ile orantılı yapılması ve VCO kazancının VCO frekansı ile orantılı olacak şekilde tasarlanması üzerine kuruludur. Sistemde kullanılan devrelerin analizi ve tasarımı adım adım verilmiştir. Sistemin tasarımı 0.18µm CMOS teknolojisi kullanılarak yapılmıştır.

Tasarımı yapılan sistem 1 MHz-50 MHz yenilenme frekansı aralığında çalışabilir. VCO'nun çalışma aralığı 500 MHz-2500 MHz'tir. Sistemin çevrim dinamikleri, üretim ve sıcaklık değişimlerinden az miktarda etkilenmektedir. Simülasyon sonuçlarına göre sistemin band genişliği üretim ve sıcaklık değişimlerinden ± %10'dan daha az etkilenmektedir.

1. INTRODUCTION

1.1 Motivation

The demand for high speed communication systems is increasing every day due to the exponential growth of internet and multimedia communications. High performance applications like fiber optic links, radio frequency communications and multi-gigahertz microprocessors require fast data transmission rates and high speed data processing. In those applications, performance of the system can be limited by the quality of clock signals. All of these high performance systems include phase locked loop (PLL) circuits in order to achieve the critical timing goals of systems such as avoiding setup/hold time violations, synchronization of internal signals to the external clock, minimization clock distribution delays and skew, multiplication of clock frequencies on chip precisely.

There are many application areas for PLLs. Many of them need different features and they have both advantages and disadvantages. These features and requirements are summarized in Table 1.1.

According to the requirements, a low bandwidth, a high bandwidth or an adaptive bandwidth PLL can be preferred. Low bandwidth PLLs can attenuate the high frequency jitter of the reference clock, but their lock time is usually longer than the lock time of high bandwidth PLLs. They also tend to have little overshoot in their frequency response. However, using a low bandwidth PLL may not be advantage, if the reference clock is not noisy. In this case, relative noise contribution of VCO to the output increases due to the lower bandwidth of PLL. If low noise is a design target with low bandwidth, high-Q VCOs can be used, but high-Q VCOs have some disadvantages such as occupying large chip area and having narrow operating range.

A high bandwidth PLL has the advantage of having low tracking jitter (long-term jitter) due to filtering of VCO noise. In this case, VCOs with a low quality factor can be used to obtain low long-term jitter. These VCOs have wide frequency range and smaller area, which make them attractive in area efficient designs. On the other hand,

high bandwidth PLLs cannot filter the reference clock jitter better than low bandwidth PLLs.

Table 1.1: Feature requirements of various PLL applications [1].

Applications	Requirements	Features
• Logic core clocks • Double-data rate (DDR) interfaces • Source-synchronous interfaces	• Minimum period jitter • Clock multiplication • May need frequency spreading	• Medium to low bandwidth • May need phase aligned divided clocks
• Synchronous interfaces (chips receiving data aligned with clock)	• Clock distribution de-skewing • Clock multiplication • Low tracking jitter	• High bandwidth • External feedback path
• SERDES (SPI4, etc.) transmit Path	• Low long-term jitter	• High bandwidth • Medium bandwidth with high-Q VCO
•High-speed SERDES (SONET) transmit path	•Very low long-term jitter	• Medium bandwidth with high-Q VCO
•SERDES receive path (clock and data recovery)	• Reject inter-symbol interference • Ignore missing transitions • Track data stream	• Medium bandwidth • May need multiple output phases
• Driving PLLs in SERDES cores	• May need low long-term jitter (if core does not use an high-Q VCO) • Clock multiplication	• High bandwidth
• Disk drive clock recovery	• Reject inter-symbol interference • Ignore missing transitions • Lock quickly to data stream	• Medium bandwidth • Fast locking
• Video clock generation	• Low long-term jitter • Low period jitter • Wide multiplication range for high fractional precision	• High tracking bandwidth • Pattern jitter rejection

There are some PLLs that have the capability of adjusting the loop dynamics adaptively. These PLLs have wide operating frequency range, wide multiplication range, low process and low temperature dependent loop dynamics. However, design of these PLLs is more complex than the other types of PLL. One of the adaptive PLLs proposed in [2] introduces a tracking mechanism between natural frequency and stabilizing zero using sample-reset loop filter technique. However, it requires programming of integral and proportional loop components according to input and

feedback divider ratios. In addition, it includes large number of switches, which increases the sensitivity to charge injection and clock feed-through. Another adaptive PLL introduced in [3] employs 3rd order loop with a fully-sampled loop filter, but its noise sensitivity degrades due to the large number of switches it includes. It also needs large amount of capacitor area to make the loop stable. One of the most popular architectures is self-biased PLL [4]. It achieves process and divider modulus independent PLL loop dynamics. However, charge pump bias voltage is provided by VCO. This may cause start-up or non-linear settling issues. Additionally, it does not use any VCO calibration methods, which may degrade noise performance of PLL.

In many applications, voltage controlled oscillators should cover wide frequency range in order to accommodate process, voltage and temperature variations. The wide frequency range with today's scaled supply voltage technology leads to a large VCO gain (Kvco). A large VCO gain makes PLL more susceptible to noise. There are some techniques to reduce VCO gain in order to reduce PLL phase noise and spurs [5-12]. These techniques are based on dividing tuning range into smaller bands using different approaches. In [5, 6], VCO control voltage is monitored continuously in closed loop operation. If the control voltage exceeds the pre-defined limits, VCO switches to another sub-range and loop tries to lock within the pre-defined control voltage limits. Calibration continues until the VCO is calibrated within the pre-defined control voltage limits. Since in each sub range PLL tries to settle to target frequency, this calibration type suffers from very long calibration time. The methods in [7, 8] are based on relative frequency comparison using analog comparison techniques. Reference and feedback signal periods of PLL are converted to voltage and these voltages are compared to find which signal is faster or slower. According to result of comparison, VCO switches another range to find a suitable range. Although calibration time of these circuits is short, their performance is much sensitive to mismatch and process variations. This problem is solved using digital frequency comparison techniques as in [9] and [10]. They count number of rising or falling edges of reference and feedback signals with digital counters to compare frequency of the signals. However, calibration takes long time for accurate comparison.

Fast and accurate frequency comparison problem is partially solved in [11, 12]. They use a high speed clock to count the reference and feedback signal periods. However,

accuracy of the comparison decreases as the frequency of reference and feedback signals increases. Therefore, they are not suitable for the comparison of the signals which have wide frequency range. In this work, this problem is solved by adding a scaler circuit. Scaler circuit divides reference and feedback signals according to the update frequency. Firstly, reference signal is divided by 2^N, where N is increased from 1 to 5 until the predefined accuracy criteria is satisfied. After N is decided, reference and feedback signals are divided by 2^N and comparison starts. This method nearly eliminates process dependency of the comparison and it is suitable for wide range signal frequency comparison. Compared to analog comparison methods [7, 8], proposed method becomes more attractive in deep submicron technologies.

As discussed above, the requirements by each application need design of different PLL circuits. Design and verification of one type PLL is simple, but as the number of designs increases, design cost and verification time increase too much. Instead of designing different PLL for each application, design of a single programmable PLL is a better and time saving strategy [4].

This thesis mainly focuses on the design of one configurable PLL that can provide large set of features in a wide frequency range without degrading the stability by adaptively adjusting the loop dynamics. An adaptive PLL requires a calibrated VCO, which also has the other advantages as discussed above. We calibrate the VCO using a frequency comparator circuit. Frequency comparator tries to make the frequency of the feedback signal close to the reference signal by changing VCO bits. A binary search algorithm is used in this thesis to reduce the acquisition time. This initial step finds the center current of VCO. VCO locks to the target frequency around this center point. VCO control voltage is applied to a linearized transconductance stage that changes VCO current linearly around the center point. Input range of this stage is proportional to the bandgap voltage, which has low temperature and process dependency. In this case, it can be shown that VCO gain becomes proportional to the update frequency. This is a key feature for building a simpler and more robust adaptive PLL as described in next sections.

Compared to self-biased PLL [4], charge pump current is determined during the coarse calibration not during the closed loop operation. Therefore, it will not bring any settling or start-up problems. Our charge pump circuit is designed such that its current is made proportional to the update frequency. Additionally, the classical loop

filter topology is changed with a sample reset loop filter. By using the sample reset loop filter, ripples on the control voltage decreases so that ripple pole is eliminated. Another advantage of the sample reset loop filter is that the zero frequency becomes proportional to the update frequency. Since VCO gain and charge pump current are proportional to the update frequency, loop bandwidth also becomes proportional to the update frequency. Therefore, PLL bandwidth can be adjusted to the desired value just by programming the loop update rate. Since the zero frequency is also proportional to the update frequency, increasing the bandwidth will not cause any stability problems as discussed in section 4.

1.2 Thesis Organization

In section 1, PLL requirements and features for different applications are discussed. This section also includes a literature review on VCO calibration methods and adaptive bandwidth PLLs with the contribution of this thesis.

Section 2 starts with the summary of the basic properties of PLLs. Furthermore, analysis of the single and dual loop charge pump PLL architectures in *s* domain using the linear model of PLLs are given in this section.

The VCO calibration techniques in literature are presented in section 3. At the end of this section, proposed VCO calibration technique is given.

Section 4 starts with general information about adaptive bandwidth PLLs. After that, proposed dual loop charge pump PLL architecture is described. Design of each of loop components are also given in this section.

Simulation results of the entire system are given in section 5. A comparative study of the designs within this research and recent significant publications are also summarized in this section.

Finally, in Section 6, a brief summary of the research is presented with the suggestions on the future work.

2. BASIC PROPERTIES OF PLLs

2.1 PLL Basic Theory

PLL is a feedback system that tries to minimize the phase error between the input and output of PLL. A simplified block diagram of PLL is shown in Figure 2.1. The phase detector (PFD) compares phase of the input and the feedback signal. The phase error information is smoothed by the loop filter to eliminate its high frequency components. The smoothed error value is used to tune VCO phase. The error information continues to change until the phase difference between the input and feedback signals is minimized. When the error signal is minimized, it is said that PLL is in locked state.

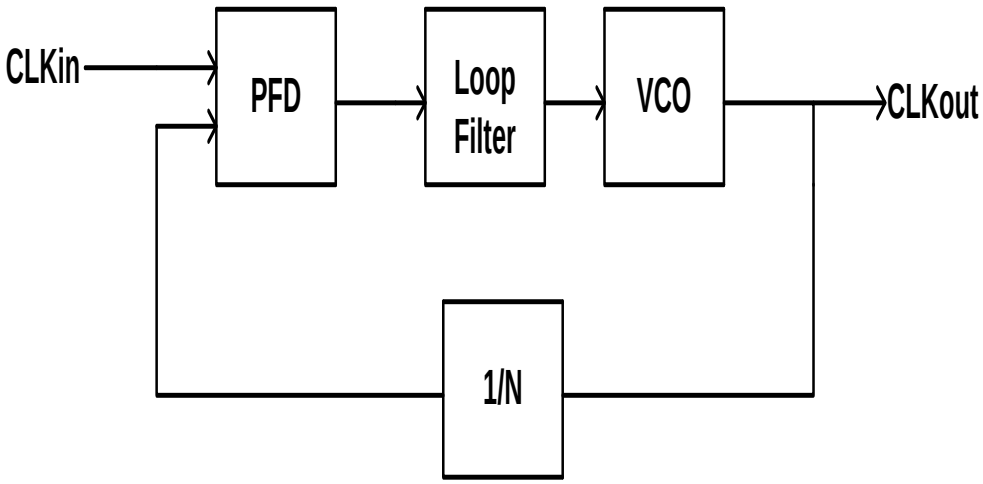

Figure 2.1: Simplified block diagram of a typical PLL.

2.2 Linear Model of PLLs

PLL is a linear system in the phase locked state [13]. A linear model makes PLL analysis simpler and it is useful to understand the overall system tradeoffs. We will start with a general linear model of PLLs and then focus on charge pump PLL linear models. A linear model for PLL is shown in Figure 2.2. It includes phase/frequency detector gain, K_{PD}, loop filter gain, G(s), VCO gain, K_{VCO}/s and divider gain, 1/N.

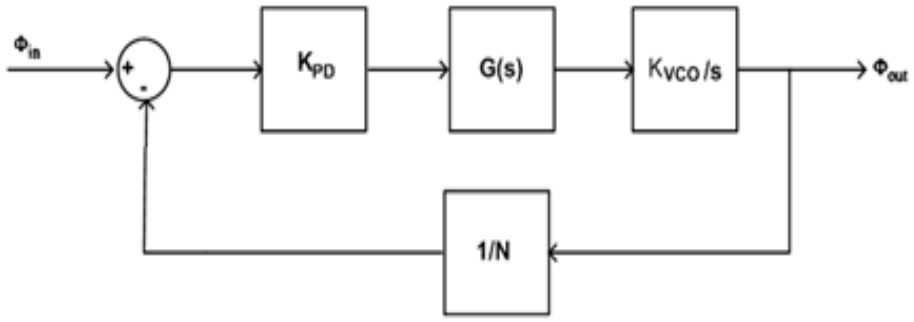

Figure 2.2: A linear model for PLL.

Phase detector can be characterized as

$$V_{PD} = K_{PD}\Delta\Phi \tag{2.1}$$

where K_{PD} is the phase detector gain and $\Delta\Phi$ is the phase difference between two inputs of the phase detector. G(s) is the transfer function of the loop filter. VCO can be modeled as an integrator. Its output phase can be given as

$$\Phi_{VCO}(s) = \frac{K_{VCO}}{s} V_{CTRL} \tag{2.2}$$

where V_{CTRL} is the control voltage of VCO and K_{VCO} is the gain of the VCO. Based on the block diagram in Figure 2.2, open loop transfer function of PLL can be written as

$$F(s) = \frac{K_{PD} G(s) K_{VCO}}{s} \tag{2.3}$$

Closed loop transfer function of PLL can be derived as

$$H(s) = \frac{F(s)}{1 + \frac{F(s)}{N}} = \frac{K_{PD} G(s) K_{VCO}}{s + \frac{K_{PD} G(s) K_{VCO}}{N}} \tag{2.4}$$

2.2.1 Linear model for conventional charge pump PLLs

Charge pump PLLs are widely used in high speed and lower jitter systems. The charge pump combined with the loop filter forms an integrator with infinite gain at DC. Therefore, it offers zero static phase error in ideal locked condition [13].

A conventional charge pump PLL is shown in Figure 2.3. It consists of a PFD, charge pump, loop filter, VCO and divider. PFD generates UP and DOWN signals according to phase difference between the input and output signals. PFD output signals are used to modify the voltage on the loop filter by adding or removing

charge through the charge pump [14]. Figure 2.4 shows change of average charge pump output current with the PFD input phase difference [15]. The gain of PFD-charge pump pair can be given as

$$K_{PD-CP} = \frac{I_{CP}}{2\pi} \tag{2.5}$$

The loop filter consists of a capacitor and a series resistor. The resulting control voltage on the loop filter controls VCO frequency.

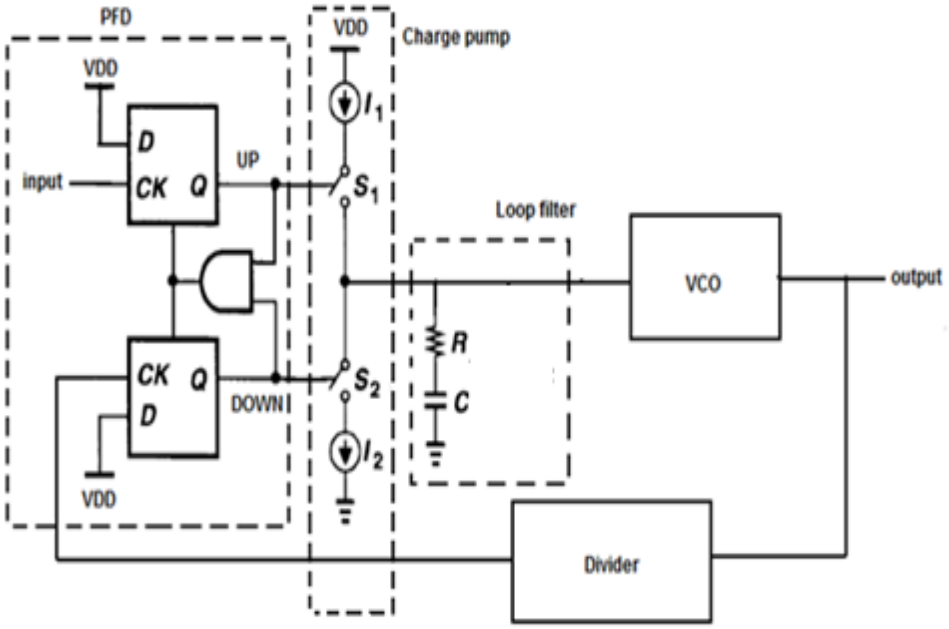

Figure 2.3: A conventional charge pump PLL.

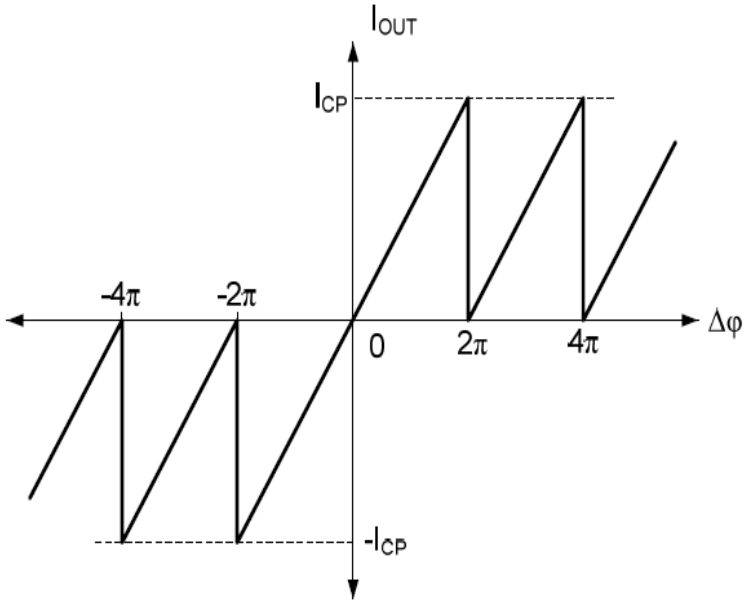

Figure 2.4: PFD-Charge pump pair waveform.

Using the linear model of the charge pump PLL shown in Figure 2.5, open loop transfer function of the charge pump PLL can be written as

$$F(s) = \frac{I_{CP}}{2\pi} \frac{K_{VCO}}{s} \frac{1+RsC}{sC} \tag{2.6}$$

Hence, the closed loop transfer function of the system is obtained as

$$H(s) = \frac{F(s)}{1+\frac{F(s)}{N}} = \frac{\frac{I_{CP}}{2\pi NC}(1+sRC)K_{VCO}}{s^2 + s\frac{I_{CP}}{2\pi N}K_{VCO}R + \frac{I_{CP}}{2\pi NC}K_{VCO}} \tag{2.7}$$

Dynamic behavior of PLL can be analyzed after converting the denominator of **(2.7)** to the generalized form of second order system: $s^2+2\zeta\omega_N s+\omega_N^2$, where ζ is the damping factor and ω_N is the natural frequency of the system. Thus, the system is characterized by

$$\omega_N = \sqrt{\frac{I_{CP}}{2\pi NC}K_{VCO}} \qquad \zeta = \frac{R}{2}\sqrt{\frac{I_{CP}}{2\pi N}K_{VCO}} \tag{2.8}$$

$$\omega_Z = -\frac{1}{RC} \tag{2.9}$$

From **(2.8)**, it is understood that the damping factor of the PLL is zero without a series resistor. Therefore, the system is unstable. This is because there are two integrators in the system. One of them is VCO and other one is the charge pump with the loop filter capacitor. Therefore, adding a series resistor to the loop filter capacitor increases system stability by creating a stabilizing zero. However, a series resistor causes voltage ripples on the VCO control voltage. For that reason, a ripple filtering capacitor is connected to the output of the loop filter. This capacitor introduces another pole that degrades the system stability.

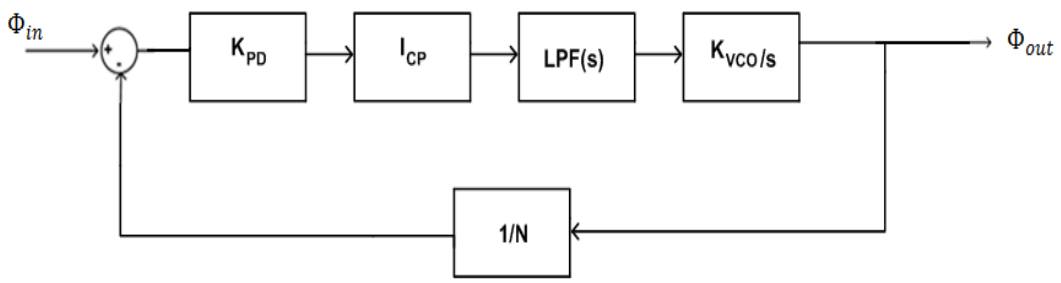

Figure 2.5: Linear model for conventional charge pump PLLs.

2.2.2 A linear model for dual loop charge pump PLLs

We have discussed that charge pump PLLs need a stabilizing zero in order to stabilize the loop. This can also be achieved by separating the fast and slow paths in the loop filter [2]. Figure 2.6 shows the dual loop charge pump PLL architecture. In this architecture, the slow path (integral path) holds the center frequency and the fast path (proportional path) responds to phase steps.

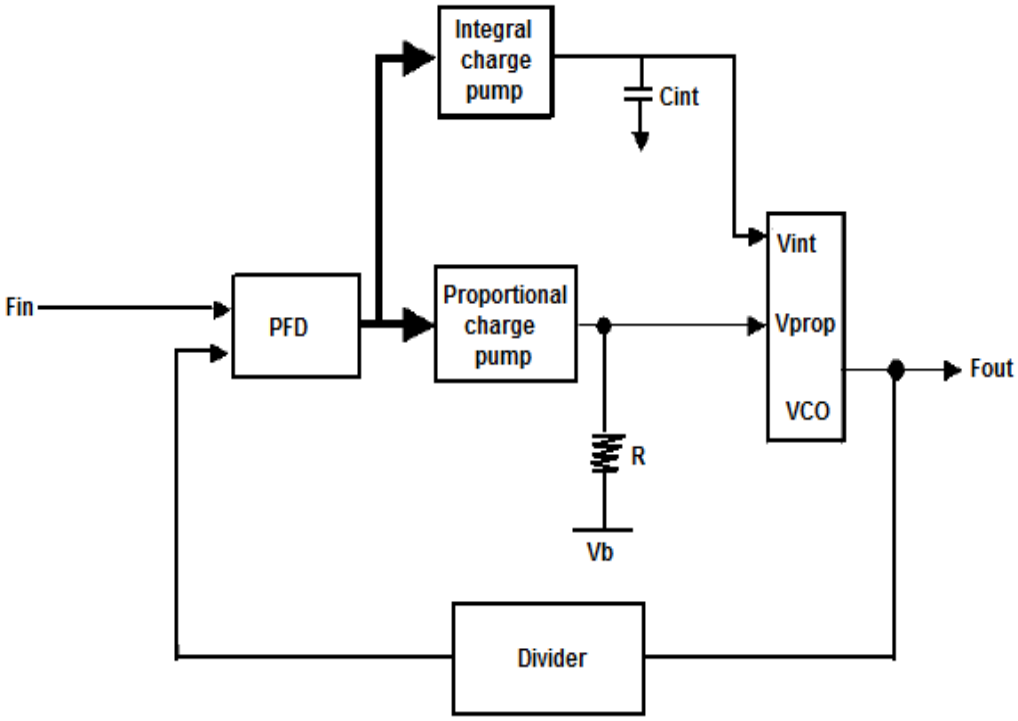

Figure 2.6: Dual loop charge pump PLL architecture.

This architecture has some advantages with respect to conventional charge pump PLLs. In conventional charge pump PLLs, VCO gain can not be increased too much due to the ripples on the control voltage. This limits the operating range of VCO and may cause VCO not to cover process, voltage and temperature variations. However, dual loop architecture allows lowering the proportional path VCO gain while keeping the integral path VCO gain high. This results in a better reference spur performance. Spurs can be decreased further with a ripple filtering capacitor connected parallel to the stabilizing zero. However, it creates another pole that degrades the system stability.

Seperating the two paths also makes the bias point of the integral and proportional path independent. As it will be shown in the next equations, adjusting the loop dynamics is also easier than the conventional charge pump PLLs.

Linear model of dual loop charge pump PLL is shown in Figure 2.7.

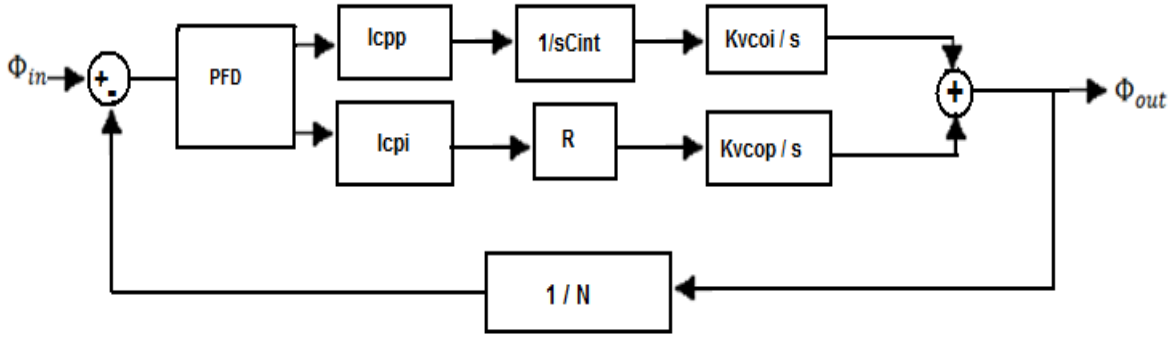

Figure 2.7: Linear model of dual loop charge pump PLL architecture.

Open loop transfer function of the system shown in Figure 2.7 can be written as

$$F(s) = \frac{I_{CPI}}{2\pi}\frac{K_{VCOi}}{s}\frac{1}{sC_{\text{int}}} + \frac{I_{CPP}}{2\pi}\frac{K_{VCOP}}{s}R \qquad \textbf{(2.10)}$$

Hence, the closed loop transfer function of the system is obtained as

$$H(s) = \frac{F(s)}{1+\frac{F(s)}{N}} = \frac{\frac{I_{CPI}}{2\pi C_{\text{int}}} + s\frac{I_{CPP}K_{VCOP}R}{2\pi}}{s^2 + s\frac{I_{CPP}K_{VCOP}R}{2\pi N} + \frac{I_{CPI}K_{VCOI}}{2\pi N C_{\text{int}}}} \qquad \textbf{(2.11)}$$

The system is characterized by

$$\omega_N = \sqrt{\frac{I_{CPI}K_{VCOI}}{2\pi N C_{\text{int}}}} \qquad \zeta = \frac{I_{CPP}RK_{VCOP}}{2}\sqrt{\frac{C_{\text{int}}}{I_{CPI}K_{VCOI}2\pi N}} \qquad \textbf{(2.12)}$$

$$\omega_Z = -\frac{I_{CPI}K_{VCOI}}{I_{CPP}RK_{VCOP}C_{\text{int}}} \qquad \textbf{(2.13)}$$

Comparing **(2.12)** and **(2.13)** with **(2.8)** and **(2.9)**, it can be said that dual loop architecture provides more design flexibility to designer. This is because there is less dependency between the loop dynamics with respect to the conventional charge pump PLLs. Additionally, in dual loop charge pump PLLs the stabilizing zero is not constant as in the single loop charge pump PLLs. In dual loop architecture, the stabilizing zero can be adjusted to the desired value by changing the charge pump currents. Therefore, dual loop architecture is more suitable for programmable PLLs.

3. VCO AUTOMATIC FREQUENCY CALIBRATION TECHNIQUES

In many applications, voltage controlled oscillators should cover a wide frequency range in order to accommodate process, voltage and temperature variations. The wide frequency range with today's scaled supply voltage technology leads to a large VCO gain (K_{VCO}). A large VCO gain makes PLL more susceptible to noise. There are some techniques to reduce VCO gain in order to reduce PLL phase noise and spurs [5-12]. These techniques are based on dividing VCO tuning range into smaller bands as shown in Figure 3.1. These sub-bands can be selected by switching capacitor arrays, resistors or changing bias currents. After choosing a proper sub-band, PLL can lock in that range.

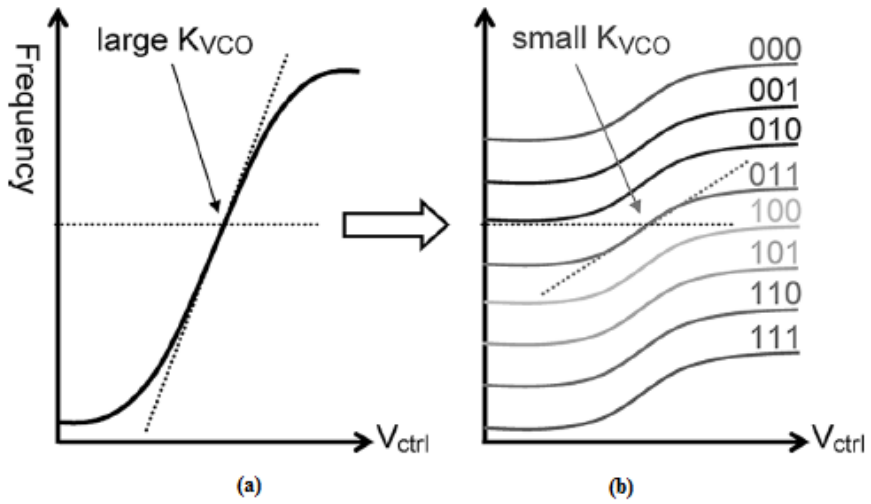

Figure 3.1: a) Single tuning curve with large Kvco and b) Tuning range is divided into sub-bands for smaller Kvco [7].

VCO calibration can be realized when PLL is in open or closed loop. Therefore, calibration techniques can be divided into two categories: open loop and closed loop calibration techniques [7].

3.1 Closed Loop Calibration Techniques

Closed loop calibration techniques are based on monitoring VCO control voltage continuously [5, 6]. A sample system, which is calibrated in closed loop, is shown in Figure 3.2.

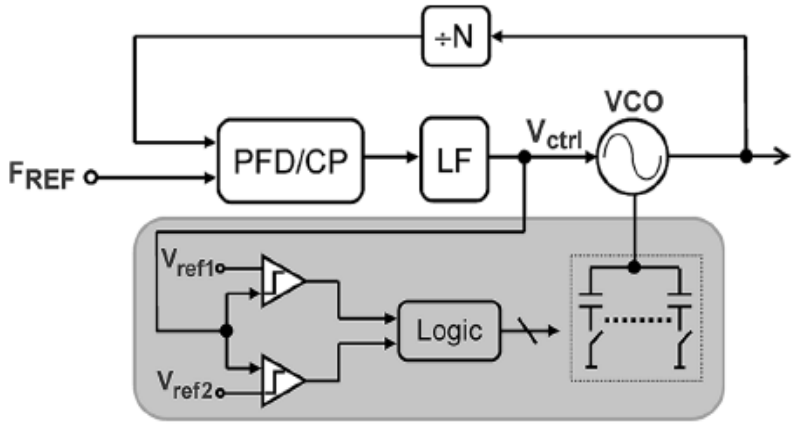

Figure 3.2: Closed loop calibration technique is based on monitoring control voltage continuously [16].

If Vctrl goes above or below the pre-defined limits, VCO switches to another sub-range and loop tries to lock within the pre-defined control voltage limits. Calibration continues until the VCO is calibrated within the pre-defined control voltage range. Since in each sub range PLL tries to settle to target frequency, this calibration type can be slow (hundreds of µsecs or msecs).

3.2 Open Loop Calibration Techniques

In open loop calibration techniques, VCO is calibrated when PLL is in open loop. VCO frequency is adjusted to the target frequency as close as possible (called as coarse tuning), then the loop is closed and PLL locks to the target frequency (called as fine tuning). This makes calibration time usually shorter than the closed loop techniques (several µsecs or sub µsec).

All of the open loop techniques are based on frequency comparison methods. Frequency comparison methods can be divided into two groups: period based [7, 8] and counter-based comparison methods [9-12].

3.2.1 Period based frequency comparison

In period based comparison systems, periods of reference and divided VCO signals are converted to voltage by time-to-voltage converter (TVC). Then, these two voltages are compared to decide which signal is faster and control logic circuit selects one of the frequency sub-bands of VCO. Comparison is repeated until the pre-defined criteria is satisfied. After comparison finishes, PLL tries to lock with the help of PLL loop.

A sample system that uses the period based comparison method is illustrated in Figure 3.3.

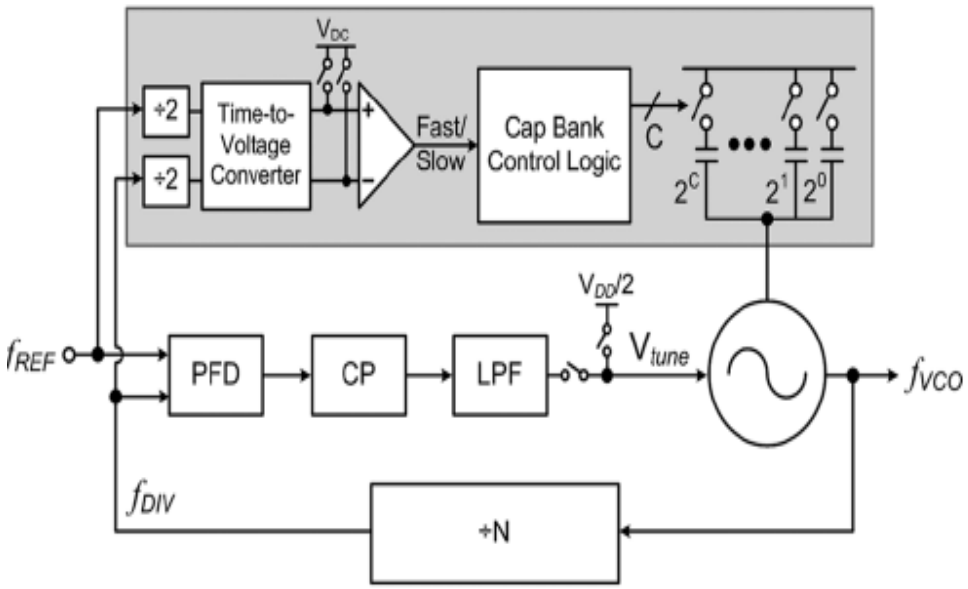

Figure 3.3: Period Based VCO calibration technique [16].

Time to voltage converters used in period based comparison systems can be much sensitive to mismatch and process variations due to their analog nature. In addition to this, comparator input offset value must be lower than the voltage difference at the comparator input. These are the basic design constraints of the period based comparison methods.

In [7] and [8], fast frequency comparison methods are proposed. Conceptual illustration of these circuits is shown in Figure 3.4. Both of the reference and the divided VCO signals are divided by 2 so that pulse widths represent signal periods. Instead of measuring the absolute periods of the signals, proposed method measures the period difference (ΔT) by a dual edge phase detector. Charge pump circuit converts period difference to voltage on C1 capacitor and the comparator decides which signal is faster according to its differential input voltage, $(I/C1).\Delta T$, where I is the charge pump current. Since $t_{dn}(I/C) \leq Vref$ is needed for proper comparison, I/C can be increased by decreasing t_{dn}. This is achieved if the phase difference between Fref/2 and $F_{VCO}/2N$ is selected properly. Higher I/C means higher differential voltage at the comparator input for the same period difference. Therefore, this method relaxes the design constraints with respect to the methods that compare absolute period of the signals.

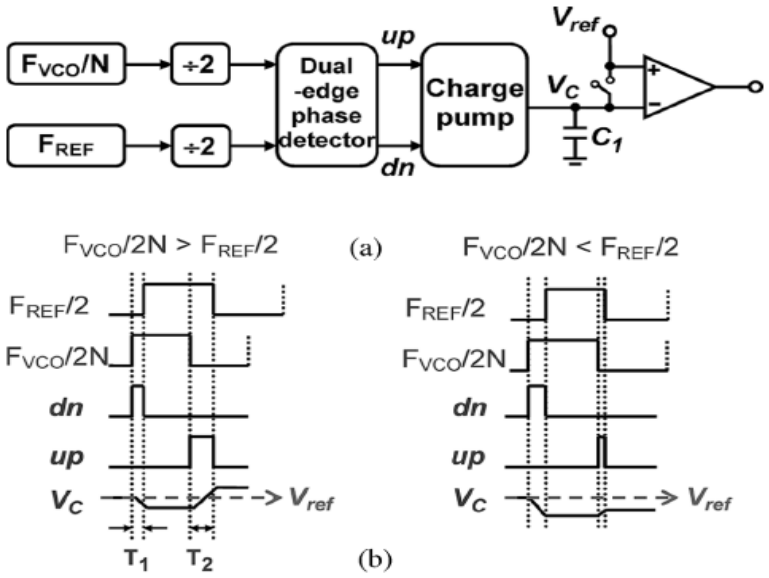

Figure 3.4: (a) Period based frequency comparison conceptual illustration. (b) Operation timing waveforms [7].

3.2.2 Counter based frequency comparison

Period based frequency comparison circuits are usually analog circuits that make them sensitive to mismatch and variations. Simple structures of digital circuits with their immunity to mismatch and variations have made them popular among the comparison methods. Modest calibration time is one of the disadvantages of this method [16]. Conceptual illustration of the counter based VCO calibration method is shown in Figure 3.5. Two counters count number of rising or falling edges of the reference and divided VCO signals. Then, the digital comparator decides which signal is faster. According to the comparator output, VCO frequency is increased or decreased by the control logic until the certain calibration accuracy is satisfied. This method is used in [9] and [10]. However, long calibration time is needed for accurate comparison.

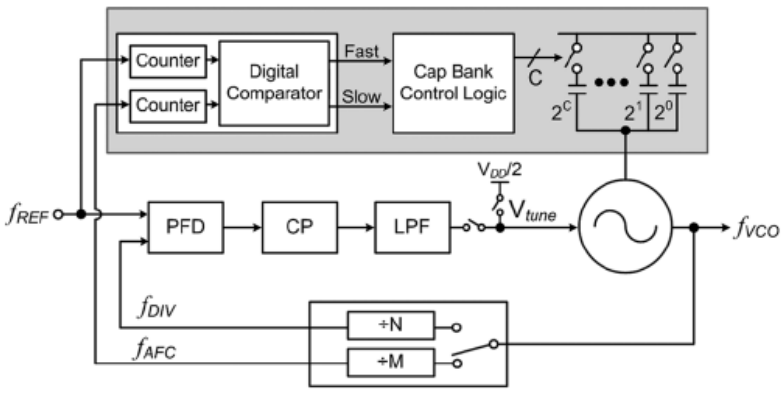

Figure 3.5: Conceptual illustration of counter based VCO calibration technique [16].

Fast and accurate frequency comparison problem is partially solved in [11, 12]. They use a high speed clock to count the number of high speed clock periods enclosed in one period of a signal. Counter output gives digital representation of the measured period in terms of high speed clock period. A digital comparator is used to compare the counter outputs. In this method, accuracy of the comparison decreases as the frequency of reference and feedback signals increase. Therefore, they are not suitable for the comparison of the signals that have wide frequency range.

3.2.3 Proposed calibration technique

Figure 3.6 shows conceptual illustration of frequency comparison used in [11, 12] and this work. Note that f_{osc} is generated by a RC oscillator.

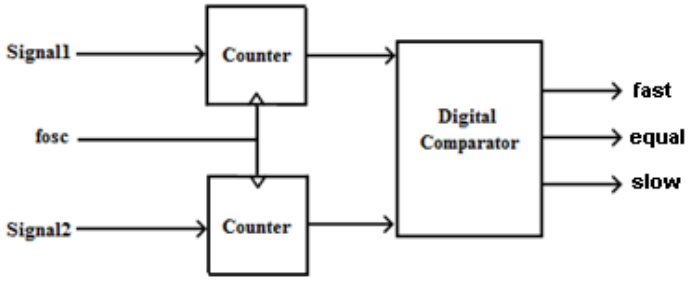

Figure 3.6: Conceptual illustration of frequency comparison using a high speed clock.

In this work, the problems in [11, 12] are solved using a scaler circuit. Since the accuracy of the frequency comparison decreases for high Fref and Fdiv values, we can compare $Fref/2^N$ and $Fdiv/2^N$ signals to have a better accuracy. Therefore, we use the scaler circuit to decide N value. Firstly, the reference signal is divided by 2^N, where N is increased from 1 to 5 until the predefined accuracy criteria is satisfied. N is chosen such that $fosc/(Fref/2^{N-1})>255$. Determined N value is presented by the 3 bit control signal. Finally, "done=1" signal is generated after the divider ratio determination process is completed.

Frequency divider block divides reference and feedback signals to N according to 3 bit control signal generated by the scaler circuit. $Fref/2^N$ and $Fdiv/2^N$ signals are counted by fosc and the frequency comparison is realized by the digital comparator. According to the comparator output, SAR logic changes DAC bits using binary search algorithm so that a suitable VCO sub-band is selected. Block diagram of PLL coarse calibration system is given in Figure 3.7.

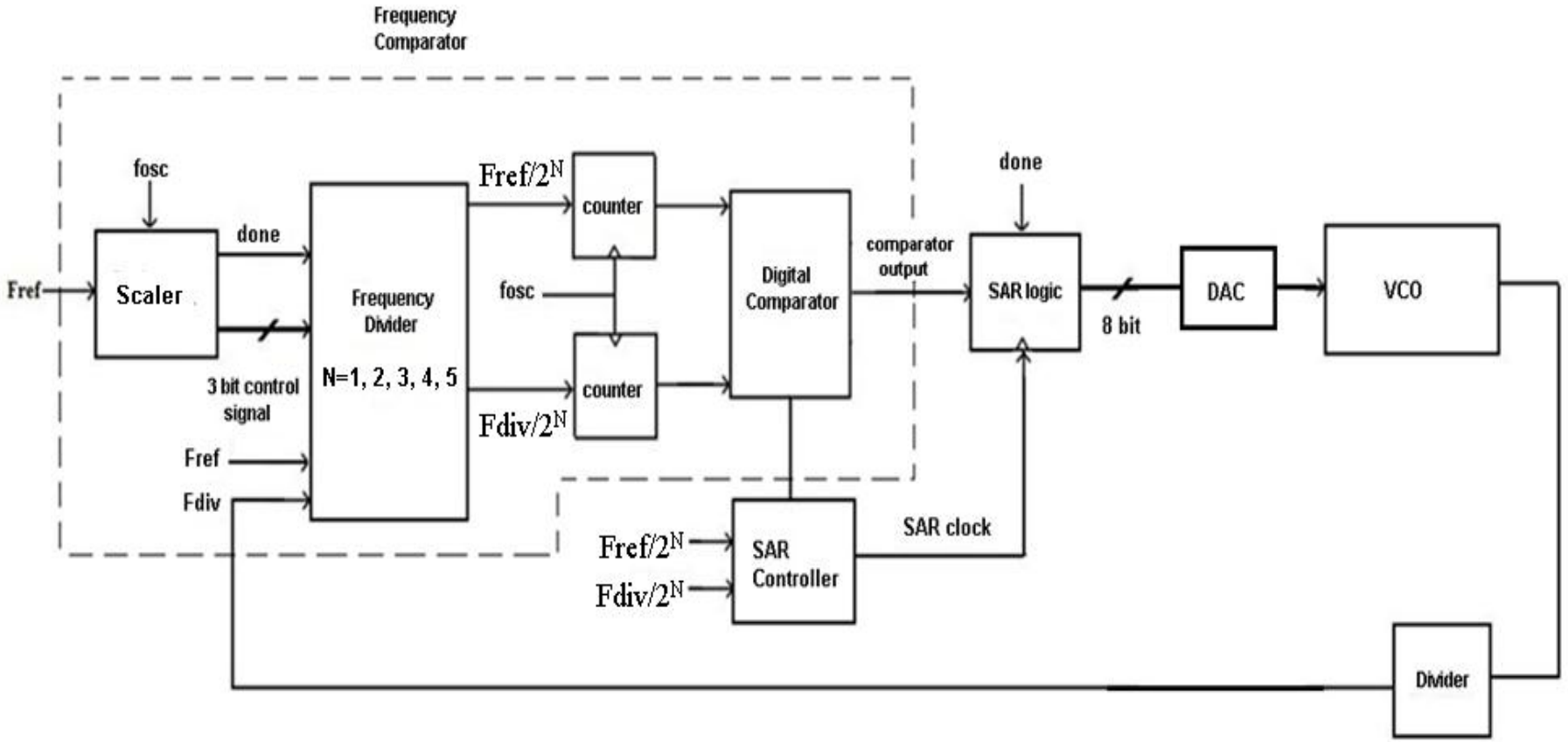

Figure 3.7: Block diagram of coarse frequency calibration circuit.

Simplified schematic of DAC with the frequency comparator is shown in Figure 3.8. 8 bit DAC is enough in this work to cover 500MHz-2500MHz VCO frequency range over process, temperature variations. Output current of DAC is used to bias VCO. Hence, this provides moving between VCO frequency sub-bands. PLL locks to the target frequency around this current. This will be discussed in the next section. DAC control word starts with '10000000'. After the 1st comparison, control word can be '11000000' or '01000000' according to digital comparator output. Frequency comparison finishes if the comparison result is equal. Otherwise, calibration continues until LSB.

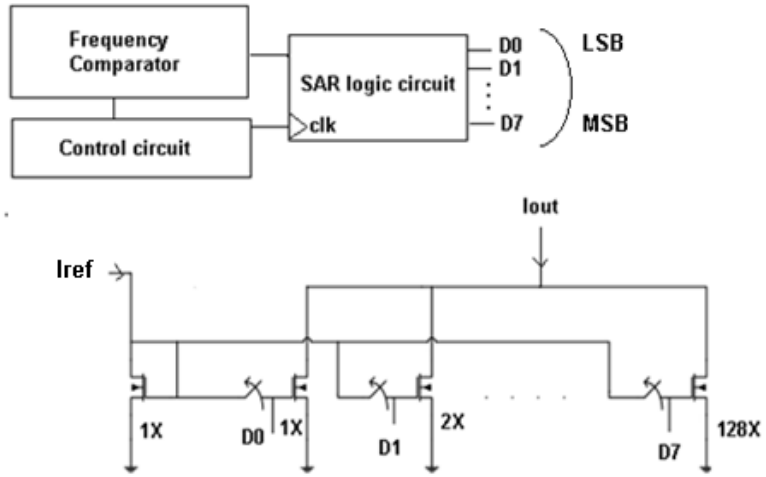

Figure 3.8: Simplified schematic of DAC with frequency comparator.

Figure 3.9 shows SAR logic schematic. Circuit consists of 8 similar cells. Each cell consists of 1 DFF, 1 Dlatch, 1 NAND, 1 OR, 1NOR and one delay element.

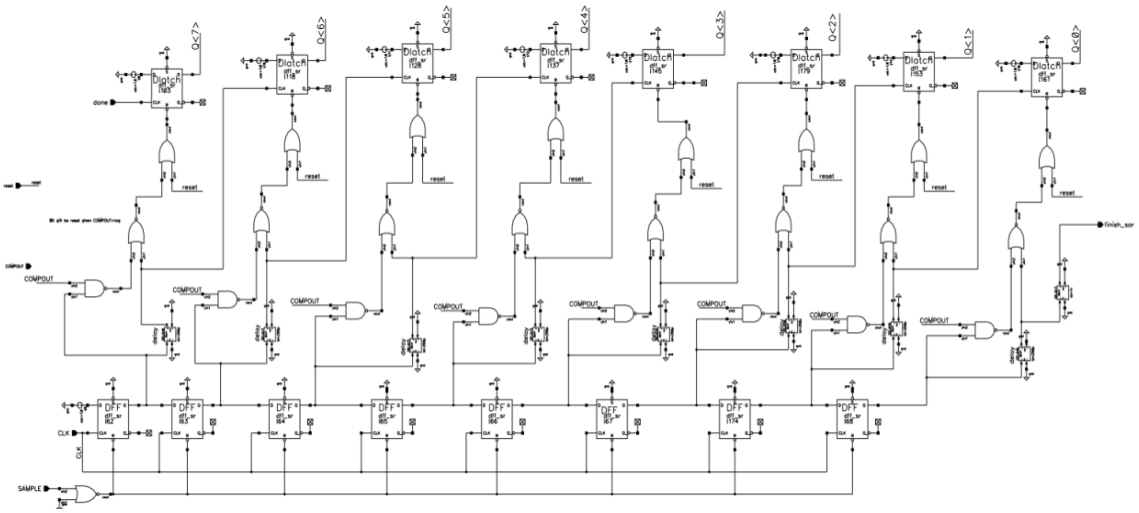

Figure 3.9: SAR logic schematic.

Figure 3.10 shows transistor level implementation of DAC current sources.

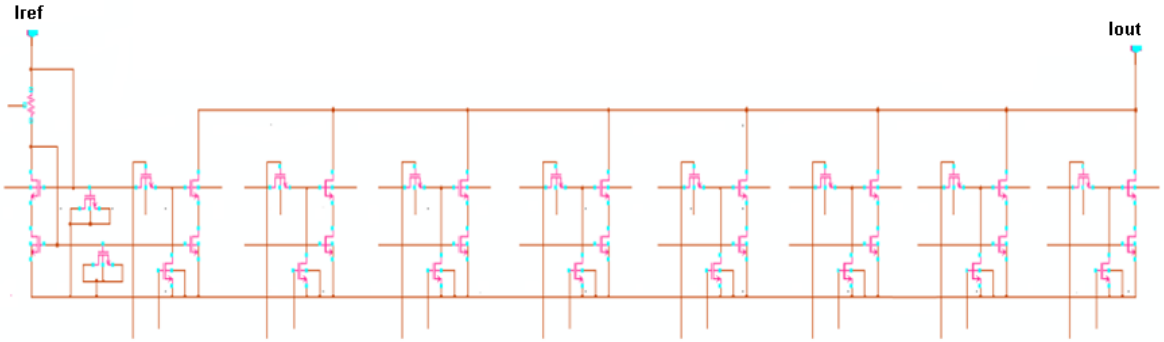

Figure 3.10: Schematic of DAC current sources.

Counters shown in Figure 3.7 are 12 bit ripple counters [17] and the digital comparator compares output of the two counters starting from MSB to LSB.

Figure 3.11 summarizes coarse frequency calibration algorithm.

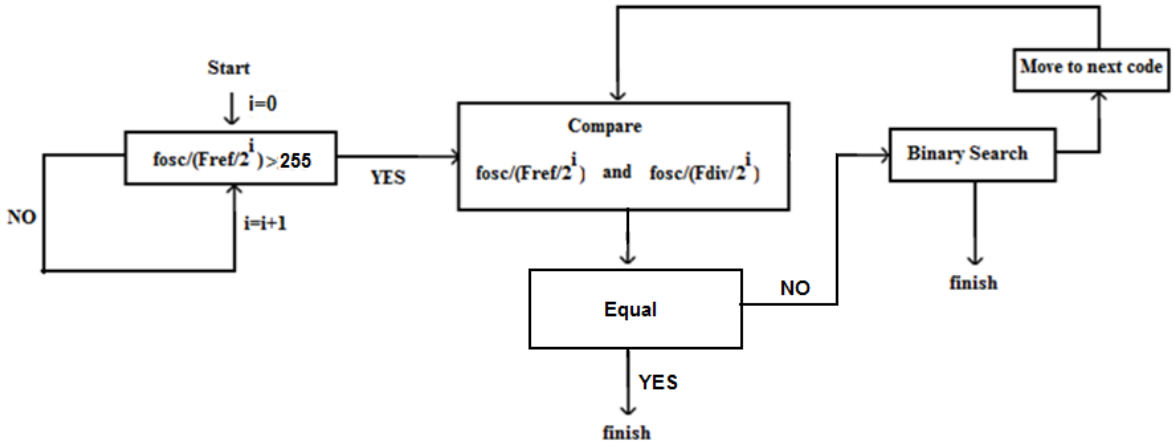

Figure 3.11: Flow chart of coarse calibration algorithm.

4. ADAPTIVE BANDWIDTH PLLs

An adaptive system has the capability of adjusting itself according to changing conditions. Therefore, these systems increase the system reliability and performance over a wide operating range. In this section, we will present a configurable bandwidth PLL using the adaptive bandwidth approach.

4.1 Proposed Programmable PLL Using Adaptive Approach

A classical PLL has a constant charge pump current, VCO gain and loop filter elements. This results in constant loop dynamics. However, process, voltage and temperature variations will cause large deviations from typical values that will not provide the optimum performance most of the time [18]. Since there are many applications that need different requirements, classical approach cannot respond to all requirements. Instead of designing different PLLs for each application, design of a single programmable PLL is a better and time saving strategy [4].

Adaptive bandwidth PLLs are not new. They have the capability of adjusting loop dynamics adaptively. These PLLs have wide operating frequency range, wide multiplication range, constant loop dynamics and low process and temperature dependency. There are some adaptive PLLs introduced in literature. One of the adaptive PLLs proposed in [2] introduces a tracking mechanism between natural frequency and stabilizing zero using sample-reset loop filter technique. However, it requires programming of integral and proportional loop components according to input and feedback divider ratios. Also, it includes large number of switches, which increases the sensitivity to charge injection and clock feed-through. Another adaptive PLL introduced in [3] employs 3^{rd} order loop with a fully-sampled loop filter, but its noise sensitivity degrades due to the large number of switches it includes. It also needs large amount of capacitor to stabilize the loop. One of the most popular architectures is self-biased PLL [4]. It achieves process and divider modulus independent PLL loop dynamics. However, charge pump bias voltage is provided by VCO. This may cause start-up problem or non-linear settling issues. Additionally, it

does not use any VCO calibration methods that may degrade the noise performance of PLL.

In order to reduce VCO gain, a new coarse calibration method was discussed in section 3. This method calibrates VCO frequency according to the update frequency using the frequency comparator circuit. Frequency comparator circuit tries to make the frequency of the feedback signal close to the reference signal frequency by changing VCO bits using binary search algorithm. This step finds center current of VCO. VCO locks to the target frequency around this center current. VCO control voltage is applied to a linearized transconductance stage that changes VCO current linearly around the center current. Input range of this stage is proportional to the bandgap voltage, which has low temperature and process dependency. In this case, it will be shown that VCO gain becomes proportional to the update frequency.

Compared to self-biased PLL [4], charge pump current is determined during the coarse calibration not during the closed loop operation. Therefore, it will not bring any settling or start-up problems. Charge pump circuit is designed such that charge pump current becomes proportional to the update frequency. Additionally, the classical loop filter topology is changed with a sample reset loop filter. By using the sample reset loop filter, ripples on the control voltage decreases so that ripple pole is eliminated. Another advantage of the sample reset loop filter is that the zero frequency becomes proportional to the update frequency. Since VCO gain and charge pump current is proportional to the update frequency, loop bandwidth also becomes proportional to the update frequency. Therefore, PLL bandwidth can be adjusted to the desired value just by programming the loop update rate.

4.2 Architecture of Proposed Programmable PLL

Proposed programmable adaptive bandwidth PLL is shown in Figure 4.1. It is composed of a frequency comparator, SAR logic circuit, 8bit DAC, phase frequency detector (PFD), proportional path and integral path charge pumps, integral path loop filter capacitor, sample-reset loop filter, integral and proportional path voltage to current converts ($V2I_i$ and $V2I_p$), current controlled oscillator (CCO), charge pump updater circuit and programmable M and N dividers.

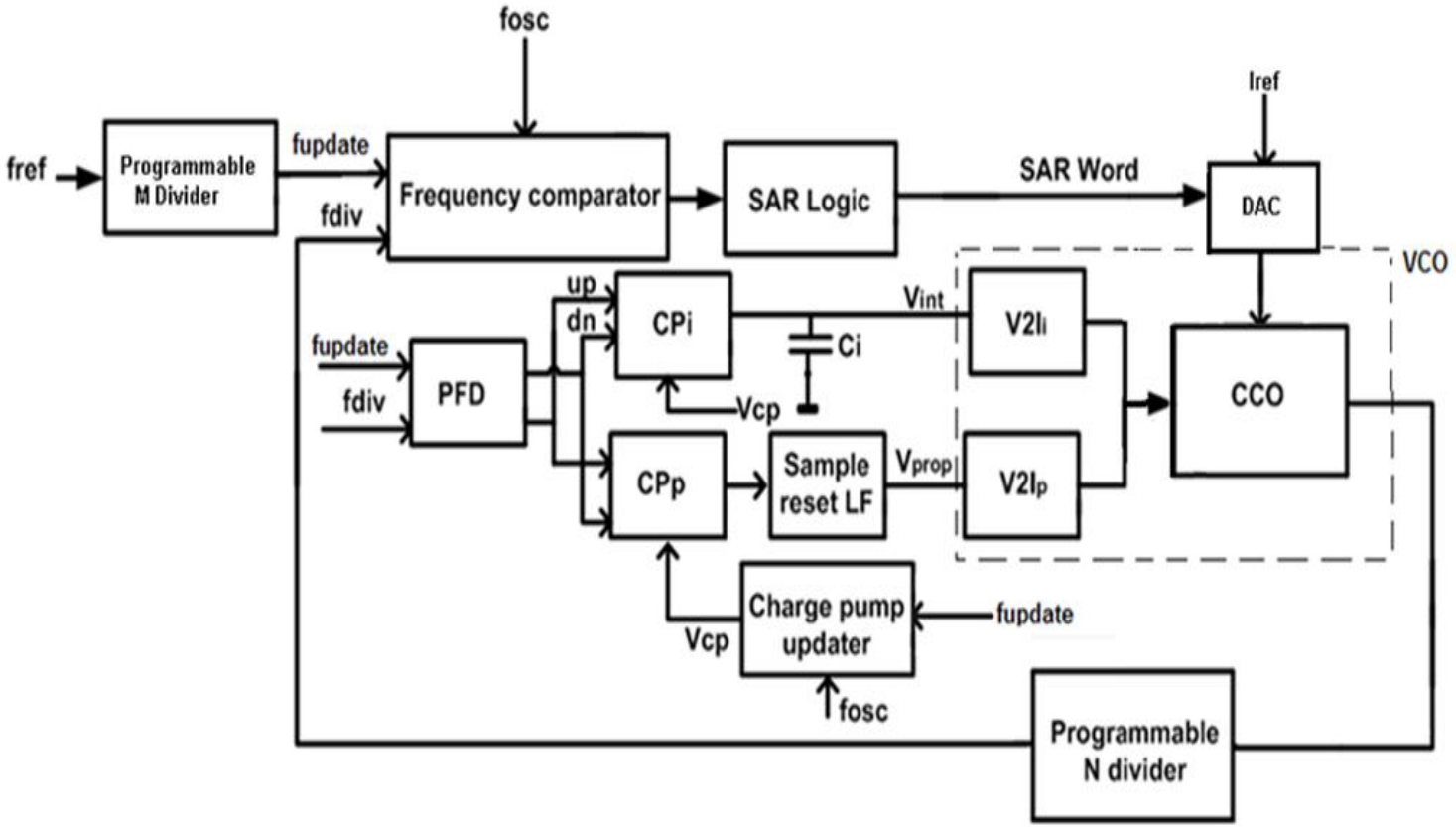

Figure 4.1: Proposed programmable adaptive bandwidth PLL architecture.

Figure 4.2 shows coarse and fine tuning steps of PLL.

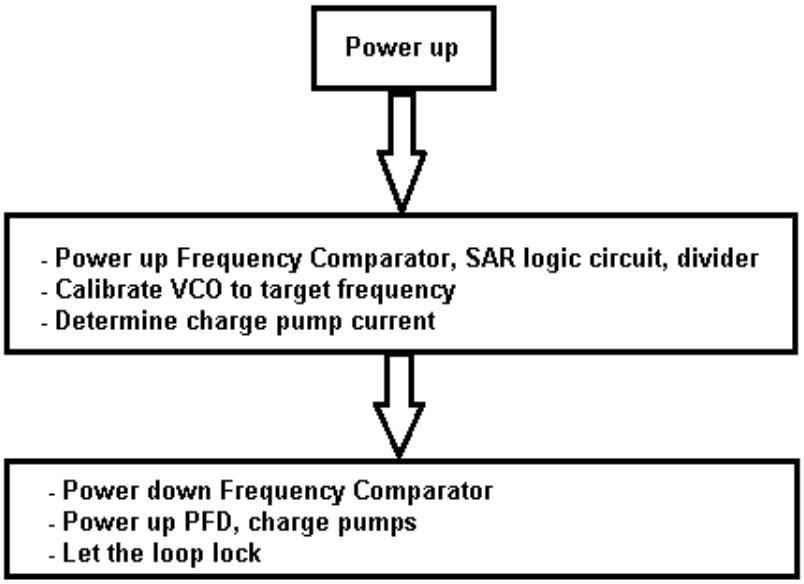

Figure 4.2: Coarse and Fine Tune steps of PLL.

4.2.1 Sample reset loop filter

In adaptive bandwidth PLLs a tracking mechanism is needed between the natural frequency, stabilizing zero and the loop update rate. In classical charge pump PLLs, there are two poles at the origin so they need a zero to stabilize the loop. There are some methods of adding a zero. One of them is adding a series resistor to loop filter capacitor. However, it creates a constant zero. Another technique of adding zero is using feed-forward method that includes two separate charge pumps to drive capacitor and resistor separately [19], but it does not provide tracking between the zero frequency and the update rate. Additionally, traditional charge pump PLLs provide narrow and high amplitude current pulses to loop filter in every update period to correct the phase difference between the reference and feedback signals [2]. These current pulses disrupt the VCO control voltage and degrade the jitter performance of the PLL. A shunt capacitor is usually added to loop filter in order to smooth VCO control voltage. However, it creates another pole that degrades the stability.

There are some sample-reset loop filter architectures and they provide tracking between the stabilizing zero and loop update rate. They can also eliminate the voltage ripples on VCO control voltage so they do not need a ripple filtering capacitor. Therefore, they provide good jitter performance without degrading the stability. In [2], a tracking mechanism is introduced between natural frequency and

zero frequency. However, it includes a large number of switches, which may degrade PLL spur performance. A simple sample-reset loop filter architecture was proposed in [20, 21]. It is shown in Figure 4.3. Note that the switches are realized with transmission gates. Before each update, C1 is reset to a reference voltage in order to remove the previous memory. This also eliminates another pole. In charging phase, phase difference between the reference and the feedback signal is sampled on C1 capacitor. It is charged to a voltage that is proportional to the update period. After sampling, the voltage on C1 is transferred to hold capacitor, C2, and S2 is opened after charge transfer has finished. This sampled data approach averages V_{prop} over the update frequency and creates staircase shaped proportional path control voltage as shown in Figure 4.4. V_{prop} determines stabilizing zero value. Since V_{prop} is proportional to the update period, the stabilizing zero becomes proportional to the update frequency. This property is very important for the designed adaptive bandwidth PLL because it provides tracking between the natural frequency and zero. This makes the damping ratio constant over a wide frequency range.

The voltage introduced on C1 capacitor is given by

$$\Delta VC1 = \Delta\Phi \frac{I_{CPP} T_{UP}}{2\pi.C1} \tag{4.1}$$

The charge on C1 is shared with C2 in transfer phase. After charge sharing, the voltage on C2 capacitor minus V_{ref}, which is the differential voltage at the input of $V2I_p$, can be given as

$$\Delta VC2(n) = \frac{C2.\Delta VC2(n-1) + C1\Delta VC1(n)}{C1+C2} \tag{4.2}$$

In z domain, transfer function can be written as in [21]

$$\frac{\Delta VC2(z)}{\Delta\Phi(z)} = \frac{I_{CPP}}{2\pi.f_{up}(C1+C2)} \frac{1}{1-\beta.z^{-1}} \tag{4.3}$$

where β is C2/(C1+C2). If we view the switched capacitor as a resistor, approximated value of the pole introduced by C2 can be written as

$$f_{pole\_C2} = \frac{f_{up}.C1}{2\pi.C2} \tag{4.4}$$

From **(4.4)**, it can be said that the pole introduced by C2 also tracks the update frequency. Therefore, it also does not threaten the stability.

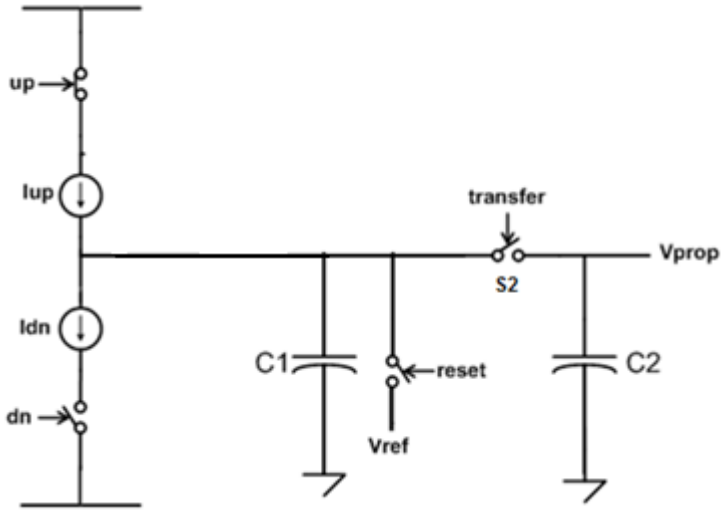

Figure 4.3: Single capacitor sample-reset proportional path architecture [20].

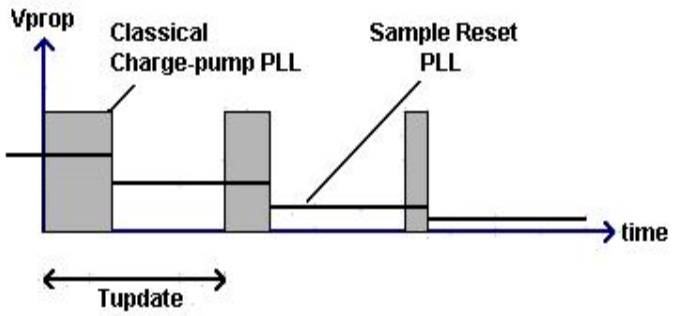

Figure 4.4: Comparison of sample reset and classical charge pump PLL proportional path voltages.

4.2.2 Charge pump

The charge pump used in both integral and proportional paths is shown in Figure 4.5. The current of charge pump is determined by the charge pump updater circuit that is discussed in charge pump updater section. NM1-NM2 and MP1-MP2 are the cascode current sources and they are biased by BIASP1-2 and BIASN1-2 bias voltages. Current of MP1-MP2 and NM1-NM2 are equal. When up is high and dn is low, PC2 and MC1 turns on and PC2 charges the output by Iup. At the same time, unity gain amplifier charges node Y to the same voltage with the output in order to prevent charge sharing after MC2 turns on. When up and dn is high, the output is tri-stated and no current flows to the output if the mismatch between the current sources is negligible. The unity gain amplifier used in charge pump is shown in Figure 4.6. It is a simple single stage differential amplifier.

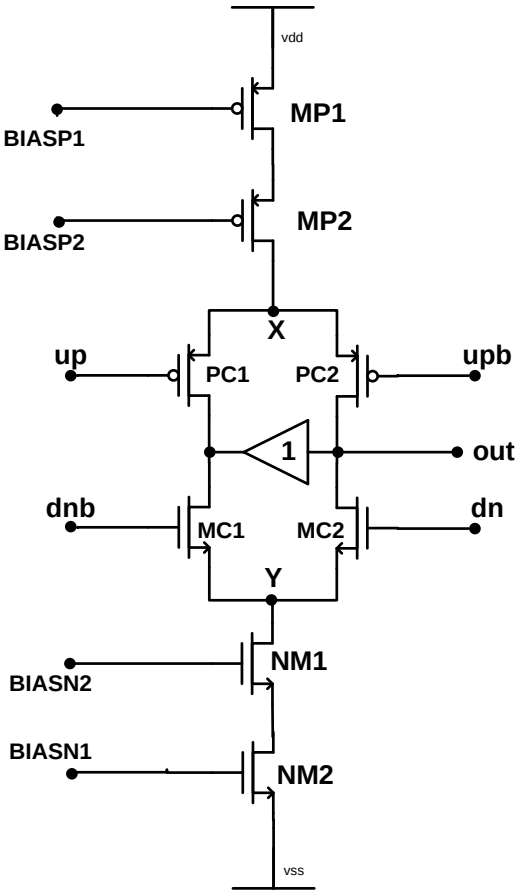

Figure 4.5: PLL Charge pump circuit with a unity gain amplifier.

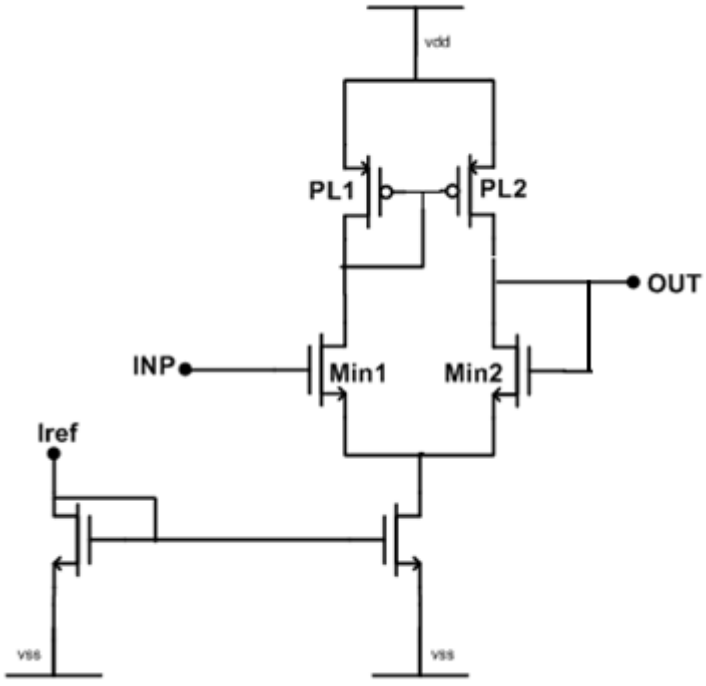

Figure 4.6: Unity gain amplifier used in charge pump.

Charge pump output current variation with the output voltage for 2µA and 100µA is shown in Figure 4.7. It is seen that charge pump can work between 0.7-1.3V range. For high output voltages, MP2-MP1 enters into triode region and up current decreases. Therefore, the mismatch between Iup and Idn currents increases. Transient response of charge pump is shown in Figure 4.8. Charge pump current determined by the charge pump updater circuit is 2µA for 1MHz update frequency and it is 100µA for 50MHz update frequency. 300pF capacitor is connected to the output in both cases. Up-down signals cause symmetric and equal voltage changes in both cases.

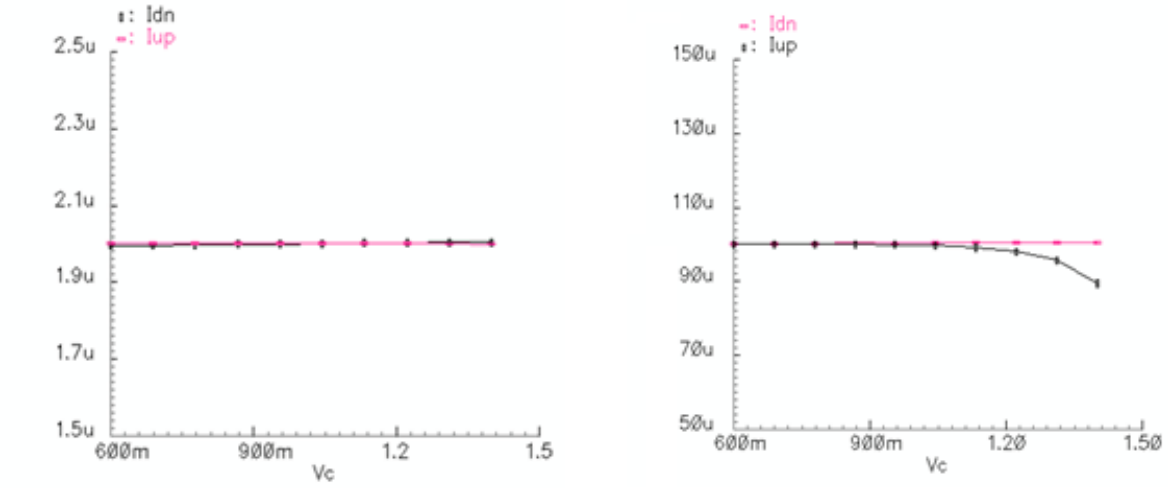

Figure 4.7: Charge pump output current change with the output voltage for I_{cp}=2µA and 100µA.

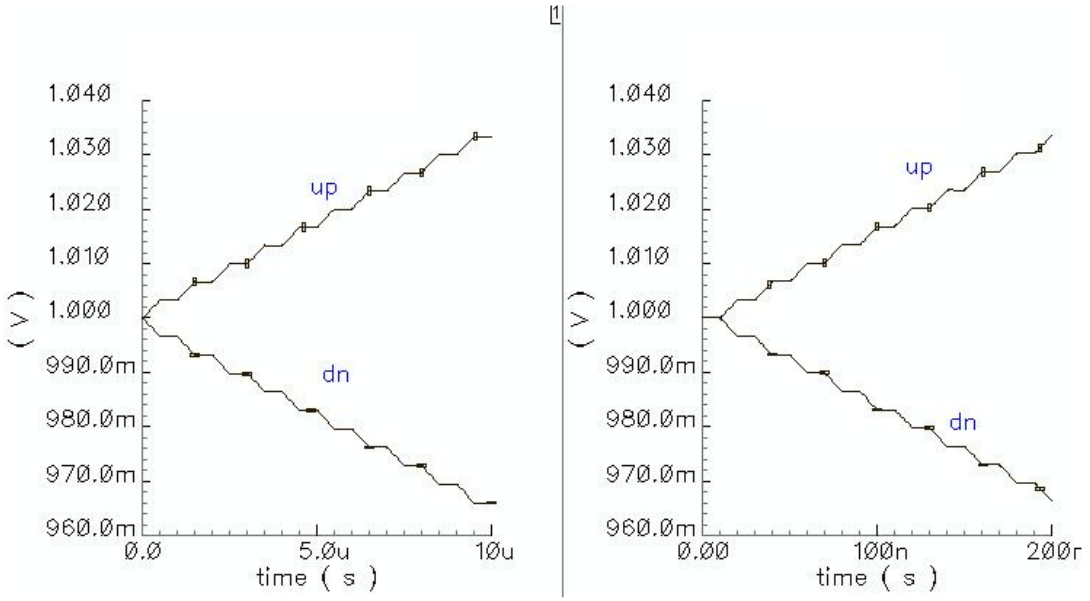

Figure 4.8: Charge pump output voltage symmetric transient change for I_{cp}=2µA and 100µA.

4.2.3 Charge pump updater circuit

Charge pump updater circuit is used to make charge pump current proportional to the update frequency. It is shown in Figure 4.9. It consists of a counter and a inverse current mirror. Counter circuit measures the update frequency by counting it using the high speed oscillator clock. Output of the counter equals to N. Inverse current mirror divides the input current by N. Divided current is used as the reference current for the charge pump circuits. As the update frequency increases, N decreases and charge pump current increases. This makes the charge pump current proportional to the update frequency. Input current of the inverse current mirror is V_{bg}/R current. High speed clock is obtained using RC ring oscillator. RC-ring oscillator frequency is given by

$$f_{OSC} = \frac{1}{2\pi . R_{eq} C_{eq}} \tag{4.5}$$

where Req and C_{eq} are the equivalent resistor and capacitor of RC oscillator. Charge pump reference current is a bandgap V_{bg}/R current and it can be written as $V_{bg}/R1$, then the output current of the inverse current mirror is given by

$$\frac{I_{bg}}{N} = \left(\frac{V_{bg}}{R1}\right)\left(\frac{f_{OSC}}{f_{up}}\right) \tag{4.6}$$

which can be re-arranged as

$$\frac{I_{bg}}{N} = V_{bg} f_{up} \frac{R_{eq}}{R1} 2\pi . C_{eq} \tag{4.7}$$

Equation **(4.7)** shows that charge pump current is proportional to the update frequency and its process and temperature dependency is very low.

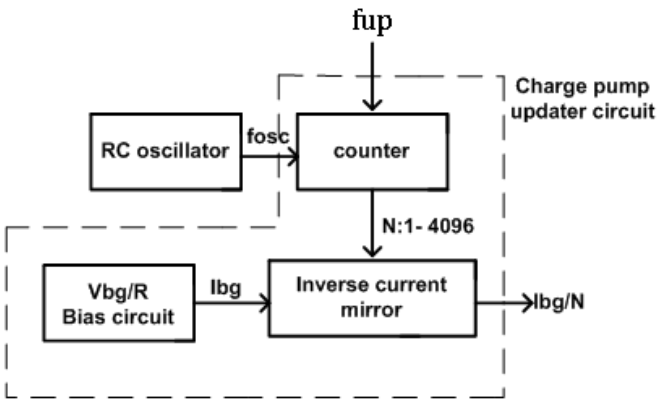

Figure 4.9: Charge pump updater circuit block diagram.

Counter value is chosen high enough in order to improve bandwidth tracking capability. However, as the N value increases, size of inverse current mirror also increases. Figure 4.10 shows simple implementation of inverse linear current mirror. This structure is simple but occupies too much area. This is because minimum and maximum device size ratio is 2048:1.

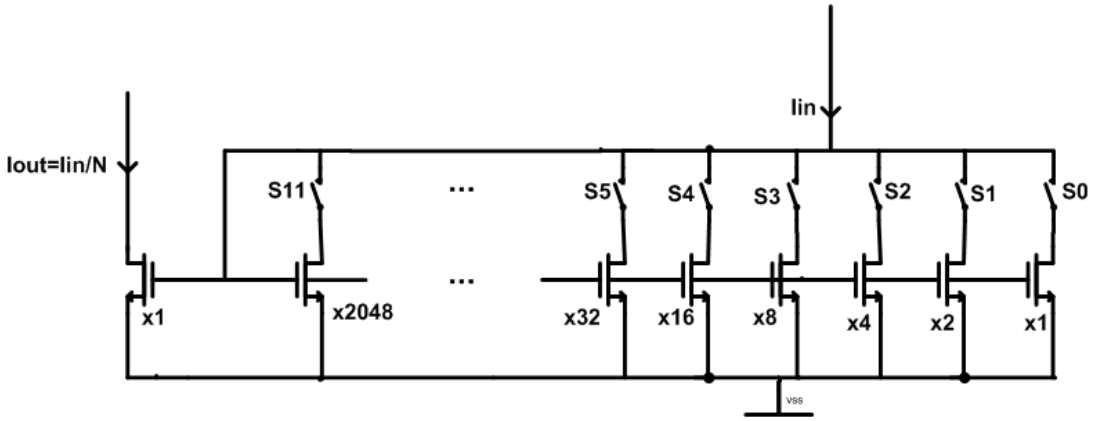

Figure 4.10: Programmable simple inverse linear current mirror.

If multistage [4] inverse linear current mirrors are used instead of conventional ones, same function can be implemented in smaller area. The circuit in Figure 4.11 is a simple implementation of multistage inverse current mirrors. It consists of two device groups with three transistors and two current mirrors. This circuit can cover a range of 0:63. We can implement a similar circuit, which covers the range of 1:4096, using the basic cell in Figure 4.11.

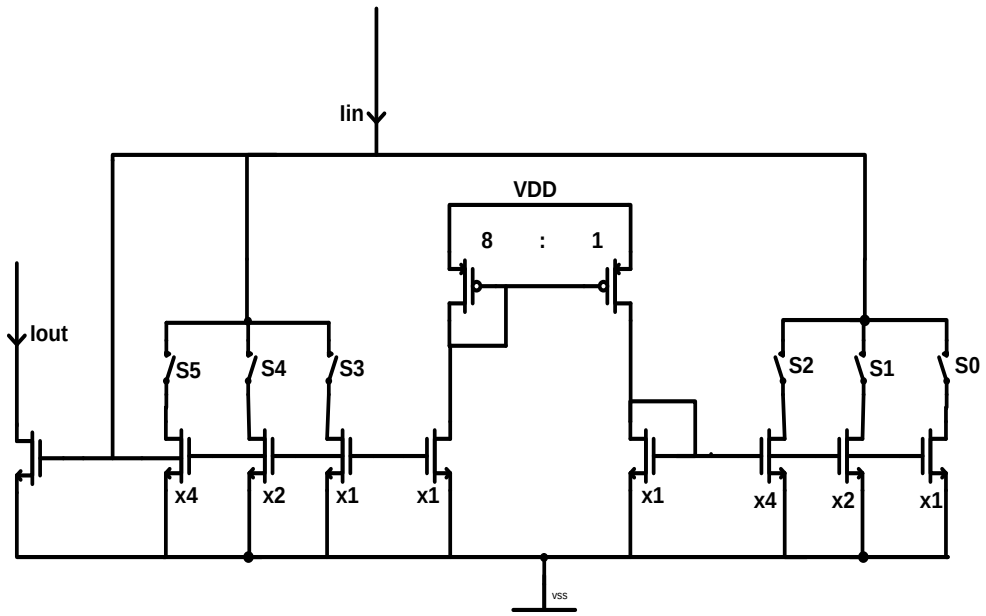

Figure 4.11: Programmable multistage inverse linear current mirror [4].

Complete implementation of multistage inverse linear current mirror, which is derived from Figure 4.11, is shown in Figure 4.12. The unused gain stages are bypassed using E2 and E3 switches for small N values. If they are not bypassed, diode connected NMOS devices may push PMOS devices intro triode region due to higher gate to source voltage.

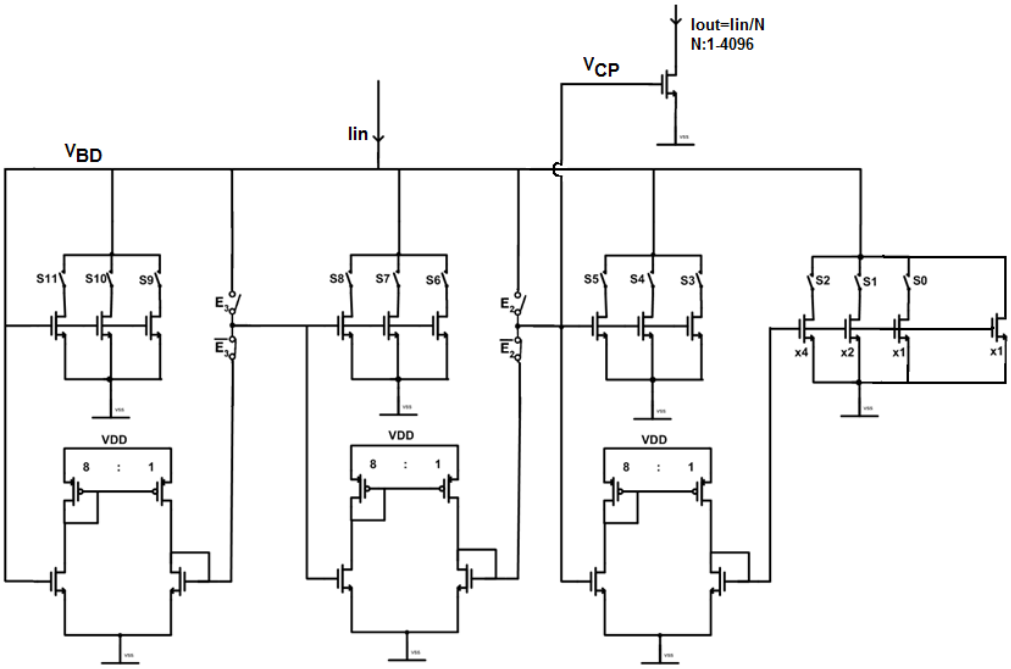

Figure 4.12: Complete multistage inverse linear current mirror [4].

Figure 4.13 shows the counter output value and charge pump current for 10MHz update frequency in typical corner.

In Table 4.1, charge pump currents for 1MHz, 10MHz and 50MHz are given. It is seen that charge pump current is proportional to the update frequency.

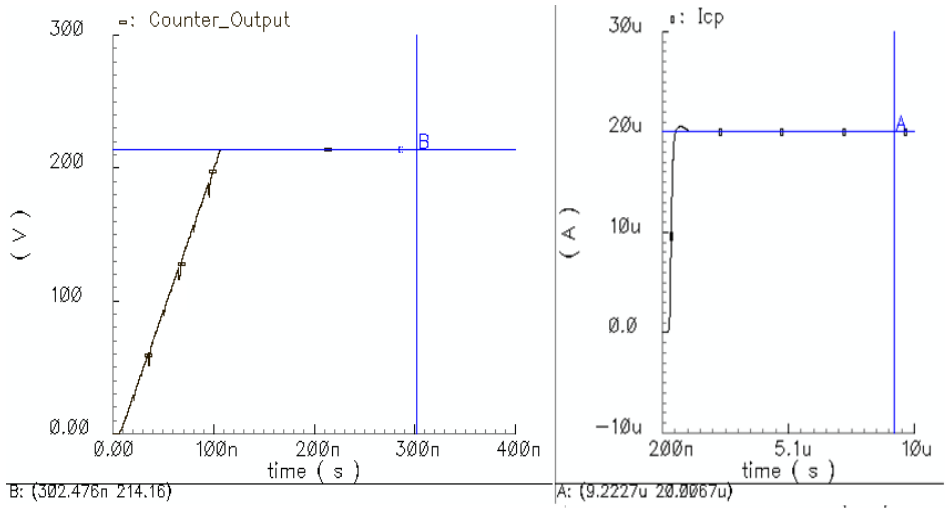

Figure 4.13: Charge pump updater counter output and charge pump current for f_{up}=10MHz.

Table 4.1 : Charge pump current variation with update frequency (f_{osc_typ} = 2149MHz).

fupdate	N	Charge pump current
1MHz (typ)	**2146**	**2µA**
10MHz (typ)	**214**	**20µA**
50MHz (typ)	**21**	**99µA**

4.2.4 Voltage to current converter design

There are two voltage to current converters: $V2I_i$ and $V2I_p$. Both of these converters are linearized G_m stages. Their input range is proportional to bandgap voltage, which has low process and temperature dependency. Their voltages to current characteristics are shown in Figure 4.14. During the coarse calibration both of Vint and Vprop is held at V_{ref} and VCO is calibrated to the target frequency as close as possible. I_{coarse} is the VCO current after the coarse calibration has finished. Integral path V2I can change VCO current between (1+B)Icoarse and (1-B)Icoarse. Proportional path V2I can change VCO current between (1+A)Icoarse and (1-A)Icoarse. Gain of $V2I_i$ and $V2I_p$ can be written as

$$\frac{\partial I_{VCO}}{\partial V_{\text{int}}} = \frac{2BI_{coarse}}{V_{range}} \quad \textbf{(4.8)}$$

$$\frac{\partial I_{VCO}}{\partial V_{prop}} = \frac{2AI_{coarse}}{V_{range}} \quad \textbf{(4.9)}$$

VCO frequency can be assumed proportional to 1/RC where R and C are equivalent resistor and capacitor of VCO. We can implement the resistor with a diode connected transistor. Since the resistance of a diode connected transistor is $1/g_m$, VCO frequency becomes proportional to g_m/C. Since g_m is proportional to the square root of the VCO current, VCO frequency becomes equal to

$$f_{VCO} = E\sqrt{I_{VCO}/C} \quad \textbf{(4.10)}$$

where E is a technology and device size dependent constant. K_{VCOI} is written as

$$K_{VCOI} = \left(\frac{\partial f_{VCO}}{\partial I_{VCO}}\right)\left(\frac{\partial I_{VCO}}{\partial V_{prop}}\right) \quad \textbf{(4.11)}$$

Using equation **(4.8)** and **(4.10)**, K_{VCOI} can be re-written as

$$K_{VCOI} = \frac{f_{VCO}B}{V_{range}} \quad \textbf{(4.12)}$$

Using the same approach for K_{VCOP}, we can write it as

$$K_{VCOP} = \frac{f_{VCO} A}{V_{range}} \tag{4.13}$$

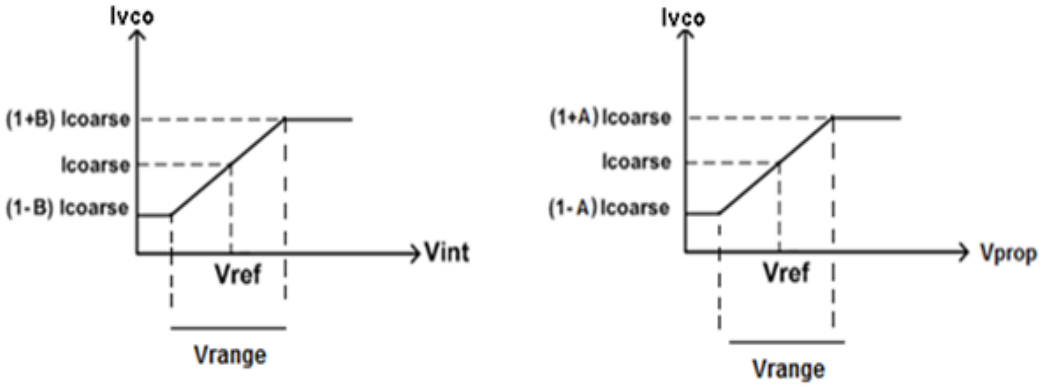

Figure 4.14: Change of VCO current with the integral and proportional loop control voltages.

Simplified schematics of these converters are shown in Figure 4.15. I_b currents are V_{bg}/R currents. V2Is are designed such that for $I_b.2R >> V_{ov,NM1\text{-}2\text{-}3\text{-}4}$, linear input range of V2Is become process and temperature independent.

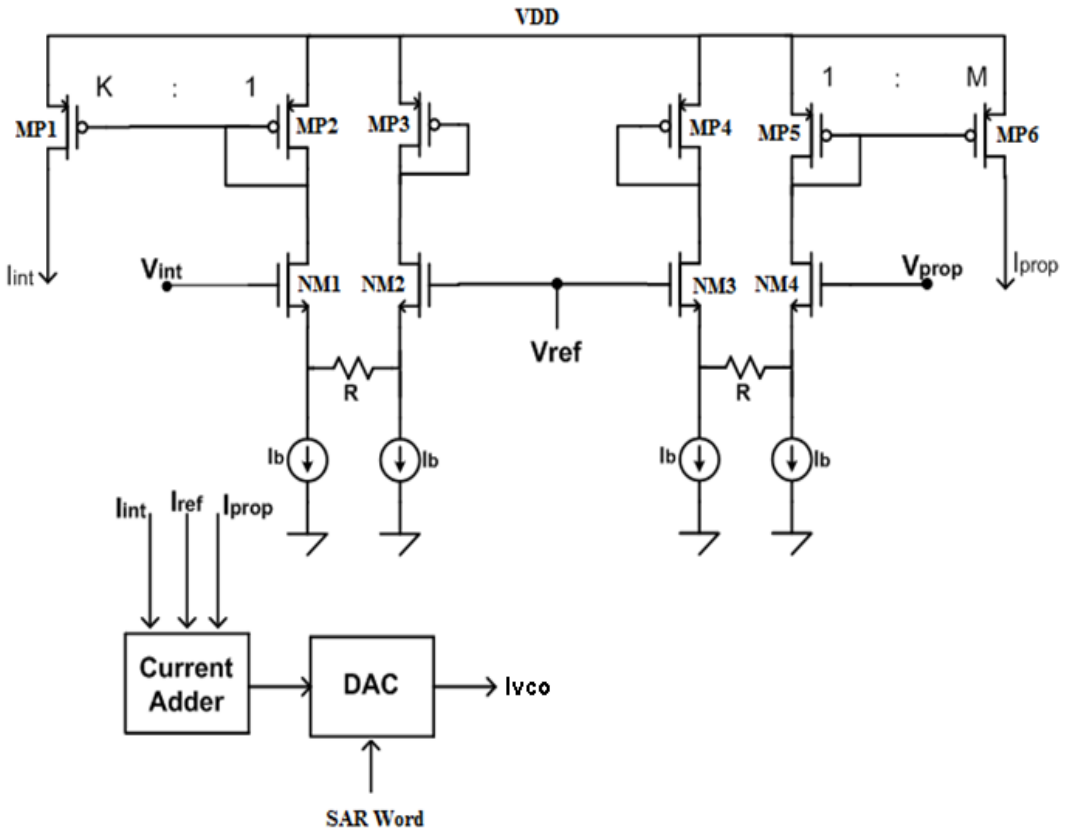

Figure 4.15: Simplified schematic of integral and proportional loop V2Is.

4.2.5 VCO design

Ring oscillators are widely used due to their simplicity and wide tuning range. They also occupy very small area compared to LC oscillators. However, LC oscillators are preferred if the phase noise and speed specifications cannot be met by the ring oscillators.

Ring oscillators consist of delay buffers. Delay of the buffer stages are affected by supply and substrate noise considerably. The change in delay increases period jitter of PLL. Therefore, differential buffers are usually preferred due to their better supply and substrate noise suppression. Figure 4.16 shows simple differential buffer with adjustable resistor. Buffer delay is determined by the effective resistance of the loads and the equivalent capacitor at the output.

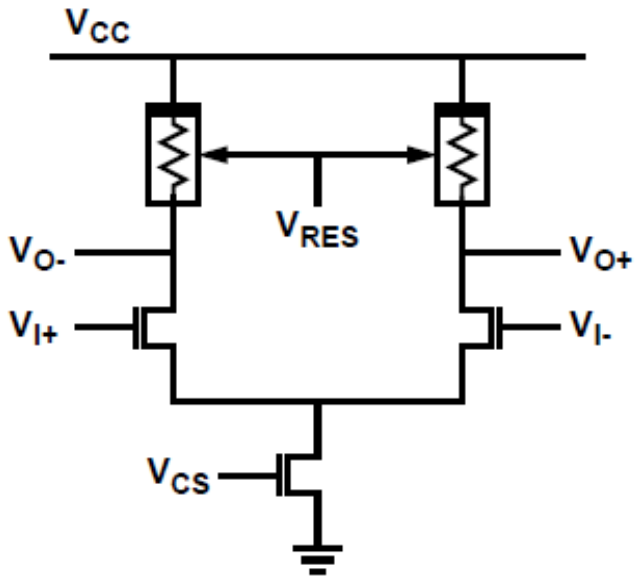

Figure 4.16: Simple differential buffer stage [22].

Figure 4.17 shows MOS realization of symmetric loads. Symmetric loads consist of two equally sized PMOS devices. One of the PMOS devices is diode connected and gate of other device is biased by the control voltage. I-V characteristics of the symmetric load are shown in Figure 4.18 for two different control voltages. Resistance of the load is changed with the control voltage in order to adjust the buffer delay. It is seen that loads are symmetric around half of the control voltage. The symmetry of the incremental resistance around the midpoint provides good supply noise suppression. If the incremental resistance is not equal to each other, the noise at V_{CC} will be coupled to the output nodes and this will cause jitter.

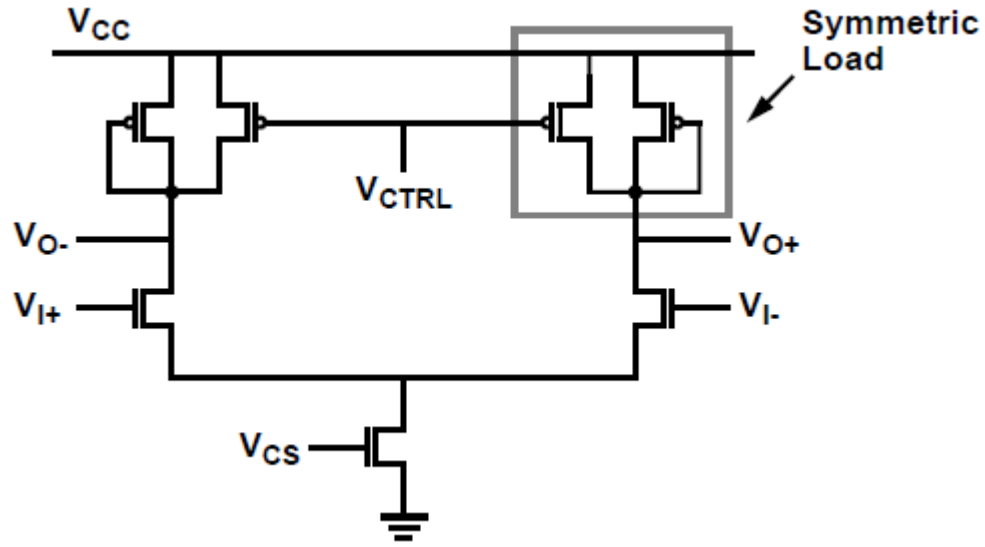

Figure 4.17: Schematic of a differential pair with symmetric loads [22].

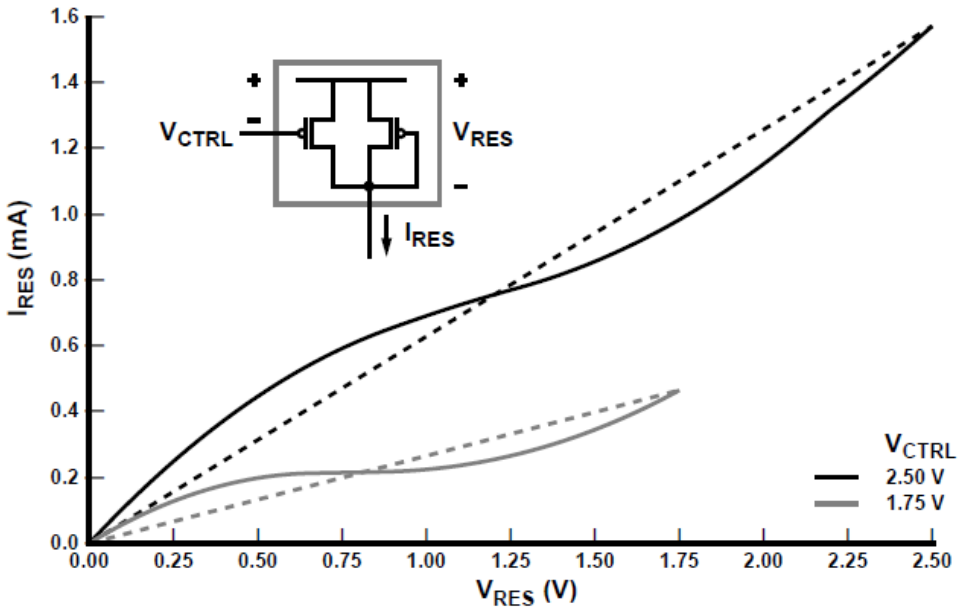

Figure 4.18: I-V characteristics of symmetric load [22].

We need special biasing circuits in order to keep the symmetry for different control voltages. When the current is fully steered to one side, lower limit of the output voltage must be limited to V_{CC}-V_{CTRL}. The circuit in Figure 4.19 shows the delay buffer with the biasing circuit, which provides symmetric load condition. The transistors PM1-PM2-PM3-PM4-PM5 are equally sized. Current of the diode connected PM1 transistor is half of the tail current so that when the tail current is fully steered to one side, output voltage of that side becomes V_{CC}-V_{CTRL}. Since the output voltage changes between V_{CC} and V_{CC}-V_{CTRL}, output swing is V_{CTRL}.

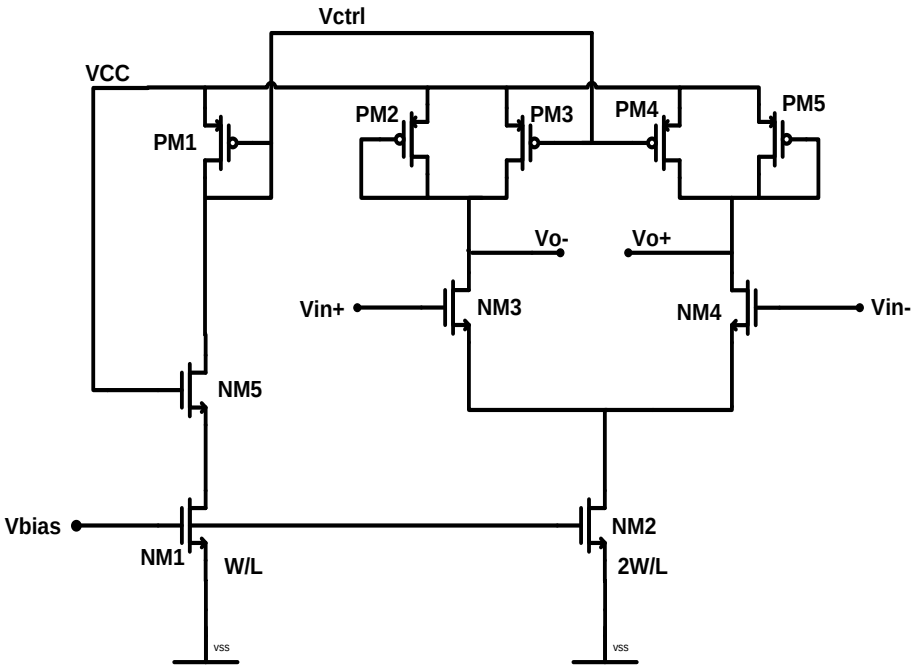

Figure 4.19: Schematic of delay buffer with biasing structure.

VCO bias block is shown in Figure 4.20. The current I_{vco} is used to generate the bias voltage of delay buffers.

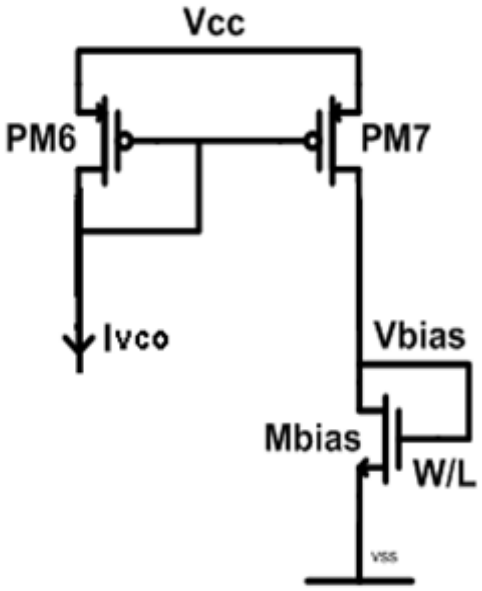

Figure 4.20: VCO bias block.

A VCO buffer is needed to isolate VCO from loading capacitance and metal routing. Figure 4.21 shows designed VCO buffer. It is a simple resistive load differential pair with output common mode supply shifting resistor, R_{cm}. Since VCO buffer drives another CML buffer, VCO buffer outputs can be shifted down with Rcm so that the input transistors of the driven stage do not enter into triode region.

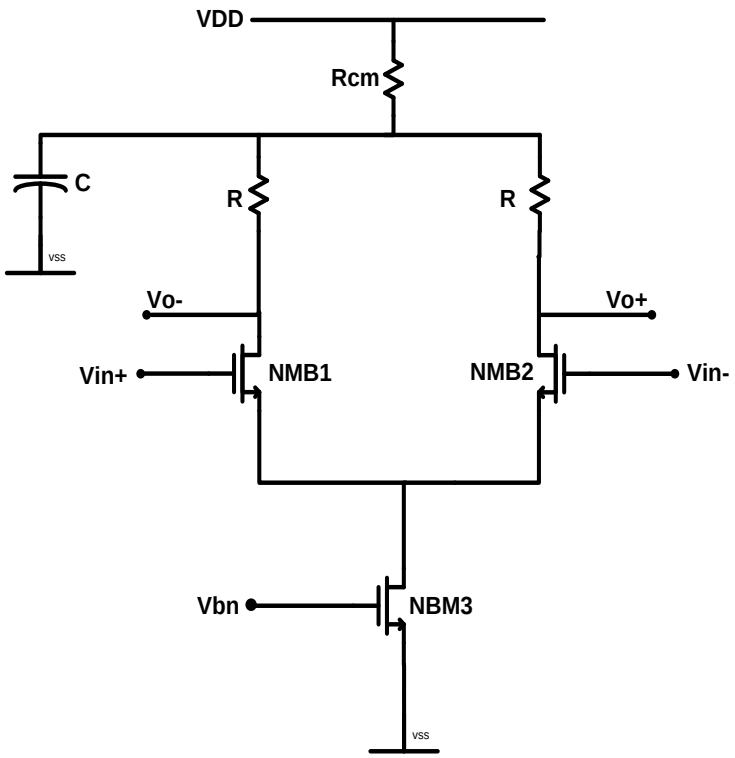

Figure 4.21: VCO Buffer.

VCO block diagram with bias block and VCO buffer is shown in Figure 4.22. 50fF loading capacitance was connected to the output of buffer. Figure 4.23 shows input and output voltage of VCO buffer.

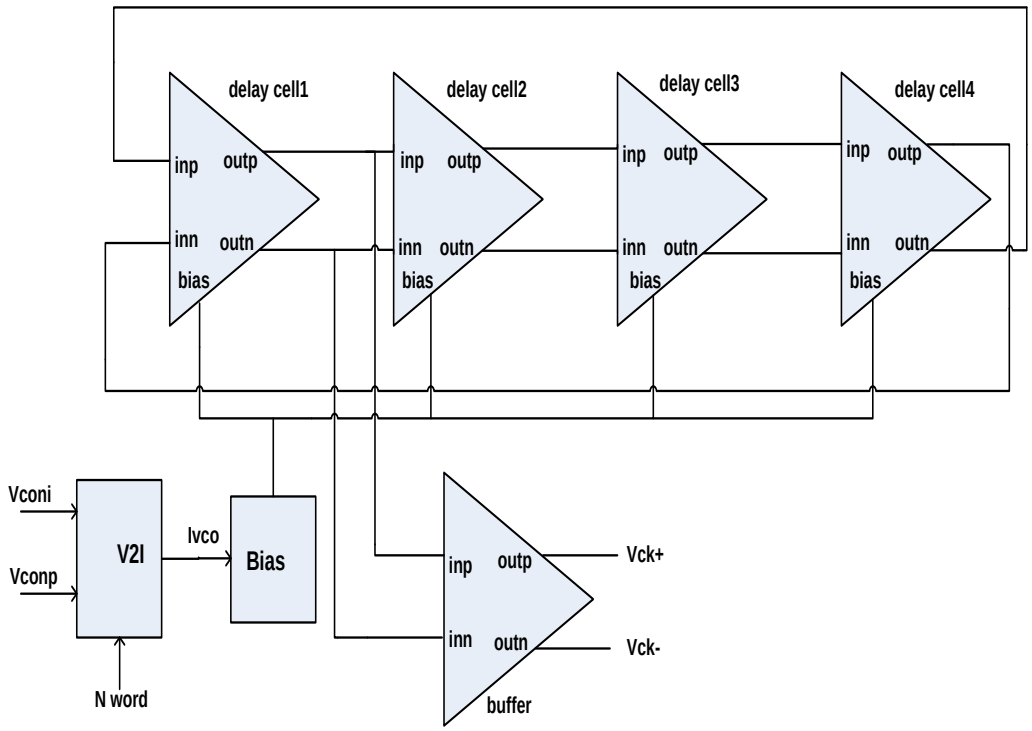

Figure 4.22: Overall VCO block diagram.

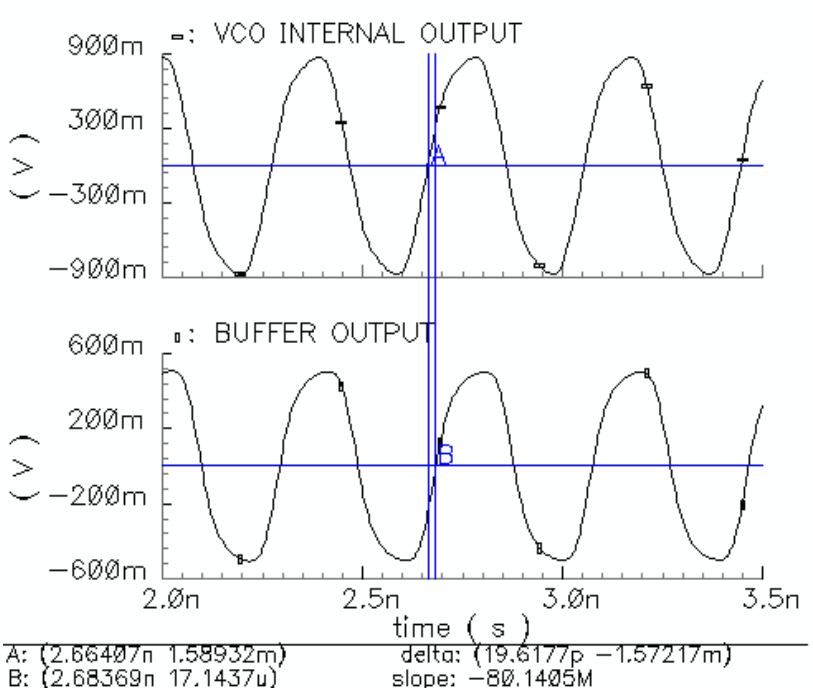

Figure 4.23: VCO internal node and buffer output voltage at 2.5GHz.

4.2.6 Programmable divider

In this work, both of input divider N and feedback divider M are programmable dividers. Programmable divider circuit consists of cascaded 2/3 divider cells. Basic programmable divider architecture is shown in Figure 4.24. This circuit is able to divide from 2^2 to $2^{(2+1)}$ -1. The used 2/3 divider cell is shown in Figure 4.25. It consists of 4 D-latch and 3 AND gates. The circuit divides by 2 unless modin and prog inputs are both high. If modin and prog inputs are both high, the circuit swallows one period and divides by three. It can swallow only one period in a division cycle. Input period of each cell is added to the output period as an extra period during division by 3. Therefore, output period is written as below:

$$T_{out} = Tin.(2^n + 2^{n-1}.p_{n-1} + \ldots + 2.p_1 + p_0) \qquad \textbf{(4.14)}$$

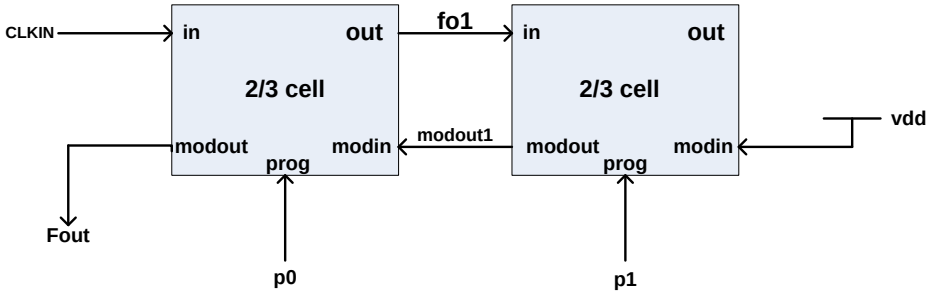

Figure 4.24: Basic programmable divider architecture.

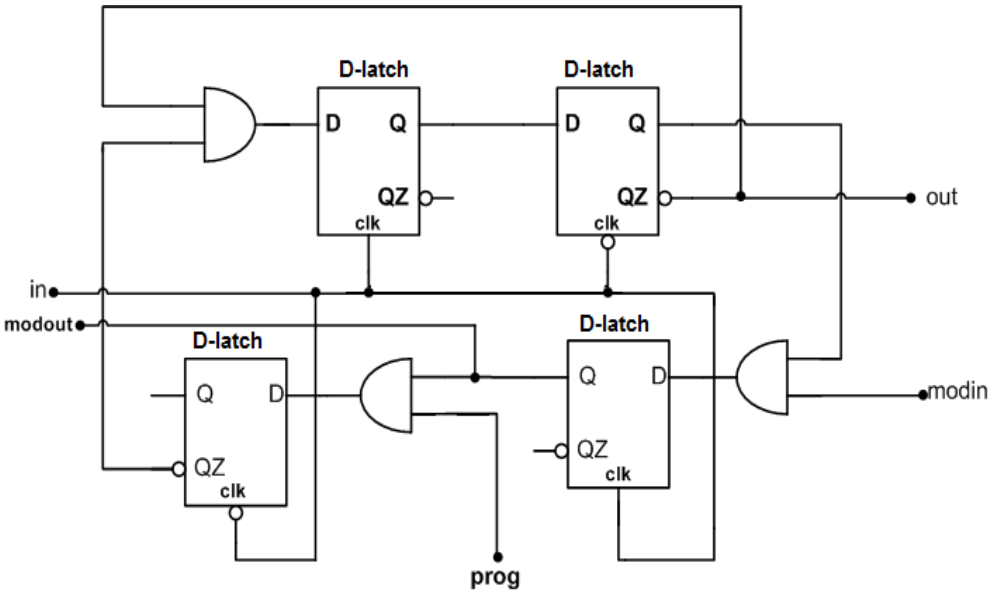

Figure 4.25: 2/3 divider cell [23].

Minimum division ratio of the circuit shown in Figure 4.24 is 2^2. If lower division ratio is needed, this can be achieved using additional control circuitry as shown in Figure 4.26. If modin input of one cell is set to 1, the previous cells do not affect the division ratio. Therefore, lower division ratio is obtained. We designed the circuit such that it divides between 5 and 2500. This requires 11 stages. The first stage runs at highest frequency and the other stages are run at 1/2, 1/4, … rates. Therefore, speed of the first stage is maximized and other stages are scaled according to their speed. First 2/3 divider cell current is 600µA, current of other cells are scaled such as 300µA, 150µA, 75µA, 35µA, 15µA, 10µA, 10µA, ..., 10µA.

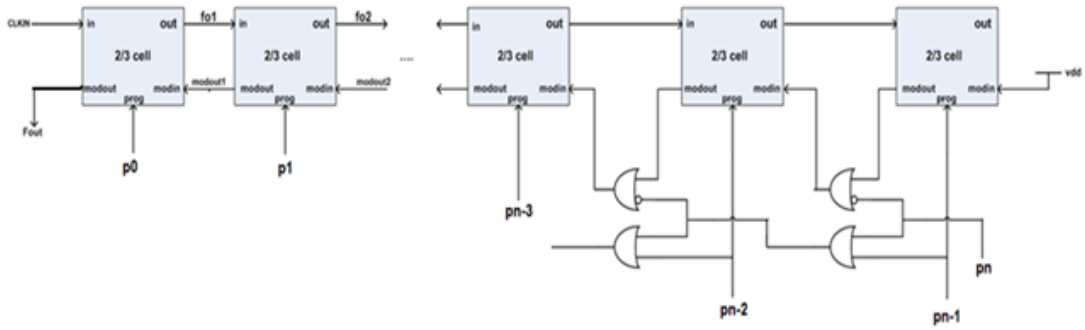

Figure 4.26: Complete divider circuit with extended division range [23].

Programmable divider must operate up to 2.5GHz. Taking overshoots into account it must operate up to 3GHz in slow-hot corner. This can be achieved with CML gates. D-latch circuit is implemented with the circuit shown in Figure 4.27. Output tracks the input when CK is high.

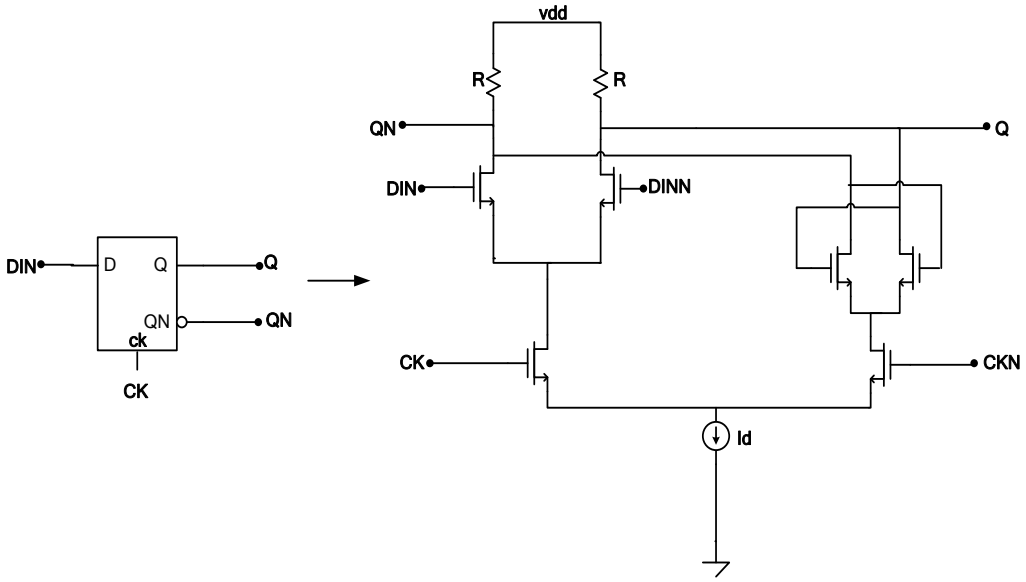

Figure 4.27: Implementation of D-Latch circuit.

The AND gate combined with D-latch circuit shown in Figure 4.25, is implemented with the circuit in Figure 4.28.

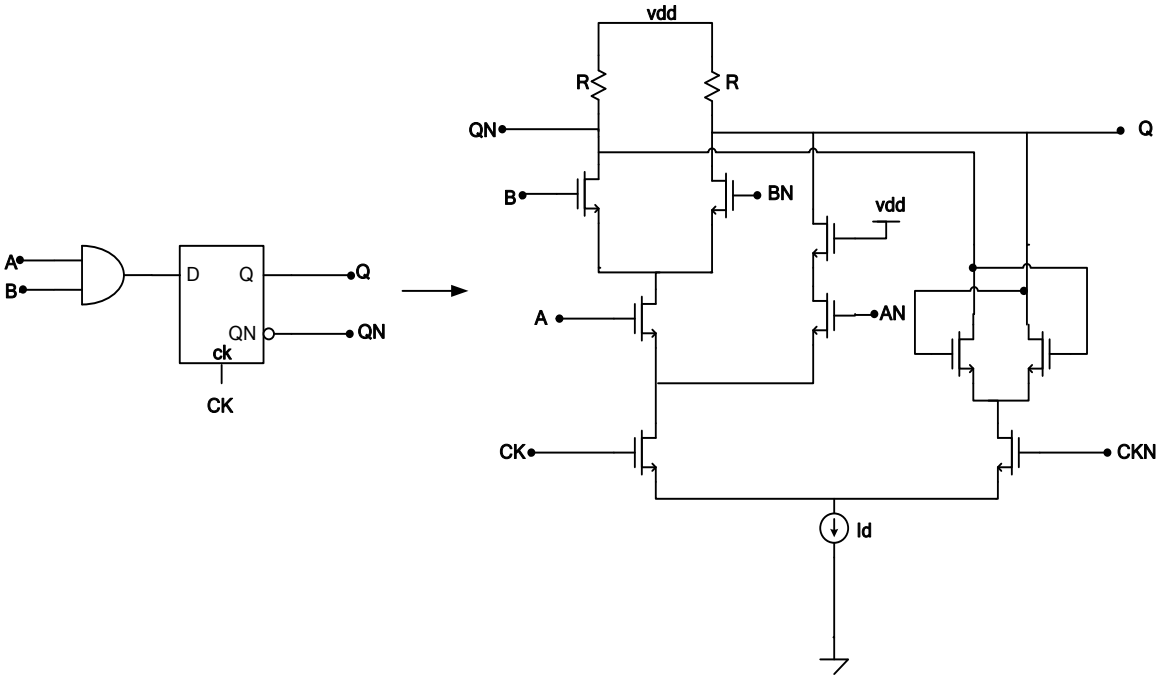

Figure 4.28: Implementation of AND gate combined with D-latch function.

CML output is converted to CMOS output using the CML to CMOS converter shown in Figure 4.29. Output of CML to CMOS converter is a narrow pulse. Its pulse width is stretched with the pulse stretcher circuit shown in Figure 4.30. Flip flop complementary output is used to reset the flip-flop over a delayed path. A schmitt trigger circuit is used in order to prevent the noise disturbance on the reset pulse. It is shown in Figure 4.31.

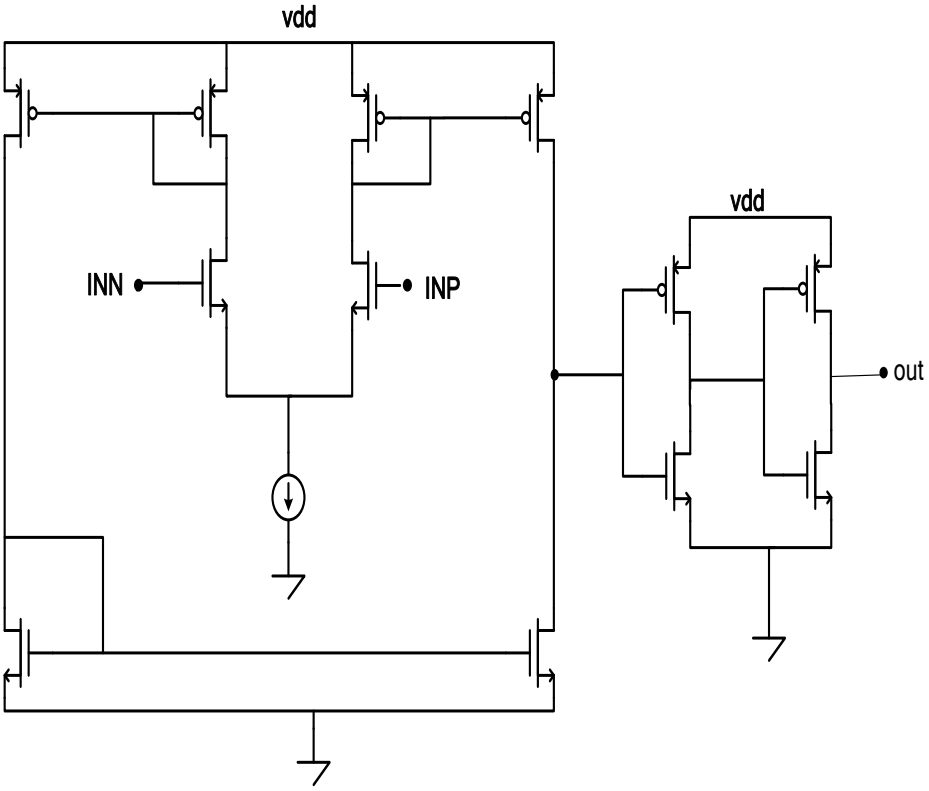

Figure 4.29: CML to CMOS converter.

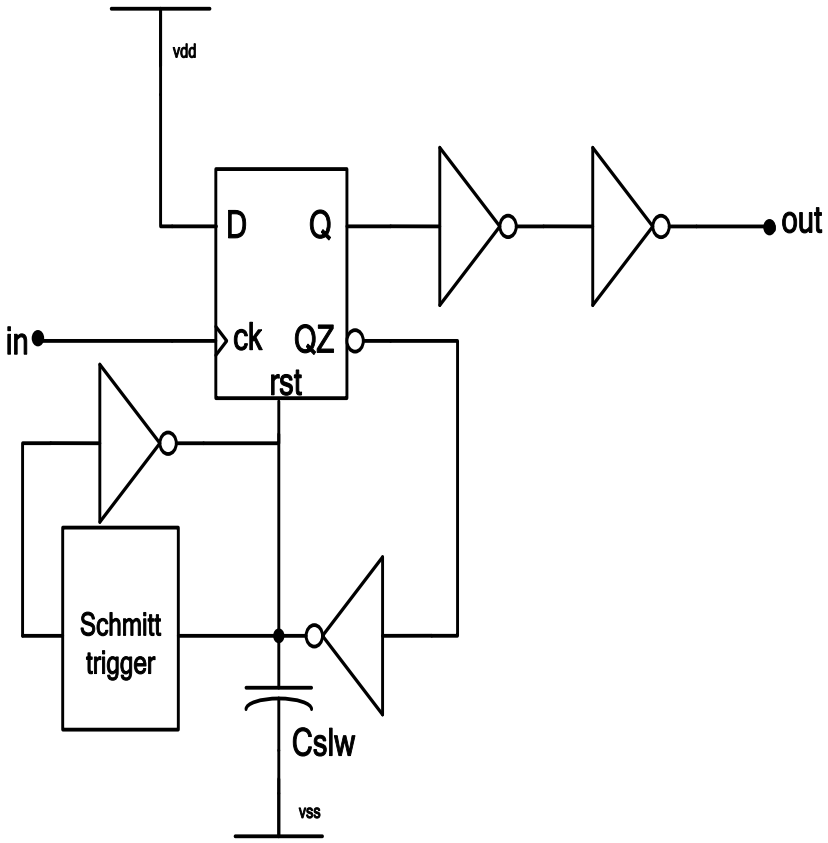

Figure 4.30: Simple pulse stretcher circuit.

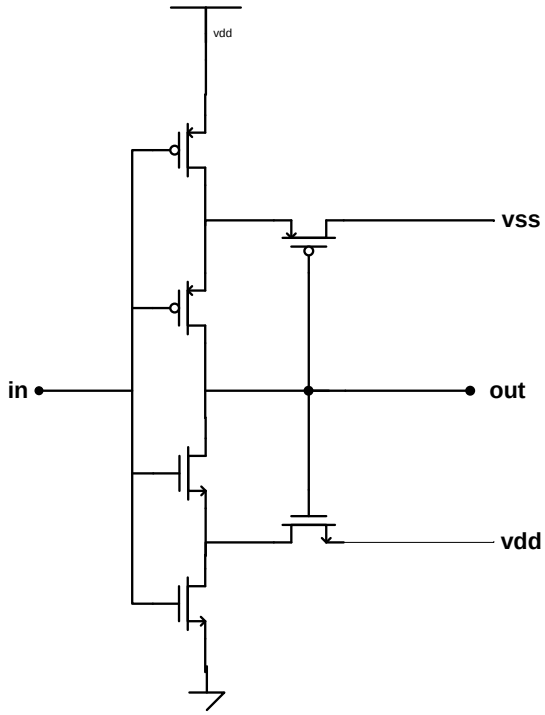

Figure 4.31: Schmitt trigger circuit.

In Figure 4.32, output of pulse stretcher, CML to CMOS converter and divider are shown for f_{in} = 2.5GHz and Ndiv = 50.

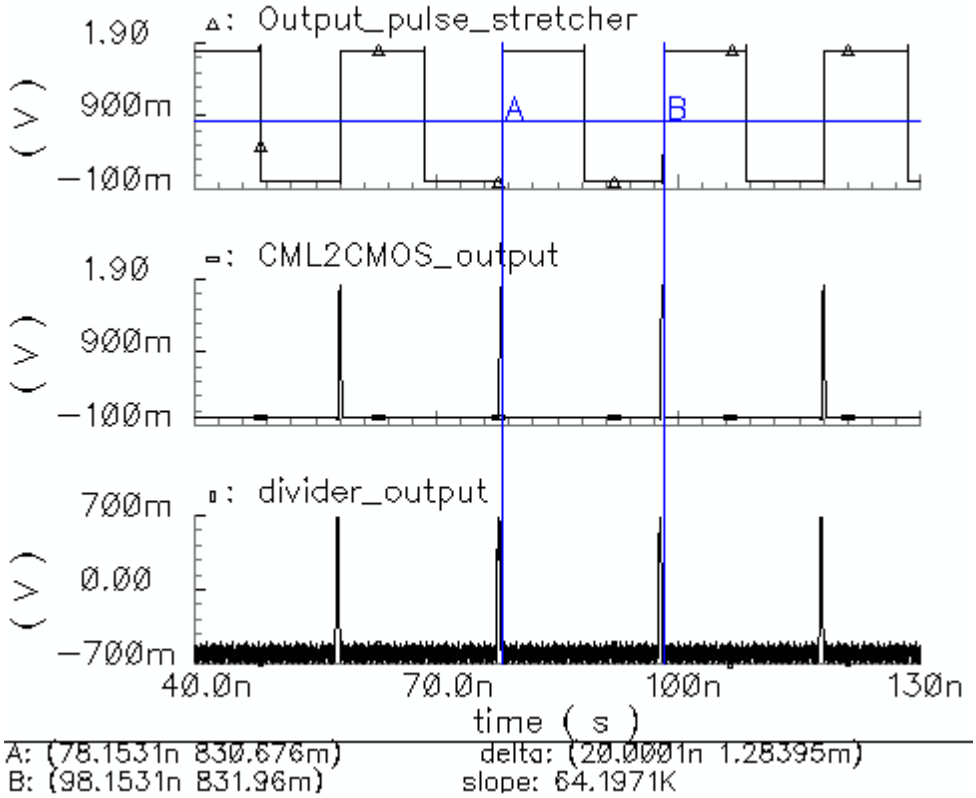

Figure 4.32: Output of CML divider, CML to CMOS converter and pulse stretcher circuit (fin = 2.5GHz and Ndiv = 50).

4.2.7 Calculation of PLL loop dynamics

Figure 4.33 shows small signal model of sample-reset charge pump PLL. It is used to calculate the loop dynamics of the proposed PLL.

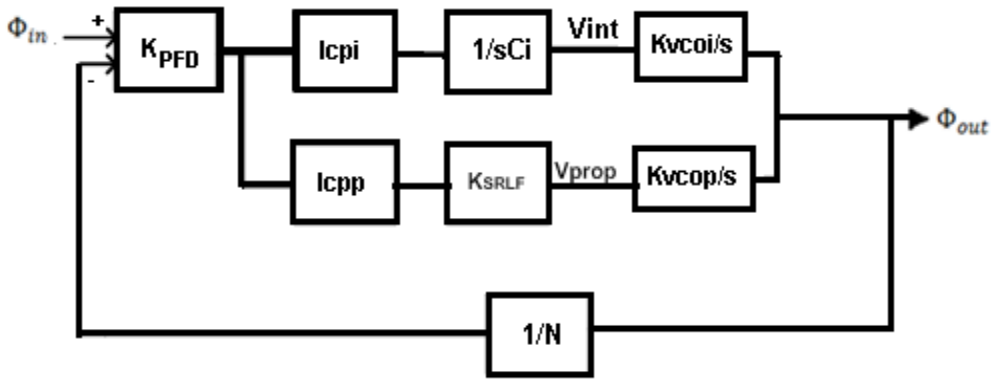

Figure 4.33: Small signal model of PLL.

The open loop gain transfer function is

$$F(s)=\left(\frac{I_{CPI}}{2\pi}\frac{K_{VCOi}}{s}\frac{1}{sC_i}+\frac{I_{CPP}}{2\pi}K_{SRLF}\frac{K_{VCOP}}{s}\right) \quad \textbf{(4.15)}$$

where K_{SRLF} is the gain from the output of proportional charge pump to the input of V2Ip. Using the equation **(4.3)**, for C1>>C2 and loop bandwidth << f_{up}, K_{SRLF} can be approximated to

$$K_{SRLF}=\frac{1}{f_{up}.C1} \quad \textbf{(4.16)}$$

Using the closed loop transfer function below

$$H(s)=\frac{F(s)}{1+\frac{F(s)}{N}} \quad \textbf{(4.17)}$$

and inserting K_{SRLF}, K_{VCOI}, K_{VCOP}, I_{CPI} and I_{CPP} equations into **(4.15)** and writing f_{vco} as f_{up}.N, natural frequency and zero frequency are obtained as

$$\omega_N=\sqrt{\frac{I_{CPI}K_{VCOI}}{2\pi NC_i}}=f_{up}\sqrt{\frac{V_{bg}}{V_{range}}\frac{C_{eq}}{C_i}\frac{R_{eq}}{R1}B} \quad \textbf{(4.18)}$$

$$\omega_Z=f_{up}\frac{I_{CPI}}{I_{CPP}}\frac{C1}{C_i}\frac{K_{VCOI}}{K_{VCOP}}=f_{up}.k.\frac{C1}{C_i}\frac{B}{A} \quad \textbf{(4.19)}$$

where k is the ratio of the integral and proportional path charge pump currents. It is seen from **(4.18)** and **(4.19)** that this PLL has an adaptive bandwidth and the zero frequency also tracks the update frequency. Therefore, the damping factor is kept constant over a wide frequency range.

5. SIMULATION RESULTS

In this section, top level simulation results of the proposed PLL will be given. The section starts with the system parameters and system specifications of the proposed PLL. After that PLL operation temperature ranges are checked to verify that re-calibration is not needed after calibrating in one sub-range if the temperature changes marginally. Next, locking behaviour of the proposed PLL is given for different conditions. Finally, an input spread tracking application is given for the proposed PLL and a conventional PLL. VCO phase noise simulation results for different PLL bandwidths are also given in the final section.

5.1 PLL System Parameters and System Specifications

PLL system parameters are given in Table 5.1. Note that charge pump currents are changed between 2 µA-100 µA by the system according to update frequency. Update frequency changes between 1 MHz to 50 MHz. VCO gains are chosen equal for both integral and proportional paths. VCO gain is 320 MHz/V when VCO frequency is 500 MHz and it is 1220 MHz/V when VCO frequency is 2500 MHz.

Table 5.1: PLL system parameters (typical values).

Loop update rate	1 MHz-50 MHz
Integral capacitor, C_i	300 pF
Sampling capacitor, C1	2.5 pF
Hold capacitor, C2	0.5 pF
Integral loop charge pump current range, I_{cpi}	2 µA-100 µA
Proportional loop charge pump current range, I_{cpp}	2 µA-100 µA
VCO integral path gain, K_{vcoi}	320 MHz/V-1220 MHz/V
VCO proportional path gain, K_{vcop}	320 MHz/V-1220 MHz/V
N divider ratio	10-2500

Table 5.2: PLL system specifications.

Update rate	1 MHz - 50 MHz
VCO operating range	500 MHz-2500 MHz
PLL bandwidth range @500MHz output frequency	86 kHz - 4.9 MHz
PLL bandwidth range @2500MHz output frequency	65 kHz - 3.64 MHz
Phase Margin	86-79°
Closed loop peaking	0.12-0.16 dB

System specifications of PLL in typical corner are summarized in Table 5.2. Change of PLL bandwidth with the update frequency at different output frequencies is shown in Figure 5.1.

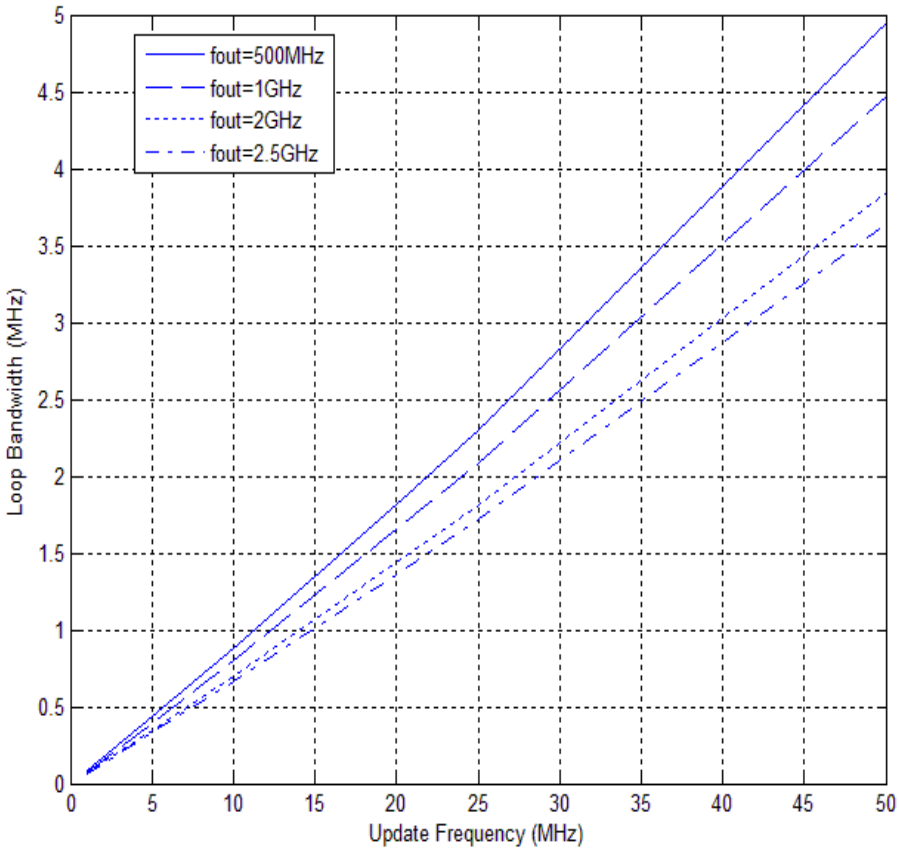

Figure 5.1: Change of PLL bandwidth with update frequency at different output frequencies (typical).

Change of phase margin and closed loop peaking of PLL at different output frequencies are shown in Figure 5.2 and Figure 5.3 respectively.

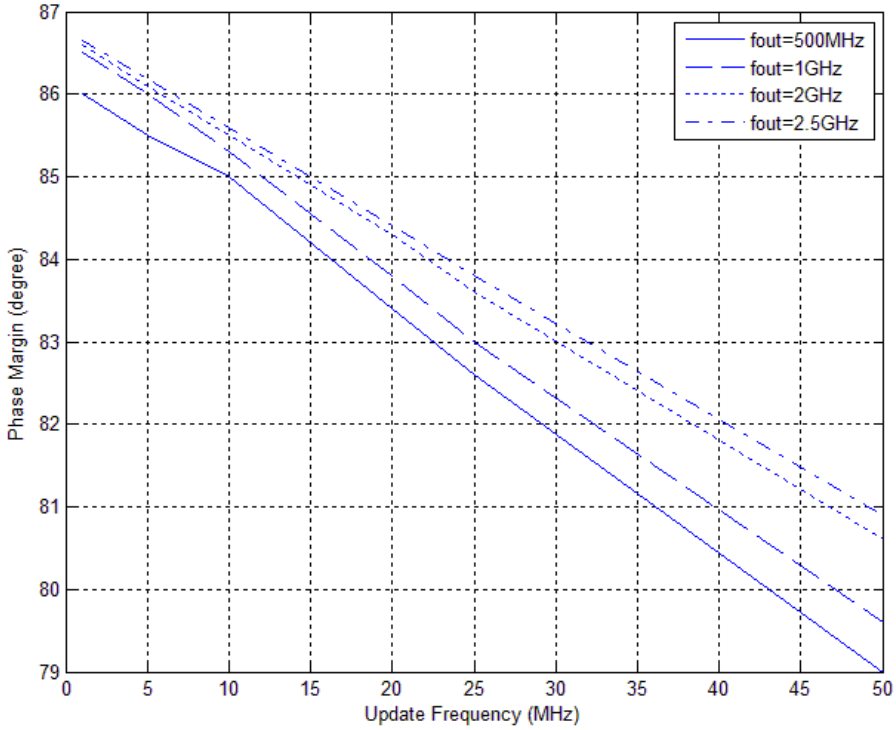

Figure 5.2: Change of PLL phase margin with update frequency at different output frequencies (typical).

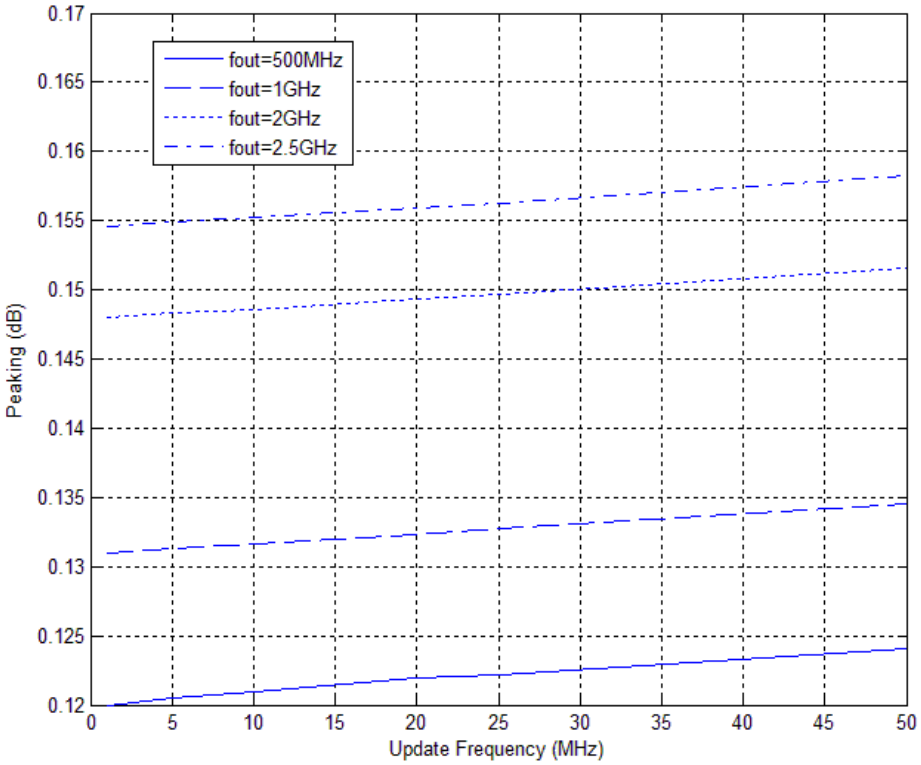

Figure 5.3: Change of PLL closed loop peaking with update frequency at different output frequencies (typical).

Change of PLL loop bandwidth, phase margin and closed loop peaking with the update frequency at 500 MHz output frequency over typical, slow and fast corners are shown in Figure 5.4, Figure 5.5 and Figure 5.6 respectively.

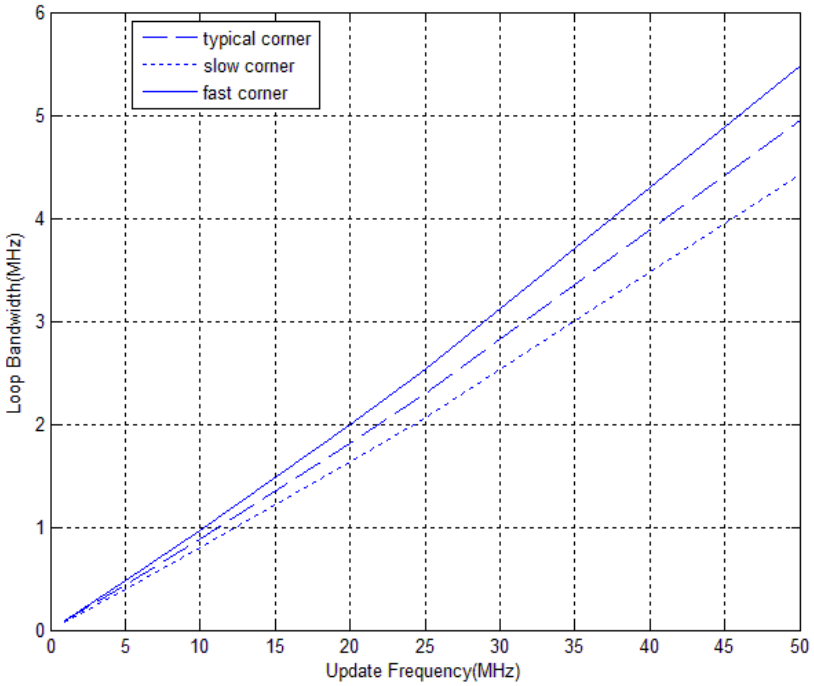

Figure 5.4: Variation of PLL loop bandwidth in different process corners (f_{out} = 500 MHz).

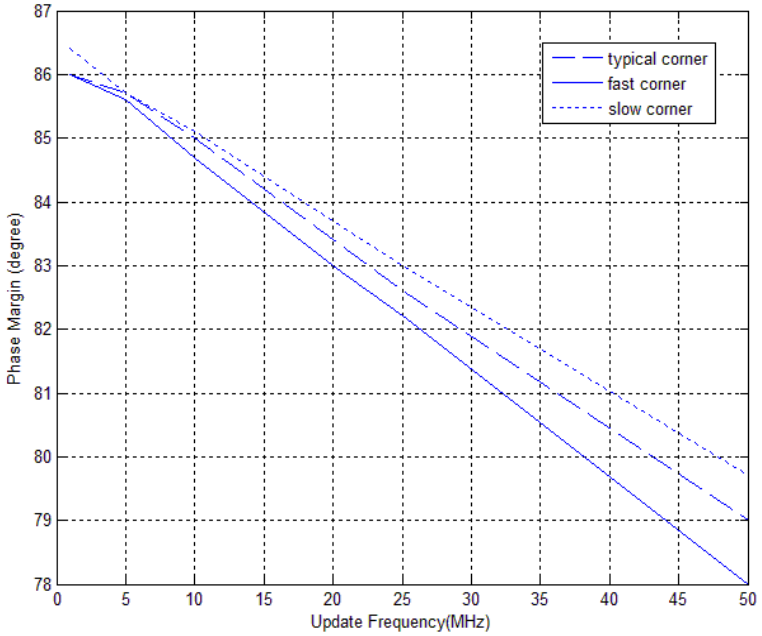

Figure 5.5: Variation of PLL phase margin in different process corners (f_{out} = 500 MHz).

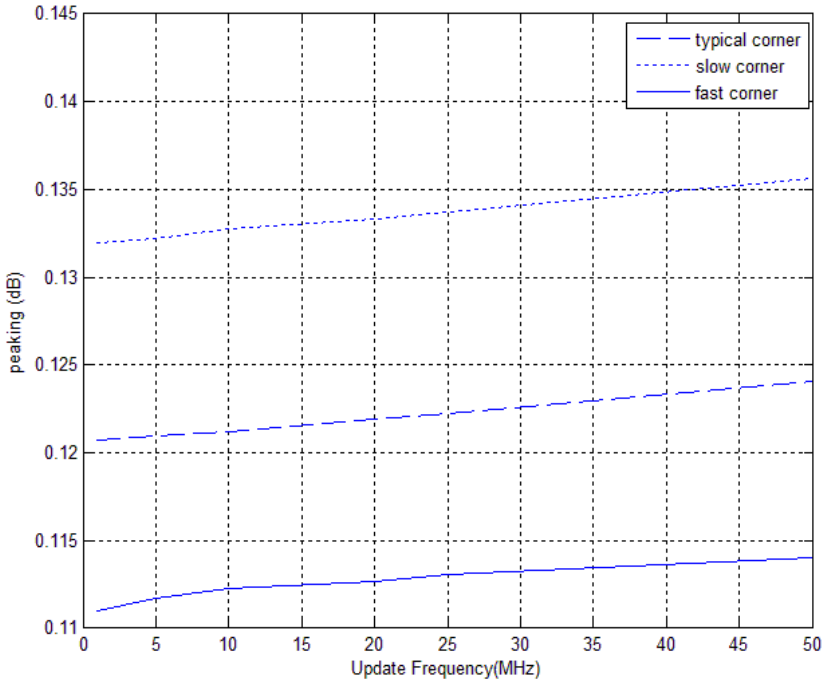

Figure 5.6: Variation of PLL closed loop peaking in different process corners (f_{out} = 500 MHz).

Change of PLL loop bandwidth, phase margin and closed loop peaking with the update frequency at 2500 MHz output frequency over typical, slow and fast corners are shown in Figure 5.7, Figure 5.8 and Figure 5.9 respectively.

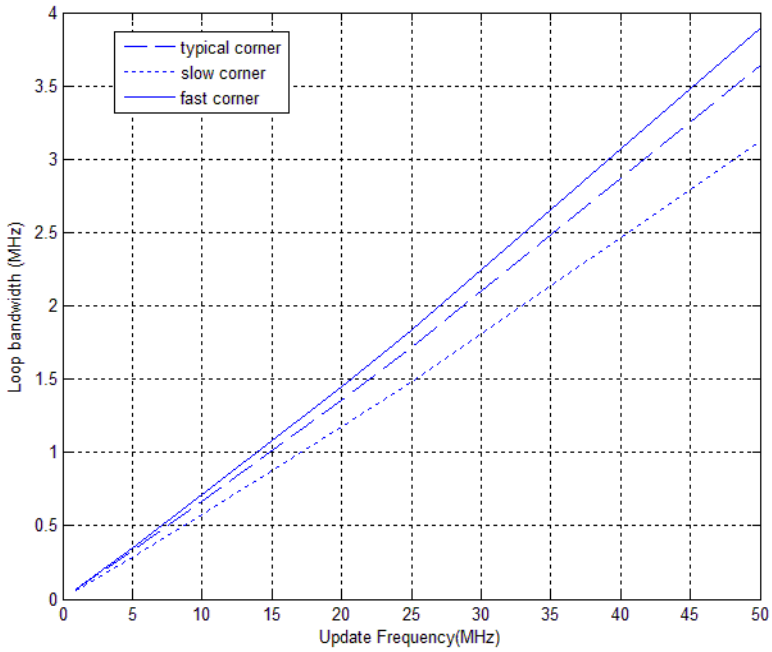

Figure 5.7: Variation of PLL loop bandwidth over different process corners (f_{out} = 2500 MHz).

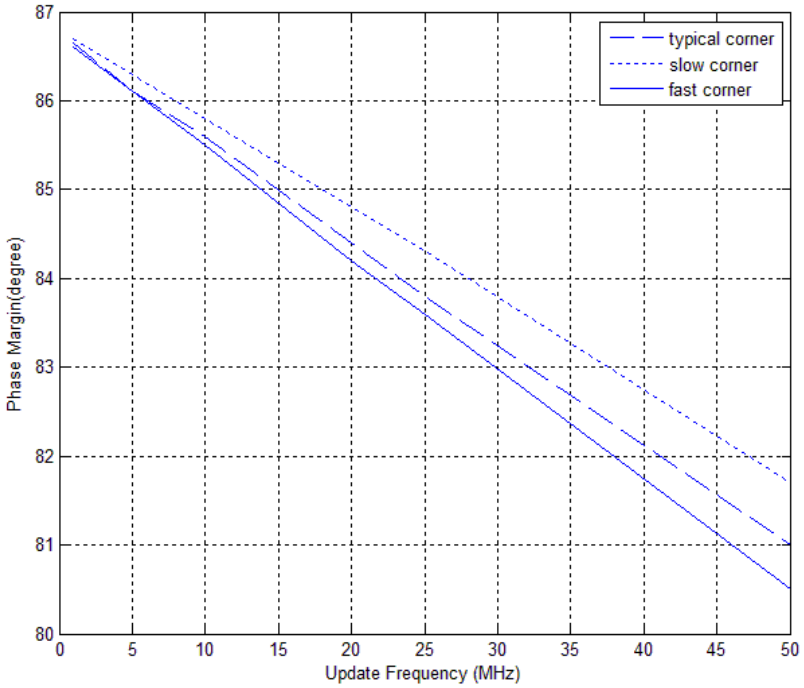

Figure 5.8: Variation of PLL phase margin in different process corners (f_{out} = 2500 MHz).

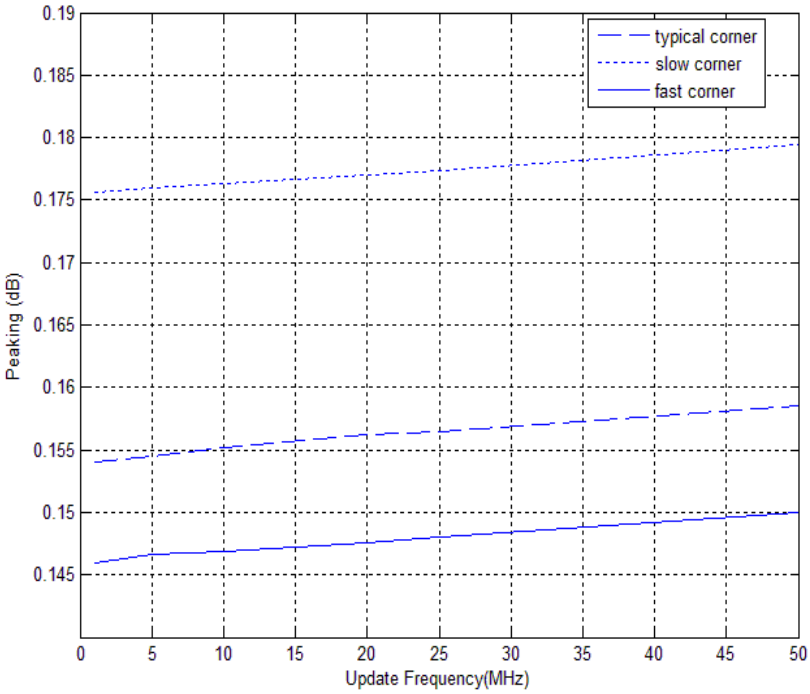

Figure 5.9: Variation of PLL closed loop peaking in different process corners (f_{out} = 2500 MHz).

According to simulations, it can be concluded that PLL bandwidth changes less than ±10 percent at one certain frequency over process corners.

The phase noise generated by the VCO is the major noise contributor to the PLL output most of the time and it is high pass filtered before reaching to the output [13]. Therefore, a high bandwidth PLL filters phase noise of VCO better than a low bandwidth PLL. In Figure 5.10, output phase noise of PLL at 2.5 GHz for different bandwidths is shown. It is clear that phase noise of VCO is better filtered as the bandwidth of PLL increases.

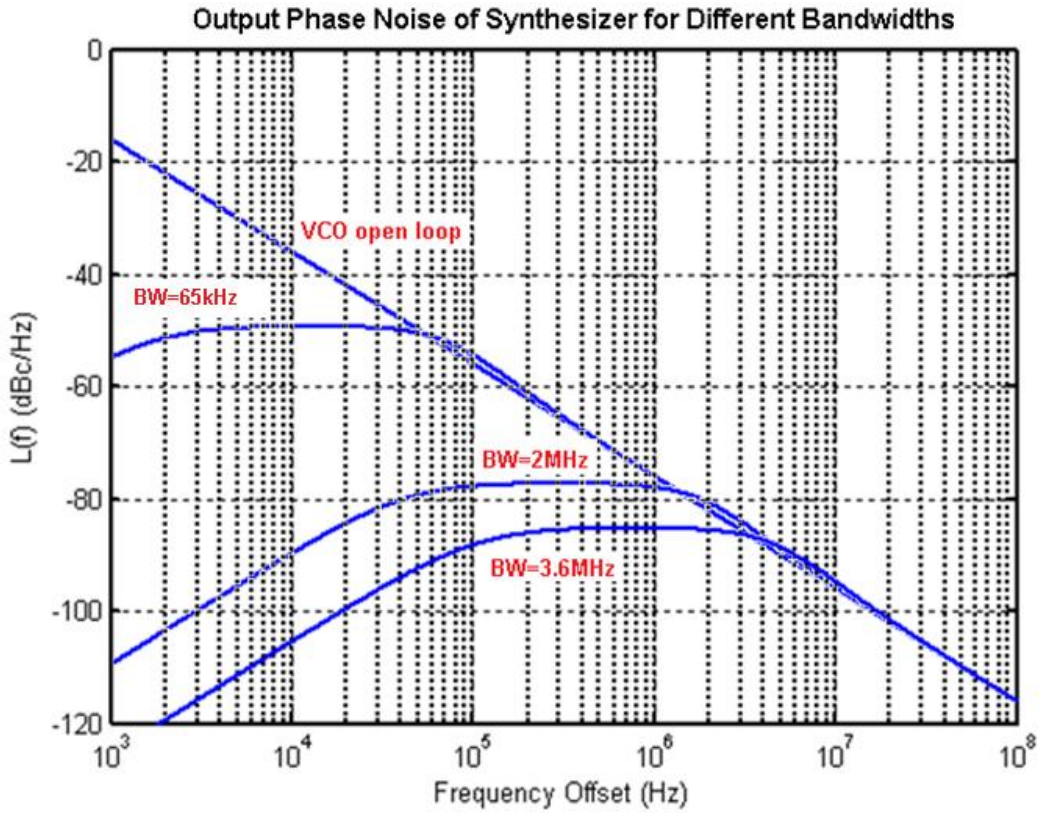

Figure 5.10: Output phase noise of PLL due to VCO phase noise at 2.5 GHz for different bandwidths (open loop, 65 kHz, 2 MHz, 3.6 MHz).

Table 5.3: PLL output rms jitter due to VCO phase noise at 2.5 GHz for different bandwidths.

BW	**65 kHz**	**2 MHz**	**3.6 MHz**
Long term rms jitter	**100ps**	**19ps**	**14ps**

5.2 Marginal Temperature Drift and Re-calibration Issue

Operating temperature range of the designed circuit is -20°C to 105°C. In this temperature range, once the VCO is calibrated in one range, VCO must stay in the same sub-range even if the temperature changes from one edge to another edge.

Frequency characteristics of the VCO were checked when it was calibrated at 105°C. Then the temperature was changed to -20°C. Simulation results show that VCO can still lock to the same frequency in the same sub-band. Thus, re-calibration is not needed. Figure 5.11, Figure 5.12 and Figure 5.13 show VCO frequency control voltage curve in typical, slow and fast corners at 500 MHz VCO frequency.

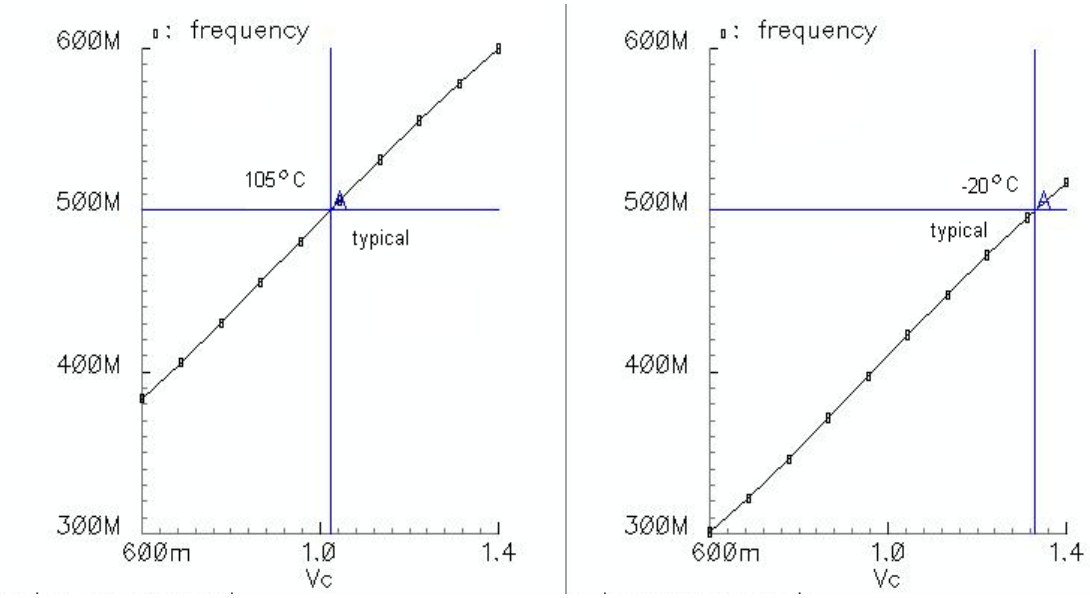

Figure 5.11: VCO voltage to frequency curve in typical corner at 105°C and -20°C when VCO is first calibrated at 105°C (f_{VCO} = 500 MHz).

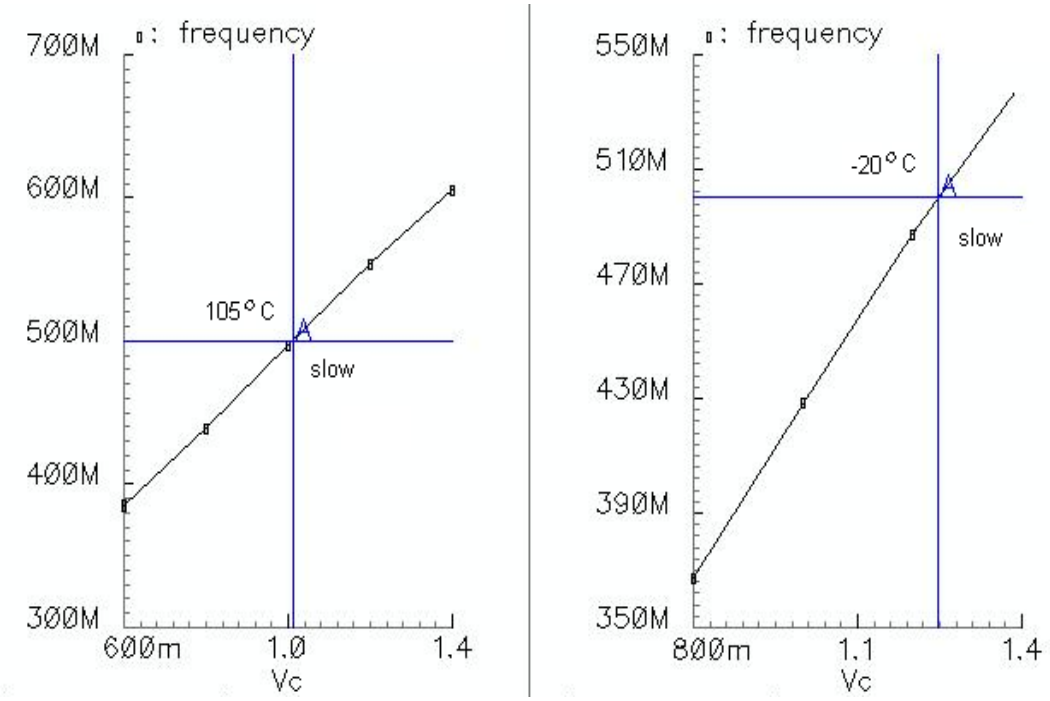

Figure 5.12: VCO voltage to frequency curve in slow corner at 105°C and -20°C when VCO is first calibrated at 105°C (f_{VCO} = 500 MHz).

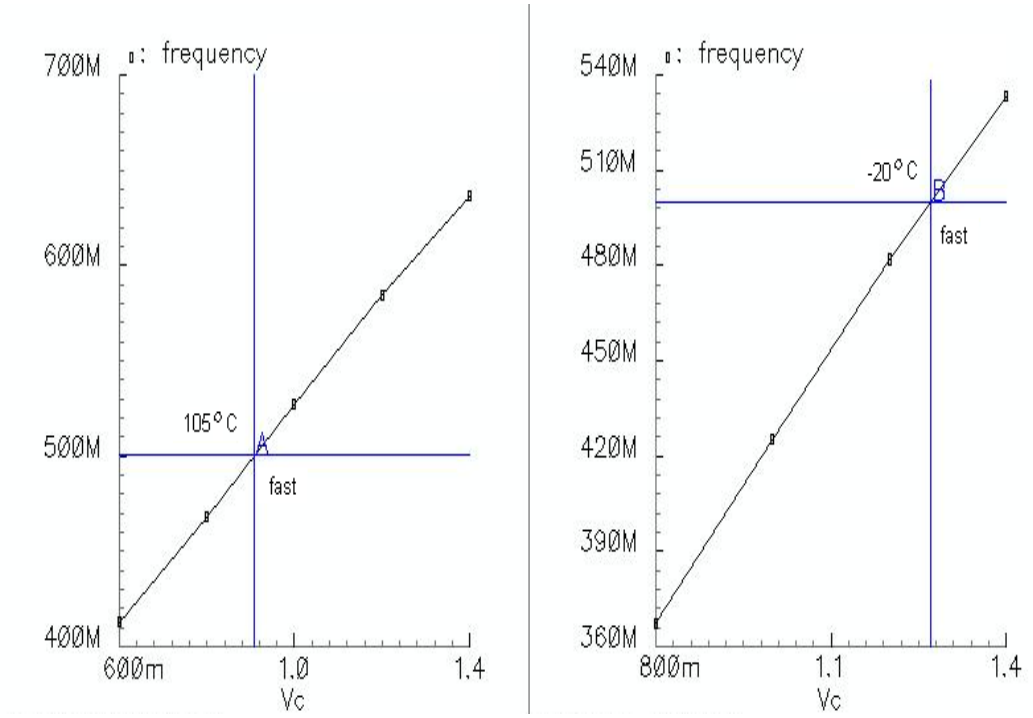

Figure 5.13: VCO voltage to frequency curve in fast corner at 105°C and -20°C when VCO is first calibrated at 105°C (f_{VCO} = 500 MHz).

VCO voltage to frequency curves are also checked at 2500 MHz VCO frequency. Figure 5.14, Figure 5.15 and Figure 5.16 show VCO frequency characteristics in typical, slow and fast corners at 2500 MHz VCO frequency.

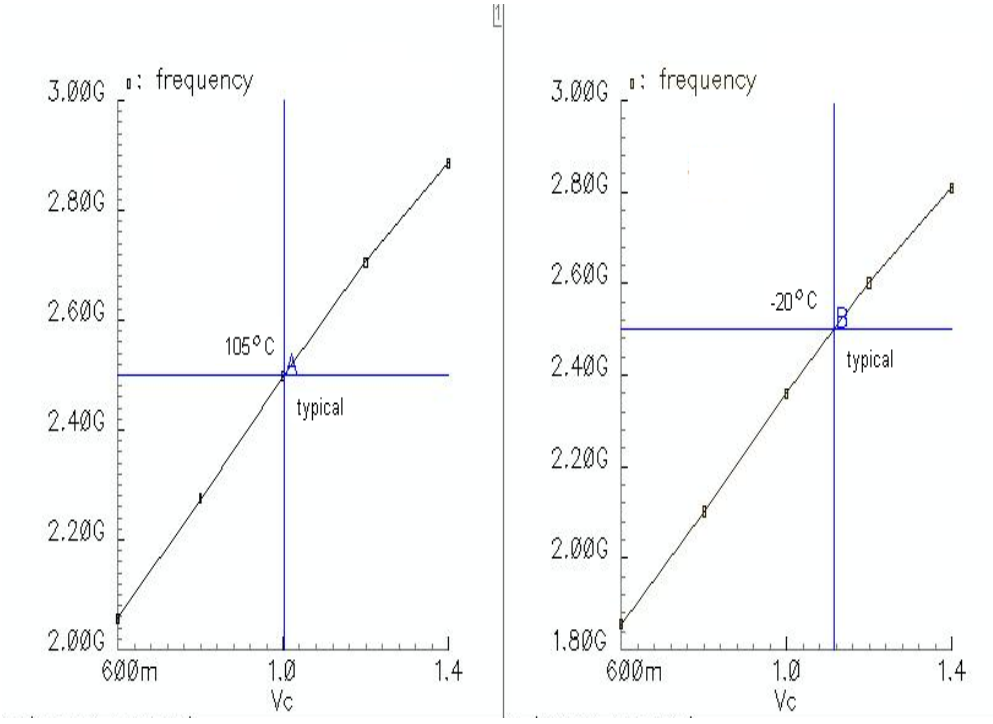

Figure 5.14: VCO voltage to frequency curve in typical corner at 105°C and -20°C when VCO is first calibrated at 105°C (f_{VCO} = 2500 MHz).

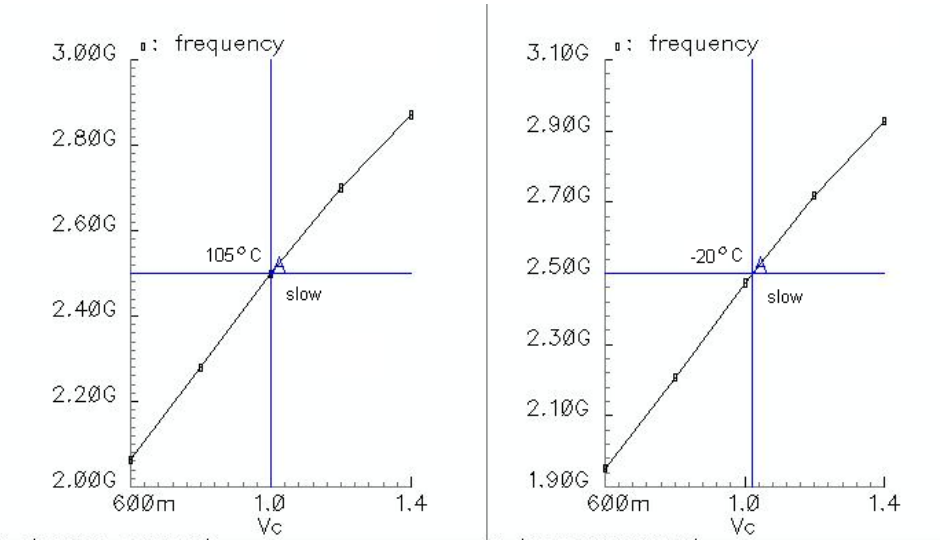

Figure 5.15: VCO voltage to frequency curve in slow corner at 105°C and -20°C when VCO is first calibrated at 105°C (f_{VCO} = 2500 MHz).

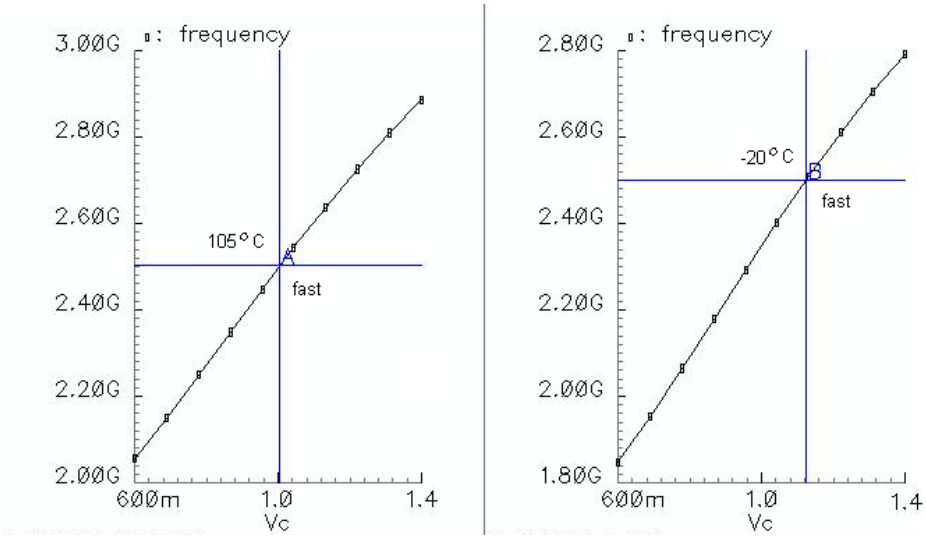

Figure 5.16: VCO voltage to frequency curve in fast corner at 105°C and -20°C when VCO is first calibrated at 105°C (f_{VCO} = 2500 MHz).

5.3 VCO Locking Simulations

VCO lock simulations were run for 10 MHz and 50 MHz update frequencies at 500 MHz and 2500 MHz VCO frequencies. Since the transistor level simulations take too much time, Verilog-A models of the designed blocks were used to simulate the system quickly. The transistor level simulation results of the system are also given in this part.

In Figure 5.17, VCO output frequency during coarse and fine tuning is shown for 10 MHz update frequency, when Ndiv = 50. In coarse calibration, VCO is calibrated in

one sub-range and VCO locks to the target frequency in this range. This is called fine tuning. Zoomed view of fine tuning is shown in Figure 5.18.

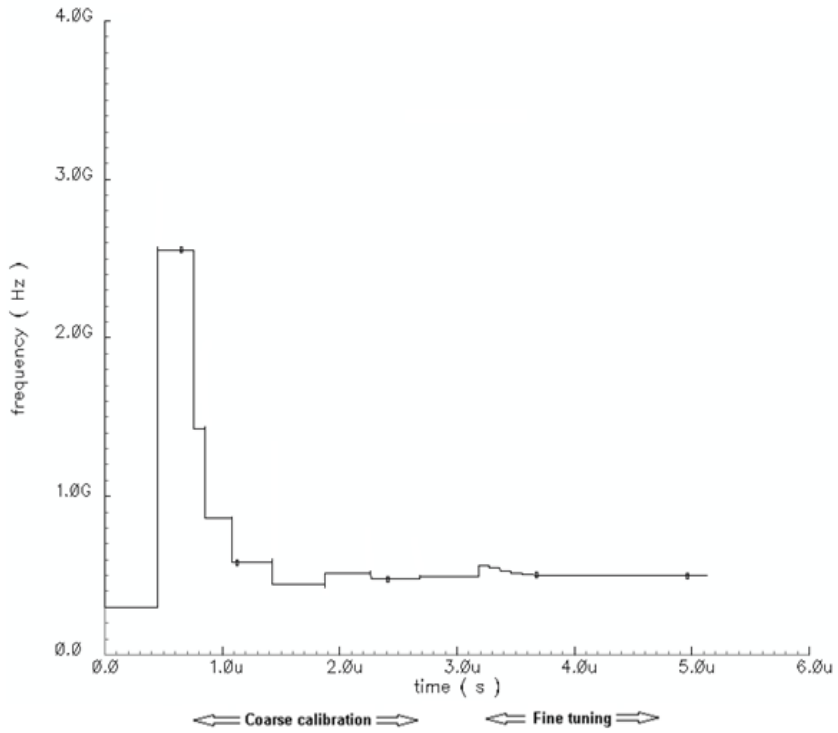

Figure 5.17: VCO output frequency during coarse and fine tuning for 10MHz update frequency (Ndiv = 50, behavioral simulation).

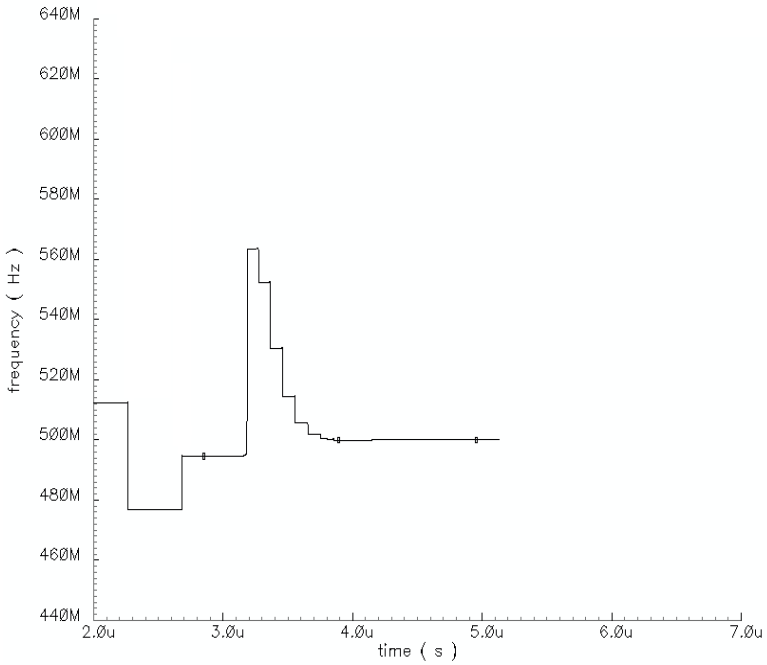

Figure 5.18: Zoomed view of VCO frequency during fine tuning for 10 MHz update frequency (Ndiv = 50, behavioral simulation).

Change of the proportional and integral path control voltages for 10 MHz update frequency is shown in Figure 5.19.

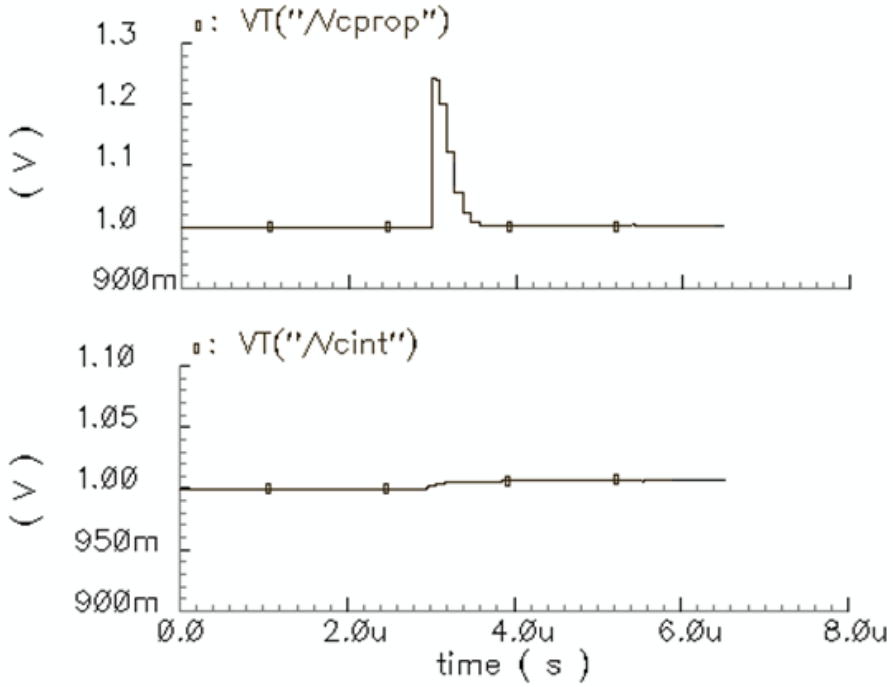

Figure 5.19: Integral and proportional path control voltage changes during fine tuning for 10 MHz update frequency (Ndiv = 50).

VCO output frequency during coarse and fine tuning is shown in Figure 5.20 for 50 MHz update frequency, when Ndiv = 10. Zoomed view of VCO output frequency during fine tuning is shown in Figure 5.21.

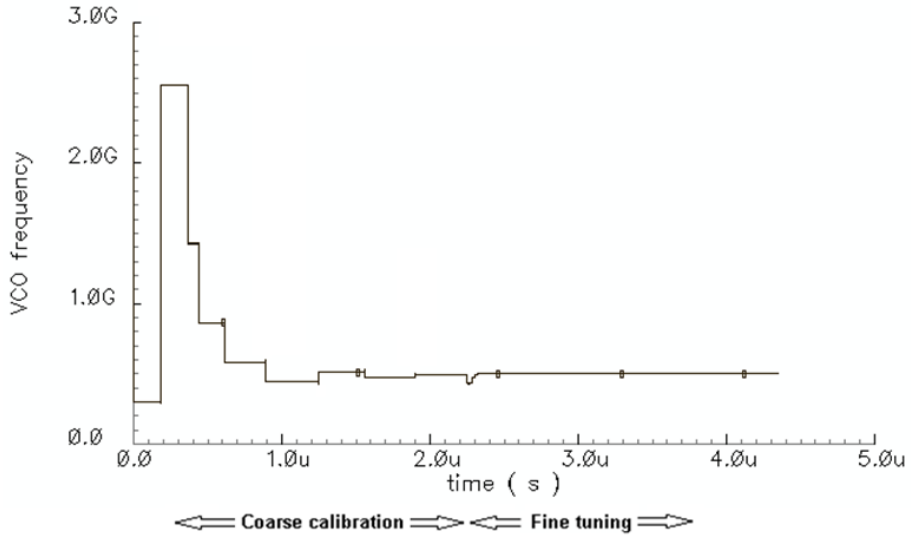

Figure 5.20: VCO output frequency during coarse and fine tuning for 50MHz update frequency (Ndiv = 10, behavioral simulation).

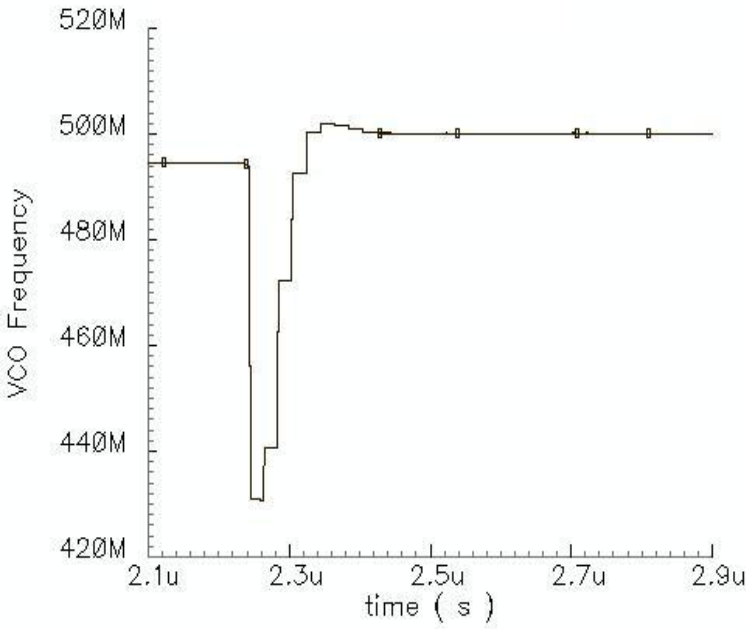

Figure 5.21: Zoomed view of VCO output frequency during fine tuning for 50MHz update frequency (Ndiv = 10, behavioral simulation).

VCO output frequency during coarse and fine tuning steps for 10MHz update frequency when Ndiv = 250 is shown in Figure 5.22. Zoomed view of the fine tuning step is shown in Figure 5.23.

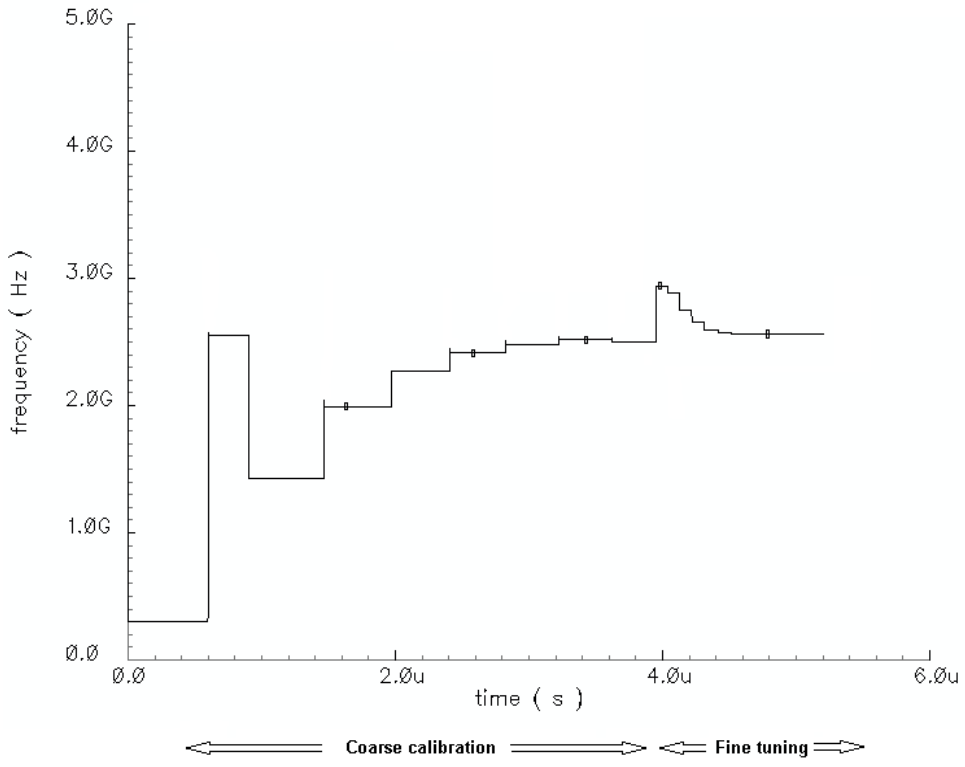

Figure 5.22: VCO output frequency during coarse and fine tuning for 10MHz update frequency (Ndiv = 250, behavioral simulation).

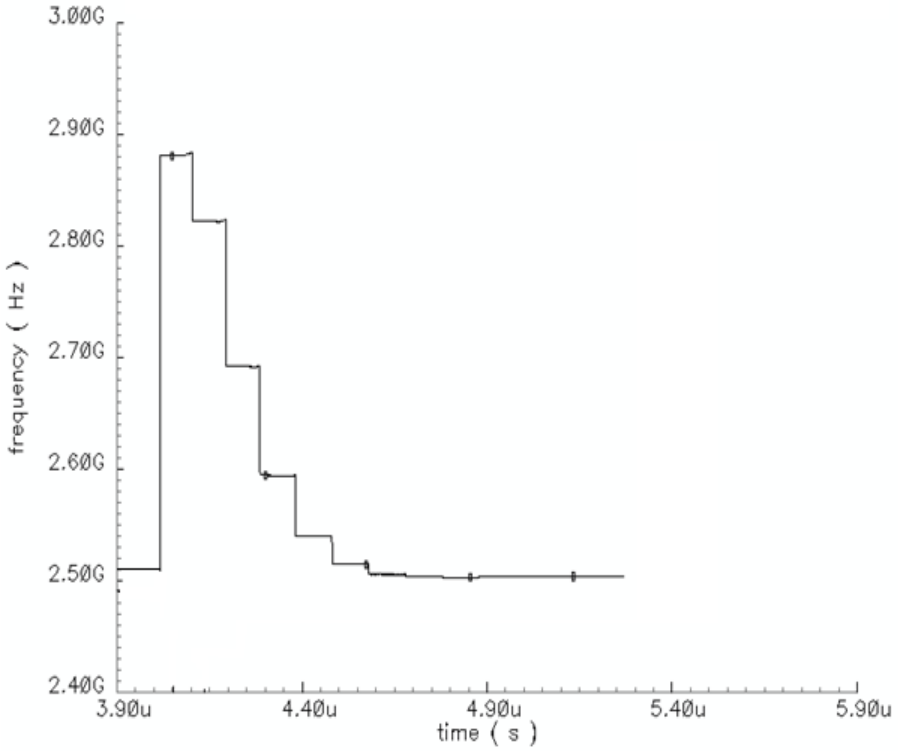

Figure 5.23: Zoomed view of VCO output frequency during fine tuning for 10 MHz update frequency (Ndiv = 250, behavioral simulation).

VCO output frequency during coarse and fine tuning for 50 MHz update frequency when Ndiv=50 is shown in Figure 5.24. Zoomed view of the fine tuning step is shown in Figure 5.25.

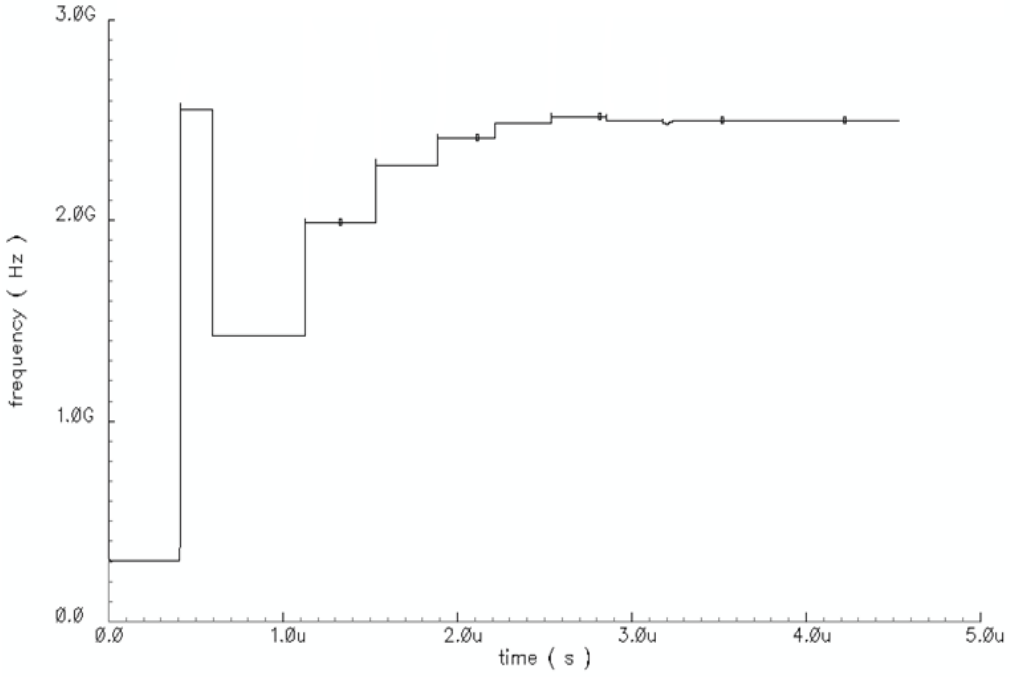

Figure 5.24: VCO output frequency during coarse and fine tuning for 50 MHz update frequency (Ndiv = 50, behavioral simulation).

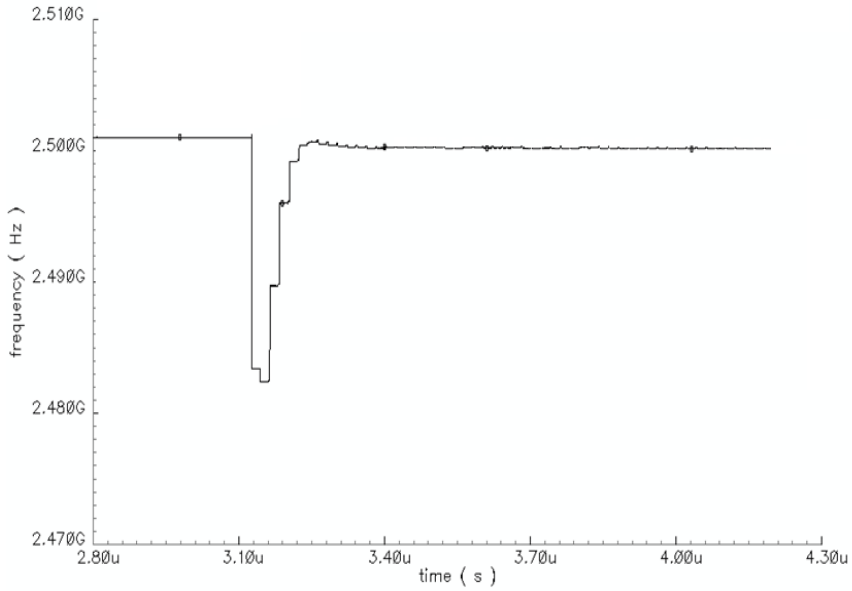

Figure 5.25: Zoomed view of VCO output frequency during fine tuning for 50 MHz update frequency (Ndiv = 50, behavioral simulation).

In this part, we will give the transistor level simulation results of the designed system. VCO output frequency during coarse and fine tuning for 10 MHz update frequency when Ndiv = 50 is shown in Figure 5.26.

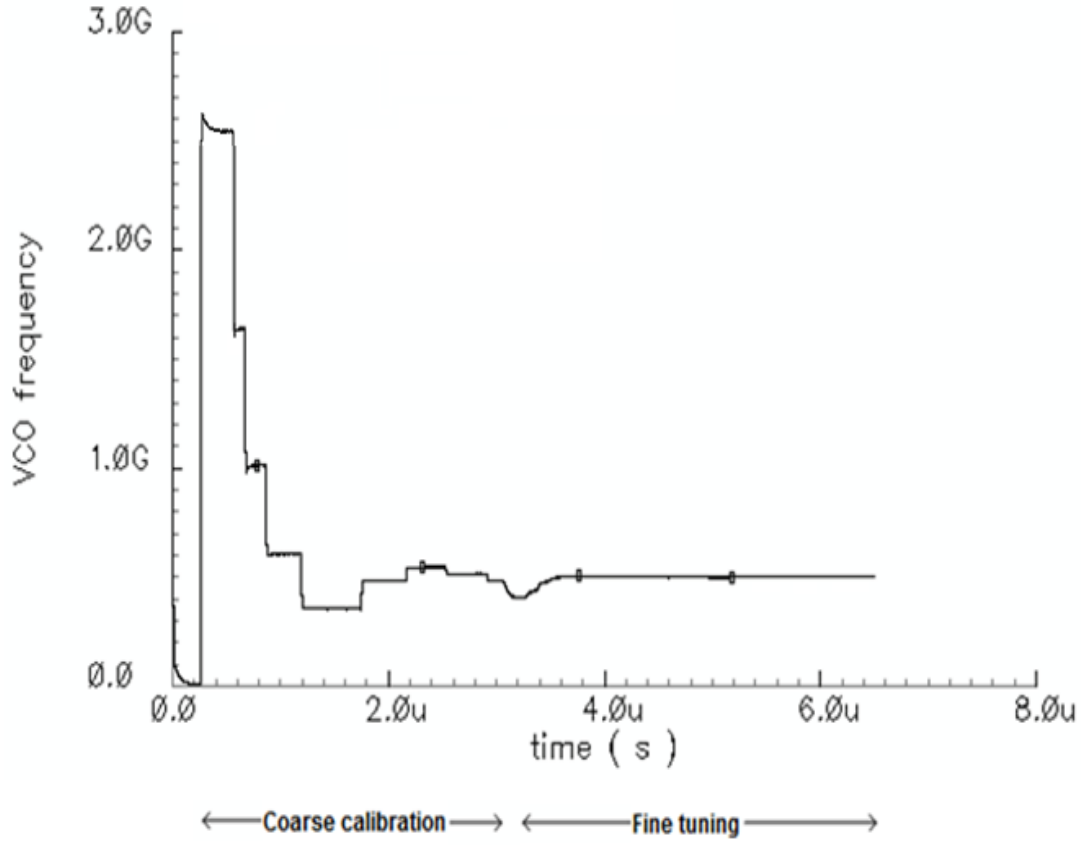

Figure 5.26: VCO output frequency during coarse and fine tuning for 10MHz update frequency (Ndiv = 50, transistor level simulation).

VCO output frequency during coarse and fine tuning for 50 MHz update frequency when Ndiv = 10 is shown in Figure 5.27. Zoomed view of fine tuning step is shown in Figure 5.28.

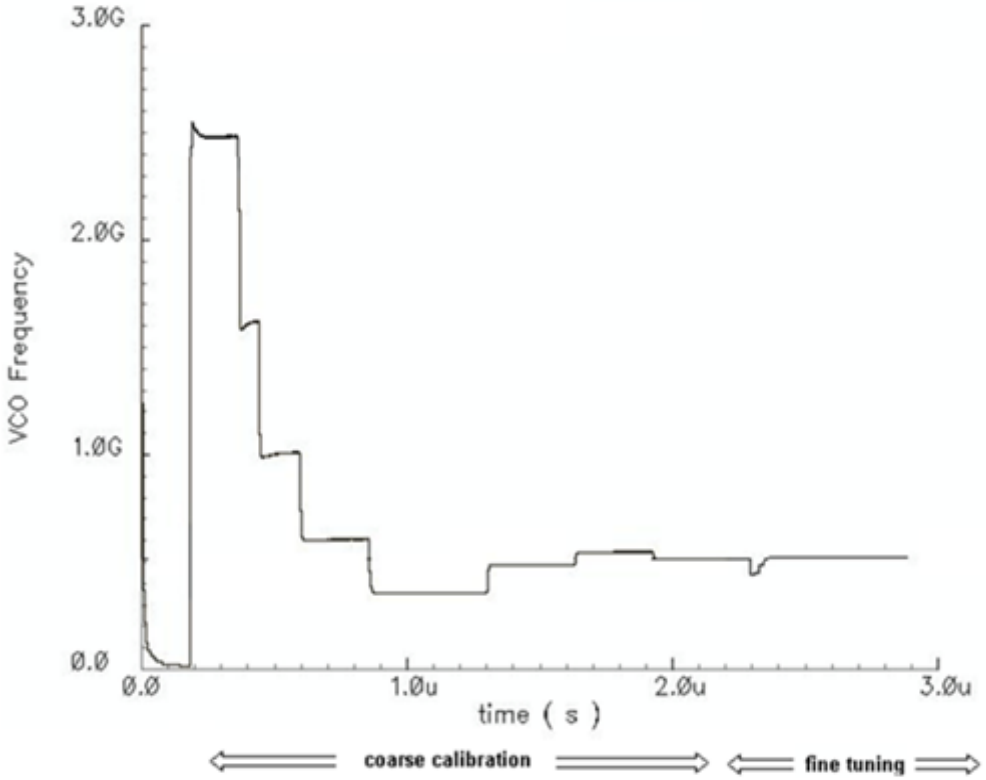

Figure 5.27: VCO output frequency during coarse and fine tuning for 50 MHz update frequency (Ndiv = 10, transistor level simulation).

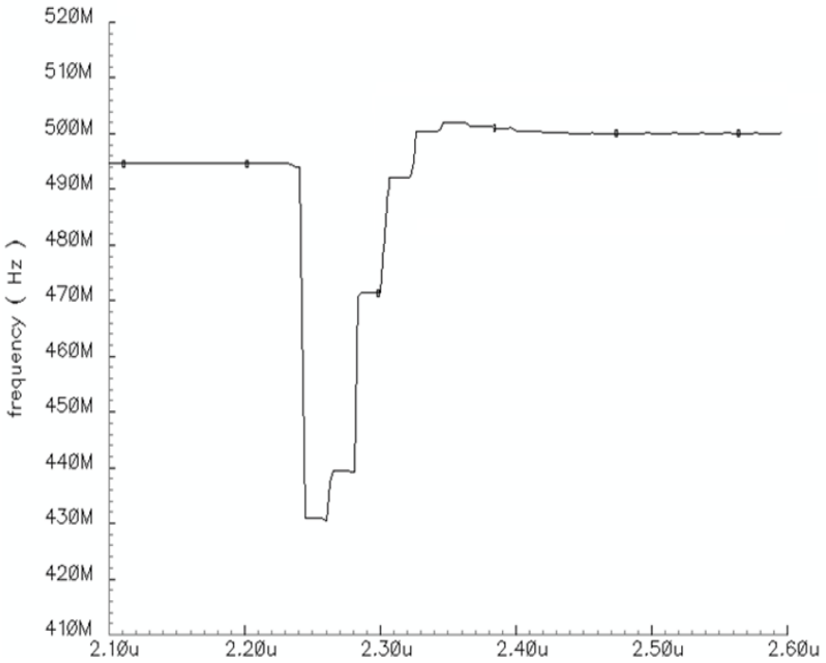

Figure 5.28: Zoomed view of VCO output frequency during fine tuning for 50 MHz update frequency (Ndiv = 10, transistor level simulation).

VCO output frequency during coarse and fine tuning for 10 MHz update frequency when Ndiv=250 is shown in Figure 5.29. Zoomed view of fine tuning step is shown in Figure 5.30.

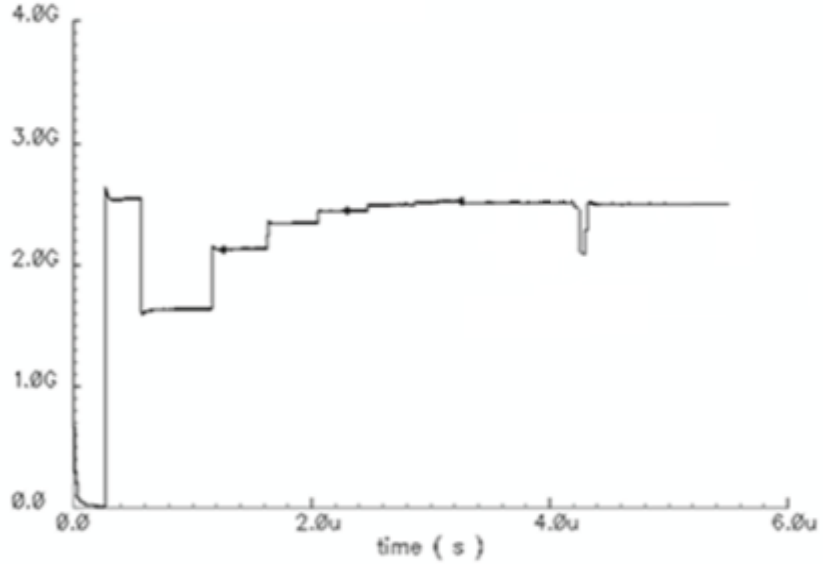

Figure 5.29: VCO output frequency during coarse and fine tuning for 10MHz update frequency (Ndiv = 250, transistor level simulation).

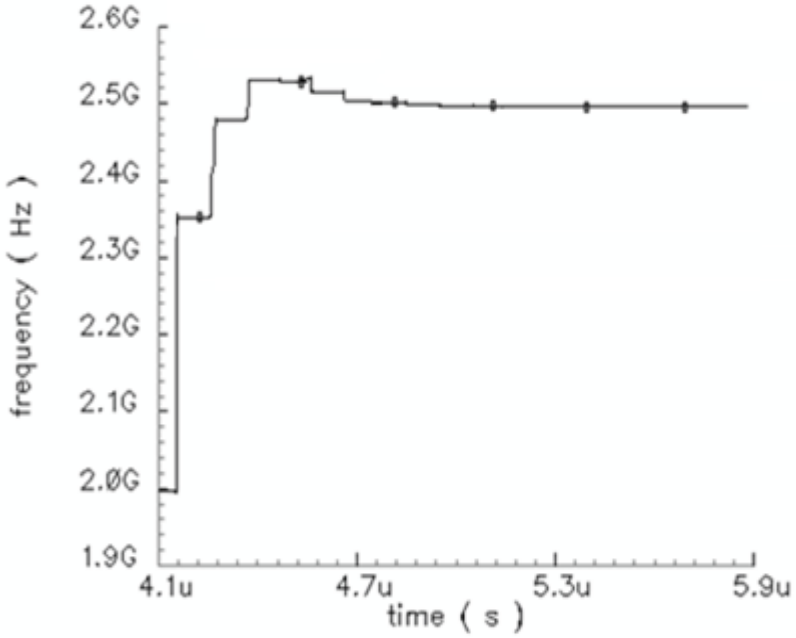

Figure 5.30: Zoomed view of VCO output frequency during fine tuning for 10 MHz update frequency (Ndiv = 250, transistor level simulation).

In Figure 5.31, VCO output frequency during coarse and fine tuning steps is shown. Update frequency is 50 MHz and Ndiv = 50 in this case. Figure 5.32 shows zoomed view of VCO output frequency during fine tuning step.

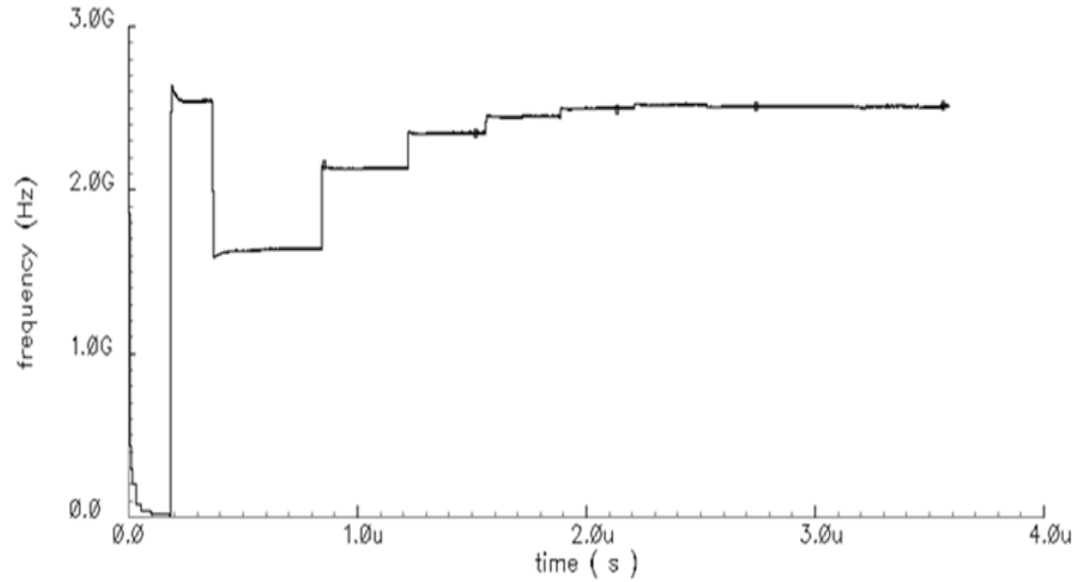

Figure 5.31: VCO output frequency during coarse and fine tuning for 50MHz update frequency (Ndiv = 50, transistor level simulation).

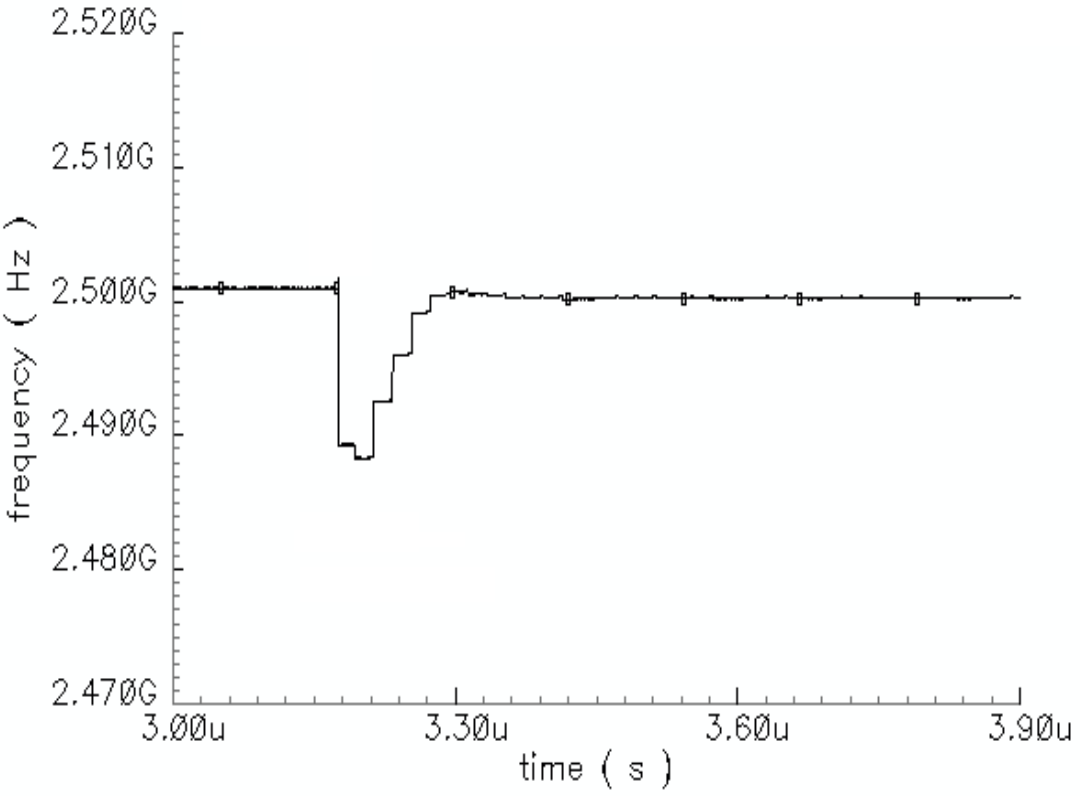

Figure 5.32: Zoomed view of VCO output frequency during fine tuning for 50MHz update frequency (Ndiv = 50, transistor level simulation).

In Figure 5.33, locking behavior of conventional and proposed PLL is shown to visualize the locking behavior difference. Note that both of the PLLs have 800kHz bandwidth.

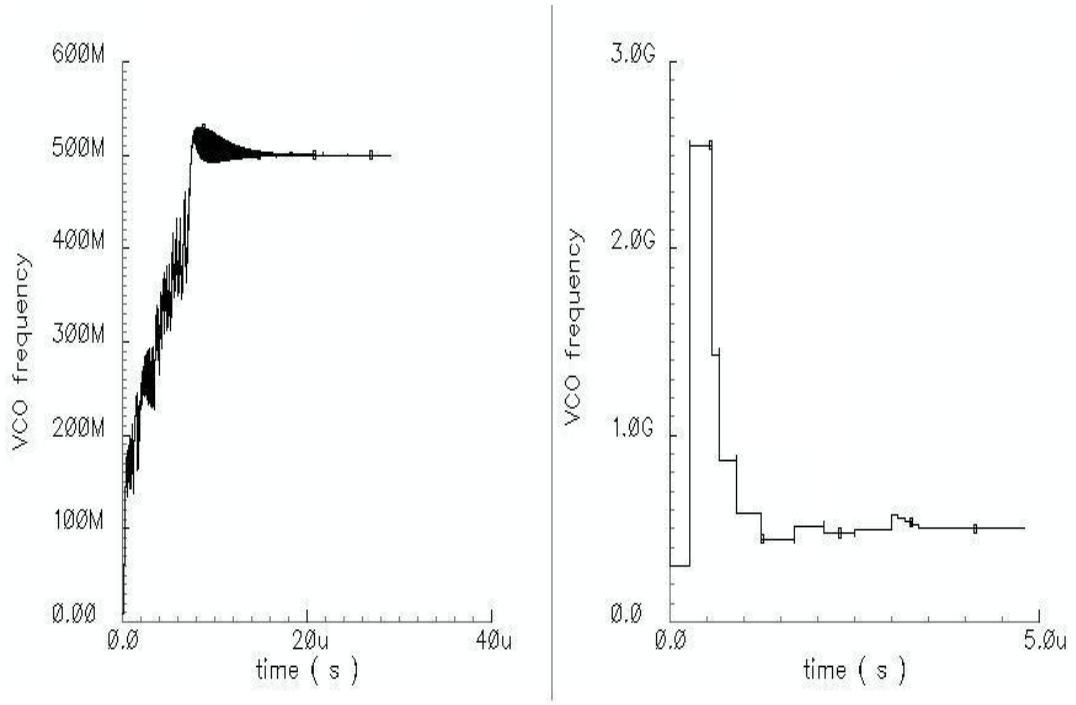

Figure 5.33: Comparison of locking behaviour of conventional and proposed PLL at 10MHz update freqeuency, Ndiv = 50 (BW = 800kHz for both of PLLs).

In Table 5.4, comparison of the basic properties of some important adaptive PLLs in literature with this work is given.

Table 5.4: Comparison of some adaptive bandwidth PLLs in literature.

	Technology	Loop update rate	VCO frequency range	Auto-calibration	Loop Filter Type	Number of switches	configuration
[2]	0.18µm CMOS	N/A	125MHz-1250MHz	No	Hybrid	6	Dual-loop
[3]	0.18µm CMOS	30kHz-250MHz	2.5MHz-1000MHz	No	Fully-sampled	11	Dual-loop
[4]	0.13µm CMOS	150kHz-30MHz	30MHz-650MHz	No	Hybrid	2	Dual-loop
This work	0.18µm CMOS	1MHz-50MHz	500MHz-2500MHz	Yes	Hybrid	2	Dual-loop

5.4 Spread Tracking Application

High date rates of today's technology leads to higher EMI (electromagnetic interference) [24]. These interferences may create disturbances in other electronic devices. There are some techniques to reduce EMI such as using filter or shielded cables. However, these techniques are expensive and occupy large area [25]. There is a technique called as spread spectrum. It is actually a special case of frequency

modulation. It spreads energy of the signal to a wider band so that lower EMI is obtained.

In this application, we will compare spread tracking behavior of a conventional PLL and adaptive bandwidth PLL. Both of the PLLs can operate down to 1 MHz update frequency. Therefore, bandwidth of PLLs were chosen as 80 kHz at 1 MHz update frequency in order to prevent instability. We compared PLLs at 10 MHz update frequency. At this frequency, adaptive PLL automatically increases its bandwidth around 10 times. However, bandwidth of the conventional PLL does not change. We used a triangular shaped input clock frequency to modulate VCOs. Note that the modulation frequency of the input clock is 40 kHz. Figure 5.34 shows spread tracking behavior of both PLLs. It is seen that conventional PLL output frequency is nosier than adaptive PLL output frequency. This is because the sample reset loop filter prevents the ripples at the VCO control voltage. Variation of the delay between the conventional PLL and adaptive PLL VCO outputs also shows that adaptive PLL tracks the input clock better than conventional PLL.

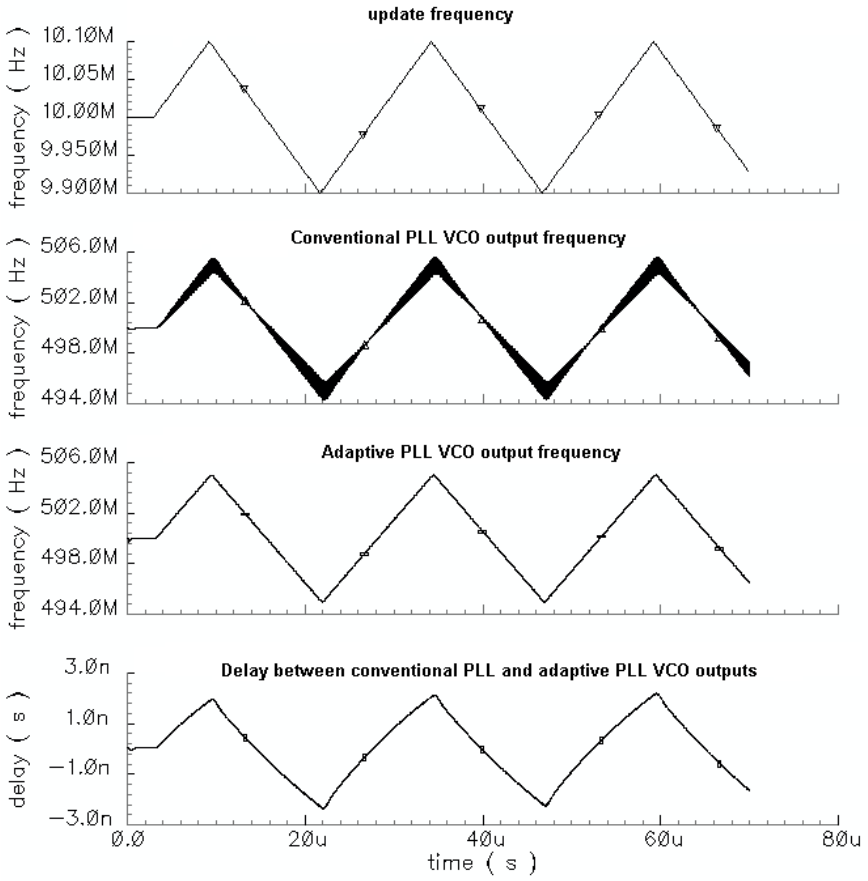

Figure 5.34: Input spread tracking behavior of a conventional PLL and adaptive bandwidth PLL for 10 MHz update frequency, Ndiv = 50.

6. CONCLUSION AND FUTURE RESEARCH

This work has presented a study of VCO calibration methods and configurable bandwidth PLLs using adaptive approach.

The research first focused on VCO calibration methods based on a comparative study of the various architectures. Then, we focused on digital calibration methods due to their low process and temperature dependency. All of these digital calibration methods use frequency comparison techniques. A new calibration method, which nearly eliminates process and temperature dependency of the comparison, was proposed and designed in 0.18µm CMOS technology. According to corner simulations, calibrated VCO does not need re-calibration even if the temperature changes marginally.

Next, we proposed a configurable bandwidth PLL using the adaptive approach. We introduced a new tracking mechanism between the natural frequency, stabilizing zero and the update frequency. Therefore, bandwidth of the proposed PLL can be adjusted to the desired value without threatening the stability just by programming the update rate. Designed circuit was verified in Cadence design environment. Loop update rate of the system can be adjusted between 1 MHz-50 MHz without threatening the stability. VCO can operate between 500 MHz-2500 MHz. It was also shown that bandwidth of the designed PLL has low process and temperature dependency. According to corner simulations, PLL bandwidth changes less than 10% with process and temperature corners.

As a future work, designed system can be fabricated and tested. Moreover, VCO gain can be reduced for high VCO frequencies by using SAR word obtained in coarse calibration. In this case, charge pump current must also be increased in order to keep the loop bandwidth constant. Additionally, VCO jitter performance can also be optimized for high performance system applications.

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