PREFACE

I find it necessary to thank everybody - without giving their names - who have encouraged and supported me while I was taking my steps at each stage of my educational life upon today.

I feel obliged to dedicate my thesis to all the trees cut down to supply the papers I spoilt during my studies and the papers you are touching now.

This thesis will probably serve directly to the high-technological progress of our century which unfortunately still serves dominantly to war technology. Therefore, if any of the ideas in my work is used in the future for high-technology developments, I hope it helps human beings and all other living creatures on earth live in peace.

Ali Zeki

13/10/1997.

CONTENTS

SUMMARY

Continuous-time filtering is still an alternative filtering technique to the switched-capacitor filtering technique for many VLSI applications, especially at high frequencies. OTA-C continuous-time filters proved to be much more suitable (especially high frequency behavior and tuning properties are better) with respect to operational amplifier based integrated continuous-time filters (MOSFET-C is the best known). However, OTA-C filters do possess some drawbacks due mainly to non-idealities of the utilized OTAs.

In this work, novel operational transconductance amplifier (OTA) structures more suitable for continuous-time OTA-C filters (and oscillators) are proposed. Therefore, the most critical properties of OTAs affecting the non-ideal behavior of an OTA-C continuous-time filter are investigated. Conventional techniques/structures reducing non-idealities are analyzed and their disadvantages and/or inefficiencies are revealed. Novel building blocks are proposed to eliminate the non-idealities in a more efficient way with respect to conventional techniques. Also, some modifications are suggested for several advanced structures to increase their efficiencies in reducing non-idealities.

The proposed structures have been compared with classical structures in the view of their performances in OTA-C filtering. Simulations prove that the OTA-C filters constructed with proposed OTA structures exhibit much greater performance characteristics with respect to classical structures.

ÖZET

SÜREKLİ-ZAMAN OTA-C SÜZGEÇLERE UYGUN YÜKSEK PERFORMANSLI YENİ OTA YAPILARI

Analog ve dijital elektronik arasındaki yarış, özellikle iletişim (sayısal işaret işleme) ve otomasyon sistemlerinde, dijital elektronik tarafından kazanılmış görülmektedir. Ancak, gerçek dünya 'analog' olduğundan, VLSI'da en azından arayüzlerde analog yapıtaşlarına gereksinim vardır. Analog-dijital arayüzlerinde analog süzgeçlerin kullanımı bir zorunluluktur [4], [5], [6].

Ayrık pasif analog süzgeçlerin tümdevreye doğrudan uyarlanması, yeterince yüksek değerli endüktans elemanlarının kırmık üzerinde gerçekleştirilememesinden dolayı olanaksızdır. Aktif RC süzgeçlerde işlemsel kuvvetlendirici yardımıyla endüktans elemanının yokluğu giderilmiş olduğundan, bu tür süzgeçler tümleştirmeye daha uygundur. Ancak kırmık üzerinde gerçekleştirildiklerinde, özellikle pasif dirençlerin kapladıkları alan, yüksek toleransları ve sıcaklığa aşırı bağımlı olmaları yüzünden birçok sorun ortaya çıkar.

Tümüyle tümleştirilmiş aktif süzgeçler, 'sürekli zaman' (continuous-time) ve 'örneklemeli veri' (sampled-data) sistemleriyle elde edilebilmektedir. Her iki türün diğerine göre bazı üstünlükleri ve dezavantajları vardır. Örneğin örneklemeli veri süzgeçleri düşük distorsiyonlu ve yüksek doğruluklu frekans yanıtı sağlayabilir ve kırmık alanını verimli kullanırlar; ancak yüksek frekanslar için uygun değildirler [4]. Sürekli zaman süzgeçleri yüksek frekanslarda kullanılabilirler, ancak üretim süreci toleransları, sıcaklık, parazitikler, yaşlanma gibi etkilere çok bağımlı olduklarından otomatik ayara (frekans yanıtını düzeltmek için) gereksinim duyarlar [5].

Anahtarlamalı kapasite süzgeçler örneklemeli veri sistemlerinden en yaygın olanıdır. İşlemsel kuvvetlendiricinin sonlu kazanç-band genişliği, sonlu dc gerilim kazancı, anahtarların sonlu dirençleri, saat girişimi (clock-feedthrough) vb. yüzünden, yüksek frekanslarda (MHz bölgesine girilirken) bunların performansı keskin biçimde düşer. Ayrıca, aliasing önleyici ve düzeltici süzgeçlerin kullanımını gerektirmeleri ve Nyquist frekansı mertebesinin seçimini kısıtlamaları bir dezavantajdır [4], [5], [6], [8], [9], [10], [11], [12], [13], [14], [15], [16].

Anahtarlamalı kapasite süzgeçlerin dezavantajları, örneklemeli veri süzgeçlerin yeterli performans gösteremediği birçok uygulama için tümüyle tümleştirilmiş yüksek performanslı sürekli zaman süzgeçlerinin geliştirilmesini gerekli kılmaktadır. Bu yüzden bu konu üzerinde yoğun çalışmalar yapılmaktadır [5], [6], [8], [10], [11], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33].

Aktif-RC süzgeçlerin gerçekleştirilmesindeki pasif dirençlerle ilgili sorun ve zorluklar, VLSI'a uygun sürekli zaman süzgeçleri olarak sunulan MOSFET-C süzgeçlerle çözüm bulmuştur [8], [13], [40], [41], [42]. Bu yapılarda klasik aktif-RC süzgeçlerdeki dirençler doğrusal bölgede çalışan ve eşdeğer direnç değeri gerilimle ayarlanabilen MOSFETlerle değiştirilmiş, böylece hem pasif dirençlerin yarattığı sorunlardan kurtulunmuş, hem de otomatik ayar olanağı sağlanmıştır. Ancak bu yapıların da bazı önemli sorunları vardır. Özellikle işlemsel kuvvetlendiricilerin band genişliği sınırlamaları, dengeli giriş-çıkışa olan gereksinim (MOSFET dirençlerin non-lineerliklerinin getirdiği etkileri gidermek için) ve MOSFET dirençlerin dar ayar aralığıyla ayarın verimli bir biçimde yapılamaması en önemli sorunlardır [10], [29], [43].

Öte yandan, geçiş iletkenliği katları (transconductor veya OTA) ile kapasitelerin kullanıldığı G_m-C süzgeçlerinde, özellikle bir OTA'nın eşdeğer bir işlemsel kuvvetlendiriciden daha geniş bandlı olması, en önemli üstünlüktür [5], [10], [17], [21], [25], [26], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55]. Diğer üstünlükler, daha az kırmık alanı kullanımı, daha düşük güç harcaması, daha etkin frekans yanıtı ayarı (bir kontrol gerilimi veya akımının değiştirilmesiyle G_m ayarlanarak), ayarlanabilir frekans bölgesinin daha geniş olması, daha az aktif eleman gereksinimi ve tasarımın basitliği, biçiminde sıralanabilir [5], [9], [29], [34], [43], [56], [57].

OTA-C süzgeçlerin bu avantajları, son yıllarda yüksek performanslı OTA-C süzgeç ve osilatör konfigürasyonlarının elde edilmesi için yoğun çalışmalara yol açmıştır [36], [43], [56], [60], [61], [62], [63], [64], [65], [66], [67], [68]. Ancak, avantajlar yanında OTA-C süzgeçlerin özellikle OTA idealsizliklerinden kaynaklanıp süzgeç davranışını kötü yönde etkileyen bazı dezavantajları da vardır. Bunların en önemlileri, giriş katının (genellikle uzun kuyruklu çift) dar doğrusallık aralığı (doğrudan yükselme eğimi davranışını etkiliyor) ve sonlu çıkış direncidir. Bu istenmeyen özellikler daha derinliğine ele alınırsa, OTA-C süzgeçlerde aşağıda sıralanan etkilere neden oldukları ortaya çıkar.

- Giriş fark gerilimi yeterince küçük genlikli değilse, nonlineer I_{OUT}-V_{IN} karakteristiği yüzünden harmonik distorsiyonu yüksektir. Bunun ötesinde, büyük giriş işaretleri için genliğe bağımlı bir 'eşdeğer' G_m (küçük işaret G_m'inden farklı) oluşur ve OTA-C süzgeç davranışında frekans distorsiyonuna neden olur (rezonans sıçraması) [9], [17], [37].
- Çıkışa bağlı bir yük kapasitesi sınırlı bir akımla, dolayısıyla sınırlanmış bir hızda dolup boşalabildiğinden çıkış geriliminde yükselme eğimi sınırlamalarına neden olur (çıkış düğümündeki eşdeğer kapasite ve olası en büyük çıkış akımına bağlı) [4], [17], [37], [59].
- Temel OTA-C entegratör yapısında (1 OTA ve çıkışına bağlı 1 kondansatör), çıkış direnci yük kondansatörünü düşük frekanslarda sürebilecek kadar büyük olmalıdır (kapasitenin empedansı düşük frekanslarda arttığı için), aksi halde düşük frekanslarda entegrasyon işlevi gerçekleştirilemez (yüksek çıkış dirençli klasik kaskod yapılarla bile birkaç pF'lık yük kapasitelerinde alt sınır kHz'ler mertebesinde olabilmektedir). Bu

sorun kayıplı entegrasyona neden olur ve süzgeç frekans yanıtının bozulmasına yol açar [10], [11], [58], [59], [69], [70].

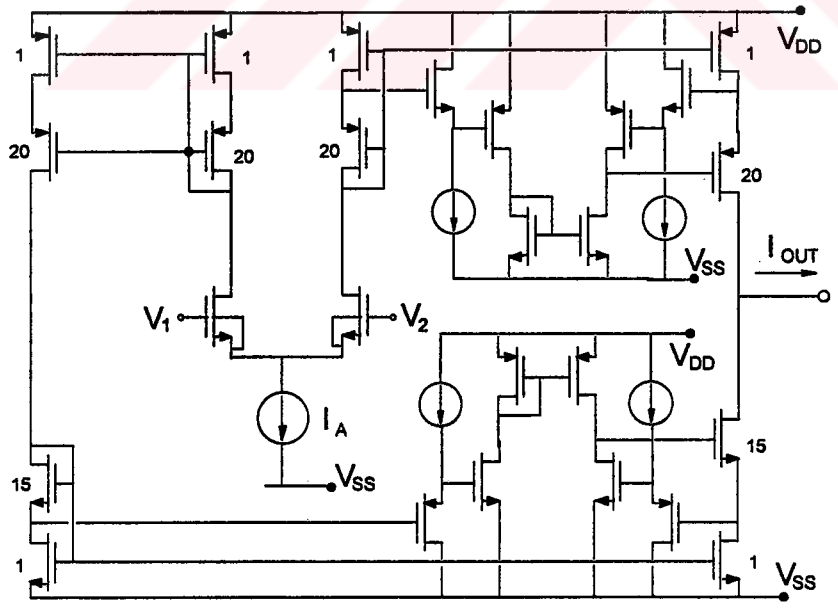
Bu çalışmanın amacı, sürekli zaman OTA-C süzgeçlere daha uygun yeni OTA yapılarının önerilmesidir. Bu yüzden OTA'nın süzgeç davranışını en çok etkileyen kritik özellikleri incelenmekte, bu özelliklerin iyileştirilmesine yönelik geleneksel teknik ve yapıların dezavantajları ve yetersizlikleri ortaya konmaktadır. Geleneksel performans artırıcı teknik ve yapıların iyileştirilmelerine yönelik öneriler getirilmekte, bunun yanında OTA performansını daha etkin artırmak için yeni devre yapıtaşları sunulmaktadır.

Giriş katının (gerilim-akım dönüştürücüsü) doğrusallaştırılmasına yönelik pek çok çalışma yapıldığından, bu çalışmada bu konu üzerinde fazla durulmamakta, daha fazla akım modu katlarında (akım kaynağı, akım aynası, akım çıkış katı) performans artırıcı öneriler ve yeni yapılar sunulmaktadır. Bu yüzden, temel akım modu katı olan akım aynaları üzerinde yoğunlaşılmaktadır.

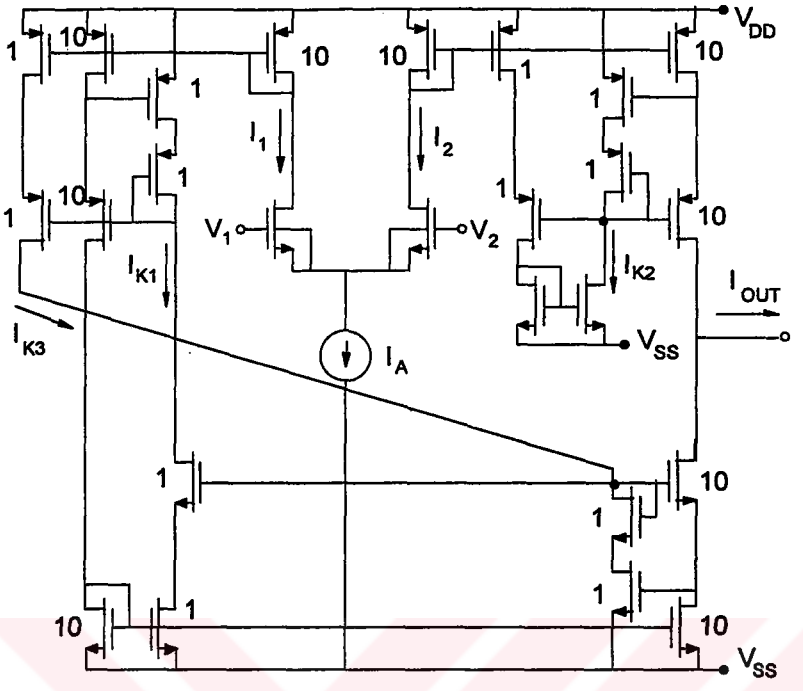
Önerilen performans artırıcı yeni yapıların aşağıdaki özelliklere sahip olmaları yaygın kullanım alanı bulabilmeleri için oldukça önemlidir.

- güç sarfiyatının klasik yapılara göre pek fazla olmaması
- parazitiklerin olabildiğince az olması
- tasarımın basit olması
- VLSI üretim süreçlerine uyumlu olması

Bu yüzden, çalışmada sunulan yapıların bu koşulları kesinlikle sağlamalarına dikkat edilmiştir. Ayrıca klasik yapıların yeterli ölçüde sağladığı yüksek performans özelliklerinin yeni yapılarca da - en azından aynı ölçüde - sağlanması gözetilmiştir.



Şekil 1 Önerilen yüksek performanslı aktif-geribeslemeli kompakt kaskod OTA.



Şekil 2 Önerilen yüksek performanslı aktif-geribeslemeli kaskod OTA.

Çalışmada sunulan akım aynalarının geleneksel akım aynalarına göre birçok üstünlükleri bulunmaktadır. Bu akım aynalarının özgün bir biçimde (güç sarfiyatı ve parazitikleri minimize edecek biçimde) simetrik OTA yapılarına uyarlanması, OTA-C süzgeç ve osilatörlere klasik yapılardan çok daha uygun yüksek performanslı OTA yapılarını olanaklı kılmaktadır. Önerilen yapılar arasından kimileri düşük besleme geriliminde çalıştırılabilmekte, kimisinde güç sarfiyatı hemen hemen klasik yapılardaki kadar olmakta, kimisindeyse parazitikleri düşük kalmaktadır. Bu ise, çalışmanın sunduğu OTA'lar arasından uygulamaya bağlı olarak seçim yapma esnekliği olduğunu göstermektedir.

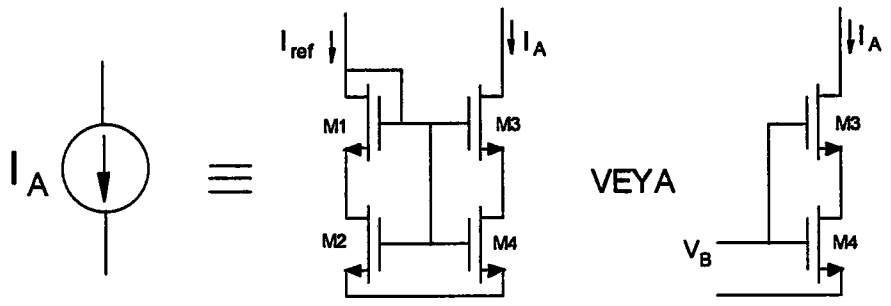
Şekil 1 ve Şekil 2'de önerilen yeni yapılar arasından genel amaçlar için en yüksek performansa sahip olanlar verilmiştir. Bu iki yapının simülasyonla elde edilen performans özellikleri, karşılaştırmaya olanak sağlamak için eşdeğer bir klasik kaskod OTA yapısınınkilerle birlikte Tablo 1'de verilmiştir (Tüm yapılarda, giriş katının kuyruk akım kaynağı olarak Şekil 3'teki yeni yapıların (akım veya gerilim kontrollü) kullanılması uygun görülmüştür). Görüldüğü gibi, yeni OTAlar özellikle çıkış direnci ve çıkış salınım aralığını oldukça iyileştirmekte, bunun yanında pek fazla dezavantaj getirmemektedir.

Şekil 4'te, yeni önerilen OTA yapıları ve eşdeğer klasik kaskod OTA'yla kurulan OTA-C entegratör frekans yanıtları çizilmiştir. Görüldüğü gibi, yeni yapılar çok düşük frekanslarda bile düzgün bir entegrasyon işlevine olanak sağlamakta, klasik kaskod OTA-C entegratör ise kHz bölgesinin altında işlevini görememektedir.

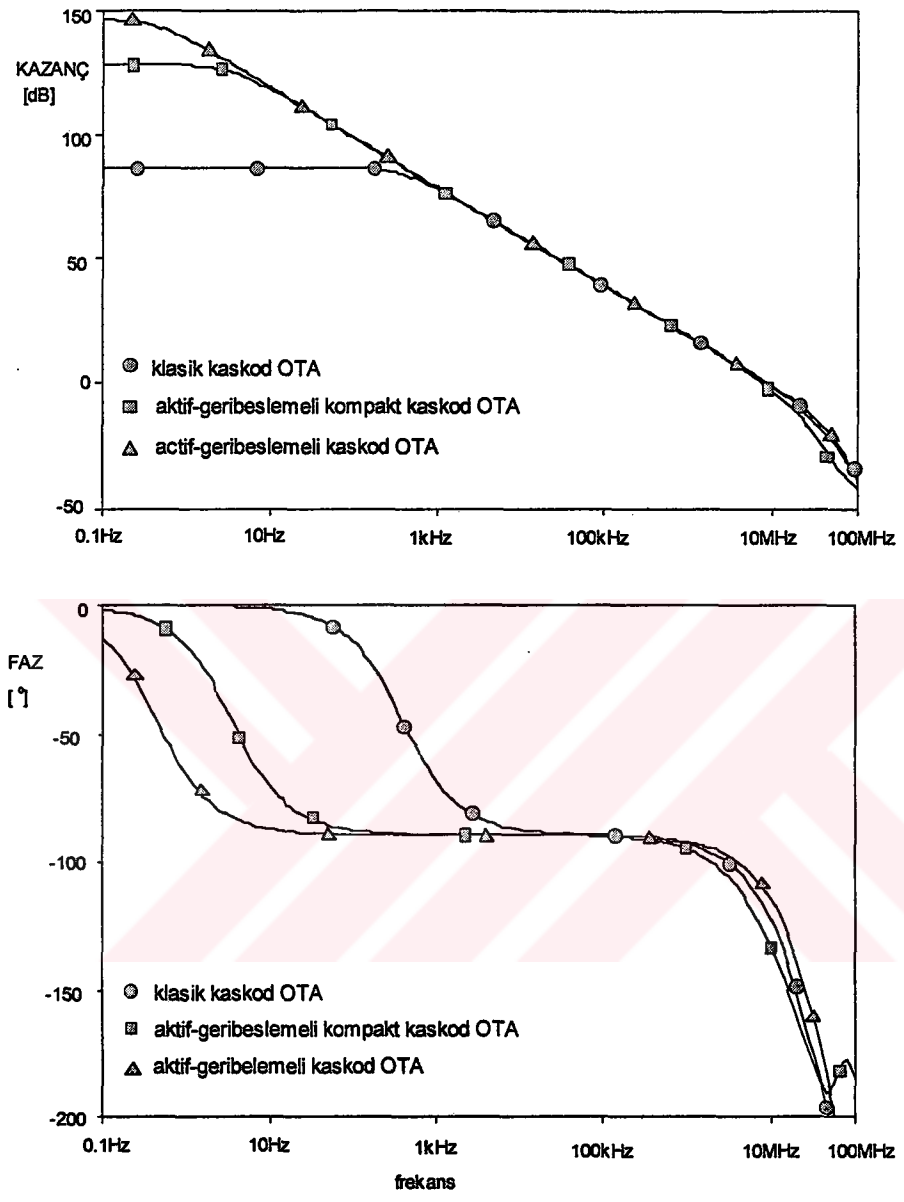
Yeni yapıların yüksek frekans davranışında klasik kaskod yapıya kıyasla belirgin bir bozulma olmaması bunların yüksek frekans uygulamalarına klasik yapılar kadar uygun olduğunun bir göstergesidir.

Tablo 1 Analiz edilen kaskod OTAların performans özellikleri (V_{DD}=-V_{SS}=5V).

	Klasik kaskod OTA	AGB kaskod OTA (Şekil 2)	AGB kompakt kaskod OTA (Şekil 1)
DC Kazanç	87.05 dB	146.4 dB	128.1 dB
GBW	169 MHz	209 MHz	49 MHz
R_{OUT}	388.4 MΩ	360 GΩ	41.5 GΩ
C_{OUT}	54.6 fF	44.2 fF	199 fF
f_{nd}	16.7 MHz	29.2 MHz	8.6 MHz
C_{Lmin}	498 fF	272 fF	933 fF
$PSRR_{DD}$	DC : 116dB f=1kHz : 116dB f=100kHz : 100dB f=1MHz : 83dB f=10MHz : 52dB	DC : 100dB f=1kHz : 115dB f=100kHz : 90dB f=1MHz : 67dB f=10MHz : 40dB	DC : 81dB f=1kHz : 96dB f=100kHz : 94dB f=1MHz : 66dB f=10MHz : 36dB
$PSRR_{SS}$	DC: 87dB f=1kHz : 87dB f=100kHz : 78dB f=1MHz : 61dB f=10MHz : 41dB	DC: 100dB f=1kHz : 115dB f=100kHz : 87dB f=1MHz : 67dB f=10MHz : 52dB	DC : 81dB f=1kHz : 96dB f=100kHz : 70dB f=1MHz : 50dB f=10MHz : 34dB
çıkış salınımı	-3.7 V ~ 3.6 V	-3.85 V ~ 3.85 V	-4.6 V ~ 4.4 V
$V_{off-set}$	110 μV	73 μV	4 mV
CMRR	87.3 dB	162.1 dB	120.8 dB
Güç sarfiyatı	0.58 mW	0.63 mW	1.15 mW



Şekil 3 Kuyruk akım kaynağı I_A için kullanılan yeni yapılar.



Şekil 4 Sunulan aktif-geribeslemeli OTAlar ve eşdeğer klasik kaskod OTA'yla kurulan üç OTA-C entegratörün frekans yanıtları (C_L=1pF).

CHAPTER 1

INTRODUCTION

The first bipolar junction transistor (BJT), thanks to its reduced power consumption and dimensions with respect to those of an electron tube, supplied its inventors, Shockley, Brattain and Bardeen, a Nobel Physics Prize. This invention was regarded as a great revolution in electronics in 1947. However, the real revolutionary developments started when it was noticed that the low power and small dimensions enabled more than one transistor be placed on the same semiconductor material, today called 'chip', on which resistors and diodes could also be formed. This was the birth of 'integrated circuits'(ICs). The first person to realize an IC was Jack S. Kilby, who managed to realize a phase-shift oscillator on a single chip. Then came Hoerni and Noyce, who introduced the planar transistor and utilized the planar technology in their company, Fairchild Semiconductors, to realize the first planar IC in 1961. In 1960 and 1962, first realizations of the metal-oxide-semiconductor field effect transistor (MOSFET) were also reported [1], [2]. Thanks to the advances in IC manufacturing technology, number of transistors that could be placed in a chip were almost doubling each year. Afterwards, the large scale integration (LSI) idea emerged, which was then suitable particularly for digital design. MOSFETs were much more suitable for large scale integration with respect to BJTs. This was because MOSFETs' structure was much simpler than the BJTs and therefore they could be made much smaller; moreover, the logical functions could be realized with less number of MOSFETs than BJTs. Then, the costs dropped sharply and a very rapid development period started in technology. This led to very large scale integration (VLSI). It was then, when the real high-tech products, like battery-operated pocket calculators and digital

the real high-tech products, like battery-operated pocket calculators and digital watches, microprocessors and mega-byte memory cells emerged. In the computer industry, the ultra-rapid development can be summarized in brief by comparing the integrated microprocessors of Intel. In the first integrated microprocessor chip '4004', which was introduced in 1971, there were 2300 transistors in a 2x2 mm^2 area. After only about 25 years, today, a 'Pentium Pro' microprocessor chip, which was introduced in 1995, employs 5.5 million transistors (cache memory discluded).

In 1970s, analog integrated circuits were mainly realized with BJTs. MOSFETs were rarely used, most of the time to make use of its very high input (gate) impedance. However, when 'complete-system' chips emerged, on which analog and digital circuitry of a system were fabricated together on the same chip, thanks to their high integration density, MOSFETs started to replace BJTs in analog IC applications. At first, higher mismatches, lower g_m for a certain bias current and worse 1/f noise performances of MOSFETs with respect to the BJTs were the most serious drawbacks. Today, these drawbacks are reduced satisfactorily and after the complementary MOS (CMOS) technology, MOS analog functional blocks show comparable and sometimes better performances in most of the applications, with respect to their bipolar competitors. Particularly, smaller area, lower power consumption and lower cost are very good reasons for use of MOSFETs. Furthermore, low-voltage low-power (LV-LP) analog techniques of the last decade [3], which mainly utilizes MOSFETs in weak inversion, are supporting the first place of MOSFETs in VLSI analog design.

The competition between analog and digital electronics seems to be won by digital electronics, especially in telecommunications (digital signal processing) and automation systems. However, since the real world is 'analog', there is still a great need for analog blocks in VLSI, at least for interfacing the digital signal processors with the real world. Use of analog filters are mandatory for analog-digital interfaces [4, p. xix], [5, p. 1], [6].

Direct implementation of discrete analog filters into integrated circuit design is not possible since an inductor with a reasonably high value cannot be achieved on silicon (Nevertheless, some IC-compatible inductors have been shown to be possible for the GHz range [7]). Active RC filters, are very good solutions in which lack of inductors are compensated for with operational amplifiers to achieve integration functions. However, when they are realized on a chip, many problems arise, especially those associated with area consumption, high tolerances and temperature dependency of on-chip passive resistors. Nevertheless, some solutions are available to overcome this problem, which will be mentioned later.

Fully-integrated active filters can be achieved with 'time continuous' (like active RC filters) and 'sampled-data' systems. Both types have some advantages and disadvantages over each other; for example, sampled-data filters enable low-distortion and accurate-response filtering with a small chip area consumption, but only for low-frequencies [4, p. 657]. Continuous-time filters can be used in high frequencies but require automatic tuning because of the significant deviations of filter responses due to process tolerances, temperature variations, parasitics, aging, etc [5].

The first fully-integrated signal processors were 'sampled-data' analog filters. This group includes 'switched-capacitor filters' and 'switched-current filters'. They make use of non-overlapping clock phases. In the switched-capacitor filters, the main frequency response characteristics (e.g. cut-off frequency and quality factor of a low-pass filter) are determined by two parameters, namely, the sampling clock frequency and the ratio of capacitors. The clock frequency and capacitor ratios are well controlled with sufficiently low tolerances (less than 5% is achievable) in an IC process, especially in the mature CMOS process. Moreover, these parameters are not affected by temperature and process parameter variations. This enables accurate filtering, thus automatic tuning is not required. When designed for low-frequencies, e.g. audio frequency region, parasitic capacitors have almost no effect on the filter

response, since the low-frequency gain is large enough to shunt the parasitic capacitors by the virtual ground supplied by the local feedback of the operational amplifiers. Moreover, total harmonic distortion is very low in these filters, owing to high linearity of the poly-silicon capacitors and the local feedback configuration of the operational amplifier, which keeps its input signal small [4, pp. 657-666], [6], [8], [9].

If, however, the frequency response of these filters is aimed to be moved towards higher frequencies, most of the mentioned advantages fade out. When entering the Mega-Hertz range, the drop in the performance is very sharp due to some problems. Before describing the most severe problems, it is worth explaining briefly a very important phenomenon, called 'aliasing'.

Sampling a continuous-time analog signal must be performed with a sampling frequency f_s larger than the Nyquist frequency, i.e. larger than 2 times the frequency of the highest spectral component of the input signal. Let's assume an audio signal to be sampled with f_s=40kHz. Since maximum audible frequency is about 15kHz, f_s is higher than $f_{Nyquist}$. Let's assume a spectral component of f_x=50kHz in the audio signal, which normally cannot be heard. Though it is away from 15kHz, after sampling, it is translated or 'aliased' into the base-band as $f_{alias}=|f_s-f_x|=10$kHz (Note that, another spectral component of f_y=30kHz could again cause a 10kHz aliased signal). Nevertheless, this problem can be solved by using anti-aliasing low-pass filters to band-limit the input signal [10], but in turn increasing area and power consumption [8].

Performance of switched-capacitor filters degrades abruptly at high frequencies due to finite GBW and finite dc gain of the operational amplifiers, finite switch resistances and clock-feedthrough. Also need for anti-aliasing and smoothing filters is a disadvantage. The most critical problems are listed and explained briefly below [4, pp. 657-666], [5, p. 2], [6], [8], [9], [10], [11], [12], [13], [14], [15], [16].

1- Because switched-capacitor filters are sampled-data systems, they require input anti-aliasing and/or output smoothing filters. This becomes a

great disadvantage about chip area consumption, when there are groups of filters in a chip, since each filter will need an anti-aliasing filter and/or a smoothing filter.

2- There is an unavoidable aliasing of the internal high-frequency (out of base-band) noise from operational amplifiers at each sampling. It is difficult to overcome this aliased noise.

3- Since high-frequency power supply rejection of the operational amplifiers is poor, high-frequency (out of base-band) noise from power supplies contaminates the signal, again by aliasing into the base-band due to sampling.

4- Clock-feedthrough, caused by switch charge injection, is signal-level-dependent and may cause distortion. As the sampling frequency is raised, its effects worsen further.

5- Mixing products and their harmonics created between the base-band input signal frequencies and the switching frequency can lead to great problems, especially in a chip employing other switching circuits with different switching frequencies or asynchronous clock rates (e.g. Modems).

6- If the base-band frequency is raised, the performance degrades sharply due to settling and slewing performance of the operational amplifiers and the finite switch resistances. The sampling frequency can be pulled down towards Nyquist frequency to relax the operational amplifiers, however, this brings the need for very-high-selectivity accurate anti-aliasing and/or smoothing filters, whose implementation is very critical.

7- The finite dc gain of the operational amplifier means a rather low high-frequency gain insufficient to keep high-frequency ac signals at the input of the operational amplifier small in amplitude with the aid of feedback. This results in degraded filter response accuracy.

The problems from which switched-capacitor filters suffer, like aliased noise, frequency limitations due to settling time of the active device, need to an anti-aliasing filter for each filter, clock-feedthrough, Nyquist order limitations, etc. and the sharp performance drops at frequencies higher than about 1MHz, bring the need of developing fully-integrated high-performance continuous-time

filters for many applications wherein sampled-data filters lack high performance. Therefore dense studies are being carried on this topic [5], [6], [8], [10], [11], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33].

It will be convenient to make a comparison of continuous-time and sampled-data filtering by supplying a one-to-one correspondence to each of the 7 items listed above about the disadvantages of the switched-capacitor filters:

1- Out of base-band frequencies are simply attenuated in continuous-time filters, without causing any problems, as long as the active devices are stabilized. An additional area consumption, however, does exist due to the automatic tuning circuit, but this is not as severe as it is in a group of switched-capacitor filters, because an entire continuous-time filtering system requires only one automatic tuning circuit [8], [17].

2- High frequency (out of base-band) noise from the active devices will not cause a significant problem in continuous-time filters; they are simply attenuated.

3- Similarly, high-frequency (out-of-band) power supply noise in continuous-time filters does not cause problems as serious as those in sampled-analog filters; it is normally not transferred into the base-band.

4- Some clock-feedthrough effects may occur in continuous-time filters too when a reference clock is used for tuning, however if the frequency of this clock is chosen outside the base-band, these effects can be made almost negligible [8].

5- Mixing normally does not occur in continuous-time systems since there is no switching, except that, noise in a complete-system induced mainly by switching of digital circuitry may produce some mixing products. However, continuous-time filters are 'totally innocent' in this process.

6- Though high-frequency effects start to show themselves at lower frequencies in continuous-time filters than in switched-capacitor filters (assuming that the same operational amplifier is used), the degradation of performance is

only gradual; not abrupt. Also, these frequency degradation effects can be compensated by using the conventional techniques which are applicable to classical active filters [8]. Furthermore, transconductance-capacitor (G_m-C) (sometimes called 'operational transconductance amplifier-capacitor (OTA-C)) filters have proven to be more suitable for higher frequencies, with respect to operational amplifier-based filtering techniques [9], [10], [17], [29], [28], [34]. Moreover, the recent rapid developments in current-mode continuous-time filtering techniques offer very-high-performance high-frequency filters [22], [28], [35], [36].

7- When an operational-amplifier-based active filter is considered, again virtual ground condition cannot be achieved at high frequencies due to the finite dc gain of the operational amplifier, causing frequency response error, [5, p. 2], [11]. However this problem is less severe in G_m-C filters since the active devices used in this type of filters (transconductors or OTAs) are used in local open-loop configuration.

Besides their advantages (especially in high-frequency applications) over switched-capacitor filters, fully-integrated continuous-time filters have many problems associated with the utilized continuous-time filtering techniques. Solutions of these problems rely on

i- advanced IC manufacturing techniques (to reduce device mismatches, parasitics and process parameter deviations)

ii- alternative VLSI-compatible high-performance continuous-time filtering techniques (e.g. recent current-mode filtering techniques [22], [28], [35], [36] is a very good example)

iii- advanced analog design techniques (to improve performances of the utilized active devices)

As mentioned before, conventional active-RC continuous-time filters cannot be realized in an integrated circuit efficiently, because, a passive resistor occupies a large area in the chip, has a large absolute tolerance, its value depends strongly on temperature, and available value range is not wide enough [34], [37],

[38]. Moreover, the devices are expected to be efficiently adjustable to enable external adjustment [9], [37], [34] or automatic tuning of the frequency behavior, which significantly declines from the desired response due to mismatches, device tolerances, temperature, aging, parasitics, process parameter variations, etc. [8], [11], [16], [17], [29], [39]. As a solution for this problem, MOSFET-C filters were introduced by Tsividis and Banu, where a MOSFET biased in triode region was used as an adjustable linear resistor to enable tuning [8], [13], [40], [41], [42].

Although MOSFET-C filters are fully-integrable, they have some important drawbacks like, bandwidth restrictions of the used operational amplifiers, the need for balanced input/output structures (for elimination of the nonlinear terms brought mainly by the MOSFET resistors) and the narrow adjustable range and adjustment inefficiency of the MOSFET resistors [10], [29], [43].

On the other hand, 'G_m-C filters', in which tranconductance stages (a transconductor or an OTA) are utilized as active devices, are much more advantageous with respect to MOSFET-C filters; particularly, wider bandwidth of a transconductor or OTA with respect to an equivalent operational amplifier is the most essential advantage [5], [10], [17], [21], [25], [26], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52], [53], [54], [55]. Others are, smaller chip area and lower power consumption, more efficient frequency response adjustment (via G_m, by varying a control voltage or control current), much wider adjustable frequency range (more than 4 decades is achievable), less number of active device requirement, simplicity of design (especially stability problems are less since transconductors and OTAs are generally used in local open-loop configuration), etc. [5], [9], [29], [34], [43], [56], [57].

What is the reason enabling G_m-C filters (or oscillators) be more suitable for high frequencies with respect to their operational amplifier-based counterparts? Actually the answer is not unique, however the answers are correlated to each other:

- In a G_m-C filter, input impedance of an integrator is capacitive; therefore, it is easy for a transconductance stage to drive an integrator. However, input impedance of an active-RC integrator is low, requiring low output impedance driver amplifiers [10], [55].

- A transconductor or an OTA is a current-output device, so, unlike an operational amplifier, it does not need an additional buffer stage (which brings additional nodes to degrade bandwidth and cause stability problems) to convert its high output impedance to a low impedance level [17].

- Since active devices (transconductance stages) in a G_m-C filter are generally used in local open-loop configuration, they don't need compensation (which is achieved by creating an 'artificial' low-frequency dominant pole; e.g. Miller OTA) which degrades bandwidth [58].

- A transconductance stage generally possesses a single dominant pole, which comes from the output node as $f_{dp}=(2\pi R_{OUT}C_{OUT})^{-1}$, where R_{OUT} and C_{OUT} are output node resistance and capacitance, respectively [4, p. 480]. In a G_m-C integrator structure, a load capacitor C_L is connected at the output to perform integration function. This means that, ultimately, a transconductance stage can be used down to its gain-bandwidth (GBW) frequency as an integrator, provided its parasitic output capacitance is utilized as C_L [17], [58]. However, for an operational amplifer to be functional in an active-RC integrator, it must have a sufficiently large voltage gain, e.g. at least 30dB, to achieve the virtual ground with aid of local-feedback. This means that, an operational amplifier in an active-RC filter can be utilized only up to the limit GBW/30 [5].

It must be mentioned that the terms 'G_m-C' and 'OTA-C' are generally used interchangably, which is actually wrong. A transconductance stage is a voltage-controlled current source (or voltage-to-current transducer) which is expected to handle large input signals linearly, i.e. with a constant transconductance (the transconductance value is very important since the filter response depends directly on it). An OTA, on the other hand, is basically an operational amplifier without a low-impedance output stage and acts like an

operational amplifier in local feedback configuration in many applications (e.g. Miller OTA); a large-signal transconductance is irrelevant unless the high voltage gain is lowered [17].

OTA-C filters utilize linearized OTAs (i.e. input stage is a transconductor with low gain to achieve a usable large signal transconductance) as transconductance stages, thus they are transconductance-C filters too; however, converse is not always true. Filter responses depend on the transconductance of the OTAs which are expected to be sufficiently constant for large signals, therefore, those OTAs which are suitable for OTA-C filters should be prefered (e.g. symmetrical OTA) and throughout this text, dominantly those type of OTAs are considered.

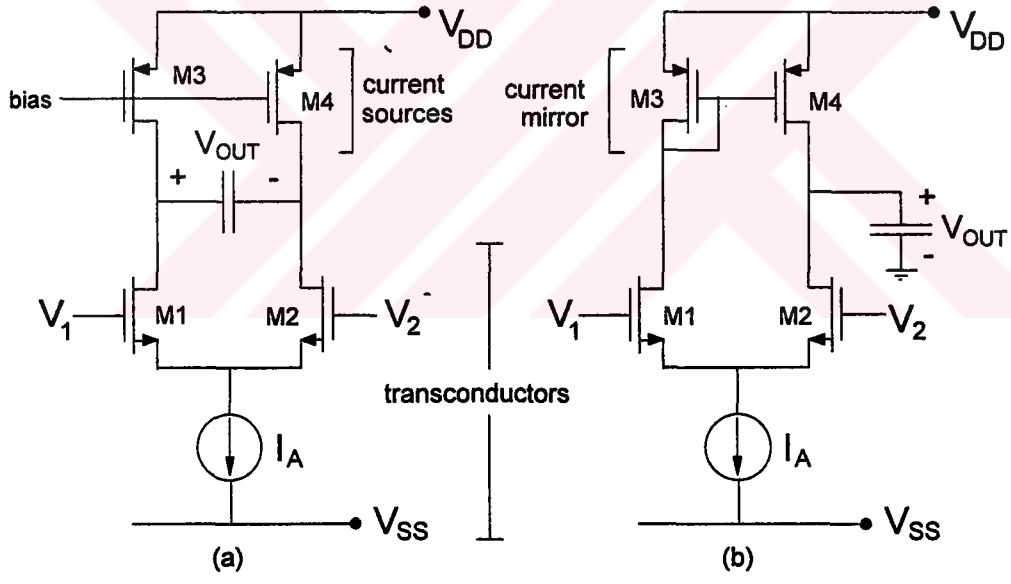


Figure 1.1 Simple transconductance-C integrators: **(a)** balanced **(b)** unbalanced.

The input stage of an OTA is a transconductor and the remaining stages are mainly current mirrors to reflect or invert (with or without amplification) the input-voltage-dependent differential current of the transconductor to obtain a single-output. The simplest transconductance-C integrators are shown in Figure 1.1, which utilize a long-tailed pair as a transconductor. These integrators are sometimes referred to as 'transconductor integrators', and sometimes as 'OTA

1.1, which utilize a long-tailed pair as a transconductor. These integrators are sometimes referred to as 'transconductor integrators', and sometimes as 'OTA integrators'. Though this makes it hard to make a distinction between a transconductor (for example a long tailed pair, like the one in Figure 1.1) and an OTA, it can be mentioned that a transconductor has a simpler structure with respect to an OTA. Nevertheless, they act very similarly in G_m-C filters. Therefore, the distinction is not so important from G_m-C filters point of view.

Linearity of an OTA very strongly depends on the linearity of its transconductor, which means that, linearity problems of particularly OTA-C, and generally transconductance-C filters are same, i.e. linearization techniques apply both. Though frequency behavior of an OTA is relatively worse, power and area consumptions are higher with respect to a transconductor due to use of additional blocks (mostly current mirrors), easily available multiple outputs (unlike voltage outputs, a current output can be replicated easily by using current mirrors), use of grounded capacitors in filter structures (thanks to the availability of a single dc-zero-Volt output) and the possibility to obtain a larger transconductance value for the same input linearity [9], [34], [37], [56], [59] are some advantages of OTA-based continuous-time filters over transconductor-based filters. Also, the large output impedance (which is required in a current-output device) can be achieved easier in OTA structures. Note that, when a linearization circuitry (which more or less degrades the bandwidth performance) is accounted for in the transconductance stage, bandwidth, power consumption and area advantages of a transconductor over an OTA can be claimed to be of less importance in most of the applications.

The mentioned advantages of OTA-C filters over other continuous-time filters yielded dense studies for building high-performance OTA-C filter (and oscillator) configurations in recent years [36], [43], [56], [60], [61], [62], [63], [64], [65], [66], [67], [68]. However, besides the advantages, there do exist some disadvantages of an OTA, influencing the filter behavior in undesired ways. The most important ones among these are, narrow linearity range of the input stage

(generally a long-tailed pair) and the finite output resistance. Linearity range of the long-tailed pair varies with the tail current (i.e. with G_m) and the nonlinear small-signal output resistance takes a different value as currents of the output transistors change. Due to these undesired properties, the following problems are frequently come across in OTA-C filters:

- Harmonic distortion is high due to the nonlinear I_{OUT}-V_{IN} characteristic, unless the differential input voltage is kept small in amplitude. Moreover, for large input signals, an 'equivalent' G_m (different from the small-signal G_m) which is dependent on amplitude of the differential input voltage appears, causing 'frequency distortion' in the filter response [9], [17], [37]. For example, a band-pass filter suffering from this problem may act as follows: When an input voltage of $1V_{p-p}$ with a frequency equal to center frequency of the filter is applied, the output may be $0.5V_{p-p}$; however, if the input amplitude is increased to $2V_{p-p}$, the output may drop to $0.3V_{p-p}$. This is called 'jump-resonance' effect and is a result of the mentioned process. A converse situation, which may happen due to the same problem, is appearance of a large-signal input voltage with a frequency outside the pass band of the filter, at the output.

- A load capacitor at the output node is charged and discharged by limited currents, thus at a limited rate, causing a slew rate limitation for the output voltage, depending on the value of the load capacitor and the maximum available output current (one of the transistors in a long-tailed pair is practically at cut-off out of the proper operating range, where the other one conducts the whole tail current, which is then reflected to the output node) [4, p. 510], [17], [37], [59].

- In the basic OTA-C integrator structure (1 OTA with 1 capacitor connected between the output node and the ground), output resistance cannot handle the load capacitor at low frequencies (for a typical case, upper limit of this low frequency range can well be the kHz range), since impedance of the capacitor increases as frequency decreases. This causes a lossy integration, in turn resulting in a frequency response degradation, especially in high-pass and band-pass filters [10], [11], [58], [59], [69], [70].

The aim of this work is to propose operational transconductance amplifier (OTA) structures more suitable for continuous-time OTA-C filters. Therefore, the most critical properties of OTAs affecting the non-ideal behavior of an OTA-C continuous-time filter are investigated. Conventional techniques/structures reducing non-idealities are analyzed and their disadvantages and/or inefficiencies are revealed. Novel building blocks are proposed to eliminate the non-idealities in a more efficient way with respect to conventional techniques. Also, some modifications are suggested for several advanced structures to increase their efficiencies in reducing non-idealities.

CHAPTER 2

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The operational transconductance amplifier (OTA), whose circuit symbol and ideal equivalent circuit is shown in Figure 2.1, is an active device with the defining equations,

$$I_{OUT} = G_m (V_p - V_n) \tag{2.1}$$

and

$$I_p = 0 \quad , \quad I_n = 0 \tag{2.2}$$

where G_m is the transconductance of the OTA, and I_p and I_n are the currents of the non-inverting and the inverting input terminals, respectively. Ideally, G_m has a constant value; nevertheless, in many applications, this value is adjustable to achieve several required G_m values in those applications, e.g. to adjust the cut-off frequency of an OTA-C filter [5], [9], [34], [37] or oscillation frequency of an OTA-C oscillator [43], [68]. This adjustment is also required for automatically adjusting the frequency response of a continuous-time active network, after the chip is manufactured. Because frequency response of a continuous-time system declines from the aimed response due to active device non-idealities, transistor and capacitor mismatches, parasitics, temperature, aging, process parameter variations, etc., this automatic adjustment (tuning) is very important [8], [11], [16], [17], [29], [39]. The adjustment is generally performed by changing the bias point of the transconductance stage with the aid of a control current or control voltage [43], [51], [72], [73], [74], [75], [76], [77],

[78], [79]; also, voltage-controlled or current-controlled current mirrors are utilized in some applications [80], [81] to adjust the outgoing current, thus G_m. Microprocessor-controlled transconductance adjustment schemes have also been reported [71]. Therefore, unlike conventional approaches, in this work, showing a certain adjustment method (e.g. an adjustable voltage source, etc.) on the circuit symbol is avoided; instead, only an 'adjust' terminal is assigned.

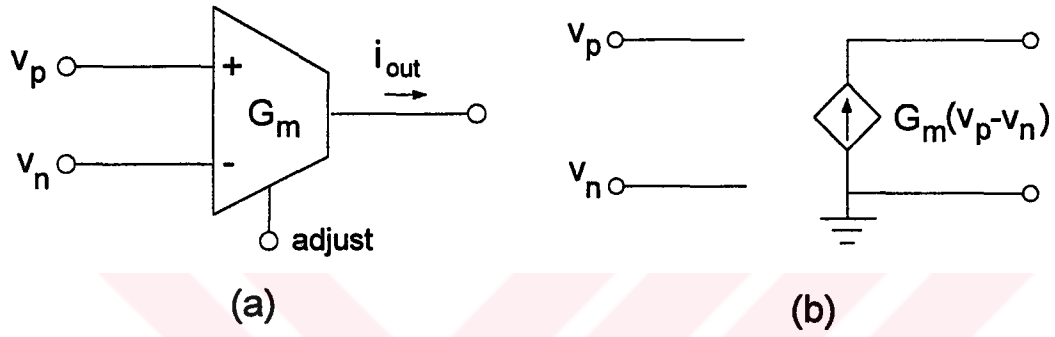


Figure 2.1 (a) circuit symbol of OTA, (b) ideal equivalent circuit of OTA.

The input stage (transconductor) of an OTA is generally a long tailed pair (LTP). The simplest CMOS OTA employing an LTP as a transconductor has already been given in Figure 1.1.b, with a capacitive load. When MOSFETs are used as the input devices, defining equations given by Eqn. 2.2 are satisfied almost ideally for a wide range of applications, since input current of a MOSFET is practically zero; except that a current will flow for the transient and very high frequency cases [17].

The defining equation given by Eqn. 2.1, however, is satisfied only for small signal cases. Ideally, G_m is expected to have a constant value for a wide input voltage range (input voltage: $V_{IN}=V_p-V_n$). This implies a constant slope for the I_{OUT}-V_{IN} curve for every V_{IN} value. However, for the long tailed pair, generally this cannot be achieved satisfactorily [59]. Since, unlike operational amplifiers, OTAs are usually used in local open-loop configurations, $V_{IN}=V_p-V_n$ can take large values, in turn bringing severe nonlinearities to the behavior [4, p. 466], [9].

2.1 INPUT LINEARITY RANGE of the LONG TAILED PAIR

Large signal transconductance of a CMOS long tailed pair (the 'transconductor' in Figure 1.1), is defined as

$$G_m = \frac{I_{D1} - I_{D2}}{V_1 - V_2} \tag{2.3}$$

and the small signal transconductance can be expressed as

$$G_m = \sqrt{2kI_A(W/L)} \tag{2.4}$$

where I_A is the tail bias current, $k=\mu C_{ox}/2$ is the transconductance parameter and W/L is the aspect ratio for the input transistors. For the LTP to operate properly (for both transistors to conduct) input voltage difference should remain within a range that can be expressed as [12], [59], [82], [83]

$$|V_{IN}| \leq \sqrt{\frac{2I_A}{k(W/L)}} \tag{2.5}$$

which can be rewritten as

$$|V_{IN}| \leq \sqrt{2}(V_{GSQ} - V_T) \tag{2.6}$$

where V_{GSQ} is the quiescent gate-source voltage for the input transistors. It is important to note that, this range is not necessarily the 'linearity range' of the LTP; it is only that range within which both input transistors conduct. Outside the range given by Eqn. 2.6, one of the input transistors is in cut-off and the other one takes the whole tail current I_A. Some nonlinearities do exist within this range which cause high harmonic distortion. It can be verified by analysis that for a

linearity error less that 1%, the differential input voltage must be kept within the range [12], [83]

$$|V_{IN}| \leq 0.28(V_{GSQ}-V_T) \tag{2.7}$$

The important point here is that, this linearity range is directly proportional to the 'proper operating range' given in Eqns. 2.5 and 2.6, thus, increasing the latter for the LTP will increase the former.

Many works using several techniques for linearizing LTP have been published which have been summarized and/or compared elsewhere [4, pp. 772-776], [5, pp. 15-45], [9], [29], [54], [84]. However, because of the creation of several additional internal nodes due to added devices/blocks for linearization, the proposed circuits' bandwidths are generally rather narrower than that of basic LTP [9], [55]. Therefore, linearization of LTP using those techniques has been assumed non-existent for a while at this stage; instead, input linearity range of basic LTP has been aimed to be widened as much as possible. It is obvious that the results of this process will help further widening of the linear range obtained by most of the advanced linearization techniques.

According to Eqn. 2.5, input linearity range of LTP (because linearity range is directly proportional to the proper operating range, as mentioned above) can be widened by increasing the tail current I_A and/or decreasing the aspect ratio $(W/L)_i$ of the input transistors. The analyses carried out have shown that the most suitable method is to keep I_A fixed and decrease the $(W/L)_i$ ratio (i.e. increase V_{GSi}), which has already been mentioned elsewhere [9], [12], [82], [83], [86]. Unfortunately, in this case G_m drops according to Eqn. 2.4. Note that this means a reduction in the voltage gain of the transconductor, thus the OTA; a requirement in an OTA for a usable G_m, which has already been mentioned in the first chapter. Widening the linearity range of an OTA is reasonable only when G_m is kept at the same value as before linearization. Therefore, the linearization procedure described above for the LTP seems inefficient at the first look.

Nevertheless, this problem can be solved in the simple symmetrical OTA easily [4, pp. 575-591], [59].

2.2 SIMPLE SYMMETRICAL OTA

For the simple symmetrical OTA of Figure 2.2, maximum current available at the output is BI_A, which determines the slew rate behavior of the circuit when a capacitive load is connected at the output node. Transconductance for this circuit can be expressed as

$$G_m = B\sqrt{2kI_A(W/L)} \tag{2.8}$$

where $k=\mu C_{ox}/2$ is the transconductance parameter for the input transistors M1-M2 and W/L is the aspect ratio for the same devices.

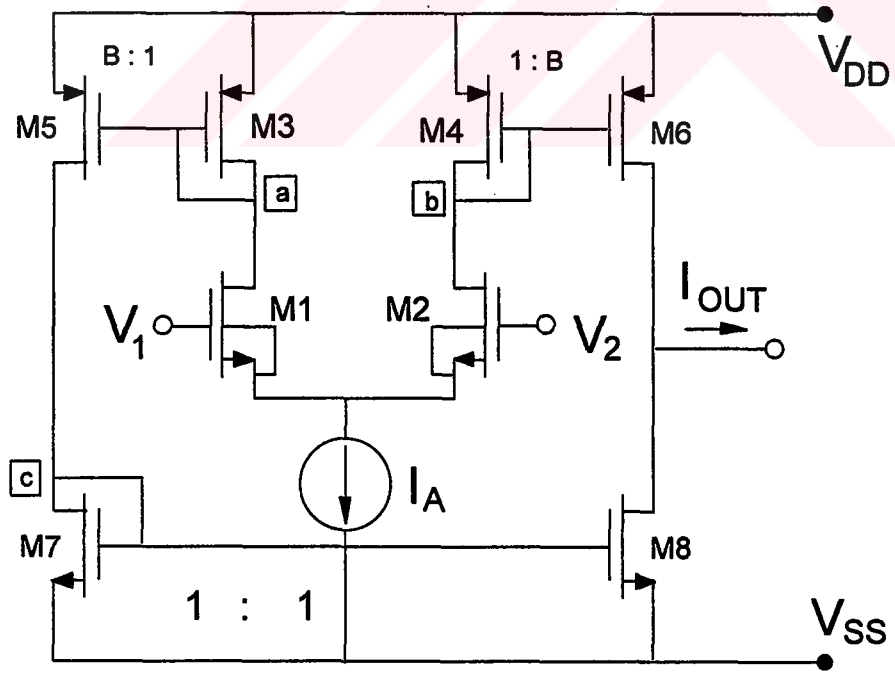


Figure 2.2 Simple symmetrical OTA.

If the effective capacitance at the output node (including a capacitive load and the parasitic output capacitance) is to be called C_L, then the slew rate can be given as

$$SR = \frac{BI_A}{C_L} \tag{2.9}$$

On the other hand, output resistance can be approximated as

$$R_{OUT} = \frac{1}{BI_A(\lambda_P + \lambda_N)} \tag{2.10}$$

where λ_P and λ_N are channel length modulation parameters for the output transistors M_6 and M_8, respectively.

Comparing Eqns. 2.4 and 2.8, one can easily notice that the drop in G_m (because of the drop in $(W/L)_i$ due to linearization) can be compensated by increasing B. This will improve slew rate according to Eqn. 2.9. However, it's a great disadvantage that output resistance R_{OUT} will decrease by the same ratio, according to Eqn. 2.10. Output resistance of OTAs is very important in OTA-C filters and oscillators for achieving lossless integration function at low frequencies. A lossy integrator possesses low-frequency phase error and causes errors in frequency responses, like quality factor degradation, cut-off or center frequency shift, gain error in the pass-band [9], [10], [11], [58], [85] or insufficient attenuation at reject-band [33], [59], [69] in continuous-time OTA-C filters. This problem can be overcome by using cascode output stages [4, p. 583], [12], [87], [88], however output voltage swing gets narrower in that case. Furthermore, positive common-mode input voltage restrictions exist because of similar effects caused by the additional load transistors inserted in the LTP stage (assuming classical double cascode current mirrors are used for high accuracy) [59], [69].

2.3 IMPORTANT FEATURES of an OTA

It has already been shown that the linearity, tunability, bandwidth, slew rate and output impedance of an OTA are of great importance. If the commonly used symmetrical OTA is considered, the most important features that must be considered in general for an OTA are those associated with

1) linearity and slew rate
2) bandwidth and stability
3) noise behavior
4) output resistance
5) common-mode rejection ratio (CMRR) and offset
6) power supply rejection ratio (PSRR)
7) input common-mode range
8) output voltage swing
9) parasitic capacitances
10) temperature dependency of G_m
11) effective adjustment of G_m
12) power consumption
13) chip area consumption
14) simplicity of design
15) compatibility with VLSI processes

It must be noted that, these features are not necessarily in the order of importance, since the order of importance differs significantly depending on the application wherein the OTA is to be used; besides filters and oscillators, OTAs are used in a large variety of applications [57], [89], [90], [91]. The first 11 features cannot be achieved in the desired way satisfactorily in a classical OTA since all of them are generally influenced by various effects. Therefore, advanced design and IC manufacturing techniques are required to reduce those effects as much as possible. The remaining features (items 12-15), on the other hand, are strongly affected from those design techniques introduced to overcome

the problems associated with the items 1-11, such that, an advanced structure for achieving improved features will probably increase, for example, power and area consumption and complexity of design of the OTA. Moreover, even if it brings superior improvements in most of the features, if it is not VLSI-compatible, it cannot have a chance for wide application. Also, some trade-offs exist between some of the features, i.e. improvement in one degrades the other, and vice versa. It will be helpful to describe briefly each of the above features, the expectations associated with them, the source of the undesired effects influencing them and some apparent-at-first-look solutions for minimizing those effects. The commonly used symmetrical OTA of Figure 2.2 will be considered for some of these considerations, when necessary.

2.3.1 Linearity and Slew Rate

It has already been mentioned in Section 2.1 that linearity of an OTA depends dominantly on the linearity of the input stage. Typical I_{OUT}-V_{IN} characteristics of an LTP input stage is given in Figure 2.3 for various G_m values. It is apparent from the figure that the linearity range is very narrow, especially for low G_m values. It has been already mentioned in Sections 2.1 and 2.2 that the linearity range can be widened by choosing W/L ratio of the input transistors small and $B>1$ such that the same transconductance value is achieved. Slew rate, on the other hand, as expressed by Eqn. 2.9, is B times larger than the previous case, for the same G_m. Figure 2.3.a shows the OTA I_{OUT}-V_{IN} characteristic before the mentioned linearization scheme ($B=1$) and Figure 2.3.b shows the the result of such a scheme, wherein $(W/L)_i$ is decreased and B is increased. This procedure may seem as if it carries the potential to solve the linearity and slew rate problems by using very long input devices and very large B values. However, first of all, even if the linearity could be achieved for the whole differential input voltage range, i.e. within $|V_{IN}| \leq V_{DD}+|V_{SS}|$, slew rate will have an ultimate limit for a certain G_m, such that

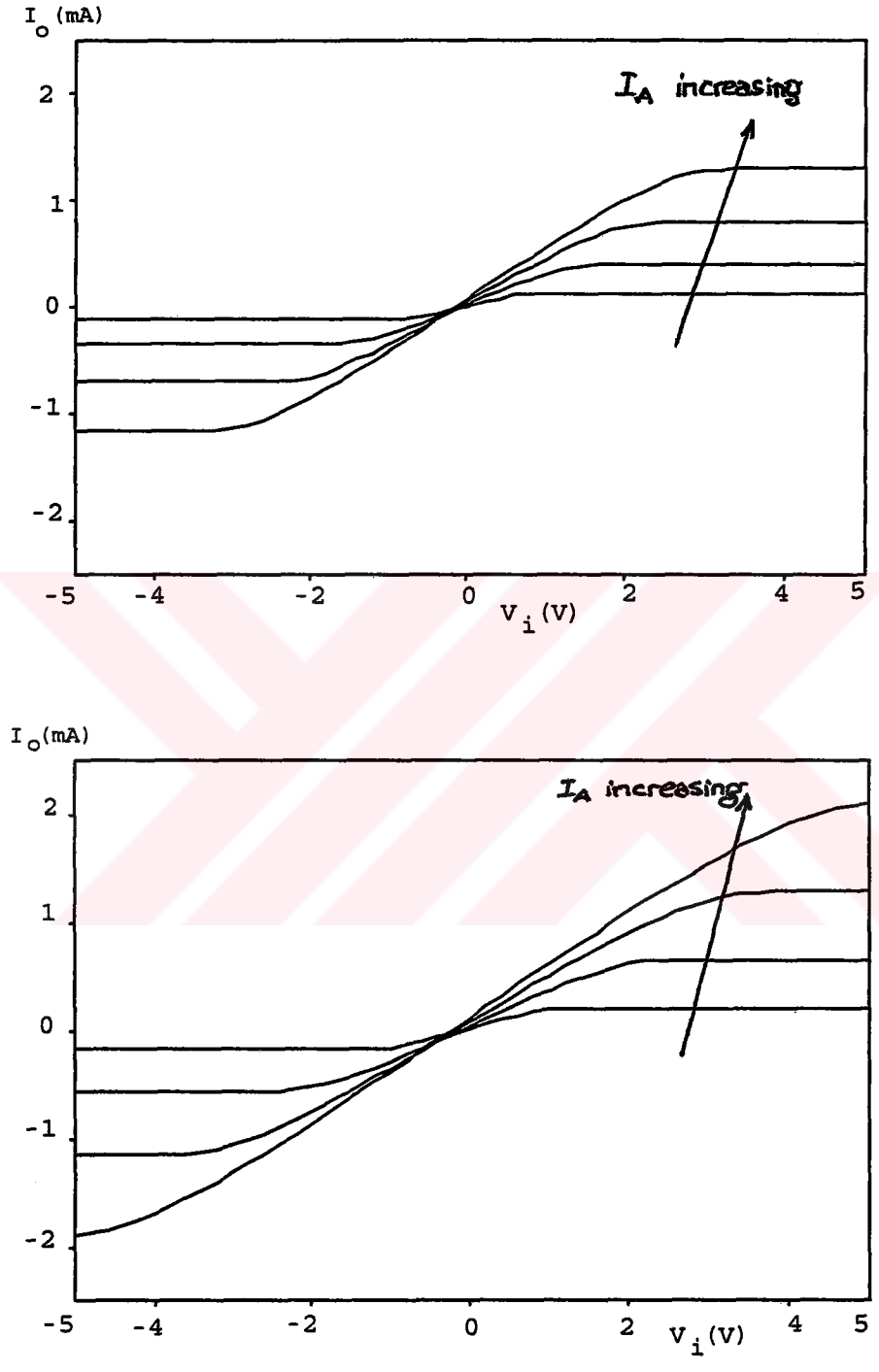


Figure 2.3 Typical I_{OUT}-V_{IN} curves of a symmetrical OTA employing the long tailed pair as its input stage: **upper curve:** $(W/L)_i$=30μm/5μm, B=1, **lower curve:** $(W/L)_i$=15μm/5μm, B=1.41. (I_A is parameter)

$$SR_{max} = \frac{I_{OUTmax}}{C_L} = \frac{G_m |V_{IN}|_{max}}{C_L} \tag{2.11}$$

Though some non-saturated and/or class AB input stages can increase the slew rate very sufficiently [29], [92], [93], [94], these solutions are restricted to operational amplifiers since in such stages the G_m is low for small signals and very high for large signals, yielding a very nonlinear input stage characteristic, which is avoided in OTAs. On the other hand, very long input devices degrade the bandwidth and noise behavior of the LTP [40], [87] and very large B values increase power dissipation and chip area a lot. Furthermore, B cannot be increased too much (in practice, $B<5$), otherwise the phase margin of the symmetrical OTA gets critically small [4, p. 579], as will be mentioned in the next sub-section. These considerations show that the symmetrical OTA with a current amplification of B, helps widening of the linear range to a limited extent, and it is less suitable for small G_m values than for large G_m values, as is apparent from Figure 2.3.

2.3.2 Bandwidth and Stability

The dominant poles in an all-transistor circuit comes from the high impedance nodes, assuming that all parasitic node capacitance values are the same order. As can be observed from Figure 2.2, all of the nodes are at low impedance levels, except that the output node is at high impedance level. This means that, a dominant pole will come from the output node as

$$f_{dp} = \frac{1}{2\pi R_{OUT}(C_{OUT}+C_L)} \tag{2.12}$$

where C_{OUT} is the parasitic output capacitance of the OTA and C_L is the load capacitance. Since this OTA acts like a single-pole amplifier, gain-bandwidth product (GBW) can be obtained as

$$GBW = A_v f_{dp} \tag{2.13}$$

where A_v is the dc voltage gain of the OTA which can be expressed as

$$A_v = G_m R_{OUT} = B\, g_{m1} R_{OUT} \tag{2.14}$$

where g_{m1} is the transconductance of M1. Then, GBW is obtained as

$$GBW = \frac{B\, g_{m1}}{2\pi(C_{OUT}+C_L)} \tag{2.15}$$

The non-dominant poles are significantly away from the dominant pole, however they cause excess phase shift which must be kept as low as possible so as to obtain a reasonably large phase margin.

The non-dominant poles from nodes **a** and **b** are equal and since each carries half of the output signal but in opposite phases, together they form a single non-dominant pole as

$$f_{ndpa} = \frac{g_{m3}}{2\pi C_a} \tag{2.16}$$

where C_a is the parasitic node capacitance at node **a**. Finally a pole comes from node **c**. However, because this node carries only half of the output signal, a zero is created at twice the pole frequency [4, p. 579]. Therefore, the effect of node **c** on the gain and phase response can be neglected. Thus, the phase margin (PM) can be approximated as

$$PM = 90° - \arctan\left(\frac{GBW}{f_{ndpa}}\right) = 90° - \arctan\left(B\frac{g_{m1}}{g_{m3}}\frac{C_a}{C_{OUT}+C_L}\right) \tag{2.17}$$

It is important to note that g_{m1}/g_{m3} is the voltage gain of the input stage, with M3-M4 as its diode-connected loads. This gain must be made low enough

to achieve a sufficiently wide input linearity range, as mentioned before [17]. Fortunately, this gain reduction for linearity helps keeping PM large, as can be viewed from Eqn. 2.17. However, for a good noise performance, this stage must perform some amplification [4, p. 581]. Therefore, increasing PM by sizing the devices M1-M2-M3-M4 is limited. It is obvious that B must be kept as low as possible for a large PM. Again, this brings a trade-off between stability and slew-rate/linearity requirements. Since normally C_L is constant, it cannot help increasing PM. C_a, on the other hand, is a small parasitic capacitance whose order of value is difficult to decrease further by a reasonable amount. Therefore, a compromise must be made between slew-rate/linearity and PM; e.g. $g_{m1}/g_{m3}=3$ and $B=3$ may be a good compromise for general cases.

It is interesting to note that, if G_m of the OTA is aimed to be changed (most generally by varying the tail current I_A), both g_{m1} and g_{m3} change by the same factor, i.e. by $(I_{Anew}/I_{Aold})^{1/2}$. Then, PM remains almost same for any G_m value, provided that C_a does not depend on bias conditions strongly.

Another point is that the above considerations about stability is done for C_L values which are mostly input capacitance value of the next amplifier. However, in OTA-C filters and oscillators, C_L, which enables integration function with an OTA, is a 'manufactured' capacitor with values relatively larger than input capacitance of an amplifier. Therefore, as long as additional low-frequency (on the order of GBW or lower) non-dominant poles are not created by introducing more complicated OTA structures than the symmetrical OTA, stability problems are relatively relaxed in OTA-C continuous-time filters.

Actually, apart from the case wherein an OTA is used in local unity gain feedback configuration (to obtain an active resistor), OTAs are generally used in local open-loop configuration in OTA-C filters or oscillators. Therefore, stability problems are usually not serious. However, a very important point is that, in an integrator structure, the phase errors are aimed to be kept low to achieve the overall filter response with low error. Therefore, the phase of the integrator transfer function should remain fixed at 90° for the whole frequency range. This is violated by the non-zero dominant pole at low frequencies and finite

non-dominant poles at high frequencies. This means that, for a C_L value, the dominant pole frequency must be kept as low, and the non-dominant pole frequencies as high as possible. This obliges keeping R_{OUT} as high as possible (to achieve a low dominant pole), and keeping PM as close to 90° as possible. The latter condition is appreciated in an operational amplifier too, but in stability point of view. In an OTA to be used in OTA-C active networks, however, a large PM is a need for precision filtering.

2.3.3 Noise Behavior

In the symmetrical OTA, the input-referred noise is inversely proportional to g_{m1}/g_{m3} and B [4, p. 581]. Therefore choosing both as large as possible helps reducing noise. However they must not be too large so as not to cause a severe reduction in PM, according to Eqn. 2.17. A good compromise is again to choose both around 3.

2.3.4 Output Resistance

Output resistance of the symmetrical OTA of Figure 2.2 is determined by the bias current and channel lengths of the output devices. The reasons why R_{OUT} of OTAs should be kept as high as possible in OTA-C active networks has been explained several times in the preceding sections. Reducing the bias current (BI_A) increases R_{OUT} according to Eqn. 2.10, however, then slew rate and linearity degrades. Choosing long channel output devices can also help but is not efficient enough for simple current mirrors; also excessively long channels worsen high frequency behavior [40], [87]. Therefore, use of cascode stages is unavoidable [4, p.583], [12], [34], [87]. They can also reduce the parasitic output capacitance significantly [95]. However, output voltage swing is thus restricted; also, - if conventional double cascode current mirrors are utilized for high accuracy - positive input common-mode voltage is restricted heavily (the amount of this degradation will be mentioned in the next sub-section) [59]. These

problems should be solved by suitable structures such that, output resistance can be increased satisfactorily with no serious degradation in common-mode input range and output voltage swing.

2.3.5 Common-mode Rejection Ratio (CMRR) and Offset

Differential nature of the input stage enables an OTA or operational amplifier to suppress the external noise induced on both inputs commonly, as long as common-mode rejection ratio (CMRR) is high. CMRR is the measure of how larger the differential voltage gain is with respect to the common-mode voltage gain. It can be kept sufficiently high, provided that M1-M2 and M3-M4 match perfectly and I_A is a high impedance current source [4, p. 544], [96]. In practice, an imbalance in the differential nature (device mismatch) causes some common-mode signals, and thus external noise to pass through the amplifier, reach the output node and contaminate the output signal.

The 'random' offset is again caused by mismatches among matched transistors [96]. It cannot be predicted but can be minimized with careful layout design, e.g. by using 'centroid layout' [4, pp. 553-555]. 'Systematic' offset depends on the design knowledge of the designer and can be made sufficiently small with design. However, some systematic offset terms remain due to current mirror errors, which are dominantly due to channel length modulation [97]. Since the simple current mirrors (M3-M5, M4-M6 and M7-M8 in Figure 2.2) suffer a lot from this effect, current mirrors with higher accuracy are required in OTA structures. Conventional double cascode current mirror is a very good solution for high accuracy, which also comes with a quite higher output resistance with respect to a simple current mirror, thus supplying the OTA with a much higher output resistance. However, it causes the maximum positive common-mode input voltage to be decreased by a gate-source voltage, due to the additional diode-connected MOSFETs coming in series to M3 and M4 in the simple

symmetrical OTA structure. Also output voltage swing is worsened 1 V_{GS} from the top and 1 V_{GS} from the bottom, because the output saturation voltage of a conventional cascode current mirror (NMOS) is $V_{DSsatU}+V_{GSL}$ (indices U and L represent the upper and the lower MOSFETs, respectively). Therefore, more efficient current mirrors with high accuracy must be developed.

2.3.6 Power Supply Rejection Ratio (PSRR)

PSRR is the measure of how larger the differential voltage gain is with respect to the power supply-to-output voltage gain. If it is large enough, the power supply noise (the spikes on the power lines which are mainly due to switching of digital or sampled-analog circuits in the same chip) cannot show itself at the output; it is suppressed [8], [9], [15], [16], [17], [29], [40], [98], [99]. Otherwise, this noise is coupled to the output node and contaminates the output signal. For example, in the Miller OTA, the compensation capacitor (to create a dominant pole for guaranteeing stability) which couples the gate and drain of the MOSFET of the second voltage gain stage, starts to exhibit a short-circuit behavior as the frequency increases; therefore, the power supply noise is directly coupled to the output node via low impedance of the diode-connected MOSFET. Thus, PSRR decreases linearly as the frequency (frequency of the power supply noise) increases. Unfortunately, high PSRR is required especially at high frequencies, since power supply noise is usually made of high-frequency spectral components.

It is well-known that, using cascode structures for ac decoupling of the amplifying stages from the power supplies yields sufficiently high PSRR values [4, pp. 585-587]. Also, in a Miller OTA, some simple techniques are available to prevent the compensation capacitance to short-circuit the input and output of the second gain stage at high frequencies [98], [99].

In the symmetrical OTA, as mentioned before, a dominant pole normally exists and no compensation is needed like the one in Miller OTA. However, at

high frequencies, the positive and negative power supplies are coupled to the output node via mainly C_{DS6} and C_{DS8}, respectively.

In some occasions where rejection of the power supply noise may still be insufficient (even if the PSRR seems to be large enough) fully-differential (differential input, differential output) balanced structures can be used, wherein, by taking the difference of the power supply noise from each symmetrical part (these noise signals are same in amplitude and phase in both parts) of the structure at the output node, full elimination of the power supply originated signals is possible [4, p.808], [5, pp. 45-59], [8], [16], [29], [40], [84], [100]. This technique, however, relies on perfect matching of transistors; mismatches in current mirrors cause an imbalance in the electrical behavior and then the improvement in PSRR is limited. Nevertheless, transistor mismatch errors can be kept within 1% by designing the transistors with relatively large aspects and utilizing centroid layouts, which was mentioned before.

An interesting point about PSRR is that, if the low-frequency PSRR (or dc PSRR) is high enough, it enables power supply flexibility for the circuit [101], which is very important in a portable equipment whose voltage of batteries decreases gradually during operation.

2.3.7 Input Common-mode Range

It has already been mentioned in the sub-section 2.3.5 that, the common signal components at inverting and non-inverting inputs of a long tailed pair are strongly rejected. However, those common-mode signals (or a common-mode dc voltage) may possess a sufficiently large amplitude or dc value to push the input stage to an undesired mode of operation. The positive maximum common-mode input voltage for the symmetrical OTA in Figure 2.2 is limited by the voltage drops across M3-M4, where the negative common-mode range is limited by the voltage drop across the input transistors and minimum compliance voltage of the tail current source I_A. Pushing the common-mode input voltage excessively towards V_{DD} causes M1 and M2 to enter the non-saturation (triode) operation

region, and pushing it excessively towards V_{SS} causes the tail current source I_A to lose its constant value (the output transistor enters the non-saturation region). Remembering that the minimum V_{DG} for a MOSFET to operate in saturation is $-V_T$, the common-mode range of the simple symmetrical OTA can be given as

$$V_{DD} - |V_{GS3}| + V_T \leq V_{INCM} \leq V_{GS1} + V_{Amin} + V_{SS} \tag{2.18}$$

where V_{Amin} is the minimum voltage across the tail current source I_A; if this current source is formed by a MOSFET with a fixed gate bias, then

$$V_{Amin} = V_{DSsatA} = V_{GSA} - V_T \tag{2.19}$$

If the current mirrors and the current source I_A are conventional cascode stages, it is obvious that the common-mode range given in Eqn. 2.18 worsenes approximately by $2V_{GS}$. Some cascode current mirrors with lower input and output voltage restrictions are available, but most of them has low accuracy.

2.3.8 Output Voltage Swing

As mentioned in some of the above sub-sections, the output swing of the symmetrical OTA depends on the type of current mirrors used to reflect the transconductor differential current to the output. Repeating the already-mentioned points is not necessary, so, it is enough to mention that output voltage swing is aimed to be maximized by using some novel current mirrors, which will be introduced in the next chapter.

2.3.9 Parasitic Capacitances

There are several types of parasitic capacitances in CMOS circuits. The oxide capacitances, junction capacitances, and interconnect capacitances affect the behavior of MOS functional blocks in a CMOS integrated circuit. A whole system (a complete-system chip in our case), however, is affected by the capacitances mentioned above, plus the bonding pad capacitances, the package pin capacitances and the protection circuitry capacitances [4, pp. 43-51]. These effects become severe as the frequency increases [8], [9], [17], [29], [40], [50]. The most important effects are bandwidth limitations and stability problems. Others are high-frequency noise (internal noise or power supply noise coupled to the output via parasitic capacitances) and frequency distortion (caused by nonlinear junction capacitances at the output node) [17]. Bandwidth and stability problems and some considerations/requirements for reasonable improvements have already been covered in preceding sections. High-frequency internal noise is of great importance in sampled-analog systems due to aliasing, however, in continuous-time systems, it does not cause a serious problem in most of the applications. Power supply noise coupling to the output by parasitic capacitances at high frequencies, however, may cause severe problems which obliges achievement of an improved high-frequency power supply rejection performance.

2.3.10 Temperature Dependency of G_m

This is a very important effect, originating from the temperature-dependency of the MOSFETs, capacitors and - in some occasions - passive resistors [8], [29], [30], [38], [75], [77]. As the ambient or chip temperature changes, only minute variations are expected from, for instance, an OTA-C filter response characteristics and performance. However, a significant deviation in frequency response always occurs in continuous-time filters due not only to temperature variations, but many other undesired effects, which have been repeatedly mentioned throughout this text. That deviation has to be compensated

by use of automatic tuning schemes [4, pp. 786-798], [5, pp. 203-205], [8], [17], [25], [29], [32], [33], [41], [43], [42], [102]. Nevertheless, dense investigations and advanced techniques to reduce the temperature-dependency of transistors, capacitors and some commonly-used blocks, have been reported [91], [103]. This work, however, will not cover the 'temperature-dependency reduction' topic.

2.3.11 Effective Adjustment of G_m

In most of the OTAs, adjustment of G_m is via I_A, and since a large dynamic range of currents are available at the output of a MOS current reference (e.g. from 1μA to 1mA, for strong inversion), adjustment range can be made sufficiently wide. However, in some applications, completely linear dependency of G_m on I_A or on a control voltage might be desired to obtain a more effective G_m-adjustment. Actually, the G_m-adjustment methods depend on the type of transconductor used. A transconductor whose transconductance cannot be adjusted electronically is almost useless in most of the OTA applications, therefore, this type of input stages must be avoided in OTAs.

2.3.12 Power Consumption

Power consumption in CMOS digital circuits is very low, enabling for example a calculator or a digital watch to operate for years with only a single lithium battery cell. Nevertheless, power consumption increases when a CMOS digital system is operated at high frequencies due to charging and discharging currents of the parasitic capacitors (for example, the microprocessors of today have cooling problems due to the excess heating caused by the clock-rates exceeding 100 MHz).

In analog integrated circuits, on the other hand, a significant power consumption always exists due at least to the bias currents. Even though

'dynamic biasing' techniques can help reducing the dc power dissipation significantly in some analog applications, ac power consumption will still exist.

Excess power consumption causes heating of the chip and as a result, many effects (associated with temperature dependency of active and passive devices) influence the circuit behavior in undesired ways, as mentioned in sub-section 2.3.10. Another important point is that, in portable equipments, wherein integrated circuits or systems are used very often, excess power consumption causes the battery life to be very short. Moreover, since the chip lies in a very compact package, continuous heating causes early aging of the chip. Therefore, power consumption in analog circuits should be kept as low as possible.

Additional blocks inserted in analog building blocks to compensate for some undesired effects do increase the power consumption. Nevertheless, as long as the level of performance improvement is high enough compared to the power consumption increment, this price is acceptable to be payed for high performance of an integrated system.

2.3.13 Chip Area Consumption

In a complete-system integrated circuit, the area occupied by the digital circuits and the capacitors is the dominant part in the total chip area. This means that, minimization of area occupied by analog circuits (excluding capacitors) is not necessarily essential. Therefore, advanced structures with larger transistors and additional blocks do not bring a severe problem about area consumption of the entire integrated system [9]; actually, increased parasitic effects and power consumption are much more important. Moreover, since there is a demand for low-voltage analog circuits in the last years [3], owing to the reduction of power supply standart of digital circuits in large systems from 5 Volts to 3.3 Volts (to reduce the power consumption of CMOS digital circuits operating at high frequencies), besides possessing low-threshold voltages, the MOSFETs have to be made larger to reduce the gate-to-source voltage drops. Consequently, if an advanced analog structure occupies a larger (e.g 50% larger) area than its

classical competitive, this increment in area consumption is not an important disadvantage to dwell on; a possible increase in power consumption and parasitics are of greater importance.

2.3.14 Simplicity of Design

An advanced analog structure must be easy to design; that is, its performance should not rely on critical absolute values or should not create severe trade-offs between its most important features. A structure with a wide design flexibility is appreciated. Also, a reasonable design plan should be easy to extract; complexity of design expressions and severe trade-offs can make such a plan very hard to obtain.

2.3.15 Compatibility with VLSI Technologies

A high-performance analog integreated structure may turn out to be totally useless, only because its performance relies on special features which are not available in VLSI technologies [8]. For instance, depletion-mode and multiple-threshold MOSFETs are normally not available in CMOS VLSI. Also, bulk-source shorting is normally not possible for n-channel devices in an n-well CMOS technology (the converse is valid for p-well), therefore it should be avoided in design. Actually, special features are realized in some applications, with additional process steps which increase manufacturing costs sharply.

CHAPTER 3

NOVEL STRUCTURES for IMPROVING OTA PERFORMANCE

In Chapter 2, the most important features expected from a high-performance CMOS OTA have been listed and explained. As can be noticed from those explanations, to overcome the problems associated with the mentioned features, an OTA requires primarily

1) a high-performance transconductor

2) high-performance current mirrors/sources

Additionally, improvements in IC manufacturing processes help some of the features to be satisfied more adequately.

The meaning of 'high-performance transconductor' for an OTA is primarily 'highly linear and effectively tunable transconductor'. There has been lots of work carried out to achieve transconductors possessing these properties; especially the long tailed pair has received many novel linearization/adjustment improvement techniques. Thus, the saturation point of linearity improvement has almost been reached for the long tailed pair. However, improvement of other performance characteristics of the OTA relying on performance of current mirrors seem to have a long way for reaching a saturation point. Therefore, precedence is given to obtaining advanced current mirrors/sources in this work, for improving most of the performance characteristics of OTA.

3.1 NOVEL CURRENT MIRRORS/SOURCES

The term 'high-performance' for the current mirrors utilized in an OTA generally points to a current mirror with the features listed below.

1) high current transfer accuracy

2) high output impedance

3) low input impedance

4) wide output voltage swing

5) low input voltage drop

6) large bandwidth

Of course, again, the listed features above are not necessarily in the order of importance. However, achieving each of the features for the current mirrors of an OTA within acceptable limits is very important to obtain high-performance OTA characteristics. It should be added that, while developing a high-performance current mirror structure, some additional features must be considered, which are expected from it very often, like,

- availability of multiple outputs
- minimal power consumption
- area efficiency
- wide dynamic range
- possibility of current transfer ratio adjustment by sizing transistors
- design simplicity
- compatibility with VLSI

Also, in some current mirrors where supply voltages are utilized, high PSRR and wide power supply flexibility are also desirable.

By reviewing the 15-item features list of the OTA, given in Section 2.3, one can easily conclude that, apart from the first feature (linearity and slew rate), all features strongly depend on performance of the current mirrors/sources employed in the OTA structure. The classical current mirrors (which are almost entirely implemented from bipolar current mirrors) cannot

achieve all of the important current mirror features required in OTAs. For instance, basic (simple) current mirror lacks high output impedance and accuracy, due to channel length modulation. By using a classical cascode current mirror, accuracy and output impedance can be increased significantly, but at the cost of degraded input and output voltage swings (1 V_{GS} of degradation for both). Some improvements are possible in the classical cascode current mirrors to reduce output and input voltage restrictions, but generally results in accuracy degradation.

In the following sub-sections, some widely used current mirrors (most of which are claimed to have improved performances in several ways) will be examined and their drawbacks will be revealed. Then, the developed novel current mirrors with higher performance characteristics will be introduced.

3.1.1 Classical Current Mirrors

3.1.1.1 Simple Current Mirror

The simplest current mirror is the simple (or basic) current mirror, shown in Figure 3.1. Assuming both transistors in saturation, strong inversion currents can be written as

$$I_{IN} = \tfrac{1}{2}\,\beta_1(V_{GS1}-V_T)^2 \qquad (3.1)$$

$$I_{OUT} = \tfrac{1}{2}\,\beta_2(V_{GS2}-V_T)^2 \qquad (3.2)$$

where $\beta_i = (W/L)_i\,\mu C_{ox}$, $i = 1,2$. Assuming $(W/L)_1=(W/L)_2$, i.e. $\beta_1=\beta_2=\beta$, the output current I_{OUT} will be exactly equal to I_{IN} according to Eqns. 3.1 and 3.2, because $V_{GS2}=V_{GS1}$. However, actually, the current of a MOSFET in saturation depends on the drain-source voltage too, due to channel length modulation effect [97].

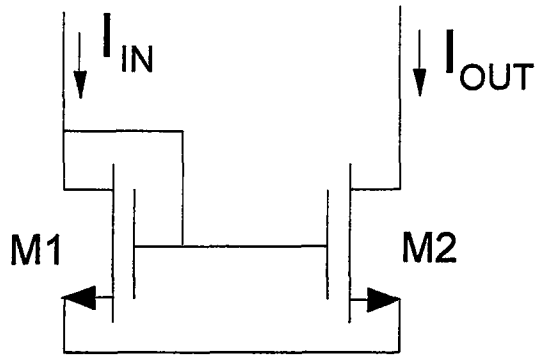


Figure 3.1 Simple current mirror.

To the first order of approximation, this dependence can be formulated as

$$I_D = \tfrac{1}{2}\,\beta(V_{GS}-V_T)^2(1+\lambda V_{DS}) \tag{3.3}$$

where λ is the channel length modulation parameter in $Volts^{-1}$. When Eqn. 3.3 is considered for the simple current mirror, the current transfer accuracy can still be kept high as long as

- λ is sufficiently small

or

- V_{DS2} is very close to $V_{DS1}=V_{GS1}$

Actually, the former condition can be reached for long channel lengths, however, it should be kept in mind that keeping the channel lengths excessively long may increase the accuracy, but worsenes the high-frequency behavior of the current mirror [40], [87]. The second condition, on the other hand, is not easy to achieve, because the output voltage $V_{OUT}=V_{DS2}$ cannot be determined by design; it is absolutely dependent on the load to which the output node is connected and the input current is reflected.

An error function for the current transfer ratio can be defined as

$$\varepsilon(\%) = 100\frac{I_{OUT}-I_{IN}}{I_{IN}} \tag{3.4}$$

Utilizing Eqn. 3.3, current transfer error for the simple current mirror (SCM) is found as

$$\varepsilon_{SCM}(\%) = 100\lambda \frac{V_{DS2} - V_{GS2}}{1+\lambda V_{GS2}} \tag{3.5}$$

If we assume a practical case wherein $\lambda=0.05\ V^{-1}$, $V_{GS2}=1.5$ V and $V_{DS2}=3$V, the error comes out to be 7 %, which is not a desirable feature for a current mirror to be used in an OTA. Note that this error increases as the difference between V_{DS2} and V_{GS2} increases.

Small-signal output resistance of a current mirror is defined as

$$R_{OUT} = \left(\frac{dI_{OUT}}{dV_{OUT}}\right)^{-1} \tag{3.6}$$

Using Eqn. 3.3, output resistance of the simple current mirror can be found as

$$R_{OUTSCM} = r_{ds2} \tag{3.7}$$

where r_{ds2} is the small signal output resistance of M2, which can be approximated as

$$r_{ds2} = (\lambda I_{OUT})^{-1} \tag{3.8}$$

Output resistance of the simple current mirror can be increased by choosing L_2 long, however, in practical cases where I_{OUT} is high, even this precaution is not enough.

If we assume a practical case wherein $\lambda=0.05\ V^{-1}$ and $I_{OUT}=50\mu A$, output resistance is found to be $R_{OUT}=400k\Omega$. If the OTA-C integrator

situation (mentioned in Chapters 1 and 2; particularly in Section 2.2) is recalled, for the integrator to be considered lossless at low frequencies, the output resistance of the OTA should be sufficiently larger than impedance of the load capacitor C_L, which is inversely proportional to frequency as

$$|Z_{CL}| = (2\pi f C_L)^{-1} \tag{3.9}$$

If a practical OTA-C integrator whose load capacitor is C_L=5pF, is assumed, with the OTA output resistance equal to the value found above (i.e. R_{OUT} = 400kΩ), it can be concluded that, the integration function cannot be achieved properly below 800kHz (the frequency value at which $|Z_{CL}|$ reaches $R_{OUT}/10$ is considered as the lossy-lossless boundary). An improvement can be achieved by choosing larger C_L values, but this is not a wise method, since achieving a lossless integration down to, for instance, 10Hz, requires a capacitor value of about 400nF, which is an impossible value to achieve on a reasonable chip area. A reasonable integration capacitor requires an OTA with a much higher output resistance. Therefore, the simple current mirror is generally not preferred in OTA applications, especially in the applications where high output resistance is mandatory (like output stage of the OTA).

The input resistance of most of the current mirrors are low enough for almost all analog applications; they are on the order of $1/g_m$, which is always satisfactorily lower than the output resistance of a preceding current source. g_m is the small signal transconductance parameter for the input transistor(s), which is defined as

$$g_m = \frac{dI_D}{dV_{GS}} \tag{3.10}$$

In most of the current mirrors, input stage transistors operate in saturation. Nevertheless, some of the recent current mirrors employ triode region transistors to reduce voltage drops [104], [105]. Therefore, a general g_m

expression for a MOSFET at the input stage of a current mirror is avoided to be given at this step.

For a current mirror, input resistance is defined as

$$R_{IN} = \frac{dV_{IN}}{dI_{IN}} \tag{3.11}$$

which takes the value $1/g_{m1}$ for the simple current mirror as proven below, using Eqn. 3.10.

$$R_{INSCM} = \frac{dV_{GS1}}{dI_{D1}} = \frac{1}{g_{m1}} \tag{3.12}$$

Since diode-connected M1 will always be in saturation unless it is in cut-off, by using Eqns. 3.1 or 3.3, R_{INSCM} can be expressed as

$$R_{INSCM} = \frac{1}{\beta(V_{GS1} - V_T)} = \frac{1}{\sqrt{2\beta I_{IN}}} \tag{3.13}$$

Though the effect of λ is neglected in obtaining g_m, Eqn. 3.13 is practically a very adequate expression to represent transresistance of a diode-connected MOSFET.

When $V_{OUT}=V_{DS2}$ drops below $V_{DSsat2}=V_{GS2}-V_T$, M2 enters the triode (non-saturation) region of operation, wherein Eqn. 3.2 is no longer valid. Therefore, the minimum output voltage V_{OUTmin} for the simple current mirror is

$$V_{OUTminSCM} = V_{DSsat2} = V_{GS2} - V_T = \sqrt{2 I_{OUT}/\beta} \tag{3.14}$$

This equation means that, as the output current increases, voltage swing at the output is restricted more. Nevertheless, it also points to a fact that, sufficiently low V_{OUTmin} values can be achieved for low currents (i.e. for V_{GS2}

values close to V_T). Actually, this is one of the most ultimate advantages of the simple current mirror over other current mirrors.

Finally, it is clear that input voltage drop V_{IN} can be given as

$$V_{INSCM} = V_{GS1} = \sqrt{2 I_{IN} / \beta} + V_T \tag{3.15}$$

Eqn. 3.15 means that, minimum achievable (achievable at low currents) voltage drop at the input of a simple current mirror is the threshold voltage, V_T, whose value is typically 1Volt. In fact, this is one of the problems which is not easy to solve for current mirrors, therefore this V_T limit is almost totally assented for strong inversion applications. However, there do exist some possibilities to lower this limit, which will be explained later. Nevertheless, this limit is much better than the lower limit in the classical cascode current mirror, which is $2V_T$, if body effect of the upper transistors is not accounted.

High frequency pole frequencies which determine the bandwidth of a current mirror can be determined from the small signal node capacitances and resistances. Assuming that the node capacitances are parasitic capacitances which are on the order of several fFs (10^{-15} Farads), dominant poles are created only at high impedance nodes. Usually, conventional current mirrors don't possess high impedance internal nodes. Therefore they continue exhibiting high performance at relatively higher frequencies.

The simple current mirror possesses only two nodes, namely, input and output nodes. The input node is at a low impedance level of $1/g_{m1}$. The output node, however, seems to be at a high impedance level, however, in most of the applications, it is to be connected to a load with an impedance sufficiently lower than the output impedance (otherwise proper operation cannot be achieved). Thus, both nodes may be at low impedance levels, therefore the dominant pole may come from the input or the output node, depending on the load and the driver circuitry.

In current output stages (like the output stage of the symmetrical OTA in Figure 2.2), the inverse is valid, where the output of the current mirrors are connected to each other [59], [69], [101], [106]. Then, the dominant pole, thus the bandwidth of the loaded current mirrors (this is also the bandwidth of the symmetrical OTA, as deduced in the sub-section 2.3.2) is determined by the output node capacitance. Therefore, a suitable current mirror to be used in an OTA should have a small output capacitance. The equivalent output capacitance is

$$C_{OUTSCM} = C_{GD2} + C_{DB2} \tag{3.16}$$

where C_{GD2} is dominantly the gate-drain overlap capacitance. Though it is connected in feedback configuration, due to Miller effect, it is reflected to the output by being multiplied by a factor $(1\text{-}1/A_{v2})$, where A_{v2} is the gain of the common source amplifier M2, which is negative and its absolute value is higher enough than unity. Thus, this factor is approximately 1. However, C_{DB2} is the dominant part of the output capacitance since it is the drain-bulk junction capacitance. Therefore,

$$C_{OUTSCM} \approx C_{DB2} \tag{3.17}$$

It was mentioned in the previous chapters that, in OTA-C filters, OTAs are mostly used in integrator configurations, that is, with a load (integration) capacitor at the output node. This integration capacitor is a highly linear and high-quality poly1-poly2 capacitor. Output capacitance of the OTA (which is the sum of output capacitances of the two complementary current mirrors employed in the output stage) must be sufficiently smaller than the integration capacitor. Since the dominant output capacitance of a simple current mirror is the drain-bulk junction capacitance, whose value is dependent on the output voltage, if this nonlinear capacitance is comparable with the integration

capacitor, equivalent integration capacitance changes significantly with output signal amplitude, in turn causing frequency distortion in the filter response [17]. This is another important reason for reducing the output capacitance of the current mirrors to be used in OTAs. Of course, since the value of the junction capacitance normally cannot be reduced with design, some alternatives, like cascode current mirrors, are preferred to decouple the output from that capacitance. As will be shown in the next sub-section, output capacitance of a cascode current mirror is quite reduced with respect to an equivalent simple current mirror.

As a consequence, it seems wiser to examine only the output capacitances of the current mirrors to get an idea about their high frequency potentials when utilized in an OTA, as long as they don't have internal high impedance nodes.

3.1.1.2 Classical Cascode Current Mirrors

Cascode current mirrors/sources are more desirable in analog applications owing to their higher output impedance and better accuracy performances, with respect to the simple current mirror.

In Figure 3.2, four classical cascode current mirrors are shown [4, p. 382], [96]. The first one in Figure 3.2.a is the classical double cascode current mirror (DCCM), which is obtained simply by connecting two simple current mirrors one over the other, in other words, in a cascode configuration. Its most desirable advantages are, high current transfer accuracy and higher output resistance and smaller output capacitance with respect to a simple current mirror. However, some prices are paid due to the doubling of the input and output devices, which will be explained shortly.

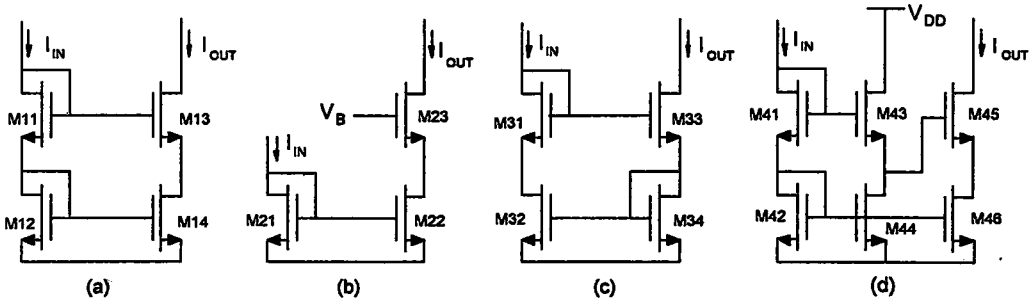


Figure 3.2 Classical cascode current mirrors: **(a)** double cascode (DCCM), **(b)** single input-transistor (SICCM), **(c)** Wilson(WCM), **(d)** Reduced compliance (RCCM).

Assuming M11-M13 and M12-M14 matched and all transistors in saturation, it can be easily observed from Figure 3.2.a that, since nominally $I_{OUT}=I_{IN}$, the equality $V_{GS11}=V_{GS13}$ is satisfied. This means that, drain voltage of M14 is always equal to that of M12, thus, the current error due to channel length modulation effect on M14 is almost eliminated in this structure, enabling an absolute zero current transfer error, theoretically. However, some mismatches always exist to cause some errors. Since the current transfer error is dominated by the mismatches in this current mirror, an error expression will not be given.

Output resistance of the classical double cascode current mirror can be calculated from the output stage formed by M13 and M14. This stage resembles a common-source stage with a source resistance, whose small signal output resistance could be given by [96]

$$R_{OUTCS} = R_S + r_{ds}(1+g_m R_S) \tag{3.18}$$

where r_{ds} and g_m are the well-known small signal parameters of the MOSFET in common-source configuration and R_S is the resistor connected to the source terminal. Eqn. 3.18 can be directly applied to the double cascode current mirror, by taking $r_{ds}=r_{ds13}$, $g_m=g_{m13}$ and $R_S=r_{ds14}$. Then, the output resistance for the double cascode current mirror can be expressed as

$$R_{OUTDCCM} = r_{ds14} + r_{ds13}(1+g_{m13}\,r_{ds14}) \approx g_{m13}\,r_{ds13}\,r_{ds14} \qquad (3.19)$$

This output resistance is $g_m r_{ds}$ times larger than that of the simple current mirror, as can be noticed by comparing Eqn. 3.19 and 3.7. Since $g_m r_{ds}$ is usually much larger than unity, this improvement is appreciated.

Minimum output voltage of the double cascode current mirror is reached when M13 enters triode region. Therefore

$$V_{OUTminDCCM} = V_{DSsat13} + V_{GS14} = \sqrt{2\,I_{OUT}/\beta_{13}} + \sqrt{2\,I_{OUT}/\beta_{14}} + V_T \qquad (3.20)$$

It is apparent that the lower limit of achievable $V_{OUTminDCCM}$ is V_T (for very low currents, or very large (W/L)s). This is one of the most important disadvantages of this current mirror. On the other hand, input voltage can be given as

$$V_{INDCCM} = V_{GS11} + V_{GS12} = \sqrt{2\,I_{IN}/\beta_{11}} + \sqrt{2\,I_{IN}/\beta_{12}} + 2V_T \qquad (3.21)$$

when body effect is ignored, or source terminal of each MOSFET is connected to its bulk (possible in p-well CMOS technology). Otherwise, due to the increment in V_{T11}, V_{INDCCM} increases by an amount

$$\Delta V_{INDCCM} = \gamma\left(\sqrt{V_{SB11}+\phi_B} - \sqrt{\phi_B}\right) = \gamma\left(\sqrt{V_{GS12}+\phi_B} - \sqrt{\phi_B}\right) \qquad (3.22)$$

where γ is the body effect parameter.

On the other hand, body effect increases output resistance further, but an expression will not be supplied here.

Input resistance is higher than the input resistance of the simple current mirror, such that

$$R_{IN\,DCCM} = \frac{1}{g_{m11}} + \frac{1}{g_{m12}} = \frac{1}{\sqrt{2\beta_{11} I_{IN}}} + \frac{1}{\sqrt{2\beta_{12} I_{IN}}} \tag{3.23}$$

if no body effect is present. However, this is not a serious degradation since $2/g_m$ is still a sufficiently low resistance value.

The output capacitance can be expressed as [95]

$$C_{OUT\,DCCM} = 2C_{GD13} + \frac{2C_{GS13} + C_{DB14} + C_{B13}}{g_{m13} r_{ds13}} + \frac{C_{DB13}}{g_{m13} r_{ds14}} \tag{3.24}$$

where C_{B13} is the p-well to n-substrate junction capacitance of M13. It is obvious from Eqn. 3.24 that output capacitance of the double cascode current mirror is almost independent of the junction capacitances, due to a reduction on the order of $g_m r_{ds}$. Thus, this capacitance can be approximated as

$$C_{OUTDCCM} \approx 2C_{GD13} \tag{3.25}$$

Value of this output capacitance is practically several times lower than that of the simple current mirror output capacitance. Moreover, this is an overlap capacitance which is almost linear, unlike the simple current mirror, whose output capacitance is nonlinear and therefore signal-dependent. This feature is appreciated in output stages of OTAs used in OTA-C filters.

The next current mirror is the classical single input-transistor cascode current mirror (SICCM), given in Figure 3.2.b. Input voltage and input resistance expressions are similar to those of the simple current mirror, and output resistance expression is similar to that of the classical double cascode current mirror, as long as all transistors are in saturation. Thus,

$$R_{IN\,SICCM} = \frac{1}{g_{m21}} = \frac{1}{\sqrt{2\beta_{21} I_{IN}}} \tag{3.26}$$

$$V_{INSICCM} = V_{GS21} = \sqrt{2 I_{IN} / \beta_{21}} + V_T \tag{3.27}$$

$$R_{OUTSICCM} \approx g_{m23} r_{ds23} r_{ds22} \tag{3.28}$$

On the other hand, output capacitance can be approximated as

$$C_{OUTSICCM} \approx C_{GD23} \tag{3.29}$$

which is half of the $C_{OUTDCCM}$, therefore this current mirror is more suitable in OTA-C filters. The factor 2 in Eqn. 3.25 may be explained by the capacitive current in the double cascode current mirror, flowing through C_{GD13} which is coupled to the input and being reflected back to the output stage by mirroring [95]. However, in the single input-transistor cascode current mirror, C_{GD23} is coupled directly to ac ground via the voltage source V_B.

Actually, the bias voltage V_B is to supply a lower gate bias for the upper transistor (M13 in DCCM and M23 in SICCM) so as to achieve the optimum V_{OUTmin}, such that

$$V_{OUTmin} = V_{DSsat23} + V_{DSsat22} \tag{3.30}$$

For low currents, output voltage can drop very close to ground potential, while the current mirror continues to operate properly. However, this optimum condition can be reached only for a single current value. Usually, a high V_B is chosen to satisfy Eqn. 3.30 for the highest possible I_{OUT}. As $I_{OUT}=I_{IN}$ decreases below the maximum value, the $V_{OUTminSICCM}$ value tends to approach $V_{OUTminDCCM}$ and increases beyond it for low currents. Therefore, Eqn. 3.30 should be corrected as

$$V_{OUTminSICCM} = V_{DSsat23} + V_B - V_{GS23} = V_B - V_T \tag{3.31}$$

V_B should be chosen as

$$V_B = V_{GS23M} + V_{DSsat22M} \tag{3.32}$$

where V_{GS23M} and $V_{DSsat22M}$ are the respective V_{GS23} and $V_{DSsat22}$ values corresponding to the maximum possible output current.

The accuracy of this current mirror is unfortunately severely degraded with respect to double cascode current mirror, because, V_{DS22} is not equal to $V_{DS21}=V_{GS21}$. Therefore, due to channel length modulation, current transfer error is high, which can be expressed as

$$\varepsilon_{SICCM}(\%) = 100\lambda \frac{V_{DS22} - V_{GS21}}{1+\lambda V_{GS21}} \tag{3.33}$$

If the optimum point is achieved for widest operation, then $V_{DS22}=V_{DSsat22}=V_{GS22}-V_T$. Then, Eqn. 3.33 takes the form

$$\varepsilon(\%) = -100\lambda \frac{V_T}{1+\lambda V_{GS21}} \tag{3.34}$$

Generally, this error is not as high as that of a simple current mirror, however comparable to it.

Adaptive biasing (V_B is dependent on I_{IN}) can be utilized in this current mirror, whose resultant structures have very appreciable features [59], [101], [106], [107].

The next current mirror is the Wilson current mirror (WCM), which is shown in Figure 3.2.c. This current mirror has very desirable features when realized in bipolar technology, mainly because of the elimination of the error due to the base currents, and the high output resistance, same as the other mentioned cascode current mirrors, which is achieved by means of the local

negative feedback with loop gain $A_{loop} = - g_{m32} r_{ds32}$. This feedback also suplies a very high accuracy, similar to the double cascode case. Moreover, V_{IN} and V_{OUTmin} are again same. However, input resistance is rather high for this current mirror, requiring very high output impedance current sources to drive it. Therefore, it is not suitable for use in OTAs; especially because it may cause additional high impedance nodes in the structure, which probably decrease frequencies of the non-dominant poles, thus causing excess phase shift problems at high frequencies [10], [11], [58], [85].

The last current mirror is the reduced compliance cascode current mirror (RCCCM), which is shown in Figure 3.2.d. This current mirror can achieve V_{OUTmin} values of

$$V_{OUTminRCCCM} \approx V_{DSsat45} + V_{DSsat46} \tag{3.35}$$

by keeping V_{GS45} very close to V_T for any I_{OUT} value (Though this seems to require an infinitely large M45, it will be shown in this work that the requirement is not so serious).

It is clear that, output resistance is the same as previously mentioned current mirrors as long as M45 and M46 are in saturation. Also, V_{IN} and R_{IN} are same as those of the double cascode current mirror. Accuracy, however, is degraded due to the difference between V_{GS46} and V_{GS42}. Since the difference is aimed to be made equal to V_T, Eqn. 3.34 is valid for this current mirror as well, which can be rewritten as

$$\varepsilon_{RCCCM}(\%) = -100\lambda \frac{V_T}{1+\lambda V_{GS61}} \tag{3.36}$$

Finally, output capacitance is again on the order of C_{GD45}, like the other cascode current mirrors.

Table 3.1 summarizes the features of five classical current mirrors. Undesired feature properties are in italics style and desired ones are bold. It is apparent from Table 3.1 that, it is hard to announce a winner. Actually, a real

winner which is expected to be suitable for use in OTA structures should particularly possess a very high R_{OUT} and very low V_{IN} and V_{OUTmin}, besides high accuracy, low C_{OUT} and low R_{IN}. The aim of the next subsection is to introduce novel current mirrors which can achieve all of these features within acceptable limits.

Table 3.1 Comparison of 5 classical MOS current mirrors.

Feature	SCM	DCCM	SICCM	WCM	RCCCM
Accuracy	*very low*	**high**	*low*	**high**	*low*
R_{OUT}	low	**high**	**high**	**high**	**high**
V_{OUTmin}	very low	*high*	low	*high*	low
R_{IN}	low	low	low	*high*	low
V_{IN}	low	*high*	low	*high*	low
C_{OUT}	*high , nonlinear*	low , linear	low , linear	low , linear	low, linear

3.1.2 Proposed-Current Mirrors

In this section, some novel high performance current mirrors are introduced, which are more suitable for OTAs to be used in OTA-C filters or oscillators. It is worth mentioning that these structures are also appreciated by other structures, like current conveyors and current amplifiers, etc. , as will be explained shortly in detail.

3.1.2.1 Accurate Active-feedback Cascode Current Mirror

It has been mentioned in the previous sub-section that the classical double cascode current mirrors achieve larger output impedance and higher transfer accuracy with respect to the simple current mirror but output voltage swing gets worse. Furthermore, input voltage restriction is increased, which may be a

problem if input current is not fixed, like in the current mirrors of an OTA. The regulated cascode (RGC) stage (Figure 3.3.a) [95] can be utilized to build the conventional active-feedback cascode current mirror (CAFCCM) of Figure 3.3.b, which achieves a much larger output impedance and a relatively wider output voltage swing than those of the classical double cascode current mirror, while keeping the same input voltage drop as that of the simple current mirror [108]. The very high output impedance is a result of the active negative feedback through the amplifier stage I_K-M_K and the source follower M_3. Output impedance is $(1\text{-}K_{loop})$ times greater than a conventional cascode current mirror, where K_{loop} is the feedback loop gain, which can be expressed as

$$K_{loop} = - g_{mK} r_{dsK} \tag{3.37}$$

This means that, this current mirror achieves an output resistance which is $(1+g_{mK} r_{dsK}) \approx g_{mK} r_{dsK}$ times larger than an equivalent conventional cascode current mirror.

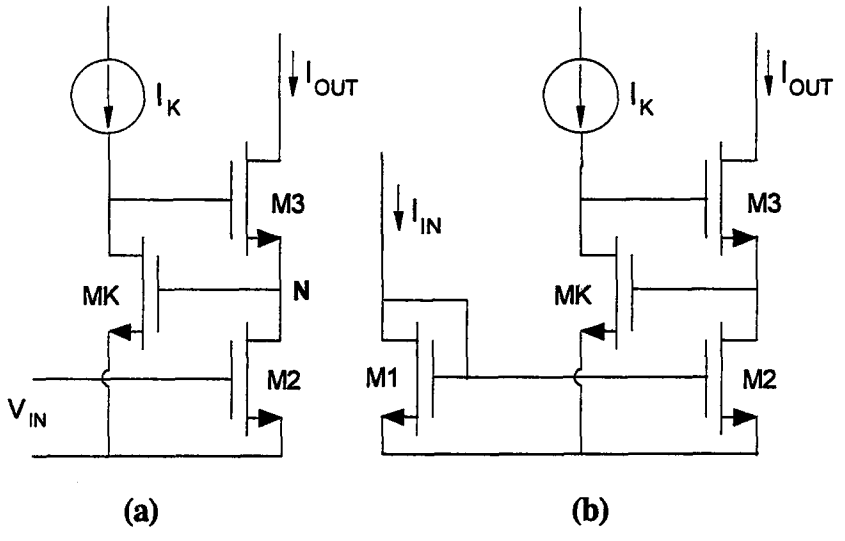


Figure 3.3 **(a)** regulated cascode stage. **(b)** conventional active-feedback current source.

The most important disadvantage of this current mirror is that, $V_{DS2}=V_{GSK}$ is determined by I_K and M_K; therefore for $I_{OUT}=I_{IN}$ to be accurately

achieved, I_K and M_K must be chosen such that $V_{DS2}=V_{GS2}$ is satisfied; otherwise transfer accuracy is rather lower than that of a classical double cascode current mirror, due to channel length modulation effect [97]. This transfer error gives rise to offset and non-linearity problems in analogue circuits [4, p. 379], [106]. On the other hand, if the input current I_{IN} is not fixed, then two problems may arise:

1) $V_{DS2}=V_{GS2}$ equality cannot be achieved, except in a single case, i.e. when $V_{GSK}=V_{GS1}$, degrading transfer accuracy (probably, this is the main reason why this circuit is proposed as a 'current source' [108]).

2) If I_{IN} (thus V_{GS2}) is large enough to drive M_2 into triode region (because of fixed V_{DS2}), then the current mirror does not operate properly.

Nevertheless, if V_{DS2} can be adjusted to be equal to V_{GS2} for any I_{IN} value, these problems are overcome optimally. Then, output swing is not fixed but dependent on V_{GS1} (thus, on I_{IN}). This dependency makes it possible to achieve an optimal output swing for every I_{IN} value, while keeping the high current transfer accuracy. Note that, V_{DS}-dependency of I_D is not too strong for a MOSFET operating in saturation; therefore, to achieve an accurate current reflection ratio, $V_{DS2}=V_{DS1}$ equality need not be precisely satisfied.

The simplest method to achieve $V_{DS2}=V_{GS2}$ is to choose M_K matched with M_1 and set $I_K=I_{IN}$. Then I_K is no more an independent current source but dependent on I_{IN}. (To distinguish between the dependent current of the new circuit and constant source current I_K of CAFCCM, the dependent current of the new circuit will be called I_{DK}) Since V_{DS2} need not be accurately equal to V_{GS2}, I_{DK} can be obtained from I_{IN} by using simple current mirrors. I_{DK} can also be chosen equal to I_{IN}/κ, where $\kappa>1$; provided that $(W/L)_K=(W/L)_A=(W/L)_1/\kappa$. This will be an advantage for keeping power and chip area consumption lower.

Small-signal output impedance for CAFCCM and for the new circuit (when $I_{DK}=I_K$ is assumed) can be approximated as [108]

$$R_{OUTCAFCCM} = r_{ds2}\, g_{m3}\, r_{ds3}\, g_{mK}\, r_{dK} \qquad (3.38)$$

where body effect is not included.

When Eqn.3.38 is compared with the output resistance expressions of the classical cascode current mirrors (e.g. Eqn. 3.19), it can be observed that output impedance of this cascode current source is $g_{mK}\, r_{dK}$ times larger than that of a conventional cascode current mirror, as have already been mentioned above. The factor $g_{mK}\, r_{dK}$ is the feedback loop gain, which can be expressed as

$$g_{mK}\, r_{dsK} = \mu_n C_{ox} \left(\frac{W}{L}\right)_K \frac{V_{GSK} - V_T}{\lambda_N I_{DK}} \tag{3.39}$$

if $r_{dK} = 1/(\lambda_N I_{DK})$ is assumed. Here, λ_N is channel length modulation parameter for the n-channel MOSFETs. It can be observed from Eqn. 3.39 that, when $(W/L)_K$ and I_{DK} are decreased by a factor κ to reduce power consumption and chip area, there can be only a slight change in the output impedance practically (no change at all, theoretically).

Eqn. 3.37 is obtained by assuming output resistance of I_K high enough and gain of source follower M3 unity. Actually, the latter assumption is reasonable, however, output resistance of I_K may not be sufficiently high in practice. Therefore, in Eqns. 3.37 and 3.38, r_{dsK} must be replaced by $(r_{dsK}//R_{OK})$ and λ_N must be replaced by $(\lambda_N+\lambda_P)$, where R_{OK} is the output resitance of the current source I_K. Nevertheless, this does not change the comments made above, about CAFCCM and the new current mirror, which from now on will be called 'accurate active-feedback cascode current mirror' (AAFCCM) [107].

Circuit diagram of the proposed accurate active-feedback current mirror is given in Figure 3.4. Though diminishing the devices increases the errors in matching of M_A and M_K, this will not affect the circuit's performance significantly since $I_{DK} = I_{IN}/\kappa$ equality need not be precisely achieved (that is why simple current mirrors are preferred for obtaining I_{DK} from I_{IN}). When designing the circuit, aspect ratios should be chosen such that M_C remains in saturation for

maximum possible input current to be handled by the circuit. In a circuit employing the new current mirror, $I_{DK}=I_{IN}/\kappa$ can be obtained easier if I_{IN} can be reflected from the device supplying it; thus, M_A and M_B can be eliminated, decreasing chip area and power consumption further. For example, in OTA and current conveyor structures, such power and area saving eliminations have been shown to be possible [59], [69].

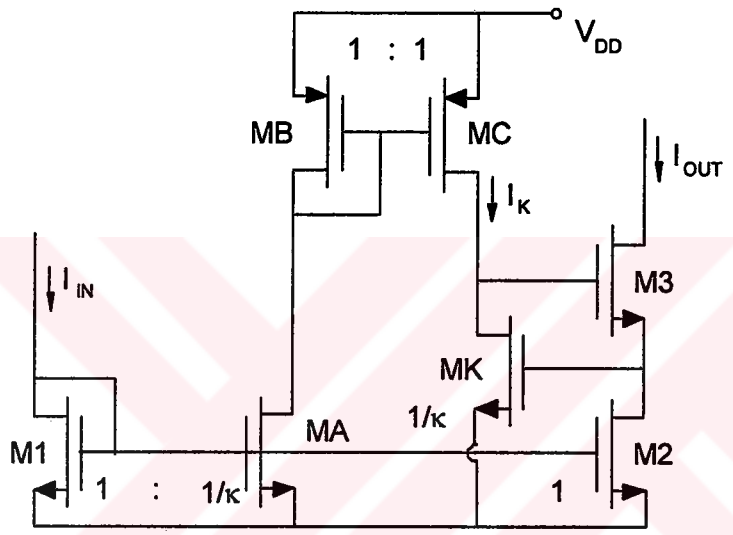


Figure 3.4 Accurate active-feedback current mirror.

The transfer error ε for AAFCCM can be extracted from the following equations (For simplicity of the analysis, $\kappa=1$ is assumed. Therefore, $(W/L)_1=(W/L)_K=(W/L)_A$; thus $\beta_1=\beta_K$, where $\beta_{1,K}=(W/L)_{1,K}\mu_n C_{ox}$. In the equations, β_N is used to represent both β_1 and β_K):

$$\begin{aligned}\frac{I_{D2}}{I_{D1}} &= 1+\varepsilon = \frac{1+\lambda_N V_{GSK}}{1+\lambda_N V_{GS1}} \\ &\approx (1+\lambda_N V_{GSK})(1-\lambda_N V_{GS1}) \\ &= 1+\lambda_N (V_{GSK}-V_{GS1})+\lambda_N^2 V_{GSK} V_{GS1} \\ &\approx 1+\lambda_N (V_{GSK}-V_{GS1})\end{aligned} \tag{3.40}$$

Here, ε is the current transfer error from input to output. The approximations in Eqn. 3.40 are made using the general approximation approach that, " if x«1 and

y«1, then (1+x)/(1+y)≈(1+x)(1-y)=1+x-y+xy≈1+x-y ", where $x=\lambda_N V_{GSK}$ and $y=\lambda_N V_{GS1}$. The voltage difference V_{GSK}-V_{GS1} can be expressed as

$$V_{GSK}-V_{GS1}=\left(\sqrt{\frac{2I_{DK}}{\beta_N}}+V_T\right)-\left(\sqrt{\frac{2I_{D1}}{\beta_N}}+V_T\right)=\sqrt{\frac{2}{\beta_N}}\left(\sqrt{I_{DK}}-\sqrt{I_{D1}}\right) \tag{3.41}$$

By using Eqns. 3.40 and 3.41, the transfer error can be extracted as

$$\varepsilon=\lambda_N\sqrt{\frac{2}{\beta_N}}\left(\sqrt{I_{DK}}-\sqrt{I_{D1}}\right)=\lambda_N\sqrt{\frac{2}{\beta_N}}\left(\sqrt{I_{D1}(1+\varepsilon_K)}-\sqrt{I_{D1}}\right)=\lambda_N\sqrt{\frac{2I_{D1}}{\beta_N}}\left(\sqrt{1+\varepsilon_K}-1\right) \tag{3.42}$$

where ε_K is the error in I_{DK}, which is defined in the following equation, in a similar way as ε:

$$\frac{I_{DK}}{I_{D1}}=\frac{1+\lambda_N V_{DSK}}{1+\lambda_N V_{GS1}}=1+\varepsilon_K \tag{3.43}$$

Using the approximation approach " √(1+x)≈1+x/2 for x«1 ", where $x=\varepsilon_K$, the transfer error expression can be simplified as

$$\varepsilon\approx\sqrt{I_D\frac{1}{2\beta_N}}\lambda_N\varepsilon_K \tag{3.44}$$

This error is also valid for CAFCCM. It can be easily observed from Eqns. 3.43 and 3.44 that, transfer error of the proposed AAFCCM can be kept very low, if ε_K is low enough, i.e. if $I_{DK}=I_{D1}$ is achieved satisfactorily. On the other hand, ε_K may be very high in CAFCCM because of the difference between I_{D1} and constant source current I_K, increasing the overall error ε.

Besides transfer accuracy, the proposed circuit has some other advantages over CAFCCM, which can be utilized by making a proper design:

1) there is no need for additional biasing circuitry to obtain a constant current I_K.

2) power consumption is $V_{DD}(2I_{IN}+I_K)$ for CAFCCM and $2V_{DD}I_{IN}(1+1/\kappa)$ for the proposed current mirror, which means that, by choosing $\kappa>1$, power consumption of the new circuit can be kept lower than that of CAFCCM; especially for input current levels lower than I_K.

3) chip area can be kept very near to that of CAFCCM, by choosing higher κ values.

Additionally, if a circuitry supplying I_K is accounted for in CAFCCM, it is possible to keep the new circuit's chip area smaller and power consumption significantly lower than those of CAFCCM.

Some words must be added about output impedance properties of CAFCCM and the proposed current mirror in order to findout whether the proposed structure achieves the high output impedance performance of CAFCCM adequately or not:

Eqn. 3.38 can be expressed to obtain the dependency of small signal output impedance on I_{IN} and I_K. By choosing $(W/L)_1=(W/L)_2=(W/L)_3=(W/L)_K$ and neglecting body effect for M3 for simplicity, one obtains

$$R_{OUT}=\frac{2\beta_N}{\lambda_N^3 I_{IN}^{3/2} I_K^{1/2}} \tag{3.45}$$

for CAFCCM, where β_N and λ_N are common parameters for M1, M2, M3 and MK. For the proposed current mirror, I_K must be replaced with I_{IN} in Eqn. 3.45. This means that, for input current levels lower than I_K, the new circuit's output impedance is better that that of CAFCCM; while for $I_{IN}>I_K$, CAFCCM has a higher output impedance. However, since the difference in output resistances is via squareroot of a ratio I_{IN}/I_K, the advantage and disadvantage of the new circuit over CAFCCM is not that much important, unless I_{IN} is extremely higher or lower than I_K of CAFCCM. For example, even if I_{IN} is 100 times higher or

lower than I_K, the difference in R_{OUT} is only by a factor 10. Since output impedance for these structures is quite high, this extreme case generally does not cause a serious performance shift when the current mirror is used in a stage where high output impedance of the current mirror is demanded. Nevertheless, some improvements can be made to improve both accuracy and output resistance of AAFCCM, which will be supllied in the following sub-sections.

Finally, it must be added that, the analyses are carried out assuming no body effect on M3. Actually M3 can be put in a separate well in a p-well process, thus body effect is eliminated. Nevertheless, even if this is not possible (like in an n-well process), since accuracy depends directly on equality of $V_{DS2}=V_{DS1}$, body effect on M3 has no effect in accuracy. Also, it was proven that body effect on M3 does not change the R_{OUT} expression given by Eqn. 3.38 [110], whose proof will not be repeated here.

3.1.2.2 AAFCCM with Improved Accuracy and Output Resistance

The accuracy of AAFCCM can be increased further if the accuracy of the current transfer via MA, MB and MC can be increased. Even the PMOS current mirrors can be changed with cascode current mirrors, however this brings excess voltage restrictions. Instead, they are chosen long (large L) in AAFCCM. However, channel length modulation still exists on MA, becasue V_{DSA} is not equal to V_{DS1}. Making it long by keeping $(W/L)_A=(W/L)_1$ will help, however, matching errors between M1 and MA will increase a lot. Therefore, since eliminating channel length modulation effect on MA by sizing MA seems inefficient, then, achieving $V_{DSA}=V_{DS1}$ is the only possibility left for increasing the accuracy of AAFCCM. Using the fact that AAFCCM achieves $V_{DS2}=V_{DS1}$, it can be concluded that setting V_{DSA} equal to V_{DS2} will also help increasing accuracy.

In the improved current mirror (which will be called AAFCCM-2), shown in Figure 3.5, the NMOS transistor, namely MD, is added to set the drain voltage of MA equal to that of M2, thus eliminating channel length modulation effect on MA. It is very amazing that, for both ac and dc conditions, MD acts as a current buffer

(I_{DD}=I_{DA}) and if it has the same aspect ratio as that of M3, together with M3, it acts as a voltage buffer (V_{DSA}=V_{DS2}) as well. Then, the transfer error from I_{IN} to I_K is significantly reduced. Note that, the PMOS transistors MB and MC need not match with any other transistor in the circuit but only with each other. Therefore, as mentioned above, the channel lengths of MB and MC can be chosen long enough to satisfactorily reduce the channel length modulation effect on MC, thus decreasing the current transfer error from I_{IN} to I_K. Hence, V_{GSK}=V_{GS1} equality is much more accurately satisfied, in turn, significantly increasing the accuracy of the equality I_{OUT}=I_{IN} [69].

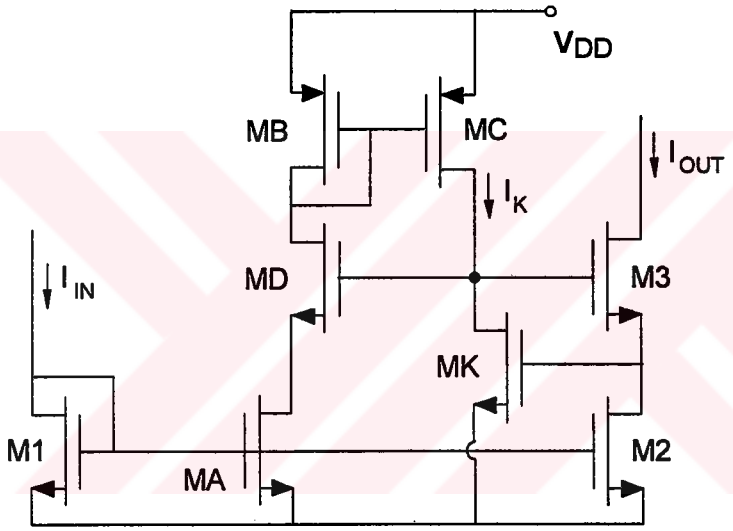


Figure 3.5 AAFCCM with improved current transfer accuracy (AAFCCM-2).

3.1.2.3 AAFCCM with Further Accuracy Improvement

In AAFCCM-2, the channel length modulation effect was significantly reduced by adding a transistor MD. Assuming the PMOS current mirror accurate, it can be easily noticed that, increasing accuracy further relies on reduction of channel length modulation effect on MK, due to the difference in drain-source voltages of MA and MK. This effect is another cause of error in achieving V_{GSK}=V_{GSA} equality, even when I_{DK}=I_{DA} is accurately achieved.

Looking at Figure 3.5, it can be deduced that the difference between V_{DSK} and V_{DSA} in AAFCCM-2 can be given as

$$V_{DSK} - V_{DSA} = V_{GS3} \tag{3.46}$$

This gives an idea about how to eliminate the error caused by channel length modulation on MK. This idea is applied in the further improved AAFCCM (which will be called AAFCCM-3) by adding another transistor, namely ME, with a similar configuration as MD (Figure 3.6) [101]. Aspect ratio of ME should be chosen equal to those of M3 and MD. Then, $V_{DSK}=V_{DSA}$ equality and thus $V_{GSK}=V_{GSA}$ equality is very accurately achieved.

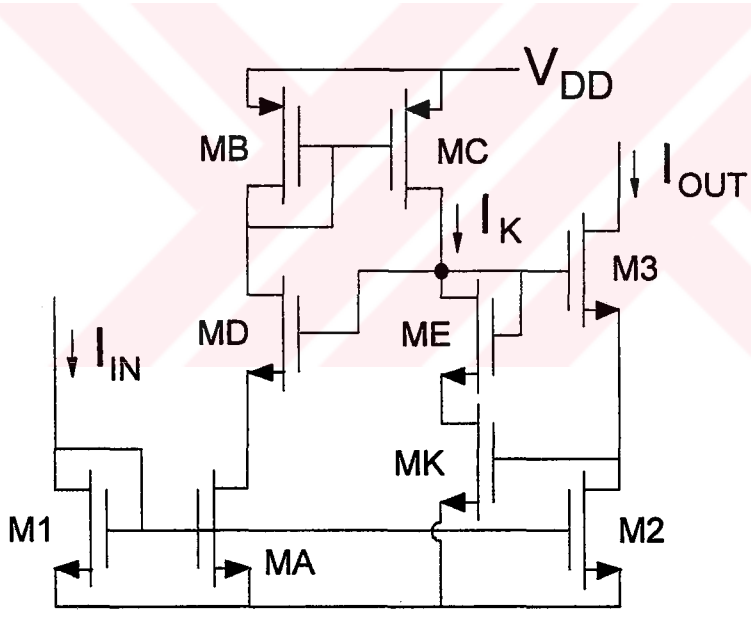


Figure 3.6 AAFCCM mirror with further accuracy improvement (AAFCCM-3).

Addition of ME brings no degradation in output resistance, since feedback loop gain does not change, as proven below:

Assuming gain of source follower M3 unity (i.e. $1/g_{m3} << r_{ds2}$), the loop gains are

$$K_{loop2} = - g_{mK} (r_{dsK} // r_{dsC}) \tag{3.47}$$

$$K_{loop3} = \frac{-g_{mK} r_{dsK} r_{dsC}}{r_{ds5K} + 1/g_{mE} + r_{dsC}} \approx - g_{mK} (r_{dsK} // r_{dsC}) \qquad (3.48)$$

for the AAFCCM-2 of Figure 3.5 and for AAFCCM-3 of Figure 3.6, respectively, where $1/g_{mE} << r_{dsK}$ is assumed, and body effect is omitted for simplicity. Then, output resistance of AAFCCM-3 can be expressed similar to other active feedback current mirrors as

$$R_{OUTAAFCCM-3} = g_{m3} g_{mK} r_{ds2} r_{ds3} (r_{dsK} // r_{dsC}) \qquad (3.49)$$

3.1.2.4 Accurate Compact Cascode Current Mirror (ACCCM)

Among the current mirrors examined and proposed upon here in this text, none can achieve high accuracy, high output resistance, low input voltage and low output voltage features at the same time. The proposed current mirrors (AAFCCMs) can achieve very high output resistance, high accuracy and low input voltage, however V_{OUTmin} is not better than that of a double cascode current mirror, i.e. 1 V_{GS} plus 1 V_{DSsat}. The single input transistor cascode current mirror (SICCM) can achieve lower output compliance (V_{OUTmin}) voltages, however, this compliance voltage is not optimal and also may drive some transistors into triode region for some current values. Also accuracy is low in SICCM (Nevertheless, accuracy of SICCM can be increased significantly with some additions [106], however, then the output compliance again rises to the value $V_{GS}+V_{DSsat}$). Here, the term 'optimal' refers to the case wherein the output transistors of a current mirror are both (conventional cascode output is considered) at onset of saturation when $V_{OUT}=V_{OUTmin}$ for any current value; thus a minimal V_{OUTmin} (i.e. approximately $2V_{DSsat}$) can always be achieved. In the literature, some current mirrors have been reported which have low compliance voltages (lower than $2V_{DSsat}$), however they rely on triode MOSFETs, which degrade output resistance seriously [104], [105]. Therefore, they cannot be used in OTA structures.

In achieving an optimal V_{OUTmin}, the current mirror of Figure 3.1.d (RCCCM) is the best among all, as is revealed in Section 3.1 and expressed by Eqn. 3.35. Though it is not clear how to choose the aspect ratios, if I_{IN} is fixed, $(W/L)_{41}$ can be chosen several times smaller than $(W/L)_{43}$ to operate M46 at onset of saturation. Then, $V_{OUTmin}=V_{DSsat45}+V_{DSsat46}$. However, I_{IN} is generally variable, therefore, for obtaining an accurate current reflection for any I_{IN} value, $(W/L)_{41}=(W/L)_{43}$ must be satisfied besides $(W/L)_{42}=(W/L)_{44}=(W/L)_{46}$. Then, $(W/L)_{45}$ must be very large for satisfying $V_{GS45} \approx V_T$ to achieve $V_{DS46} \approx V_{DSsat46} = V_{GS46}-V_T$. Besides the high-W/L device requirement, this current mirror has another drawback caused by inequality of V_{DS52} and V_{DS56}, degrading accuracy due to channel length modulation, as have already been expressed by Eqn. 3.36.

In Figure 3.2.d, since $V_{GS41}=V_{GS43}$, gate voltages of both M45 and M46 are equal. This is also valid for the output stage of the proposed cascode current mirror of Figure 3.7, in which gates of M3 and M4 are connected, provided that $(W/L)_1=(W/L)_3$ and $(W/L)_2=(W/L)_4$. Since all gates are compactly connected via a single node, this current mirror will be named as 'accurate compact cascode current mirror' (ACCCM). If all devices can be operated in saturation, this current mirror will have a high current transfer accuracy, since $V_{DS4}=V_{DS2}$. Similar to the current mirror in Figure 3.1.d (RCCCM), $(W/L)_{1,3}$ must be chosen very high in the proposed current mirror to force M2 and M4 into saturation. As proven below, this disadvantage has been exagerrated only due to frequent use of simplified MOSFET models in hand analyses. Therefore, very simple but functional structures, like the one in Figure 3.7, have probably been missed or evaluated wrongly. The triode region current is [4, p. 22], [110, p. 125]

$$I_D = \beta[(V_{GS}-V_T)V_{DS} - \tfrac{1}{2}(1+\delta)V_{DS}^2] \qquad (3.50)$$

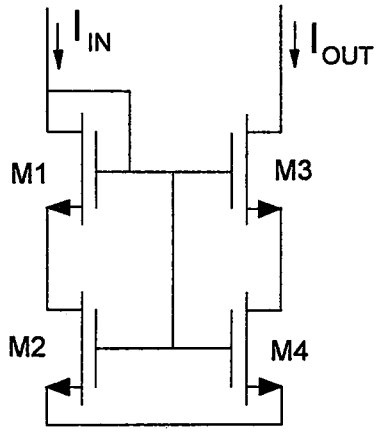


Figure 3.7 Accurate compact cascode current mirror (ACCCM).

In Eqn. 3.50, δ represents the body effect in triode region current and can be expressed as

$$\delta = \frac{\gamma}{2\sqrt{V_{SB} + 2\phi_F}} \tag{3.51}$$

where γ is the body effect factor. Eqn. 3.50 is obtained by expressing the accurate but complex '3/2 power' triode region current expression [111] into Taylor series and taking the lower power terms. Though Eqn. 3.50 is very simple, it represents the actual current expression quite adequately. Precision of Eqn. 3.50 can be increased further by making δ V_{DS}-dependent [97], however, δ cannot be omitted even if V_{SB}=0, as implied by Eqn. 3.51. In present CMOS technologies, δ varies typically from 0.35 to 0.7, for V_{SB}=0. Eqn. 3.50 implies that, at onset of saturation, V_{DS} is not equal to V_{GS}-V_T but lower, such that

$$V_{DSsat} = \frac{V_{GS} - V_T}{1+\delta} \tag{3.52}$$

and saturation current should be given by [110, p. 125]

$$I_D = \frac{\frac{1}{2}\beta(V_{GS} - V_T)^2}{1+\delta} \tag{3.53}$$

Eqn. 3.52 means that, saturation is still achieved below V_{GS}-V_T down to $(V_{GS}$-$V_T)/(1+\delta)$. This makes possible operating M2 and M4 exactly in saturation, by choosing a suitable $(W/L)_{1,3}$ value. Note that, this possibility couldn't have been noticed if δ was neglected. For M4 to operate at onset of saturation for widest output voltage swing, $V_{DS4}=V_{GS4}-V_{GS3}$ should be equal to $V_{DSsat4}=(V_{GS4}-V_T)/(1+\delta)$. Then,

$$V_{GS3} - V_T = \frac{\delta}{1+\delta}(V_{GS4} - V_T) \tag{3.54}$$

and since $I_{D3}=I_{D4}$, assuming both M3 and M4 in saturation, and no body effect on M3 (i.e. source and bulk is shorted)

$$\frac{\frac{1}{2}\beta_3(V_{GS3} - V_T)^2}{1+\delta} = \frac{\frac{1}{2}\beta_4(V_{GS4} - V_T)^2}{1+\delta} \tag{3.55}$$

Using Eqn. 3.54 and 3.55 and assuming equal $\mu_n C_{ox}$ for both M3 and M4, the required W/L of M3 can be obtained as

$$\left(\frac{W}{L}\right)_3 = \frac{(1+\delta)^2}{\delta^2}\left(\frac{W}{L}\right)_4 \tag{3.56}$$

For $\delta=0.35$ (the lowest typical value), Eqn. 3.56 implies that, choosing $(W/L)_{1,3}$ 15 times higher than $(W/L)_{2,4}$ is enough for keeping M2 and M4 in saturation (for a typical value of δ, 10 is sufficient), but very close to saturation-triode region boundary, thus supplying an almost optimal V_{OUTmin}. It is worth noting that, if $(W/L)_{1,3}$ is chosen lower than the required value, M2

and M4 will be driven into triode region and output resistance will degrade, but high accuracy will remain since $V_{DS4}=V_{DS2}$ will still be satisfied. This is an interesting feature which does not exist in any other current mirror. Additionally, input voltage restriction is less for the proposed current mirror since V_{IN} is only V_{GS2}.

The proposed current mirror has a very simple structure and achieves high accuracy, low V_{IN} and low V_{OUTmin} features for any I_{IN} values without any requirements for a bias voltage, a bias current or complementary transistors (p-channel devices in this case). A drawback may be the requirement of source-bulk shorting, which is possible only in a p-well CMOS process for n-channel MOSFETs. This means that in an n-well process the current mirror may suffer from the body effect on M1 and M3, which drives M2 and M4 into triode region (due to the drop in δ according to Eqn. 3.51), causing a severe drop in output resistance of the current mirror (PMOS version of the proposed current mirror may suffer from the same effect in a p-well process). However, because $V_{SB3} = V_{DSsat4}$ when source-bulk shorting is not done, and since V_{DSsat4} is a sufficiently low voltage as long as the drain current is not too high, this effect can be compensated by taking some precautions. One is to increase transconductance of M4 to reduce V_{DSsat4} (which is proportional to $V_{GS4}-V_T$), which can be done by increasing $(W/L)_4$ (Note that this is required for achieving sufficiently low V_{IN} values even for high currents). The second precaution is to choose $(W/L)_3$ larger than the required value to compensate for the drop in δ (For example, choosing $(W/L)_3=20(W/L)_4$ is sufficient for general cases). Then, the proposed technique becomes applicable to both PMOS and NMOS structures, regardless of whether the process is p-well or n-well.

While looking up literature, it has been discovered that the output stage of the proposed current mirror (M3 and M4 with their gates connected to each other) was reported as a 'self cascode' voltage gain stage [112] (more efficiently analyzed in [113]) and utilised in a 'simple (but low accuracy)

cascode current mirror' [114], but there, the structure has been operated in weak inversion where V_{DSsat} restrictions are less strict. Either narrow channel effects [112] or multiple threshold CMOS process [114] were utilised to obtain $V_{T4} > V_{T3}$ so as to operate M4 in or at onset of saturation. However, results of the analyses carried out here prove that, narrow channel effects or multiple threshold voltages are not necessary for operating M4 in saturation. This is also valid in weak inversion for the proposed current mirror.

Though V_{OUTmin} is quite low ($V_{DSsat3}+V_{DSsat4}$) for the ACCCM, since its output resistance is equal to that of an equivalent classical cascode current mirror (assuming M3 and M4 in saturation) it is still not suitable to be used as a current mirror at the output stage of the symmetrical OTA (A solution for this problem will be proposed in the following sub-sections shortly). Nevertheless, it would be very convenient to use it as the tail current source I_A, since it will drive a low impedance node. When an equivalent classical cascode current source is considered, it can be noticed that use of the proposed current mirror brings an improvement of almost $1V_T$ (conventionally about 1 Volt) to the negative common-mode range (See Figure 2.2). Also, adjustment of I_A via a control-current is more accurate.

3.1.2.5 Active-feedback Compact Cascode Current Mirror

It is possible to apply the regulated cascode technique [95] to the proposed compact cascode current mirror without any accuracy degradation. An implementation for the active-feedback compact cascode current mirror can be observed in Figure 3.8.

If aspect ratios are such that $(W/L)_A=(W/L)_K$ and $(W/L)_B=(W/L)_C$, then, thanks to current mirroring via the PMOS current mirror, $V_{DS4}= V_{DS2}$ is achieved. It is appearent that active feedback can be composed only when $V_{DS2,4}$ is greater than V_T, so that MA and MK are not in cut-off. Since $V_{DS2,4} = V_{DSsat2,4}$ is achieved for widest output swing (by choosing for example $(W/L)_{1,3} = 15(W/L)_{2,4}$), this means that the current mirror can operate only for

sufficiently large V_{DSsat} values (i.e. only for large V_{GS} -V_T , thus large I_D values), which is a serious drawback. Nevertheless this problem can be solved by insering level-shift stages with unity ac gains. The resultant current mirror is given in Figure 3.9.

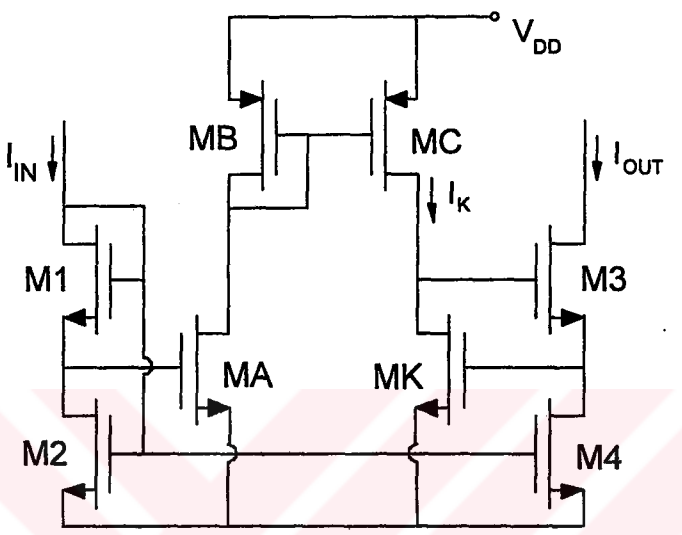


Figure 3.8 Active-feedback compact cascode current mirror suitable for only large currents.

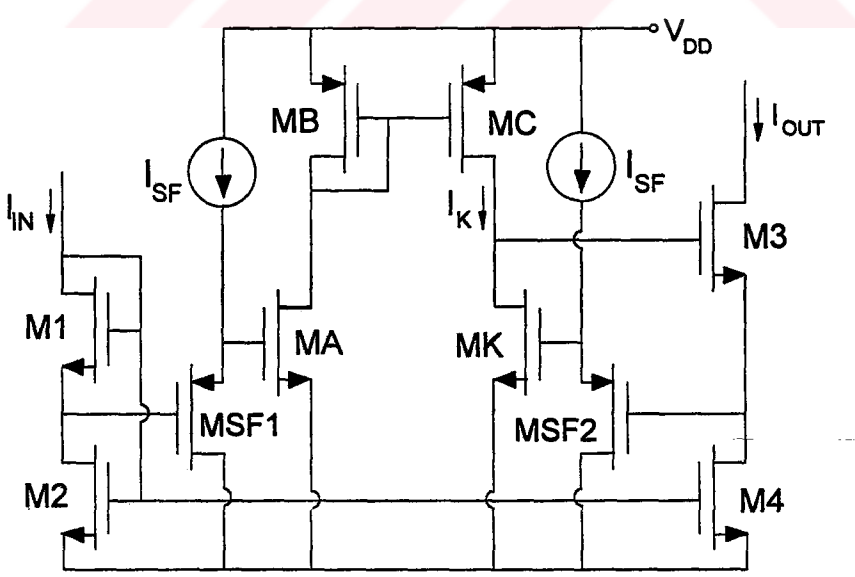


Figure 3.9 Active-feedback compact cascode current mirror with level shifters to enable operation for any current level.

The value of the bias currents of PMOS source followers (level-shifters) can be made very low to prevent excess power consumption, because even a voltage shift of $|V_{TP}|$ will be enough to keep MA or MK in conduction ($V_{GSK}=|V_{GSSF2}|+V_{DSsat4}$ will be very sufficient to keep $V_{GSK}>V_T$ for any current level, even when $|V_{GSSF2}| \approx |V_{TP}|$). As a result, a very high output resistance is achieved, with a low V_{OUTmin}. It is worth mentioning that, the very-high-resistance feature of this current mirror avails the possibility of operating M4 in triode region, while the output resistance is still sufficiently high. Thus V_{OUTmin} values well below $2V_{DSsat}$ (e.g. less than 0.2V even for large currents) are easily achievable. However, the lower limit of V_{IN} is still $1V_T$ (generally about 1 Volt) for strong inversion. Next sub-section introduces a novel method to reduce V_{IN} of the compact cascode current mirror well below V_T.

3.1.2.6 Compact Cascode Current Mirror with Reduced V_{IN}

In Figure 3.10, the V_{IN} reduction technique is shown on the compact cascode current mirror. n is the ratio $(W/L)_3:(W/L)_4$, as given in Eqn. 3.56. A stable positive shunt current feedback ($\beta_{FB}=1/K<1$) is applied through MN, MPr, MPi and M1, to set M2 always almost at onset of saturation. It can be shown by analysis that, the positive feedback causes the drain current of M2 be not equal to I_{IN}, but

$$I_{D2}=\frac{1}{1-\frac{1}{K}}I_{IN}=\frac{K}{K-1}I_{IN} \qquad (3.57)$$

where $K>1$ for a stable positive feedback. For example, $K=10$ is a good choice to avoid excess power consumption due to currents of MPi, MPr and MPo. Then, $I_{D2}=1.111I_{IN,}$ and thus, $I_{DA}=I_{D2}/10=0.1111I_{IN}$. $(W/L)_1$ should be chosen n/K times $(W/L)_2$ to keep M2 very close to onset of saturation, to achieve minimum V_{IN} value, such that

$$V_{IN} \approx V_{DSsat2} \tag{3.58}$$

This is a quite appreciated result, because, unlike the current mirrors examined or proposed upon here, this input voltage drop is not limited by the threshold voltage V_T; actually, it can be made very close to zero for sufficiently large $(W/L)_2$ values. Note also that, M1 now is not much larger than M2, but n/K times larger (for n=15 and K=10, this yields only $(W/L)_1=1.5(W/L)_2$).

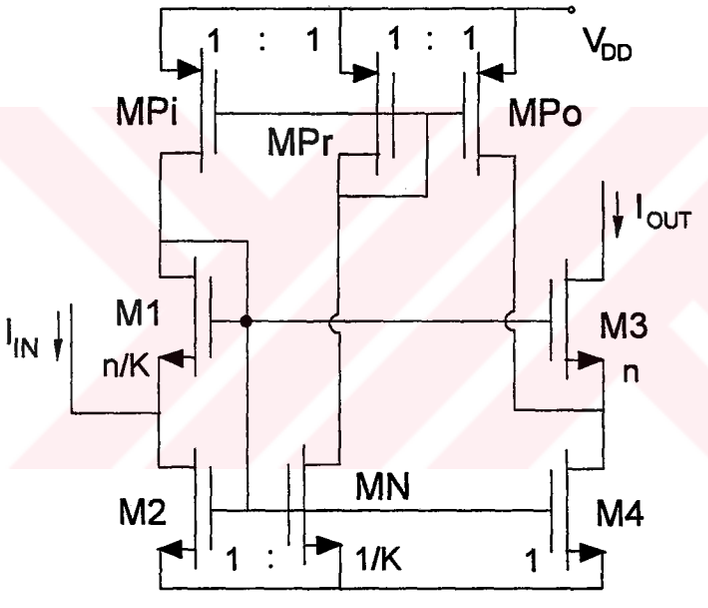


Figure 3.10 Compact cascode current mirror with reduced V_{IN}.

MPo performs a feed-forward job, to eliminate the error caused by feedback, i.e. it inserts a current equal to 0.111 I_{IN} to the output branch (assuming K=10), such that

$$I_{OUT} = I_{D4} - |I_{DPo}| = 1.111\ I_{IN} - 0.111\ I_{IN} = I_{IN} \tag{3.59}$$

provided that $(W/L)_3$ is chosen as

$$\left(\frac{W}{L}\right)_3 = n\left(1-\frac{1}{K}\right)\left(\frac{W}{L}\right)_4 \qquad (3.60)$$

since $I_{D3}=(1-1/K)I_{D4}$ (In the figure, assuming $K>>1$, this ratio is approximated with n). Then, V_{OUTmin} again takes the value $V_{DSsat3}+V_{DSsat4}$.

3.1.2.7 Active-feedback Reduced-V_{IN} Compact Cascode Current Mirror

The active-feedback technique can be applied to the reduced-V_{IN} compact cascode mirror, as shown in Figure 3.11. This active feedback supplies a very high output resistance. Consequently, the resultant current mirror possesses

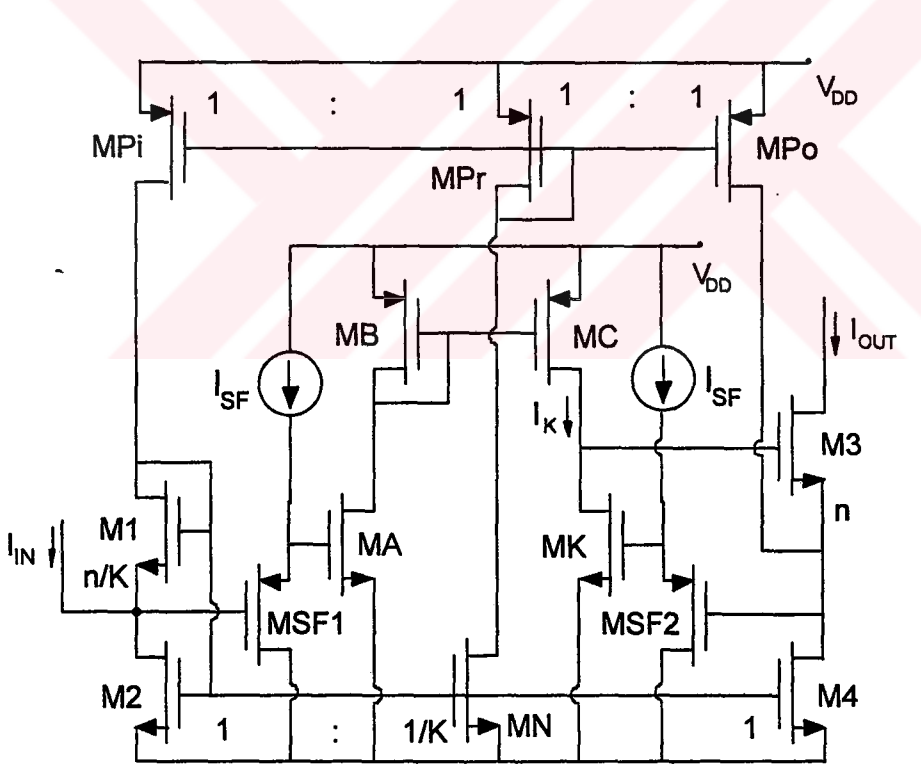


Figure 3.11 Active-feedback reduced-V_{IN} compact cascode current mirror.

- high accuracy
- very high output resistance

- very low V_{OUTmin}
- very low V_{IN}

however, the parasitics and power consumption increase. These are prices to pay for achieving a high performance current mirror.

Note that, M2 and M4 can be made smaller to operate in linear region, thus lowering V_{IN} and V_{OUTmin}, further. Nevertheless, since the output resistance is very high when M2 and M4 were in saturation, pushing them into triode region will reduce the output resistance, but only to a level not worse than that possessed by a conventional cascode current mirror.

3.1.3 Performance Verification of the Proposed Current Mirrors

Performance characteristics of the proposed current mirrors are verified by the circuit simulation program PSpice 5.0. To allow comparison, equivalency of all current mirrors is aimed. Though it is hard to achieve a reasonable equivalency, a point of equivalency was chosen as the aspect ratios of the very lower transistors,

Some abbreviations are used in the figures and tables, whose meanings are listed below:

DCCM: Classical double cascode current mirror
AAFCCM: Accurate active-feedback cascode current mirror
AAFCCM-3: Accurate active-feedback cascode current mirror - 3
ACCCM: Accurate compact cascode current mirror
AFCCCM: Active-feedback compact cascode current mirror
RVCCCM: Reduced-V_{IN} compact cascode current mirror
AFRVCCCM:Active-feedback reduced-V_{IN} compact cascode current mirror

Table 3.2 Asspect ratios for transistors of the simulated current mirrors.
(Note: default channel length is L=3μm)

DCCM	M1 W=30μm M2 W=30μm	M3 W=30μm M4 W=30μm
AAFCCM	M1 W=30μm M2 W=30μm M3 W=30μm MA W=30μm	MB W=300μm L=9μm MC W=300μm L=9μm MK W=30μm
AAFCCM-3	M1 W=30μm M2 W=30μm M3 W=30μm MA W=30μm MK W=30μm	MB W=300μm L=9μm MC W=300μm L=9μm MD W=30μm ME W=30μm
ACCCM	M1 W=450μm M2 W=30μm	M3 W=450μm M4 W=30μm
AFCCCM	M1 W=450μm M2 W=30μm M3 W=450μm M4 W=30μm MSF1 W=200μm MSF2 W=200μm	MA W=300μm L=9μm MB W=300μm L=9μm MC W=300μm L=9μm MK W=300μm L=9μm I_{SF} = 1μA
RVCCCM	M1 W=45μm M2 W=30μm M3 W=405μm M4 W=30μm	MA W=3μm MPi W=200μm L=9μm MPr W=200μm L=9μm MPo W=200μm L=9μm
AFRVCCCM	M1 W=45μm M2 W=30μm M3 W=405μm M4 W=30μm MN W=3μm MSF1 W=300μm MSF2 W=300μm MA W=45μm	MB W=200μm L=9μm MC W=200μm L=9μm MK W=200μm L=9μm MPi W=300μm L=9μm MPr W=300μm L=9μm MPo W=300μm L=9μm I_{SF} = 1μA

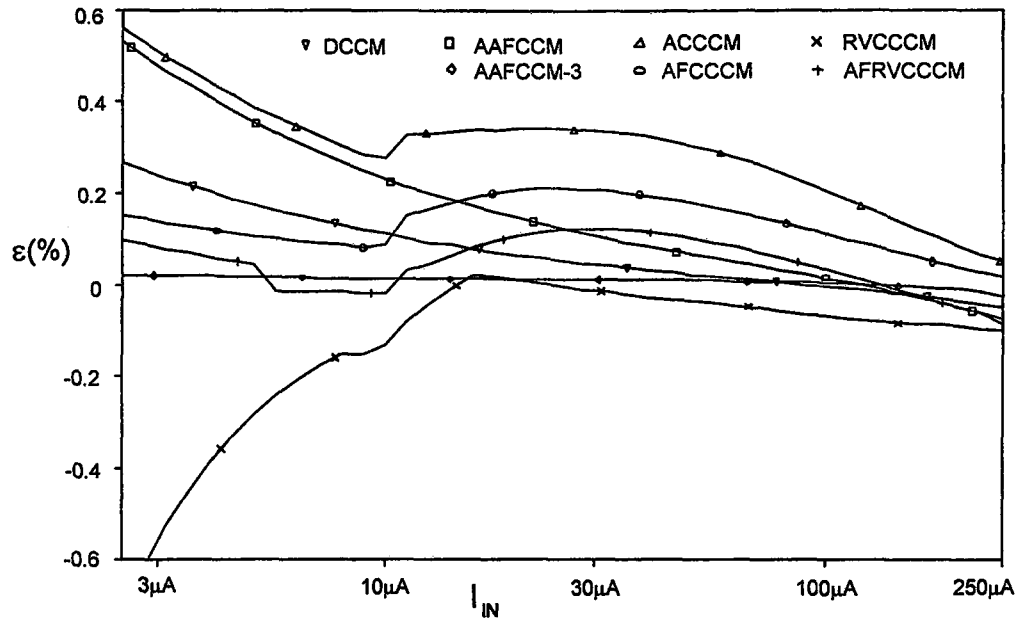


Figure 3.12 Error plots of DCCM and proposed current mirrors (V_{OUT}=3V).

In Figure 3.12, the error in the output current is plotted for the proposed current mirrors and the classical double cascode current mirror, for I_{IN}=2.5μA -250μA range, where V_{OUT}=3 V. It is appearent that, all proposed current mirrors can achieve more than 99.5% current transfer accuracy for the whole range. This precision is lower than the maximum achievable device matching precision, which is typically around 95% and not more than 99.5%, even when advanced layout techniques are used.

Figure 3.12 proves that the highest precision is achieved by AAFCCM-3, proving itself to be very suitable for high precision applications.

The results of all simulations for the current mirrors are summarized in Table 3.3, which allows comparison of DCCM and the proposed seven current mirrors.

Some comments must be made over the obtained results. Taking each current mirror one by one and making brief comments on each feature separately seems reasonable. Therefore, another table for comparing all current mirrors is useful. In Table 3.4, a comparison of the current mirrors based on brief comments are supplied.

Table 3.3 Important parameters of DCCM and the proposed current mirrors, obtained by simulation(R_{OUT} and C_{OUT} values are obtained for $I_{OUT}=I_{IN}=50\mu A$)

	ε [%]	R_{OUT} [Ω]	C_{OUT} [fF]	V_{OUTmin} [V]			V_{IN} [V]		
				2.5μA	25μA	250μA	2.5μA	25μA	250μA
DCCM	-0.05 ~ 0.27	39.8 M	6.35	1.1	1.35	2.5	2.075	2.467	3.847
AAFCCM	-0.09 ~ 0.53	2.89 G	3.28	1.05	1.3	2.4	1.037	1.233	1.923
AAFCCM-3	-0.03 ~ 0.02	37 G	3.25	1.05	1.25	2.4	1.037	1.233	1.923
ACCCM	0.06 ~ 0.56	42.6 M	93.4	0.09	0.26	0.85	1.048	1.245	1.945
AFCCCM	0.02 ~ 0.21	5.41 G	47.4	0.1	0.23	0.8	1.048	1.245	1.945
RVCCCM	-0.7 ~ 0.02	40.8 M	86.7	0.1	0.26	0.9	0.165	0.250	0.825
AFRVCCCM	-0.08 ~ 0.12	5.99 G	42.9	0.1	0.24	0.85	0.131	0.238	0.815

Table 3.4 Brief comments on important parameters of DCCM and the proposed current mirrors, to avail easy comparison.

	Accuracy	R_{OUT}	C_{OUT}	V_{OUTmin}	V_{IN}
DCCM	**high**	*insufficient*	**small**	*high*	*very high*
AAFCCM	**high**	**very high**	**small**	*high*	**low**
AAFCCM-3	**very high**	**very high**	**small**	*high*	**low**
ACCCM	**high**	*insufficient*	*large*	**low**	**low**
AFCCCM	**high**	**very high**	*large*	**low**	**low**
RVCCCM	**high**	*insufficient*	*large*	**low**	**very low**
AFRVCCCM	**high**	**very high**	*large*	**low**	**very low**

Table 3.4 shows that if input and output swing limitations is not so strict for a current mirror to be used in an OTA (e.g. power supplies are not low), AAFCCM-3 is the most suitable current mirror among all.

If output swing is important, then AFCCCM is more suitable, however output capacitance is larger for that case. If output node of the current mirror is the output node of the OTA, when a load capacitance large enough (e.g 1pF) is connected at the output node, the effect of this parasitic capacitance on the dominant poe is negligible, however, if this is not the case, then this large output capacitance lowers the non-dominant pole in the OTA.

For very low power supplies (e.g. a single 3.3V supply), AFRVCCCM is the most suitable current mirror for use in an OTA, thanks to its low input and output voltage requirements, however the large output capacitance and parasitics must be taken under consideration.

CHAPTER 4

PROPOSED OTA STRUCTURES

In this chapter, the proposed current mirrors are implemented in symmetrical OTA structures to achieve high performance characteristics. The success of high performance achievement is proven by computer simulations (schematic and post-layout simulations).

4.1 IMPLEMENTATION of PROPOSED BUILDING BLOCKS in OTA STRUCTURES

Implementation of the proposed building blocks in OTA structures is carried out not directly but in an economical way of design. That is to say, some parts of the proposed current mirrors can be eliminated in the OTA structures, thus supplying area and power savings and less parasitics. For example, Figure 4.1 and Figure 4.2 show two possibilities of implementing AAFCCM in OTA structure, in an economical way. Instead of using separate current reflecting devices (MA, MB and MC) to supply dependent I_K currents for each current mirror, already existing currents or current subtraction techniques are utilized.

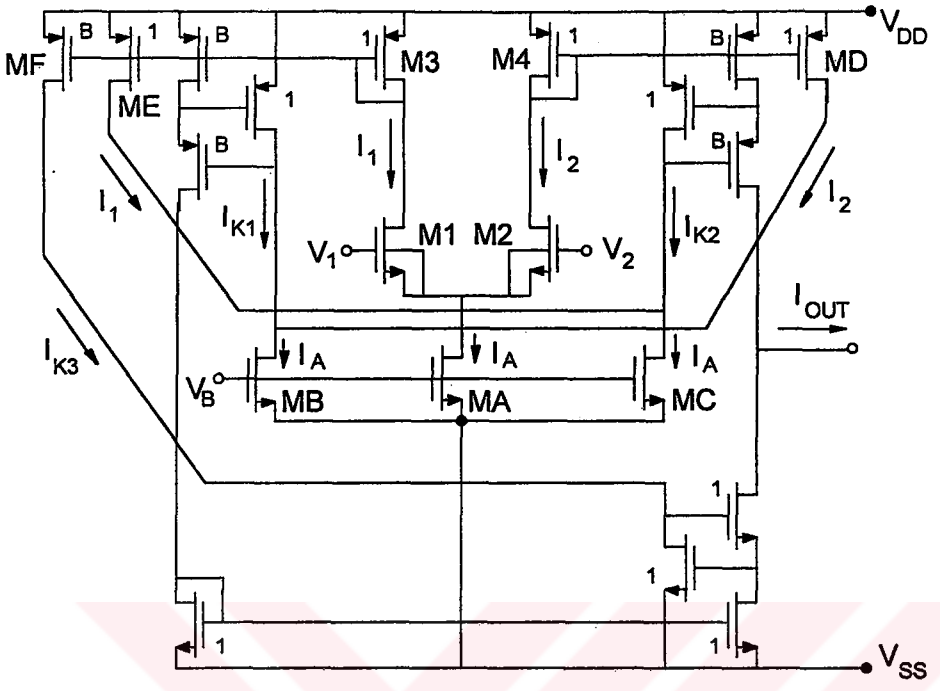


Figure 4.1 An implementation of active-feedback cascode OTA.

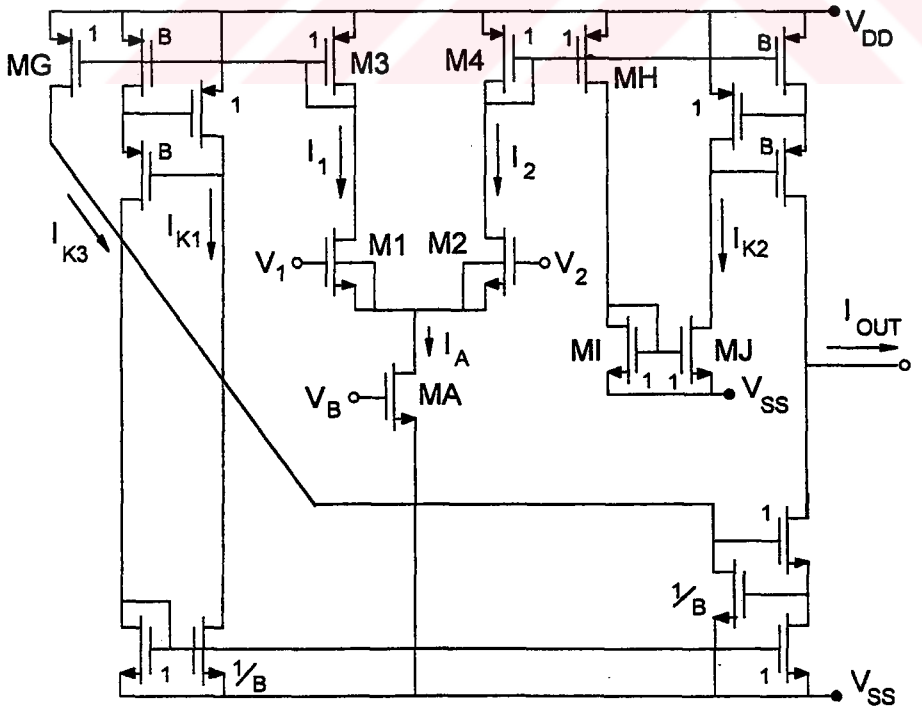


Figure 4.2 Another implementation of active-feedback cascode OTA.

The OTA structure of Figure 4.1 has been designed such that, dependent bias currents for the active-feedback cascode stages are $I_{K1}=I_1$, $I_{K2}=I_2$ and $I_{K3}=BI_1$ which are supplied by M_B, M_C, M_D, M_E and M_F, utilizing current subtraction, such that, since $I_1+I_2=I_A$,

$$I_{K1}=I_A-I_2=I_1 \tag{4.1}$$

$$I_{K2}=I_A-I_1=I_2 \tag{4.2}$$

is achieved easily. $I_{K3}=BI_1$ is directly supplied by M_F.

In Figure 4.2, no current subtraction is used, instead, already inverted currents are utilized.

Implementation of active feedback compact cascode current mirror is also not direct; since accuracy does not rely on active-feedback in that current mirror, only output stage current mirrors are made active-feedback (Figure 4.3). The n factor is chosen larger (n=20) in PMOS current mirrors, to compensate for the body effect, which reduces δ.

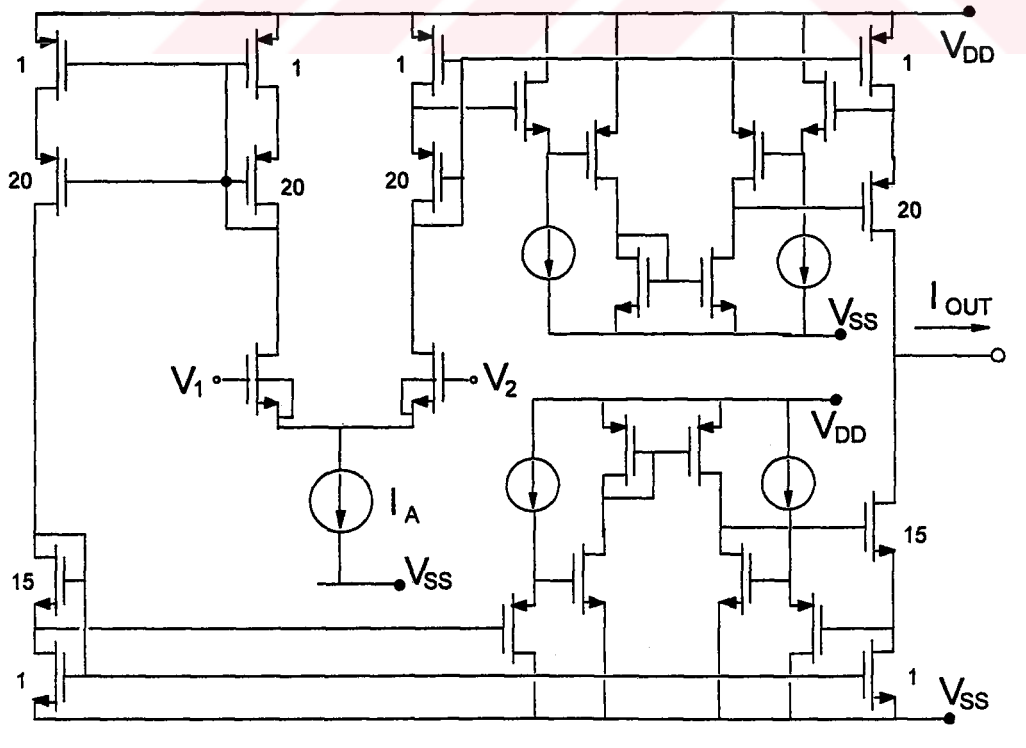


Figure 4.3 Implementation of active-feedback compact cascode OTA.

In Figure 4.4, implementation of AAFCCM-3 is shown. The economical use of devices is apparent. Also, power consumption is aimed to be kept low, therefore, additional blocks supplying active-feedback are operated at 10 times lower currents than the main devices, as shown on Figure 4.4

The tail current source I_A to be used in OTA structures should possess high output resistance and low output compliance. Therefore, current source I_A in the given structures is realized with compact cascode structures as shown in Figure 4.5

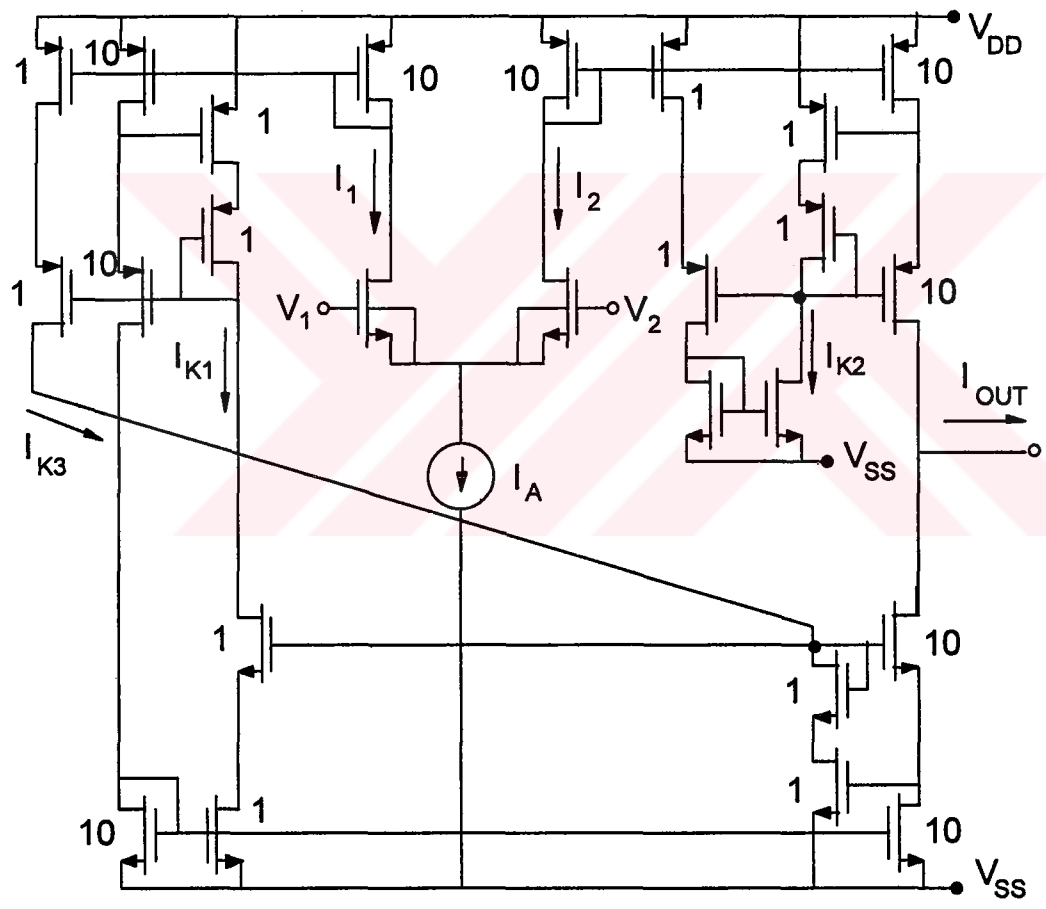


Figure 4.4 An implementation of AAFCCM-3 in OTA.

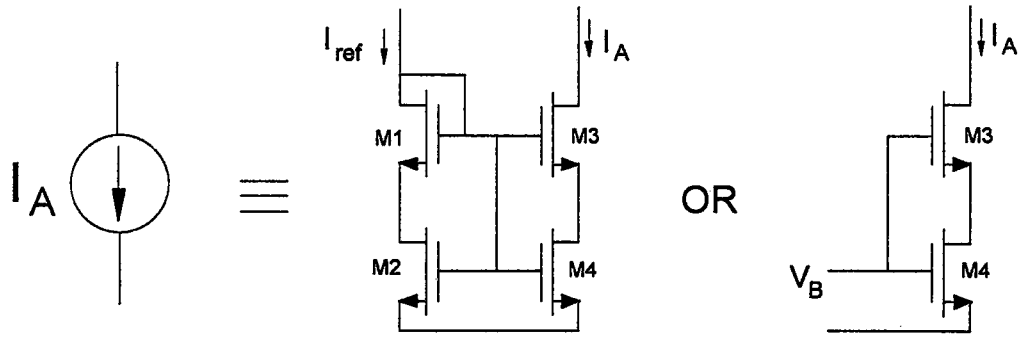


Figure 4.5 Structures to be used as tail current source I_A.

4.2 PERFORMANCE VERIFICATION of the PROPOSED OTA STRUCTURES

Recently, the active-feedback cascode OTA of Figure 4.1 was compared with an equivalent classical cascode OTA, where the biasing conditions, transistor aspect ratios and G_m parameter were kept same[59].

In Figure 4.6, frequency responses for the simple OTA-C integrator, employing the active-feedback cascode OTA and classical cascode OTA have been shown, where C_L=5pF. It is obvious that the proposed circuit enhances OTA-C integrator to be almost lossless down to 50 Hz, where the classical cascode OTA-C integrator is lossy below 5kHz; the improvement is almost 2 decades. The reason for this improvement is the significant increase in the output resistance in the new circuit.

So as to show the effect of this non-ideality in OTA-C active networks, the band-pass filter (BPF) structure [62] of Figure 4.7 has been simulated by utilizing the active-feedback cascode OTA of Figure 4.1 and an equivalent classical cascode OTA. The frequency responses for two cases can be observed from Figure 4.8.

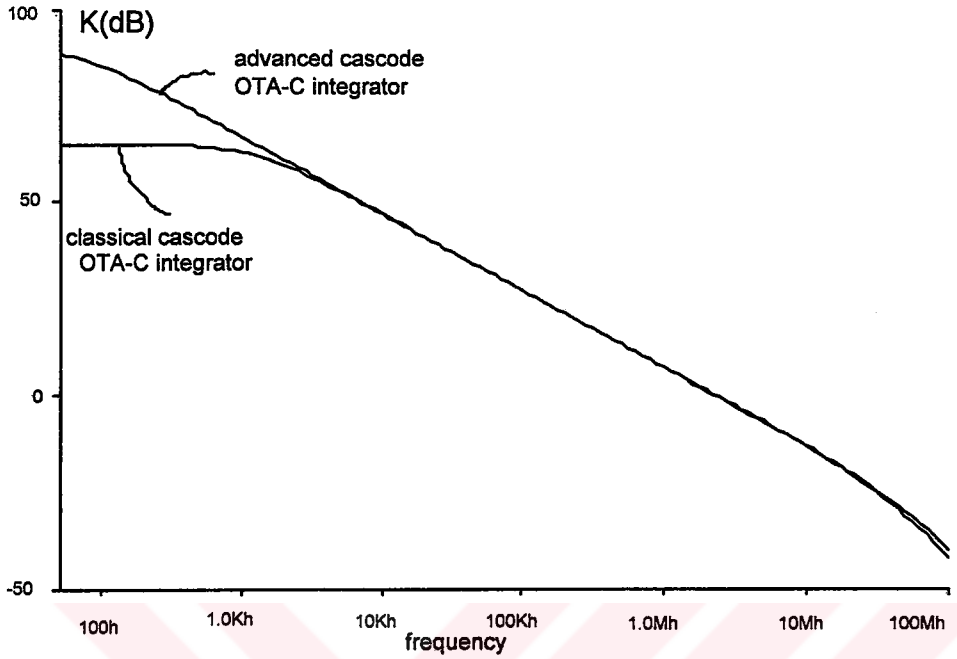


Figure 4.6 Integrator behavior of active-feedback cascode (Fig. 4.1) and classical cascode OTAs. (C_L=5pF)

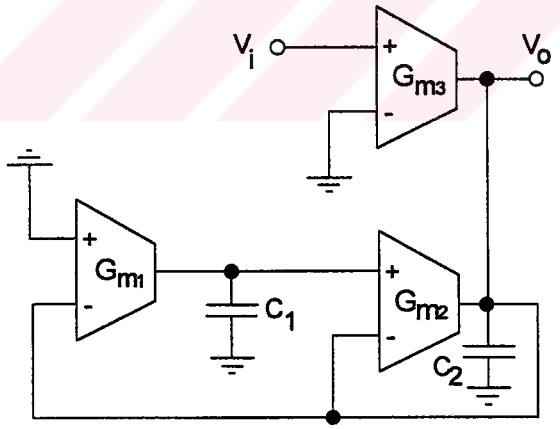


Figure 4.7 OTA-C band-pass filter.

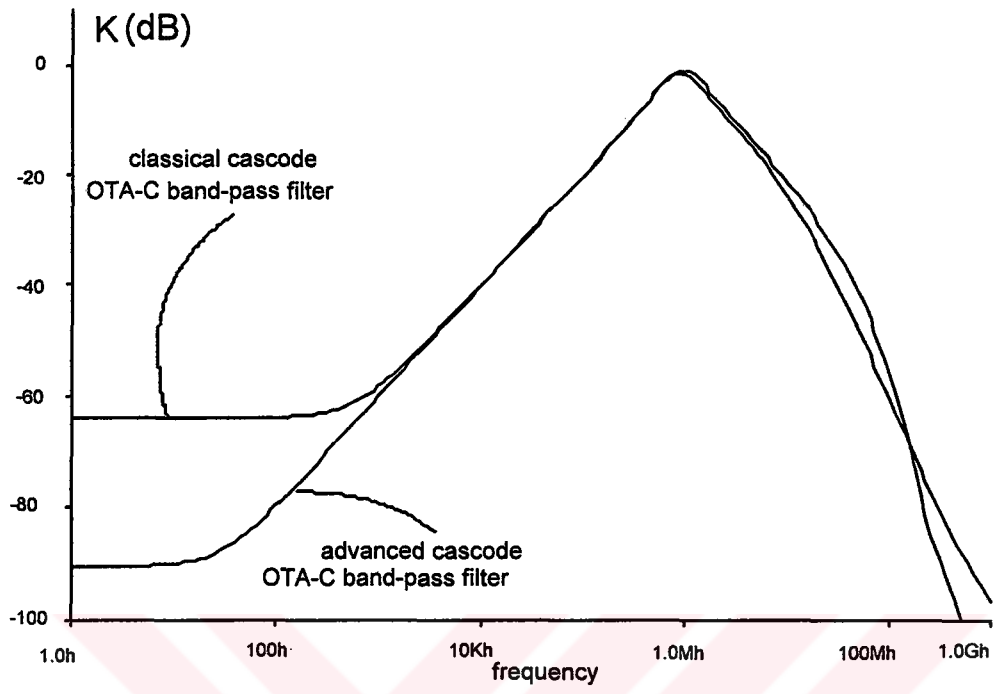


Figure 4.8 Frequency responses of OTA-C band-pass filters built with the active-feedback cascode OTA and an equivalent classical cascode OTA.

The attenuation for classical cascode OTA-C band-pass filter at low frequencies is about 65dB. However, the new OTA structure supplies about 90dB. Note that for the same band-pass filter structure employing the simple symmetrical OTA of Figure 2.2 would supply only about 20-30dB attenuation for low frequencies.

Active-feedback OTAs of Figure 4.3 and 4.4 were analyzed by simulation and compared with an equivalent classical cascode OTA in Table 4.1. G_m parameters of all OTAs were made same (G_m=60μS was achieved by choosing $(W/L)_1=(W/L)_2$=12μm/5μm and using the current source structures shown in Figure 4.5, as tail current, where I_A=30μA). Supply voltages are V_{SS}=-5V, V_{DD}=5V and minimum channel lengths are L=5μm. B was chosen unity.

DC Gain enhancement in proposed OTAs with respect to the equivalent classical cascode OTA is because of the boosted output resistance, which is

supplied by active-feedback current mirrors. Nevertheless, power consumption did not increase seriously with respect to the classical cascode OTA.

Table 4.1 Performance characteristics of simulated cascode OTAs.

	Classical cascode OTA	AFB cascode OTA	AFB compact cascode OTA
DC Gain	87.05 dB	146.4 dB	128.1 dB
GBW	169 MHz	209 MHz	49 MHz
R_{OUT}	388.4 MΩ	360 GΩ	41.5 GΩ
C_{OUT}	54.6 fF	44.2 fF	199 fF
f_{nd}	16.7 MHz	29.2 MHz	8.6 MHz
C_{Lmin}	498 fF	272 fF	933 fF
$PSRR_{DD}$	DC : 116dB f=1kHz : 116dB f=100kHz : 100dB f=1MHz : 83dB f=10MHz : 52dB	DC : 100dB f=1kHz : 115dB f=100kHz : 90dB f=1MHz : 67dB f=10MHz : 40dB	DC : 81dB f=1kHz : 96dB f=100kHz : 94dB f=1MHz : 66dB f=10MHz : 36dB
$PSRR_{SS}$	DC: 87dB f=1kHz : 87dB f=100kHz : 78dB f=1MHz : 61dB f=10MHz : 41dB	DC: 100dB f=1kHz : 115dB f=100kHz : 87dB f=1MHz : 67dB f=10MHz : 52dB	DC : 81dB f=1kHz : 96dB f=100kHz : 70dB f=1MHz : 50dB f=10MHz : 34dB
output swing	-3.7 V ~ 3.6 V	-3.85 V ~ 3.85 V	-4.6 V ~ 4.4 V
V_{offset}	110 μV	73 μV	4 mV
CMRR	87.3 dB	162.1 dB	120.8 dB
Power dissipation	0.58 mW	0.63 mW	1.15 mW

Output capacitance of active-feedback cascode OTA (Figure 4.3) is smaller than output capacitance of classical cascode OTA, thanks to the lower output capacitance value of employed active-feedback current mirrors with respect to double cascode current mirrors. This brought an improvement in GBW of active-feedback cascode OTA, with respect to the classical cascode OTA. A prediction which came out to be true is the relatively larger output capacitance of the active-feedback compact cascode OTA, degrading its GBW. This large capacitance is due to the employed current mirrors. It was mentioned before and will be proven by simulation that, when a sufficiently large load capacitor is coupled to the output, the output capacitance will have almost no effect, however, a similar capacitance from the internal current mirrors will bring

a relatively lower non-dominant pole f_{nd} with respect to other simulated OTAs (See Table), thus degrading high frequency behavior of the active-feedback compact cascode OTA. This will also be revealed by simulation.

A sufficiently large load capacitor guarantees stability for a unity-gain feedback configuration (which is usually used to obtain an equivalent resistance equal to G_m^{-1}). The minimum required C_L values for a stable unity-gain feedback configuration were determined utilizing C_{OUT}, f_{nd} and GBW values. The results are close to each other, but a bit worse for the active-feedback compact cascode OTA. It is worth mentioning once agin that this compensation capacitor is generally not required in integrator structures, therefore the simulated OTAs can be operated as integrators down to their GBW frequencies, provided that they utilize their parasitic capacitances as their integrator capacitors.

Output swing of the active-feedback cascode OTA is slightly better than that of the classical cascode OTA. This is because of the high output resistance of the former [69], [95], [101], as was mentioned before. However, output swing of the active-feedback compact cascode OTA is much wider with respect to both of those OTAs. This enables it to operate effectively with, for instance, a single 3.3 V dc supply.

The PSRR, CMRR and V_{os} features in the table may be misleading since no mismatch analysis (device mismatches affect these features strongly) were carried out. Since the classical cascode OTA has a much more symmetrical structure, an analysis without mismatches may result in a mistakenly high performance. Nevertheless, looking at the table, one can get the idea that the proposed OTAs can achieve comparable performance characteristics (corresponding to PSRR, CMRR and V_{os}) with respect to the classical cascode OTA.

The three OTAs were used as OTA-C integrators with a load capacitor of value $C_L = 1pF$ for each. The gain and phase plots are given in Figure 4.9. It is clear that very high output resistance values of the proposed OTAs enable lossless integration at very low frequencies, where the classical cascode OTA-C

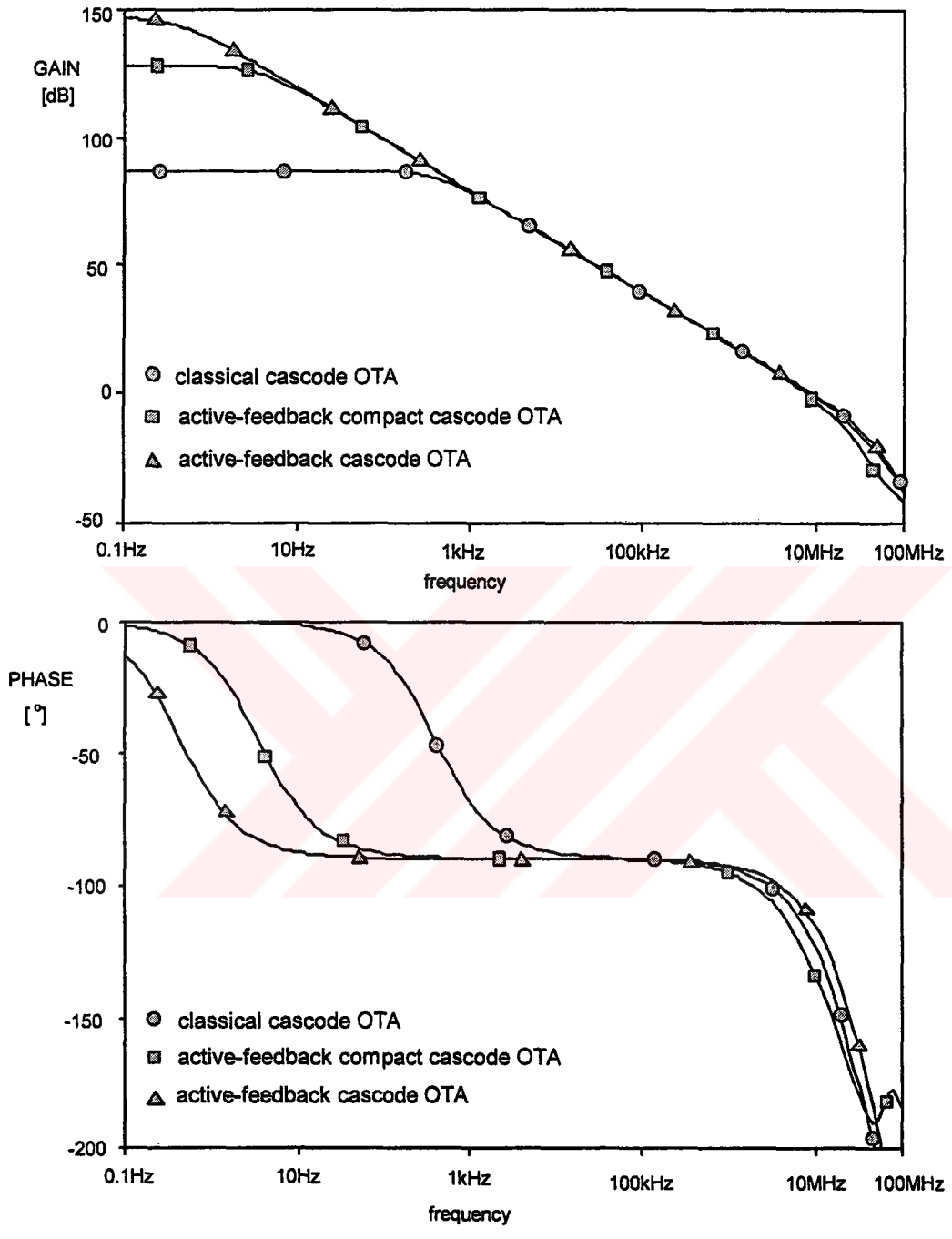


Figure 4.9 Frequency responses of three OTA-C integrators (C_L=1pF) employing proposed active-feedback OTAs and an equivalent classical cascode OTA.

integrator is absolutely lossy below the kHz range. The lower non-dominant pole frequency of the active-feedback compact cascode OTA caused a slight degradation at high frequencies. It should be noted that, output capacitance doesn't have a significant effect on integration since the load capacitor C_L is

dominant. This can be observed from the plots, where all three OTA-C integrators act the same way within the proper operating frequency range, i.e. the range within which $\phi \approx -90^{o}$ (A method to minimize this is acoounting for the value of C_{OUT} in the integrator capacitor such that $C_{Leff} = C_L + C_{OUT} = 1pF$).

As mentioned before, fully balanced structures can achieve much better PSRR, CMRR, distortion, slew rate and input/output swing performances [8], [16], [29], [40], [84]. Fully balanced OTA (Differential-output OTA: DOTA) structures are also possible with the proposed structures. A fully-balanced active-feedback cascode DOTA is given in Figure 4.10. Note that this structure enables simpler achievement of the dependent I_K currents of each active-feedback stage. This DOTA is simulated with PSpice and compared with an equivalent classical cascode DOTA. The simulation results are supplied in Table 4.2, Table 4.3 and Figure 4.11.

Table 4.2 supplies a list of performance properties of the simulated cascode DOTAs. Note that, R_{OUT} and C_{OUT} are now the differential (i.e. floating) small signal output resistances and capacitances of the DOTAs. To obtain a The main disadvantage of the proposed active-feedback cascode DOTA structure is the increase in power dissipation, which is only about %10 with respect to its classical cascode counterpart. This is a price to be paid to achieve the other better performance characteristics (especially higher R_{OUT}, lower C_{OUT}, thus higher DC gain and higher GBW).

It is worth mentioning that PSRR, CMRR and V_{offset} are not supplied for the simulated DOTAs because these values were found absolutely very close to their ideal values, thanks to the fully-balanced structures. Though this gives an idea about the PSRR, CMRR and offset performance improvement of the DOTA structures, device mismatches will affect these parameters and they will take more realistic values (A mismatch analysis can supply these realistic values).

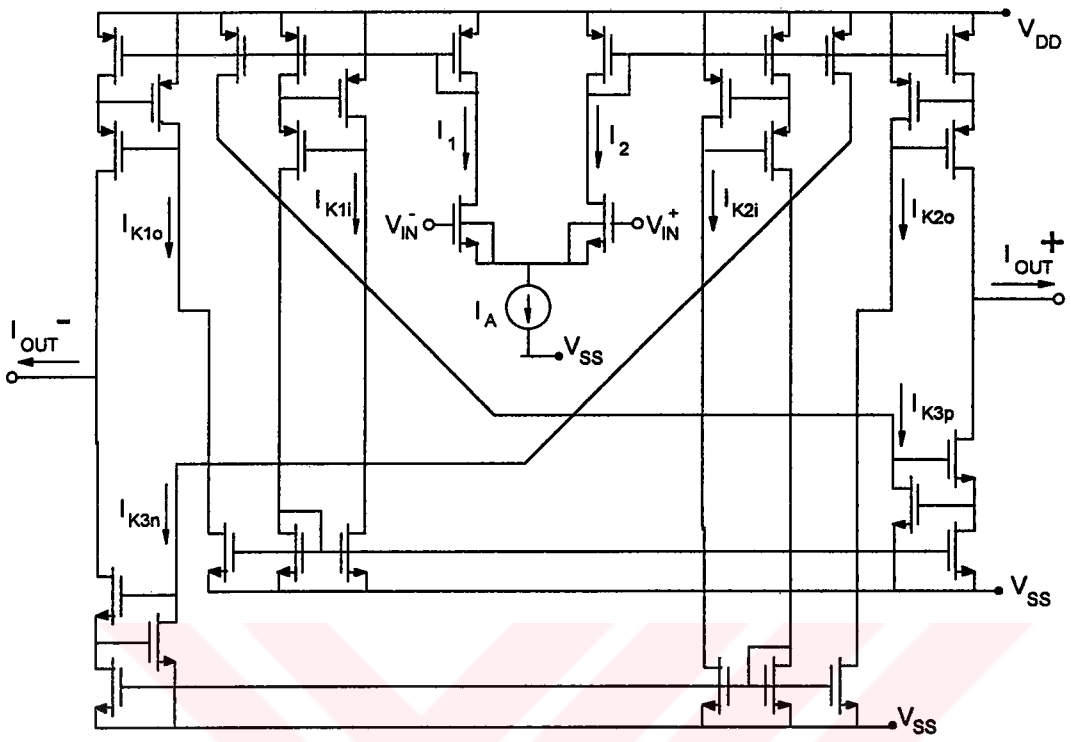


Figure 4.10 Novel differential-output active-feedback OTA.

Table 4.2 Performance characteristics of simulated cascode DOTAs.

	Classical cascode DOTA	AFB cascode DOTA
Differential DC Gain	91.67 dB	132.6 dB
GBW	276 MHz	372.8 MHz
R_{OUT}	659.2 MΩ	35.74 GΩ
C_{OUT}	33.5 fF	25.6 fF
f_{nd}	13.5 MHz	28 MHz
C_{Lmin}	650 fF	315 fF
Power dissipation	0.9 mW	0.995 mW

As a consequence, the PSRR, CMRR and offset characteristics of DOTAs are much better with respect to those of equivalent single-output OTAs, wherein several imbalances exist degrading PSRR, CMRR and offset characteristics.

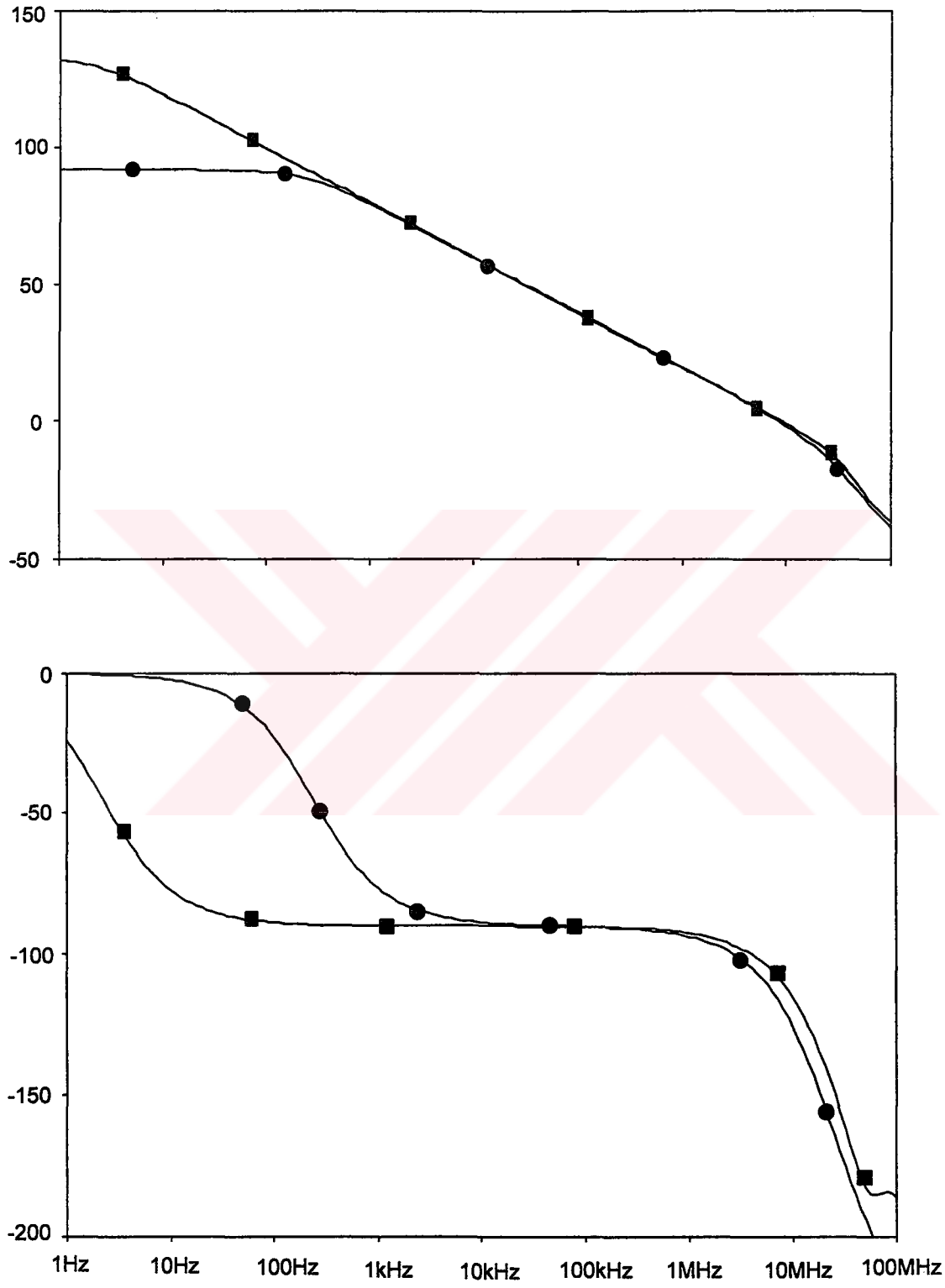


Figure 4.11 Frequency responses of DOTA-C integrators (C_L=1pF).
■: Active-feedback DOTA (Fig.4.10).●: An equivalent classical cascode DOTA.

Figure 4.11 shows the gain and phase responses of two DOTA-C integrators (C_L=1pF) constructed with active-feedback and classical cascode DOTAs, respectively (Note that, a DOTA-C integrator employs a load capacitor C_L connected across two output terminals of a DOTA, while the input is fully-differential, i.e. $V_{i1} = -V_{i2}$). It is again clear from the AC plots that the proposed active-feedback DOTA-C integrator achieves lossless integration within a much wider frequency range with respect to that of the equivalent classical cascode DOTA-C filter. The phase error characteristics of the simulated DOTA-C integrators are compared in Table 4.3. The range within which $\phi = -90° \pm 10°$ and the range within which $\phi = -90° \pm 1°$ are supplied to avail easy comparison. Both of these ranges are much wider for the proposed active-feedback DOTA-C integrator with respect to those of the equivalent classical cascode DOTA-C integrator.

Table 4.3 Comparison of phase errors of simulated DOTA-C integrators.

	Classical cascode DOTA-C integrator	**AFB cascode DOTA-C integrator**
$\phi = -80°$	f = 1.32 kHz	f = 12.3 Hz
$\phi = -100°$	f = 2.15 MHz	f = 3.9 MHz
$\phi = -89.1°$	f = 12.6 kHz	f = 123 Hz
$\phi = -90.9°$	f = 227 kHz	f = 393 kHz

The layout of the DOTA structure of Figure 4.10 is drawn for AMS 0.8μm n-well CMOS technology (Austria Mikro Systeme International) and post-layout simulations are performed (using SpectreS simulation) with aid of Cadence. The layout of the circuit which lies in a 95μm x 245μm area, is shown in Figure 4.12. The circuit is biased from a single DC supply of V_{DD}=5V, while input and output terminals are at 2.5V for DC operation. All channel lengths are 1.5 μm. Channel widths are 6 μm for the p-channel input devices, 30 μm and 60 μm for the basic n-channel and p-channel devices in current mirrors, respectively. The tail current is 55 μA to supply G_m=50.8μS.

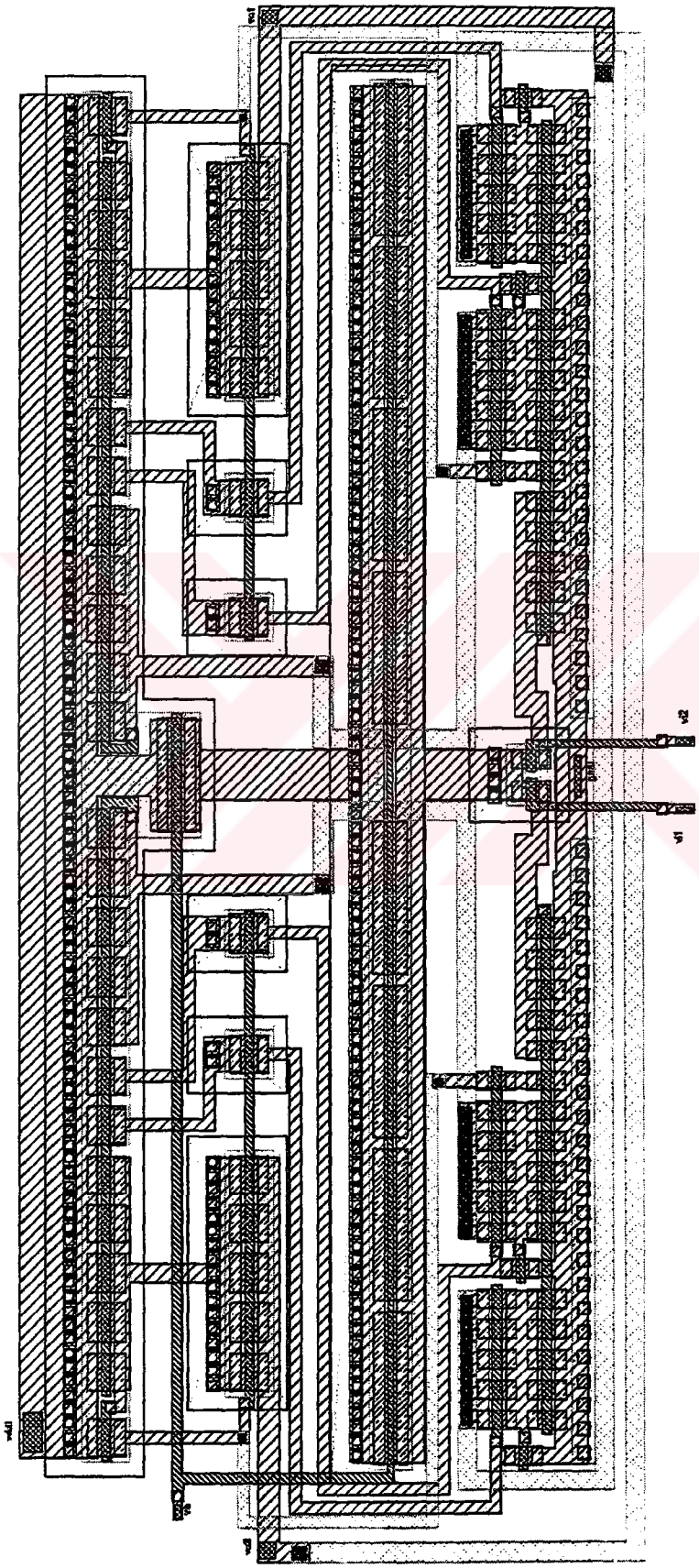


Figure 4.12 Layout of the active feedback cascode DOTA

The reduction factor κ in the active-feedback current mirrors are chosen 5 for reducing excess power dissipation with respect to a classical cascode DOTA. Thus, the auxillary transistors' channel widths are 6 μm for the n-channel and 12 μm for the p-channel devices, respectively. The simulation results are summarized in Table 4.4.

Table 4.4 Performance characteristics of the active-feedback cascode DOTA obtained by post-layout simulations with SpectreS.

DC Gain (differential)	131.6 dB
GBW	93.7 MHz
R_{OUT}	74.4 GΩ
C_{OUT}	86.2 fF
f_{nd}	90.5 MHz
C_{Lmin}	3.05 fF
Power dissipation	0.986 mW

CHAPTER 5

CONCLUSION

This work was based mainly on the fact that, use of conventional cascode structures cannot supply the performance requirements of an OTA to be used in OTA-C continuous-time filters or oscillators. Commonly used cascode structures were analyzed and drawbacks of each were revealed. It was shown that, none of the conventional cascode structures can avail all of the performance characteristics of an OTA which are needed for proper filtering in OTA-C structures. Therefore, developing some new building blocks is a must.

The proposed novel building blocks helped building high performance OTA structures suitable for use in OTA-C filters and oscillators. The original use of active-feedback in the current mirrors supplied the OTAs with very high output resistance values and low offsets. As has already been revealed, the new OTA structures have many advantages over a classical cascode OTA, which is used very frequently. However, it has been proven that the new structures can be designed with an economical manner, such that power consumption, parasitics and complexity can be minimized. Actually, as has been shown in the fourth chapter, it is possible to keep the excess power consumption of the active-feedback cascode OTA less than 10% (with respect total power consumption that of an equivalent classical cascode OTA). Furthermore, thanks to halving of the output capacitances of the internal current mirrors (those which are not directly coupled to the output node), the effects of parasitics were less in the active-feedback cascode OTA.

Thanks to various structures proposed in this work, it is possible to choose a suitable OTA structure that fits the demand of the designer. For example, when very high output swing is required, an active-feedback compact

cascode OTA can be used. If the OTA is aimed to be operated with low supply voltages (e.g. a single 3.3 V supply), then an active-feedback compact cascode OTA employing 'reduced-V_{IN} current mirrors' can be used. If a very high output resistance is not required, then instead of active-feedback, plain compact cascode structures are more useful than classical cascode ones.

Advanced linearity enhancement techniques for the input stage was kept out of scope of this work, because too much works have been carried out on that topic and a saturation point has almost been reached; however, as revealed in the second chapter, most of the non-idealities arise from the current-mode blocks, like current mirrors/sources, which have not received sufficient improvement proposals upon today. Nevertheless, the proposed OTAs can be built with linearized transconductors to achieve high linearity and slew rate performances.

The structures proposed in this work were aimed to be easy-to-design, VLSI-compatible and power-saving, while possessing high performance characteristics. Therefore they have a great chance to be widely used in high precision analog design in a very near future. Particularly, proposed building blocks offer very high performance structures to the current-mode analog integrated circuit design, which is attracting dense interest at the moment, as standard supply voltages of complete-system chips run beyond 3.3V. An application of the introduced techniques in current-mode design has already been introduced recently [69].

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APPENDIX

MOSFET MODEL PARAMETERS UTILIZED in SIMULATIONS

Table A.1 Model parameters of TÜBİTAK-YİTAL 3μm n-well CMOS process.

.MODEL NYITAL NMOS LEVEL=2 VTO=.99 TOX=400E-10 NSUB=7E15 XJ=.18U LD=.341U UO=710 VMAX=1.5E5 DELTA=.3 THETA=.15 ETA=.15 KAPPA=.6 TPG=1 GAMMA=.65 NFS=2.4E11 CGSO=87P CGDO=87P CGBO=27.9P PB=.6 CJ=1.78E-4 JS=8.2E-8 MJ=.481 CJSW=358P MJSW=.218 LAMBDA=.02

.MODEL PYITAL PMOS LEVEL=2 VTO=-.8 TOX=400E-10 NSUB=4E15 XJ=.21U LD=.45U UO=300 VMAX=3E4 DELTA=.75 THETA=.4 ETA=.15 KAPPA=1.5 TPG=-1 GAMMA=.46 NFS=1.68E11 CGSO=124P CGDO=.124N CGBO=40.3P PB=.6 CJ=1.83E-4 JS=3.46E-8 MJ=.526 CJSW=229P MJSW=.172 LAMBDA=.01

Table A.2 Model parameters of AMS 0.8μm n-well CMOS process.

.MODEL NAMS NMOS LEVEL=2 UO=462 VTO=.844 NFS=.835E12 TOX=15.5E-9 NSUB=63.8E15 UCRIT=37.7E4 UEXP=0.324 VMAX=61.9E3 RSH=25 XJ=0.08E-6 LD=0.060E-6 DELTA=0.237 PB=.860 JS=0.01E-3 NEFF=10 CJ=0.290E-3 MJ=460E-3 CJSW=0.230E-9 MJSW=.33 CGSO=.035E-9 CGDO=.35E-9 CGBO=0.15E-9 UTRA=0 WD=0.580E-6 KF=0.276E-25 AF=1.53

.MODEL PAMS PMOS LEVEL=2 UO=160 VTO=-.734 NFS=.483E12 TOX=15.5E-9 NSUB=32.8E16 UCRIT=30.8E4 UEXP=0.336 VMAX=61.3E3 RSH=47 XJ=0.087E-6 LD=-0.076E-6 DELTA=0.949 PB=.8 JS=0.04E-3 NEFF=2.57 CJ=.49E-3 MJ=0.47 CJSW=0.21E-9 MJSW=.29 CGSO=0.350E-9 CGDO=0.350E-9 CGBO=0.15E-9 UTRA=0 WD=0.331E-6 KF=0.466E-26 AF=1.61

BIOGRAPHY

Ali Zeki was born in Cyprus in 1968. He completed his primary and secondary education in Çayırova İlkokulu in 1980 and in Türk Maarif Koleji in 1986, respectively. He received the B.Sc. and the M.Sc. degrees in electronics and communication engineering from Istanbul Technical University Faculty of Electrical and Electronics Engineering Department of Electronics and Communication Engineering in 1990 and Istanbul Technical University Institute of Science and Technology Department of Electronics and Communication Engineering in 1993, respectively. Since 1991, he has been a research assistant at the Department of Electronics and Engineering of Istanbul Technical University Faculty of Electrical and Electronics Engineering. During November 1995 - February 1996 he was in Japan for the 'Microcomputers' course organized by Japan International Cooperation Agency. His research interests includes analog integrated circuit design and semiconductor device modeling.