İSTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY



# HIGH EFFICIENCY 1 W CLASS B PUSH-PULL AMPLIFIER DESIGN FOR HIPERLAN/2

M.Sc. Thesis by

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# HIPERLAN/2 UYGULAMALARI İÇİN YÜKSEK VERİMLİ 1W B SINIFI SİMETRİK GÜÇ KUVETLENDİRİCİ TASARIMI

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## ABBREVIATIONS

| | |
|---|---|
| **WAN** | : Wide area Network |
| **LAN** | : Local Area Network |
| **HIPERLAN** | : High Performance Local Area Network |
| **RLAN** | : Radio Based Local Area Network |
| **PC** | : Personal Computer |
| **ISM** | : Industrial, Scientific and Medical |
| **ERC** | : Electrical Rules Check |
| **ETSI BRAN** | : European Telecommunications Standards Institute Broadband Radio Access Networks |
| **Mb/s** | : Megabit Per Second |
| **H/1** | : Hiperlan 1 |
| **GHz** | : Gigahertz |
| **US** | : United States |
| **AP** | : Access Point |
| **QoS** | : Quality of Support |
| **OFDM** | : Orthogonal Frequency Division Multiplex |
| **MAC** | : Medium Access Control |
| **MT** | : Mobile Terminal |
| **PCB** | : Printed Circuit Board |
| **RF** | : Radio Frequency |
| **PAE** | : Power Added Efficiency |
| **FET** | : Field Effect Transistor |
| **DC** | : Direct Current |
| **VSWR** | : Voltage Standing Wave Ratio |

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## LIST OF SYMBOLS

| | |
|---|---|
| $w$ | : Width |
| $h$ | : Height |
| $\epsilon_r$ | : Dielectric Constant |
| $\epsilon_0$ | : Dielectric Constant of free space |
| $\epsilon_{eff}$ | : Effective Dielectric Constant |
| $Z_0$ | : Characteristic Impedance |
| $Z_f$ | : Wave Impedance in Free Space |
| $Z_{in}$ | : Input Impedance |
| $Z_L$ | : Load Impedance |
| $Z_r$ | : Impedance of Ring Segments |
| $Z_c$ | : Impedance of Coupled Line |
| $Z_{0e}$ | : Even Mode Impedance |
| $Z_{0o}$ | : Odd Mode Impedance |
| $\mu_0$ | : Permeability |
| $\lambda$ | : Wavelength |
| $c$ | : Speed of Light |
| $f$ | : Frequency |
| $f_0$ | : Center Frequency |
| $V$ | : Voltage |
| $I$ | : Current |
| $\Gamma_0$ | : Reflection Coefficient |
| $T$ | : Thickness |
| **Rho** | : Metal Bulk Resistivity normalized to Gold |
| **dB** | : Decibel |
| $C$ | : Mean value of Coupling in dB |
| $x_1, x_2$ | : Input Signals |
| $y_1, y_2$ | : Output Signals |
| $G$ | : Gain Constant |
| $\eta$ | : Efficiency |
| $P_{1dB}$ | : 1dB Compression Point |
| $IP_{3rd}$ | : Third Order Intercept Point |
| $I_d$ | : Drain Current |
| $P_{dc}$ | : DC Power |
| $V_\Phi$ | : Internal Barrier Voltage of Schottky Diode |
| $\omega_o$ | : Resonance Frequency |

## HIGH EFFICIENCY 1 W CLASS B PUSH-PULL AMPLIFIER DESIGN FOR HIPERLAN/2


### SUMMARY

Developments in computer networks has increased the demand for wide area and local area networks. To make advanced communication systems faster, it is required to use modulation techniques that are highly efficient. For these types of modulation techniques, linearity is an important factor and low noise receiver and transmitter stages are necessary.

By the development of laptop computers, the demand for the Wireless Local Area Network has grown and new standars have emerged. One such standard is Hiperlan/2, which works in the 5.2 to 5.8GHz frequency band. In this thesis, by taking into account that laptop computers operate on low power batteries, a high efficiency power amplifier stage is designed for this type of standard.

In this design, ClassB push-pull amplifier in IC, working between 5.2 and 5.8GHz band, is chosen. Here, GaAS MESFET is used due to its advantages.

In section II, general information about Hiperlan/2 is given.

In section III, characteristics of transmission lines are investigated and instead of using a transformer which is necessary for push-pull type to form 180 degree phase diffrence signals, another solution suitable for IC is studied and the modified ring hybrid is defined. Simulation results for this hybrid are also presented.

In section IV, linear and non-linear circuits and power amplifier types are examined. A Class B push-pull amplifier stage is designed and necessary design changes are applied to increase the efficiency.

**HIPERLAN/2 UYGULAMALARI İÇİN YÜKSEK VERİMLİ 1W B -SINIFI SİMETRİK GÜÇ KUVVETLENDİRİCİ TASARIMI**

## ÖZET


Bilgisayar ağlarının gelişimi, geniş alan ağlarına ve yerel ağlara olan talebi arttırmıştır. Gelişmiş haberleşme sistemlerinin daha hızlı olabilmesi, haberleşme bandını daha verimli kullanan modülasyon türleri kullanılması ile mümkündür. Bu tip modülasyon türleri için doğrusallık önemlidir ve düşük gürültülü alıcı ve vericilere ihtiyaç duyulmaktadır.

Taşınabilir bilgisayarların gelişimi ile kablosuz yerel ağ bağlantılar önem kazanmış ve çeşitli standartlar ortaya çıkmıştır. Bunlardan biri olan Hiperlan/2 standardı, 5.2 ile 5.8GHz bandında çalışan ve yüksek performanslı bir standarttır. Bu çalışmada, bu tür standarda yönelik, taşınabilir bilgisayarların da pille çalıştığı düşünülerek, yüksek verimliliği olan güç kuvvetlendiricisi tasarlanmıştır.

Bu tasarımda, tümleşik devre içerisinde olan ve 5.2 ile 5.8GHz bandında çalışan simetrik B sınıfı güç kuvvetlendiricisi tercih edilmiştir. Burada GaAS MESFET kullanılmıştır.

İkinci bölümde genel olarak Hiperlan/2 standardı hakkında temel bilgiler verilmiştir.

Üçüncü bölümde ise, iletim hatlarının özellikleri incelenmiş ve simetrik kuvvetlendiricide gerekli olan ve 180 derece faz farkına sahip iki işaret oluşturan trafo yerine, tümleşik devreye uygun genişbantlı bir çözüm aranmış ve bu durum için geliştirilmiş halka hibriti tanımlanmıştır. Bu halka hibrit ile ilgili olarak simülasyon sonuçları sunulmuştur.

Dördüncü bölümde ise, doğrusal ve doğrusal olmayan devreler ile güç kuvvetlendirici tipleri incelenmiştir. Simetrik B sınıfı tipi devre tasarlanmış ve yüksek verimli olabilmesi için gerekli durumlar araştırılmıştır.

# 1. INTRODUCTION

Computer networks began to emerge in the late 1960's with the introduction of the first wide area network (WAN). With WAN's growing through the 70's and 80's and local area networks (LAN) beginning to gain acceptance in the 80's, it became apparent that networking capability was the future of modern computer infrastructures. Since that time, technologies to enhance both WANs and LANs have been high demand. At first, networks were only established at large corporations; however, today it is not uncommon to see small networks within a small office or even a person's home. As a result, most people have come to depend on network connections. This had lead to the era of abundant transfer of information known as the Information Age. As demand grows for Internet and Intranet access, the following shortcomings of network implementations have been discovered: connections in rural areas, rising expenses, and inflexibility [2].

Network technology is widely accessible in large metropolitan areas for use by corporations, public uses, and educational institutions. However, as distance from the city grows so does the lack of these technologies. For corporations, this barrier is easily overcome, but schools and individuals do not posses the means or the knowledge necessary to overcome this barrier. To satisfy network demands, there are increasing costs to implement networks capable of effectively handling user demand. As needs change, networks must be able to easily adapt and expand. Currently, this is not the case with widely used networks. A specific network may be limited to a certain amount of accessible and active network connections based on pre-wiring. It is extremely difficult, if not impossible, to exceed the current number of available connections to a particular network without massive re-wiring of the building and the introduction of new hardware. With the problems of connections to rural areas, costs, and inflexibility. These problems are only continuing to grow as demand continues to grow so new technologies are beginning to emerge. One possible solution is wireless LANs [3].

WLAN standards are currently under development. They are Hiperlan/2 and IEEE802.11a. Both will work in 5 – 6GHz using OFDM modulation, so linear power amplifiers are highly demanded. Another important point is the power consumption. Because these standards will work, especially by laptops, power consumption is an important point. To have an efficient power amplifier, push-pull amplifier can be used. Due to the modulation technique, the most suitable class is ClassB amplifier. Class B amplifier has higher efficiency than ClassA amplifier, and also the input signal is not distorted in this type of amplifier.

To realize the push-pull type amplifier, a transformer is necessary, but realizing transformer in an IC is very difficult. This transformer is to be used in 5.2 – 5.8GHz frequency range. The transformers at the input and output can be designed on GaAs substrate as ring hybrid. A modified ring hybrid is proposed by March, S. in 1968. By making some design changes this modfied ring hybrid can be broadbanded [6].

GaAs technology offers low cost solutions for realizing these type of circuits. In this technology, the transistor cut off frequency $f_T$ is obtained over 50Ghz and maximum oscillation frequency $f_{max}$ is obtained over 40GHz. Furthermore noise figure level is very low in this technology compared to others.

Another important point is to define a non linear MESFET model which will be used in the simulation and have proper results, so that the simulation results can be assumed as they will not be so much different from the realized circuit [13].

To increase the efficiency, some techniques reducing the harmonic power is investigated. One of the methods is proposed by Bahl, J.; Griffin, E. in 1989. In this design some design changes is made to reduce the area [11].

Single ended amplfiers proposed in 1986 is modified to get a push-pull type amplifier [12].

# 2 THE HIPERLAN/2 NETWORK

HIPERLANs (High Performance Radio Local Area Networks) are radio based local area networking (RLAN) solutions, intended for connectivity between traditional business products such as PCs, laptops, workstations, servers, printers and other networking equipment as well as digital consumer electronic equipment in the wireless home network environment. HIPERLANs thus enable the replacement of physical cables for the connection of data networks within a building, providing a more flexible and, possibly, a more economic approach to the installation, reconfiguration and use of such networks within the business and industrial environments.

Existing RLANs and other wide band data transmission systems are already operating in the ISM frequency bands. In order to ensure high reliability and high data transfer rates HIPERLANs, however, require a predictable sharing environment. The ISM bands are, therefore, not suitable to meet the requirement of HIPERLANs and other frequency bands have been identified for these kinds of services.

In 1996, the ERC adopted ERC/DEC/(96)03, "on the harmonised frequency band to be designated for the introduction of High Performance Radio Local Area Networks (HIPERLANs)". This Decision harmonised the use of the band 5150-5250 MHz for HIPERLANs [1].

## 2.1 Introduction to HIPERLAN/2

ETSI BRAN (European Telecommunications Standards Institute Broadband Radio Access Networks) develops standards and specifications for broadband radio access networks that cover a wide range of applications intended for different frequency bands. A system currently being specified by BRAN is HIPERLAN type 2 (H/2) which will provide high speed (up to 54 Mb/s data rate) communications between portable computing devices attached to an IP, ATM or UMTS backbone network. H/2 will be capable of supporting multimedia applications and the typical operation

environment is indoor with restricted user mobility. In Europe, the frequency band 5.15-5.25 GHz currently allocated to H/1, will most likely be available also for H/2 systems. Additional spectrum above 5.25 GHz may also be available for H/2 systems, which than will share the spectrum with earth exploring satellites and/or radar equipment. H/2 can also be deployed in the U-NII band in the US. Here it is assumed that 200 MHz uninterfered bandwidth can be used for an H/2 system in both Europe and USA. Ongoing discussions may also result in H/2 being deployed in a similar frequency band in Japan. In order to support the required peak data rate of 25 Mb/s, a channel spacing/bandwidth of 20 MHz has been adopted in ETSI BRAN. With 200 MHz bandwidth, typically nine frequency carriers are available if a guard band of one channel is applied. Since H/2 will be used in an unlicensed band, it may occur that an operator can not utilize the entire frequency band due to interference from other operators in the close vicinity. Furthermore, a high radio quality is required to fulfil the peak data rate requirement of 25 Mb/s. The H/2 system is likely to be deployed in a wide range of environments, such as office buildings, exhibition halls, airports, industrial buildings and outdoor deployment. Altogether, this implies that deploying a full coverage, multicell system is challenging. It is clear that the system must be able to adapt to different propagation and interference environments [2].

### 2.1.1 HIPERLAN/2 System Description

A typical H/2 system consists of a number of access points (APs) connected to a backbone network, e.g. an Ethernet LAN. An AP can use an omni antenna, a multi beam antenna, or a number of distributed antenna elements. The system supports mobility between access points on the same backbone network, i.e. handover is made between APs [2].

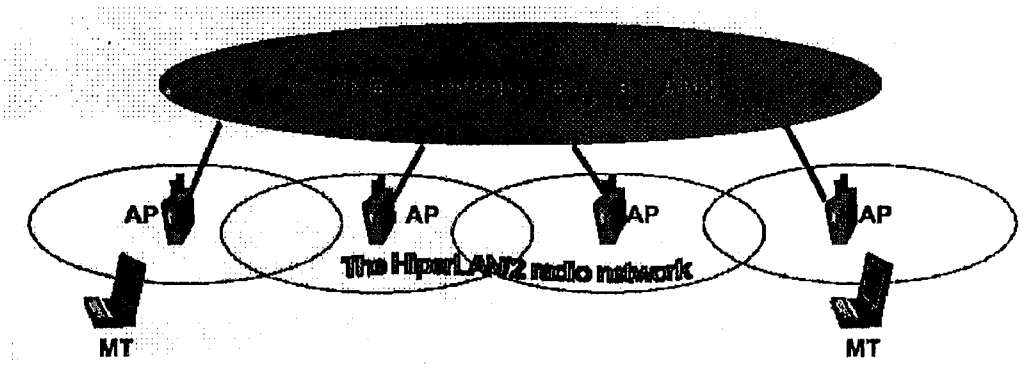


Figure 2.1 System Overview HIPERLAN type 2 (H/2)

## 2.2 Features of HIPERLAN/2

The general features of the HiperLAN/2 technology can be summarized in the following list.

- High-speed transmission
- Connection-oriented
- Quality-of-Service (QoS) support
- Automatic frequency allocation
- Security support
- Mobility support
- Network & application independent
- Power save

A short description of each of these features are given below.

### 2.2.1 High-Speed Transmission

HiperLAN/2 has a very high transmission rate, which at the physical layer extends up to 54 Mbit/s and on layer 3 up to 25 Mbit/s. To achieve this, HiperLAN/2 makes use of a modularization method called Orthogonal Frequency Digital Multiplexing (OFDM) to transmit the analogue signals. OFDM is very efficient in time-dispersive environments, e.g within offices, where the transmitted radio signals are reflected from many points, leading to different propagation times before they eventually

reach the receiver. Above the physical layer, the Medium Access Control (MAC) protocol is all new which implements a form of dynamic time-division duplex to allow for most efficient utilization of radio resources.

### 2.2.2 Connection-Oriented

In a HiperLAN/2 network, data is transmitted on connections between the MT and the AP that have been established prior to the transmission using signaling functions of the HiperLAN/2 control plane.

Connections are time-division-multiplexed over the air interface. There are two types of connections, point-to-point and point-to-multipoint. Point-to-point connections are bidirectional whereas point-to-multipoint are unidirectional in the direction towards the Mobile Terminal. In addition, there is also a dedicated broadcast channel through which traffic reaches all terminals transmitted from one AP.

### 2.2.3 QoS Support

The connection-oriented nature of HiperLAN/2 makes it straightforward to implement support for QoS. Each connection can be assigned a specific QoS, for instance in terms of bandwidth, delay, jitter, bit error rate, etc. It is also possible to use a more simplistic approach, where each connection can be assigned a priority level relative to other connections. This QoS support in combination with the high transmission rate facilitates the simultaneous transmission of many different types of data streams, e.g. video, voice, and data.

### 2.2.4 Automatic Frequency Allocation

In a HiperLAN/2 network, there is no need for manual frequency planning as in cellular networks like GSM. The radio base stations, which are called Access Points in HiperLAN/2, have a built-in support for automatically selecting an appropriate radio channel for transmission within each AP's coverage area. An AP listens to neighboring APs as well as to other radio sources in the environment, and selects an appropriate radio channel based on both what radio channels are already in use by those other APs and to minimize interference with the environment.

### 2.2.5 Security Support

The HiperLAN/2 network has support for both authentication and encryption. With authentication both the AP and the MT can authenticate each other to ensure authorized access to the network (from the AP's point of view) or to ensure access to a valid network operator (from the MT's point of view). Authentication relies on the existence of a supporting function, such as a directory service, but which is outside the scope of HiperLAN/2. The user traffic on established connections can be encrypted to protect against for instance eaves-dropping and man-in-middle attacks.

### 2.2.6 Mobility Support

The MT will see to that it transmits and receives data to/from the "nearest" AP, or more correctly speaking the MT uses the AP with the best radio signal as measured by the signal to noise ratio. Thus, as the user and the MT move around, the MT may detect that there is an alternative AP with better radio transmission performance than the AP which the MT is currently associated to. The MT will then order a hand over to this AP. All established connections will be moved to this new AP resulting in that the MT stays associated to the HiperLAN/2 network and can continue its communication. During handover, some packet loss may occur. If an MT moves out of radio coverage for a certain time, the MT may loose its association to the HiperLAN/2 network resulting in the release of all connections.

### 2.2.7 Network and Application Independent

The HiperLAN/2 protocol stack has a flexible architecture for easy adaptation and integration with a variety of fixed networks. A HiperLAN/2 network can for instance be used as the "last hop" wireless segment of a switched Ethernet, but it may also be used in other configurations, e.g. as an access betwork to 3 rd generation cellular networks. All applications which today run over a fixed infrastructure can also run over a HiperLAN/2 network.

### 2.2.8 Power Save

In HiperLAN/2, the mechanism to allow for an MT to save power is based on MT-initiated egotiation of sleep periods. The MT may at any time request the AP to enter a low power state (specific per MT), and requests for a specific sleep period. At the expiration of the negotiated sleep period, the MT searches for the presence of any wake up indication from the AP. In the absence of the wake up indication the MT reverts back to its low power state for the next sleep period, and so forth. An AP will defer any pending data to an MT until the corresponding sleep period expires. Different sleep periods are supported to allow for either short latency requirement or low power requirement [3].

# 3 MODIFIED RING HYBRID

## 3.1 Microstrip Line

It is a common practice to use planar printed circuit boards (PCBs) as the basic medium to implement most electronic systems. When dealing with actual RF circuits, it is necessary to consider the high frequency behavior of the conducting strips etched on the PCBs, as shown in Figure 3.1.

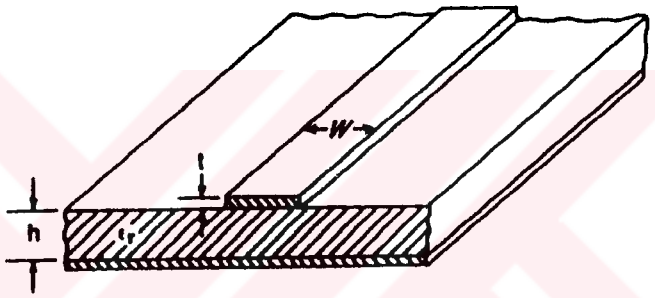


Figure 3.1 Microstrip transmission line representation

The ground plane below the current carrying conductor traces helps prevent excessive field leakage and thus reduces radiation loss

One of the disadvantages of single layered PCBs is that they have rather high radiation loss and are prone to "crosstalk" between neighboring conductor traces. The severity of field leakage depends on the relative dielectric constants is shown in Figure 3.2.

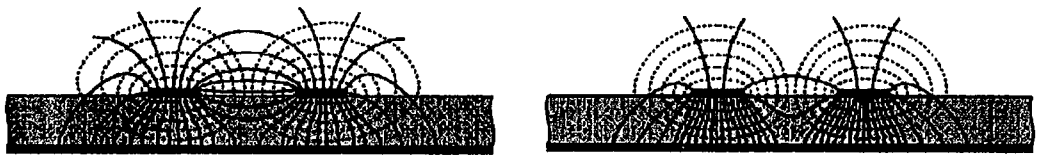


Figure 3.2 Electric field leakage as a function of dielectric constants

Direct comparison of the field lines in Figure 3.2 suggests that to achieve high board density of the component layout, substrates with high dielectric constants must be used, since they minimize field leakage and cross coupling [4].

### 3.1.1 Microstrip Transmission Line

If the substrate thickness $h$ increases or if the conductor width $w$ decreases, fringing fields become more prominent and cannot be ignored in the mathematical model. Over the years a number of researchers have developed approximate expressions for the calculation of the characteristic line impedance, taking into account conductor width and thickness. The most precise expressions describing microstrip lines are derived by using conformal mapping, but these expressions are also the most complex, requiring substantial computational efforts.

As a first approximation, it is assumed that the thickness $t$ of conductor forming the line negligible compared to the substrate height (t/h<0.005). In this case, emprical formulas that depend only on the line dimensions ($w$ and $h$) and the dielectric constant $\varepsilon_r$ can be used. They require two separate regions of applicability depending on whether the ratio $w/h$ is larger or less than unity. For narrow strip lines, $w/h<1$, the line impedance can be obtained as;

$$Z_O = \frac{Z_f}{2\pi\sqrt{\varepsilon_{eff}}} \ln(8\frac{h}{w} + \frac{w}{4h}) \tag{3.1}$$

where $Z_f = \sqrt{\mu_0 / \varepsilon_0} = 376.8\,\Omega$ is the wave impedance in free space, and $\varepsilon_{eff}$ is the effective dielectric constant given by;

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[(1 + 12\frac{h}{w})^{-1/2} + 0.04(1 - \frac{w}{h})^2\right] \tag{3.2}$$

For a wide line, $w/h>1$, it is necessary to resort to a different characteristic line impedance expression:

$$Z_0 = \frac{Z_f}{\sqrt{\varepsilon_{eff}}\,(1.393 + \frac{w}{h} + \frac{2}{3}\ln(\frac{w}{h} + 1.444))} \tag{3.3}$$

with

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}(1 + 12\frac{h}{w})^{-1/2} \tag{3.4}$$

According to the expressions above, characteristic line impedance and effective dielectric constant can be plotted as shown in Figure 3.1 and Figure 3.2.

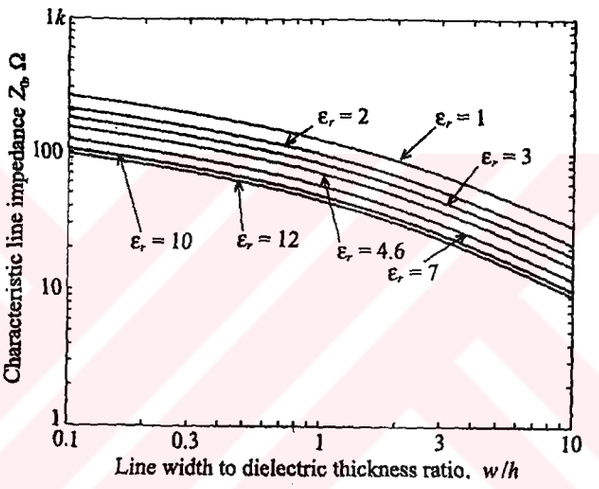


Figure 3.3 Characteristic line impedance as a function of w/h

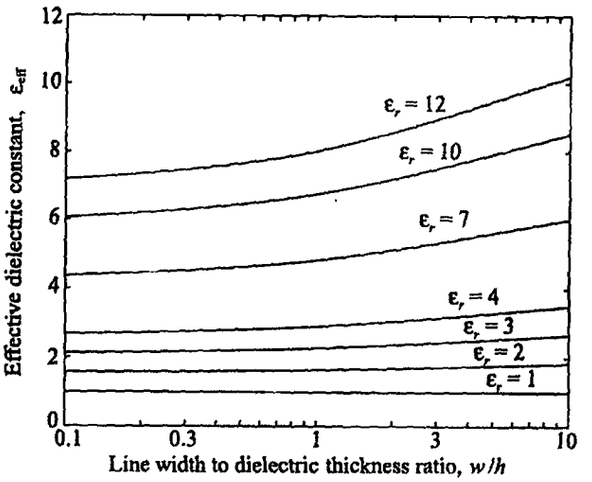


Figure 3.4 Effective dielectric constant vs. w/h for different dielectric constants

With the knowledge of the effective dielectric constant the phase velocity of the strip line can be computed as $v_p = c/\sqrt{\varepsilon_{eff}}$. This leads to an expression for the wavelength of

$$\lambda = \frac{v_p}{f} = \frac{c}{f\sqrt{\varepsilon_{eff}}} = \frac{\lambda_0}{\sqrt{\varepsilon_{eff}}} \tag{3.5}$$

where, $c$ is the speed of light and $f$ is the operating frequency [4].

## 3.2 Special Termination Conditions

### 3.2.1 Input Impedance of Terminated Lossless Line

At a distance $d$ away from the load the input impedance is given by the expression

$$Z_{in}(d) = \frac{V(d)}{I(d)} = Z_0 \frac{V^+ e^{j\beta d}(1+\Gamma_0 e^{-2j\beta d})}{V^+ e^{j\beta d}(1-\Gamma_0 e^{-2j\beta d})} \tag{3.6}$$

The reflection coefficient $\Gamma_0$ can be expressed as;

$$\Gamma_0 = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{3.7}$$

By replacing (3.7) in (3.6), the following expression can be obtained;

$$Z_{in}(d) = \frac{e^{j\beta d} + (\frac{Z_L - Z_0}{Z_L + Z_0})e^{-j\beta d}}{e^{j\beta d} - (\frac{Z_L - Z_0}{Z_L + Z_0})e^{-j\beta d}} Z_0$$

$$= \frac{Z_L \cos(\beta d) + jZ_0 \sin\beta d)}{Z_0 \cos(\beta d) + jZ_L \sin(\beta d)} Z_0 \tag{3.8}$$

By dividing nominator and denominator by cosine term,

$$Z_{in}(d) = Z_0 \frac{Z_L + jZ_0 \tan(\beta d)}{Z_0 + jZ_L \tan(\beta d)} \tag{3.9}$$

This expression shows how the load impedance $Z_L$ is transformed along a line of characteristic impedance $Z_0$ and length $d$. Depending on the application β can be expressed in terms of wave length as $\beta = 2\pi/\lambda$.

### 3.2.2 Short-Circuit Transmission Line

If $Z_L$=0 ( the load is represented by a short-circuit) expression (3.9) simplifies to;

$$Z_{in}(d) = jZ_0 \tan(\beta d) \tag{3.10}$$

According to equation (3.10); if $d=0$, the impedance is equal to the load impedance, which is zero. For increasing d the impedance of the line is purely imaginary and increases in magnitude. The positive sign of the impedance at this location shows that the line exhibits inductive behavior. When d reaches quarter wave length, the impedance is equal to infinity, which represents an open-circuit condition. Further increase in distance leads to negative imaginary impedance, which is equivalent to a capacitive behavior. At distance $d = \lambda/2$ the impedance becomes zero and entire periodic process is repeated for $d > \lambda/2$.

### 3.2.3 Open-Circuit Transmission Line

If $Z_L \rightarrow \infty$ the input impedance (3.9) simplifies to the expression

$$Z_{in}(d) = -jZ_0 \frac{1}{\tan(\beta d)} \tag{3.11}$$

According to equation (3.11); if $d=0$, the impedance is equal to the load impedance, which is ∞. For increasing d the impedance of the line is purely imaginary and increases in magnitude. The negative sign of the impedance at this location shows that the line exhibits capacitive behavior. When d reaches quarter wave length, the impedance is equal to zero, which represents an short-circuit condition. Further increase in distance leads to positive imaginary impedance, which is equivalent to a inductive behavior. At distance $d = \lambda/2$ the impedance becomes ∞ and entire

periodic process is repeated for $d > \lambda/2$.

### 3.2.4 Quarter-Wave Transmission Line

As evident from equation (3.8), it is possible to make the input impedance of the line equal to the load impedance by setting $d = \lambda/2$.

$$Z_{in}(d = \lambda/2) = Z_0 \frac{Z_L + jZ_0 \tan(\frac{2\pi}{\lambda} \cdot \frac{\lambda}{2})}{Z_0 + jZ_L \tan(\frac{2\pi}{\lambda} \cdot \frac{\lambda}{2})} = Z_L \tag{3.12}$$

in other words, if the line is exactly a half wavelength long, the input impedance is equal to the load impedance, independent of the characteristic line impedance $Z_0$.

When $d = \lambda/4$ ,the equation (3.8) becomes;

$$Z_{in}(d = \lambda/4) = Z_0 \frac{Z_L + jZ_0 \tan(\frac{2\pi}{\lambda} \cdot \frac{\lambda}{4})}{Z_0 + jZ_L \tan(\frac{2\pi}{\lambda} \cdot \frac{\lambda}{4})} = \frac{Z_0^2}{Z_L} \tag{3.13}$$

The implication of (3.13) leads to the **lambda-quarter transformer,** which allows the matching of a real load impedance to a desired real input impedance by choosing a transmission line segment whose characteristic impedance can be computed as the geometric mean of load and input impedance:

$$Z_0 = \sqrt{Z_L Z_{in}} \tag{3.14}$$

This is shown in Figure 3.5, where $Z_{in}$ and $Z_L$ are known impedances and $Z_0$ is determined based on (3.14) [4].

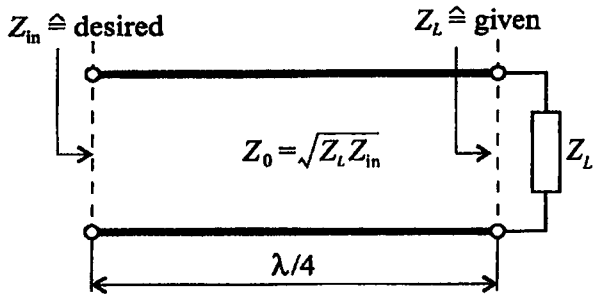


Figure 3.5 Input impedance matched to load impedance through a $\lambda/4$ line

### 3.3 Ring Hybrid

Figure 3.6 shows the ring, or rat-race, hybrid. Unlike the transformer hybrid, the ring hybrid requires frequency-sensitive elements, namely transmission lines of a precise length, that make it a narrow-band component. Figure 3.6 shows a ring hybrid in a form that can be realized in microstrip or stripline.

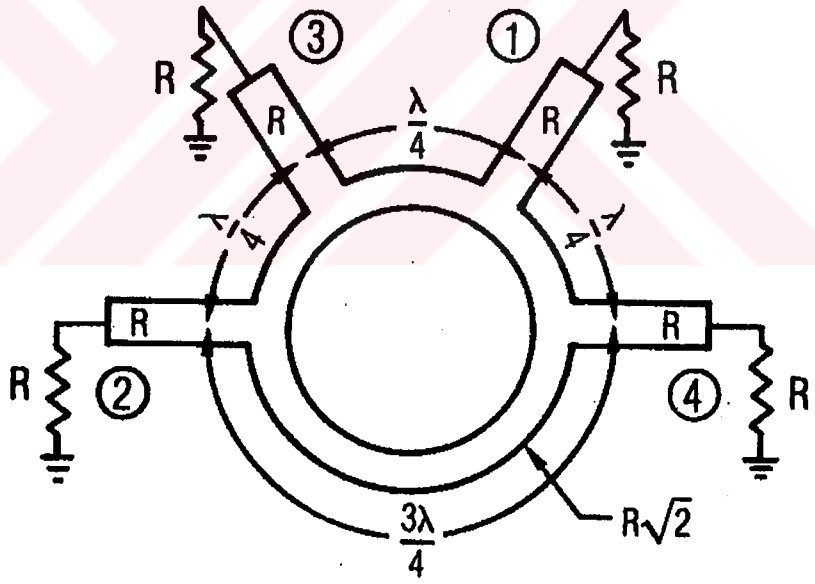


Figure 3.6 The ring hybrid in microstrip or stripline form.

Power applied to any port of the ring hybrid is divided equally between the two adjacent ports. The remaining port is isolated because there are always two paths between the input port and the isolated port: Going around the ring in one direction leads from the input to the isolated port over a 0.5-wavelength path; in other direction, the path is 1.0 wavelength, or 0.5-wavelength longer. The longer path introduces a phase reversal that cancels the voltage at the isolated port and creates a

virtual ground at its point of connection to the ring. Because of the extra half wavelength of transmission line, the path from Port 4 to Port 2 has the 180-degree phase shift.

Because of its relatively low loss and the simplicity of its design and fabrication, the ring hybrid is a very popular design. All the ports have the same impedance, and the ring's characteristic impedance is $\sqrt{2}$ times the port impedance. If transmission line dispersion and junction effects are negligible, the VSWR of each port is less than 2.0 over nearly 100 percent bandwidth; however, the transmission bandwidth is much narrower than the VSWR bandwidth, 10-20 percent at most, depending upon the critically of the application [5].

### 3.3.1 Schematic and Simulation Results for Ring Hybrid

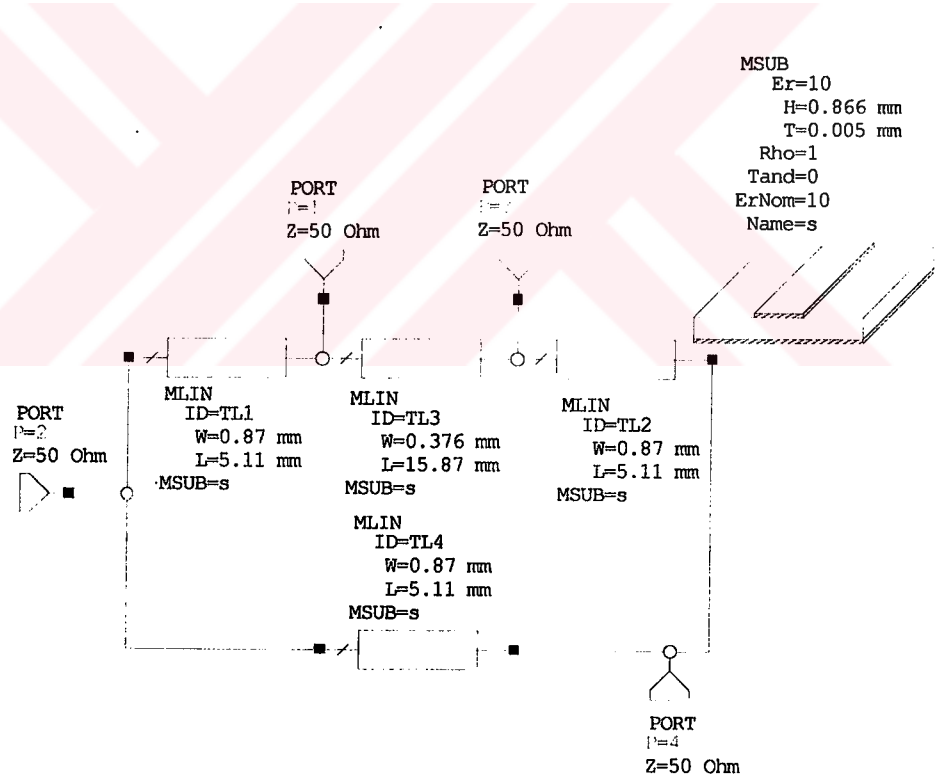


Figure 3.7 Schematic for Ring Hybrid

If power is fed from port 1, s parameters and phase relations will be as follows;

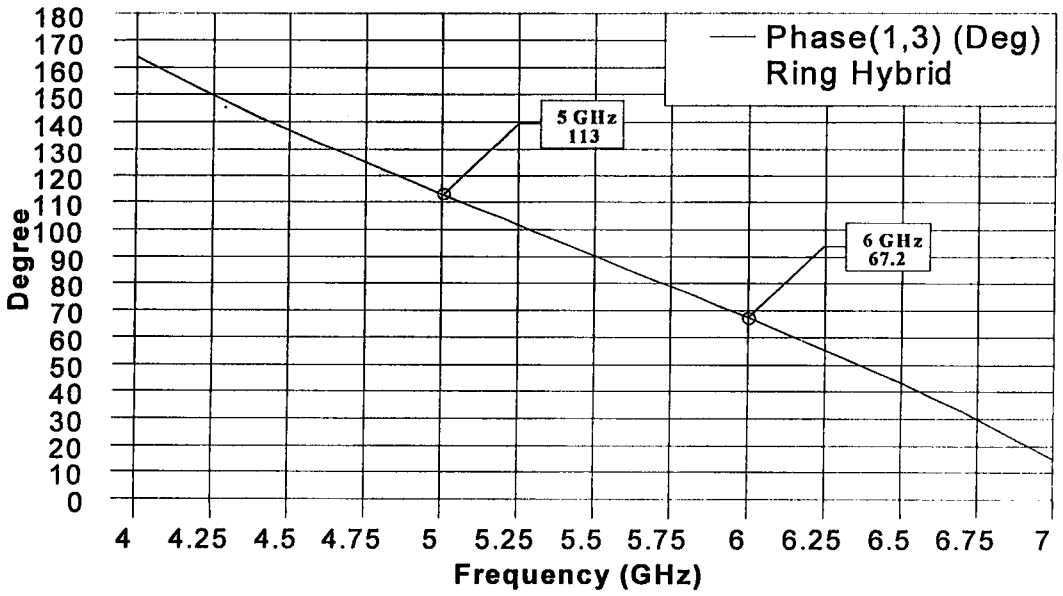


Figure 3.8 Phase difference between Port 1 and Port 3

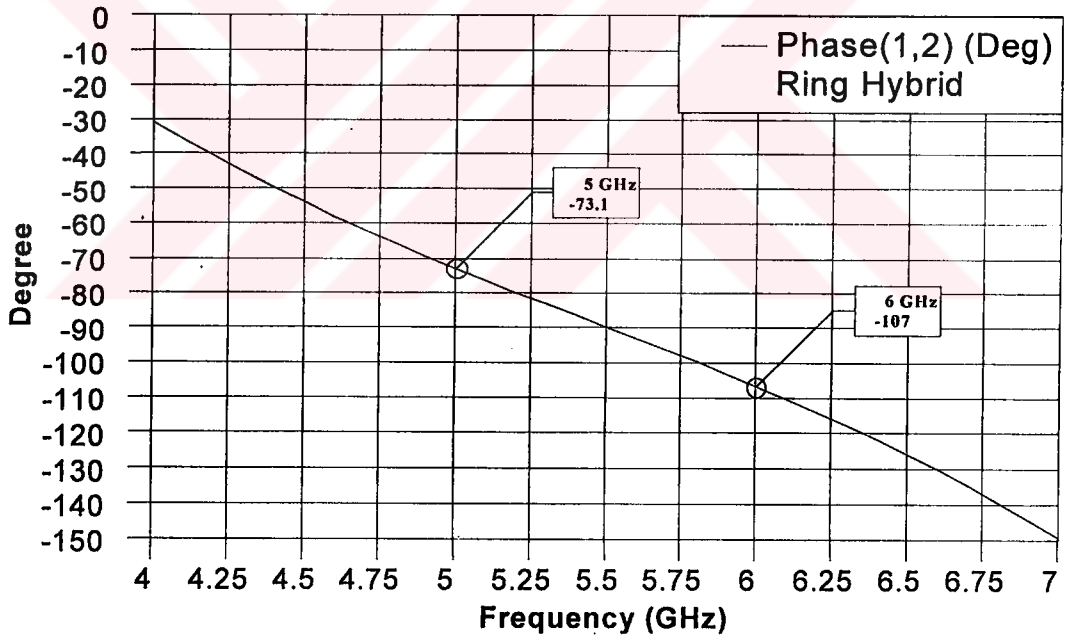


Figure 3.9 Phase difference between Port 1 and Port 2

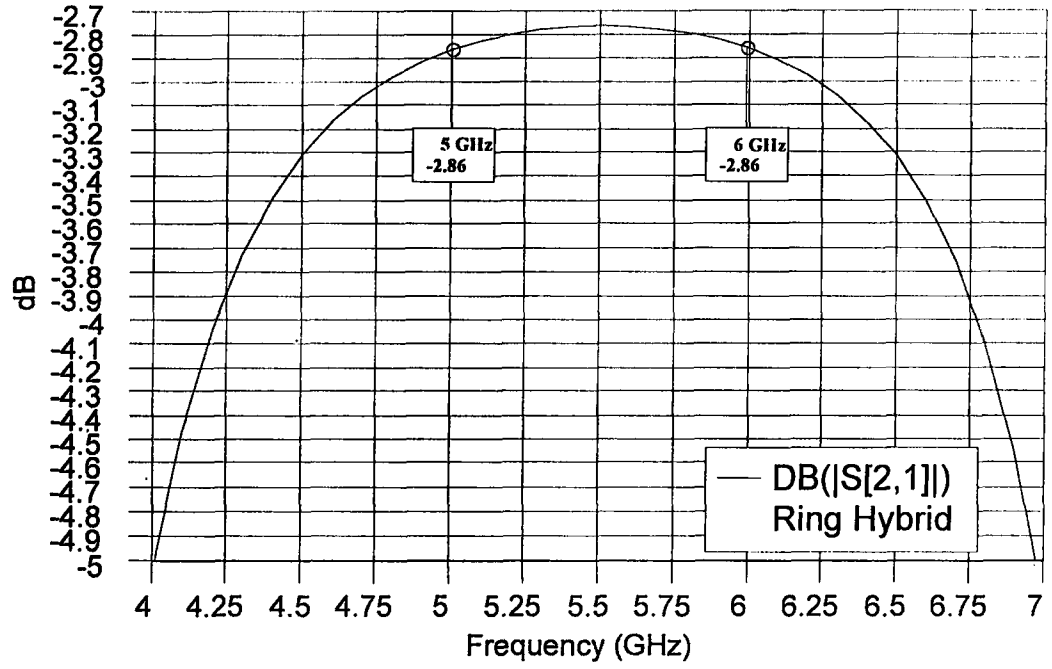


Figure 3.10 S-Parameter from port 1 to Port 2

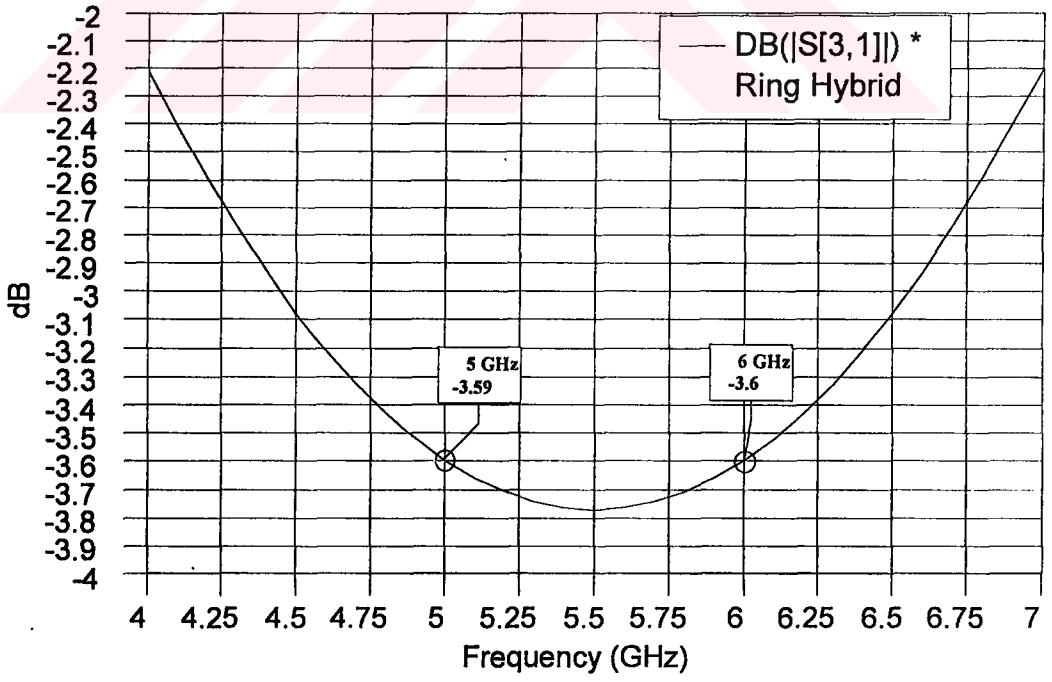


Figure 3.11 S-Parameter from port 1 to Port 3

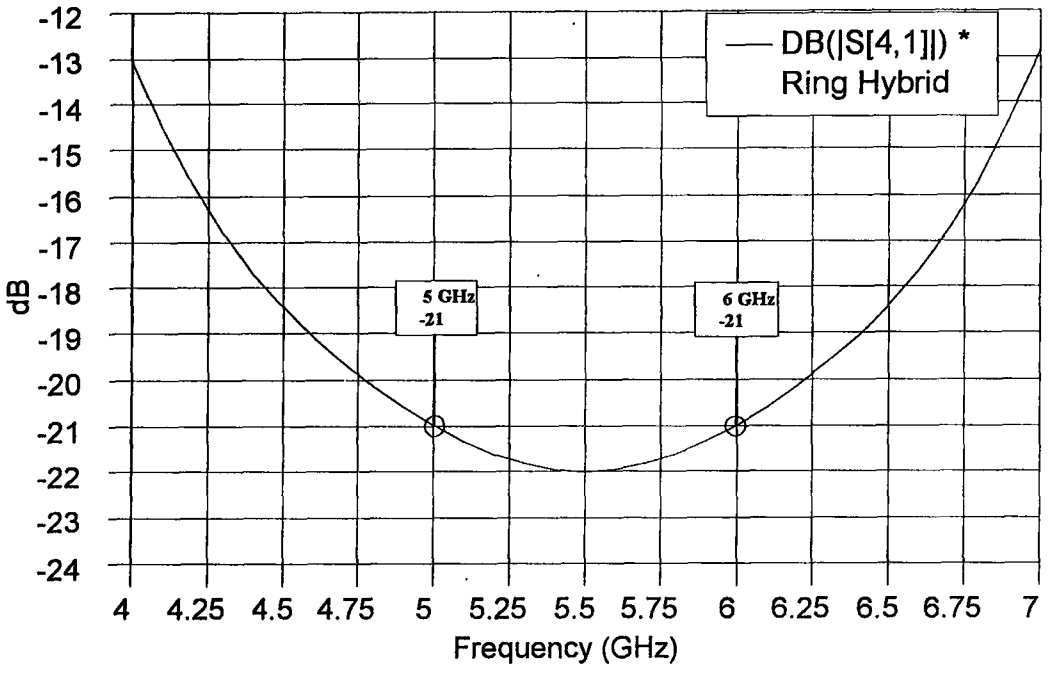


Figure 3.12 S-Parameter from Port 1 to Port 4

### 3.4 Modified Ring Hybrid

Ring Hybrid can be accepted as a narrow band device, but by making several design changes ring hybrid can be broad-banded for good performance over an octave. The limiting factor in the ring hybrid is the three-quarter wavelength section, which restricts the useful frequency range for the 180° hybrid to $f_0 \pm 0.23 f_0$ where $f_0$ is the center frequency in the band of interest. The ring hybrid configuration exhibits -3.0 dB of coupling when the impedance of each the ring segments, $Z_r$, is $\sqrt{2}Z_0$, where $Z_0$ is the characteristic impedance of both the input and output lines.

However, to realize $-3.0 \pm 0.3 dB$ of coupling over an octave while maintaining a low VSWR and a minimum of 20dB of isolation to the fourth port, the characteristic impedance of the arcs should be derived for –3.3dB of coupling, instead of the usual –3.0dB, at midband. Hence, for any desired values of coupling, $Z_r$ can be calculated from;

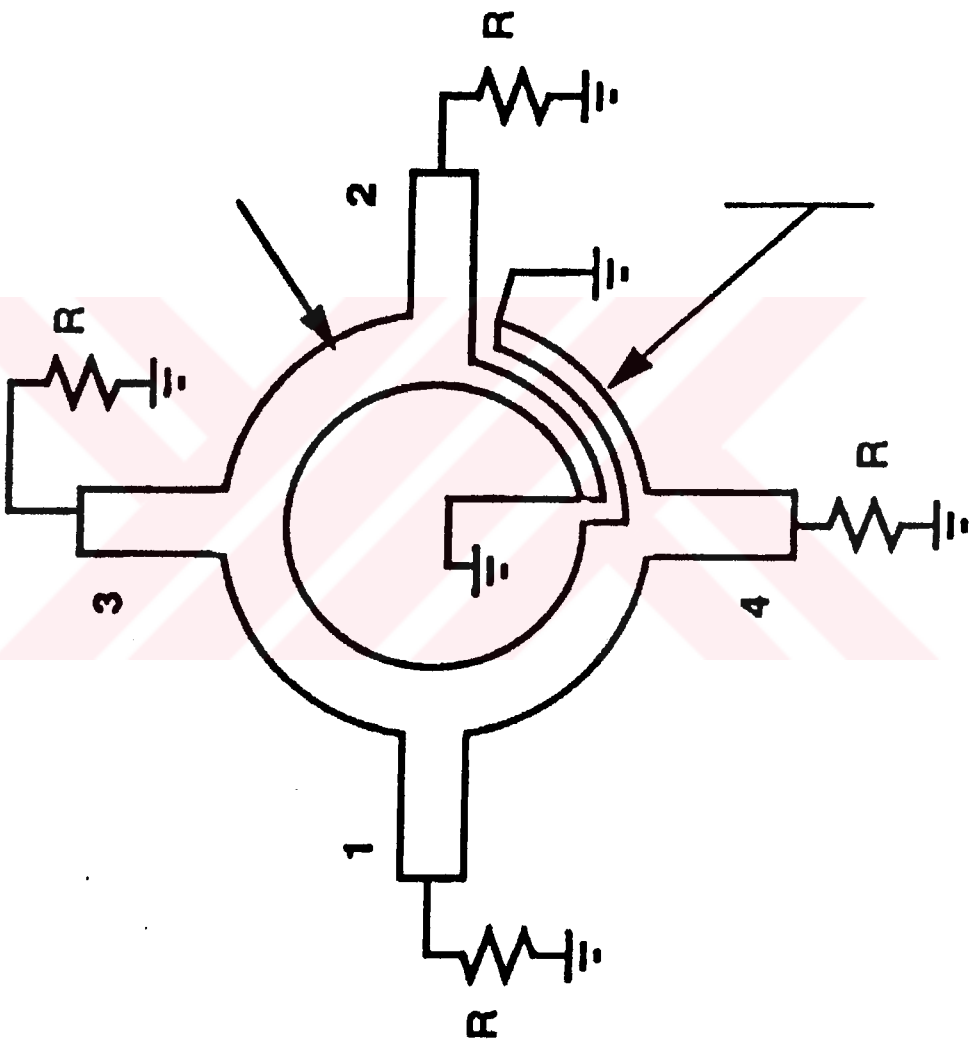


Figure 3.13 Modified Ring Hybrid

$$Z_r = Z_0[\log^{-1}(-1.1C/20)] \tag{3.15}$$

where C is the mean value of coupling in decibels. For the usual-3.0dB coupling, the ring impedance should be $1.46Z_0$.

Decreased frequency sensitivity can be achieved by replacing the three-quarter wavelength section by one having the same mid-band impedance, but whose electrical length is realized by a quarter wavelength of line exhibiting the characteristics of an ideal phases reversing network. A pair of equilateral broadside-coupled segments of strip transmission line having diametrically opposing ends short-circuited approximates a phase-reversing network over a wide frequency range.

The characteristic impedance of the coupled section $Z_c$ is given by;

$$Z_c = \frac{2Z_{0e}Z_{0o}\sin\theta}{[(Z_{0e}-Z_{0o})^2-(Z_{0e}+Z_{0o})^2\cos^2\theta]^{1/2}} \tag{3.16}$$

where $Z_{0e}$ and $Z_{0o}$ are the even and odd mode impedances, respectively, and $\theta$ is the physical length of the coupled region in degrees. Since $180^\circ+\theta$ is the total signal path length for this arrangement, $\theta$ must be $90^\circ$ in order to realize $270^\circ$ of phase shift. Setting theta to ninety degrees, (3.16) reduces to

$$Z_c = \frac{2Z_{0e}Z_{0o}}{Z_{0e}-Z_{0o}} \tag{3.17}$$

which for proper operation should be also equal $Z_r$.

$$Z_c = \sqrt{Z_{0e}Z_{0o}} \tag{3.18}$$

By combining (3.17) and (3.18);

$$\begin{aligned} Z_{0e} &= (\sqrt{2}+1)Z_r \\ Z_{0o} &= (\sqrt{2}-1)Z_r \end{aligned} \tag{3.19}$$

for $Z_c=Z_r$. For a 50-ohm transmission system and a coupling of –3.0dB $Z_{0e}$ must be 176.2Ω and $Z_{0o}$ must be 30.2Ω [6].

### 3.4.1 Schematic and Simulation Results for Modified Ring Hybrid

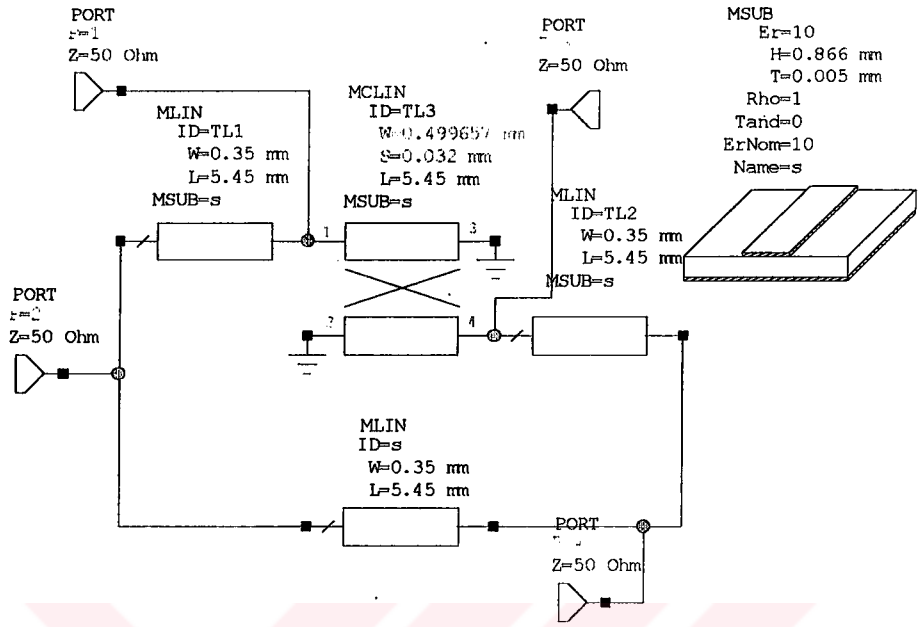


Figure 3.14 Schematic for Modified Ring Hybrid

If power is fed from port 1, s parameters and phase relations will be as follows;

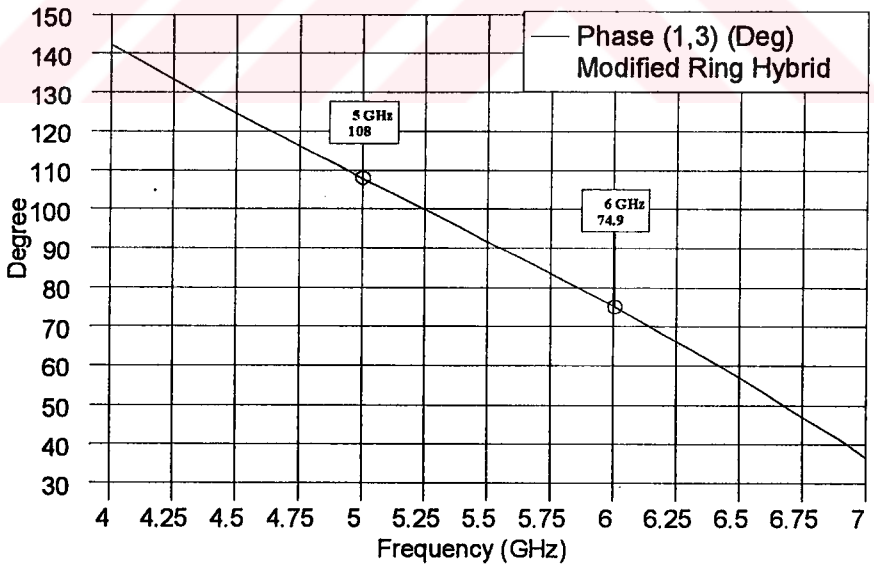


Figure 3.15 Phase difference between Port 1 and Port 3

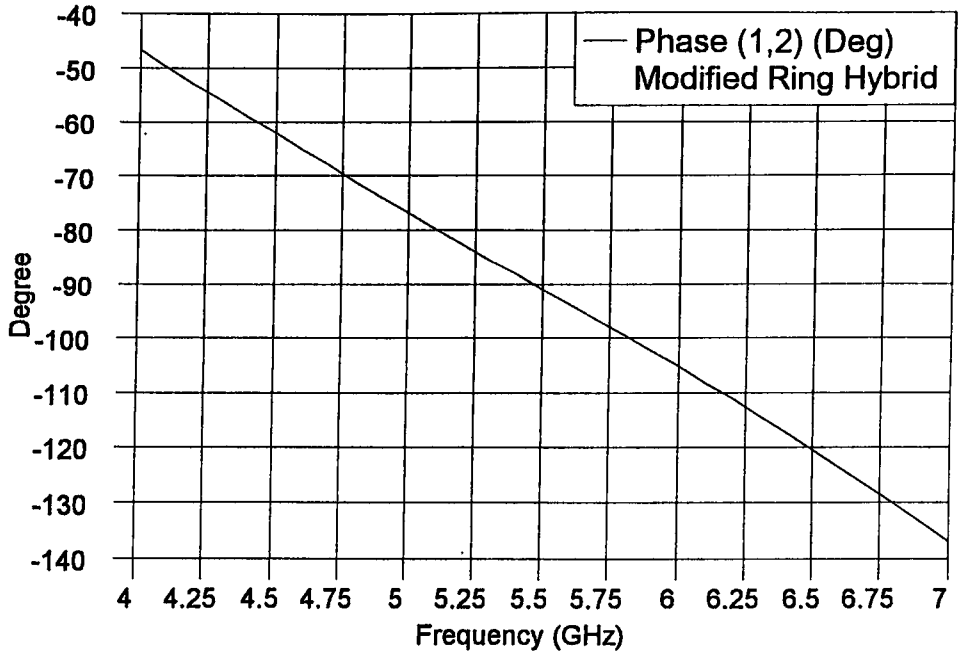


Figure 3.16 Phase difference between Port 1 to Port 2

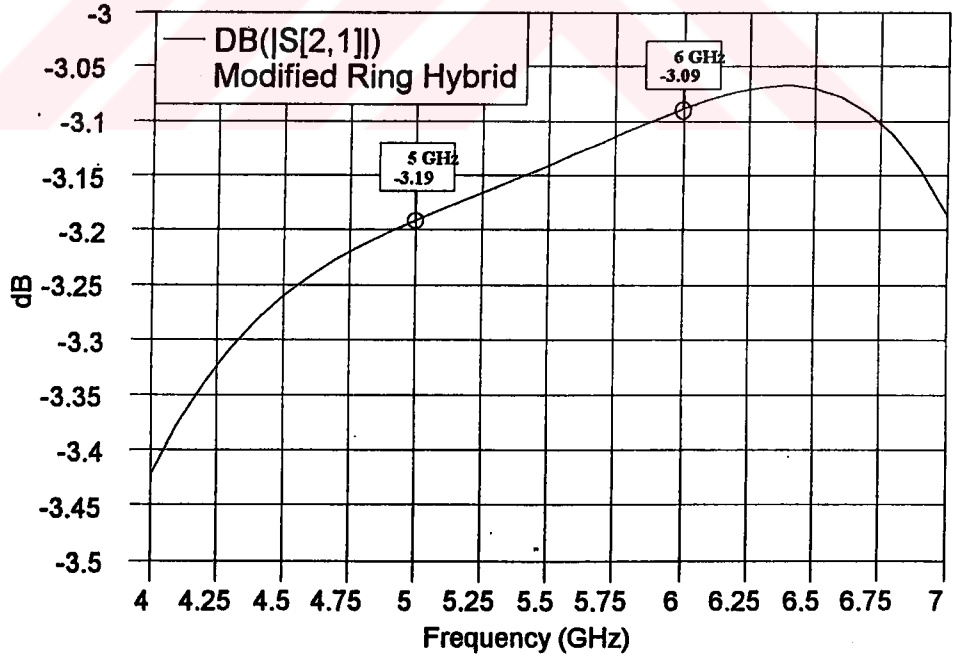


Figure 3.17 S-Parameter from port 1 to Port2

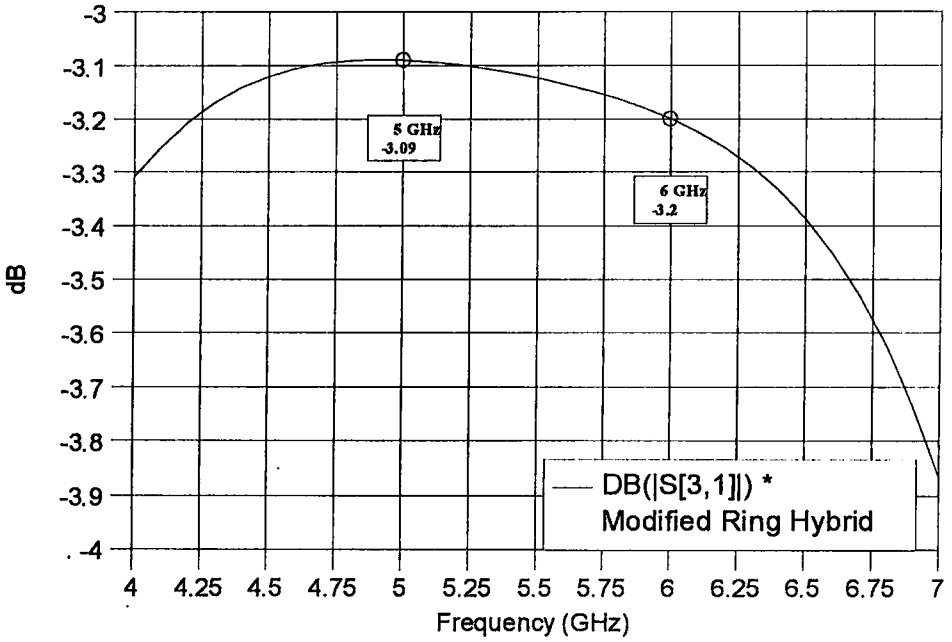


Figure 3.18 S-Parameter from port 1 to Port 3

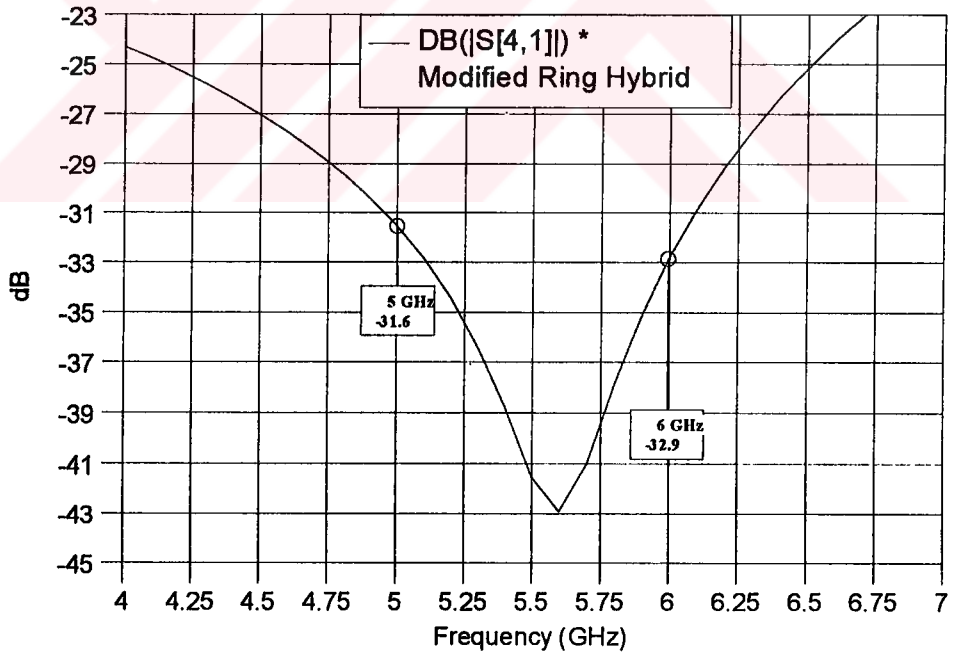


Figure 3.19 S-Parameter from Port 1 to Port 4

# 4 HIGH EFFICIENCY POWER AMPLIFIER

## 4.1 Linear and Non-Linear Circuits

Linear circuits are defined as those for which superposition principle holds. If excitations $x_1$ and $x_2$ are applied separately to a circuit having responses $y_1$ and $y_2$, the response to the excitation $ax_1 + bx_2$ *is* $ay_1 + by_2$, where a and b are arbitrary constants [5]. For perfectly linear amplifier, the output voltage is simply a constant times the input voltage as shown in equation (4.1).

$$V_{out}(t) = G \cdot V_{in}(t) \tag{4.1}$$

All signals are increased in magnitude by the same factor $G$ and there is fixed phase shift between input and output for a signal at a given frequency. An ideal amplifier has constant characteristics over a bandwidth of the input signal, that is constant gain, linear phase and constant delay. The response of the amplifier at any point in time is determined solely by the value of the input signal at that moment and not by any previous values, this means that an ideal amplifier is also memoryless [7].

In practice, all electronic circuits are nonlinear. The linear assumption in circuit theory is only an approximation. Some circuits such as small-signal amplifiers, are only very weakly nonlinear and are used in systems as if they are linear.

The nonlinearities of solid state devices are well known, but it is generally recognized that even passive components such as resistors, capacitors, and inductors are also nonlinear in the extremes of their operating ranges. When large voltages or currents are applied to the resistors, their resistance change as a result of thermal and other effects. The same is true for capacitances, even RF connectors. Thus the linear circuit concept is an idealization [5].

## 4.2 Frequency Generation in Nonlinear Circuits

### 4.2.1 One - Tone Excitation

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples of the input frequency. If $x(t) = A\cos\omega t$ is applied to a system expressed in equation (4.2);

$$y(t) \approx a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \tag{4.2}$$

then;

$$\begin{aligned} y(t) &= a_1 A\cos\omega t + a_2 A^2 \cos^2 \omega t + a_3 A^3 \cos^3 \omega t \\ &= a_1 A\cos\omega t + \frac{a_2 A^2}{2}(1+\cos 2\omega t) + \frac{a_3 A^3}{4}(3\cos\omega t + \cos 3\omega t) \\ &= \frac{a_2 A^2}{2} + (a_1 A + \frac{3a_3 A^3}{4})\cos\omega t + \frac{a_2 A^2}{2}\cos 2\omega t + \frac{a_3 A^3}{4}\cos 3\omega t \end{aligned} \tag{4.3}$$

In equation (4.3) the term with the input frequency is called the fundamental and the higher order terms the harmonics.

From the above expansion, two observations can be made, first; even order harmonics result from $a_j$ with even j and vanish if the system has odd symmetry. Second, in (4.3) the amplitude of the nth harmonic consists of a term proportional to $A^n$ and other terms proportional to higher powers of A. It can be assumed that the nth harmonic grows in proportion to $A^n$ [8].

### 4.2.2 Two Tone Excitation

When two signals with different frequencies are applied to a nonlinear system, the output in general exhibits some components that are not harmonics of the input frequencies. These components are called Intermodulation Products. To understand this concept, two tone input signal defined as $x(t) = A_1\cos\omega_1(t) + A_2\cos\omega_2 t$ is applied to the system expressed in equation (4.2). Thus;

$$y(t) = a_1(A_1\cos\omega_1 t + A_2\cos\omega_2 t) + a_2(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^2 + a(A_1\cos\omega_1 t + A_2\cos\omega_2 t)^3 \quad (4.4)$$

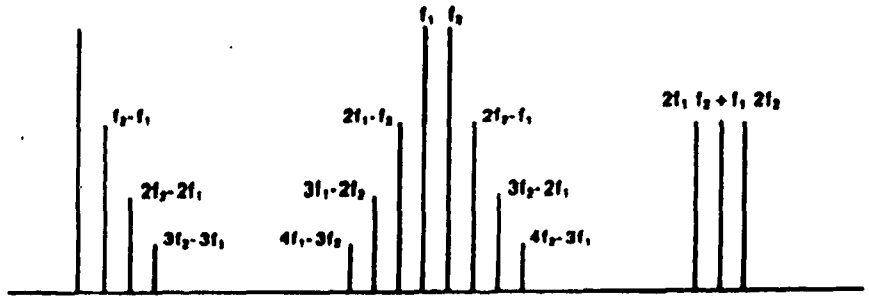


Figure 4.1 A schematic spectrum showing two signals at frequencies $f_1$ and $f_2$

Expanding the left side and discarding dc terms and harmonics, the following intermodulation products can be obtained [8];

$$\begin{aligned}\omega &= \omega_1 \pm \omega_2 : a_2A_1A_2\cos(\omega_1+\omega_2)t + a_2A_1A_2\cos(\omega_1-\omega_2)t \\ &= 2\omega_1 \pm \omega_2 : \frac{3a_3{A_1}^2A_2}{4}\cos(2\omega_1+\omega_2)t + \frac{3a_3{A_1}^2A_2}{4}\cos(2\omega_1-\omega_2)t \\ &= 2\omega_2 \pm \omega_1 : \frac{3a_3{A_1}^2A_2}{4}\cos(2\omega_2+\omega_1)t + \frac{3a_3{A_1}^2A_2}{4}\cos(2\omega_2-\omega_1)t\end{aligned} \quad (4.5)$$

and these fundamental components;

$$\begin{aligned}\omega &= \omega_1,\omega_2 : (a_1A_1 + \frac{3}{4}a_3{A_1}^3 + \frac{3}{2}a_3A_1{A_2}^2)\cos\omega_1 t \\ &\quad + (a_1A_2 + \frac{3}{4}a_3{A_2}^3 + \frac{3}{2}a_3A_2{A_1}^2)\cos\omega_2 t\end{aligned} \quad (4.6)$$

### 4.3 Power Amplifiers

All amplifiers are current-control devices. The input signal to an amplifier controls the current output of the amplifier. Amplifiers are classified as voltage and power amplifiers. A voltage amplifier is an amplifier in which the output signal voltage is larger than the input signal. A power amplifier is an amplifier in which the output signal power is greater than the input signal power. In other words, power amplifier amplifies, the power of the input signal. Most power amplifiers are used as the final

amplifier and control the output device. The output device could be a speaker, an antenna, etc. Whatever the device, the power to make it work comes from the final stage of amplification, which is a power amplifier.

### 4.3.1 Basic Definitions For PAs

#### 4.3.1.1 Amplifier Efficiency

Power conversion efficiency is a measure of how effectively an amplifier converts power drawn from the DC supply to useful (RF) power delivered to a load, that is;

$$\eta = \frac{P_{load}}{P_{DC}} \tag{4.7}$$

Another definition for the efficiency is Power Added Efficiency. That is;

$$\eta_{PAE} = \frac{P_{load} - P_{in}}{P_{DC}} \tag{4.8}$$

#### 4.3.1.2 Gain Bandwidth Product

Amplifiers are designed for operation over specific bandwidth, the transmitter band, and ideally have a gain that is constant over this bandwidth. Outside the transmitter band, the gain response tends to drop off at both low and high frequencies. At low frequencies, components such as coupling and bypass capacitors have increasing impedances; at higher frequencies, a similar effect occurs for internal device capacitances. Example of gain bandwidth product is the transition frequency $f_T$ of a transistor that is; the theoretical frequency at which the CE current gain is unity.

For a given transistor, Gain BW product is often constant. This means that they are inversely proportional. For example, if a negative feedback is applied to an amplifier, the BW increases but on the other hand gain decreases.

#### 4.3.1.3 Compression Point

As the input power increases, the amplifier transfer function becomes nonlinear, the output power is lower than the predicted by the small signal gain. This nonlinear behavior in amplifiers introduces distortion in the amplified signal. The output power

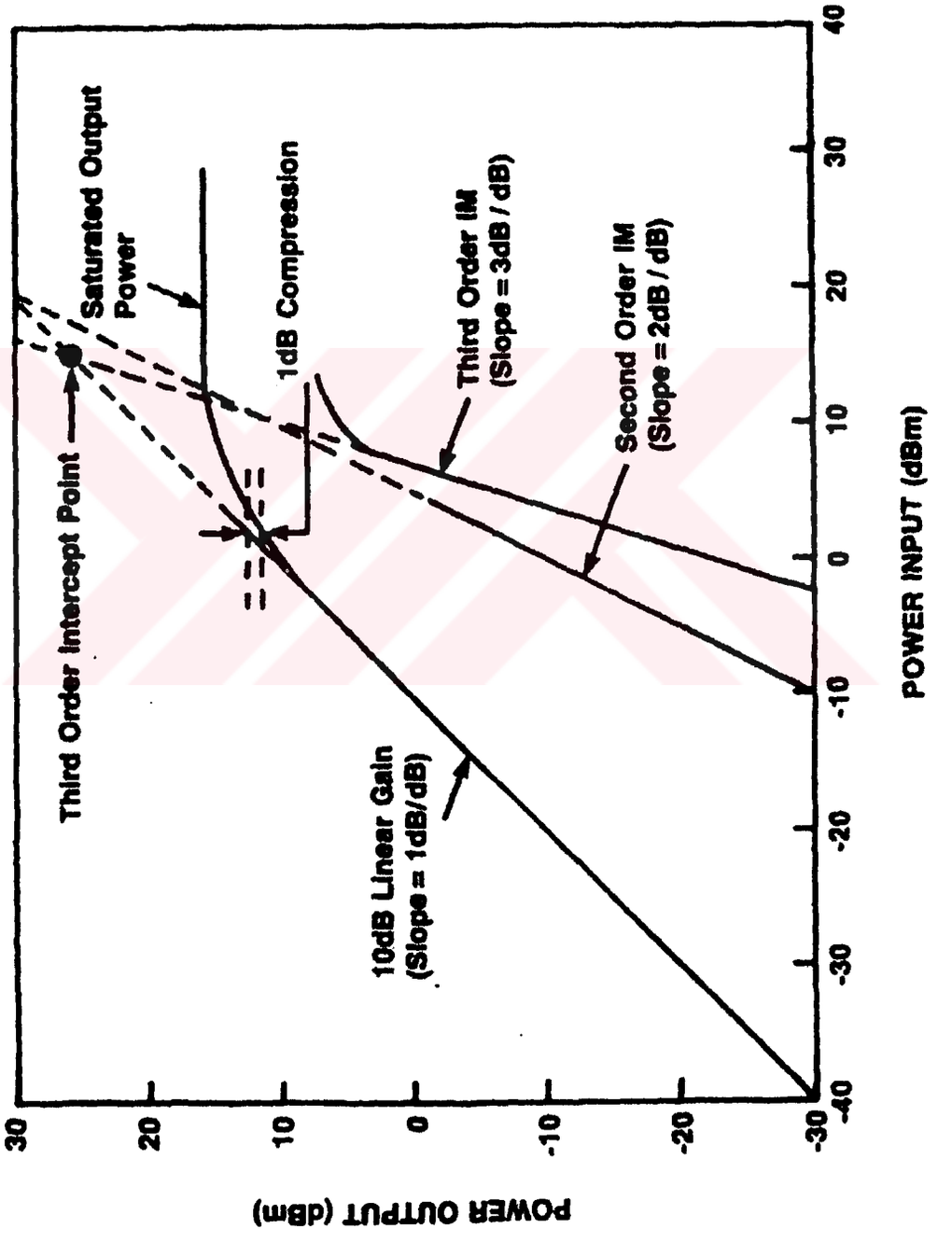


Figure 4.2 The variation of output power and intermodulation products with input power for a non-linear amplifier.

at which the gain has dropped by 1dB below the linear gain is called the 1-dB compression point, $P_{1dB}$. The gain will rapidly drop above $P_{1dB}$ reaching a maximum or a fully saturated output power within 3 or 4 dB above as shown in Figure 4.2 [9].

#### 4.3.1.4 Intercept Point

Third order intercept point is the point where the power in the third-order product and fundamental tone are equal when the amplifier is assumed to be linear as shown in Figure 4.2. $IP_{3rd}$ power is typically 10 or 12 dB above the $P_{1dB}$.

### 4.3.2 Classes of Amplifier Operation

The manner in which transistors are operated is called the class of operation and refers to the output current waveform when an input signal is applied. The class of operation has implications for power amplifiers from the linearity and efficiency point of view. The relation between efficiency and linearity is inversely proportional. This means that when the efficiency increases linearity decreases and vice versa.

There are different classes of amplifier operation. These are Class A, AB, B, C, D, E and F [7].

#### 4.3.2.1 Class A Amplifier

An ideal Class A amplifier is shown in Figure 4.3. As it is seen from the figure RF choke is used to present an infinite impedance (open circuit) to any RF signal while the series blocking capacitor is designed to be a short circuit to any RF signal. In Figure 4.4 idealized (input and output impedances are infinite) IV characteristic is shown.

For class A operation the bias point for maximum output power is $I_d = I_F/2, V_{ds} = V_s, V_{gs} = (-|V_p| + V_\phi)/2$, in which case the dc power delivered by the supply and dissipated in FET is;

$$P_{dc} = V_s I_F / 2 \tag{4.7}$$

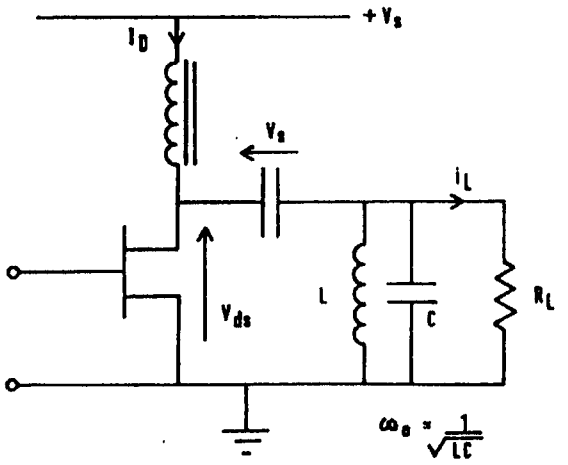


Figure 4.3 Circuit diagram of a Class A or B amplifier

It can be seen that dc power supplied is independent of the RF input and output power level, which is the major drawback of Class A amplifiers. This is because, this amount of power is consumed even with no applied signal. $I_{dss}$ is the drain current that flows when $V_{gs}$=0 V, but since the gate contact is a Schottky barrier the channel is not fully open in this condition due to internal barrier voltage $V_{\varphi}$ of the Schottky diode. The drain current can be increased by up to 20% above $I_{dss}$ by forward biasing the gate with respect to the source by about 0.5V to partially overcome the internal barrier voltage and thus increase the channel opening this enables a larger RF current swing and hence higher output power is achieved. In practical applications thermal and reliability considerations may preclude the use of $I_F/2$ as a bias point and it is better to use $I_{dss}/2$ as biasing point.

From the figures and equations above, it can be calculated that the RF power delivered to the load is given by;

$$P_{RF} = v_{ds_{peak}} \cdot i_{d_{peak}} / 2 \tag{4.8}$$

The minimum instantaneous value of $v_{ds_{peak}}$ must not fall below the knee voltage $V_K$ and the maximum instantaneous voltage must not exceed the breakdown voltage; but breakdown is normally specified in terms of the maximum drain to gate voltage $V_{dgB}$ when the gate is biased to pinch-off, that is $V_{gs} = -|V_P|$.

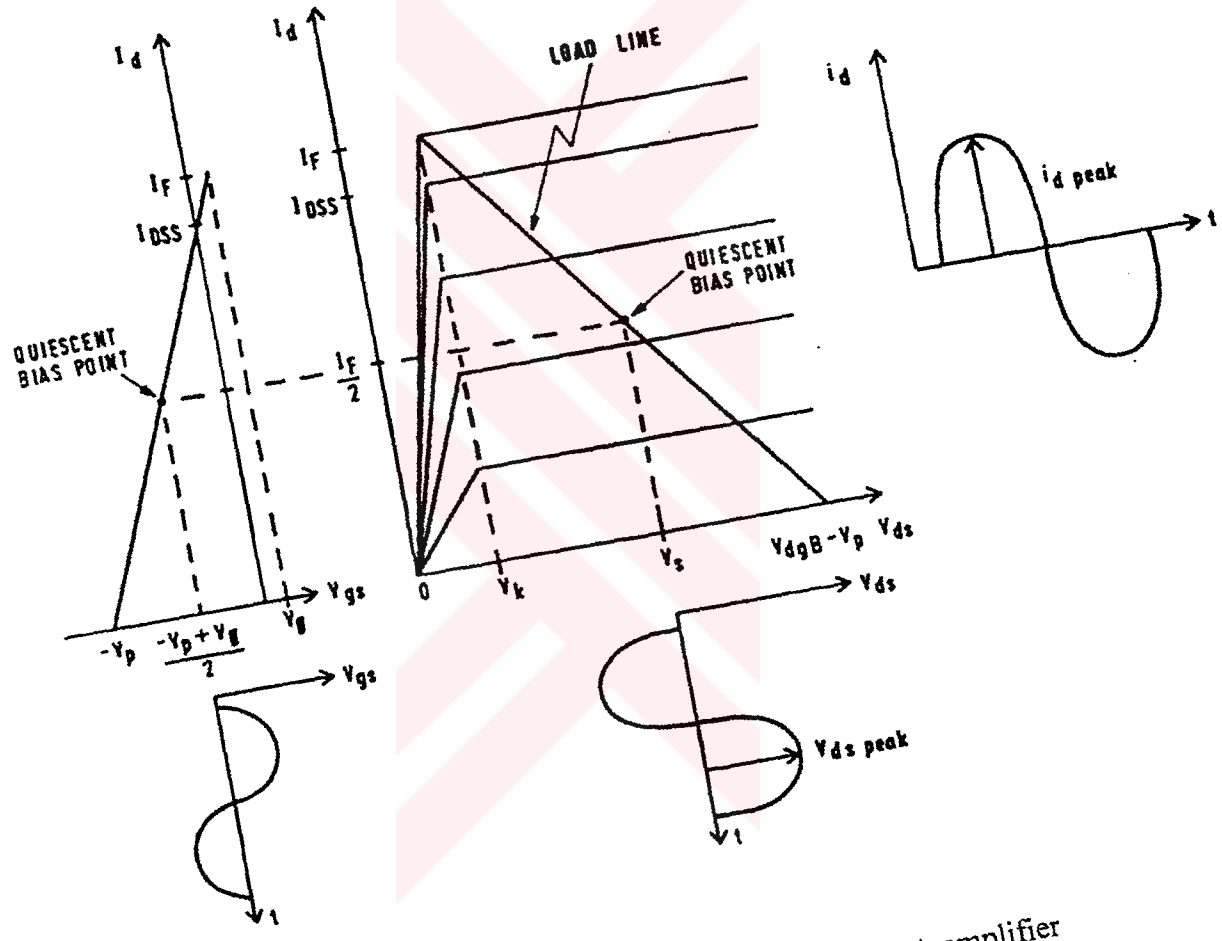


Figure 4.4 Voltage-Current waveforms for a Class A amplifier

So, the maximum drain to source voltage is $V_{dsB} - |V_P|$ and so the maximum value for $v_{ds_{peak}}$ is;

$$v_{ds_{peak}} = (V_{dgB} - |V_P| - V_K)/2 \tag{4.9}$$

So the maximum RF output power is given by;

$$P_{RF_{max}} = I_F (V_{dgB} - |V_P| - V_K)/8 \tag{4.10}$$

The equation (4.10) shows the maximum linear RF output power, and the output voltage and current are pure single-frequency sinusoids.

When the previous equations are used, power added efficiency can be calculated as;

$$\eta_{max} = (1 - 1/G)(V_{dgB} - |V_P| - V_K)/4V_S \tag{4.11}$$

From Figure 4.1 and 4.2, it can bee seen that the supply voltage $V_S$ for maximum output power is given by;

$$V_S = V_K + v_{ds_{peak}} = (V_{dgB} - |V_P| + V_K)/2 \tag{4.12}$$

If equation (4.12) is substituted in equation (4.11),

$$\eta_{max} = \frac{1}{2}(1 - \frac{1}{G})\frac{1-\alpha}{1+\alpha}; \quad \alpha = \frac{V_K}{V_{dgB} - |V_P|} \tag{4.13}$$

From equation (4.13) in the limit of infinite gain and zero knee voltage, the classical result of 50% maximum PAE is obtained for a Class A amplifier.

The most serious problem in for Class A amplifiers is for low-gain power FETs, the efficiency reduces drastically. Practical effects such as circuit losses and non-optimum load impedances will also reduce the efficiency [7].

#### 4.3.2.2 Class B Amplifier

The only difference between a Class B amplifier and the preceding Class A amplifier

is that the quiescent point is changed to $I_d = 0, \quad V_{ds} = V_S, \quad V_{gs} = -|V_P|$.

The RF drain current waveform is a half-sine wave given by;

$$i_d = \begin{cases} i_{d_{peak}} \sin \omega_0 t & 0 < \omega_0 t < \pi \\ 0 & \pi < \omega_0 t < 2\pi \end{cases} \qquad (4.14)$$

with $i_{d_{peak}} \leq I_F$. This waveform can be Fourier Analyzed into;

$$i_d = i_{d_{peak}} \left( \frac{1}{\pi} + \frac{1}{2} \sin \omega_0 t - \frac{2}{\pi} \sum_{n=2,4,\ldots}^{\infty} \frac{1}{n^2 - 1} \cos n\omega_0 t \right) \qquad (4.15)$$

that is, the current waveform contains a DC component that is a function of the RF power output, a component at $\omega_0$, and only even order harmonics. It is seen that a Class B amplifier always generates harmonics even when operated in its linear region.

Because the tuned circuit allows only the fundamental and DC components of drain voltage to exist, the ac part of $V_d(t)$, which is equal to $V_L(t)$, is a continuous sinusoid. The tuned circuit also allows only the fundamental component of $I_d(t)$ to pass through $R_L$. The power delivered to the load is ;

$$P_{dc} = V_S I_F / \pi . \qquad (4.16)$$

RF power delivered to the load is given by

$$P_{RF} = v_d i_d / 2 \qquad (4.17)$$

$v_d$ is $V_S$ and $i_d$ is $i_{dpeak}/2$. So;

$$P_{RF} = V_S I_F / 4 \qquad (4.18)$$

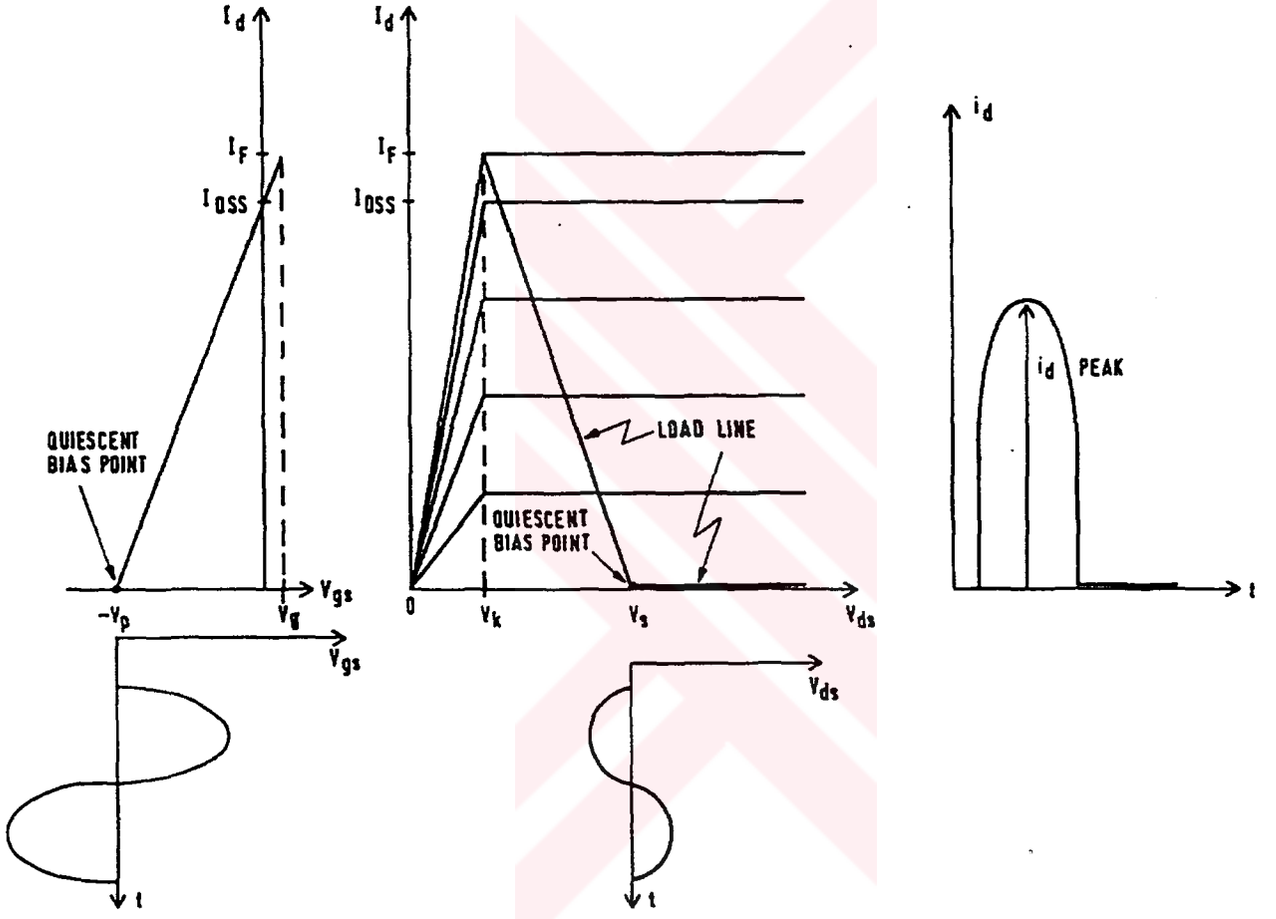


Figure 4.5 Voltage-Current waveforms for a Class B amplifier

If PAE is calculated;

$$\eta = (1-1/G)P_{RF} / P_{DC}$$

$$\eta = (1-1/G)\frac{V_S I_F / 4}{V_S I_F / \pi} \tag{4.19}$$

For infinite gain maximum PAE is 78.5% for class B amplifier.

In practice class AB bias is used with a quiescent current of about 10 to 20% of $I_{dss}$. The slight degradation in efficiency resulting from nonzero quiescent current is more than compensated for by the increased gain. An additional complication in calculating the gain reduction in Class B is caused by the fact that the gate source capacitance $C_{gs}$ decreases as $V_{gs}$ is made more negative and thus a larger fraction of the input voltage is dropped across $C_{gs}$, which reduces the amount of gain reduction.

#### 4.3.2.3 Push-Pull Amplifiers

RF Communication signals are fundamentally sinusoidal in nature, the information being carried as much slower amplitude and phase variations. In this case, it is acceptable to distort of rectify the RF carrier provided the modulation is kept intact. The audio case is quite different in that the input signal consists of a highly complex time-varying signal whose form has to be accurately preserved during the amplification process. A simple single ended class B amplifier would be unacceptable for this kind of application, because the negative excursions of the signal would be distorted. so the push pull concept is the necessity.

A push-pull amplifier is shown in Figure 4.6., together with the voltage and current waveforms at various points in the circuit.. In that figure; 0-180 degree power splitter drives two transistors in anti-phase so that only one transistor is conducting at any time. Fourier analysis of the two drain current waveforms shows that fundamental [10]

$$i_{d1} = i_{dpeak}\left(\frac{1}{\pi} + \frac{1}{2}\sin\omega_0 t - \frac{2}{\pi}\sum_{n=2,4,\ldots}^{\infty}\frac{1}{n^2-1}\cos n\omega_0 t\right)$$

$$i_{d2} = i_{dpeak}\left(\frac{1}{\pi} - \frac{1}{2}\sin\omega_0 t - \frac{2}{\pi}\sum_{n=2,4,\ldots}^{\infty}\frac{1}{n^2-1}\cos n\omega_0 t\right) \tag{4.20}$$

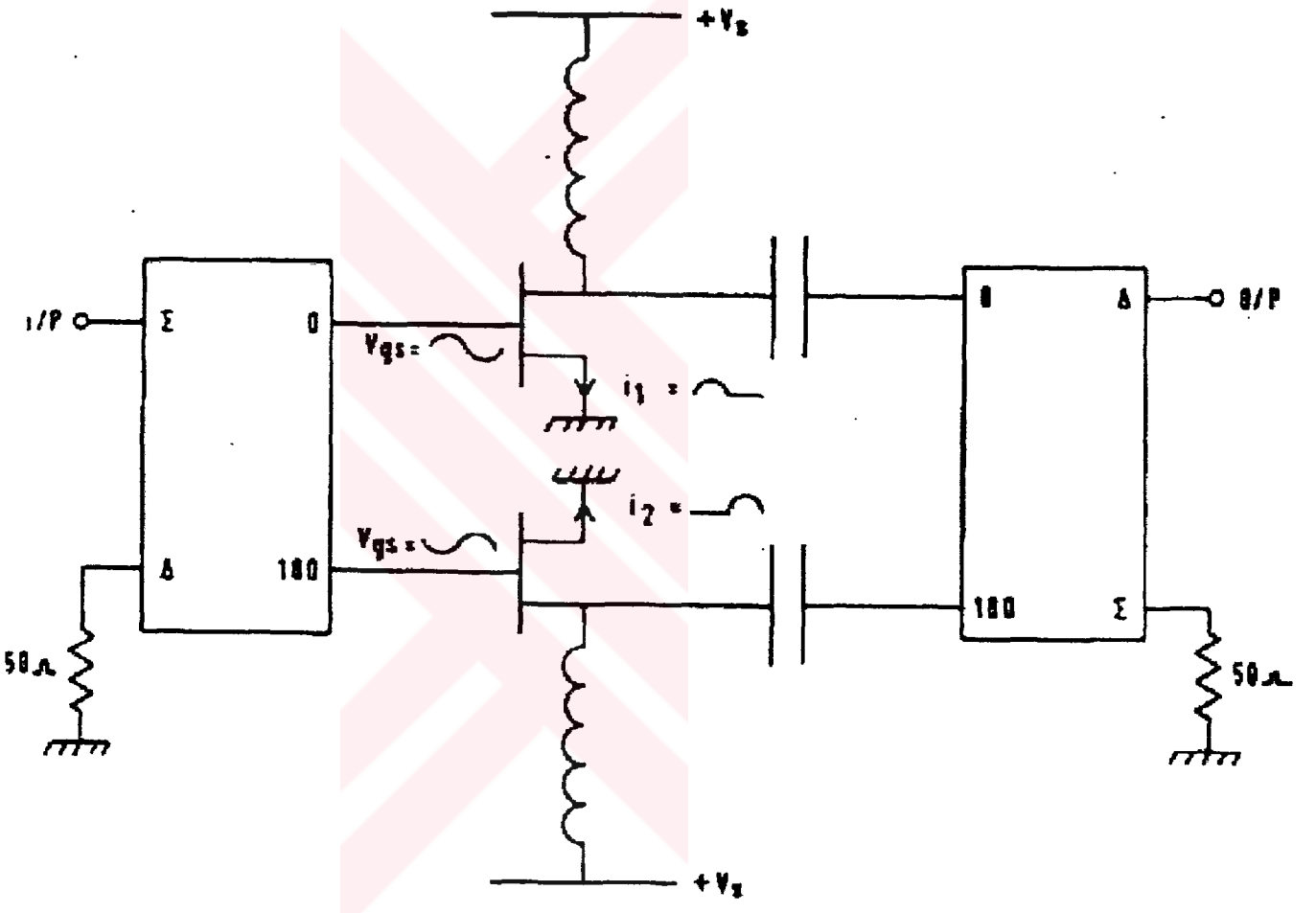


Figure 4.6 a Class B Push-Pull Amplifier with Resistive Load

components are in antiphase while the harmonics are in phase. The dc components pas through the chokes while the ac components pass through the capacitors and are combined in the output in the output 0-180 degree coupler such that fundamental components add up in phase at the Δ port and the harmonics add up in phase at the Σ port and are dissipated in the dummy load [7].

## 4.4 Power Amplifier Specifications

The maximum output power of 1W required from an amplifier chain with the maximum flat gain of 30dB at the frequency band 5.2 GHz and 5.8 GHz. The amplifier will consist with three cascaded push-pull stages. The stages will all be designed on a microstrip substrate and wide band baluns will also be part of the microstrip structure. The power supply voltage of 10V is preferable.

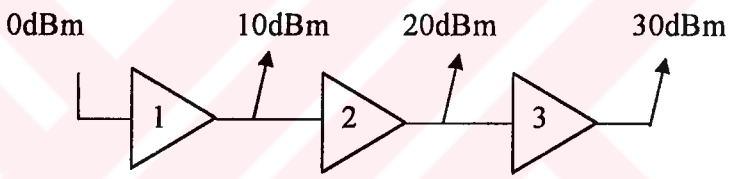


Figure 4.7 3-Stage Amplifier Chain with 1W output.

## 4.5 Power Amplifier Design Considerations

Before designing the amplifier, the class of the amplifier has to be determined. Because this amplifier will be used in Laptops, efficiency will be an important parameter. According to that reason, it is a necessity to find an efficient amplifier for this application. While finding an efficient amplifier, linearity is also an important parameter. So, if it is investigated, there can be seen that classB amplifiers have the following potential advantages compared to classA amplifiers. These are;

- Higher power added efficiency.
- Negligible power dissipation at no RF power.
- Under backoff, the efficiency of the classB amplifier does not degrade as rapidly as that of the classA amplifier [11].

The transconductance of almost all microwave power GaAs FET's is fairly constant

over most of the gate-to-source input voltage range but decreases rapidly as the channel pinches off. This degrades both the small-signal and power gain of an amplifier when attempts are made to bias it at or very near pinchoff. As a reasonable compromise between high efficiency and gain over a large dynamic range, the amplifiers can be biased to a quiescent drain current value of $I_{DQ}$=10%.$I_{DSS}$. hence they do not operate purely as Class B, but to close approximation where the conduction angle is not much larger than 180°; this is to be distinguished from general ClassAB operation, defined as having a conduction angle anywhere between 180° and 360°. At zero RF drive, $P_{DC}$ and $P_{DISS}$ are not zero, which would correspond to true class B, but they are a small fraction of the values they would have for classA operation.

### 4.5.1 FET Parameters

Prior to the design the FET is to be identified. In this implementation, Curtice FET model with the equivalent circuit and parameters, respectively, is used.

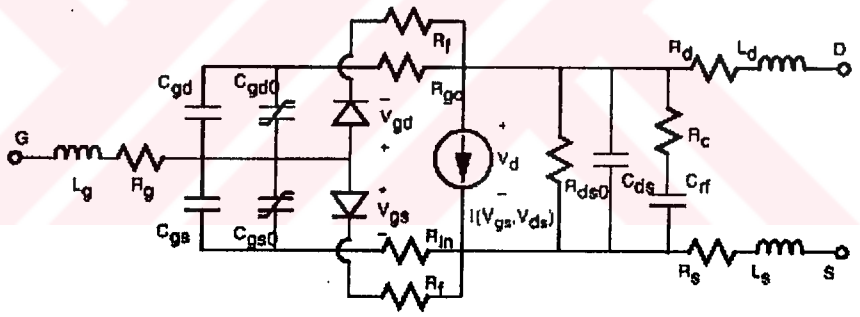


Figure 4.8. Equivalent circuit of Curtice Model GaAs MESFET

Table 1 Parameters for Curtice FET Model

| | | |
|---|---|---|
| BETA | Subthreshold Conduction Parameter | 0.06 |
| GAMMA | Drain I7V knee Parameter | 2 |
| VOUTO | Vds at which subthreshold effects begin | 10V |
| VTO | Pinch-off voltage | -3V |
| A0 | Gate I/V polynomial coefficient | 0.5 |
| A1 | Gate I/V polynomial coefficient | 0.27 |
| A2 | Gate I/V polynomial coefficient | 0.013 |
| A3 | Gate I/V polynomial coefficient | -0.006 |
| R1 | Resistance | 0.001Ω |
| R2 | Resistance | 0.001Ω |
| VBO | Gate-channel breakdown voltage | 1e+06V |
| VBI | G-S capacitance built-in voltage | 1V |
| RF | Gate diode forward bias resistance | 1e+06V |
| IS | Gate conduction diode current parameter | 1e-8mA |
| N | Gate conduction ideality factor | 1 |
| RDS | Drain source resistance | 250Ω |
| CRF | Cap. That sets the RF Rds break freq. | 1e+6pF |
| RD | Drain Resistance | 0.5Ω |
| RG | Gate Resistance | 0.5Ω |
| RS | Source Resistance | 0.5Ω |
| RIN | Intrinsic Resistance | 2Ω |
| CGS0 | CGS at 0V | 0.9pF |
| CGD0 | CGD at 0V | 0.2pF |
| FC | Gate cap. Linearization Parameter | 0.5 |
| CDS | Drain Source Capacitance | 0.4pF |
| TNOM | Temperature | 27degree |
| RGD | Gate Drain Resistance | 0.001Ω |
| RDS0 | Constant drain-source res. | 1e+6Ω |
| LG | Gate Inductance | 0.25nH |
| LS | Source Inductance | 0.1nH |
| LD | Drain Inductance | 0.25nH |
| AFAC | Gate-width scale factor | 1 |

Curtice model uses a third-order polynomial to fit the $I_{ds}$ versus $V_{gs}$ characteristic and is often referred to as the cubic model given by;

$$I_{ds} = (A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3)\tanh(\alpha V_{ds}) \tag{4.21}$$

where $V_1$ is the input voltage, and expressed as follows;

$$V_1 = V_{gs}[1 + \beta(V_{ds0} - V_{ds})] \tag{4.22}$$

$\beta$ controls the change in the pinch off voltage with $V_{ds}$, and $V_{ds0}$ is the drain-source voltage at which the $A_i$ coefficients are evaluated.

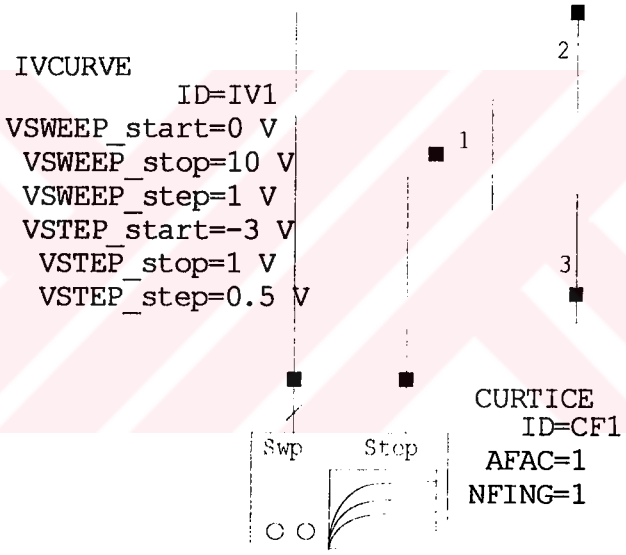


Figure 4.9. FET Characteristic determination Schematic

Simulations can be applied to the circuit shown in Figure 4.9 and the following results can be obtained as shown in Figure 4.10 .

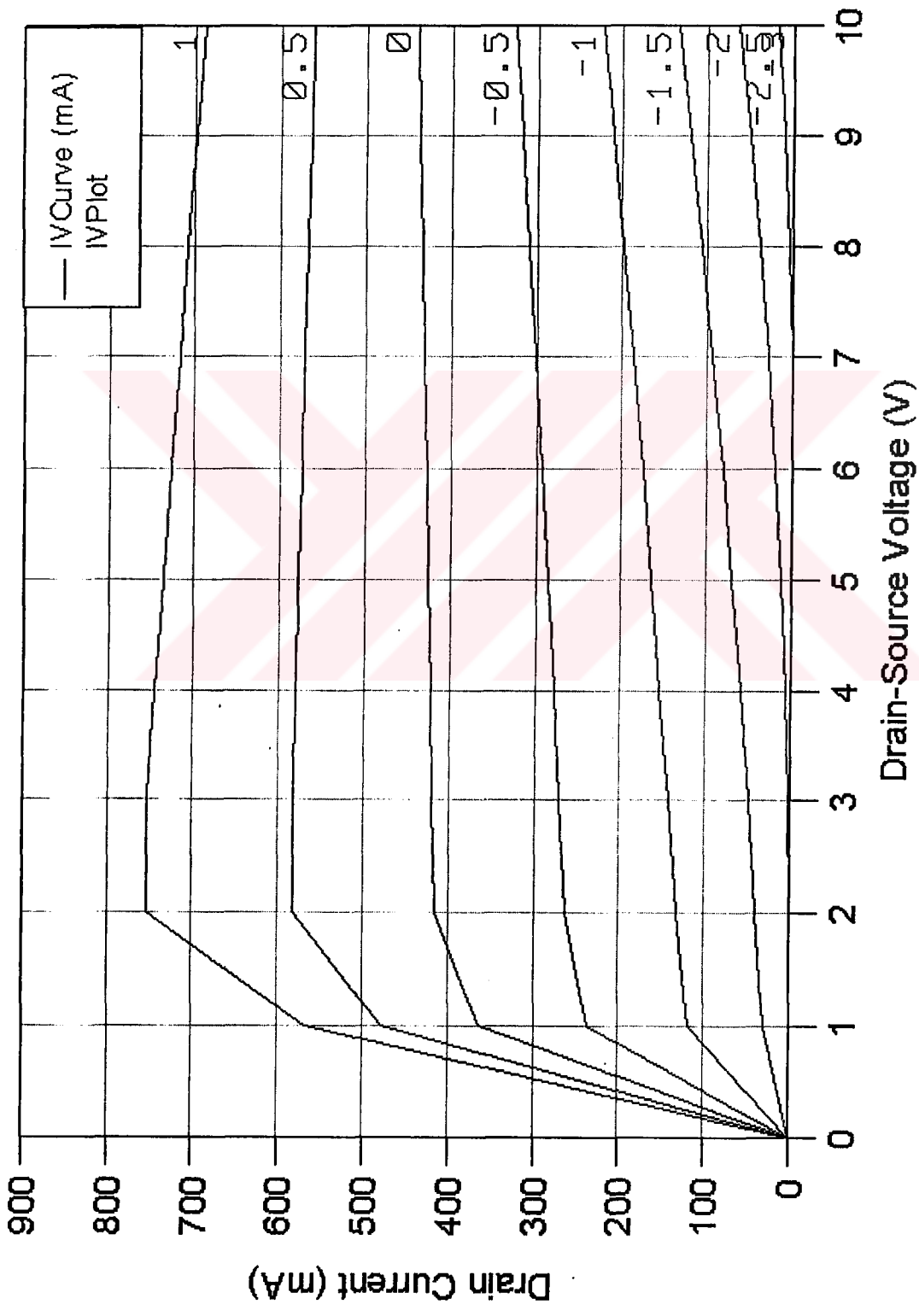


Figure 4.10 The I-V curves for the Curtice FET Model used in the Design

The smith chart of Figure 4.11 shows the curves of $S_{11}$ and $S_{22}$ taken from the large signal model biased at $I_{ds} = 43mA$ *and* $V_{ds} = 10V$. The fits to $S_{21}$ adn $S_{12}$ in decibels versus frequency is also shown in Figure 4.12.

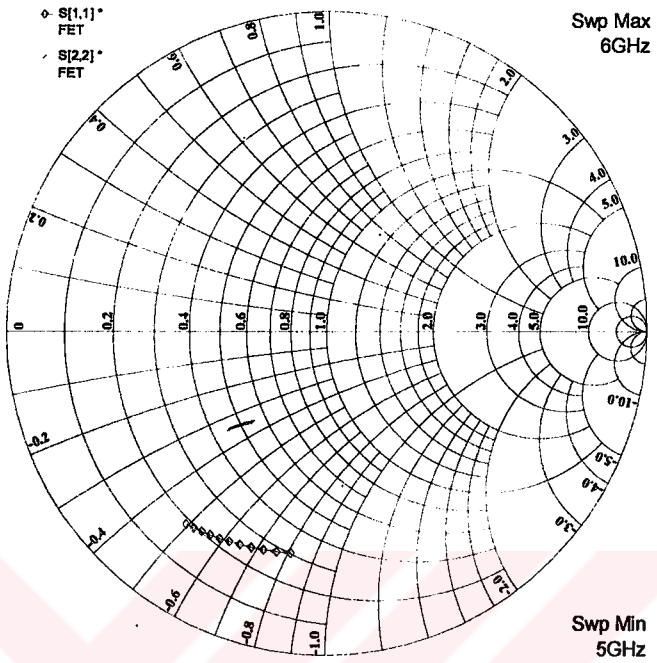


Figure 4.11 Curves of $S_{11}$ and $S_{22}$ for large-signal model from 5to 6GHz.

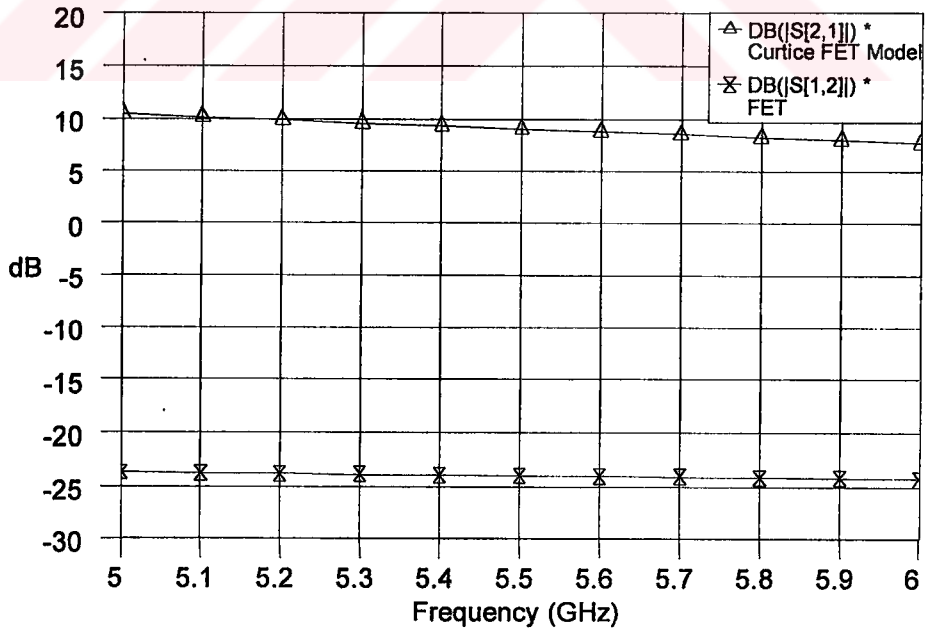


Figure 4.12 Curves of $S_{21}$ and $S_{12}$ for large-signal model from 5 to 6 GHz.

### 4.5.2 Simulation of the 5.2 GHz and 5.8GHz, 1W Class B Push-Pull Amplifier

The microstrip schematic of the designed stage is shown in Figure 4.13.including circuit capacitors, dc bias voltages, matching circuit, and the designed modified ring hybrid. Here, at the input and at the output, modified ring hybrid is used to obtain $180^{o}$ phase shift which is necessary for the push-pull configuration.

The transmission lines called TL19, TL20 (at the input of the FET) and TL21, TL22 (at the output of the FET) is used as inductance to match the input and output impedance of the FET.

This circuit is biased at $I_{dsQ}$=43mA at $V_{ds}$=10V. This is 10%$I_{dss}$. Hence, this shows that, the circuit does not work purely as class B but conduction angle is not much larger than $180^{o}$, and this is to be distinguished from ClassAB.

As a matching circuit, TL1, TL19 , TL11, TL7 is used at the input. By the helps of this matching circuit the input impedance is matched to a resistive value and by the helps of TL4 and TL10 quarter wave length transmission lines, these values are matched to 50Ω. On the other hand, at the output, as a matching circuit, TL2, TL6, TL8, TL12 is used and matched to a resistive value, and by using the quarter wave length transmission lines TL3 and TL9 these resistive values are matched to 50Ω.

One important point of this circuit is the usage of quarter wavelength and λ/12 transmission lines at the drain location. RF bypass capacitor terminated (5pF) short-circuited stubs connected at the drain reactively shorts the second harmonic. However, at twice the fundamental frequency, the line becomes λ/2 long, providing low impedance to the second harmonic. λ/12 open stub is used to short the third harmonics. Three times the fundamental frequency the lines shows low impedance and shorts the third harmonics. These are all done to increase the over all efficiency of the circuit. These transmission lines are also part of the matching networks [11].

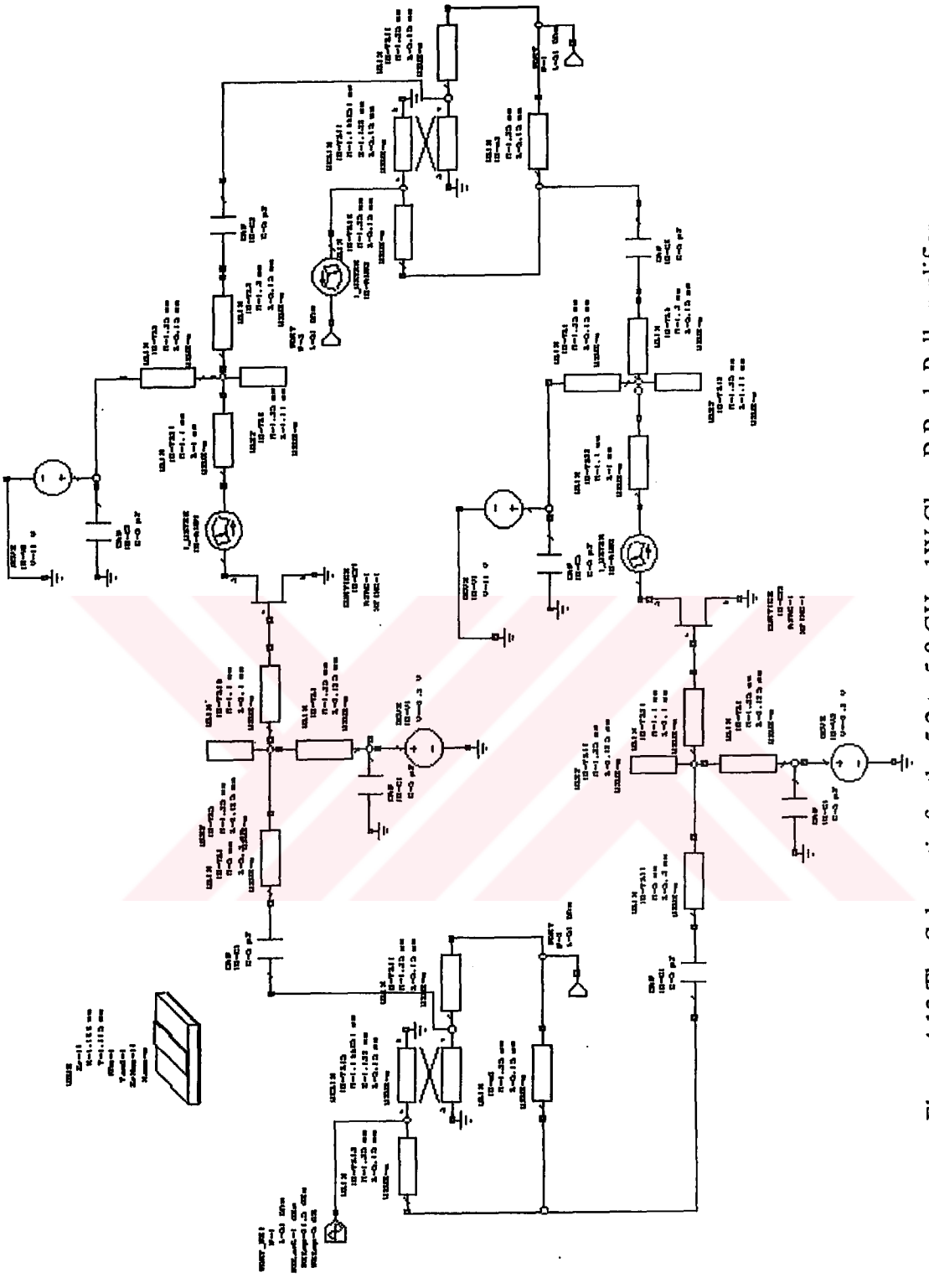

Figure 4.13 The Schematic for the 5.2 to 5.8 GHz, 1W Class B Push-Pull amplifier

The input and output matching results are shown in Figure 4.14 on a smith chart. Here, 1 is defined as the input, 3 is defined as the output port.

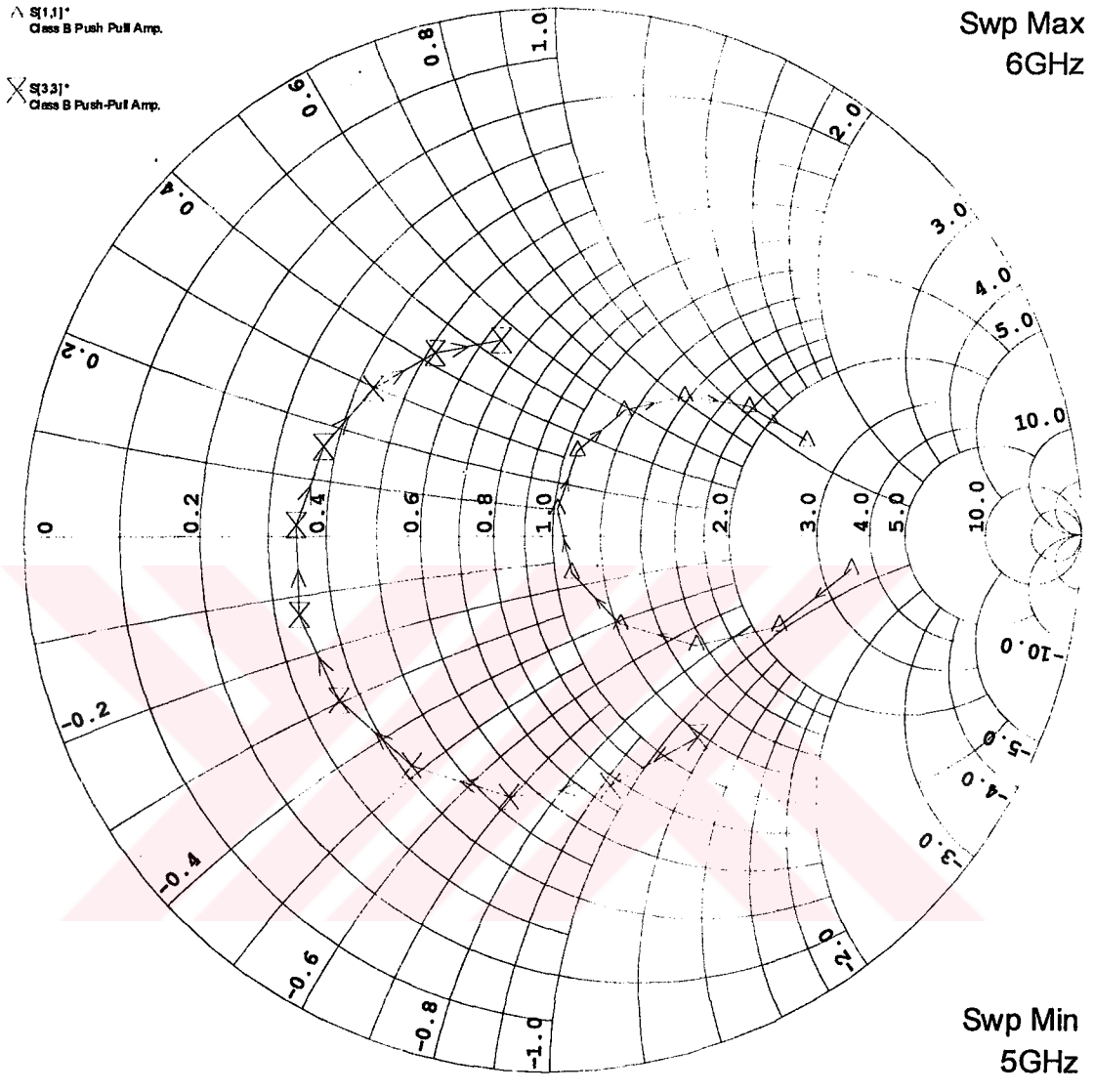


Figure 4.14 Curves of $S_{11}$ and $S_{33}$ for large-signal model from 5to 6GHz for ClassB Push Pull amplifier circuit.

If the values at the previous simulation is calculated in dB. Following results occurs;

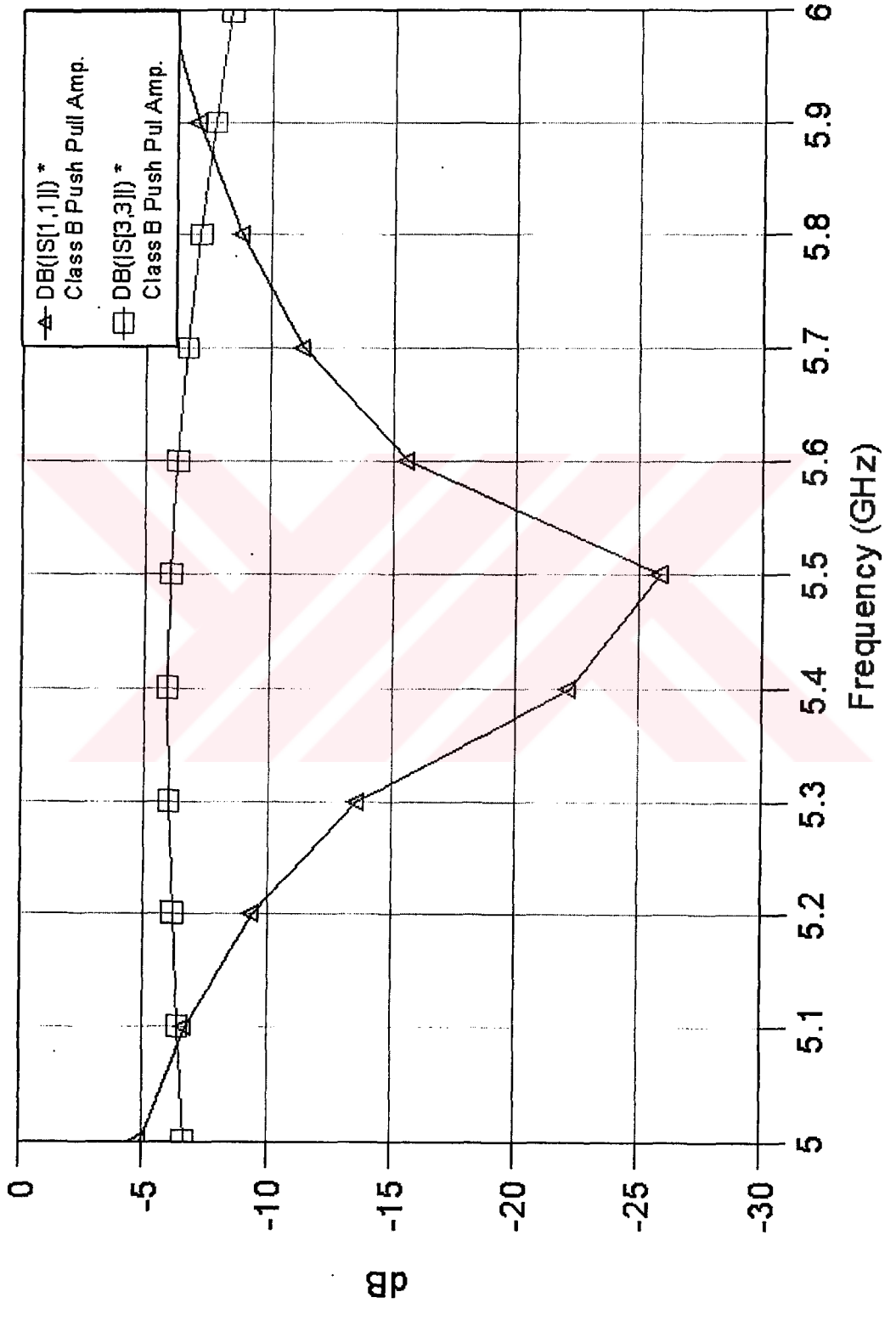


Figure 4.15 S parameters in dB for Class B Push Pull Amplifier Circuit

As it can be seen from the smith chart and the figure input and output is properly matched to 50Ω.

Total Current waveforms are monitored at three points, at the drain point of FET1 and FET2, and at the output when $P_{in}$=20dBm. As it is seen from the figure the current in the drain point quite similar to the classB half sine wave.

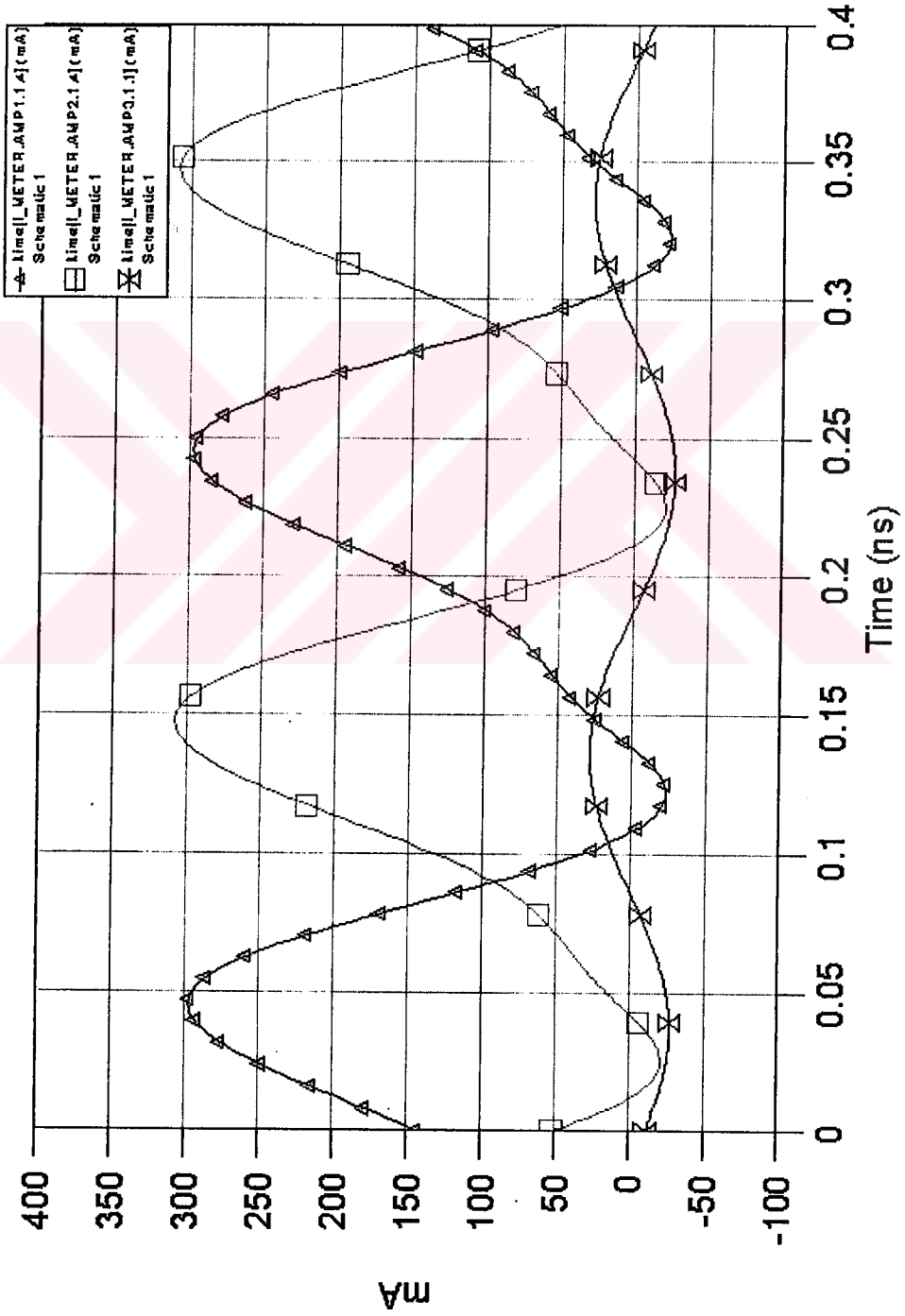


Figure 4.16 Current Waveforms in simulated circuit

Finally, for the circuit shown in Figure 4.13, power sweep analysis between 5GHz and 6GHz is done by the helps of Harmonic balance simulator. While making this simulation, the circuit is driven by a power source sweeping from 0dBm to 25dBm. So that, it can be possible to see the important data from simulation such as 1dB compression point, gain at different input signals.

From Figure 4.17, Output 1dB compression point is detected as 34dBm and input 1dB compression point is 22Bm. When $P_{in}$=17dBm, output power $P_{out}$ is 30dBm. At this point efficiency is 34.5%.

From Figure 4.18 it can be easily seen that, in the frequency band the gain can be accepted as constant with maximum 1dB fluctuation.

To see harmonic product levels the circuit is driven with a source with $P_{in}$=0dBm at the fundamental frequency, 5.5 GHz.

From Figure 4.19, the second and third harmonic levels are below -47.3dBm and -60.6dBm,respectively.

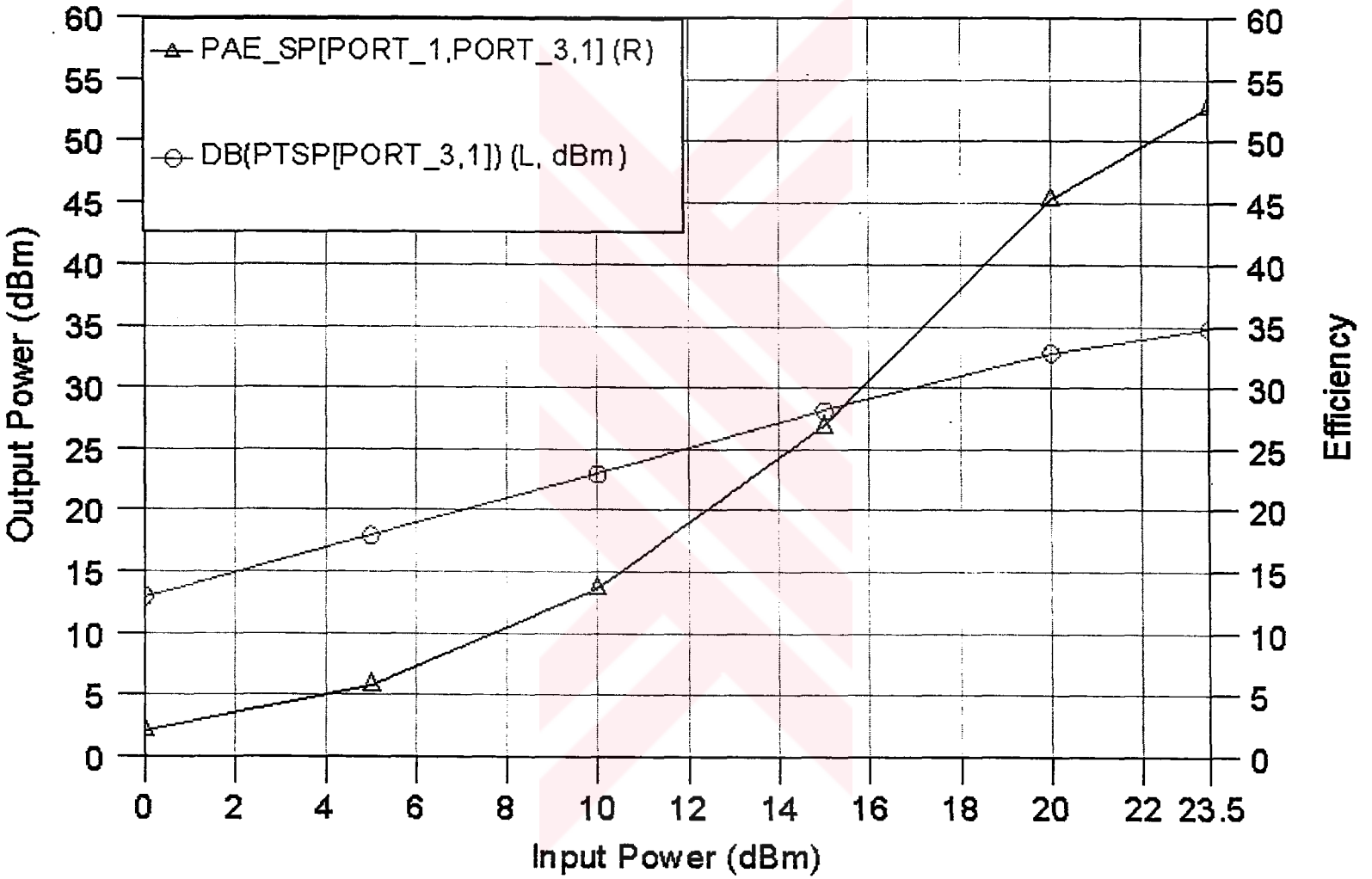


Figure 4.17 Output Power and Efficiency vs Input Power (dBm)

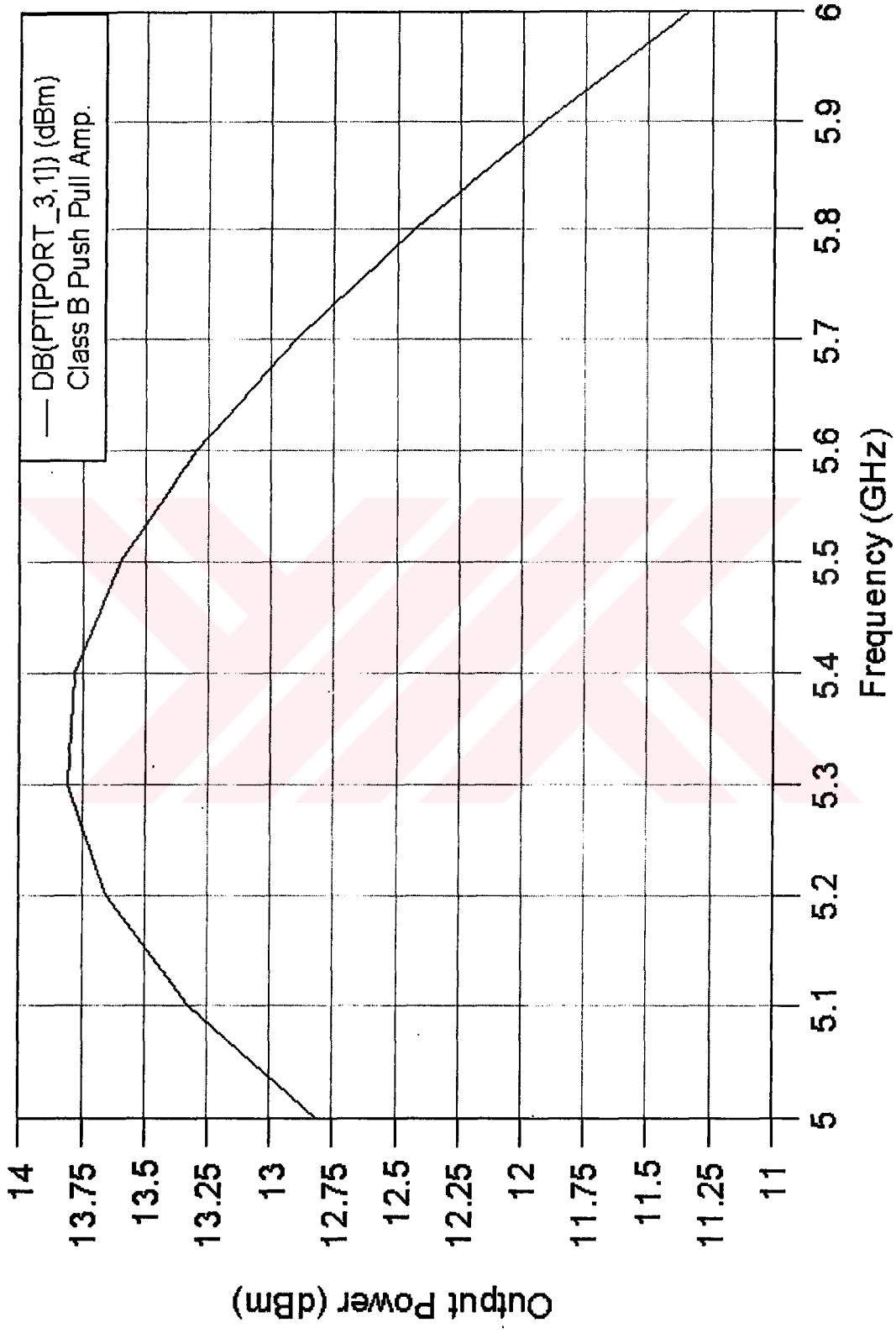


Figure 4.18 Output Power (dBm) vs. Frequency (GHz)

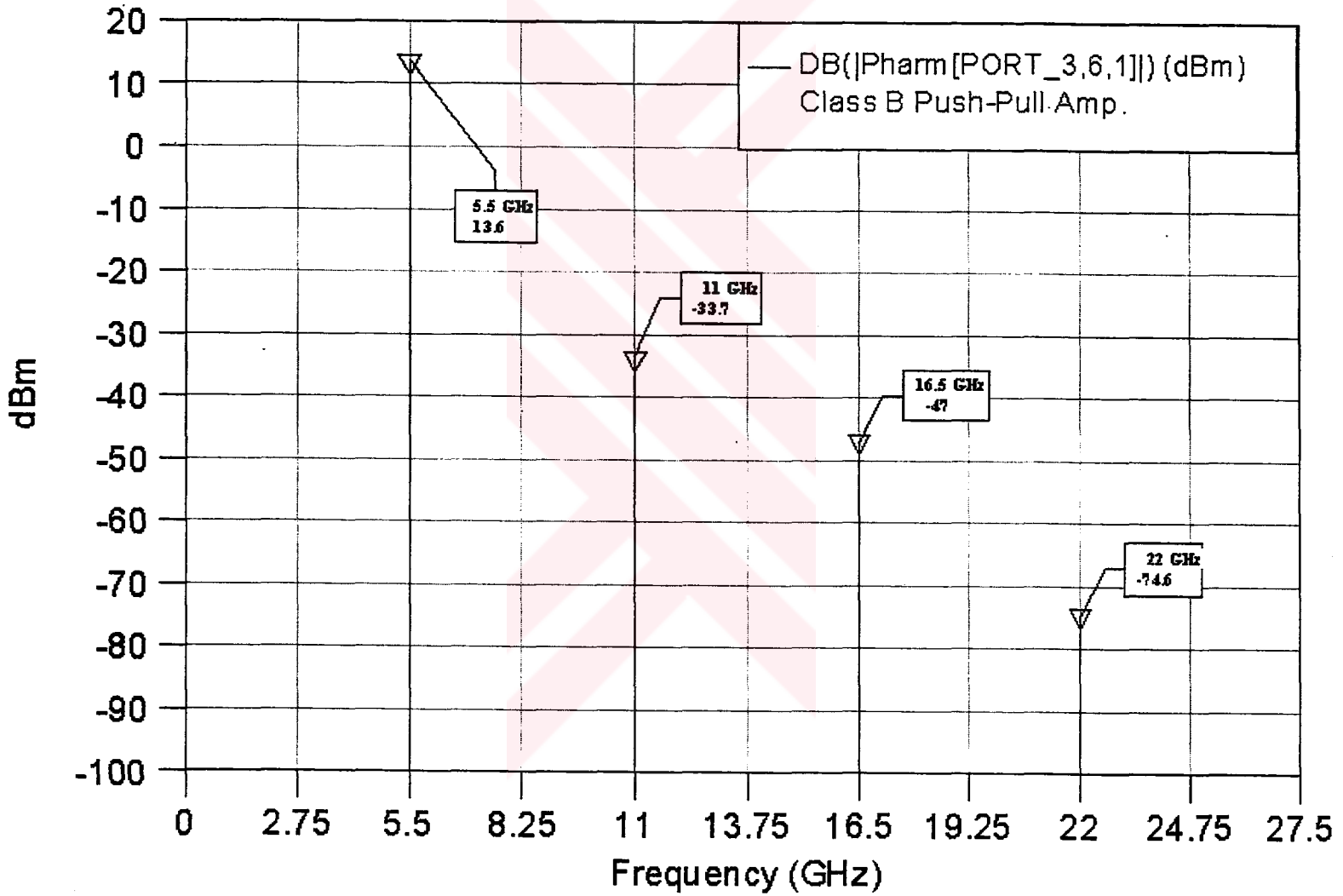


Figure 4.19 Output Power for fundamental, second and Third harmonic

# 5 CONCLUSION

In this work, a high efficiency 1W ClassB amplifier is designed for Hiperlan/2 applications. First, the process which will be used in the design is investigated as GaAs MESFET technology.

Secondly, the important things for Hiperlan/2 transceiver is investigated, and according to the results the class and the type of the amplifier is identified. As an efficient and proper solution Class B push pull amplifier type is chosen.

For push pull type, a transformer is necessary for 180° phase reversal, but in an IC it is very difficult to obtain a transformer. An alternative solution is found for this situation. This is 180° Modified ring hybrid.

The ring hybrid investigated is used in the circuit and this circuit is designed in a way that harmonic components are compressed by the helps of proper design rules.

Finally, an efficient power amplifier is obtained, which has 1W output with 34.5% efficiency.

For further enhancements, the circuit can be developed by power supply modulation. The amplifier voltage supply is modulated with the envelope of the RF signal, for lower input signal levels, the nominal supply voltage is low, and increased only when required In a such case, power amplifier efficiency increases greater than 15% are reported in the literature.

## REFERENCES


[1] **European Radio Communications Committee,** 1999. ERC Decision of 29 November 1999 on the harmonised frequency bands to be designated for the introduction of High Performance Radio Local Area Networks (HIPERLANs), *European Conference of Postal and Telecommunications Administrations.*

[2] **Torsner, J. And Malmgren, G.,** Radio Network Solutions For Hiperlan/2, Sweden.

[3] **Johnsson, M.,** 1999. Hiperlan/2 – The Broadband Radio Transsmission Technology Operating in the 5 GHz Frequency Band, *Hiperlan/2 Global Forum*, 1999.

[4] **Ludwig, R. And Bretchko, P.,** 2000. RF Circuit Design Theory and Applications, Prentice Hall, New Jersey

[5] **Maas, S. A.,** 1988. Nonlinear Microwave Circuits, Artech House, MA.

[6] **March, S.,** 1968. A Wideband Stripline Hybrid, *IEEE Transactions on Microwave Theory and Techniques.* pp361.

[7] **Pothecary, N.,** 1999. Feedforward Linear Power Amplifiers, Artech House, MA.

[8] **Razavi, B.,** 1998. RF Microelectronics, Prentice Hall, NJ

[9] **Bahl, I. And Bhartia, P.,** 1988. Microwave Solid State Circuit Design, John Wiley & Sons

[10] **Walker, J. L. B.,** 1993. High-Power GaAs FET Amplifiers, Artech House, MA.

[11] **Bahl, J. B., Griffin, E. L., Geissberger, A. E., Andricos, C., Brukiewa, T. F.,** 1989. Class-B Power MMIC Amplifiers with 70 Percent Power-Added Efficiency, *IEEE Transactions on Microwave Theory and Techniques.* pp1315

[12] **Lane, J. R., Freitag, R. G., Hahn, H., Degenford, J. E., Cohn, M.,** 1986. High-Efficiency 1-, 2-, and 4-W Class-B FET Power Amplifiers, *IEEE Transactions on Microwave Theory and Techniques.* pp1318.

[13] **Curtice, W. R., Ettenberg, M.,** 1985. A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers, *IEEE Transactions on Microwave Theory and Techniques.* pp1383

[14] **Bowick, C.,** 1982. RF Circuit Design, Newnes, MA.

[15] **Larson, L. E.,** 1997. RF and Microwave Circuit Design for Wireless Communications, Artech House, MA:

[16] **Walrand, J., VARAIYA, P.,** 2000. High-Performance Communication Networks, Morgan Kaufmann Publishers, San Francisco.

[17] **Hanington, G., Chen, P., Asbeck, P., Larson, L.,** 1999. High Efficiency Power Amplifier Using Dynamic Power Supply Voltage for CDMA Applications, *IEEE Transactions on Microwave Theory and Techniques*. pp1471.

## APPENDIX A: Harmonic Balance Method

The solution to the nonlinear circuit problem can always be found by integrating the differential equations that describe the system. However, in most microwave circuits; steady state response with periodic excitations and periodic responses with a limited number of significant harmonics are interested in. In that situation Harmonic balance technique is much more efficient.

In the conventional harmonic balance technique, each state variable in the total nonlinear network is represented by a Fourier Series that satisfies the requirement of periodicity. An optimization algorithm is then used to adjust the coefficients of the Fourier Series such that the system equations are satisfied with least error. Although this method avoids the computationally expensive process of numerically integrating the dynamic equations, its main disadvantage is the large number of variables that must be optimized.

This method is working as follows:

The nonlinear network is decomposed into a minimum possible number linear and nonlinear subnetworks. The frequency-domain analysis of the linear subnetwork is carried out at a frequency $\omega_0$ and its harmonics.

$I_k(k\omega_0) = Y(k\omega_0)V_k(k\omega_0) + J_k(k\omega_0)$ where k=1, ....., N, N being the number of significant harmonic considered, I and V are the vectors of current and voltage phasors at subnetwork, Y represents its admittance matrix, J is a vector of Norton Equivalent Current Sources. The nonlinear subnetwork is analyzed in the time domain. A Fourier Expansion of the current yields;

$$i(t) = \left\{ \mathrm{Re} \sum_{k=0}^{N} F_k(k\omega_0) \exp(jk\omega_0 t) \right\} \qquad \text{(A.1.)}$$

where coefficients $F_k$ are obtained by a FFT algorithm. The harmonic balance technique involves a comparison of A.1 and A.2 Y to yield a system of equation as;

$$F_k(k\omega_0) - Y(k\omega_0)V_k(k\omega_0) - J_k(k\omega_0) = 0, \qquad k = 0,1,\ldots..,N \tag{A.2.}$$

The solution of this system of equations yields the response of the circuit in terms of voltage harmonics $V_k$. Numerically the solution of A.3. is obtained by minimizing the harmonic balance error

$$\Delta\varepsilon_b(V) = \left\{\sum\left|F_k(k\omega_0) - Y(k\omega_0)V(k\omega_0) - K_k(k\omega_0)\right|^2\right\}^{1/2} \tag{A.3.}$$

**APPENDIX B: Power Amplifier Netlist**

```
DIM
  VOL V
  CAP PF
  LNG MM
 TIME NS
  RES OH
  CUR MA
 TEMP C
  IND NH
  PWR DBM
  ANG DEG
CKT
DCVS 12 0 ID="V1" V=-2.2
CAP 12 0 ID="C1" C=5
DCVS 22 0 ID="V2" V=10
CAP 22 0 ID="C2" C=5
MLIN 12 11 ID="TL1" W=0.35 L=2.725 MSUB="s"
MLIN 21 22 ID="TL2" W=0.35 L=5.45 MSUB="s"
MLIN 21 7 ID="TL3" W=1.3 L=5.45 MSUB="s"
CAP 15 7 ID="C3" C=5

CURTICE 8 28 0 ID="CF1" BETA\0.06 GAMMA\2 VOUTO=10 &
  VTO=-3 A0=0.5 A1=0.27083 A2=0.01389 A3=-0.00694 &
```

```
   TAU=0 R1=0.001 R2=0.001 VBO=1e+06 VBI=1 RF=1e+06 &
   IS=1e-08 N=1.3 RDS=250 CRF=1e+06 RD=0.5 RG=0.5 &
   RS=0.5 RIN=2 CGSO=0.9 CGDO=0.2 FC=0.5 CDS=0.4 &
   CGS=0 CGD=0 TNOM=27 LAMBDA=0 RGD=0.001 RDSO=1e+06 &
   LG=0.25 LS=0.1 LD=0.25 AFAC=1 NFING=1
MLIN 29 11 ID="TL4" W=5 L=5.3 MSUB="s"
MLEF 11 ID="TL5" W=0.35 L=2.725 MSUB="s"
MLEF 21 ID="TL6" W=0.35 L=1.81 MSUB="s"
DCVS 1 0 ID="V3" V=-2.2
CAP 1 0 ID="C4" C=5
DCVS 17 0 ID="V4" V=10
CAP 17 0 ID="C5" C=5
MLIN 1 9 ID="TL7" W=0.35 L=2.725 MSUB="s"
MLIN 18 17 ID="TL8" W=0.35 L=5.45 MSUB="s"
MLIN 18 20 ID="TL9" W=1.3 L=5.45 MSUB="s"
CAP 19 20 ID="C6" C=5
CURTICE 10 23 0 ID="CF2" BETA\0.06 GAMMA\2 VOUTO=10 &
   VTO=-3 A0=0.5 A1=0.27083 A2=0.01389 A3=-0.00694 &
   TAU=0 R1=0.001 R2=0.001 VBO=1e+06 VBI=1 RF=1e+06 &
   IS=1e-08 N=1.3 RDS=250 CRF=1e+06 RD=0.5 RG=0.5 &
   RS=0.5 RIN=2 CGSO=0.9 CGDO=0.2 FC=0.5 CDS=0.4 &
   CGS=0 CGD=0 TNOM=27 LAMBDA=0 RGD=0.001 RDSO=1e+06 &
   LG=0.25 LS=0.1 LD=0.25 AFAC=1 NFING=1

MLIN 34 9 ID="TL10" W=5 L=5.3 MSUB="s"
MLEF 9 ID="TL11" W=0.35 L=2.725 MSUB="s"
```

```
MLEF 18 ID="TL12" W=0.35 L=1.81 MSUB="s"
MLIN 5 3 ID="TL13" W=0.35 L=5.45 MSUB="s"
MLIN 6 4 ID="TL14" W=0.35 L=5.45 MSUB="s"
MCLIN 3 0 0 6 ID="TL15" W#0.2 0.499657 0.7 S\0.032 &
  L=5.45 MSUB="s"
MLIN 5 4 ID="s2" W=0.35 L=5.45 MSUB="s"
MSUB Er=10 H=0.866 T=0.005 Rho=1 Tand=0 ErNom=10 Name="s"
MLIN 19 16 ID="TL16" W=0.35 L=5.45 MSUB="s"
MLIN 15 14 ID="TL17" W=0.35 L=5.45 MSUB="s"
MCLIN 16 0 0 15 ID="TL18" W#0.2 0.499657 0.7 S\0.032 &
  L=5.45 MSUB="s"
MLIN 19 14 ID="s3" W=0.35 L=5.45 MSUB=""
CAP 6 29 ID="C7" C=5
CAP 5 34 ID="C8" C=5
MLIN 11 8 ID="TL19" W=1.4 L=2.1 MSUB="s"
MLIN 9 10 ID="TL20" W=1.4 L=2.1 MSUB="s"
I_METER 16 39 ID="AMP3"
MLIN 40 21 ID="TL21" W=0.8 L=1 MSUB="s"
MLIN 41 18 ID="TL22" W=0.8 L=1 MSUB="s"
I_METER 40 28 ID="AMP1"
I_METER 41 23 ID="AMP2"
PORT_PS1 3 P=1 Z=50 PStart=0 PStop=20 PStep=5 Ang=0
PORT 4 P=2 Z=50
PORT 39 P=3 Z=50
PORT 14 P=4 Z=50
DEF0P circuit_1
```

## BIOGRAPHY

Serkan TOPALOĞLU was born in Samsun, Turkey in 1977. He received his B.S. degree in Electronics and Communication Engineering from Istanbul Technical University in 1999. Since 1999, he has been working as a research and teaching asistant at the Faculty of Engineering – Architecture, Electrical and Electronics Engineering Department of Yeditepe University, Istanbul Turkey. In his spare time, he enjoys playing and watching basketball, plane modeling, collecting hologram pictures.