ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

LOW POWER AND COMPACT VLSI NEURONS WITH NETWORK DYNAMICS

Ph.D. THESIS

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Department of Electronics and Communication Engineering

Electronics Engineering Programme

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

AĞ DİNAMİĞİNE SAHİP DÜŞÜK GÜÇLÜ VE KOMPAKT VLSI SİNİR HÜCRELERİ

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Ahmet Şamil DEMİRKOL, a **Ph.D.** student of ITU **Graduate School of Science Engineering and Technology** student ID **504072201**, successfully defended the **dissertation** entitled "**LOW POWER AND COMPACT VLSI NEURONS WITH NETWORK DYNAMICS**", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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To my family,

FOREWORD

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ABBREVIATIONS

Izh	**:** Izhikevich
AdEx	**:** Adaptive Exponential Integrate and Fire
HH	**:** Hodgkin Huxley
IF	**:** Integrate and Fire
CM	**:** Current Mirror
SSCM	**:** Source Shifted Current Mirror
ACM	**:** Active Diode Connected Current Mirror
PTAT	**:** Proportional to Absolute Temperature
TC	**:** Temperature Coefficient
MC	**:** Monte Carlo

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LOW POWER AND COMPACT VLSI NEURONS WITH NETWORK DYNAMICS

SUMMARY

In this thesis, three low power and compact VLSI neurons, operating at biological timescale, are designed. Each neuron circuit realizes a mathematical neuron model. The models utilized are namely Izhikevich (Izh), Adaptive Exponential Integrate and Fire (AdEx) and Hodgkin-Huxley (HH) neuron model. Additionally, two synaptic circuits with temporal dynamics are realized. Using these synaptic circuits, two AdEx neurons and three/nine Izhikevich neurons are coupled between each other to establish a network. The coupled neurons exhibit the expected network dynamics successfully.

Due to low power and compactness strategy, all the three neurons and synapses are designed with log domain circuits operating in subthreshold region with a current mode approach. Basic building blocks of the neurons and the synaptic circuits are the first order log domain filter and the translinear loop current multiplier/divider circuit. The variables take values in pA range and the values of the bias current are in fA range. To handle such low current values maximally at a few hundreds of Hz frequency, we make use of source shifting and active diode connection techniques in the neuron circuits.

The neuron and synapse circuits are simulated using 0.15 μm CMOS process parameters using Spectre in Cadence design tool. The neurons consume power at only nW level and occupy an estimated chip area below 1000 μm^2. The operating frequency of the VLSI neurons changes from a few Hz to a few hundreds Hz as in biological neurons. Firing patterns of the VLSI neurons match accurately with numerical simulation results proving the success of the designs.

To implement pA and fA current sources, a CMOS only, wide temperature range, low temperature coefficient, pA level current reference circuit is designed. The circuit is based on a well-known topology except the core of proposed design involves serially connected transistors. Thus, voltage offset and temperature compensation method is applied more accurately. The fA level current sources are obtained using a simplified current splitter circuit. Due to the feedback mechanism in the splitter circuit, a stable output current is obtained independent from process and temperature fluctuations. It is shown that a 50 fA DC current source within a reasonable temperature range can be generated.

In order to realize the exponential term in AdEx model, a wide range current mode exponential circuit is designed. For this purpose, Pade approximation method is exploited rather than the traditional Taylor approximation. The exponential circuit is mainly composed of translinear loop current multiplier/divider circuits. As a result, an output range of 43.4 dB is obtained with 0.2 dB error for nominal case and 0.5 dB error for the worst case.

Two similar synaptic circuits, both of which operate linearly with temporal dynamics, are designed. The synaptic model involves a first order differential

equation with sigmoidal steady state and time constant functions. These sigmoidal functions are realized utilizing the exponential circuit in one of the synaptic circuits. In the other synaptic circuit, the exponential circuit is replaced with a differential pair as a simplification. Two AdEx and three and nine Izh neurons are coupled among each other to investigate the synchronization activity of the network. Coupling nine Izh neurons, travelling wave behavior is also observed. The neurons exhibit the expected network dynamics successfully.

AĞ DİNAMİĞİNE SAHİP DÜŞÜK GÜÇLÜ VE KOMPAKT VLSI SİNİR HÜCRELERİ

ÖZET

Biyolojik organizmaların sinir sistemleri yüksek seviyeli bilgi işleyebilen birimlerdir. Bir memeli beyni, görüntü işleme, karar verme, davranış belirleme, motor kontrol gibi görevleri, zorlanmadan hızlı bir biçimde ve az miktarda enerji harcayarak gerçekleştirebilmektedir. Beyin bu görevleri yerine getirirken, yoğun parallel yapısı, dağılmış depolama yeteneği, asenkron çalışabilme, kendi kendine organize olabilme gibi özelliklerini yavaş ve davranış kesinliği yüksek olmayan birimlerle sağlar. Beyin, şaşırtıcı bir şekilde, günümüzdeki bir bilgisayara enerji tüketimi, kapladığı alan ve performans açısından kolayca üstünlük sağlamaktadır. Beynin nasıl çalıştığını tam olarak anlamakan çok uzak olsak da, en azından bazı küçük alt kısımların yapısı ve işlevselliği hakkında detaylı bilgiye sahibizdir. Mühendislik bakış açısından, beyni daha alt seviyelerde incelemek ve anlamaya çalışmak, donanımsal benzetim araçları, beyin performanslı sistemler veya akıllı makineler gibi biyomimetik sistemlerin tasarımı için ümit vermektedir.

Biyolojik sistemlere yapısal olarak, hesaplama yeteneği ve verimi açısından benzeyen ve taklit eden analog devrelere nöromorfik devreler denmektedir. Nöromorfik mühendisliği iki ana kısımdan oluşmaktadır: beynin hesaplama özelliğini araştırmak için uygun devrelerin tasarımı ve endüstriyel üretime uygun verimli nöromorfik devrelerin tasarımı. İlk kısım biyolojik sinir sistemlerinin silikon bir donanımda incelenmesi anlamına gelirken ikinci kısım ise beyin performanslı özgün sistemlerin tasarımını ifade etmektedir. Her iki durumda da, mevcut bilgisayar sistemlerin seri yapısının aksine, beynin yoğun paralel yapısı ve asenkron veri işleme yeteneği, yazılımsal çözümlerin yavaş ve kompleks yapıda olmasına neden olmaktadır. Örnek vermek gerekirse, algılayıcı ya da beyin performanslı sistemlerin tasarımı donanımsal olarak daha hızlı ve ucuz gerçeklenebilir. Benzer şekilde donanımsal bir sistem, bir araştırmacı için gerçek zamanlı veri toplama ve işlemeyi mümkün kılmaktadır. Aynı zamanda, hesaplamalı sinirbiliminde donanımsal sistemlere olan ilgi de artmaktadır. Dahası, bazı çalışmalarda büyük ölçekli ağların bezetiminde detaylı sinir hücresi modelleri tercih edilmektedir. Bu nedenle güçlü bilgisayar sistemlerine ihtiyaç duyulmaktadır. Fakat bu yavaş ve pahalı bir çözümdür. Bundan dolayı, donanımsal çözümler halen güçlü bir çözüm seçeneği oluşturmaktadır.

Sinir hücresi modelleri, hesaplama kolaylığı açısından basit bir system olan Tut ve Ateşle (I&F) modelinden biyolojik anlamlılığı olan Hodgkin-Huxley (HH) modeline kadar çeşitlilik göstermektedir. Donanımsal bir gerçekleme için uygun model seçimi, uygulamadaki hassasiyete ve elektronik gerçekleme koalylığına göre değişebilir. Nöromorfik mühendisliğinin ilk yıllarında genellikle algılayıcı sistemlerle ilgilenilmiştir. Bu çalışmalarda da elektronik gerçeklemesi kolay basit modeler tercih edilmiştir. Fakat hesaplamalı sinirbiliminde son dönemdeki gelişmelerin gösterdiğine

göre, indirgenmiş dinamik modeller dinamik özelliklere etki etmekte ve hesaplama özelliğini önemli derecede azaltmaktadır. Bu nedenle, belirgin bir sebep olmadıkça, beyin performanslı sistemler için indirgenmiş modeler kullanmak doğru bir yol değildir. Bu gerçekten yola çıkarak, son dönemlerde, dinamik olarak tatminkar elektronik nöronlar tasarlanmıştır. Fakat bu durum, donanım tasarımı hakkında bilgisi olmayan bir araştırmacı için faydanılması zor bir çözüm yoludur. Bundan dolayı gerçekçi bir tasarımın, zengin dinamiklere sahip gerçekçi bir nöron modeli içermesi gerekmektedir. Böylece daha güçlü donanımsal benzetim gereçleri ve beyin performanslı sistemlerin tasarımı mümkün olacaktır.

Bir sinir ağını oluşturan nöronlar, birbiriyle sinaps adı verilen özelleşmiş birimlerle bağlıdırlar. Son dönemki deneysel ve hesaplamalı çalışmaların gösterdiği üzere, sinapslar öğrenme ve hafıza için temel olan uzay zamansal örüntülerin kodlanmasında önemli bir yere sahiptir. Buna karşın, hesaplamalı modellerde sinapsların zamana bağlı özellikleri çoğu kez göz ardı edilmiş ve tipik olarak anlık çarpım işleci olarak kabul edilmiştir. Sinir ağlarının çok geniş ölçekli tümdevre (VLSI) uygulamalarında da, silikon sinapslar basit çarpma devrelerine indirgenmiştir. Sinaptik modellerin önemi daha iyi anlaşıldığından dolayı gerçekçi sinir ağlarının tasarımında zamana bağlı özellikleri içeren sinapslar tercih edilmelidir.

Bu tez çalışmasında, yukarıdaki fikirlerden yola çıkarak, üç adet düşük güçlü, kompakt ve biyolojik zaman ölçeğinde çalışan VLSI sinir hücresi tasarlanmıştır. tasarlanan her bir sinir hücresi matematiksel bir modele sahiptir. Bu modeler, sırasıyla, Izhikevich (Izh), Uyarlamalı Üstel Tut ve Ateşle (AdEx) ve Hodgkin-Huxley (HH) sinir hücresi modelleridir. Ayrıca, zamana bağlı bir dinamiğe sahip iki adet sinpatik devre tasarlanmıştır. Bu sinaptik devreler kullanılarak, iki AdEx nöronu ve üç/dokuz Izh nöronu birbirine bağlanılarak bir sinir ağı oluşturulmuştur. Bu nöronlar, beklenen ağ dinamiğini başarılya sergilemiştir.

Düşük güç ve kompaktlık amacından dolayı nöron ve sinapslar, eşikaltı bölgede çalışan logaritmik tabanlı devreler kullanılarak akım modlu olacak şekilde tasarlanmıştır. Nöron ve sinaps devrelerinin temel blokları, birinci derece logaritmik tabanlı filtre ve translineer çevrimli akım çarpma/bölme devresidir. Değişkenler pA mertebesinde değerler almaktayken kutuplama akımları fA mertebesinde değerler almaktadır. Sinir hücrelerinde bu derece düşük akım değerlerinde ve en fazla birkaç yüz Hz frekanslarında çalışabilmek için, kaynak gerilimi öteleme ve aktif diyot bağlama tekniği kullanılmıştır.

Sinir hücresi ve sinaps devrelerinin benzetimi, 0.15 µm CMOS proses parametreleri kullanılarak Spectre programıyla Cadence ortamında yapılmıştır. Nöronlar nW mertebesinde güç harcamakta ve kapladıkları alan 1000 μm^2 den daha küçük olmaktadır. Çalışma frekansları, gerçek nöronlarda olduğu gibi bir kaç Hz ile birkaç yüz Hz arasında değişmektedir. VLSI nöronlardan elde edilen ateşleme örüntüleriyle sayısal benzetim yapılarak elde edilen örüntüler çok iyi uyum göstererek ve tasarımın başarısını ortaya koymaktadır.

Ayrıca, pA ve fA mertebesindeki akım kaynaklarını gerçekleyebilmek için salt transistörlü, geniş sıcaklık aralığına sahip, düşük sıcaklık katsayılı, pA mertebesinde bir akım referans devresi gerçeklenmiştir. Bu devre bilinen bir topolojiye dayanmakla beraber, devrenin çekirdek kısmı seri bağlı transistörlerden oluşmaktadır. Böylece offset gerilimi ve sıcaklık kompanzasyon tekniği daha isabetli bir şekilde uygulanmıştır. fA mertebesindeki akımlar, basitleştirilmiş bir akım dağıtıcı devreyle sağlanmıştır. Bu devreye ait geri besleme mekanizması sayesinde üretim ve sıcaklık değişikliğinden bağımsız kararlı akım değerleri elde edilmiştir. Bu

sayede makul bir sıcaklık aralığında 50 fA değerinde sabit akım kaynağı elde edilebileceği gösterilmiştir.
Ek olarak, AdEx modelindeki üstel terimi gerçeklemek üzere, geniş çıkış aralığına sahip akım modlu bir üst alma devresi tasarlanmıştır. Bu amaçla geleneksel olan Taylor yaklaşımı yerine Pade yaklaşıklığı kullanılmıştır. Üst alma devresi temel olarak translineer çevrimli akım çarpma/bölme devrelerinden oluşmaktadır. Sonuçta, 43.4 dB çıkış aralığına sahip, tipik değerler için 0.2 dB ve en kötü durumda 0.5 dB hataya sahip bir devre elde edilmiştir.
Son olarak, doğrusal ve zamana bağlı dinamiklere sahip iki adet benzer sinaptik devre tasarlanmıştır. Kullanılan sinaptik model sigmoidal zaman sabitine ve kararlı hal fonksiyonuna sahip birinci derece bir diferansiyel denklem içermektedir. Bu sigmoidal fonksiyonlar, ilk sinaptik devrede üst alma devresi kullanılarak gerçeklenmiştir. Diğer sinaptik devrede ise basitleştirme amaçlı olarak sigmoidal işaretler fark kuvvetlendiricisi kullanılarak gerçeklenmiştir. İki AdEx ve üç/dokuz Izh nöronu kendi aralında birbirine bağlanarak iki küçük ağ oluşturulmuş ve senkronizasyon davranışları incelenmiştir. Nöronlar, başarılı bir şekilde ağ dinamiği davranışı sergilemişlerdir.

1. INTRODUCTION

1.1 Motivation

The nervous system of a biological organism is a very high-level information-processing unit. A mammalian brain can perform complex tasks such as vision processing, decision-making, action selection, and motor control and so on, effortlessly, fast and energy efficiently. The brain performs these tasks utilizing massive parallelism, distributed storage, asynchronous processing, and self-organization with slow and imprecise elements. Impressively, the brain can easily outperform today's computers in terms of power consumption, occupied area and performance easily. Although we are far away from understanding how the whole brain works, there exist detailed knowledge about the structure and functionality of small portions of the brain. From engineering point of view, studying the brain even at lower levels and trying to understand it give us hope to design biomimetic systems such as hardware simulating tools, brain-like performing systems, or intelligent machines in future. For these reasons, electronic implementations of neural systems have been an attractive research area for engineers from past to date [1-12].

Analog circuits that mimic the behaviors of biological neural systems with similar structure, computational property and efficacy are called neuromorphic circuits. The research of neuromorphic engineering is composed of two main parts: designing proper circuits in order to investigate the computational properties of the brain, and developing efficient neuromorphic systems for industrial applications. Following the first part, one can get insight to the biological neural systems in silicon hardware and for the second part, one can attempt to observe brain-like performance of a dedicated system. For both of the cases, massively parallel and asynchronous processing properties of the neural systems in contrast to sequential nature of computer systems make it complex and slow for software solutions. For instance, when it is the case to design a real time system such as sensory or brain-machine interface system, hardware solutions are much more attractive in terms of speed and expense.

Similarly, a hardware solution will also let scientists to interact and process real time data. At the same time, there is also an increasing interest of hardware neural systems in computational neuroscience. Moreover, in some studies, it is preferred to use detailed neuron models while simulating large-scale networks. Therefore, powerful parallel computer systems are required [13] resulting in a slow and expensive solution. Hence, hardware implementations stand for an alternative solution again.

Neuron models vary from the computationally simple Integrate and Fire (I&F) model to biologically meaningful Hodgkin-Huxley (HH) model. The choice of the model for a hardware implementation depends on the accuracy requirements of the application and electronically eases of implementation. During in its' infant phase, neuromorphic engineering applications mostly covered sensory systems [1, 14]. In these works, simple neuron models were preferred for ease of electronic implementation. However, recent improvements in computational neuroscience showed that reducing neuron models affects dynamical property, which also reduces the computational property significantly [15]. Therefore, simple neuron models or reduced neuron models are not proper choices for brain-like performing systems unless a remarkable reason exists. Due to this fact, in some recent works, dynamically satisfactory neurons are designed. However, this choice makes it difficult to benefit from the hardware for someone who has no knowledge of hardware design. Therefore, a realistic design should utilize a realistic electronic neuron relying on a mathematical model with rich dynamics. Thus, it will be possible to design more powerful simulation tools and brain-like performing systems.

In a neural network, neurons are connected with each other via specialized units called synapse. Recent experimental and computational results suggest that synapses play a crucial role in neural coding and encoding spatiotemporal patterns that is essential for learning and memory. On the other side, in computational models of neural systems, the temporal dynamics of synapses have often been neglected where synaptic transmission is typically modeled as an instantaneous multiplier operator. Also in VLSI implementations of neural systems, silicon synapses have often been reduced to simple multiplier circuits. Since the importance of synaptic models are well understood, realistic designs involving temporal dynamics should be considered to build powerful neural networks [16, and references therein].

1.2 Thesis Proposal

In this thesis, based upon the ideas mentioned above, low power and compact VLSI neurons, which rely on very recent and powerful mathematical models and operate at real (biological) timescale, are designed. Additionally, two synaptic circuits with temporal dynamics are implemented in order to couple the designed neurons. By this way, certain network dynamics are observed.

The mathematical models utilized are namely Izhikevich (Izh), Adaptive Exponential Integrate and Fire (AdEx) and Hodgkin-Huxley (HH) neuron model. The neurons consume power at only nW level and occupy an estimated area at the order of 1000 μm^2. The operating frequency of the VLSI neurons changes from a few Hz to a few hundreds Hz as in biological neurons. Firing patterns of the VLSI neurons resemble successfully the numerical simulation results proving the success of the designs. A low power and compact neuron circuit allows designing large-scale neural networks including massive number of neurons. The real time operation property allows designing real time experiment hardware tools or human-machine interface systems. An accurate implementation of a mathematical neuron model creates an opportunity to compare the results with numerical solutions and come up with a robust and successful design.

While designing the neurons, fA level current sources were required because of the low power and compactness strategy. Therefore, a CMOS only, wide temperature range, pA level current reference circuit is designed. Then fA level current sources are obtained using a simplified current splitter circuit. In addition, a wide range current model exponential circuit is designed in order to realize the exponential term in AdEx model. Utilizing the exponential circuit to realize ionic channel equations, a fully current mode Hodgkin-Huxley neuron is also designed.

Lastly, two similar synaptic circuits are designed. Both of these synapses operate linearly with temporal dynamics, different from most of the works in the literature. Two of AdEx and three/nine of Izh neurons are coupled in order to show that they are capable of exhibiting synchronous network dynamics, as a possible application. Synchronization behaviors of the coupled neurons supported with numerical simulations demonstrates the success of the design once again.

1.3 Thesis Structure

The second chapter introduces the biological neuron, its anatomy and electrophysiological behavior. Brief explanations of some useful dynamical systems terms are given. Lastly, some important mathematical neuron models are mentioned.

In the third chapter, operation of transistors in subthreshold region is mentioned. Then sub-circuit blocks required for the low power and compact operation are explained. The design of the current reference circuit and the exponential circuit are given. A comparison between these designs and other similar works in the literature concludes this chapter. A literature overview of VLSI neuron implementations is covered lastly.

The circuit implementations of the low power and compact VLSI neurons are given in the fourth chapter. The firing patterns reproduced from these circuits are compared to that of numerical solutions. The performances of the circuits are also compared with similar works in the literature.

The synaptic equations and circuits are given in chapter five. The synchronization patterns as network dynamics are presented. The numerical and circuit simulation results are compared with each other.

Finally, the thesis concludes with chapter six.

2. NEURONS, NEURON DYNAMICS AND MODELS

2.1 Neurons

Human brain is a very complex system which is continuously receiving information and processing it. The elementary processing units are the nerve cells, or so called *neurons*. There are roughly 10^{11} neurons in the brain, mostly in a region called cortex. Each cortical neuron has approximately 10^4 connections with other neurons. All the neurons and connections are packed into a very small area forming a dense and complex network. To illustrate the density, 10^4 neurons exist per cubic millimeter with several kilometers of wires [17].

Neurons, in fact, form a small portion of all the cells in the brain but they are unique in the sense of data processing and transmitting of electrical signals. Therefore, special interest exists about its structure and operation.

2.1.1 The signal of a Neuron

In neurons, as in other cells, a measurement of the voltage across the membrane using an intracellular electrode shows that there exist a voltage difference across the membrane, called the *membrane potential*. In neurons, this membrane potential is used to transmit signals. Neurons communicate with each other via electrical signals called *action potentials* or breifly *spikes*. The spike signal is an essential measurument of a neuron's activity [18].

Spikes are the result of ionic currents flowing through the ion channels on the cell membrane. A typical spike signal is drawn in Figure 2.1. As seen from this figure, spikes occur by a sharp change of the membrane voltage with a typical peak to peak value of 100 mV and a duration of 1-2 ms. A detailed description of a spike will be given in the following sections.

2.1.2 Anatomy of Neurons

A typical neuron, illustrated in Figure 2.1 has three regions: soma, dendrites and axon. Soma is the cell body where all the metabolic events occur. From engineering point of view, it is the central processing unit.

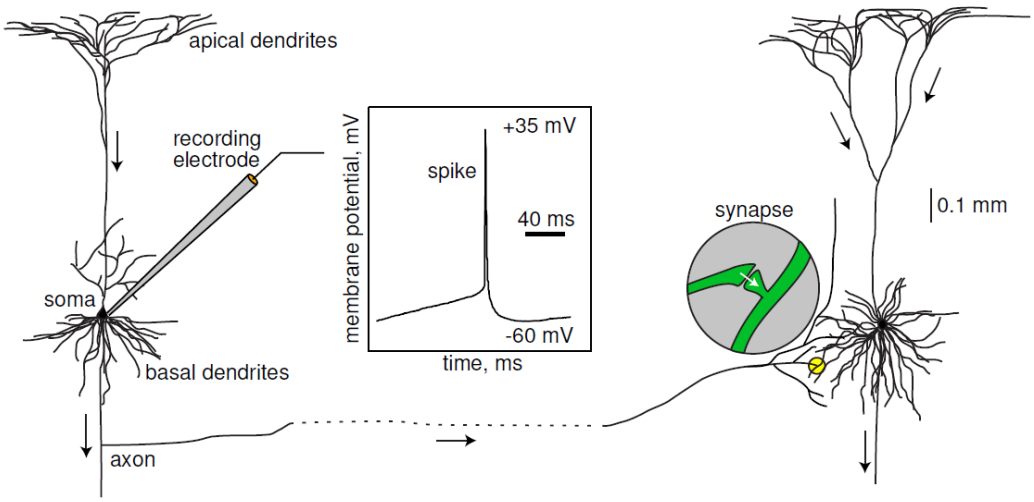

Figure 2.1 : Two interconnected cortical pyramidal neurons (hand drawing) and in vitro recorded spike [15].

Neurons are connected to each other via tree-like dendrites. Dendrites serve as input ports of a neuron. Axons play role on transmitting the signal generated by the soma to another neuron's dendrites, just like an electrical cable, forming the output port. The length of an axon can vary from 0.1 mm to meters [17].

The connection between dendrites and axons are formed by junctions called synapses. The cells, sending and receiving the signal are called presynaptic and postsynaptic neurons, respectively. A typical cortical neuron makes connection with 10^4 postsynaptic neurons. The most common type of a synapse is the chemical synapse. At a chemical synapse, anatomically, there does not occur a direct connection of axons and dendrites. Instead, there exist a tiny gap between pre-and postsynaptic cell membranes, called the synaptic cleft. When the electrical signal arrives at a synapse, it triggers a complex chain of biochemical processing. In the end, the chemical signal is translated into an electrical response again.

2.1.3 Basic Electrophysiology of Neurons

Electrical activity of a neuron occurs due to transfer of ionic currents through the membrane of that neuron. The basic charge carries responsible of the ionic current flows are sodium (Na^+), potassium (K^+), calcium (Ca^{2+}), or chloride (Cl^-). In the

inside and the outside of a cell, these ions exist with different concentrations resulting ionic gradients. These ionic gradients are the major forces driving neural activity. The extracellular medium has a high concentration of sodium and chloride ions like the salty seawater, and a relatively high concentration of calcium ions. The intracellular medium has high concentrations of potassium ions and different negatively charged molecules (denoted by A^-). Since the existing ion channels do not permit these ions to flow through and pass in the extracellular medium, they are trapped in the intracellular medium. The flows of sodium and calcium ions appears to be not very significant, at least at rest, while the flows of potassium and chloride ions are quite important. This, however, does not eliminate the concentration asymmetry for two reasons.

- Passive redistribution. The immobile anions A^- attract more K^+ into the cell and repel more Cl^- out of the cell, thereby creating concentration gradients.
- Active transport. Ions are pumped in and out of the cell via ionic pumps. For example, the Na^+-K_+ pump depicted Figure 2.2 in pumps out three Na^+ ions for every two K^+ ions pumped in, thereby maintaining concentration gradients.

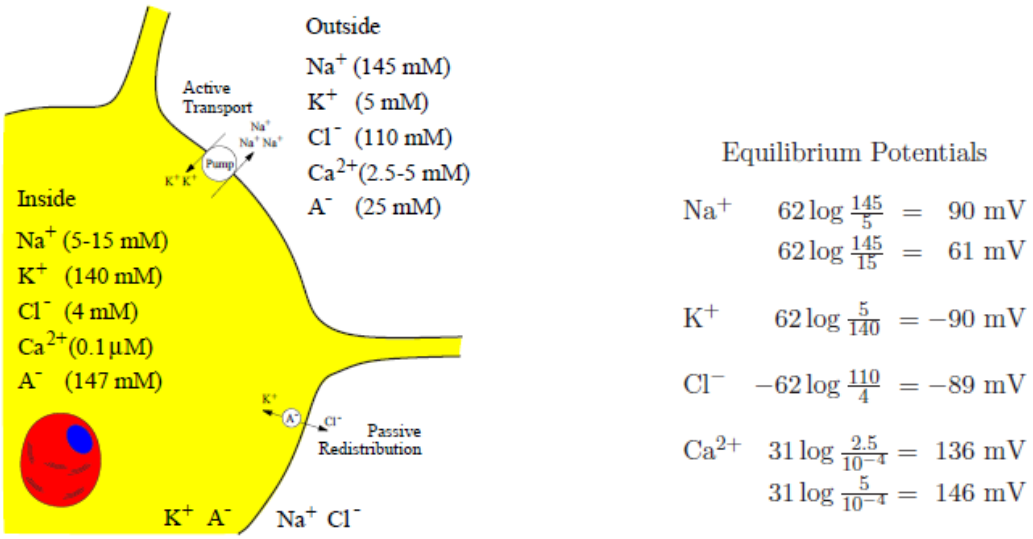

Figure 2.2 : Ion concentrations and Nernst equilibrium potentials in a typical mammalian neuron [15].

Concentration and electric potential gradients are the two forces that drive each ion species through the membrane channel. First, the ions diffuse down the concentration gradient. For example, the K^+ ions depicted in Figure 2.3 (a) diffuse out of the cell because K^+ concentration inside is higher than that outside.

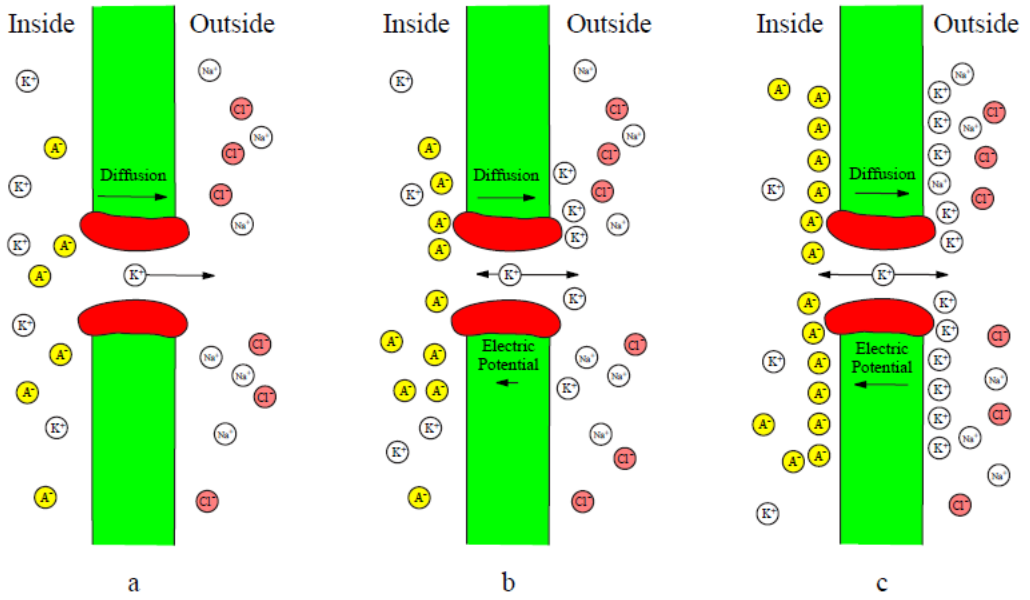

Figure 2.3 : (a) Diffusion of K+ ions down the concentration gradient through the membrane (b) creates an electric potential force pointing in the opposite direction (c) until the diffusion and electrical forces counter each other [15].

While exiting the cell, K^+ ions carry a positive charge and leave a net negative charge inside the cell (consisting mostly of impermeable anions A^-), thereby producing the outward current. The positive and negative charges accumulate on the opposite sides of the membrane surface, creating an electric potential gradient across the membrane that we call transmembrane potential or membrane voltage. This potential slows the diffusion of K^+, since K^+ ions are attracted to the negatively charged interior and repelled from the positively charged exterior of the membrane, as illustrated in Figure 2.3 (b). At some point, equilibrium is achieved. The concentration gradient and the electric potential gradient maintain equal and opposite forces that balance each other, and the net cross-membrane current is zero, as in Figure 2.3 (c). The value of such an equilibrium potential depends on the ionic species, and it is given by the Nernst equation:

$$E_{ion} = \frac{RT}{zF} ln \frac{[Ion]_{out}}{[Ion]_{in}} \qquad \textbf{(2.1)}$$

where $[Ion]_{in}$ and $[Ion]_{out}$ are concentrations of the ions inside and outside the cell, respectively; R is the universal gas constant T is temperature in degrees Kelvin; F is Faraday's constant z is the valence of the ion (z = 1 for Na^+ and K^+; z =-1 for Cl^-;

and z = 2 for Ca^{2+}). Substituting the numbers, taking $\log_{10}$ instead of natural ln and using body temperature T = 310°K (37°C) results in:

$$E_{ion} \approx 62log\frac{[Ion]_{out}}{[Ion]_{in}} \text{(mV)} \quad \textbf{(2.2)}$$

for monovalent (z = 1) ions. Figure 2.2 shows the equilibrium Nernst potential for different ionic species for a typical mammalian neuron.

2.1.4 Electrophysiological Model of Neurons

According to eq. (2.2), the definition of Nernst equilibrium potential, for instance for K^+, is denoted by E_K. When the membrane potential, let us say V, is equal to E_K, the net ionic current of K^+ is equal to zero. Otherwise, for a single ion, the current increases or decreases approximately linearly when the membrane potential deviates from the equilibrium potential value. We can define this behavior for any ion by the equation $I_i = g_i(V - E_i)$ where i denotes the ion type, g_i is the conductance for the related ion channel and $(V - E_i)$ is called as the driving force. Similarly, the total current of membrane flowing from inside to outside can be given as below.

$$I_M = \sum_i g_i(V - E_i) \quad \textbf{(2.3)}$$

When this total ionic is equal to zero, we say that the value of the membrane potential corresponds to the *resting membrane potential* defined by eq. (2.4) .

$$V_{rest} = \frac{g_{Na}E_{Na} + g_{Ca}E_{Ca} + g_K E_K + g_{Cl}E_{Cl}}{g_{Na} + g_{Ca} + g_K + g_{Cl}} \quad \textbf{(2.4)}$$

It is usually more convenient to represent electrical properties with an electrical circuit as given in Figure 2.4. In the figure, the membrane is traditionally modeled as a capacitor. By this way, the membrane current equation of a neuron is given by eq. (2.5).

$$I = C\dot{V} + I_{Na} + I_{Ca} + I_K + I_{Cl} \quad \textbf{(2.5)}$$

It rather more convenient to express this equation in a differential equation form explicitly as below.

$$C\dot{V} = I - g_{Na}(V - E_{Na}) - g_{Ca}(V - E_{Ca}) - g_K(V - |E_K|) - g_{Cl}(V - |E_{Cl}|) \quad \textbf{(2.6)}$$

In eq. 2.6, when the conductances are constant, the current is said to be *ohmic*. In general, ionic currents in neurons are not ohmic, since the conductances may depend on time, membrane potential, and pharmacological agents, e.g., neurotransmitters, neuromodulators, second-messengers, etc. The time-dependent variation in conductances allows a neuron to generate an action potential, or spike. Therefore, conductances should also play an important role.

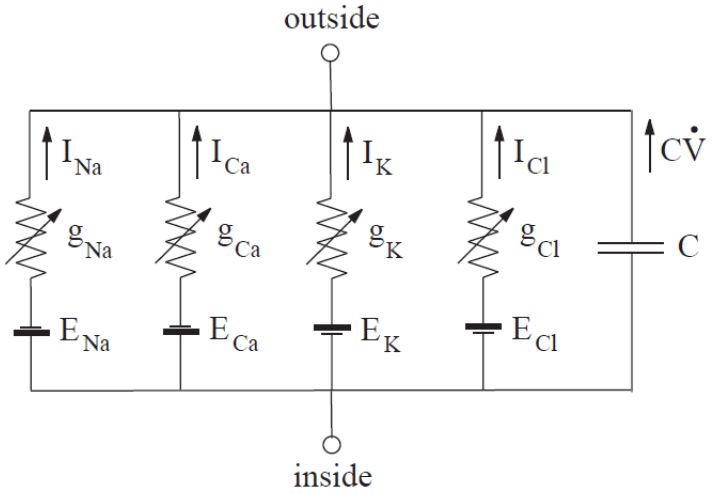

Figure 2.4 : Equivalent representation of a cell membrane [15].

2.1.5 Conductances

Electrical conductances of the ion channels are controlled by gates. These channels are called voltage-gated channels. These gates can activate (open) or inactivate (close) the channels (depicted in Figure 2.5) depending on the membrane voltage value. Hence, an ionic current can be redefined by eq. (2.7).

$$I = \bar{g}p(V - E) \quad \textbf{(2.7)}$$

where $\bar{g}$ is the maximal conductance, p is the average proportion of channels in the open state and E is the reversal potential. Hodgkin and Huxley defined the probability of an activation gate being in the open state by the variable m (sometimes the variable n is used for K^+ and Cl^- channels) and the probability of an inactivation gate being in the open state is denoted by the variable h. The proportion of open channels in a large population is,

$$p = m^a h^b \tag{2.8}$$

where a is the number of activation gates and b is the number of inactivation gates per channel.

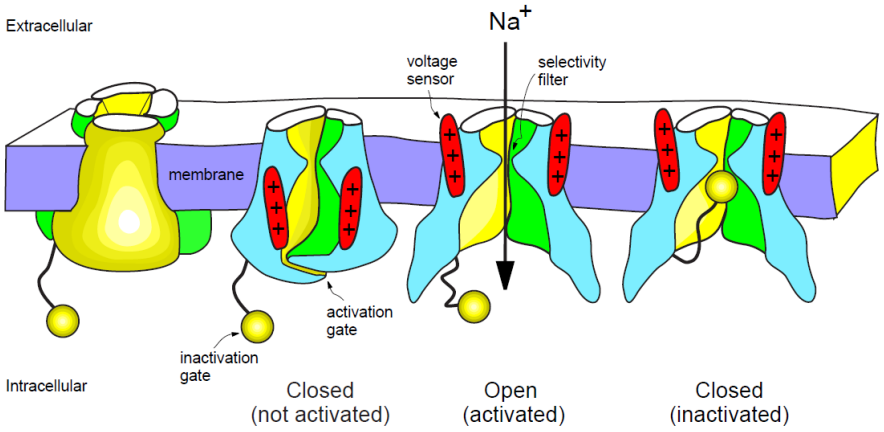

Figure 2.5 : Structure of voltage-gated channels [15].

Some channels do not have inactivation gates (b = 0), hence $p = m^a$. Such channels do not inactivate, and they result in persistent currents. In contrast, channels that do inactivate result in transient currents.

The dynamics of the activation variable m is classically described by a general first order differential equation:

$$\frac{dm}{dt} = \frac{m_\infty(V) - m}{\tau(V)} \tag{2.9}$$

where $m_\infty(V)$ is called the steady-state activation function, and τ (V) is the activation time constant. These two functions can be measured experimentally. The activation function has a sigmoidal characteristics and the time constant has a unimodal shape (see Figure 2.6). Similarly, the inactivation variable h is described by a first order differential equation:

$$\frac{dh}{dt} = \frac{h_\infty(V) - h}{\tau(V)} \tag{2.10}$$

where $h_\infty(V)$ is called the steady-state inactivation function, and $\tau(V)$ is the inactivation time constant. These functions are depicted in Figure 2.6.

2.1.6 The Hodgkin-Huxley Neuron Model

One of the most important models in computational neuroscience is the Hodgkin-Huxley model of the squid giant axon. Using pioneering experimental techniques of that time, Hodgkin and Huxley (in 1952) determined that the squid axon carries three major currents: voltage-gated persistent K^+ current with four activation gates, voltage gated transient Na^+ current with three activation gates and one inactivation, and ohmic leak current, I_L, which is carried mostly by Cl^- ions. The complete set of space-clamped Hodgkin-Huxley equations is:

$$C\frac{dV}{dt} = I - g_{Na}m^3h(V - V_{Na}) - g_K n^4(V - V_K) - g_L(V - V_L)$$

$$\frac{dm}{dt} = a_m(V)(1-m) - b_m(V)m$$

$$\frac{dh}{dt} = a_h(V)(1-h) - b_h(V)h \qquad \textbf{(2.11)}$$

$$\frac{dn}{dt} = a_n(V)(1-n) - b_n(V)n$$

where

$$a_m(V) = 0.1\frac{(V+40)}{1-e^{\frac{-(V+40)}{10}}}$$

$$a_h(V) = 0.07e^{\frac{-(V-35)}{20}}$$

$$a_n(V) = 0.1\frac{(V+55)}{1-e^{\frac{-(V+55)}{10}}} \qquad \textbf{(2.12)}$$

$$b_m(V) = 4e^{\frac{-(V+65)}{18}}$$

$$b_h(V) = \frac{1}{1+e^{\frac{-(V+35)}{10}}}$$

$$b_n(V) = 0.125e^{\frac{-(V+65)}{80}}$$

These parameters, provided in the original Hodgkin and Huxley paper [15], correspond to the membrane potential shifted by approximately 65 mV, so that the resting potential is at V ≈ 0. The Nernst potentials and typical maximal conductance values are,

V_K = -12 mV, V_{Na} = 115 mV, V_L = 10.6 mV; $\overline{g_K} = 36$, $\overline{g_{Na}} = 120$, $g_L = 0.3$.

The functions α(V) and β(V) describe the transition rates between open and closed states of the channels. However, it is convenient to represent these rates in a standard form as below $(x = m, n, h)$:

$$\dot{x} = \frac{x_\infty(V) - x}{\tau_x(V)} \tag{2.13}$$

where

$$x_\infty = \alpha_x/(\alpha_x + \beta_x)$$
$$\tau_x = 1/(\alpha_x + \beta_x) \tag{2.14}$$

as depicted in Figure 2.6. Furthermore, these sigmoidal and unimodal functions are usually approximated by the Boltzmann and Gaussian functions [15].

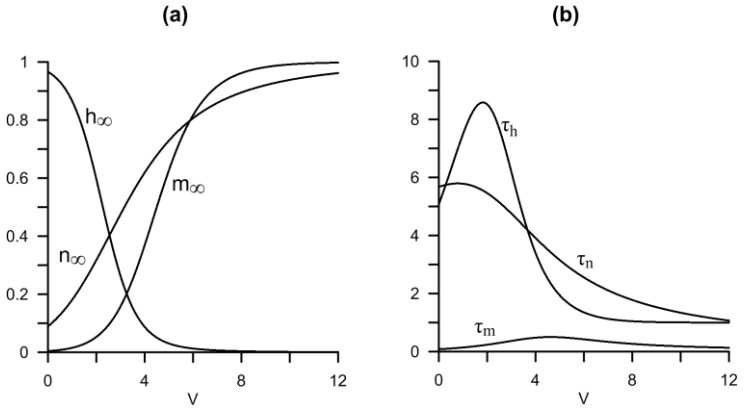

Figure 2.6 : Steady-state (in)activation functions (left) and voltage-dependent time constants (right) in the Hodgkin-Huxley model.

2.1.6.1 The Action Potential of the Hodgkin-Huxley Neuron Model

A detailed spike shape with an input current is given in

Figure 2.7. An input current is applied to the neuron at time 2 ms and a small increase called *depolarization* occurs. Then the neuron turns back to resting state as called *repolarization*. When a strong input pulse arrives, a sharp rise occurs and the

neuron elicits a spike. Since the time constants, τ_n and τ_h are large, variables *n* and *h* are slow. Therefore, membrane potential value goes below V_{rest}, a phenomenon known as *afterhyperpolarization*. In addition, variable *h* is still at small values, which makes the neuron insensitive to the inputs. Thus, a phase called *absolute refractory* occurs and the neuron cannot generate a second spike. After a while, the value of h gets bigger and the neuron becomes able to generate a spike, if the stimulus is relatively strong. This phase is called *relative refractory*.

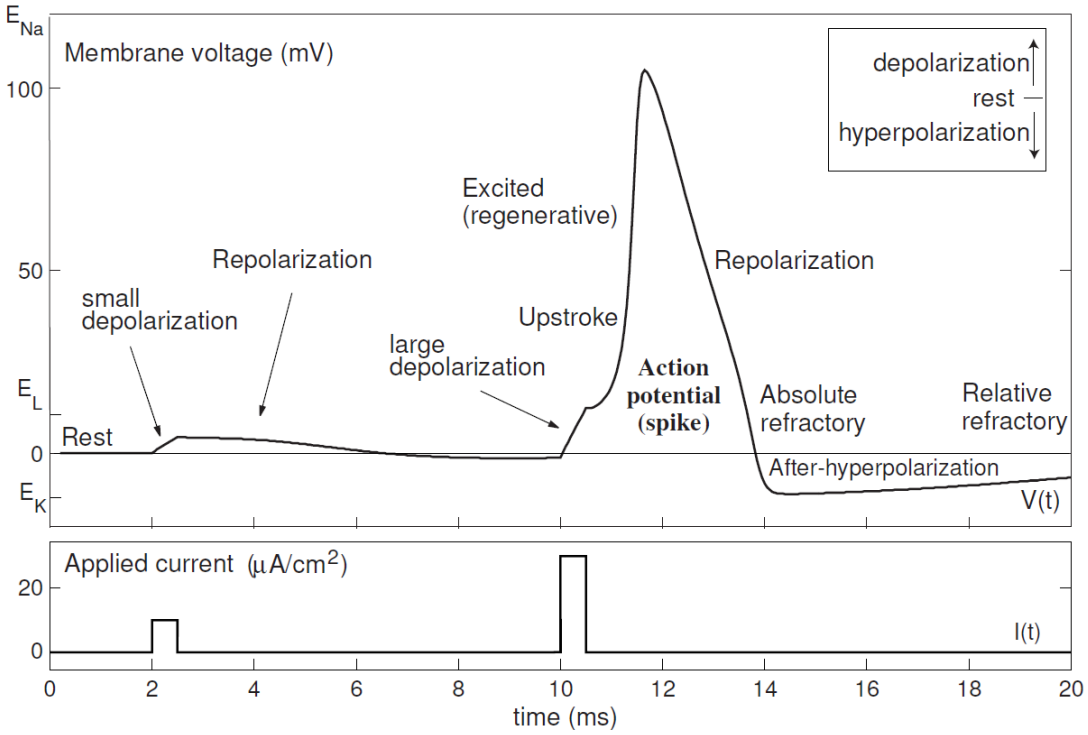

Figure 2.7 : Action potential in the Hodgkin-Huxley model [15].

2.2 Neuron Dynamics

Neurons are dynamical systems. Therefore, knowledge of dynamical systems makes it easy to deal with neuron model implementations. For this reason, some brief explanations about dynamical systems are presented in this part.

2.2.1 Dynamical Systems

A *dynamical system* consists of a set of variables that describe its state and a law that describes the evolution of the state variables with time. The evolution laws are usually ordinary differential equations in neuroscience. Let us consider a two dimensional system as given below.

$$\dot{x} = f(x, y)$$
$$\dot{y} = g(x, y) \quad \textbf{(2.15)}$$

Where f and g describe the evolution law of the sate variables x(t) and y(t). The equations $f(x, y) = 0$ define *x-nullcline* and $g(x, y) = 0$ define *y-nullcline*. The intersection points of the nullclines give *equilibrium points* or *fixed points*. When the system is at equilibrium, it means that there is no motion since $\dot{x} = \dot{y} = 0$.

The coordinates system, where the axis are x and y (state variables) are called *phase plane*. A solution curve on the phase plane is called *trajectory*.

An equilibrium is *stable* if any trajectory starting sufficiently close to the equilibrium remains near it for all $t \geq 0$. If, in addition, all such trajectories converge to the equilibrium as $t \to \infty$, the equilibrium is *asymptotically stable*. An equilibrium is called *unstable*, if it is not stable. For instability, it suffices to have at least one trajectory that diverges from the equilibrium no matter how close the initial condition is to the equilibrium. There are three major types of equilibriums. The equilibrium point is a;

Node when the eigenvalues are real and of the same sign. The node is stable when the eigenvalues are negative and unstable when they are positive.

Saddle when the eigenvalues are real and of opposite signs. Saddles are always unstable, since one of the eigenvalues is always positive.

Focus when the eigenvalues are complex conjugate. Foci are stable when the eigenvalues have negative real parts, and unstable when the eigenvalues have positive real parts.

The phase plane depicting equilibrium points and all possible trajectories is called *phase portrait*. Phase portrait is a very useful tool for investigating qualitative properties of dynamical systems. In a phase portrait, stable points are usually shown with filled circles where unstable points are shown with empty circles.

When two systems are qualitatively equivalent, they are said to be *topologically equivalent*. An example of topological equivalence for two one-dimensional systems ($\dot{V} = F(V)$) is given in Figure 2.8.

The final and most advanced step in the qualitative analysis of any dynamical system is the bifurcation analysis. In general, a system is said to undergo a *bifurcation* when its phase portrait changes qualitatively. According to [15], although there are millions of different electrophysiological mechanisms of spiking, there only four type of bifurcations in neuron systems. These bifurcation types are summarized below.

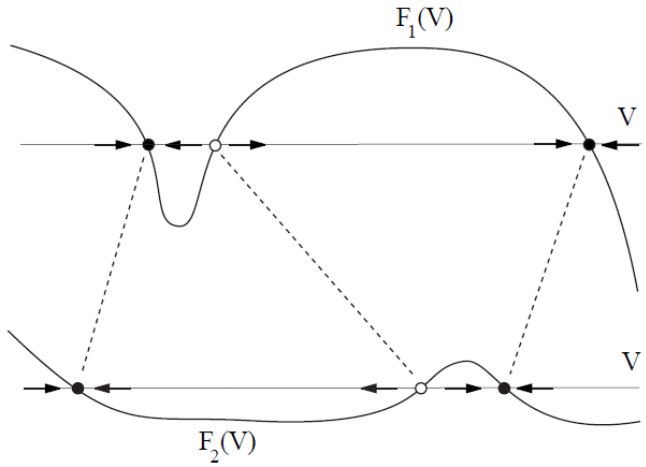

Figure 2.8 : Two topologically equivalent systems [15].

Saddle-node bifurcation: As the magnitude of the bifurcation parameter changes, a stable equilibrium corresponding to the resting state (black circle marked "node" in Figure 2.9 (a)) is approached by an unstable equilibrium (white circle marked "saddle"); they coalesce and annihilate each other, as in Figure 2.9 (a) (middle). Since the resting state no longer exists, the trajectory describing the evolution of the system jumps to the limit cycle attractor, indicating that the neuron starts to fire tonic spikes.

Saddle-node on invariant circle bifurcation: It is similar to the saddle-node bifurcation except that there is an invariant circle at the moment of bifurcation, which then becomes a limit cycle attractor, as in Figure 2.9 (b).

Subcritical Andronov-Hopf bifurcation: A small unstable limit cycle shrinks to a stable equilibrium and makes it lose stability, as in Figure 2.9 (c). Because of instabilities, the trajectory diverges from the equilibrium and approaches large amplitude spiking limit cycle or some other attractor.

Supercritical Andronov-Hopf bifurcation: The stable equilibrium loses stability and gives birth to a small-amplitude limit cycle attractor, as in Figure 2.9 (d). As the

magnitude of the bifurcation parameter changes, the amplitude of the limit cycle increases and it becomes a full-size spiking limit cycle. These four bifurcations for a spiking neuron behavior are given in Figure 2.9. The ramp input current is the bifurcation parameter here.

There is a basic difference between saddle-node and Andronov-Hopf bifurcations. Systems undergoing Andronov-Hopf bifurcations, whether subcritical or supercritical, exhibit damped oscillations of membrane potential, whereas systems near saddle-node bifurcations, whether on or off an invariant circle, do not.

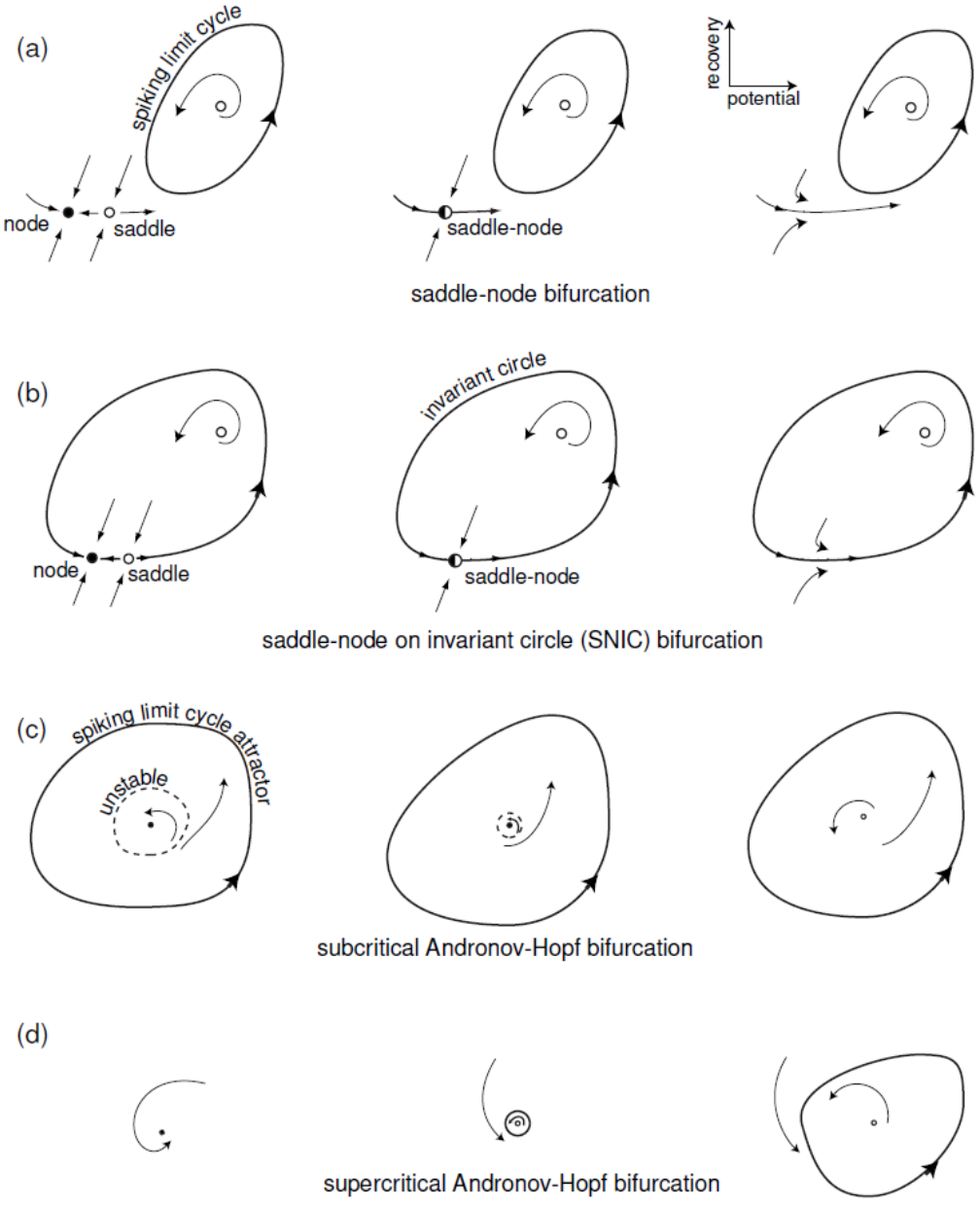

Figure 2.9 : Four bifurcations of an equilibrium state leading to the transition from resting to periodic spiking behavior in neurons [15].

There exist commonly used classifications of neurons:

Neurons with damped subthreshold oscillations referred as *resonators* and those that do not have this property as *integrators*.

Neurons spiking with arbitrarily low frequency, depending on the strength of the applied current, depicts *Class I* behavior.

Neurons spiking in a certain frequency band that is relatively insensitive to changes in the strength of the applied current depicts *Class II* behavior.

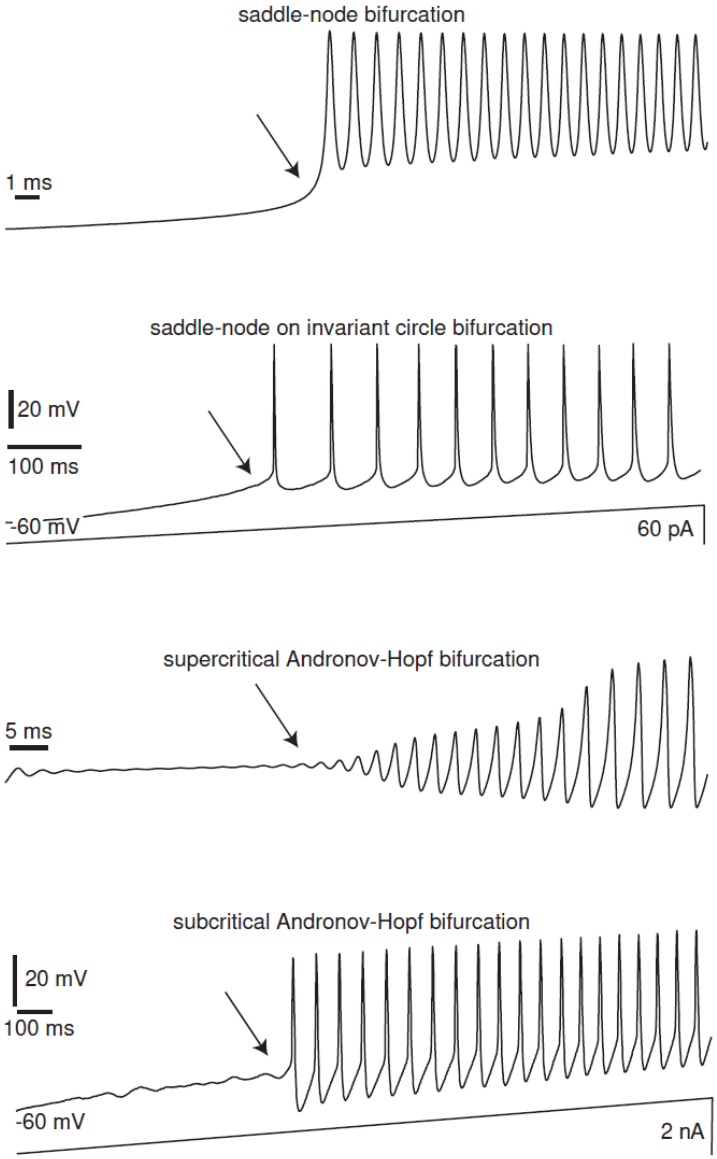

Figure 2.10 : Transitions from resting to tonic (periodic) spiking occur via bifurcations of equilibrium (marked by arrows) [15].

2.3 Neuron Models

The Hodgkin-Huxley model is the most accepted electrophysiological neuron model that made the inventors won the Nobel Prize. However, its high complexity and dimensionality, which prevent from analytical studies and efficient simulations, is the main drawback of the model. Therefore, different reduced models and simple models have been presented. To make a comparison between the models, we first introduce Figure 2.11, which shows 20 possible behaviors of a cortical neuron and then, count the number of behaviors each neuron model can exhibit.

2.3.1 Integrate and Fire (I&F) Neuron Model

One of the most widely used models in computational neuroscience is the Integrate and Fire (I&F) neuron model. This model is also called Leaky I&F. The origin of the model goes back to 1907 [20]. The defining equation of the model is given by eq. (2.16).

$$\frac{dv}{dt} = I + a - bv$$
$$v = v_{reset}, \quad v \geq_{vthresh} \tag{2.16}$$

According to the model, when the variable v reaches the peak value v_{thresh}, a spike is assumed to be fired and the variable v is reset to v_{reset} value. From engineering point of view, the equation set corresponds to a parallel RC circuit driven by a constant current. The model is electronically very simple but a very poor choice for a large-scale VLSI network design because of limited dynamical behavior. It can exhibit sub-figures A, G and L of Figure 2.11.

2.3.2 Quadratic Integrate and Fire (QI&F) Neuron Model

This model is an alternative model to I&F. It is also called the *Theta Neuron* model. It is simplest neuron model that can generate a spike itself and has a canonical form of saddle-node bifurcation with a quadratic nonlinearity. The equation set is as given in eq. (2.17). This model can exhibit sub-figures A, G, I, L, O and P of Figure 2.11.

$$\frac{dv}{dt} = I + a(v - v_{rest})(v - v_{thresh})$$
$$v = v_{reset}, \quad v = v_{peak} \tag{2.17}$$

2.3.3 FitzHugh-Nagumo (FN) Neuron Model

This two variable model is a reduced form of the Hodgkin-Huxley model using phase plane analysis for the first time. FitzHugh first suggested the model in 1961 and Nagumo designed a circuit of the model in 1962.

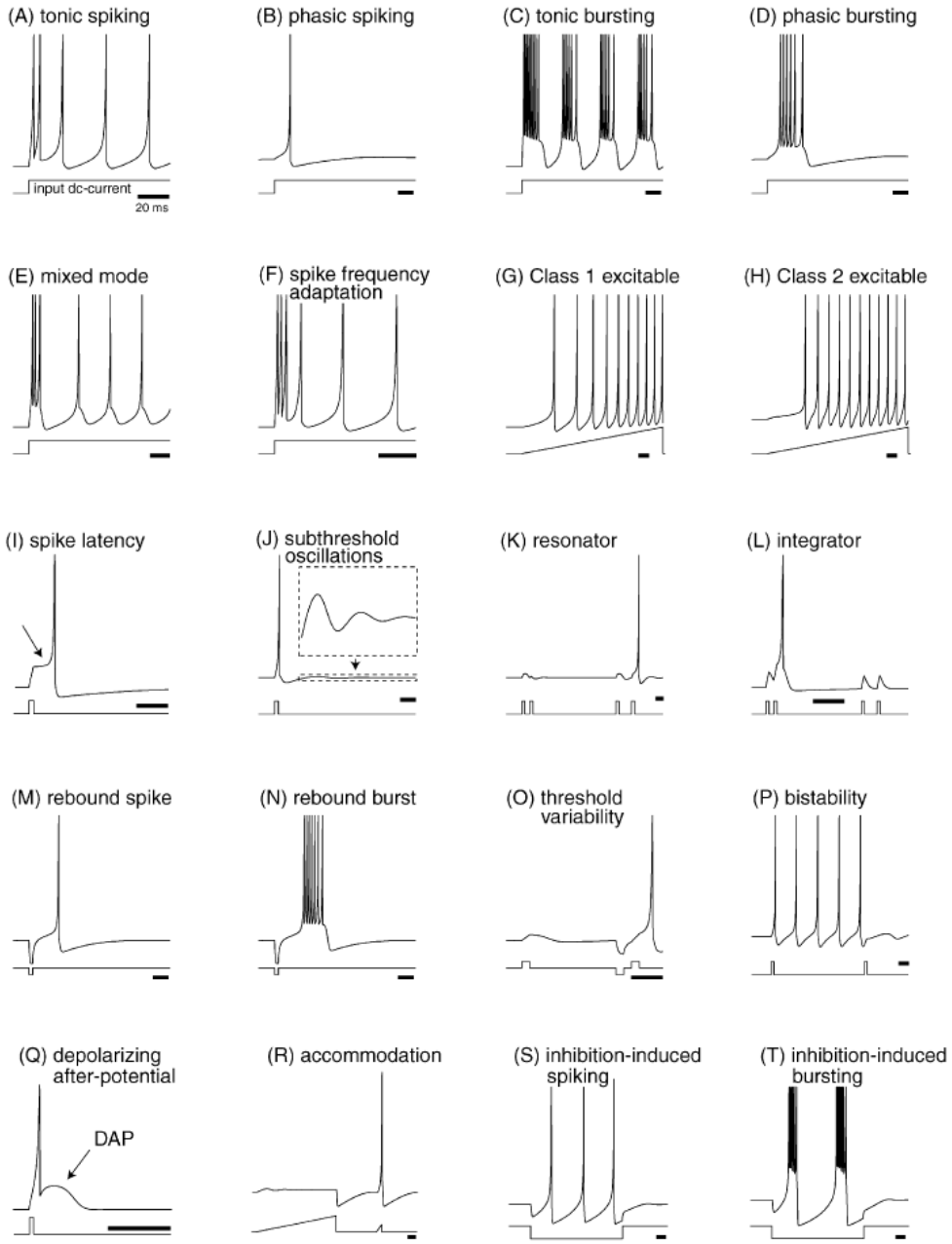

Figure 2.11 : Summary of the neuro-computational properties of biological spiking neurons [19].

The system includes a cubic nonlinearity. The nullclines are shown in Figure 2.12. The equation set is as given by eq. (2.18) [21].

$$\dot{v} = v - \frac{v^3}{3} - w + I$$
$$\dot{w} = 0.08(v + 0.7 - 0.8w) \tag{2.18}$$

This model can exhibit sub-figures A, B, G, I, J, K, M, O, P, R, and S of Figure 2.11.

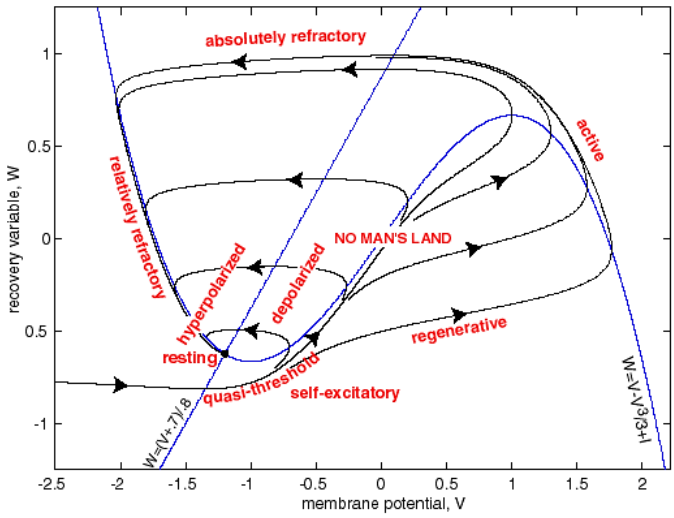

Figure 2.12 : Phase portrait of FitzHugh-Nagumo model [21].

2.3.4 Hindmarsh-Rose (HR) Neuron Model

Realizing that some variables can be replaced with constants, Hindmarsh and Rose offered a reduced version of the Hodgkin-Huxley model in 1982. Since the model has a very rich dynamics, it has been a source of interest for engineers. The model includes both cubic and quadratic nonlinearity. However, it is a difficult task to determine the proper parameter set for all kind of cortical behaviors. The equation set is as given by eq. (2.19) [23].

$$\frac{dx}{dt} = y - x^3 + 3x^2 - z + I$$
$$\frac{dy}{dt} = 1 - 5x^2 - y \tag{2.19}$$
$$\frac{dz}{dt} = r(s(x - x_1) - z)$$

This model can exhibit all of the sub-figures of Figure 2.11 theoretically.

2.3.5 Izhikevich (Izh) Neuron Model

In 2003, Izhikevich introduced a very simple model that can exhibit the dynamics of the Hodgkin-Huxley model with the simplicity of two equations and four parameters. Thus, the model became quite popular for simulating and realizing large-scale networks. The equation set is given by eq. (2.20) [23]. This model can exhibit all of the sub-figures of Figure 2.11. The parameter set can be found in [23]. An excellent review of the model with phase plane analysis [15] provides convenience for a circuit designing engineer.

$$\begin{aligned} \dot{v} &= 0.04v^2 + 5v + 140 - u + I_{in} \\ \dot{u} &= a(bv - u) \\ if\ v \geq v_{peak}, v &\leftarrow c, u \leftarrow u + d \end{aligned} \tag{2.20}$$

The drawback of the models is that, the spiking behavior (timing) may change according to the value of v_{peak} (spike cut-off value) parameter [24]. Therefore a careful design should be done. In fact, Izhikevich reported a solution for this problem [25] but it is a non-trivial solution in terms of circuit implementation. Nevertheless, a low power and compact VLSI implementation of this model is given in chapter 4.

2.3.6 Adaptive Exponential Integrate and Fire (AdEx) Neuron Model

Similar to Izh model, a simple but dynamically rich model is the AdEx neuron model introduced in 2005 [26]. The difference between the Izh model and this model is that, the quadratic term is replaced with and exponential term. The equation set is as given by eq. (2.21).

$$\begin{aligned} C\frac{dV}{dt} &= -g_L(V - E_L) + g_L\Delta_T\, exp\left(\frac{V - V_T}{\Delta_T}\right) - w + I_{in} \\ \tau_w\frac{dw}{dt} &= a(V - E_L) - w \\ if\ V > V_{peak}, &\qquad V \rightarrow V_r, \qquad w \rightarrow w + b \end{aligned} \tag{2.21}$$

This model can exhibit all of the sub-figures of Figure 2.11. A set of firing patterns, also shown in phase plane, are given in Figure 2.13.

The advantage of the model is that there is no spike cut-off value sensitivity. This model also matches with direct measurement results better in terms of subthreshold

behavior [28]. A helpful review of the model can be found in [27, 29, 30]. A VLSI implementation of this model is given in chapter 4.

There exist some other useful models in the literature: Resonate&Fire Model [31], Morris-Lecar Model [32] and Spike Response Model [17]. These models are not presented here but plenty of information exists in the literature.

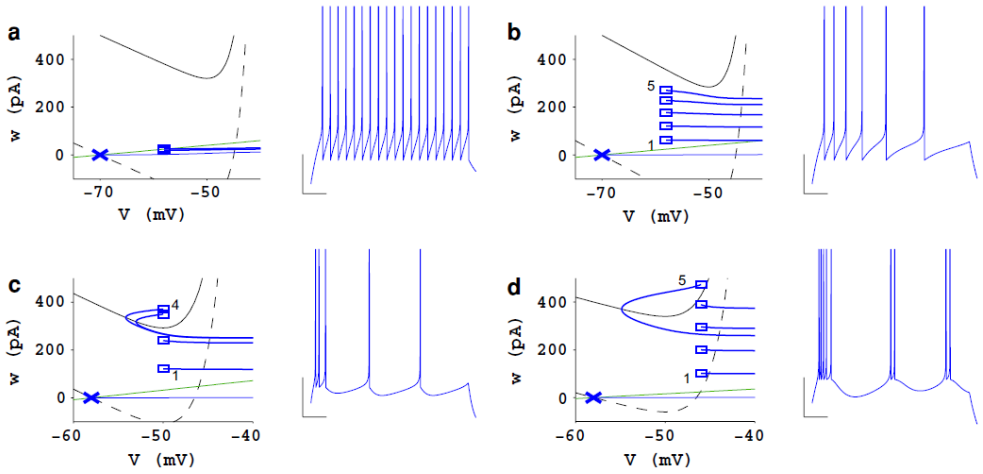

Figure 2.13 : Phase plane representation of four firing patterns. Firing patterns observed during a step current stimulation are: (a) tonic spiking, (b) adaptation, (c) initial burst, (d) regular bursting [27].

3. LOW POWER CMOS CIRCUIT BLOCKS

In this chapter, we firstly introduce some basic concepts of circuit design used in neuromorphic engineering. Secondly, we present a wide temperature range, CMOS only current reference circuit. Then a current mode, wide range input exponential circuit is introduced. Lastly, we mention about similar low power and compact neurons in the literature.

3.1 Subthreshold Operation

Digital circuits dominate today's integrated circuit technology, which employ MOSFETs as switching elements. Analog circuits comprise a small part of the designs and even a smaller part of these designs employs MOSFETs in subthreshold domain where neuromorphic circuits are among these examples.

A transistor is said to operate in subthreshold (weak inversion) region when the gate-source voltage is below the threshold voltage. In this region, the relationship between drain current and gate voltage is an exponential form rather than the square law. Additionally, the current flowing through the transistor varies from femtoamperes to a few nanoamperes. The subthreshold current for a (NMOS) transistor is given by:

$$I_D = rI_o \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right) \exp\left(\frac{(n-1)V_{BS}}{nV_T}\right) \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad \textbf{(3.1)}$$

$$I_o = \mu C_{ox} (n-1) {V_T}^2 \quad \textbf{(3.2)}$$

where r is the aspect ratio, μ is the carrier mobility, C_{ox} is the gate-oxide capacitance, V_T is the thermal voltage, V_{TH} is the threshold voltage, $n \approx 1.2$ is the subthreshold slope factor [33]. For $V_{DS} > 0.1V$, by merging the second exponential term in eq. (3.1) with I_o, we can obtain a simple equation given in eq. (3.3).

$$I_D = rI_S \exp\left(\frac{V_{GS}}{nV_T}\right) \quad \textbf{(3.3)}$$

3.2 Basic Building Blocks

The bottom limit of current for a transistor is its reverse diode leakage current. A typical value for 0.15 μm process is around 0.1 fA. However, ion implantation in order to lower the threshold value increases the leakage current seriously, up to a few pA for the worst case. To make use of the complete current range, one can apply source-shifting technique [34]. According to the simulation data of typical values, for instance, $I_S = 200$ fA for $V_S = 0$ V and $I_S = 4$ fA for $V_S = 300$ mV for an NMOS device with $W = L = 450$ nm. Another applied method is to shift gate voltage below the source voltage. Both source and gate shifting effects can also be deduced from eq. (3.1).

For a low power design, the transistor should be able to handle fA current levels at a few ten of Hz frequency. Therefore, we make use of source shifting and active diode connection techniques in our neuron circuits. To be clear, a useful way of comparison done for current mode circuits is made between classical (CM), source shifted (SSCM) and active diode connected (ACM) current mirrors that are shown in Figure 3.1. The source shifting amount is $V_{sn} = 300$ mV and $W = L = 450$ nm. The buffer Figure 3.1 (c) is indeed a simple differential pair with an unbalanced input pair in order to create an offset voltage between drain and source terminals of the input transistor to improve DC behavior [34]. The buffer is supplied by a 10 pA bias current.

DC worst-case analysis results of the current mirrors are given in Figure 3.2. The x-axis is input current swept from 10 aA to 100 pA and y-axis is the output current. It is obvious that active diode connection together with source shifting definitely improves the DC behavior. On the other hand, AC worst-case analysis results are given for a 25 fA DC input current in Figure 3.3. Since CM topology is eliminated due to its very large DC gain error, we have only compared SSCM and ACM topologies. The AC bandwidth improvement (bandwidth is doubled) of ACM with respect to SSCM, while the DC input current is 25 fA, can be clearly seen from the simulation results given in Figure 3.3. In fact, an alternative topology exist in [34] utilizing a high-gain opamp. However, this topology is inconvenient for our future designs because of the high biasing currents of the opamp resulting in high power consumption.

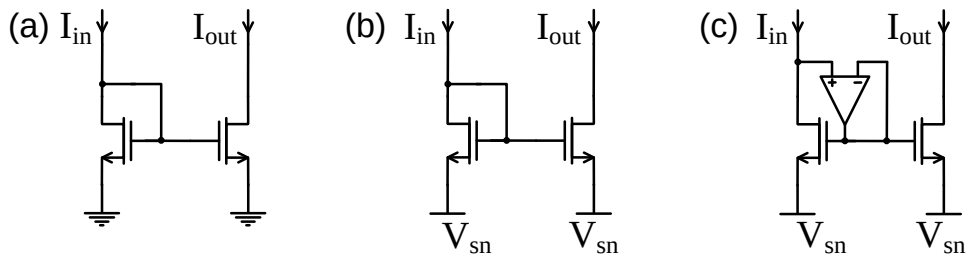

Figure 3.1 : Current mirror topologies: (a) classical, (b) source shifted, (c) active diode connected.

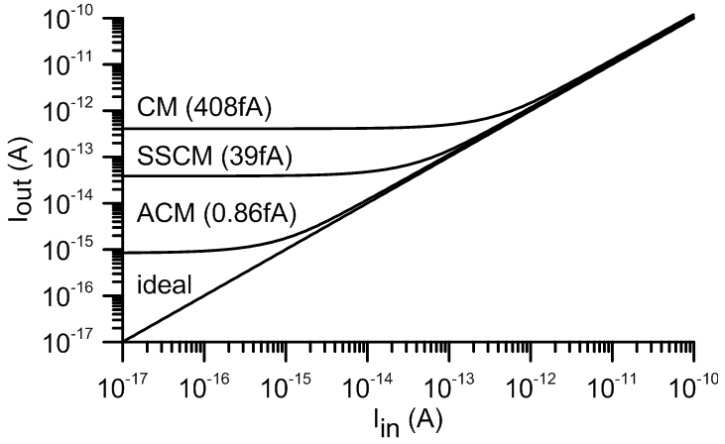

Figure 3.2 : DC worst case analysis results.

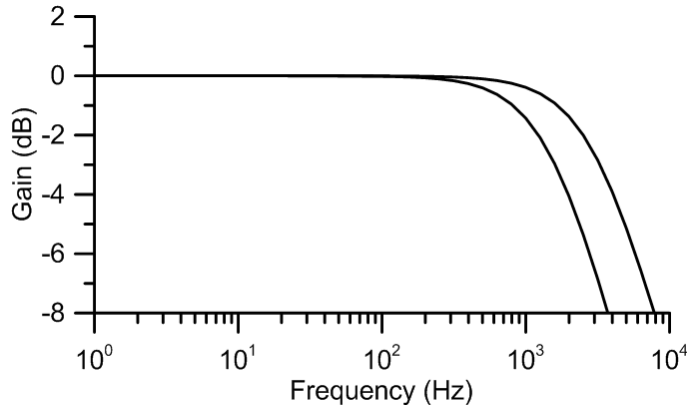

Figure 3.3 : AC worst case analysis results.

Another useful circuit block employed in neuromorphic circuits are log domain integrators, which is also the fundamental part of our neuron and synapse circuits. A first order log domain filter circuit is given in Figure 3.4.

Using translinear principle, one can easily show that the state equation of the log domain filter is given by eq. (3.4),

$$C\frac{dI_{out}}{dt} = -I_{out}(\alpha I_d) + I_{in}(\alpha I_b)(r_2 r_4 / r_1 r_3) \quad \textbf{(3.4)}$$

where r_1-r_4 are the aspect ratios of M_1-M_4 respectively and $\alpha = \frac{1}{nV_T} \cong 32$.

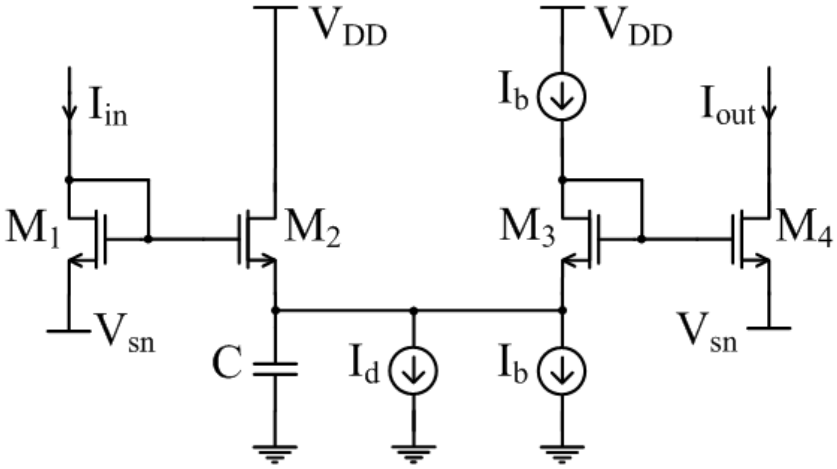

Figure 3.4 : Log domain integrator.

Another useful circuit block is, by excluding the capacitor in Figure 3.4, the translinear loop current multiplier/divider circuit. Using translinear principle again, the equation of this circuit appears as follows:

$$I_{out} = \frac{I_{in} I_b}{I_d} \quad \textbf{(3.5)}$$

3.3 A Low ppm/°C CMOS Only Temperature Compensated Current Reference

Due to large time constants, circuits operating at low frequencies usually employ large value capacitors. On the other side, our main strategy is to obtain compact circuits for massively large networks. It was mentioned in the previous part that log domain filters comprise the main block of the neuron and synapse circuits. Therefore, after checking eq. (3.4) again, we notice that in order to scale down the value of the capacitor, we have to scale down both of the currents I_d and I_b. Hence, we prefer fA level (I_d and I_b) DC current sources to reduce the capacitor value as much as possible.

On the other hand, temperature dependency is a very common problem of circuits based on subthreshold operation. Therefore, the dependence of bias currents with temperature should be as low as possible in a reasonable temperature range. To

generate a fA level bias current source, utilizing (a few hundreds of) nA level master current source, using current splitter circuits is not reasonable because splitter circuits introduce temperature dependency at each step of current dividing. Therefore, the master current source itself should generate at least a few nA or less currents. For this reason, we designed a pA level bias current reference with very low temperature dependency over a wide range. Furthermore, a simplified current divider circuit, rather than the mostly used M2M ladder (see Figure 3.12), is used to show that one can obtain fA level bias currents within a reasonable temperature range.

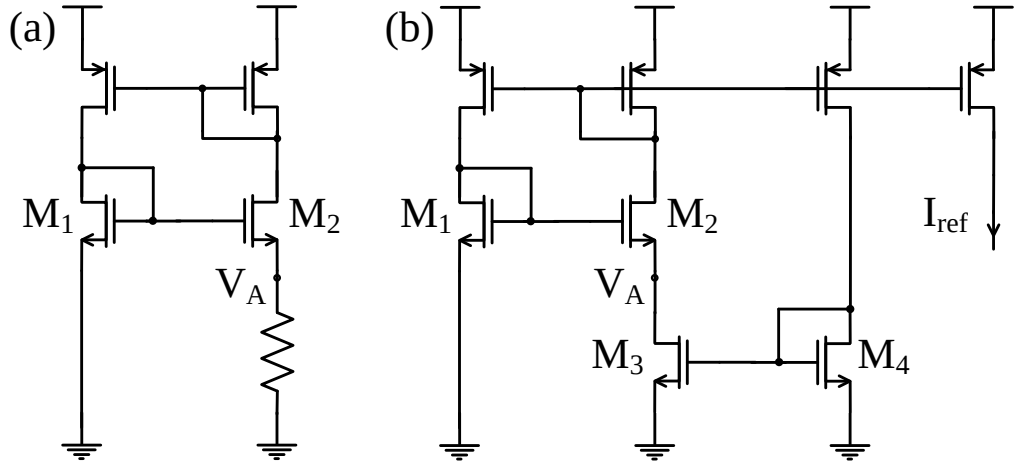

Figure 3.5 : (a) Conventional PTAT current source (b) Resistorless version of the circuit in (a).

A traditional PTAT (proportional to absolute temperature) current source is Figure 3.5 (a). Here, both M_1 and M_2, so called the core transistors, operate in subthreshold region with an i-v relationship given in eq. (3.3). The reference current flowing through the resistor can be given by the eq. (3.6).

$$I_{ref} = \frac{nV_T \ln(r_2/r_1)}{R} = \frac{V_A}{R} \tag{3.6}$$

To simplify the notation, we denote $V_A = nV_T \ln(r_2/r_1)$ (valid for the rest of circuits in this part) which is also equal to source voltage of M_2. Choosing $R = 1$ MΩ gives approximately $I_{ref} = 100$ nA with a temperature coefficient (TC) around 3000 ppm/°C. Therefore, this basic circuit is not a solution for a low temperature sensitivity design.

A resistorless version of this circuit is presented by [35] that is shown in Figure 3.5 (b). In the circuit, M_3 and M_4 operate in strong inversion while M_3 is in triode and M_4

is in saturation region. I_3 and I_4 is given by eq. (3.7) where V_A is the V_{DS} voltage of M_3 and V_{GS} denotes gate-source voltage of M_3 and M_4.

$$I_3 = r_3 \mu C_{ox}(V_{GS} - V_{th})V_A$$
$$I_4 = \frac{1}{2} r_4 \mu C_{ox}(V_{GS} - V_{th})^2 \quad \textbf{(3.7)}$$

Here the designer can determine the ratio I_3/I_4=M by adjusting the current mirror gain. Solving these equations together gives I_{ref} and V_G=V_{GS} as below.

$$I_{ref} = r_3 \mu C_{ox} {V_A}^2 \left(\frac{r_3}{r_4} M - 0.5 + \sqrt{\frac{r_3}{r_4} M (\frac{r_3}{r_4} M - 1)} \right) \quad \textbf{(3.8)}$$

$$V_G = V_{th} + V_A \left(\frac{r_3}{r_4} M + \sqrt{\frac{r_3}{r_4} M (\frac{r_3}{r_4} M - 1)} \right) \quad \textbf{(3.9)}$$

The first order definition of temperature dependent parameters, μ, V_T and V_{th} are expressed as,

$$V_{th} = V_{th0} - \kappa T \quad \textbf{(3.10)}$$

$$V_T = \frac{k}{q} T \quad \textbf{(3.11)}$$

$$\mu = \mu_0 \left(\frac{T}{T_0} \right)^{-m} \quad \textbf{(3.12)}$$

where, V_{th0} is the 0 K (zero Kelvin) threshold voltage, κ is the TC of V_{th}, k is the Boltzmann constant, q is the electron charge, μ_0 is the mobility at T_0 K and m is the mobility temperature exponent with an approximate value of 1.5. Thus, TC of I_{ref} is as follows:

$$TC = \frac{1}{I_{ref}} \frac{dI_{ref}}{dT} = \frac{2 - m}{T} \quad \textbf{(3.13)}$$

However, for this design, I_{ref} value is still around a few hundreds of nA with a TC value of 2000 ppm/°C. Hence, this circuit is also inadequate for a low TC current reference circuit.

The key point of this and most other designs [36-40] is the dependency of I_{ref} to V_A. The I_{ref} expressions are usually in the form of "$\mu V_A{}^2$" as in eq. (3.8) where the rest of parameters are related to transistor dimensions and hence temperature independent. Therefore, it is expected to have similar TC values as derived in eq. (3.13). In another reference current circuit design [41], a different topology is preferred in order to change the multiplier of "$\mu V_A{}^2$" term to lower the reference current value. Some other works introduce multi-threshold process [42] in order to alter the TC expression in eq. (3.13), which is an expensive solution.

A useful idea is introduce an offset to the voltage term V_A. For instance, while V_A has a form of $\alpha_1 T$ as in eq. (3.6), introducing an offset voltage results in a form of $\alpha_2 T + \beta$. By this way, a new TC equation is reached [43] that can be made closer to zero. A method to introduce an offset parameter may be to make use of an offset generating circuit as in [43] that is shown in Figure 3.6. The source terminal of M_1 in Figure 3.5 is connected to the nodes either V_{D1} or V_{D2} (to generate different offset values) resulting in a new V_A voltage and TC value as given in eq. (3.14) and (3.15). In other words, the current of the core transistor M_1 is injected to an internal node of a transistor ladder.

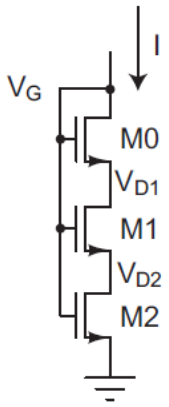

Figure 3.6 : Offset generating MOS resistor ladder circuit.

$$V_A = \alpha T + \beta \qquad \textbf{(3.14)}$$

$$TC = \frac{1}{I_{ref}} \frac{dI_{ref}}{dT} = \frac{1-m}{T} + \frac{1}{T + {}^{\beta}/_{\alpha}} \qquad \textbf{(3.15)}$$

By increasing the number of transistors in Figure 3.6, different α and β values be generated in order to minimize the TC value [43].

In the proposed circuit in this thesis, we use the topology introduced in [41], which is also presented in [40]. The simplified version of the circuit in [41] with an additional temperature compensation transistor is given in Figure 3.7.

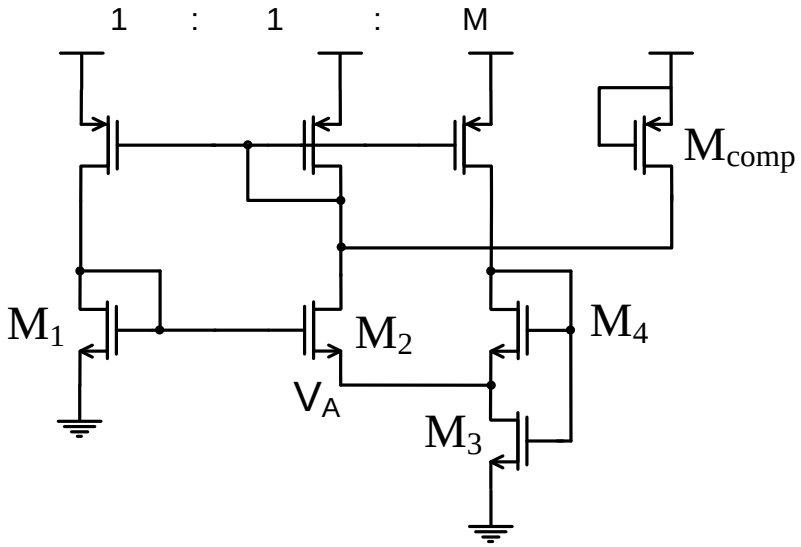

Figure 3.7 : Simplified version of the current reference in [41] with an additional temperature compensation transistor.

After analyzing the circuit with a similar fashion done for the conventional PTAT circuit, one can reach the following I_{ref} equation having a "$\mu V_A{}^2$" form given by:

$$I_{ref} = r_3 \mu C_{ox} V_A{}^2 \frac{1}{M+1}\left(\frac{r_3}{r_4}\frac{M}{M+1} + 0.5 + \sqrt{\frac{r_3}{r_4}\frac{M}{M+1}\left(\frac{r_3}{r_4}\frac{M}{M+1} + 1\right)}\right) \qquad \textbf{(3.16)}$$

The complete proposed circuit, which is a modified and improved version of Figure 3.7 with offset generation and temperature compensation, is given in Figure 3.8.

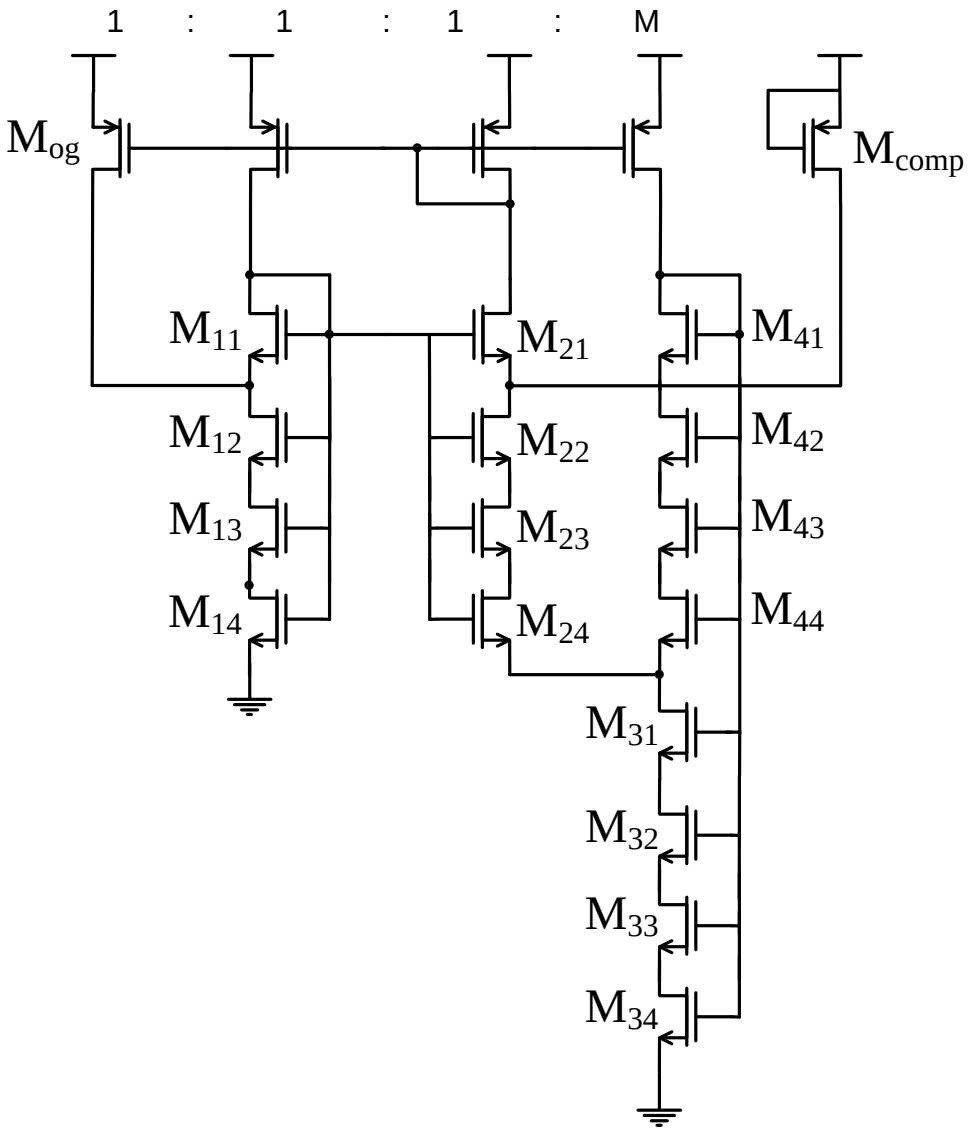

Figure 3.8 : Proposed current reference circuit.

In contrast to [43], to generate an offset voltage, we make use of transistor ladder in the core of the reference circuit (M_{11}-M_{14}) and inject current to the internal node of this transistor ladder by means of a single transistor (M_{og}). Moreover, we also replace M_3 and M_4 with transistor ladders, which help to improve TC value. Additionally, we apply temperature compensation to the internal node of the transistor ladder to obtain a better result.

As a result, a reference current of 519 pA with a very low TC of 57 ppm/°C, over a wide temperature range (-40 °C,+120 °C) has been obtained. The reference current as a function of temperature is shown in Figure 3.9. Although most of the works give TC values only for a typical simulation result, it is more accurate to give Monte

Carlo simulation results for a realistic TC value and distribution of the reference current to measure mismatch and process sensitivity.

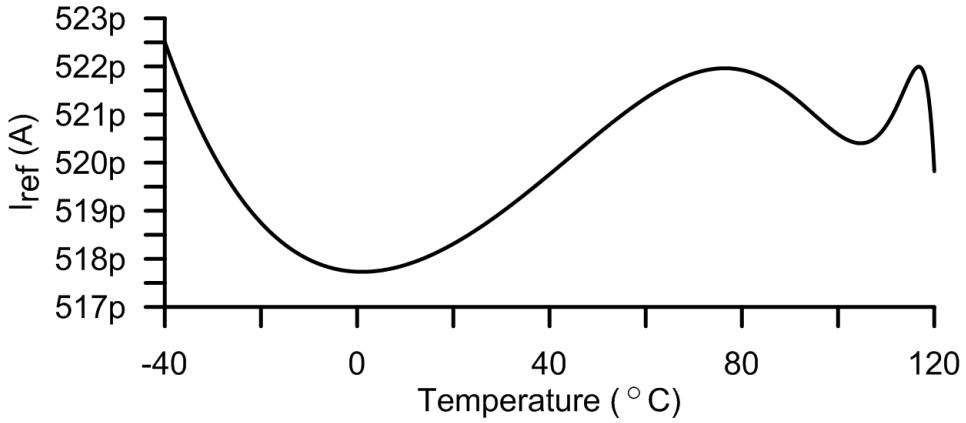

Figure 3.9 : Reference current as a function of temperature.

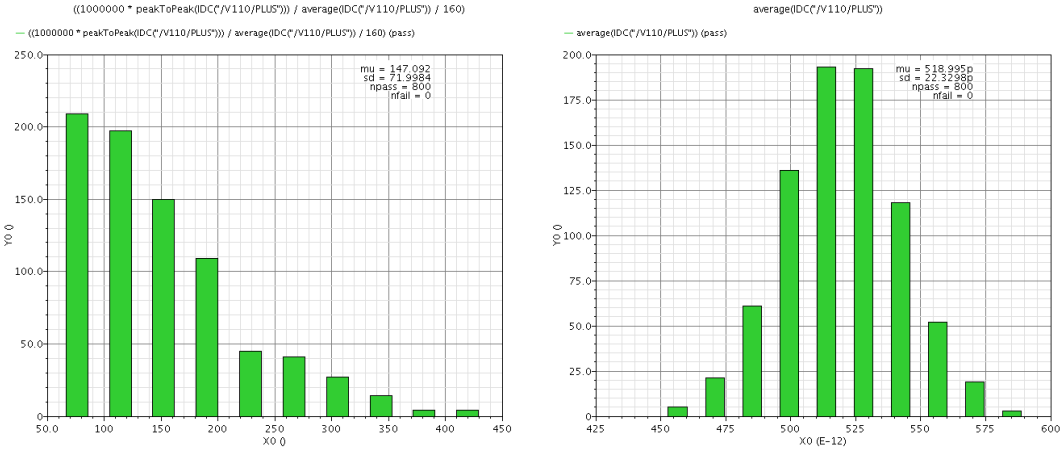

Figure 3.10 : Distribution of TC value (on left) and reference current (on right).

For this reason, we run Monte Carlo simulations of 800 runs and obtain an average TC value of 147 ppm/°C. The mean value of reference current is 519 pA with σ/μ = % 4.3. The results of Monte Carlo simulations are given in Figure 3.10.

As a concluding note, during the simulations, a way to decrease the value of the reference current was to lower the value of V_A. Moreover, using small size transistors also improved the TC value. Using these ideas, simulating the proposed circuit gave a TC value of 37 ppm/°C for a single simulation but an average value of 300 ppm/°C after the Monte Carlo simulation and worsened σ/μ value. Therefore, it is more convenient to give Monte Carlo simulation results. Using larger transistors and bigger V_A values degrades the performance for a typical simulation but enhances the performance of Monte Carlo simulations.

Lastly, we give a table comparing the results of the proposed work and literature. As a result, our design generates a subnanoampere current with a very low TC over a wide temperature range.

Table 3.1 : Performance comparison between this work and literature.

	This work	[36]	[37]	[38]	[40]	[41]	[43]	[44]
Process [µm]	**0.15**	0.35	0.35	0.35	0.18	1.5	0.35	0.09
I_{ref} [nA]	**0.519**	9.14	9.95	96	2.1	0.41	93	0.5
TC [ppm/°C]	**57**	44	1190	520	91	2500	288	526
Temp. range [°C]	**-40,120**	0,80	-20,80	0,80	0,150	-20,70	-20,100	-40,150
Area [mm^2]	**0.0024**	0.035	0.12	0.015	-	0.046	-	-
Power [nW]	**108**	36.6	68.1	1000	5.1	2	811	10
σ/μ [%]	**4.3**	6.5	14	-	-	-	7.55	-

A widely used way to split a reference current to smaller values is the simple R2R ladder circuit that is given in Figure 3.11. A transistor only version of R2R ladder, that is M2M ladder, is depicted in Figure 3.12.

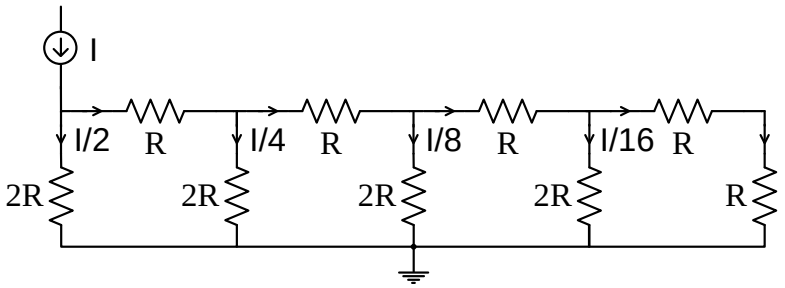

Figure 3.11 : R2R Ladder.

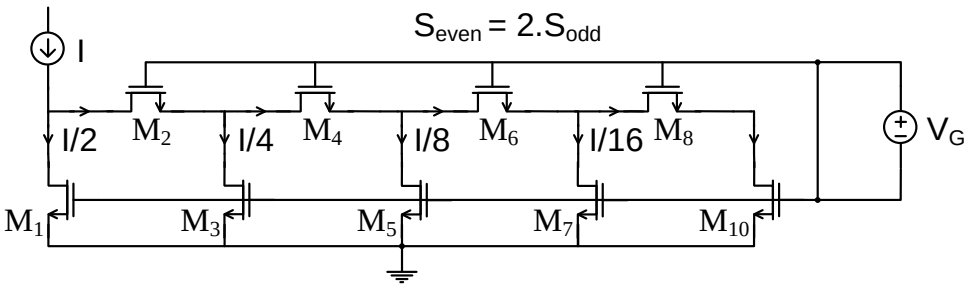

Figure 3.12 : M2M Ladder.

However, down to a few ten of picoamperes, the M2M circuit introduces temperature dependency and gain error. Therefore, this simple circuit is not a proper choice for generating pA and fA level current. To overcome this problem, a simplified version of the current divider that is involving a feedback system and presented in [45] is utilized. The simplified version of the current divider circuit is shown in Figure 3.13. In this circuit, the current KI_{out} is compared to I_{in} by two current mirrors and fed back to gate of M_f to adjust the output current. Hence, an output current equal to I_{in}/K is

obtained. Due to the feedback mechanism, a stable output current independent from process and temperature fluctuations is obtained.

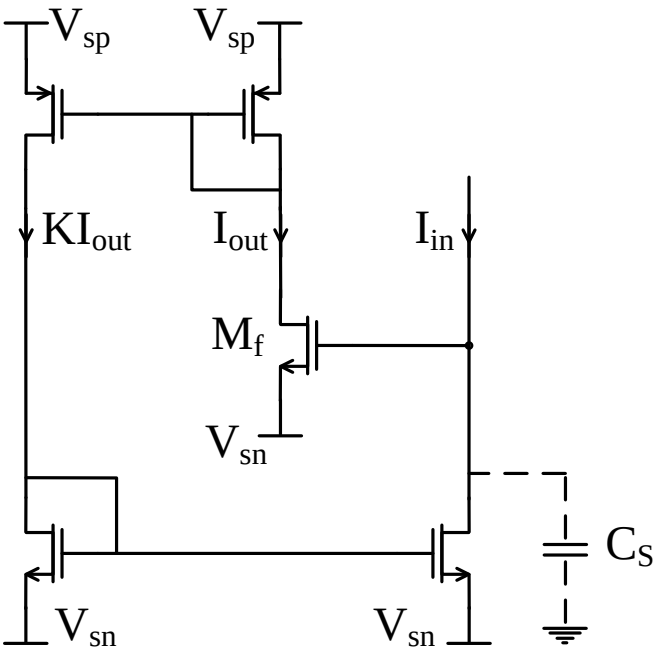

Figure 3.13 : Current divider circuit involving feedback.

In order to show the performance of the divider, we set the dividing ratio K to 10, and cascade four dividers. Thus, we obtain approximately a 50 fA and a 500 fA DC current source within a temperature range of (-40 °C, +60 °C) as depicted in Figure 3.14 while a 5 pA and a 50 pA DC current source is obtained in the range of (-40 °C, +120 °C) as depicted in Figure 3.15. The Monte Carlo simulations are also performed for these four level of currents which are given in Figure 3.16-3.19. As seen from these figures, the TC values are still in a reasonable range. To improve the process variations behavior, active current mirrors can also be used as in [46]. For a further enhancement, differential mode operation should be considered [46] but in the context of this thesis, a single ended mode operation gives satisfactory results.

In [34], it is reported that current levels as low as 3.5 fA has been obtained using the topology in Figure 3.12 on a fabricated chip in 0.35 µm technology. Additionally, in [47], a 100 fA bias current is generated in 0.18 µm technology utilizing the same topology and the outcomes are said to be in agreement with simulation results. In both works, master bias currents are PTAT current sources. Considering these studies, one can expect to observe such low current levels with a better topology in terms of process and temperature stability on a fabricated chip.

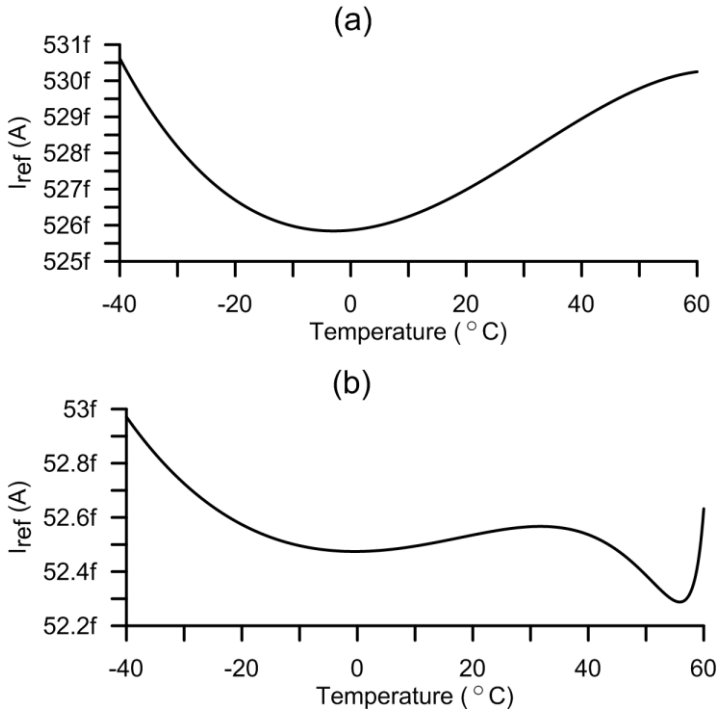

Figure 3.14 : 500 fA and 50 fA bias currents as a function of temperature.

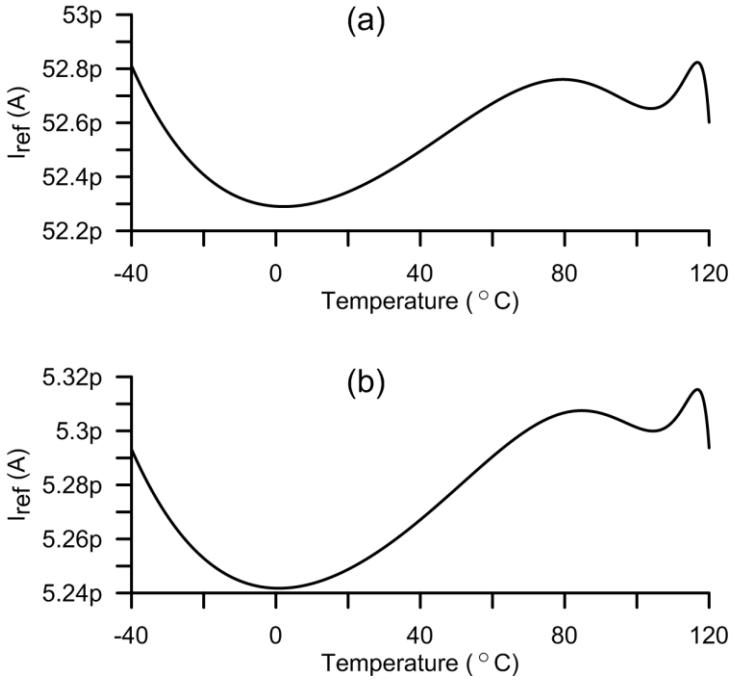

Figure 3.15 : 50 pA and 5 pA bias currents as a function of temperature.

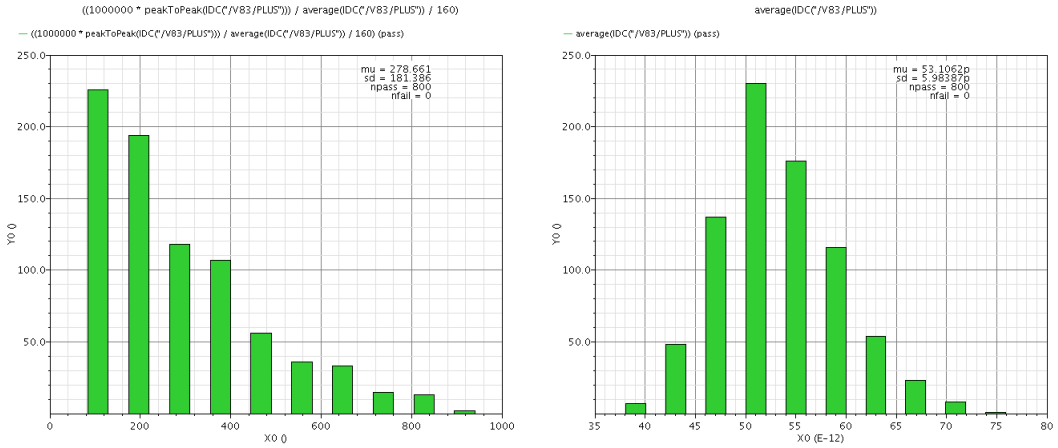

Figure 3.16 : MC simulation results for 50 pA current level.

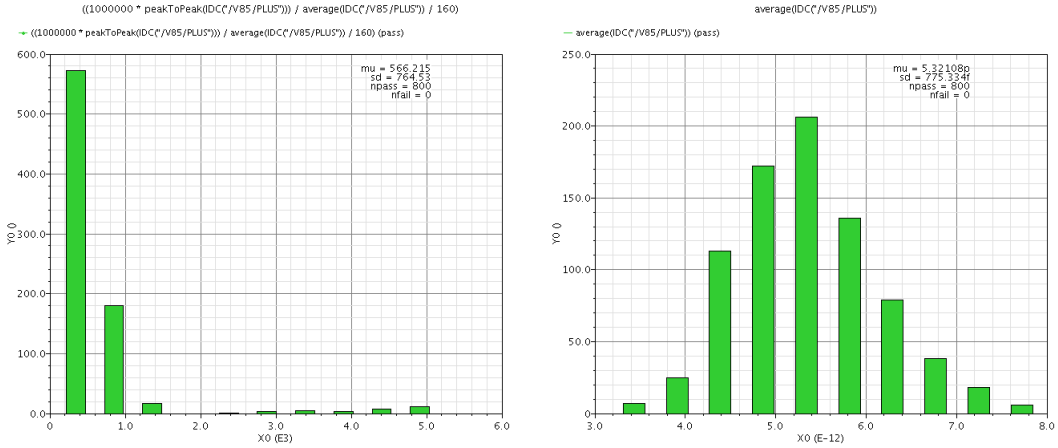

Figure 3.17 : MC simulation results for 5 pA current level.

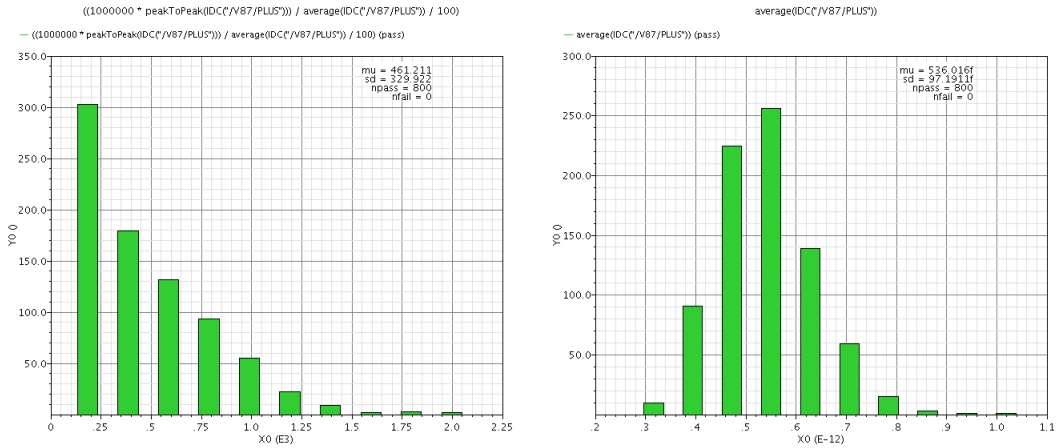

Figure 3.18 : MC simulation results for 500 fA current level.

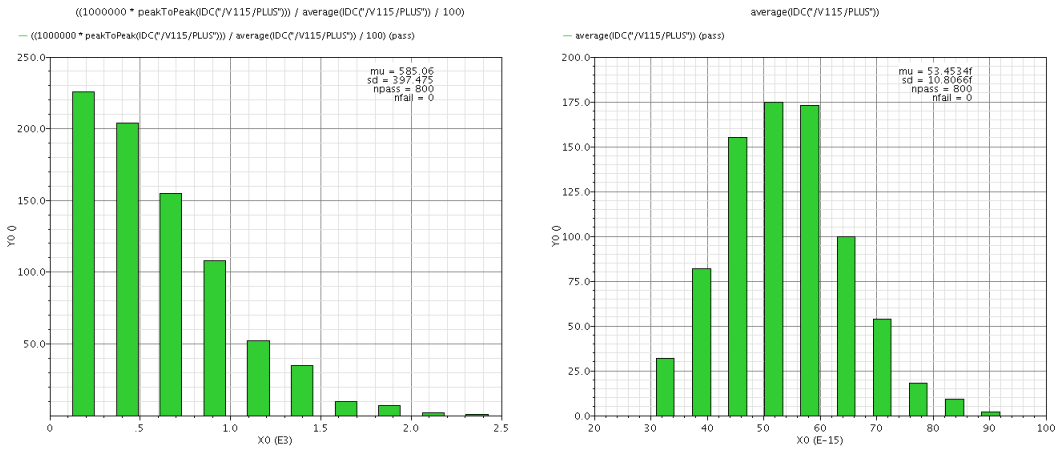

Figure 3.19 : MC simulation results for 50 fA current level.

3.4 A Wide Input Range Current Mode Exponential Circuit

In AdEx neuron model there exist and exponential term as repeated in eq. (3.17) where V is the input and V_T and Δ_T are constant parameters of the model.

$$\exp\left(\frac{V - V_T}{\Delta_T}\right) = \exp(x) \tag{3.17}$$

According to normalized behavior of the model, the variable *V* varies between (-60, 0) which corresponds to an interval of (-5, 25) for *x* in eq. (3.17). A solution to realize such a wide range may be to make a voltage mode design and make use of inherent characteristics of a MOSFET's subthreshold exponential behavior. However, a real time voltage mode design violates the low power and compactness strategy. Therefore, a current mode realization has to be considered. At the first moment, a realization of such a wide range looks practically impossible. Fortunately, there is no need to make a full range realization due to model dynamics. When the role of the exponential term is better understood, then the problem can be solved with an appropriate approximation method.

For a better insight, the nullclines of the AdEx neuron model are drawn in Figure 3.20. According to eq. (2.21), *V* nullcline is a combination of linear and exponential functions and has a convex form where the *w* nullcline is a straight line. For this reason, there occur only two possible fixed points rising from the intersection of these nullclines [29]. Due to the exponential term, the right arm of the nullcline has a high slope. Once the variable *V* increases and the right arm dominate, the trajectory diverges and a spike occurs. In the sharp rise (over threshold) phase, the role of the

exponential term is to create an undelayed sharp jump and prevent spike cutoff value sensitivity [24]. In the subthreshold phase, although the exponential term does not have an essential role, the value of the function cannot be neglected in order to sustain consistency and compatibility with the model. Moreover, bifurcation types, which occur around the fixed points, determine dynamical properties of such a system and fixed points exist in the subthreshold interval for the model.

In order to preserve dynamical properties and the shapes of firing patterns, the approximation error in the subthreshold phase is crucial. Thus, the order of approximation should be meticulously chosen by carefully evaluating the error in the subthreshold phase. Checking the firing patterns (also see Figure 4.4), one can see that the subthreshold range is roughly between the interval (-55,-45) for the variable *V* which corresponds to a range of (-2.5, 2.5) for the variable *x*.

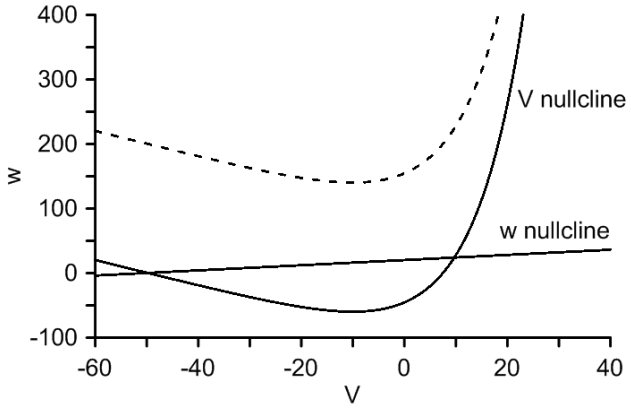

Figure 3.20 : The nullclines of AdEx neuron model. Dashed line corresponds to *V* nullcline in the presence of input current.

Determining the necessary range of approximation, a proper approximation method has to be chosen to realize the exponential term. Conventional approximation methods such as Taylor series expansion would require high order terms to obtain a wide output range. However, there is always a tradeoff between the accuracy and the circuit complexity. To overcome this problem, we use Padé approximation method and obtain a wide output range function. The basic property of Padé approximation is that, it generates a rational function rather than a series and gives better accuracy with same number of terms when compared to Taylor series expansion. Since the current dividers/multipliers have good accuracy in subthreshold domain, rational functions do not introduce any circuit complexity.

On the first step, keeping the tradeoff in mind, the Padé (2, 2) approximant is chosen as given by eq. (3.18).

$$P(2,2) = f(x) = \frac{1 + {}^{x}/_{2} + {}^{x^2}/_{12}}{1 - {}^{x}/_{2} + {}^{x^2}/_{12}} \cong \exp(x) \qquad \textbf{(3.18)}$$

As mentioned above, the *V* nullcline should have a convex form in order to intersect *w* nullcline twice. Note that this can only be achieved if the convex form of the approximation function is kept even out of the subthreshold phase. The function P(2,2) has a convex form for the subthreshold phase but fails to keep this property for the rest of the range. To guarantee the convexity, we had to have to obtain *exp(x/4)* function and take square of this function twice in succession to have a convex form throughout all the range. Furthermore, this method provides an extra advantage, i.e. it widens the output range of the approximation function. It is obvious that when the input range is narrowed, the output accuracy increases at the cost of the decreased output range. Since the double squaring operation introduces less error than the approximation function, we can get enhanced output range at the end with this method. In other words, the limitation of the dynamic range is mainly caused by the approximation function rather than the double squaring operation. Applying such a method is also reported directly in [48] and indirectly in [49-51]. Thus, the final approximation function obtained after applying this method is given in eq. (3.19).

$$\exp(x) = \exp\left(\frac{x}{4}\right)^4 \cong \left(\frac{1 + {}^{x}/_{8} + {}^{x^2}/_{192}}{1 - {}^{x}/_{8} + {}^{x^2}/_{192}}\right)^4 = \left(1 + \frac{48x}{(x-12)^2 + 48}\right)^4 \qquad \textbf{(3.19)}$$

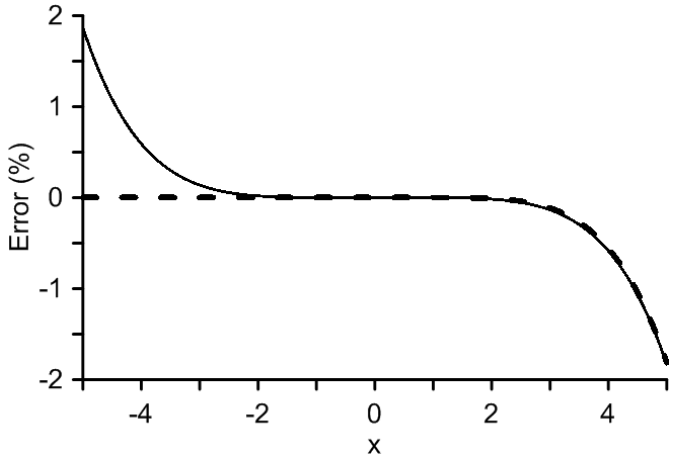

Figure 3.21 : Error rates. The solid line corresponds to exponential approximation and the dashed line stands for the V nullcline equation.

The error rate of the exponential approximation itself is given in Figure 3.21 indicated by the solid line. To investigate how much of this approximation error is reflected to the model, we insert the approximation function into the *V* nullcline in the presence of input, which is depicted in Figure 3.20 with dashed line. For the new case, the error rate transforms to the dashed line in Figure 3.20. Since the error rate is less than %2, we conclude that the P(2,2) function is an enough choice for our case.

To implement the approximation function, we need the denormalized version of it, which is given in eq. (3.20) (see chapter 4 for interval the steps) where *V* is replaced with I_v.

$$\exp(x) \rightarrow \frac{1}{(1pA)^3}\left(1pA + \frac{8pA(I_V - 2pA)}{\frac{(I_V - 4.4pA)^2}{1.2pA} + 1.6pA}\right)^4 \qquad \textbf{(3.20)}$$

For this purpose, the block diagram of the circuit realizing the function in eq. (3.20) is given in Figure 3.22 where all the multiplication and division operations are done by translinear loop multiplier/divider circuits. By the way, to minimize the current duplication errors, all the currents are copied with cascode or regulated cascode current mirrors when needed. Additionally we prefer p-type multiplier/divider circuit in order to lower DC gain error.

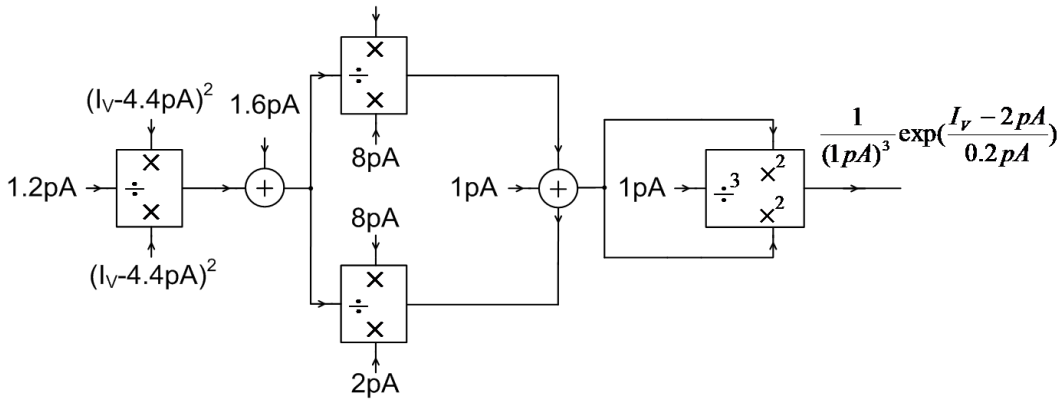

Figure 3.22 : Block diagram of the circuit that realizes eq. (3.20).

According to the simulation results for the exponential circuit, the error rates for the nominal case and worst cases are shown in Figure 3.23. As a result, an output range of 43.4 dB is obtained with 0.2 dB for nominal case and 0.5 dB error for the worst case, which is a very good performance when compared to some other works [49-51]. The main difference of the proposed design from other works is that the error

(0.2 dB) is very small where the most common error rate of exponential circuits are 1 dB in the literature.

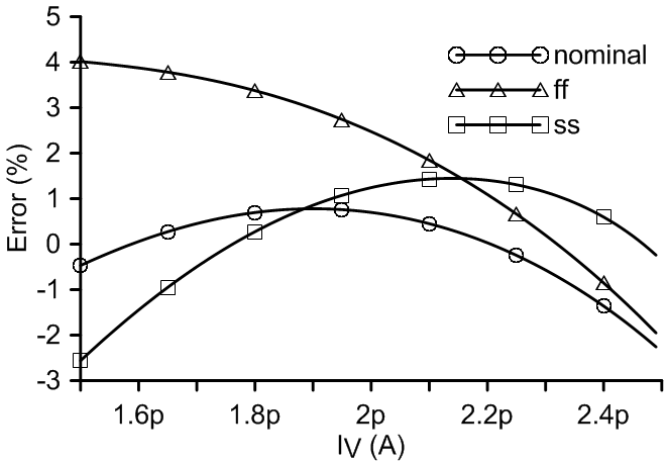

Figure 3.23 : Error rates of the exponential circuit.

An advantage of the exponential circuit is that, it can be utilized for implementing wide range sigmoidal functions. Such functions already exist as time constants and steady state functions in HH neuron model and biological synapse models. Therefore, this wide range exponential circuit is also utilized in HH neuron and in synaptic circuits, which will be explained in chapter 4 and 5.

3.5 Literature Overview of VLSI Neurons

Designing silicon neurons have been investigated in past, and still there is an ongoing research about it [1-12]. In this part, we mention some recent and popular works. A late review of silicon neurons with a wide reference list also can be found in [52]. Note that, we accept Figure 2.11 as a reference for evaluating the firing patterns of literature work. A performance comparison of the reviewed designs and designs of this thesis will be given at the end of next chapter all together.

In [53], Livi and Indiveri proposed a low power, compact neuron operating at real time scale. The design relies on a current-mode approach, but rather than using conventional log-domain filters, it uses the diff-pair integrator (DPI) for implementing tunable dynamic conductances. However, the design does not rely on a neuron model and presents poor dynamic behavior. A firing pattern obtained from this work is given in Figure 3.24.

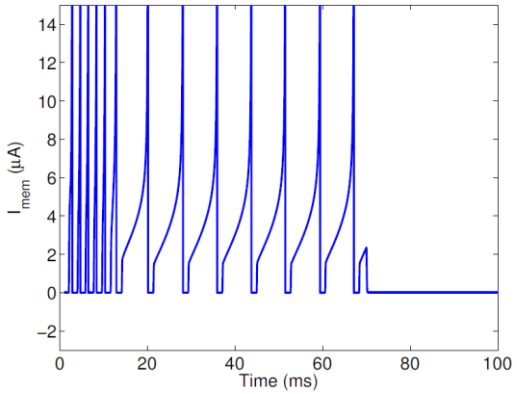

Figure 3.24 : A firing pattern obtained from [53].

In [54], Wijekoon and Dudek proposed a compact, voltage-mode neuron operating at real time scale. The design is said utilize a modified Izhikevich model however, the dynamics of the model is not considered during the design. The firing patterns of this work are given in Figure 3.25. Unfortunately, the patterns are poor to be preferred in a future implementation.

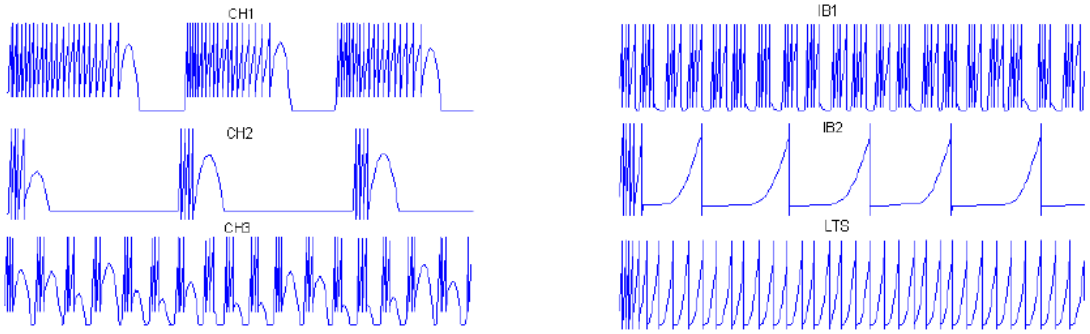

Figure 3.25 : Firing patterns obtained from [54].

In [55], Van Schaik et al. proposed a successful log domain implementation of Izhikevich neuron model. Although the neuron is dynamically satisfactory, it consumes and occupies large power and large area, respectively. The firing patterns of this work are given in Figure 3.26.

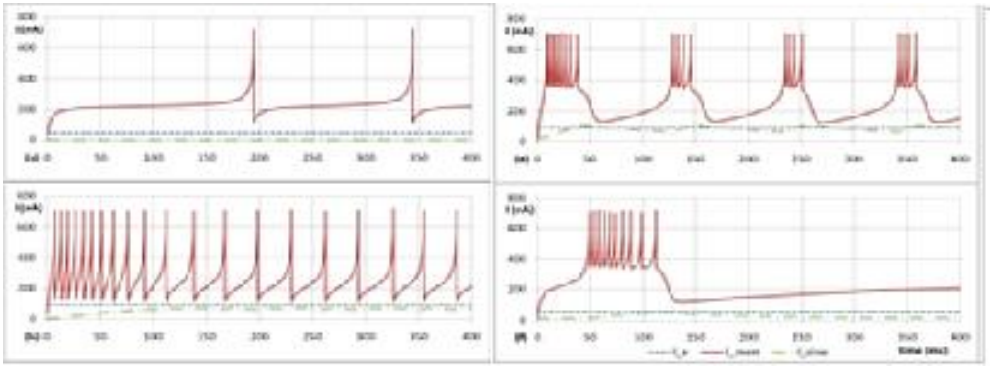

Figure 3.26 : Firing patterns obtained from [55].

In [56], Rangan et al. also proposed a log domain implementation of Izhikevich neuron model. However, the circuit consumes considerable power for a 90 nm design and the spike shapes are not fair considering different phases of an action potential such as depolarization and repolarization phases, probably due to poor resetting circuitry. The firing patterns of this work are given in Figure 3.27.

In [57], Millner et al. proposed a VLSI implementation of AdEx model for the first time that is in order to utilize in a wafer-scale neuromorphic hardware system for large-scale neural modeling [58]. However, this voltage mode design is neither a low power nor a low area design and works 10^5 times faster than biological timescale. The firing patterns of this work are given in Figure 3.28.

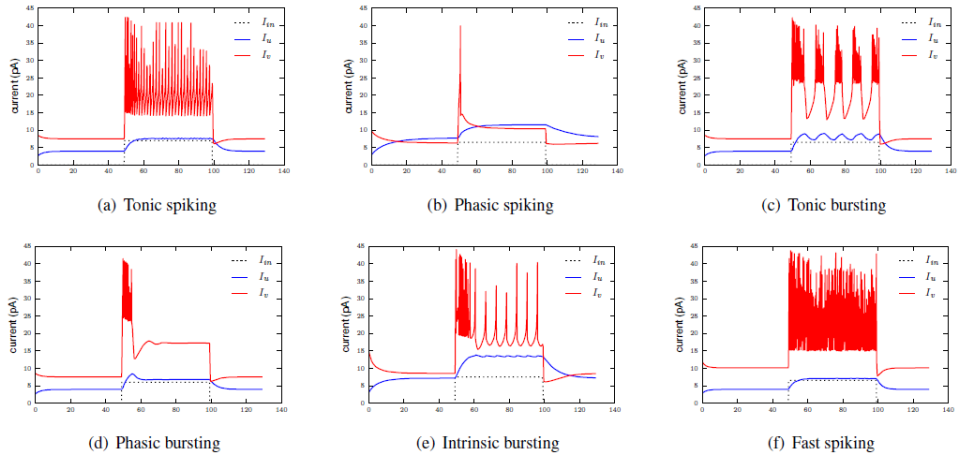

Figure 3.27 : Firing patterns obtained from [56].

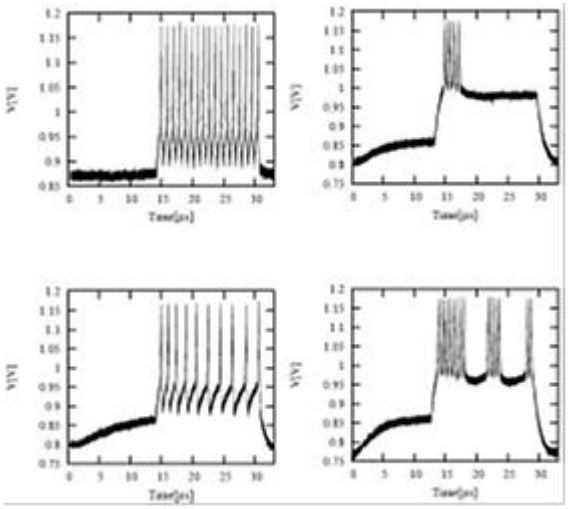

Figure 3.28 : Firing patterns obtained from [57].

In [59], Yu and Cauwenberghs proposed an analog VLSI Hodgkin-Huxley neuron in a fully programmable chip containing 4 neurons and 12 synapses. The channel

dynamics of the neurons are realized in log domain. The wide range sigmoidal functions are realized with a seven-segmented piecewise function. In this design, the channel membrane variable is a voltage signal where the rest of variables are represented by current signal. The action potential with channel variables and a synchronization pattern from this work are given in Figure 3.29 and Figure 3.30, respectively.

Except the works mentioned here, some other successful designs exist but they usually do not rely on a mathematical model [60] or require too much biasing voltages [61-63].

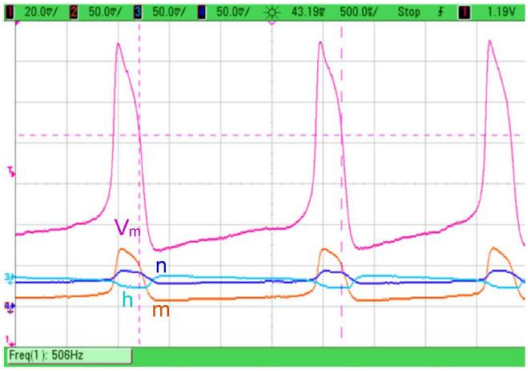

Figure 3.29 : The action potential with channel variables obtained from [59].

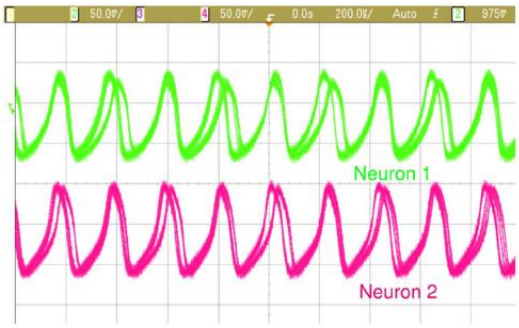

Figure 3.30 : A synchronization pattern obtained from [59].

Lastly, in a series of inspiring studies, a group of researchers design and fabricate reconfigurable HH neurons in a BiCMOS process. Then they communicate their chip with a computer in order to compare the chip output with numerical simulation results. According to the difference between these signals, they update their parameter set on chip until a matching occurs between the hardware and software. The aim of these studies is to build a hardware simulating system of HH neurons and conduct real time experiments with biological neurons [64-70].

4. LOW POWER COMPACT VLSI NEURONS

This chapter presents three low power and compact VLSI neurons, each relying on a mathematical model and operating at real (biological) timescale. The mathematical models utilized are namely Izhikevich (Izh), Adaptive Exponential Integrate and Fire (AdEx) and Hodgkin-Huxley (HH) neuron model.

The low power and compactness strategy allows designing massively parallel networks. Such a network may be useful for investigating computational properties of the brain or creating brain-like performing systems. On the other side, the performance of such implementations depends on the choice of the neuron model. A simple model with poor dynamics can affect the expected behavior of the network negatively. A complex model can also make the design complicated and restrict massive production. Therefore, we prefer neuron models that can exhibit a real neuron's dynamics and behaviors successfully while not causing a complicated electronic design.

4.1 The Izhikevich Neuron

A recent neuron model with rich dynamics and computational efficiency has been proposed by Izhikevich [23]. This model exhibits various firing patterns of cortical neurons by adjusting only four parameters and represented by two variables enabling a simple electronic design.

Two state equations and a pair of reset conditions as given below describe the neuron model:

$$\dot{v} = 0.04v^2 + 5v + 140 - u + I_{in} \quad \textbf{(4.1)}$$

$$\dot{u} = a(bv - u) \quad \textbf{(4.2)}$$

$$if\ v \geq v_{peak}, v \leftarrow c, u \leftarrow u + d \quad \textbf{(4.3)}$$

where v is the membrane potential, u is the membrane recovery variable, I_{in} is the external input current, v_{peak} is the spike cutoff value, a is the recovery time constant while the sign of b determines whether u is an amplifying ($b < 0$) or a resonant ($b > 0$) variable, c is the reset value of variable v and d is the increment amount of variable u at reset time. A set of parameters that leads to a typical neuron behavior is, $a = 0.02$, $b = 0.2$, $v_{peak} = 30$, $c = -65$ and $d = 8$. For these parameter values, regular spiking behavior is observed with an approximate period of 45 s where v takes value between (-75, +30) and u changes between (-8, 0). It should be noted that the parameters a and b are dimensionless and the rest of parameters have the same dimension with two variables.

To realize the model equations with log domain circuits, we need to express the variables in terms of currents that always take positive values. Therefore, we shift the variables up and then, for low power consumption, scale the magnitudes such that the variables vary in pA range. We lastly adjust the time scale for real time operation and obtain the equation set as described below:

$$10\tau\dot{I}_v = 4I_v(I_v - 4.5pA)10^{12} + (21pA + I_{in} - I_u) \quad \textbf{(4.4)}$$

$$\tau\dot{I}_u = a(10bI_v - I_u) \quad \textbf{(4.5)}$$

$$if\ I_v \geq I_{peak}, I_v \leftarrow I_c, I_u \leftarrow I_u + I_{incr} \quad \textbf{(4.6)}$$

where τ stands for the time constant and equal to 1ms, I_{peak} is the spike cutoff value, I_c is the reset value of I_v and finally I_{incr} is the amount of increment of I_u at reset time. Note that the variables and parameters in eq. (4.5) and (4.6) are currents in the pA range while a and b are still dimensionless. Here we note that we reduce the magnitude of the membrane variable v to one tenth as different from other realizations [55, 56].

The basic building block of the neuron circuit is the first order log domain filter given in Figure 3.4. For the circuit in Figure 3.4, the source voltages of M_2 and M_4 are shifted by an amount of V_{sn} (V_{sp} for PMOS transistors). We use source-shifting technique during all the design for a proper DC behavior as explained in chapter 3.

With a rearrangement of the eq. (4.4) and (4.5), we obtain eq. (4.7) and (4.8) in the form of eq. (3.4) and can realize these equations utilizing the circuit in Figure 3.4.

$$C_v\dot{I}_v = -4I_v(4.5pA - I_v)10^{12}C_v/(10\tau) + (21pA + I_{in} - I_u)C_v/(10\tau) \quad \textbf{(4.7)}$$

$$C_u\dot{I}_u = -I_u(aC_u/\tau) + I_v(10abC_u/\tau) \quad \textbf{(4.8)}$$

The overall neuron circuit with additional reset circuitry is given in Figure 4.1. When eq. (3.4) is reconsidered, we see that the lower bound of the capacitance value is limited by the currents I_b and I_d. Now it is clear that, scaling the magnitude of the membrane variable one to tenth introduces a coefficient of *10b* in eq. (4.8) (instead of *b*) and enables us to lower the capacitance value in this equation. In addition, the role of active diode connections is the same as explained in chapter 3.

As a result, we determine the minimum current level as 100 fA and choose $C_v = 80$ fF and $C_u = 160$ fF. The values of the DC currents are $I_{d-v} = 4.5$ pA, $I_{b-v} = 250$ fA, $I_{d-u} = a * 5$ pA, $I_{b-u} = 10ab * 5$ pA and $I_{DC} = 21$ pA. For typical values of the parameters *a* and *b*, values of the bias currents are $I_{d-u} = 100$ fA and $I_{b-u} = 200$ fA. The transistors M_5-M_8 realize the state equation in (4.8) related to I_u, while M_{11}-M_{14} and M_{16} realize the state equation in (4.7) related to I_v. The transistors M_{10} and M_{15} serve as a switch to reset the current I_v to I_c and I_u to I_u+I_{incr}. The values of the currents I_c and I_{inc} are made adjustable through the voltages V_c via M_{15} and V_d via M_9, respectively. Transistors M_{17}-M_{19} compose multiple output current mirror generating replicas of the current I_v. The comparator producing V_{reset} signal is composed of three cascaded differential pairs and the comparator generating $\overline{V_{reset}}$ is single differential pair. The diode connections of M_7 and M_{13} are also supplied by simple differential pairs with 10 pA bias current and unbalanced input transistors in order to create an offset voltage between drain and gate nodes for improved DC behavior [34,45].

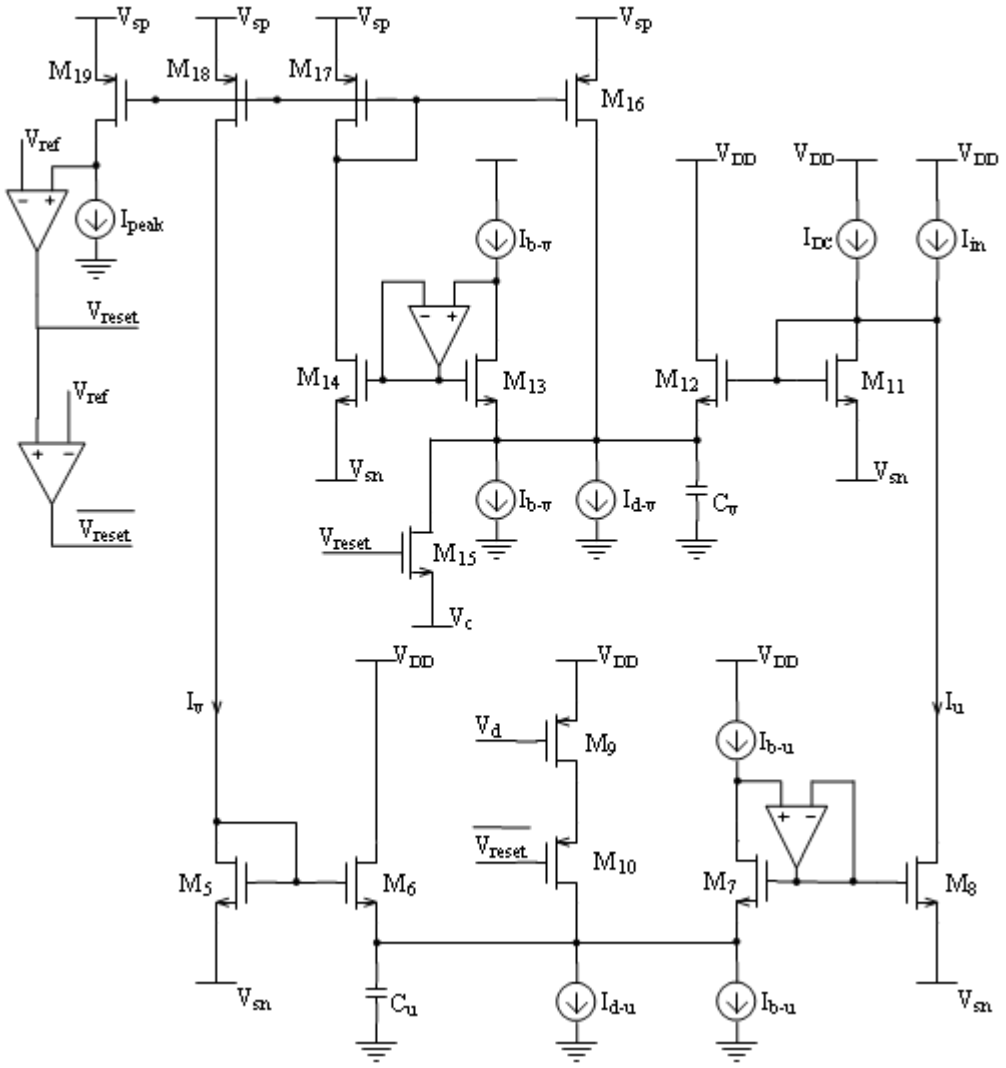

Figure 4.1 : The Izhikevich neuron circuit.

We simulated the neuron circuit using 0.15 µm CMOS process parameters with Spectre simulator in Cadence design tool. Supply voltage is V_{DD} = 1.5 V, V_{ref} = $V_{DD}/2$ and amount of source shifting is 300 mV. All the transistors have W/L = 450 nm / 450 nm. Differential pairs constituting the active diode connections and comparators are built with minimum size transistors. The tuning range of V_c and V_d are (355, 367) mV and (1.22, 1.35) V respectively. The estimated chip area for the neuron circuit is 275µm^2 where we predict the chip area by concerning the capacitance values and number of transistors used. At resting state, i.e. zero input state, I_v = 1.58 pA, I_u = 3.36 pA and the current and power consumption of the circuit is 166 pA and 249 pW, respectively. While the circuit is in regular spiking regime with a period of 45 ms, the circuit only consumes 270 pW.

Figure 4.2 shows different type of firing patterns reproduced from the circuit. The input is a step current except in Figure 4.2 (f) where it is a ramp current. The figures

4.2 (a-e) are reproduced according to parameter set in [23]. Since $b > 0$ in this design, the neuron circuit behaves as a resonator rather than an integrator. Therefore, we expect to see a *Class II* behavior as depicted in Figure 4.2 (f). Here, the neuron starts to fire at a non-zero frequency and the frequency of spiking changes slightly with increasing input current. Meanwhile, the neuron can be modified to behave as an integrator by simply shifting the *u* variable up and subtracting *v* variable from the drain node of M_5 instead of adding, in Figure 4.1, which corresponds to $b < 0$ behavior. Thus, a *Class I* behavior is obtained under a ramp input current as depicted in Figure 4.3. All the results, when compared with numerical simulation results in [23], show the success of the design.

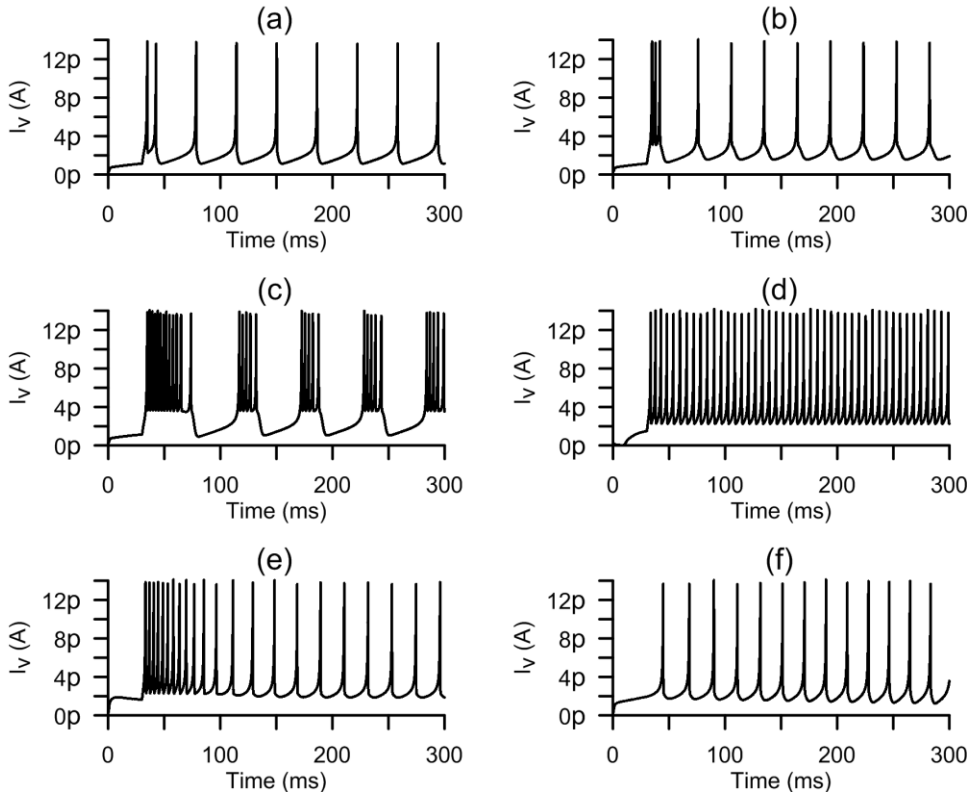

Figure 4.2 : Firing patters. (a) Regular Spiking, (b) Intrinsically bursting, (c) Bursting, (d) Fast Spiking, (e) Low Threshold Spiking (Spike Frequency Adaption), (f) Class II Behavior.

At this point, we want to note a general mistake done in the literature while interpreting the dynamical properties of firing patterns in *Class II* resonator. In *Class II* behavior, observing long periodic behaviors by supplying very low input currents or resetting the first variable to a low value may mislead to conclude the neuron as an integrator, i.e. shows *Class I* behavior. However, in order to properly justify the *Class* of the behavior, the firing patterns should be studied and obtained following

the way explained in [15] by exciting the neuron by a ramp input current and obtaining *f-I* characteristic of the neuron. The study of the dynamical behavior of the proposed neuron model according to this approach leads us to conclude that the proposed circuit is indeed a *Class II* neuron.

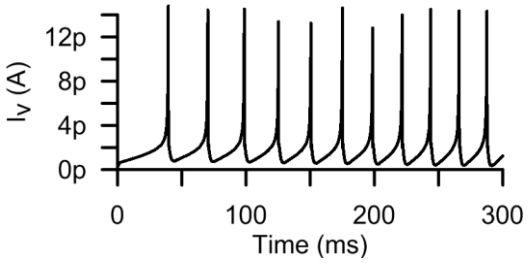

Figure 4.3 : Class I behavior.

For a robust design, we perform corner analysis of the neuron circuit. Since the parameter V_c corresponds to resetting value, it is not affected by any process variations. Fortunately, the other two parameters a and b are flexible and the effect of process variations does not affect the behavior of the neuron and hence we fix these two parameters. Thus, we only vary V_d for all corners in order to obtain the for main firing patterns in Figure 4.2 (a-d). The values of V_d for all corners producing four main firing patterns are summarized in Table 4.1.

As a result, we conclude that all firing patterns can be obtained just varying one of the parameters of the model in a narrow range.

Table 4.1 : V_d values for all corners producing four main firing patterns.

	Typical	**SS**	**FF**	**FS**	**SF**
RS	1.22	1.15	1.3	1.15	1.3
IB	1.24	1.18	1.3	1.18	1.29
LTS	1.35	1.28	1.4	1.27	1.4
Burst	1.32	1.28	1.37	1.24	1.36

Lastly, as reported in [24], the shapes of firing patterns are sensitive to v_{peak} (I_{peak}) value. Although not considered in the above design, this drawback has to be considered. Nevertheless, the low power and compact reliability make the design attractive [71].

4.2 The AdEx Neuron

Similar to the Izhikevich model, there is also a similar model in terms of efficiency and dynamics, called Adaptive Exponential Integrate and Fire (AdEx) neuron model,

which has two reported advantages over the Izhikevich model. The first one is that, the parameters of AdEx neuron model can be easily related to physiological quantities [28] and the model can successfully fit to real recordings of cortical cells. Secondly, the AdEx neuron model has almost no sensitivity to spike cut-off value whereas the Izhikevich neuron model suffers seriously because of this sensitivity [24], which can cause problems both in numerical simulations and circuit design. In fact, Izhikevich reported a solution for this problem [25] but it is a non-trivial solution in terms of circuit implementation.

In [57], a VLSI implementation of AdEx model is reported but this voltage mode design is neither a low power nor a low area design and works 10^5 times faster than real time. Therefore, in this work, we present a low power and compact implementation the AdEx neuron model, involving a wide output range current mode exponential circuit, operating at real time scale. We also demonstrate a log domain current mode design of the model for the first time.

The model consists of two differential equations and a pair of reset conditions as described below [27].

$$C\frac{dV}{dt} = -g_L(V - E_L) + g_L\Delta_T \exp\left(\frac{V - V_T}{\Delta_T}\right) - w + I_{in} \quad \textbf{(4.9)}$$

$$\tau_w\frac{dw}{dt} = a(V - E_L) - w \quad \textbf{(4.10)}$$

$$if\ V > V_{peak}, \qquad V \to V_r, \qquad w \to w + b \quad \textbf{(4.11)}$$

Here the variable V is the membrane voltage and w is the adaption variable, C is the membrane capacitance, g_L is the leak conductance, E_L is the leak reversal potential, V_T is the spike threshold, Δ_T is the slope factor, τ_w is the adaption time constant, a is the subthreshold adaption parameter, V_{peak} is the spike cutoff value, V_r is the reset value of the variable V, b is the spike triggered adaption parameter which occurs as an increment in the amount of the adaption variable w at reset moment and I_{in} is the injected input current. Although it looks like there are nine parameters, five of them are scaling parameters. After rescaling there are four parameters remaining: a, τ_w, V_r and b [27]. A set of parameters for four basic behaviors, namely tonic spiking, adaption, initial bursting and regular bursting, are given in Table 4.2. Note that, the

parameter V_{peak} can be chosen arbitrarily and is set to zero, as expressed in [27]. The four firing patterns are given in Figure 4.4. A detailed study of firing patterns and dynamical behavior analysis can be found in [27] and [29, 30] respectively.

Since the eq. (4.9)-(4.11) are in normalized form, a rearrangement is needed obtain the proper circuit implementation. Considering a low power, compact current-mode log domain operation, DC level shifting, amplitude and time scaling are applied such that the state variables always take positive values in pA range and operate at biological time scale.

Table 4.2 : Parameter values for various firing patterns

	C	g_L	E_L	V_T	Δ_T	a	τ_w	b	V_r	I_{in}
Tonic spiking	200	10	-70	-50	2	2	30	0	-58	500
Adaption	200	12	-70	-50	2	2	300	60	-58	500
Inital Burst	130	18	-58	-50	2	4	150	120	-50	400
Regular Burst	200	10	-58	-50	2	2	120	40	-46	210

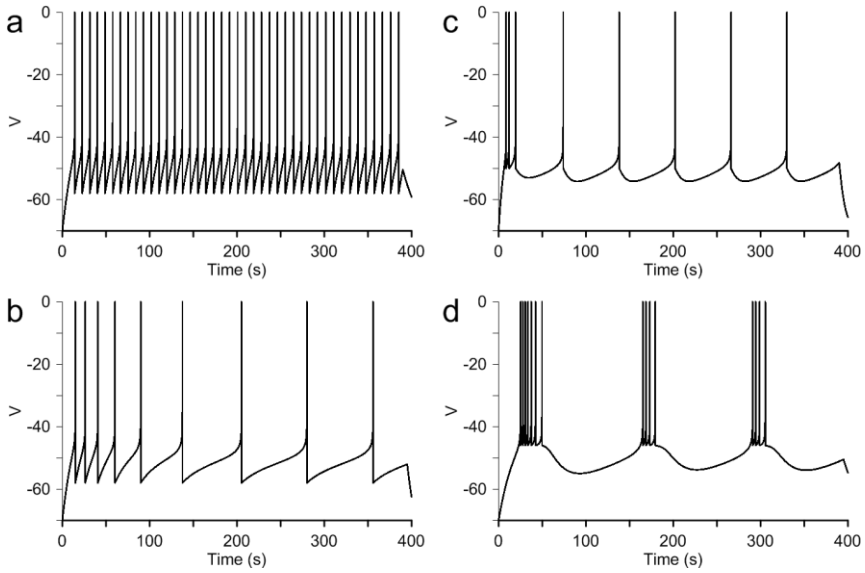

Figure 4.4 : Various firing patterns: (a) tonic spiking, (b) adaption, (c) initial burst, (d) regular bursting.

The final set of equation for the neuron is given as follows:

$$C_V \frac{dI_V}{dt} = -g_L I_V(1pA) + \left(\underbrace{\frac{g_L I_\Delta}{10} \exp\left(\frac{I_V - I_T}{I_\Delta}\right)}_{I_{exp}} - I_w + I_{DC} + I_{in} \right)(1pA) \qquad \textbf{(4.12)}$$

$$C_w \frac{dI_w}{dt} = aI_V(1pA) - I_w(1pA) \qquad \textbf{(4.13)}$$

$$if\ I_V > I_{V_{peak}}, \qquad I_V \to I_r, \qquad I_w \to I_w + I_b \tag{4.14}$$

where I_{DC}stands for the current required for DC level shifting and involving parameter E_L. All the other parameters are renamed according to their dimensions with corresponding indices. To be clear, for instance, the parameter set for a bursting neuron is given in Table 4.3. Note that dimensions of parameters are expressed in brackets.

Table 4.3 : Parameter values for a bursting neuron.

	C_V [fF]	g_L [-]	I_{DC} [pA]	I_T [pA]	I_Δ [pA]	a [-]	C_w [fF]	I_b [pA]	I_r [pA]	I_{in} [pA]
Regular Burst	200	10	14.4	2	0.2	2	120	3	2.4	21

The main blocks of the neuron circuit are the first order log domain filter and the exponential circuit. We realize each of state equations (4.12) and (4.13) with log domain filters. The realization of the exponential term had been given in the previous chapter. The V-cell with additional reset circuitry and w-cell are drawn in Figure 4.5 and Figure 4.6, respectively. Comparing eq. (4.12) and eq. (4.13) with eq. (3.4), one can see that $\alpha I_{b-V} = 1$pA, $\alpha I_{d-V} = g_L x1$ pA, $\alpha I_{b-w} = \alpha x1$ pA and $\alpha I_{d-w} = 1$ pA. For a low area design, the values of the capacitors are set to $C_V = 200$ fF, and $C_w = 240$ fF. Thus, the values of the DC currents are $I_{d-V} = 250$ fA, $I_{b-V} = 25$ fA, $I_{d-w} = 50$ fA, $I_{b-w} = 100$ fA and $I_{DC} = 14.4$ pA. The transistors M_5-M_8 and M_{11}-M_{14} form the translinear loops while M_9 and M_{16} serve as a switch to reset I_V to I_r and I_w to I_w+I_b. The current values I_V and I_b made adjustable through the voltages V_r via M_9 and V_b via M_{15}, respectively. M_{10} mirrors the current I_V and the comparator along with the NOT gates produce the voltages V_{reset} and $\overline{V_{reset}}$. The diode connection of M_7 and M_{13} is formed by a buffer which is indeed a simple differential pair with an unbalanced input pair in order to create an offset voltage between drain and source terminals of M_7 and M_{13} to improve DC behavior [34,45] and supplied by a 10 pA bias current.

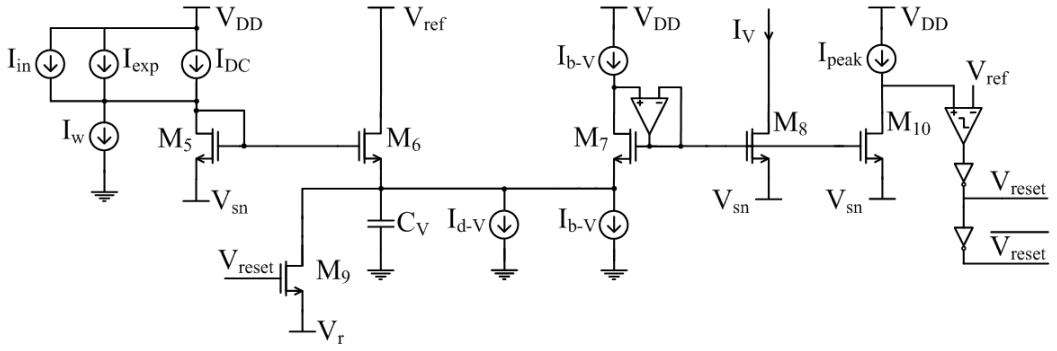

Figure 4.5 : V-cell with additional reset circuitry.

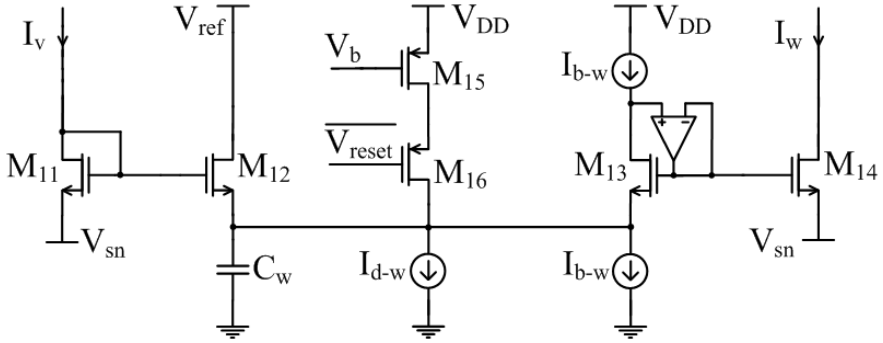

Figure 4.6 : w-cell.

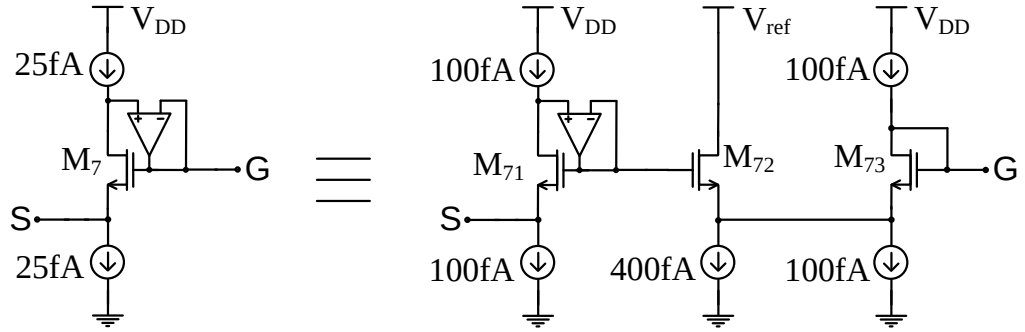

Figure 4.7 : Equivalent circuit for M_7 in V-cell.

The bottleneck of this design is the value of $I_{b-V} = 25$ fA, which is difficult to generate with respect to other bias currents. Such a low current value also deteriorates the AC behavior. To get rid of these disadvantages, we replace M_7 in Figure 4.5 with an equivalent translinear loop circuit, as depicted in Figure 4.7. By this way, the minimum current level is increased to 100 fA and a better AC behavior is obtained.

The neuron circuit is simulated using 0.15 µm CMOS process parameters using Spectre in Cadence design tool. Supply voltage is V_{DD} = 1.5 V, V_{ref} = V_{DD}/2 and

amonut of source shifting is 300 mV. All the transistors have W/L = 450 nm / 450 nm except for M_{15}, the DC current generator of w-cell, with a ratio W/L = 450 nm / 1.5 µm. Transistors in the buffers forming the active diode connections are also minimum sized. The tuning range of V_r and V_b are (390, 415) mV and (1.15, 1.3) V respectively. It should be noted that, in eq. (3.4), I_b and the aspect ratios of transistors composing the translinear loop appear as a product term for the log-domain filter block. Therefore, the deviations of transistors' aspect ratios can be tolerated by adjusting I_{b-V} and I_{b-w} currents. The estimated chip area for a single neuron is 490 µm^2. At resting state, i.e. zero input state, I_V = 1.45 pA, I_w = 3 pA and power consumption of the neuron circuit is 462.1 pW. While the neuron is in tonic spiking regime with a period of 25 ms, the circuit consumes only 9.3 nW.

Figure 4.8 shows the firing patterns reproduced from the circuit where the input is a step current. The similarity between firing patterns in Figure 4.8 and the ideal patterns in Figure 4.4 is remarkable. To show the robustness of the design, corner analyses of the neuron circuit are performed. Similar to Izh neuron, only one of the variables V_b is tuned to obtain the firing patterns. The corresponding parameter set for each corners is given in Table 4.4.

As a result, all the firing patterns are reproduced successfully by tuning only one parameter in a reasonable range.

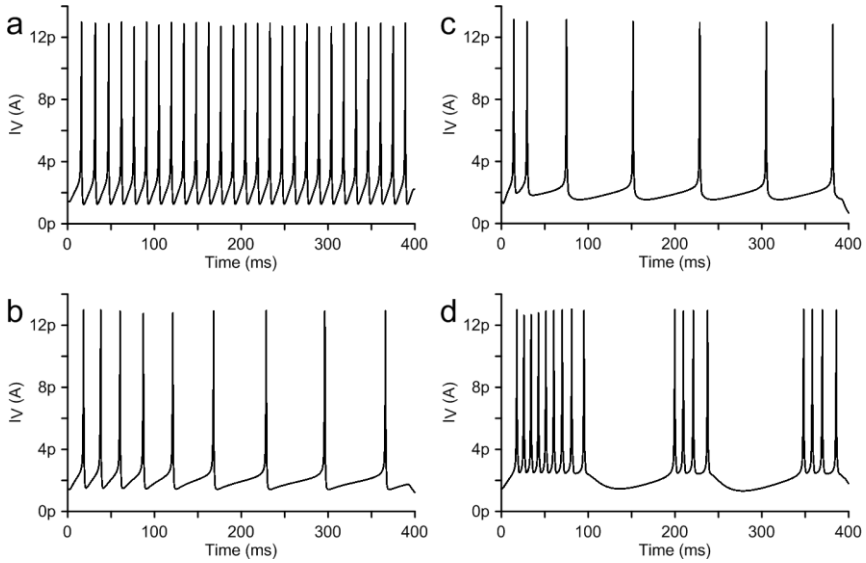

Figure 4.8 : Firing patterns reproduced from the neuron circuit: (a) tonic spiking, (b) adaption, (c) initial burst, (d) regular bursting.

Table 4.4 : V_b value for all corners producing four main firing patterns.

	Typical	SS	FF	FS	SF
TS	-	-	-	-	-
IB	1.22	1.16	1.3	1.16	1.28
Adapt.	1.24	1.18	1.3	1.18	1.3
Burst	1.28	1.24	1.35	1.22	1.36

On the other side, the AdEx neuron circuit consumes more power when compared to Izhikevich neuron. The main reason is the exponential circuit because e^x term takes bigger values than x^2 during the resetting phase resulting in more current consumption. Therefore, we conclude that a tradeoff exists between a more accurate model and power consumption.

4.3 The Hodgkin-Huxley Neuron

The Hodgkin Huxley model is both computationally and electronically, an expensive model. However, the model involves a full biophysical meaning and hence still being realized electronically at the cost of power and area [59, 63-70]. In these works, as in a real nerve cell, the membrane variable is represented by a voltage signal and the other variables by current variables. Here, the main reason of an expensive electronic realization is wide range sigmoidal steady state functions and unimodal time constants, which are depicted in Figure 2.6. To implement such functions for each channel variable increases the cost of the design.

In this part, we demonstrate a fully current mode realization of Hodgkin-Huxley model. These sigmoidal and unimodal functions, which are approximated by the Boltzmann and Gaussian functions, are realized using the wide range exponential circuit introduced in chapter 3. Therefore, the membrane variable becomes a current variable.

The equation set of the HH model in a brief form is:

$$C\frac{dV}{dt} = I - g_{Na}m^3h(V - V_{Na}) - g_K n^4(V - V_K) - g_L(V - V_L) \qquad \textbf{(4.15)}$$

$$\dot{x} = \frac{x_\infty(V) - x}{\tau_x(V)} \qquad \textbf{(4.16)}$$

where *x* stands for *m*, *n* and *h* variables. The sigmoidal steady state function x_∞ is approximated by a Boltzmann function:

$$x_\infty(V) = \frac{1}{1 + \exp\left(\frac{(V_{1/2} - \mathrm{V})}{k}\right)} \tag{4.17}$$

where k is the slope factor and the parameter $V_{1/2}$ satisfies $x_\infty(V_{1/2}) = 0.5$. Similarly, the unimodal time constant function is approximated by a Gaussian function:

$$\tau_x(V) = C_{base} + C_{amp} exp\left(-\left(\frac{V - V_{max}}{\sigma}\right)^2\right) \tag{4.18}$$

where C_{base} is the base level, C_{amp} is the amplitude of the function. Geometrical interpretations of Boltzmann and Gaussian functions are given in Figure 4.9. In addition, the parameter set of the Boltzmann function for the *m*, *n* and *h* variables and parameter set of the Gaussian function for the same variables are given in Table 4.5. To avoid confusion, original set of parameters is given, to be in accordance with literature. The values in the brackets correspond to the shifted values that are used during the design.

Table 4.5 : Parameter set for Boltzmann and Gaussian functions of HH model.

$x_\infty(V)$	$V_{1/2}$	k	$\tau_x(V)$	V_{max}	σ	C_{amp}	C_{base}
m_∞	25 (45)	9	τ_m	27 (47)	30	0.46	0.04
n_∞	12 (32)	15	τ_n	-14 (6)	50	4.7	1.1
h_∞	3 (23)	-7	τ_h	-2 (18)	20	7.4	1.2

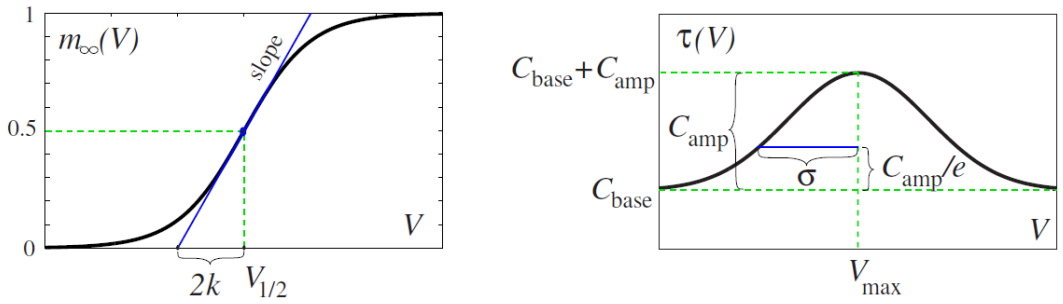

Figure 4.9 : Geometrical interpretation of Boltzmann and Gaussian functions parameters.

Before circuit simulation, we present numerical simulation results presenting a typical action potential and channel variables in Figure 4.10 and Figure 4.11.

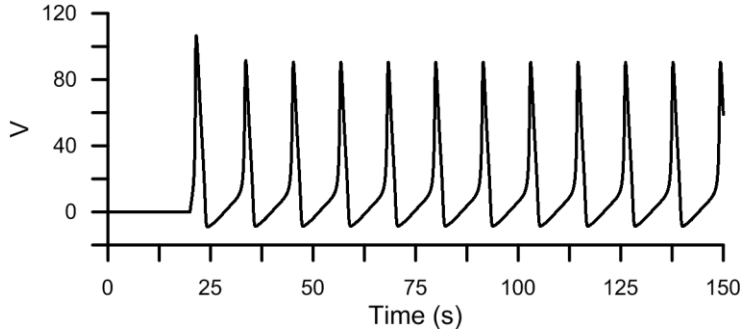

Figure 4.10 : The action potential of HH model.

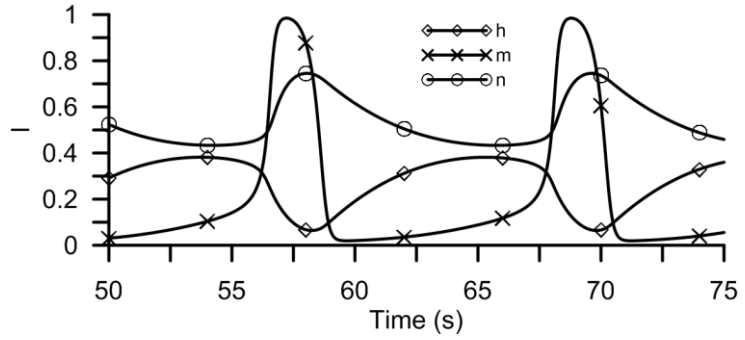

Figure 4.11 : Channel variables of HH model.

In order to obtain a low power, compact current-mode log domain operation, DC level shifting, amplitude and time scaling are applied such that the state variables always take positive values in pA range and operate at biological time scale. To simplify the equation, we also replace conductance parameters and reversal potentials with their numerical values. Thus, we arrive the following final set of equation for the neuron:

$$aC_V\dot{I_V} = -I_V\left(120\frac{{I_m}^3 I_h}{1pA^3} + 36\frac{{I_n}^4}{1pA^3} + 0.3pA\right)a + \left(I_{in} + 120\frac{{I_m}^3 I_h}{1pA^3}13.5 + 36\frac{{I_n}^4}{1pA^3}0.8 + 0.918pA\right)a(1pA) \quad \textbf{(4.19)}$$

$$aC_x\dot{I_x} = -I_x\frac{1pA^2}{I_{\tau_x}}a + I_{x_\infty}\frac{1pA^2}{I_{\tau_x}}a \quad \textbf{(4.20)}$$

where a is used to enlarge both sides of eq. (4.19) and (4.20) and x stands for m, n, and h.

To give an example for the terms $I_{\tau_x}$and I_{x_∞}, the expressions for $I_{\tau_n}$and I_{n_∞} are given as below.

$$I_{\tau_n} = 1.1pA + 4.7pAexp\left(-\left(\frac{I_v - 0.6pA}{5pA}\right)^2\right) \quad \textbf{(4.21)}$$

$$I_{n_\infty} = \frac{1pA^2}{1pA + 1pAexp\left(\frac{3.2pA - I_v}{1.5pA}\right)} \quad \textbf{(4.22)}$$

The time constant and steady state functions in eq. (4.21) and (4.22) are realized systematically using exponential circuits and the current multiplier/divider circuits. The circuit realizing eq. (4.20) is given in Figure 4.12 where a translinear loop current multiplier/divider circuit is combined with a first order log domain filter. Similarly, a log domain filter is used in order to realize eq. (4.19) where,

$$I_{in-V} = I_{in} + 120\frac{{I_m}^3 I_h}{1pA^3}13.5 + 36\frac{{I_n}^4}{1pA^3}0.8 + 0.918pA \quad \textbf{(4.23)}$$

$$I_{d-V} = 120\frac{{I_m}^3 I_h}{1pA^3} + 36\frac{{I_n}^4}{1pA^3} + 0.3pA \quad \textbf{(4.24)}$$

and all the capacitance values are fixed to $C_x = C_V = 200$ fF. Finally, the translinear multiplier/divider loop circuit producing gated conductances, for instance $120\frac{{I_m}^3 I_h}{1pA^3}$ and $120\frac{{I_m}^3 I_h}{1pA^3}13.5$, are given in Figure 4.13.

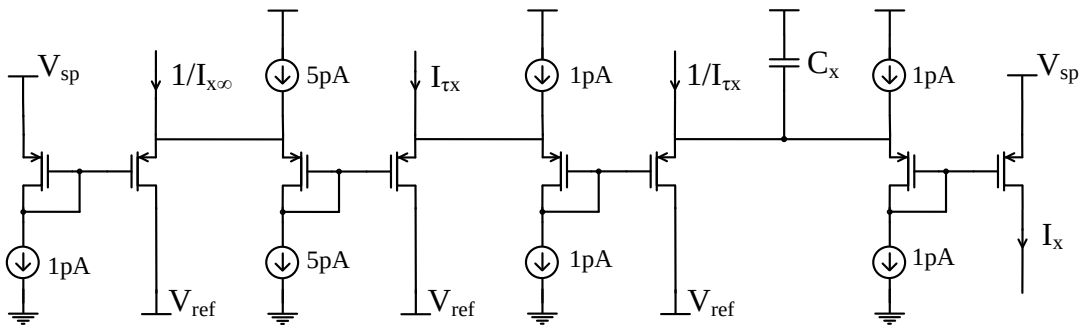

Figure 4.12 : The circuit realizing eq. (4.20).

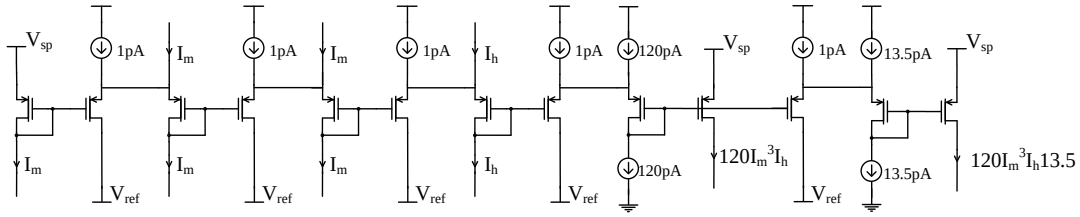

Figure 4.13 : Translinear loop producing gated conductances.

According to the circuit simulation results, the steady state and time constant functions are obtained as depicted in Figure 4.14. When compared to Figure 2.6, one can see that the functions are realized with a good accuracy.

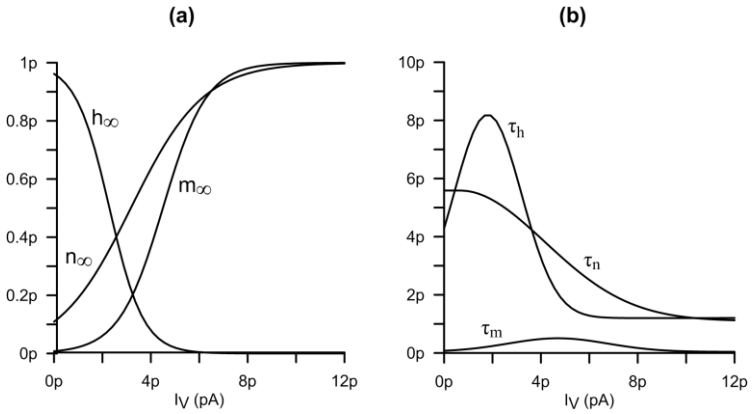

Figure 4.14 : Steady state (a) and time constant functions (b) of channel variables obtained from the circuit.

The action potential and channel variable currents obtained from the circuit are given in Figure 4.15 and 4.16. The results again agree well with the numerical simulations given in Figure 4.9 and 4.10.

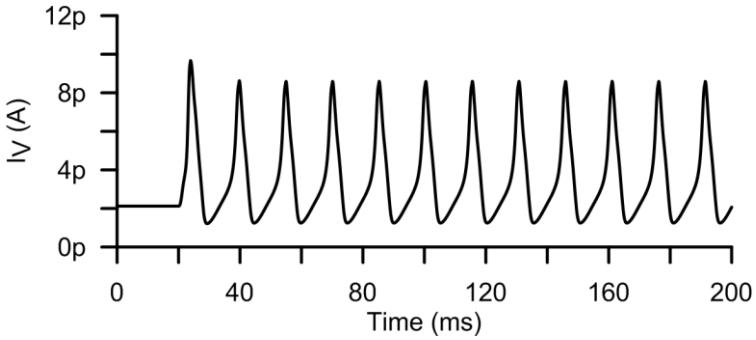

Figure 4.15 : The action potential obtained from the circuit.

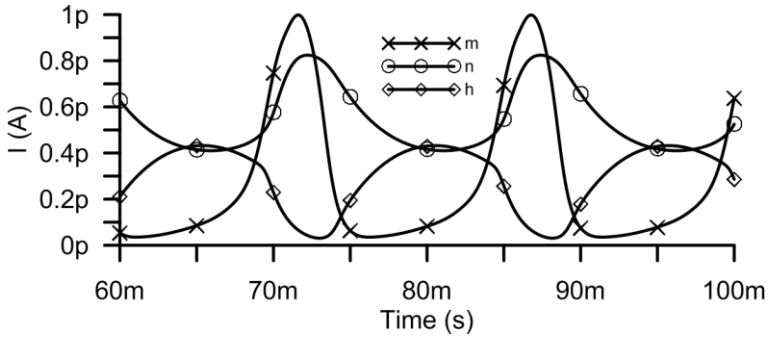

Figure 4.16 : Channel variables obtained from the circuit.

The estimated chip area for the neuron circuit is 1200 μm^2. At resting state, I_v = 2.13 pA and the current and power consumption of the circuit is 2.26 nA and 3.4 nW, respectively. The neuron circuit consumes 3.57 nW power during the spiking regime with 65 Hz frequency. The area occupied is high when compared to the Izh and AdEx neuron because the number of variables realized is much more. In addition, six exponential circuits are used. Nevertheless, when compared to other works in literature, the HH neuron designed can still be assumed as a low power and compact neuron circuit.

In conclusion, a comparison between the designed neurons and some other similar works is given in Table 4.6.

Table 4.6 : A comparison table between our work and some other works.

	Area [μm2]	**Power [nW]**	**Time Scale**	**Patterns**	**Model**
[53]	913	2.67	real	fair	modified IF
[54]	4900	-	real	poor	modified Izh
[55]	20.000	20.000	real	good	Izh
[56]	2980	7	x10	Not fair	Izh
[57]	-	100.000	x10^5	good	AdEx
[59] (estimated)	400.000	50.000	x10	good	HH
Izh (This work)	275	0.27	real	very good	Izh
AdEx (This work)	490	9.3	real	very good	AdEx
HH (This work)	1200	3.57	real	very good	HH

5. SIMPLE NETWORK DYNAMICS OF THE IZH AND ADEX NEURON

In this chapter, we show that the Izh and AdEx neurons can produce synchronization patterns with in a simple network. Two AdEx neurons are coupled via a linear synaptic circuit, which relies on a chemical synapse model. We also couple three and nine Izh neurons with the simplified version of this synapse. In both of the networks, two types of coupling, i.e. excitatory and inhibitory, are provided. As a result, the neurons successfully exhibit network dynamics.

Synapses play a crucial role in information transfer. Due to synaptic dynamics, important properties exist in a network such as cognition, learning etc. However, in most of the VLSI synapse designs, temporal dynamics are neglected and synapses are assumed as an instantaneous multiplier operator. For this reason, in order to build a powerful neural network, realistic synaptic models should be preferred. Therefore, we adopt a biological chemical synapse model for coupling the designed neurons [72].

Synchronized activity of neurons takes role in a wide range from cognitive functions to rhythmic movements of animals. Therefore, we set excitatory and inhibitory coupling between neurons and investigate the synchronization activity of the network. When an excitatory coupling exists between two neurons, it means that the presynaptic neuron encourages the postsynaptic neuron to generate a spike. In contrast, when an inhibitory coupling exists, it means that the presynaptic neuron inhibits the postsynaptic neuron from generating a spike [17]. The expected synchronization patterns are inphase (zero phase difference), antiphase (180° phase difference) and n-phase (arbitrary phase difference).

Running long transient simulations in time is a tedious task and care must be taken. Therefore, the circuit simulation results are also supported with numerical simulation results in order to show the success of the design.

5.1 Two Coupled AdEx Neurons

To show that the designed AdEx neuron can exhibit network dynamics, we couple two of them via a chemical synapse model [72]. The equation set of the synapse model is given below:

$$I_{syn}(N_i, N_j) = g_{ij} S_i (E_{syn} - V_j) \tag{5.1}$$

$$\tau_S \frac{dS_i}{dt} = \frac{-S_i + S_\infty}{(1 - S_\infty)} \tag{5.2}$$

$$S_\infty(V_i) = 1 \Big/ \left\{ 1 + \exp\left(\frac{(V_{1/2} - V_i)}{k} \right) \right\} \tag{5.3}$$

where $I_{syn}(N_i, N_j)$ is the synaptic current received by postsynaptic neuron N_j from presynaptic neuron N_i, g_{ij} is the peak synaptic conductance, S_i denotes the synaptic activity, E_{syn} is the synaptic reversal potential, S_∞ is the steady state activation function, τ_S is the time constant, k is the synaptic slope factor and the parameter $V_{1/2}$ satisfies $S_\infty(V_{1/2}) = 0.5$. Additionally, we set $E_{syn} = 0$ and $E_{syn} = -80$ for excitatory and inhibitory coupling, respectively. We also determine the value of g_{ij} such that the synaptic current I_{syn} is less than %5 of the injected input current I_{in} to provide a weakly coupling [73]. Here, one can notice that the synaptic equations are quite similar to HH type ionic channel equations. Therefore, a similar design strategy is followed during the circuit design.

Synchronization of AdEx neurons has been investigated in [73] for tonic spiking neurons for both excitatory and inhibitory coupling. To be in accordance with the results given in [73], we make numerical analysis firstly for tonic spiking neurons. Then we repeat the simulations for bursting neurons and show that the same synchronization behaviors occur. Besides, we replace the exponential expression in eq. (5.3) with the exponential approximation function in eq. (3.19) and observe completely the same outcomes. According to [73] we expect to see inphase behavior for excitatory coupling and antiphase behavior for inhibitory coupling.

Before circuit simulations, we give numerical simulation results. The correct way to observe synchronous behavior, initially the cells should oscillate independently and the coupling should be activated later. The initial state of phase difference should

also be set properly. For instance, if it is expected to see an inphase behavior after coupling, the initial phase difference must be different from 0°, and if possible, set to 180° as the worst case. Similarly, one should set initial phase difference close to 0°, if expecting an antiphase behavior.

The steady state activation function of the synaptic model is determined (with numerical simulation) as in eq. (5.4) and drawn in Figure 5.7 with dashed black line. The normalized excitatory synaptic currents for tonic spiking and bursting neurons are given in Figure 5.1. The excitatory coupling results are given in Figure 5.2 and Figure 5.3 and the inhibitory coupling results are also given in Figure 5.4 and Figure 5.5. In Figure 5.2-5.5, in (a) and (c), the neurons spike independently with an initial phase difference just before the coupling is activated. In (b) and (d), neurons spike synchronously after a sufficient time is passed from activation.

$$S_{\infty}(V_i) = 1 \Big/ \left\{ 1 + \exp\left(\frac{-35 - V_i)}{2.5} \right) \right\} \qquad \textbf{(5.4)}$$

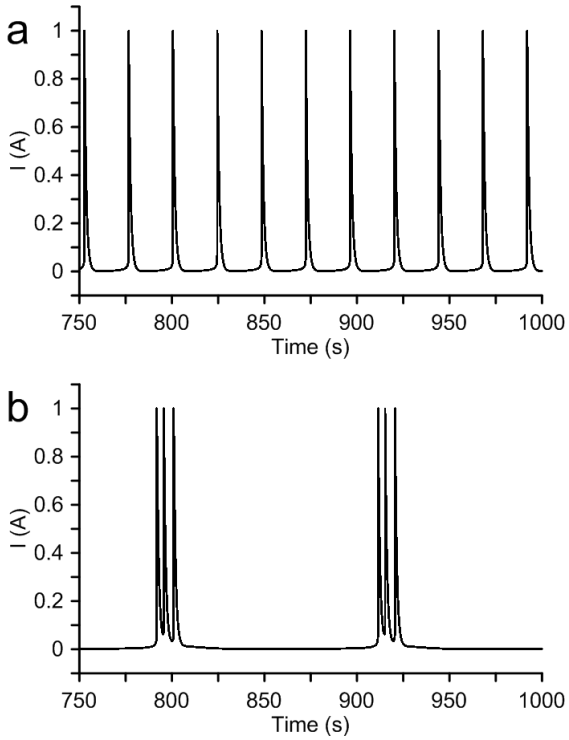

Figure 5.1 : Synaptic currents for: (a) tonic spiking and (b) bursting neurons, numerical simulation results.

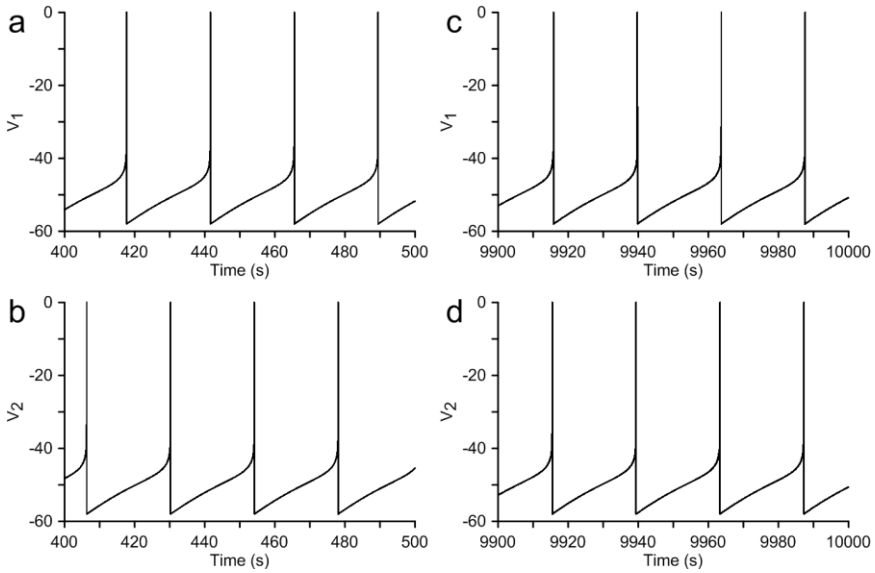

Figure 5.2 : Excitatory coupling results for tonic spiking. Initial state of (a) neuron 1, (b) neuron 2 and final state of (c) neuron 1, (d) neuron 2, numerical simulation results.

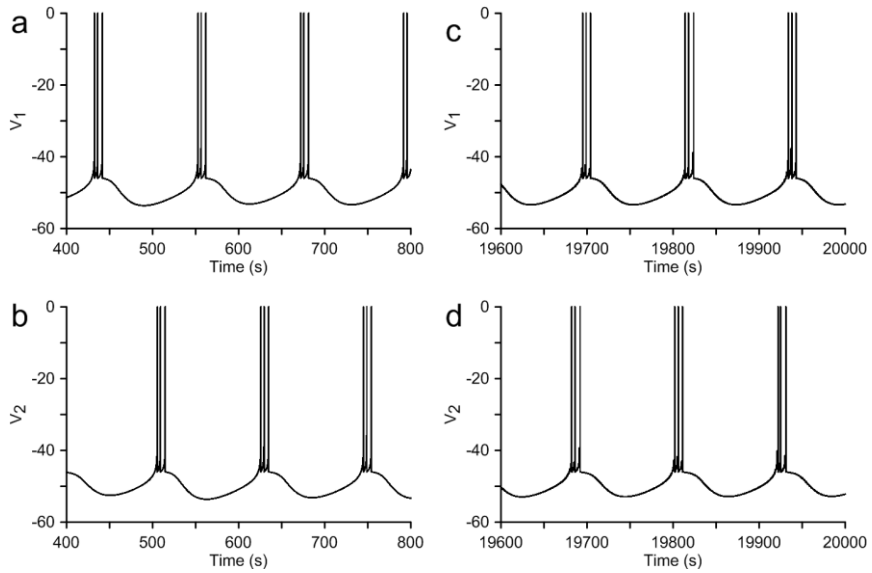

Figure 5.3 : Excitatory coupling results for bursting. Initial state of (a) neuron 1, (b) neuron 2 and final state of (c) neuron 1, (d) neuron 2, numerical simulation results.

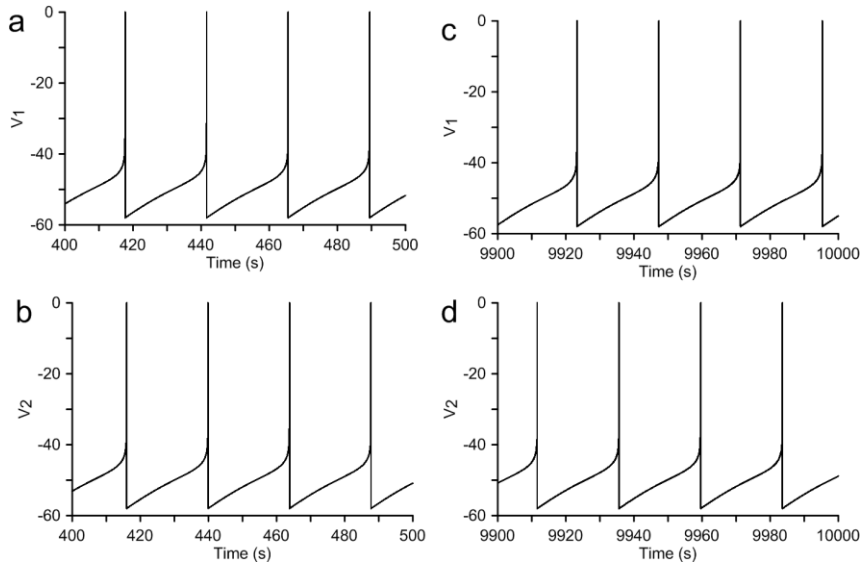

Figure 5.4 : Inhibitory coupling results for tonic spiking. Initial state of (a) neuron 1, (b) neuron 2 and final state of (c) neuron 1, (d) neuron 2, numerical simulation results.

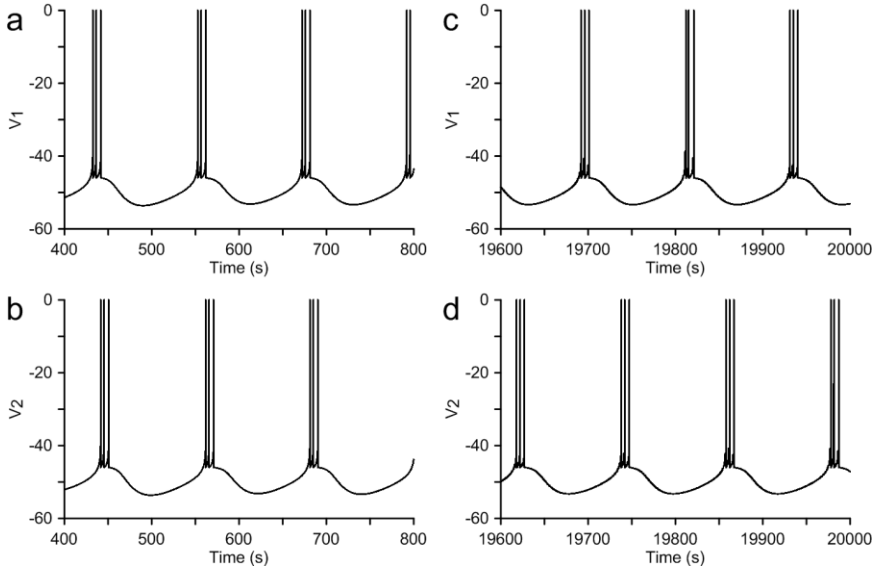

Figure 5.5 : Inhibitory coupling results for bursting. Initial state of (a) neuron 1, (b) neuron 2 and final state of (c) neuron 1, (d) neuron 2, numerical simulation results.

Before circuit realization, we rearrange the synaptic equations (5.1)-(5.4) for a proper log domain current mode operation. The final equation set is given below.

$$I_{syn}(N_i, N_j) = \frac{I_{S_i}(I_{E_{syn}} - I_j)}{1pA/g_{ij}} \tag{5.5}$$

$$\kappa C_{S_i} \frac{I_{S_i}}{dt} = -I_{S_i}\left((1pA) + (1pA)\exp\left(\frac{(I_i - I_{1/2})}{I_k}\right)\right)\kappa + (1pA)\exp\left(\frac{(I_i - I_{1/2})}{I_k}\right)\kappa \tag{5.6}$$

$$\exp\left(\frac{I_i - I_{1/2}}{I_k}\right) = \exp\left(\frac{I_i - 3.5pA}{0.25pA}\right) \rightarrow \frac{1}{(1pA)^3}\left(1pA + \frac{8pA(I_i - 3.5pA)}{\frac{(I_i - 6.5pA)^2}{1.5pA} + 2pA}\right)^4 \quad \textbf{(5.7)}$$

Then we realize the synaptic circuit realizing eq. (5.5) and (5.6) as shown in Figure 5.6 where a log domain filter corresponding to eq. (5.6) and a current multiplier circuit corresponding to eq. (5.5) are combined. Using similarity between eq. (5.5), eq. (5.6) and eq. (3.4), (3.5), it can be easily achieved that $I_{in-S} = exp\left(\frac{I_i - I_{1/2}}{I_k}\right)$, $\alpha I_{b-S} = (1pA)\kappa, \quad \alpha I_{d-S} = (1pA)\kappa + (1pA)\kappa \exp\left(\frac{(I_i - I_{1/2})}{I_k}\right)$, $I_{b-syn} = (I_{E_{syn}} - I_j)$ and $I_{d-syn} = 1pA/g_{ij}$. Here we choose $\kappa = \alpha$ for simplicity and therefore we reach $C_S = \kappa C_{S_i} \approx 40$ fF. Here it should be noted that, only one exponential circuit is enough to obtain the sigmoidal steady state and time constant functions together. The reason is that normalized forms of currents are,

$$\frac{1}{1 - S_\infty(x)} = 1 + \exp(x), \frac{S_\infty(x)}{1 - S_\infty(x)} = \exp(x) \quad \textbf{(5.8)}$$

resulting in eq. (5.6) with a single exponential term.

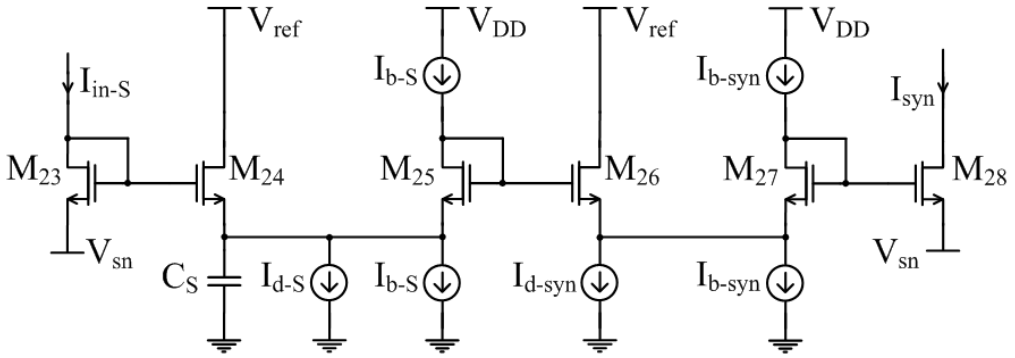

Figure 5.6 : The synaptic circuit for coupling AdEx neurons.

Next, we perform circuit simulations. Steady state activation function obtained from the synapse circuit is depicted in with a solid gray line, which shows an obvious agreement with the ideal function represented by the black dashed line. Additionally, the synaptic currents for tonic spiking and bursting neurons are given in Figure 5.8.

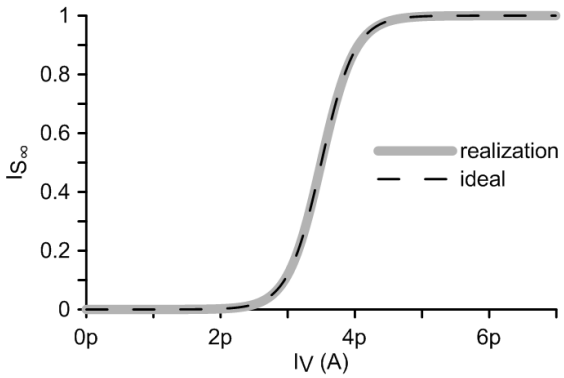

Figure 5.7 : Steady state activation functions of the synapse circuit.

To show the network dynamics, we couple neurons using two identical synapses as shown in figure 5.9. Firstly, we build the network with tonic spiking neurons and establish both excitatory and inhibitory coupling. Then we repeat the same simulation steps for bursting neurons. According to numerical simulation results demonstrated in Figure 5.2-5.5, inphase behavior is expected for excitatory coupling and antiphase behavior is expected for inhibitory coupling.

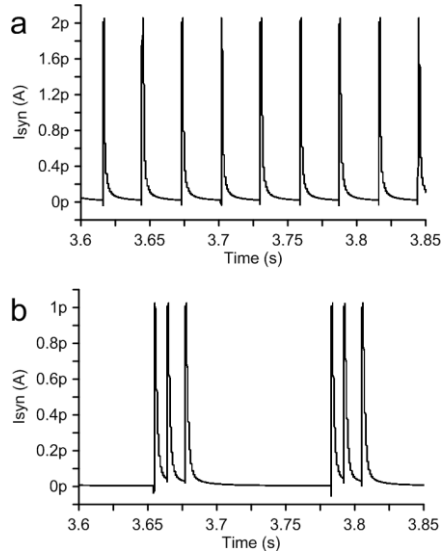

Figure 5.8 : Synaptic currents for tonic spiking and bursting neurons, circuit simulation results.

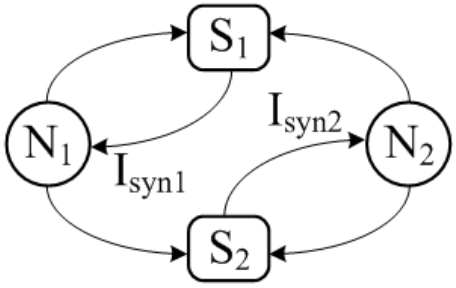

Figure 5.9 : Coupling diagram of AdEx neurons.

Throughout the first second of the simulation, neurons spike independently with an initial phase difference and then the coupling is activated. Since inphase behavior is expected for excitatory coupling, we set initial phase difference approximately 180° as the worst case. Similarly, we set initial phase difference approximately 0° for inhibitory coupling. Simulation results of the network behavior are given in Figure 5.10-5.13. As seen from these figures, all the results match with numerical simulation results in Figure 5.2-5.5.

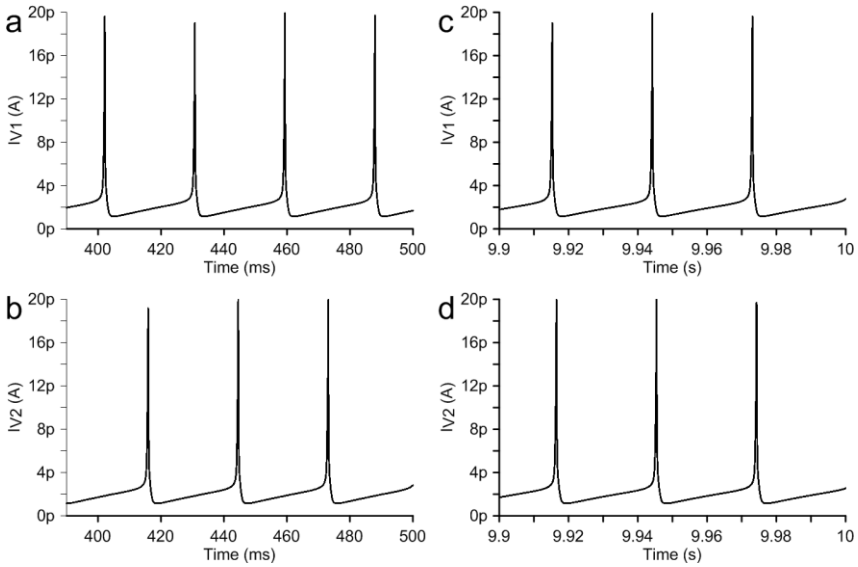

Figure 5.10 : Excitatory coupling results for tonic spiking. Initial state of (a) neuron 1, (b) neuron 2 and final state of (c) neuron 1, (d) neuron 2, circuit simulation results.

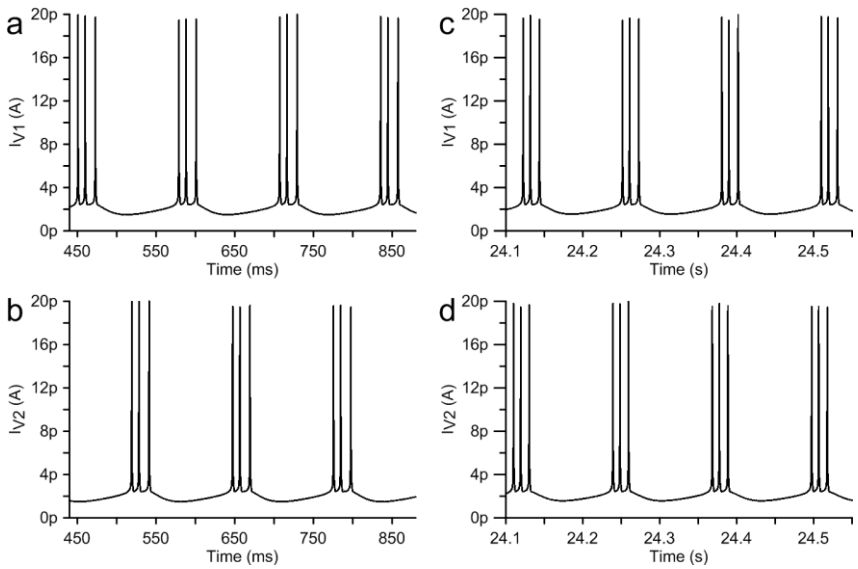

Figure 5.11 : Excitatory coupling results for bursting. Initial state of (a) neuron 1, (b) neuron 2 and final state of (c) neuron 1, (d) neuron 2, circuit simulation results.

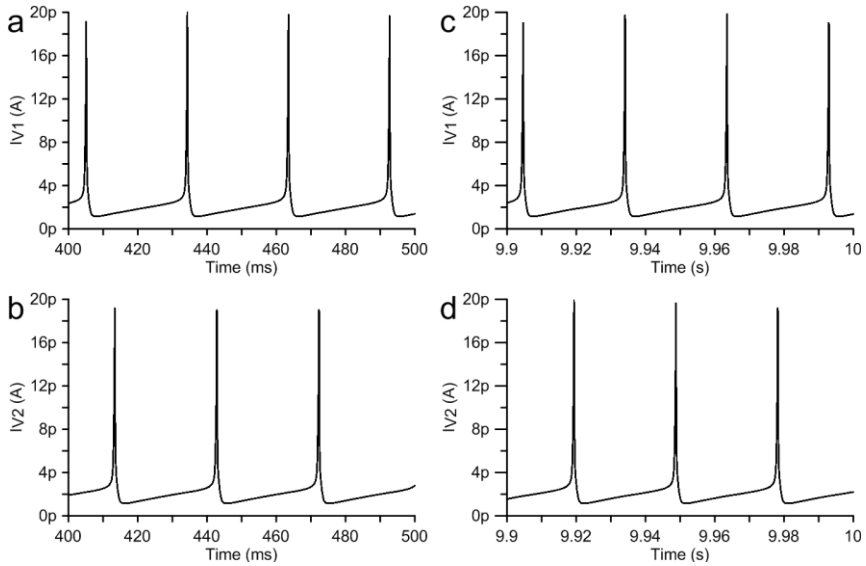

Figure 5.12 : Inhibitory coupling results for tonic spiking. Initial state of (a) neuron 1, (b) neuron 2 and final state of (c) neuron 1, (d) neuron 2, circuit simulation results.

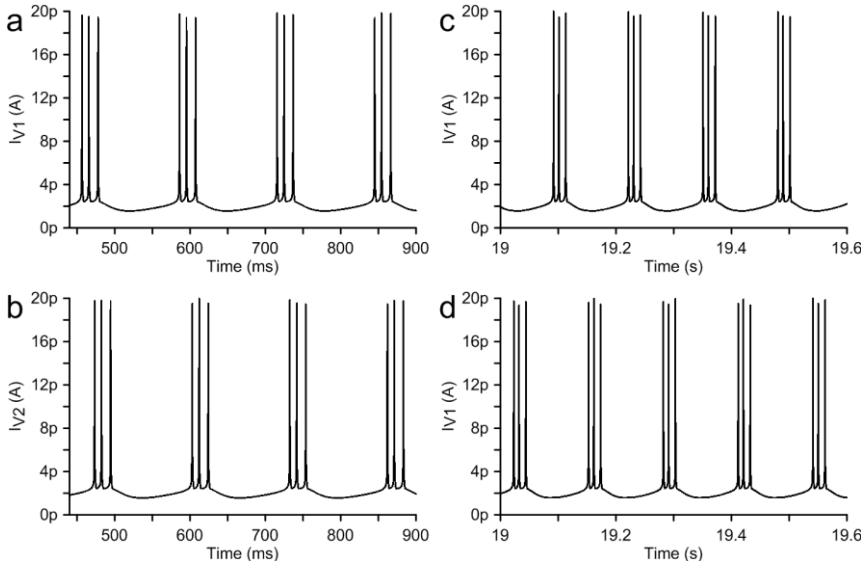

Figure 5.13 : Inhibitory coupling results for bursting. Initial state of (a) neuron 1, (b) neuron 2 and final state of (c) neuron 1, (d) neuron 2, circuit simulation results.

5.2 Three Coupled Izhikevich Neurons

In this part, we couple three Izh neurons in order to observe network dynamics. The synaptic model is the same used in the previous part where eq. (5.3) was inserted into eq. (5.2) in order to reach eq. (5.6). Now, we express eq. (5.6) in an implicit form in eq. (5.9) once again.

$$\tau_S \frac{I_{S_i}}{dt} = -I_{S_i} \frac{1}{(1 - S_\infty)} + \frac{S_\infty}{(1 - S_\infty)} (1pA) \qquad \textbf{(5.9)}$$

Instead of realizing the exact equation of eq. (5.3) utilizing an exponential circuit, we make a simplification in terms of circuit realization. Since the spike signal is a pulse like signal, we prefer to use the V_{reset} voltage signal instead of the original current variable spike signal in order to generate the sigmoid function easily utilizing a simple differential pair. The complete synapse circuit is given in figure 5.14.

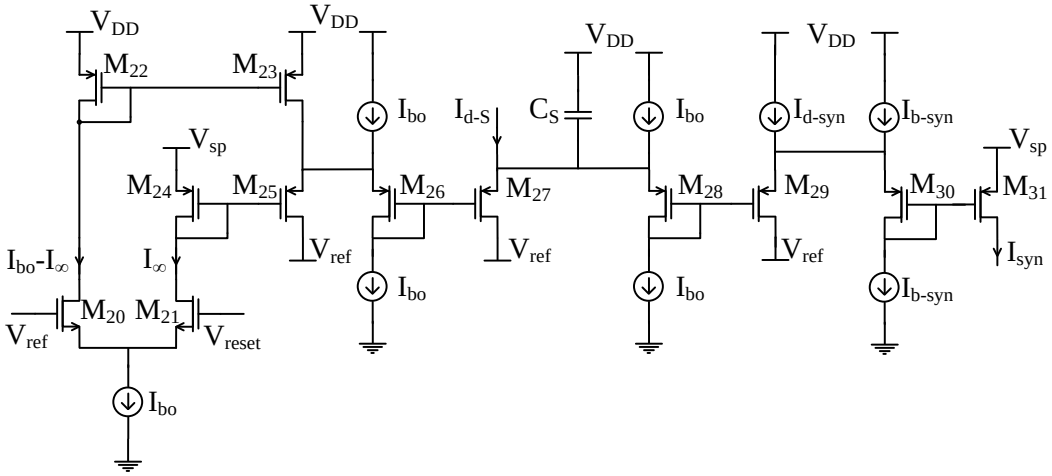

Figure 5.14 : The synaptic circuit for coupling Izh neurons.

The transistors M_{20} and M_{21} with I_{bo} current source form the differential pair the branch current of which is given by eq. (5.10) matching eq. (5.3).

$$I_\infty = \frac{I_{bo}}{1 + \exp(\alpha(V_{reset} - V_{ref}))} \qquad \textbf{(5.10)}$$

To realize (5.10), we combine a translinear current multiplier loop composed of M_{24}-M_{27} and a log domain filter composed of M_{26}-M_{29}. Here $I_{d\text{-}S}$ is equal to $\frac{{I_{bo}}^2}{(I_{bo} - I_\infty)}$ generated by a translinear current multiplier loop not shown in the figure 5.14 for simplicity. The output of log domain filter is also combined with a second translinear current multiplier loop composed of M_{28}-M_{31} in order to realize eq. (5.1). Here $I_{d\text{-}syn}$ is equal to $1pA/g_{ij}$ and $I_{b\text{-}syn}$ is equal to $(I_{E_{syn}} - I_j)$. We also want to note that the synaptic activity current I_S does not appear directly but appear indirectly as a voltage signal at the gate of M_{28}. Simplification of the synapse results in an estimated chip area of 130 μm^2.

The synaptic output currents for inputs of regular spiking and bursting are given in Figure 5.15. We adjust the peak of the synaptic current to 0.5 pA in order to obtain a weakly coupling between neurons. When the input spikes arrive to the synapse frequently such as a bursting pattern, the synapse integrates the inputs linearly according to eq. (5.1)-(5.3) suggesting that simplification of eq. (5.3) does not affect the results.

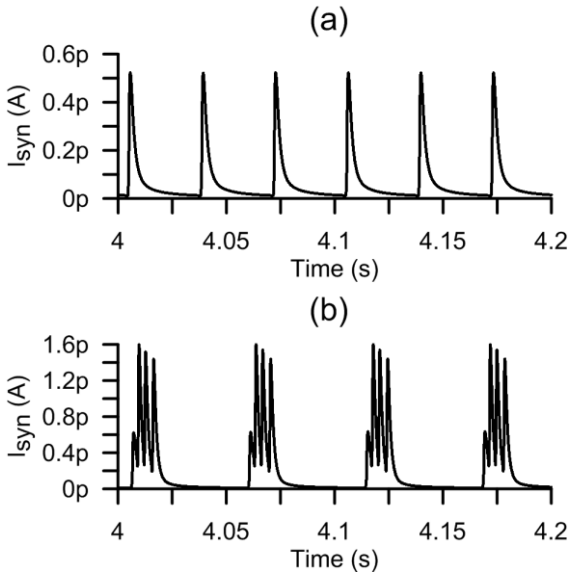

Figure 5.15 : Synaptic currents for inputs of (a) regular spiking and (b) bursting.

In order to show that the neuron designed can exhibit network dynamics, we couple three neurons (n=3) according to the network coupling diagram given in Figure 5.16.

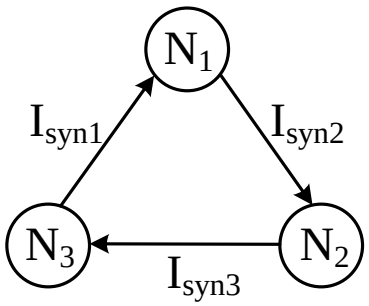

Figure 5.16 : Network coupling diagram of Izh neurons.

We investigate the network dynamics for both regular spiking and bursting behavior. Similar to AdEx network, we create both excitatory and inhibitory coupling and expect to see inphase synchronization, i.e. 0° difference, for excitatory coupling and n-phase synchronization, i.e. 120° phase difference, for inhibitory coupling [74]. Firstly, we make the neurons oscillate independently with proper initial phase differences and activate coupling after the first second of the simulation. After a

sufficient time, we observe the type of synchronization. Additionally, we consider the worst case to determine the initial phases. For instance, if we expect n-phase synchronization, we set almost no initial phase difference between neurons and vice versa.

Simulation results of the network dynamics is given in Figure 5.17 to Figure 5.20. Left column of the figures are initial states of the neurons while the right columns are representing the final synchronized states.

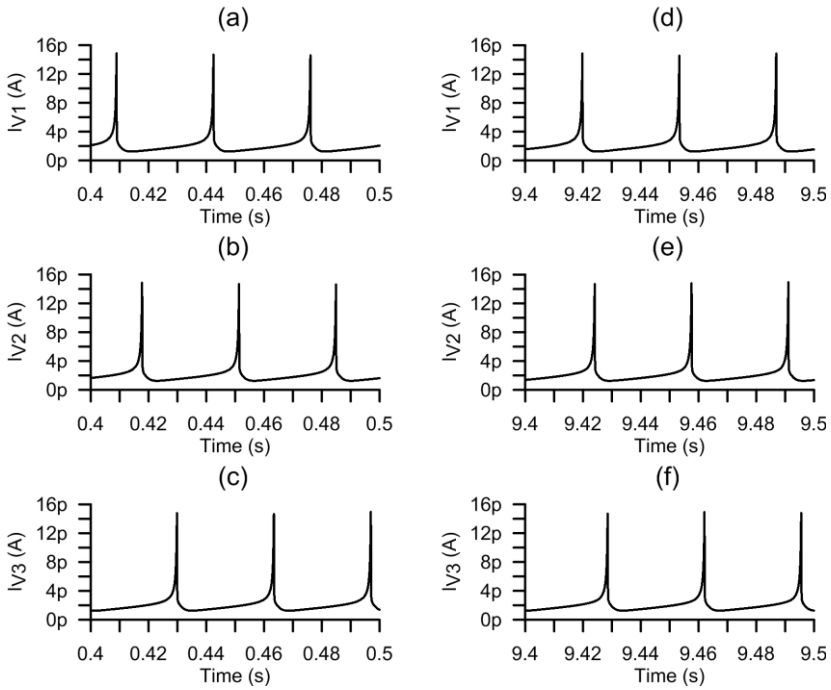

Figure 5.17 : Excitatory coupling results for regular spiking. Initial state of (a) neuron 1, (b) neuron 2, (c) neuron 3, and final state of (d) neuron 1, (e) neuron 2, (f) neuron 3.

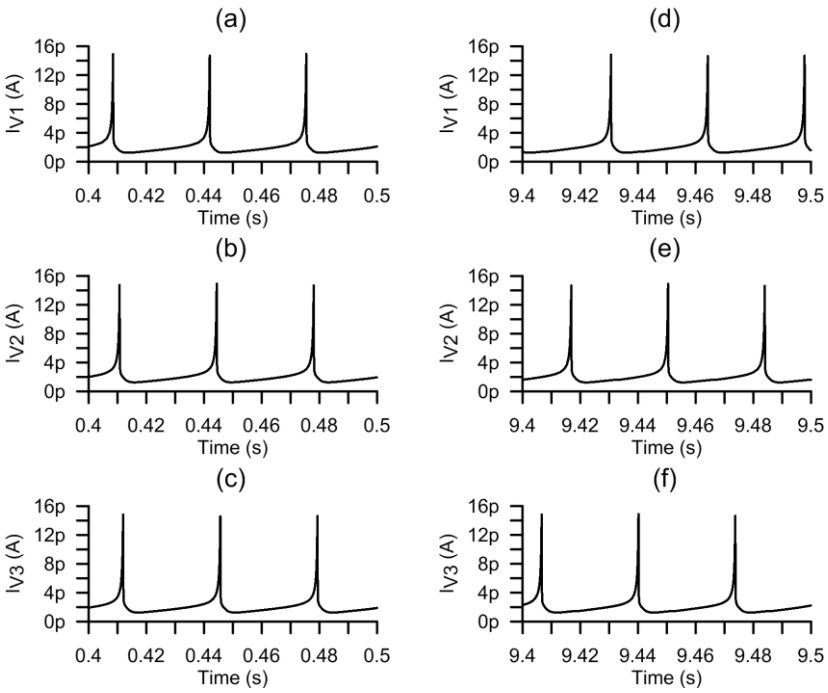

Figure 5.18 : Inhibitory coupling results for regular spiking. Initial state of (a) neuron 1, (b) neuron 2, (c) neuron 3, and final state of (d) neuron 1, (e) neuron 2, (f) neuron 3.

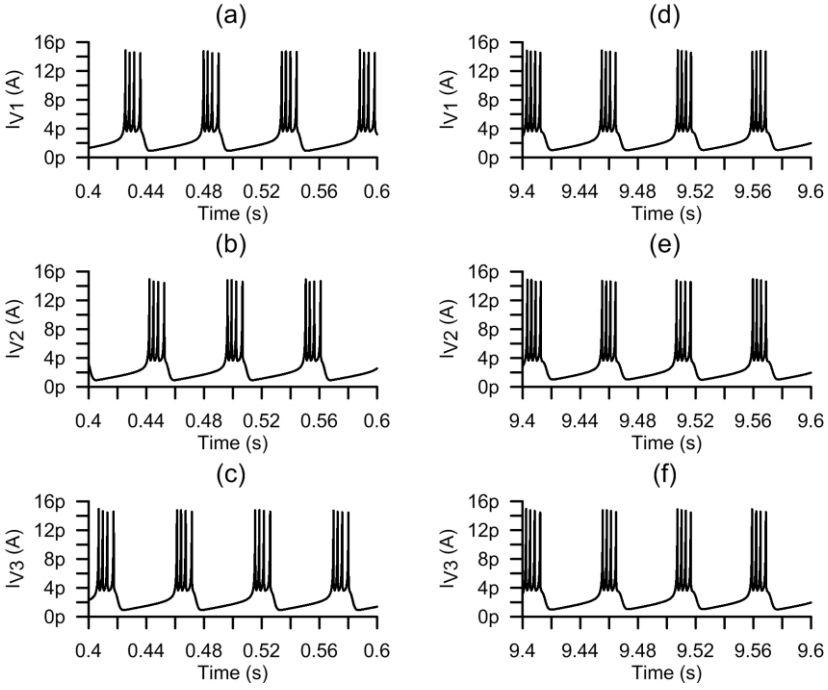

Figure 5.19 : Excitatory coupling results for bursting. Initial state of (a) neuron 1, (b) neuron 2, (c) neuron 3, and final state of (d) neuron 1, (e) neuron 2, (f) neuron 3.

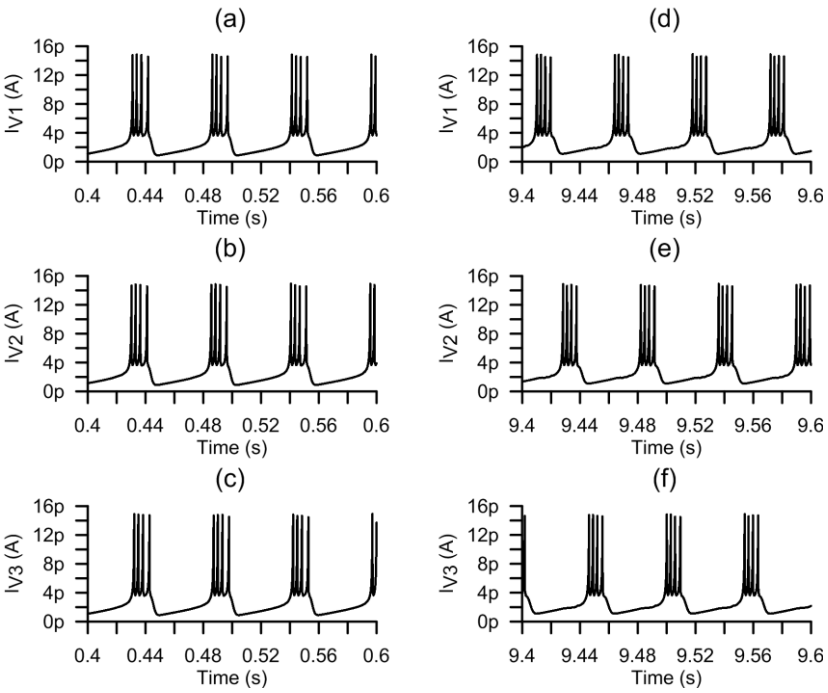

Figure 5.20 : Inhibitory coupling results for bursting. Initial state of (a) neuron 1, (b) neuron 2, (c) neuron 3, and final state of (d) neuron 1, (e) neuron 2, (f) neuron 3.

To emphasize n-phase behavior, we set inhibitory coupling between nine neurons in the same ring structure given in Figure 5.9. For ring structure networks involving even numbers of neurons, it expected to see antiphase behavior between neighbor neurons for inhibitory coupling. However, when there are odd numbers of neurons, the phase difference cannot be exactly 180° due to the boundary condition of the ring structure [74]. Therefore, a phase shift occurs where it is easier to observe this behavior for increased number of neurons. The simulation results for regular spiking neurons are given in Figure 5.21. It can be seen that the phase difference between the neighbor neurons are slightly different from 180°. Moreover, there exists a phase shift among even and odd numbered neurons and each other resulting in a travelling wave. To illustrate this, only the behavior odd numbered neurons are given in Figure 5.22. Note that the phase difference of the first and ninth neuron is close to 180° in the figure. We replace regular spiking neurons with bursting neurons and repeat the simulations. To better illustrate n-phase behavior, we only give the behavior of odd numbered neurons in Figure 5.23.

Differently from the AdEx network, we observe n-phase behavior by increasing the number of coupled neurons successfully. Besides, the simplified synaptic circuit also allows a compact and low power design.

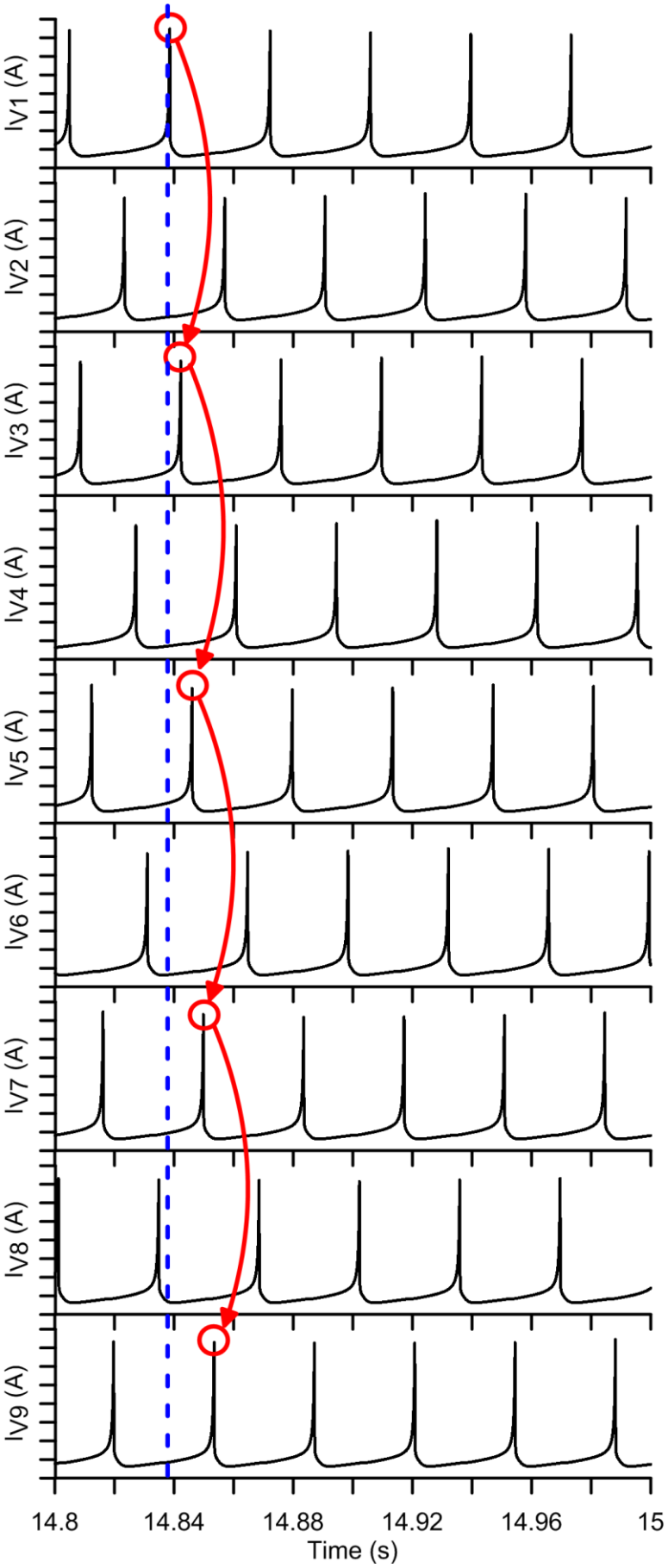

Figure 5.21 : Final state of nine regular Izh spiking neurons.

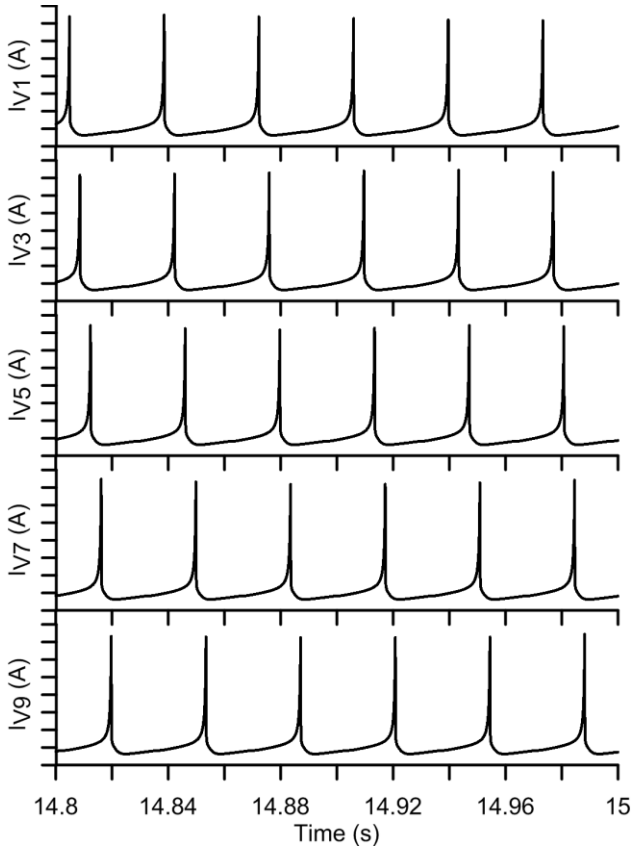

Figure 5.22 : Final state of odd numbered Izh regular spiking neurons.

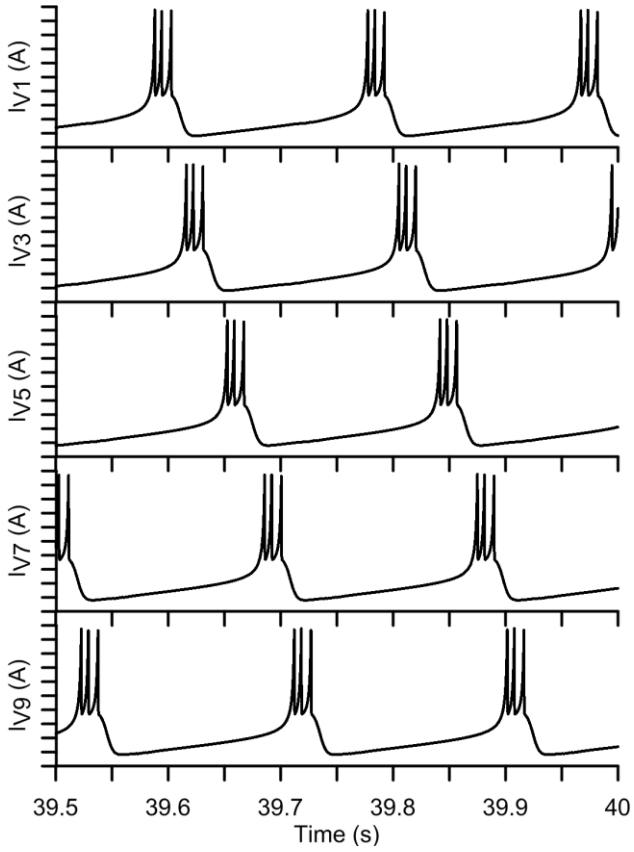

Figure 5.23 : Final state of odd numbered Izh bursting neurons.

6. CONCLUSION

In this thesis, three low power and compact VLSI neurons, operating at biological timescale, are designed. Each neuron circuit realizes a mathematical neuron model. The models utilized are namely Izhikevich (Izh), Adaptive Exponential Integrate and Fire (AdEx) and Hodgkin-Huxley (HH) neuron model. Additionally, two synaptic circuits with temporal dynamics are realized. Using these synaptic circuits, two AdEx neurons and three Izhikevich neurons are coupled between each other forming small networks.

The Izh model and AdEx model are, recently introduced, quiet similar models. Both are dynamically rich and computationally efficient models. They only involve four parameters and two variables resulting in a simple electronic realization. On the other side, despite its complex form, the HH neuron model is the only model that is biophysically meaningful. An accurate implementation of such mathematical neuron models creates an opportunity to compare the results with numerical solutions and come up with a robust and successful design. Therefore, we prefer to implement these three mathematical neuron models.

A low power and compact neuron circuit allows designing large-scale neural networks including massive number of neurons. Using a large-scale network one can investigate computational properties of the utilized mathematical models or one can design brain-like performing systems. Besides, the real time operation property allows designing real time experiment hardware tools or human-machine interface systems. Thus, our strategy is to design low power and compact real time neurons.

Due to low power and compactness strategy, all the three neurons are designed with log domain circuits operating in subthreshold region with current mode approach. Basic building blocks of the neurons are first order log domain filter and the translinear loop current multiplier/divider circuit. The variables take values in pA range and the values of the bias current are in fA range. To handle such low current

values at a few ten of Hertz frequency, we make use of source shifting and active diode connection techniques in the neuron circuits.

The neuron circuits are simulated using 0.15 µm CMOS process parameters using Spectre in Cadence design tool. Supply voltage is V_{DD}=1.5V and amount of source shifting is 300 mV. The Izh neuron occupies 275 μm^2 chip area and power consumption is 249 pW and 270 pW for resting state and regular spiking state, respectively. The neuron is showed to exhibit both Class I and Class II behaviors. The AdEx neuron occupies 490μm^2 chip area and power consumption is 462 pW and 9.3 nW for resting state and regular spiking state, respectively. Both of the neurons produce various firing patterns by tuning the parameters. The similarity between these patterns and numerical simulation results are remarkable. The AdEx neuron consumes much power due to the exponential circuit during the resetting phase. A HH neuron is also designed as a current mode prototype. It occupies 1200 μm^2 chip area and power consumption is 3.4 nW and 3.57 nW for resting state and regular spiking state, respectively. The action potential generated matches with numerical simulation results.

To implement pA and fA current sources, a current reference circuit is required. Therefore, a CMOS only, wide temperature range, pA level current reference circuit is designed. The circuit is based on a well-known topology but the core of it involves serially connected transistors. The offset voltage generating and temperature compensating currents are injected into internal nodes of these serial transistors improving the behavior of the circuit. As a result, a reference current of 519 pA with a very low TC of 57 ppm/°C over a wide temperature range (-40°C,+120°C) has been obtained. For a better evaluation of reference circuits, Monte Carlo analysis is performed. We run 800 simulations and obtain a TC value of 147 ppm/°C. The mean value of reference current is 519 pA with $\sigma/\mu = \%4.3$. We want to note that, directly simulating the circuit in Figure 3.7 gives a TC value of 39 ppm/°C for a single simulation but 300 ppm/°C after a Monte Carlo analysis. The fA level current sources are obtained using a simplified current splitter circuit rather than a M2M ladder. Due to the feedback mechanism in the splitter circuit, a stable output current is obtained independent from process and temperature fluctuations. We obtain 50 fA and 500 fA DC current sources within a temperature range of (-40 °C, +60 °C) while 5pA and 50 pA DC current sources are obtained in the range of (-40 °C, +120 °C).

In order to realize the exponential term in AdEx model, a wide range current mode exponential circuit is designed. For this purpose, Pade (2, 2) approximation function is exploited rather than the traditional Taylor approximation. The exponential circuit is mainly composed of translinear loop current multiplier/divider circuits. As a result, an output range of 43.4 dB is obtained with 0.2 dB error for nominal case and 0.5 dB error for the worst case.

In the last section of the thesis, two similar synaptic circuits, both of which operate linearly with temporal dynamics, are designed. The synaptic model involves a first order differential equation with sigmoidal steady state and time constant functions. In the first synaptic circuit, these functions are realized using exponential circuit. In the second synaptic circuit, the sigmoidal functions are realized with a simple differential pair as a simplification. The rest of the circuits are composed of first order log domain filter and translinear loop current multiplier/divider circuits again. Two AdEx and three Izh neurons are coupled among each other. To investigate the synchronization activity of the network we set excitatory and inhibitory coupling between neurons. The observed synchronization patterns are inphase (zero phase difference) behavior for excitatory coupling, antiphase (180° phase difference) behavior for inhibitory coupling and n-phase (arbitrary phase difference) behavior. N-phase behavior was obtained for n=3 and n=9. We successfully observe the expected patterns in both of the networks. Therefore, it is concluded that the neurons can exhibit network dynamics successfully.

As a future work, the magnitude of the current values and operation speed of the circuits mentioned in this thesis can easily be scaled up just by altering the bias current values, without corrupting the dynamical behavior of the circuits. This way, depending on the performance of the bias current generator circuit, it becomes feasible to fabricate prototype circuits with low area and low power consumption. A digitally controllable current generator circuit will also result in controllable neuron and synaptic circuits. Thus, it will be possible to build configurable VLSI neural networks. Lastly, the computational modeling of very large scale neural networks utilizing smaller size networks and their VLSI realization will result in hardware emulators for experimental scientists and/or real time interface circuits.

REFERENCES

[1] **Mead, C. A.** (1989). *Analog VLSI and neural systems*: Addison-Wesley.

[2] **Linares-Barranco, B., Sanchez-Sinencio, E., Rodriguez-Vazquez, A., Huertas, J. L.** (1991). A CMOS Implementation of FitzHugh-Nagumo Neuron Model. *IEEE Journal of Solid State Circuits, 26*, 956–965.

[3] **Dupeyron, D., Le Masson, S., Deval, Y., Le Masson, G., & Dom, J. P. P.** (1996). A BiCMOS implementation of the Hodgkin-Huxley formalism. *Proceedings of Fifth International Conference on Microelectronics for Neural Networks,* (pp. 1784-1787).

[4] **Patel, G. N., DeWeerth**, **S. P.** (1997). Analogue VLSI Morris Lecar Neuron. *Electronic Letters*, *33*, 997-998.

[5] **Arena, P., Fortuna, L., Frasca, M.** (2000). Extended SC-CNN Implementation of the Hindmarsh-Rose Neuron. *IEEE Int. Workshop on CNN and Their App. Proc.*, 339-344.

[6] **Nakada, K., Asai, T., Hayashi, H.** (2005). A Silicon Resonate-and-Fire Neuron Based on the Volterra System. *NOLTA*, 82-85.

[7] **Lazaridis, E., Drakasis, E. M., Barahoma, M.** (2007). Full analogue electronic realization of the Hodgkin-Huxley neuronal dynamics in weak-inversion CMOS. *EMBS*, 1200-1203.

[8] **Arthur, J. V., Boahen, A. K**. (2007). Synchrony in Silicon: The Gamma Rhythm. *IEEE Transactions on Neural Networks, 18*, 1815-1825.

[9] **Wijekoon, J. H. B., Dudek, P.** (2008). Integrated Circuit Implementation of a Cortical Neuron. *ISCAS*, 1784-1787.

[10] **Folowosele, F., Harrison, A., Cassidy, A. S., Andreou, A. G., Etienne-Cummings, R. R., Mihalas, S., et al.** (2009). A switched capacitor implementation of the generalized linear integrate-and-fire neuron. *ISCAS*, 2149-2152.

[11] **Yu, T., Cauwenberghs, G.** (2009). Biophysical synaptic dynamics in an analog VLSI network of Hodgkin-Huxley neurons. *EMBC* 3335-3338.

[12] **Ma, Q., Haider, M. R., Shrestha, V. L., Massoud, Y.** (2012). Bursting Hodgkin–Huxley model-based ultra-low-power neuromimetic silicon neuron. *Analog Integrated Circuits and Signal Processing, 73*, 329–337.

[13] **Hill, S., Markram, H.** (2008). The Blue Brain Project. *EMBS*, 158-158.

[14] **Andreou, A. G., Boahen, K. A., Pouliquen, P. O., Pavasovic, A., Jenkins, R. E., Strohbehn, K.** (1991). Current-mode subthreshold MOS circuits

for analog VLSI neural systems. *IEEE Transactions on Neural Networks*, *2*, 205-213.

[15] **Izhikevich, E. M**. (2007). *Dynamical Systems in Neuroscience: The Geometry of Excitability and Bursting.* The MIT press.

[16] **Bartolozzi, C., Indiveri, G.** (2007). Synaptic dynamics in analog VLSI. *Neural Comput., 19,* 2581–2603.

[17] **Gerstner W., Kistler W. M.** (2002). *Spiking Neuron Models*. Cambridge University Press.

[18] **Sterratt, D., Graham B., Gillies, A., Willshaw, D.** (2011). *Principles of Computational Modelling in Neuroscience*. Cambridge University Press.

[19] **Izhikevich, E. M.** (2004). Which model to use for cortical spiking neurons?. *IEEE Transactions on Neural Networks, 15,* 1063-1070.

[20] **Brunel, N., Van Rossum, M. C.** (2007). Lapicque's 1907 paper: from frogs to integrate-and-fire. *Biological cybernetics*, *97*, 337-339.

[21] **Izhikevich, E. M., FitzHugh, R.** (2006). Fitzhugh-Nagumo model. *Scholarpedia*, *1*(9), 1349.

[22] **Corson, N., Aziz-Alaoui, M. A.** (2008). Dynamics and complexity of Hindmarsh-Rose neuronal systems. *EPNACS.*

[23] **Izhikevich, E. M**. (2003). Simple model of spiking neurons. *IEEE Transactions on Neural Networks*, *14*, 1569-1572.

[24] **Touboul J.** (2009). Importance of the cutoff value in the quadratic adaptive integrate-and-fire model. *Neural Computation, 21*, 2114-2122.

[25] **Izhikevich, E. M.** (2010). Hybrid Spiking Models. *Philosophial Transactions of The Royal Society A, 368*, 5061-5070.

[26] **Brette, R., Gerstner, W.** (2005). Adaptive exponential integrate-and-fire model as an effective description of neuronal activity. *Journal of neurophysiology, 94*, 3637-3642.

[27] **Naud, R., Marcille, N., Clopath, C., & Gerstner, W.** (2008). Firing patterns in the adaptive exponential integrate-and-fire model. *Biological Cybernetics*, *99*, 335-347.

[28] **Badel, L., Lefort, S., Brette, R., Petersen, C. C. H., Gerstner, W., & Richardson, M. J. E.** (2008). Dynamic I-V Curves Are Reliable Predictors of Naturalistic Pyramidal-Neuron Voltage Traces. *Journal of Neurophysiology, 99*, 656-666.

[29] **Touboul J., & Brette R**. (2008). Dynamics and bifurcations of the adaptive exponential integrate-and-fire model. *Biological Cybernetics*, *99*, 319-334.

[30] **Touboul J.** (2008). Bifurcation Analysis of a General Class of Nonlinear Integrate-and-Fire Neurons. *SIAM Journal on Applied Mathematics, 68*, 1045-1079.

[31] **Izhikevich, E. M.** (2001). Resonate-and-fire neurons. *Neural networks*, *14*, 883-894.

[32] **Lecar, H.** (2007). Morris-lecar model. *Scholarpedia*, *2*(10), 1333.

[33] **Taur, Y., Ning, T. H.** (1998). *Fundamentals of modern VLSI devices*. *2*, Cambridge University Press.

[34] **Linares-Barranco, B., Serrano-Gotarredona, T., Serrano-Gotarredona, R., & Serrano-Gotarredona, C.** (2004). Current Mode Techniques for Sub-pico-Ampere Circuit Design. *Analog Integrated Circuits and Signal Processing*, *38*, 103-119.

[35] **Oguey, H. J., Aebischer, D.** (1997). CMOS current reference without resistance. *IEEE Journal of Solid-State Circuits*, *32*, 1132-1135.

[36] **De Vita, G., Iannaccone, G.** (2007). A 109 nW, 44 ppm/°C CMOS Current Reference with Low Sensitivity to Process Variations. *ISCAS 2007*, 3804-3807.

[37] **Hirose, T., Osaki, Y., Kuroki, N., Numa, M.** (2010). A nano-ampere current reference circuit and its temperature dependence control by using temperature characteristics of carrier mobilities. *ESSCIR*, 114-117.

[38] **Ueno, K., Hirose, T., Asai, T., Amemiya, Y.** (2010). A1-μW 600-ppm/℃ Current Reference Circuit Consisting of Subthreshold CMOS Circuits. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *57*, 681-685.

[39] **Wei, Y., Xin, T., Wenhong, L., Ran, L.** (2011). A resistorless CMOS current reference with temperature compensation. *Journal of Semiconductors*, *32*, 035006.

[40] **Huang, Z., Luo, Q., Inoue, Y.** (2010). A CMOS Sub-l-V nanopower current and voltage reference with leakage compensation. *ISCAS*, 4069-4072.

[41] **Camacho-Galeano, E. M., Galup-Montoro, C., Schneider, M. C.** (2005). A 2-nW 1.1-V self-biased current reference in CMOS technology. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *52*, 61-65.

[42] **Zhao, C., Geiger, R., Chen, D**. (2012). A compact low-power supply-insensitive CMOS current reference. *ISCAS* 2825-2828.

[43] **Osaki, Y., Hirose, T., Kuroki, N., Numa, M**. (2010). Nano-ampere CMOS current reference with little temperature dependence using small offset voltage. *MWSCAS*, 668-671.

[44] **Olmos, A., Vilas Boas, A., Soldera, J**. (2007). A sub-1V low power temperature compensated current reference. *ISCAS*, 2164-2167.

[45] **Zhang, L., Yu, Z., He, X.** (2006). Circuit Design and Verification of On-Chip Femto-Ampere Current Mode Circuit Using 0.18μm CMOS Technology. *ICSICT* 1624-1626.

[46] **Mizuno, K., Ohta, N., Kitagawa, F., Nagase, H.** (1998). Analog CMOS integrated circuits for high-temperature operation with leakage current compensation. *HITEC*. 41-44.

[47] **Delbruck, T., Berner, R., Lichtsteiner, P., Dualibe, C.** (2010). 32-bit configurable bias current generator with sub-off-current capability. *ISCAS*, 1647-1650.

[48] **Saatlo, A. N., Ozoguz, S.** (2011). A new CMOS exponential circuit with extended linear output range. *ECCTD*, 893-896.

[49] **Maundy, B., Gift, S.** (2005). Novel pseudo-exponential circuits. *IEEE Transactions on Circuits and Systems II: Express Briefs, 52*, 675-679.

[50] **Kao, C. H., Tseng, C. C., Hsieh, C. S.** 2005. Low-voltage exponential function converter. *IEE Proceedings- Circuits, Devices and Systems, 152*, 485-487.

[51] **Duong, Q. H., Nguyen, T. K., Lee, S. G.** (2003). Low-voltage low-power high dB-linear CMOS exponential function generator using highly-linear V-I converter. *ISLPED*, 349-352.

[52] **Indiveri, G., Linares-Barranco, B., Hamilton, T. J., Van Schaik, A., Etienne-Cummings, R., Delbruck, T., et al.** (2011). Neuromorphic silicon neuron circuits. *Frontiers in neuroscience, 5*.

[53] **Livi, P., Indiveri, G.** (2009). A current-mode conductance-based silicon neuron for address-event neuromorphic systems. *ISCAS*, 2898-2901.

[54] **Wijekoon, J. H., Dudek, P.** (2009). A CMOS circuit implementation of a spiking neuron with bursting and adaptation on a biological timescale. *BioCAS*, 193-196.

[55] **Van Schaik, A., Jin, C., McEwan, A., Hamilton, T. J**. (2010). A log-domain implementation of the Izhikevich neuron model. *ISCAS*, 4253-4256.

[56] **Rangan, V., Ghosh, A., Aparin, V., Cauwenberghs, G**. (2010). A subthreshold aVLSI implementation of the Izhikevich simple neuron model. *EMBC*, 4164-4167.

[57] **Millner, S., Grübl, A., Meier, K., Schemmel, J., Schwartz, M. O.** (2010). A VLSI implementation of the adaptive exponential integrate-and-fire neuron model. *Advances in Neural Information Processing Systems, 23*, 1642-1650.

[58] **Schemmel, J., Bruderle, D., Grubl, A., Hock, M., Meier, K., Millner, S.** (2010). A wafer-scale neuromorphic hardware system for large-scale neural modeling. *ISCAS*, 1947-1950.

[59] **Yu, T., Cauwenberghs, G.** (2010). Analog VLSI Biophysical Neurons and Synapses With Programmable Membrane Channel Kinetics. *IEEE Transactions on Biomedical Circuits and Systems, 4*, 139-148.

[60] **Hynna, K. M., Boahen, K. A.** (2003). A silicon implementation of the thalamic low threshold calcium current. *EMBS*, 2228-2231.

[61] **Hynna, K. M., Boahen, K.** (2006). Neuronal ion-channel dynamics in silicon. *ISCAS*, 3614-3617.

[62] **Farquhar, E., Hasler, P.** (2005). A bio-physically inspired silicon neuron. *IEEE Transactions on Circuits and Systems I: Regular Papers, 52*, 477-488.

[63] **Simoni, M. F., Cymbalyuk, G. S., Sorensen, M. E., Calabrese, R. L., DeWeerth, S. P.** (2004). A multiconductance silicon neuron with biologically matched dynamics. *IEEE Transactions on Biomedical Engineering, 51*, 342-354.

[64] **Saighi, S., Tomas, J., Bornat, Y., Renaud, S**. (2005). A conductance-based silicon neuron with dynamically tunable model parameters. *EMBS* 285-288.

[65] **Zou, Q., Bornat, Y., Tomas, J., Renaud, S., Destexhe, A.** (2006). Real-time simulations of networks of Hodgkin–Huxley neurons using analog circuits. *Neurocomputing*, *69*, 1137-1140.

[66] **Tomas, J., Bornat, Y., Saighi, S., Levi, T., Renaud, S.** (2006). Design of a modular and mixed neuromimetic ASIC. *ICECS*, 946-949.

[67] **Renaud, S., Tomas, J., Bornat, Y., Daouzli, A., Saïghi, S**. (2007). Neuromimetic ICs with analog cores: an alternative for simulating spiking neural networks. *ISCAS*, 3355-3358.

[68] **Saïghi, S., Buhry, L., Bornat, Y., N'Kaoua, G., Tomas, J., Renaud, S.** (2008). Adjusting the neurons models in neuromimetic ICs using the voltage-clamp technique. *ISCAS*, 1564-1567.

[69] **Buhry, L., Saïghi, S., Ben Salem, W., Renaud, S.** (2009). Adjusting neuron models in neuromimetic ICs using the Differential Evolution algorithm. *EMBS*, 681-684.

[70] **Saïghi, S., Bornat, Y., Tomas, J., Le Masson, G., Renaud, S.** (2011). A library of analog operators based on the Hodgkin-Huxley formalism for the design of tunable, real-time, silicon neurons. *IEEE Transactions on Biomedical Circuits and Systems*, *5*, 3-19.

[71] **Demirkol, A. S., Ozoguz, S.** (2011). A low power VLSI implementation of the Izhikevich neuron Model. *NEWCAS*, 169-172.

[72] **Lee, Y. J., Lee, J., Kim, K. K., Kim, Y. B., Ayers, J**. (2007). Low power CMOS electronic central pattern generator design for a biomimetic underwater robot. *Neurocomputing*, *71*, 284-296.

[73] **Ladenbauer, J., Augustin, M., Shiau, L., Obermayer, K.** (2012). Impact of adaptation currents on synchronization of coupled exponential integrate-and-fire neurons. *PLoS computational biology*, *8*, e1002478.

[74] **Uwate, Y., Nishio, Y., Stoop, R**. (2010). Complex pattern in a ring of van der Pol oscillators coupled by time-varying resistors. *Journal of Circuits, Systems, and Computers*, *19*, 819-834.

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List of Publications:

Vedat Tavas, **A. Samil Demirkol**, Serdar Ozoguz, Ali Zeki, Ali Toker, "An ADC Based Random Bit Generator Based on a Double Scroll Chaotic Circuit", *J. Circuits, Systems and Computers*, Vol.19 No.7,pp1621-1639, 2010.

Ali Oksasoglu, Serdar Ozoguz, **A. Samil Demirkol**, Tayfun Akgul, and Qiudong Wang, "Experimental Verification of Rank-one Chaos in Switch-Controlled Chua Circuit", *Chaos* Vol.19, No.1, 013116, pp19-27, 2009.

V. Tavas, **A. S. Demirkol**, S.Ozoguz, A. Toker, and A. Zeki. "An Integrated Cross-Coupled Chaos Oscillator Applied to Random Number Generation" *IET Circuits, Devices & Systems.* Vol.3, No.1, pp1-11, 2009.

V. Tavas, **A. S. Demirkol**, S. Ozoguz, S. Kılınç, A. Toker and A. Zeki. "An IC random number generator based on chaos", Proc. of Int. Conf. on Applied Electronics, pp. 347-350, Pilsen, Czech Republic, 8-9 September 2010.

Serdar Ozoguz, **A. Samil Demirkol**. "Simplified chaotic systems generating Butterfly chaotic attractor", Proc. of Applied Electronics Conference, pp. 195-198, Pilsen, Czech Republic, 9-10 September 2009.

A. S. Demirkol, S. Ozoguz, V. Tavas, and S. Kılınç. "A CMOS Realization of Double-Scroll Chaotic Circuit and its Application to Random Number Generation" ISCAS'08, pp. 2374-2377, Seattle, USA, 18-21 May, 2008.

A. S. Demirkol, V. Tavas, S.Ozoguz and A. Toker. "High frequency chaos oscillators with applications" Proc. of 2007 European Conference on Circuit Theory and Design (ECCTD'2007), pp. 1026-1029, Sevilla, Spain, 26-30 August, 2007

PUBLICATIONS/PRESENTATIONS ON THE THESIS

A. Samil Demirkol, S. Ozoguz. "A Low Power VLSI Implementation of the Izhikevich Neuron Model", NEWCAS'11, pp. 169-172, Bordeaux, France, 26-29 June 2011.

A. Samil Demirkol, S. Ozoguz. "A Low Power Real Time Izhikevich Neuron with Synchronous Network Behavior" İstanbul Commerce University Journal of Science, accepted for publication.