ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

ZERO-IF SECOND HARMONICALLY PUMPED SiGe TRANSCEIVER INTEGRATED CIRCUIT

Ph.D. THESIS

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

SIFIR ARA SIKLIKLI İKİNCİ HARMONİK POMPALAMALI SiGe ALICI-VERİCİ TÜMDEVRESİ

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To my wife Özgecan and my son Deniz

FOREWORD

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ABBREVIATIONS

BiCMOS : Bipolar Complementary Metal Oxide Semiconductor
BPF : Band Pass Filter
CMOS : Complementary Metal Oxide Semiconductor
HBT : Heterojunction Bipolar Transistor
HPF : High Pass Filter
IC : Integrated Circuit
IF : Intermediate Frequency
IR : Image Reject
LNA : Low Noise Amplifier
LO : Local Oscillator
LPF : Low Pass Filter
MPW : Multi-Project Wafer
PA : Power Amplifier
PCB : Printed Circuit Board
Q : Quality Factor
RF : Radio Frequency
RFIC : Radio Frequency Integrated Circuit
SiGe : Silicon Germanium

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ZERO-IF SECOND HARMONICALLY PUMPED SiGe TRANSCEIVER INTEGRATED CIRCUIT

SUMMARY

The increasing number of mobile devices and the variety of new application areas arisen recently, accelerate the evolution of wireless communication systems. As the technology approaches to the concept of communicating everything, the improvement of wireless systems appear as a necessity to step forward. Thus, the requirements of the evolving technology determine the specifications to be satisfied by the transceivers of the wireless systems. To be deployed by many mobile devices, the transceivers should be simple in structure and integrated, since the area and the power consumption are main concerns of these kind of devices. Besides, it is expected from the mobile devices to include different types of wireless applications operating simultaneously. For the sustainability of the development of the mobile devices, they should benefit from simple and integrated transceivers.

As it is explained in Chapter 1, the purpose of the study is to develop a compact and integrated receiver solution for the wireless communication systems. The Homodyne, namely the Zero-IF architecture is selected to be implemented to use the advantage of simplicity of this type of receivers. It is aimed to provide adequate solutions to the well known problems of Zero-IF receivers by utilizing the proper techniques with the proper technology. The current literature is reviewed and the contributions made on the issue is summarized in Chapter 1.

Since the most of the problems of the Zero-IF transceivers are arisen from the equality of the local oscillator (LO) frequency and carrier frequency, the second harmonic mixing technique brings fundamental solutions to these problems. The half of the carrier frequency is used as the LO frequency in the second harmonic mixing technique. The fundamental mixing product at the output is suppressed and the second harmonic term is taken as the output signal. Using such a mixing technique breaks the equality of the carrier frequency and the LO frequency. Using the virtual signal of which frequency is two times the LO frequency as the mixing signal also prevents conversion of the phase noise of the oscillator signal into the signal band at the output. Realizing the local oscillator for half of the actually required frequency eases the design concerns of the oscillator. The advantages brought by using the second harmonic mixing technique is explained in details in Section 1.4.

For the integration of the Zero-IF receiver topology, SiGe BiCMOS semiconductor processing technology is selected to be used. SiGe is a semiconductor technology which is suitable for RFIC applications. The technology includes high speed transistors, high quality passive components and CMOS transistors. The variety of high performance devices provided together with the CMOS transistors suitable for dense digital circuits make it possible to easily integrate the complex mixed signal high frequency systems on the same chip. SiGe technology evolves from the well known Si

processes thus the knowledge and the infrastructure transfer during the development of the process make it easily accessible and low cost. The details about the SiGe technology is explained in Section 1.5.

The transceiver architectures Heterodyne and Homodyne are explained in Chapter 2. The Heterodyne is the widely used architecture which is mainly performing the frequency conversion in two steps by using an intermediate frequency (IF). Although they include more circuit blocks, these kind of architectures are preferred in many applications just to be stay away from the problems of the direct conversion. Heterodyne architectures are mostly realized with discrete components because of the complexity and the requirement of extra filtering. On the other hand, the Homodyne architectures, namely the Zero-IF architectures perform the frequency conversion in one step. Decreasing the number of building blocks and eliminating some filters, Homodyne architectures present a much simpler structure. However, Homodyne architectures bring some serious problems to be solved. These problems are detailed in Chapter 2.

To build up a Zero-IF receiver circuit, a low noise amplifier (LNA), a second harmonic mixer and an IF amplifier circuits are combined on a single integrated circuit. The topologies of these building blocks of the Zero-IF receiver circuit is explained in details separately in Chapter 3. The circuit schematics are given and the design concerns are explained. A fully differential structure is constructed through out the signal path. The topologies are selected accordingly to provide wide band operation. The receiver covers a variety of applications with a single structure. Covering variety of application bands also provides the ability to reuse the receiver for different services.

In Chapter 3, a new topology for the second harmonic mixer is proposed. The new topology on which the primary contribution is made provides an adequate mechanism to prevent the well known DC offset voltage problem of the Zero-IF receivers. By satisfying a constant DC current flow through the mixer circuit, the propagation of the large signal LO to the RF signal path through the supply lines and the substrate is prevented. The new mixing concept of operating with a constant DC current in some sense isolates the noisy mixer circuit from the rest of the building blocks. The large signal pumping current only occurs locally within the proposed mixer circuit. This is a crucial advantage especially for large scaled integrated mixed signal solutions.

The explanation of the new topology is made in Chapter 3. A detailed analysis is performed on the circuit and proper biasing conditions are exhibited. The effects of the biasing conditions over the circuit performance is shown with analytical results. The equations for the pumping current of which dominant frequency component is two times the LO frequency and the residue current which is the remaining part of the total DC current drawn from the supply voltage are derived from the large signal analysis. The change of the relevant harmonic components of the pumping current are shown according to the amplitude of LO signal and the DC biasing levels. On the graphs, how to find an optimum biasing point for a given LO amplitude is shown.

The explained circuit schematics are constructed and simulated within various test benches. The simulation results of the individual circuit blocks and the combined blocks are given in Chapter 4. The simulations of the LNA and the IF amplifier circuits are performed separately to examine the performance of these blocks. The proposed mixer simulations are given to show not only the performance of the mixer but also to verify the results given in the analysis in Chapter 3. It is exhibited that the

similar results with the analysis regarding the performance of the mixer is obtained in simulations. The pumping current and the residue current graphs are obtained for the same biasing conditions as in the analysis. The simulation results of the overall receiver is also shown in Chapter 4.

Chapter 5 is where the realization of the designed receiver is explained. The layout of the whole receiver circuit and the building blocks separately are drawn and placed for a Multi-Project Wafer (MPW) production. According to the predefined 5 mm$\times$5 mm integrated circuit area for MPW production, several separate layouts are prepared and placed for testing purposes. The prepared layouts are given in Chapter 5 and explained.

In Chapter 6, the preparation of the test setups and the testing environment are described and the acquired measurement results are given. Two separate Printed Circuit Boards (PCB) are designed to measure two test structures on the manufactured IC. Measurements performed on the first PCB is aimed to show the conversion gain performance of mixer on which the main contribution is made and to show the effectiveness of the proposed structure on the DC offset problem. The second PCB is used to measure the overall receiver structure consisting of LNA, mixer and the IF amplifier. Measurement results are compared to simulation results to show the correlation between theory and the practice.

The conclusions of the study are summarized in Chapter 7.

SIFIR ARA SIKLIKLI İKİNCİ HARMONİK POMPALAMALI SiGe ALICI-VERİCİ TÜMDEVRESİ

ÖZET

Mobil cihazların gün geçtikçe artması ve yeni kablosuz iletişim uygulama alanlarının ortaya çıkması, kablosuz iletişim sistemlerinin gelişimini hızlandırmaktadır. Teknoloji herşeyi birbiriyle haberleştirme kavramına yaklaştıkça, daha ileriye gidebilmek için kablosuz iletişim sistemlerinin geliştirilmesi bir gereklilik olarak ortaya çıkmaktadır. Bu nedenle, gelişen teknoloji ihtiyaçları kablosuz haberleşme sistemlerinde kullanılan alıcı-vericirilerin de sağlaması gereken teknik özellikleri belirlemektedir. Mobil cihazlar için en önemli kriterler alan ve güç tüketimi olduğundan, bir çok mobil cihaz tarafından kullanılabilmesi için alıcı-vericilerin basit ve tümleşik bir yapıya sahip olmaları gerekmektedir. Ayrıca, bu mobil cihazların farklı kablosuz iletişim uygulamalarını barındırması ve bu uygulamaları eş zamalı olarak çalıştırabilmesi beklenmektedir. Mobil cihazlarıdaki bu hızlı gelişimin sürdürülebilir olabilmesi için bu cihazların, basit ve tümleşik alıcı-verici bloklarının faydalarını kullanmaları gerekmektedir.

Bölüm 1'de anlatıldığı gibi bu çalışmanın amacı kablosuz iletişim sistemlerinde kullanılmak üzere basit bir yapıya sahip ve tek tümdevre üzerinde tümleştirilmiş bir alıcı yapısı geliştirmektir. Bu amaca yönelik olarak Homodyne, diğer adıyla Sıfır Ara Sıklıklı yapı kullanılarak bu yapıların basitliğinden faydalanılmıştır. Uygun teknikleri ve uygun teknolojiyi kullanarak bu yapıların herkesçe bilinen önemli sorunlarına çözümler sunulması amaçlanmıştır. Konu ile ilgili var olan literatür araştırması ve bu çalışmada yapılan katkılar Bölüm 1'de özetlenmiştir.

Sıfır Ara Sıklıklı alıcı-verici yapılarının sorunlarının büyük çoğunluğu yerel osilatör sıklığı ile taşıyıcı sıklığının birbirine eşit olmasından kaynaklanmaktadır. Bu nedenle ikinci harmonik pompalamalı karıştırma tekniği bu sorunlara temel çözümler sunmaktadır. İkinci harmonik pompalamalı karıştırma tekniğinde yerel osilatör sıklığı olarak taşıyıcı sıklığının yarısı kullanılmaktadır. Karıştırıcı çıkışında temel karıştırma terimi bastırılarak, yerel işaretin ikinci harmoniği ile ilgili karıştırma terimi çıkış işareti olarak seçilmektedir. Böyle bir karıştırma tekniğinin kullanılması yerel osilatör sıklığının taşıyıcı sıklığına eşitliğini bozmaktadır. Karıştırma için yerel osilatör sıklığının iki katı sıklıkta sanal bir işaret kullanılması, bir başka önemli sorun olan yerel osilatör faz gürültüsünün çıkıştaki işaret bandı içerisine dönüştürülmesini de engellemektedir. Ayrıca, yerel osilatörü gerçekte ihtiyaç duyulan sıklığın yarısını sağlayacak şekilde tasarlamak, yerel osilatörün gerçekleştirilmesindeki zorlukları da kolaylaştırmaktadır. İkinci harmonik pompalamalı karıştırma tekniğinin kullanılması ile sağlanan yararlar Bölüm 1.4'de detaylı olarak anlatılmaktadır.

Tasarlanan Sıfır Ara Sıklıklı alıcı topolojisinin tümleştirilmesinde kullanılmak üzere SiGe BiCMOS üretim teknolojisi seçilmiştir. SiGe özellikle yüksek sıklıklı tümdevre (RFIC) tasarımları için uygun olan bir yarıiletken teknolojisidir. Bu teknoloji,

yüksek hızlı transistorlar, yüksek kalite faktörlü pasif devre elemanarı ve yoğun sayısal devre tasarımları için uygun olan CMOS transistorları içermektedir. Böylece, yüksek karmaşıklıkta karışık işaret tasarımlarının tek tümdevre üzerinde kolayca tümleştirilmesine olanak sağlamaktadır. SiGe teknolojisi iyi bilinen silisyum (Si) üretim teknolojilerinden geliştirilmiş bir teknoloji olduğundan dolayı, geliştirilme aşamasında Si teknolojilerinde elde edilmiş olan bilgi birikimi ve altyapının kullanılması, bu teknolojinin kolayca ve ucuza ulaşılabilir olmasını sağlamıştır. SiGe teknolojisi hakkında detaylı bilgi Bölüm 1.5'de verilmiştir.

Heterodyne ve Homodyne alıcı-verici yapıları Bölüm 2'de detaylı olarak anlatılmaktadır. Heterodyne yapıları geniş olarak tercih edilen ve sıklık dönüştürme işlemini bir ara sıklık (IF) kullanarak iki adımda gerçekleştiren alıcı-verici yapılarıdır. Daha fazla devre bloğu kullanılmasına rağmen bu alıcı-verici yapıları doğrudan sıklık dönüştürme işleminin getirdiği sorunlardan uzak durulması için bir çok uygulamada tercih edilmektedirler. Yapılarındaki karmaşıklık ve ihtiyaç duyulan fazladan filtreleme işlemlerinden dolayı Heterodyne alıcı-verici yapıları genel olarak ayrık elemanlarla gerçekleştirilmektedirler. Homodyne yapılar, diğer adıyla Sıfır Ara Sıklıklı alıcı-vericiler ise sıklık dönüştürme işlemini doğrudan tek bir adımda gerçekleştirmektedirler. Kullanılan devre bloklarının azaltılması ve bazı filtrelerin atılması sayesinde bu alıcı-vericiler çok daha basit bir yapı sağlamaktadırlar. Fakat, Homodyne alıcı-vericiler beraberinde bazı önemli sorunlar getirmektedirler. Homodyne alıcı-vericilere ait bu önemli sorunlar Bölüm 2'de detaylı olarak anlatılmaktadır.

Sıfır Ara Sıklıklı bir alıcı devresi oluşturmak için, bir düşük gürültülü kuvvetlendirici (LNA), bir ikinci harmonik karıştırıcı ve bir IF kuvvetlendirici devresi tek bir tümdevre üzerinde bir araya getirilmiştir. Sıfır Ara Sıklıklı alıcı devresine ait bu yapı bloklarının devre topolojileri ayı ayrı olarak Bölüm 3'de anlatılmaktadır. Bu bloklara ait devre şemaları verilmiş ve tasarım aşamasında dikkat edilen noktalar açıklanmıştır. Bütün işaret yolu boyunca tam dengeli farksal bir yapı oluşturulmaya çalışılmıştır. Yapı blokları için seçilen topolojiler geniş bantlı çalışmaya uygun olacak şekilde seçilmiştir. Böylece alıcı devresinin tek bir yapı ile çeşitli uygulamaları bir arada destekleyebilmesi sağlanmıştır. Çeşitli uygulamaları desteklemesi aynı zamanda alıcı devresinin çoklu kullanılabilirliğini de sağlamıştır.

Bölüm 3'de ikinci harmonik karıştırıcı için yeni bir devre topolojisi önerilmiştir. Asıl katkının sağlandığı bu yeni devre topolojisi, içerdiği uygun bir mekanizma sayesinde, Sıfır Ara Sıklıklı alıcıların en önemli sorunlarından biri olan DC dengesizlik gerilimi sorununa çözüm getirmektedir. Bütün karıştırıcı devresinin üzerinden akan, beslemeden çekilen toplam akımın sabit tutulmasından dolayı, büyük genlikli yerel osilatör işaretinin besleme hatları ve taban üzerinden diğer bloklara ve RF işaret yoluna sızması engellenmektedir. Yeni sunulan sabit akım akıtarak karıştırma işlemini gerçekleştirme kavramı bir anlamda yüksek gürültülü karıştırıcı devresini diğer devre bloklarından izole etmektedir. Büyük işaret pompalama akımı karıştırıcı içerisinde sadece yerel olarak oluşmaktadır. Bu özellikle, büyük ölçekli tümleştirilmiş karışık işaretli tümdevreler için büyük fayda sağlamaktadır.

Önerilen yeni yapının açıklanması Bölüm 3'de yapılmıştır. Devre üzerinde detaylı bir analiz yapılmış ve uygun kutuplama koşulları gösterilmiştir. Kutuplama koşullarının devre performansı üzerindeki etkisi analitik sonuçlarla gösterilmiştir. Gerçekleştirilen büyük işaret analizinden, baskın sıklık bileşeni yerel osilatör sıklığının iki katı olan

pompalama akımı ve beslemeden çekilen toplam sabit akımın pompalama akımından geriye kalan kısmı olan fark akımı için denklemler çıkartılmıştır. Bu akımların ilgili harmonik bileşenlerinin DC kutuplama koşullarına ve yerel osilatör genliğine bağlı olarak değişimi gösterilmiştir. Verilen bir yerel osilatör genliği için en uygun kutuplama koşullarının nasıl bulunacağı grafikler üzerinde gösterilmiştir.

Açıklamaları yapılan devre şemaları kurulmuş ve çeşitli test düzenekleri için benzetimleri yapılmıştır. Yapı bloklarının ayrı ayrı benzetim sonuçları ve blokların birleştirilmiş hallerinin benzetim sonuçları Bölüm 4'de verilmiştir. LNA ve IF kuvvetlendiriciye ait benzetimler ayrı ayrı gerçekleştirilerek bu blokların performansları incelenmiştir. Önerilen ikinci harmonik karıştırıcı devresine ait benzetimler ise hem devre performansını incelemek hem de Bölüm 3'de verilen analiz sonuçlarını doğrulamak amacıyla gerçekleştirilmiştir. Karıştırıcı devresi performansı ile ilgili olarak Bölüm 3'de verilen analiz sonuçlarına benzer sonuçlar elde edildiği gözlenmiştir. Analizlerde kullanılan aynı kutuplama koşulları kullanılarak pompalama akımı ve fark akımının grafikleri elde edilmiştir. Tüm alıcı devresine ait benzetim sonuçları da Bölüm 4'de verilmiştir.

Tasarımı yapılan alıcı devresinin gerçeklenmesi Bölüm 5'de anlatılmıştır. Tüm alıcı devresinin serimi ve yapı bloklarının ayrı ayrı serimleri oluşturularak çok projeli pul (MPW) üretimi için hazırlanmıştır. MPW üretim şekilnin önceden belirlenmiş 5 mm$\times$5 mm tümdevre alınına uygun şekilde çeşitli serimler test amacıyla hazırlanmış ve yerleştirilmiştir. Hazırlanan serimler Bölüm 5'de gösterilmektedir.

Bölüm 6'da, ürettirilen tümdevrenin ölçülmesi için hazırlanan test düzenekleri ve test ortamı anlatılmış ve elde edilen ölçüm sonuçları verilmiştir. Üretilen test tümdevresindeki iki farklı test yapısını ölçmek için iki farklı baskılı devre (PCB) tasarlanmıştır. İlk PCB'de gerçekleştirilen ölçümler, çalışmada asıl katkı sağlanan karıştırıcı devresinin test edilmesi için kullanılmıştır. Karıştırıcının dönüştürme kazancı grafiği verilmiş ve önerilen yapının DC dengesizlik gerlimi sorunu üzerindeki etkisini göstermek amacıyla ölçümler yapılmıştır. İkinci PCB ise LNA, karıştırıcı ve IF kuvvetlendiricisinden oluşan tüm alıcı devresinin dönüştürme kazancının ölçülmesinde kullanılmıştır. Elde edilen sonuçlar benzetim sonuçlarıyla karşılaştırılarak uyumlulukları gösterilmiştir.

Çalışmadan elde edilen sonuçlar Bölüm 7'da özetlenmiştir.

1. INTRODUCTION

In todays world, electronic devices using wireless communication increase in enormous numbers and varieties. In conjunction with the recent developments and the new capabilities of the semiconductor industry, the evolution of the communication systems is accelerated exponentially. The variety of new application areas are arisen and started to be used widely in our daily lives.

The fast pace evolution of the wireless systems escalate the expectations on the transceivers. Transceivers shall present excellent performance while satisfying financial concerns of the market. Especially, the consumer electronic market in the recent years has turned into an arena where worldwide manufacturers strive to lead the relevant technology to survive. The mobile devices include several types of communication applications with different frequency bands and operate them simultaneously. It is crucial to provide advanced services including different communication protocols for these devices with limited resources. Due to the limited resources of the mobile devices, the power consumption specifications gain great importance. Along with the technical difficulties and limitations, the massive pressure of the market brings the price and the time to market parameters as merits of the success of a transceiver. The requirement of low price and short time to market leads the designers to simple, compact and more integrated solutions [1, 2].

Different types of transceivers exist, each having individual advantages and disadvantages. According to the requirements of the application area, generally, a specific type of transceiver is preferred. Depending on the number of steps they use to perform frequency conversion, transceivers are separated into two main categories; Heterodyne and Homodyne. Heterodyne architectures perform the frequency conversion in two steps while the Homodyne architectures accomplish in one step. Mainly, Heterodyne architectures have more complex structures but have some advantages over Homodyne transceivers. In spite of their complex structures, they are widely preferred in many applications just to stay away from the serious

problems of the Homodyne transceivers. On the other hand, Homodyne architectures have the advantage of being simple in structure. Nevertheless, their problems are to be solved to benefit its simplicity [1, 2]. The two main types of transceivers, Heterodyne and Homodyne transceivers, are summarized with their problems in Chapter 2.

1.1 Purpose of Thesis

In this study, a simple and integrated receiver topology is aimed to be designed. Thus, the Homodyne architecture is selected to be realized. The simplicity of the architecture is used to get a compact and integrated receiver solution. The problems of the architecture are handled by utilizing the advantages of the subharmonic mixing technique and the Silicon-Germanium (SiGe) technology.

In subharmonic mixing technique, the fundamental mixing product at the output of the mixer is suppressed and another product regarding a harmonic of the pumping signal is taken as output. Generally, the second harmonic product is preferred and the mixing is called the second harmonic mixing in this case. Utilizing the second harmonic mixing technique brings some remarkable solutions to some of the problems of Homodyne architectures. The details of the subharmonic mixing technique is given in Section 1.4.

For the implementation of the proposed receiver, SiGe technology is used which is a rising technology for radio frequency integrated circuits (RFIC) due to its high performance components. Another main advantage of the SiGe technology is being easily available and being suitable for integration. The SiGe technology is explained briefly in Section 1.5.

By utilizing the proper techniques with the proper technology, it is aimed to develop an integrated Homodyne receiver topology which has adequate solutions to the well known problems. A novel second harmonic mixer topology is proposed and the circuit analysis is performed on it. The theoretical results and the detailed description of the proposed mixer are given in Section 3.2.

1.2 Literature Review

To clarify the technical problem, the literature is reviewed for the transceiver architectures and their problems. In [3–6], the general transceiver topologies and

their well known problems are detailed. Wide band operation of the transceivers is touched in [7]. Since the aim of the study is to propose an appropriate Zero-IF topology for integration, [8–11] are investigated to understand the difficulties in integrating the overall structure. The effectiveness of the Zero-IF topology for the integrability and for providing compact solutions is explained in [2]. Regarding the solutions to the problems of the Zero-IF transceivers, [12] propose adaptive filtering technique for I/Q imbalance compensation and [13–17] includes some advance tuning techniques for second order intermodulation distortion. Recent works [8, 18–24] on Zero-IF transceivers show the state of the art.

SiGe BiCMOS semiconductor processing technology is selected to be utilized for the Zero-IF receiver integrated circuit. The references [25–28] show the capabilities of the SiGe technology. It is noted that the SiGe technology is a suitable choice for high integration RFICs. The available devices and the performance limits of the HBTs are shown in the given references.

Subharmonic mixing technique is one of the key components of the study, since it is used to overcome most of the problems of the Zero-IF topology. In [29], it is shown how second harmonic mixing is realized with an anti-parallel diode pair. It is also shown in [29] that the phase noise of the local oscillator signal is not converted, since a virtual local oscillator (LO) signal of which frequency is two times the actual LO signal is used for mixing. Recent implementation of subharmonic mixing in Zero-IF topologies are given in [2, 18–20, 20, 23, 30–43]. The references [20, 30, 35–38, 41, 43] introduce some subharmonic mixers designed in CMOS technology while the implementations given in [23, 32–34, 40, 42] utilize the advantages of SiGe BiCMOS technology. In the given references, the subharmonic mixers are designed for Zero-IF applications to provide integrated solutions. Investigated references as the embodiments of the subharmonic mixers in different technologies are compared with the proposed mixer topology in this study in Chapter 7. The design concerns for different applications are investigated from these references. In [44], a low-IF solution is proposed to use the advantages of Zero-IF receivers without dealing with its difficulties. There are works done in [45–48] for MESFET mixers and distributed MESFET mixers and nonlinear analysis of them.

The most effective problem of Zero-IF transceivers, DC offset voltage is investigated in [49–53]. These references propose some techniques to overcome the problem and give some results regarding the effectiveness of the techniques. The references [54–56] propose some techniques against LO pulling problem and the reference [49] considers second order intermodulation distortion together with the DC offset problem. The IQ mismatch problem and related solutions are given in [57, 58]. In [59], a single chip Zero-IF CMOS implementation is proposed using one-third frequency LO.

For the design of wide band LNA, the reference [60–62] are used. The proposed circuits show the state of the art. The LNA implementations given in [60, 62] use the CMOS technology. The reference [63] is an SiGe implementation which is an integrated front-end solution for transceivers. In [64], a bias feed circuit is proposed for a SiGe LNA implementation. The IF amplifier topologies are also searched and recent works are studied. In [65, 66], recent topologies for the IF amplifier are shown. In the design of LNA and IF amplifier, [3, 5, 6, 67, 68] are also used.

1.3 Contributions

The aim of the study is to develop an integrated Zero-IF receiver topology for compact and dense applications. To achieve this goal, the proper components are combined together. One is utilizing the second harmonic mixing technique which provides some fundamental solutions to the problems of the Zero-IF transceivers naturally. The main cause of the well known problems of the Zero-IF transceivers is the equality of the LO frequency and the carrier frequency. By using second harmonic mixing technique, this equality is broken since the half of the carrier frequency is used as the LO frequency instead. The advantages brought by the second harmonic mixing technique is explained in details in Section 1.4.

Other important component utilized to get an integrated Zero-IF receiver topology is SiGe BiCMOS processing technology. SiGe is an emerging technology for the RFIC applications. Since it is developed from the advanced techniques obtained in well known Si process, it is easily accessible and affordable. Providing the complementary metal oxide semiconductor (CMOS) transistors together with the high speed SiGe heterojuntion bipolar transistors (HBT) and other analog circuit components, the SiGe

technology constitutes a proper environment for the integration of complex high speed designs.

Along with combining the proper techniques and technology, the development of individual building block topologies is carried out purposefully according to the problems of the Zero-IF transceivers. A wide RF range is targeted to construct a general receiver structure covering the frequency bands of variety of applications. Besides obtaining the area and cost efficient topology, it is also intended to provide a single solution for different types of applications.

The main contribution is made on the mixer of the receiver topology. A novel second harmonically pumped Zero-IF mixer topology is proposed. Although the DC offset problem is treated by using second harmonic mixing technique, there still may be DC offset voltage at the output due to the leakage of the second harmonic of the LO signal to the RF signal path. Especially, when both the LNA and the mixer are integrated on the same chip, the leakage to the input of LNA through the substrate may cause considerable DC offset voltage. The proposed topology contains a unique mechanism to cancel the DC offset voltage at the output.

Due to the unique mechanism, a constant total DC current flows through the overall mixer circuit. First, the constant DC current is split into two and the pumping current containing the proper frequency components is obtained. After performing the mixing, the split pumping current and the residue current is combined again to form the constant DC current. Thus, the total current drawn from the supply lines is kept constant. Thanks to this attribute of the proposed mixer topology, the noisy large signal mixing operation take place locally in the mixer circuit and it is isolated from the supply and ground lines from which generally the leakage to the other circuit components occur.

In the proposed mixer topology, the leakage of the second harmonic of the LO signal to the RF input is also suppressed. Although the overall current of the mixer is kept constant, the RF input signal conducts to the transistors on which the pumping current flows. To prevent the leakage of the second harmonic of the LO signal to the RF input through the input transistors, the RF input transistors are replicated and the residue current containing the opposite frequency components is flown through these

transistors. By also considering the symmetry, the overall leakage to the RF input of the mixer is also suppressed. The details of the DC offset cancellation mechanism is explained in Section 3.2.

Along with providing a new second harmonic mixer topology with conceptually new mechanism for DC offset voltage cancellation, the circuit analysis of the topology is performed for the SiGe techology. The proper biasing conditions for appropriate mixing is determined. The effects of the biasing conditions on the linearity and the efficiency of the circuit is investigated and approved with analytical results.

1.4 Subharmonic Mixing Technique

Mixers widely preferred in different types of transceivers generally use fundamental mixing. In fundamental mixing technique, the upconverted or the downconverted output signal is selected as the fundamental product of the multiplication of two inputs. When the Fourier series expansion is investigated, it is seen that the fundamental term of the mixing products has the greatest coefficient among others. Thus, the fundamental mixing is widely used basically to maximize the conversion gain of the mixer. Although the conversion gain is maximized in fundamental mixing technique, some disadvantages come along with it [3–5].

Maximizing the conversion gain at the mixer decreases the effect of the noise of the following stages to the signal. However, strict restrictions are brought to the design specs of the oscillator. When the fundamental mixing technique is used in Zero-IF reception, the phase noise of the oscillator is directly converted into the signal band [3, 29]. Since, the oscillator frequency is needed to be equal to the carrier frequency, it gets more difficult to design such an oscillator. Thus, the phase noise performance of the oscillator gains great importance in the overall system performance. To design a low phase noise oscillator, it is required to have circuit components with high quality factors which is a difficult requirement to be satisfied in integrated circuits. Therefore, low phase noise oscillators are not suitable for integration so that they are implemented with discrete components.

In subharmonic mixing technique, an harmonic component of the mixing products, generally the second harmonic, is selected to be the converted output [29]. The

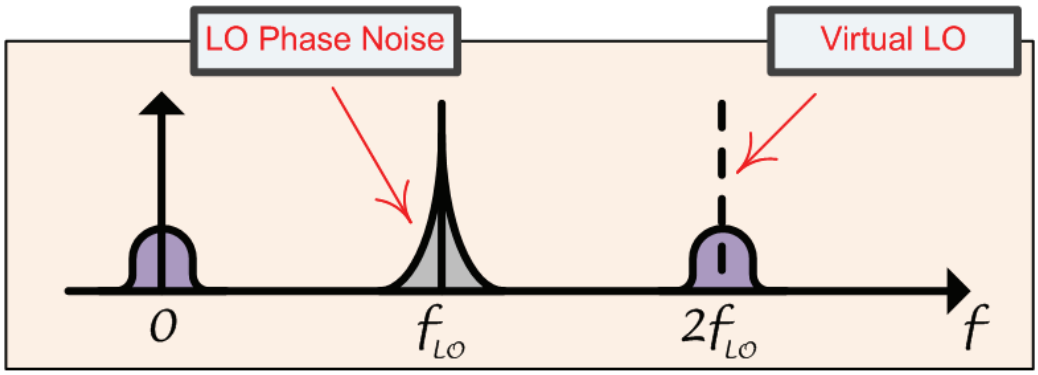

Figure 1.1 : The conversion mechanism of the second harmonic mixing technique when used in Zero-IF mixers.

fundamental mixing product is suppressed at the output. Although the harmonic component of the mixing product has a lower Fourier coefficient than the fundamental product, selecting the harmonic component as the mixing result provides some advantages. Since the fundamental mixing product is suppressed at the output, in this type of mixing the phase noise of the oscillator is not converted into the signal band [29]. The natural elimination of the phase noise of the oscillator from the signal band relieves the design specs on the oscillator in great extend. It can even be possible to integrate the oscillator together with other circuit blocks.

When second harmonic mixing technique is used in Zero-IF transceivers, it reveals even greater advantages for this specific situation. In a Zero-IF transceiver using the second harmonic mixing technique the LO frequency is arranged to be the half of the carrier frequency. Since the most severe problems specific to Zero-IF transceivers grow out from the equality of the LO frequency and carrier frequency, second harmonic mixing technique arises as an fundamental solution to these problems. The conversion mechanism of second harmonic mixing technique when used in Zero-IF mixers is shown in Figure 1.1 [29]. Here, it is shown that the RF signal band is downconverted to the base band by a virtual LO signal of which frequency is $f_{2LO} = 2 \times f_{LO}$, thus the phase noise spectrum around f_{LO} is not converted into baseband.

1.5 SiGe Technology

SiGe is a rapidly developing semiconductor technology which has great use in high frequency microelectronics. The advantages it brought help designers to solve many

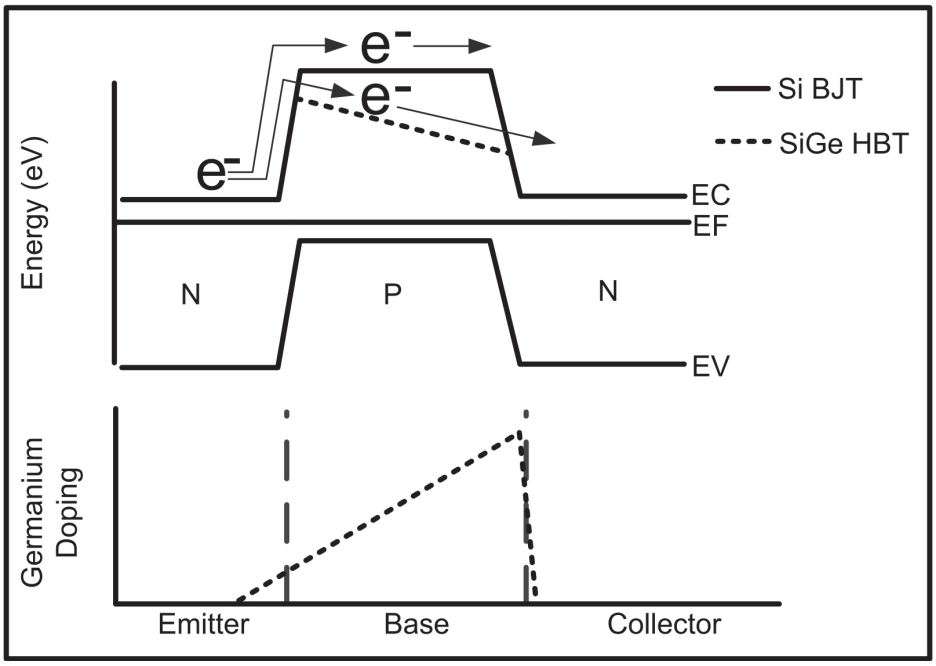

Figure 1.2 : Energy band diagram and Ge doping profile of a SiGe HBT.

problems of RF applications. Since it has evolved from the well known and widely used CMOS technology, the use of readily developed infrastructure and knowledge of CMOS technology makes SiGe technology low cost and easily accessible. Being low cost and easily accessible, SiGe technology finds place in many RF applications [25–27].

SiGe technology involves Germanium (Ge) doping into the standard Silicon (Si) substrate. As shown in Figure 1.2, the Ge doping in the base of the transistor changes in a linear fashion and bends the energy band diagram respectively. This bending of the energy band diagram creates an internal electrical field which increases the velocity of the electrons passing the base region [27, 28]. Thanks to this mechanism, very high speed transistors are obtained in SiGe technology. The high speed transistor obtained by Ge doping in the base region is called Heterojunction Bipolar Transistor (HBT). These transistors have also the advantages of being low noise and having high breakdown voltage.

2. TRANSCEIVER TOPOLOGIES

Two main transceiver topologies, Heterodyne and Homodyne, are summarized in this Chapter. Advantages and drawbacks of the both architectures are exposed. The problems of the Homodyne transceivers are explained in details and some techniques from the current literature used to solve these problems are given. Since the Homodyne transceiver architecture is the one to be used in this study, the reasons and the possible solutions to this kind of transceivers are given to present the technical problem clearly.

2.1 Transceiver Topologies

In the current literature, there are various transceiver topologies in use, all having different advantages and disadvantages. In transceiver circuits, the topology to be used is selected according to the application area and the frequency range. Due to the challenging required specifications of the communication standards and the difficulties of the high frequency electronic design, different topologies optimized for each specific application are generally used. Necessity of high order filters, passive circuit elements with high quality factors, low jitter oscillators and impedance matching in high frequency electronics prevents the integration of the whole transceiver topology on a single chip [3–5]. The required passive components with high quality factors, high order filters and low jitters oscillators are implemented with discrete components.

Transceiver topologies are categorized in two main types of architectures; heterodyne and homodyne [3]. Heterodyne architecture performs the frequency conversion between the radio frequency (RF) and the baseband in two steps by using an intermediate frequency (IF). This architecture comes along with a well known image problem [3]. Thus, the transceivers implemented in this architecture include additional filters to suppress the image frequency. Including two conversion steps and additional filters increase the architectures complexity, yet it is a widely preferred architecture in many applications due to its advantages [4, 7]. However, the complex structure of the heterodyne architecture makes this type of transceivers difficult to integrate on a

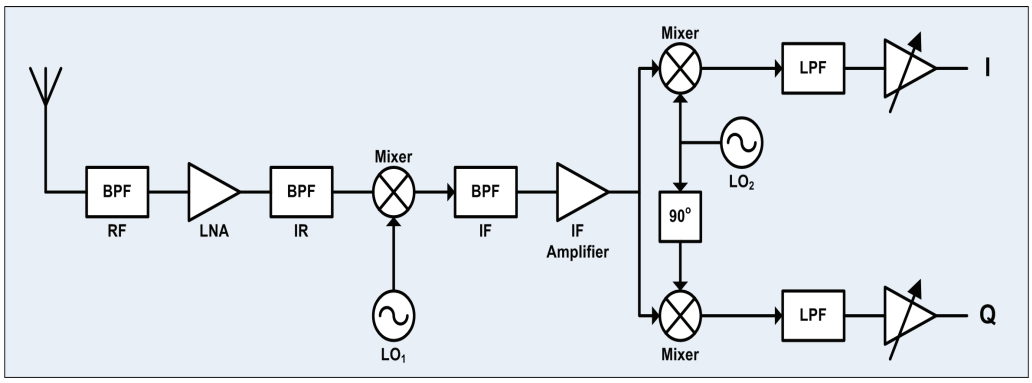

Figure 2.1 : Block diagram of the receiver part of the heterodyne transceivers.

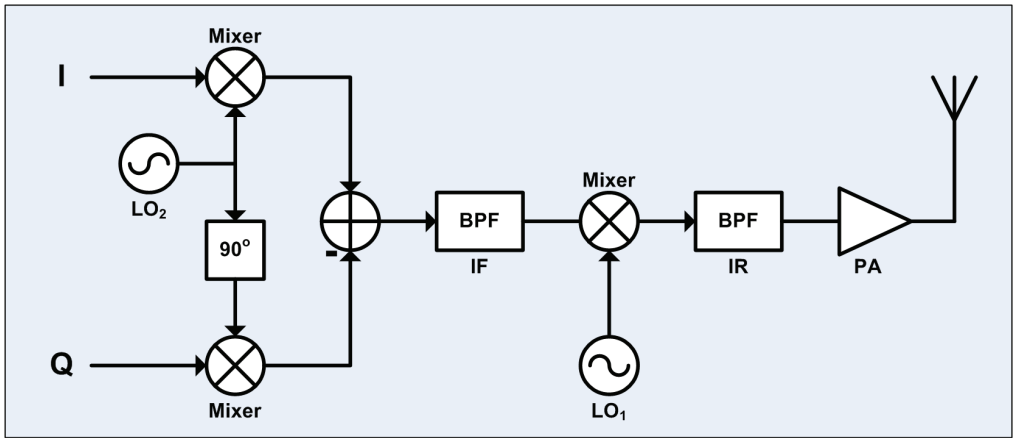

Figure 2.2 : Block diagram of the transmitter part of the heterodyne transceivers.

single chip. Block diagram of the heterodyne transceivers is shown in Figure 2.1 and Figure 2.2 [3].

Homodyne transceivers on the other hand, performs the frequency conversion in one step. This type of transceivers are also known as direct conversion transceivers or Zero-IF transceivers. The frequency conversion in one step prevents the image problem and the additional filters used to filter out the image frequency is omitted in these transceivers [3, 4, 6]. The number of mixers, local oscillators (LO) and amplifiers are also decreased because of the single step conversion. This architecture has a more simple structure when compared to heterodyne transceivers. The simplicity of the architecture makes this type of transceivers more suitable for integration on a single chip. However, simplicity and being suitable for integration brings some other serious problems; DC offset voltage, I/Q mismatch and Flicker noise [3,4]. These problems of the homodyne transceiver architecture will be explained in Section 2.2. Block diagram of the homodyne transceivers is shown in Figure 2.3 and Figure 2.4.

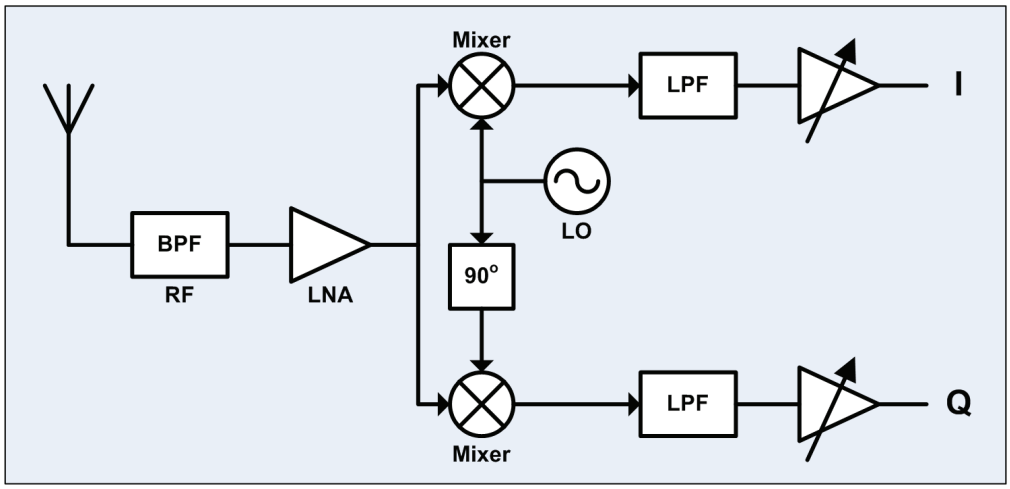

Figure 2.3 : Block diagram of the receiver part of the homodyne transceivers.

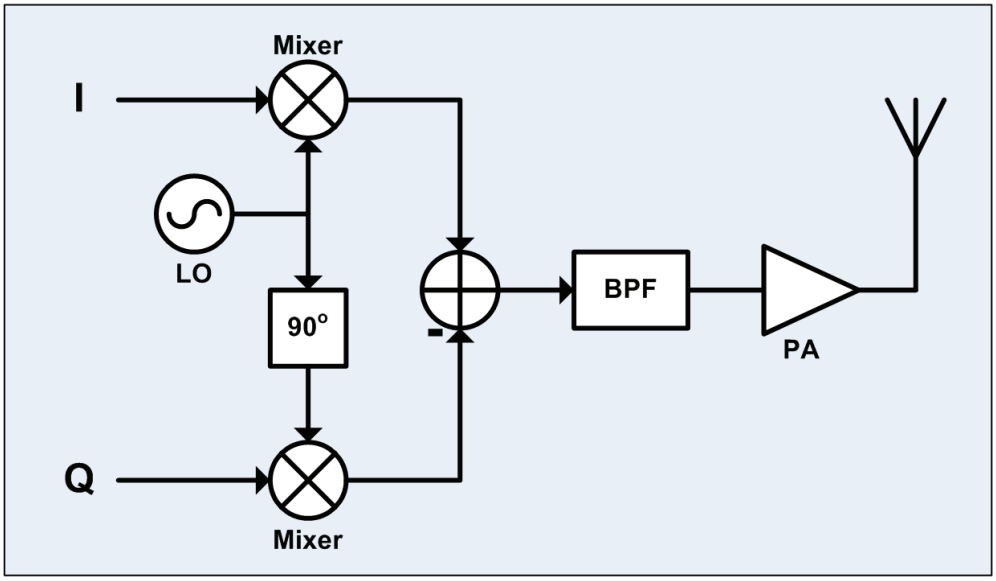

Figure 2.4 : Block diagram of the transmitter part of the homodyne transceivers.

2.2 Problems of Homodyne Transceivers

Homodyne Transceivers, also known as Zero-IF transceivers, has a simple structure with fewer building blocks when compared to heterodyne counterparts because the frequency conversion occurs in only one step. Beside this basic advantage, since the LO frequency is equal to the carrier frequency in Zero-IF transceivers, the image problem does not occur in this type of transceivers [3]. Thus, the image reject (IR) filter is omitted. Omitting the IR filter also simplifies the design of the low noise amplifier

(LNA) in the structure, since the output of the LNA is not needed to be matched to an 50 Ω discrete filter [3].

Channel selection in Zero-IF transceivers is made by lowpass filter (LPF) in the baseband. Since this filter operates in low frequency region, it is suitable to be realized as an on-chip active filter. All the components including this LPF except the high frequency bandpass filter (BPF) and the power amplifier (PA) at the transmitter output can be integrated on a single chip. The suitability to integration of the Zero-IF transceiver topology is depicted as being promising in various works [2, 44].

2.2.1 DC Offset Voltage

One of the most important problems of the Zero-IF transceivers is the DC offset voltage occurring at the output of the receiver. This problem appears in only Zero-IF transceivers because of the equality of the LO frequency and the carrier frequency. There are two mechanisms to be investigated as a reason of this problem. These mechanisms are shown in Figure 2.5 and Figure 2.6 [3].

In the first mechanism which is shown in Figure 2.5, the LO signal leaks to the RF path and it is downconverted in the mixer by the LO signal itself [3, 50, 69]. This results in a DC offset voltage at the mixer output. Especially the leakage to the input of the LNA may result in a greater problem since the leaked signal is amplified along with the RF signal in the LNA.

The other mechanism of the DC offset voltage problem is the RF signal leakage to the LO port of the mixer as shown in Figure 2.6. The leaked RF signal mixes itself in the mixer resulting in a varying DC offset voltage at the output of the receiver [3, 50, 69]. This mechanism is less severe according to the LO leakage mechanism since the RF signal has less power compared to LO signal even after being amplified in the LNA.

In the literature, there are some precautions proposed to solve the DC offset voltage problem. One of them is using a high pass filter (HPF) at the output [3]. This can be applied only if a suitable modulation technique removing the data close to DC is applied. Otherwise, applying a HPF results in data loss near DC. Even when the data is removed from vicinity of the DC with a suitable modulation technique, a HPF with a very low cutoff frequency is needed. To realize a very low cutoff frequency,

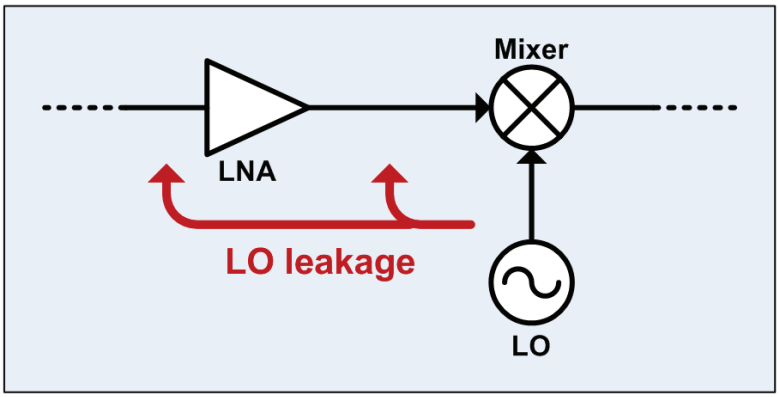

Figure 2.5 : DC offset voltage due to LO leakage mechanism.

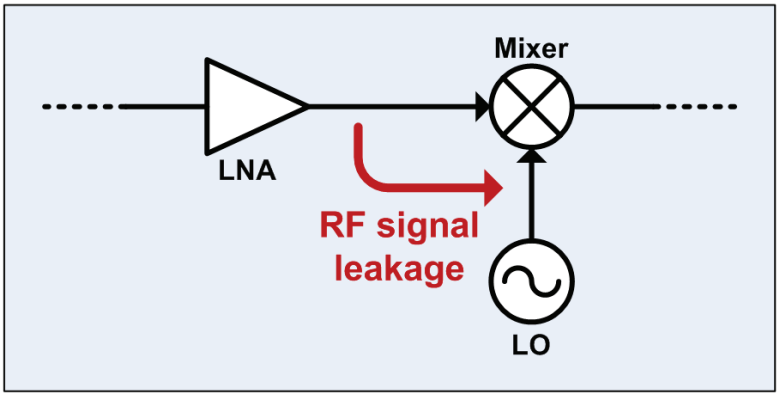

Figure 2.6 : DC offset voltage due to RF leakage mechanism.

a huge capacitor is needed to be used which is only possible with usage of discrete components. Using a HPF with a very low cutoff frequency has another drawback that is insufficient filtering of the DC offset voltage [3].

As it is not feasible to filter out the DC offset voltage at the output in Zero-IF receivers, more complex solutions involving digital and analog signal processing techniques are proposed [58, 69, 70]. These techniques rely on the fact that the DC offset voltage has a very low dependency on time. The DC offset voltage of system is characterized during idle time and then the DC offset voltage when it is functional is predicted [3]. Examples of some other techniques introduced in the literature are given in [49–53,58].

Designing a fully symmetrical transceiver is also used as a precaution to this problem. It is tried to make the symmetrical paths to be effected equally form the leakages and other reasons of DC offset voltage problem. The relevant isolations in the circuit should also be considered to minimize the leakages.

2.2.2 I/Q Mismatch

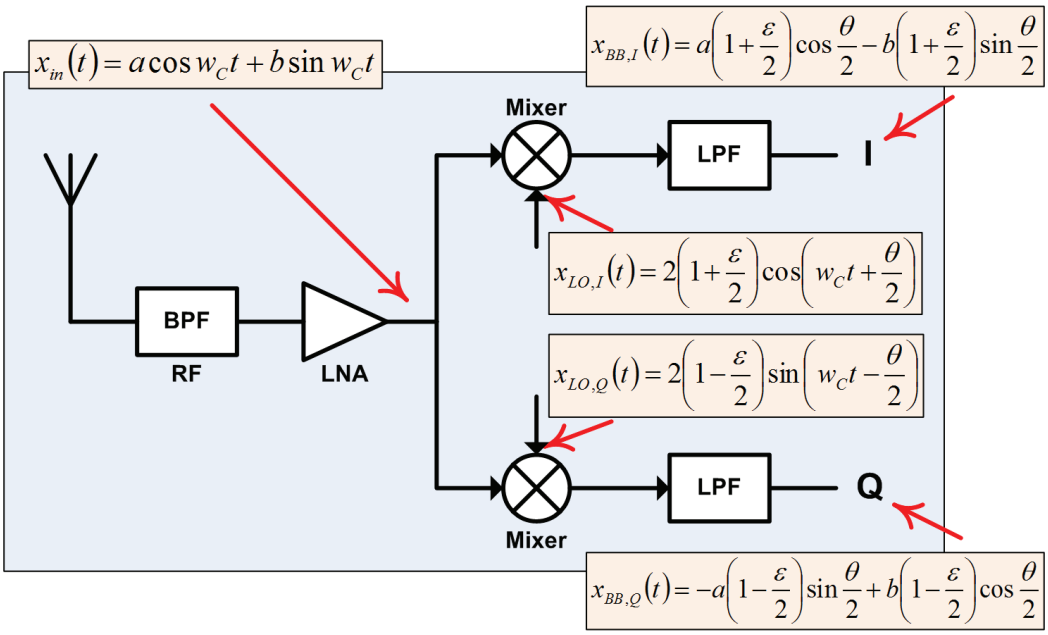

Figure 2.7 : IQ mismatch mechanism on Zero-IF mixers.

In Zero-IF transceivers, the LO frequency is equal to the carrier frequency. Thus, when the RF signal is downconverted, left and right sidebands overlap. This does not cause a problem in the modulation techniques like amplitude modulation (AM) since the left and the right sidebands carry the same information. However, in the modulation techniques like frequency modulation (FM) and phase modulation (PM) where the left and the right sidebands carry different information, the Zero-IF transceiver should produce quadrature outputs [3]. These quadrature outputs, I and Q, are produced as shown in Figure 2.3. Two equivalent paths are used for both outputs and the mixers are driven with 90^o out of phase LO signals. Following two different paths after LNA, the RF signal may be subject to different gain and phase errors [3]. Similarly, the 90^o out of phase LO signals may also come under different errors. This mismatch between two paths of the quadrature outputs may cause improper separation of I and Q parts of the RF signal and one output may disturb the other [3]. In Figure 2.7, the IQ mismatch mechanism in Zero-IF mixers is shown.

Here, ε is the gain error and the θ is the phase error between the LO signals applied to two symmetrical paths. The resultant effects of the gain error and the phase error are shown separately in Figure 2.8 and Figure 2.9 respectively.

I/Q mismatch problem has a greater possibility to occur in discrete implementations where it is harder to make the both paths symmetrical enough. To prevent this problem,

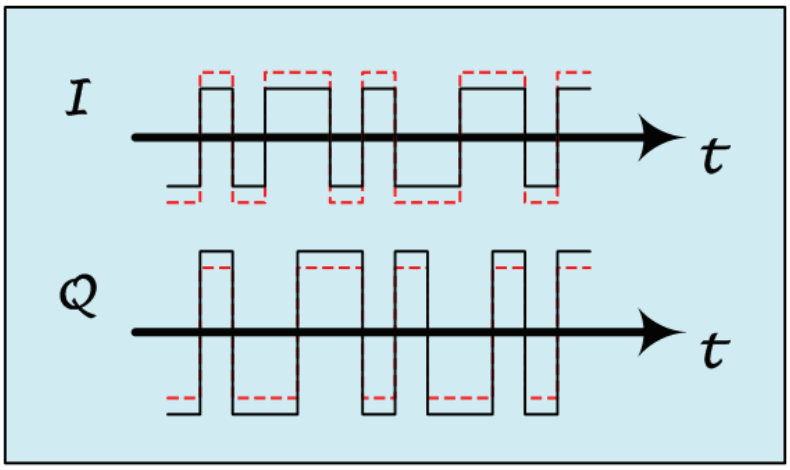

Figure 2.8 : Gain error between I and Q outputs of the Zero-IF mixer.

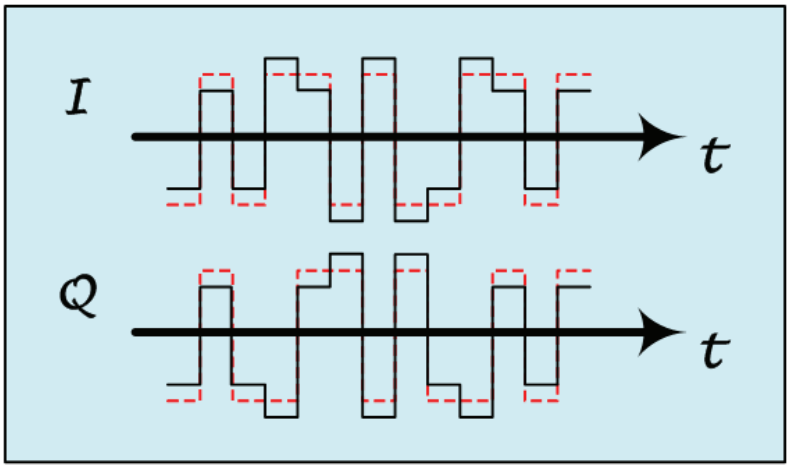

Figure 2.9 : Phase error between I and Q outputs of the Zero-IF mixer.

implementing the two paths on a single integrated circuit helps in great extend. Since I/Q mismatch varies slightly with time, various post processing techniques may also be used to recover the signals [12, 57, 58]. However, these techniques increase the complexity of the circuit.

2.2.3 Even Order Distortion

Even Order Distortion is another issue to be solved in Zero-IF transceivers which is caused due to the equality of the LO frequency and the carrier frequency. An ideal mixer outputs only the products of the multiplication of its two inputs. In actual realizations, the signals at the inputs themselves are also transferred to the output with some loss. Because of the nonlinear behavior of the LNA and the RF input of the mixer, any two interferer signals close to the RF signal band may cause unwanted low frequency components at the RF input of the mixer [13–17]. These unwanted

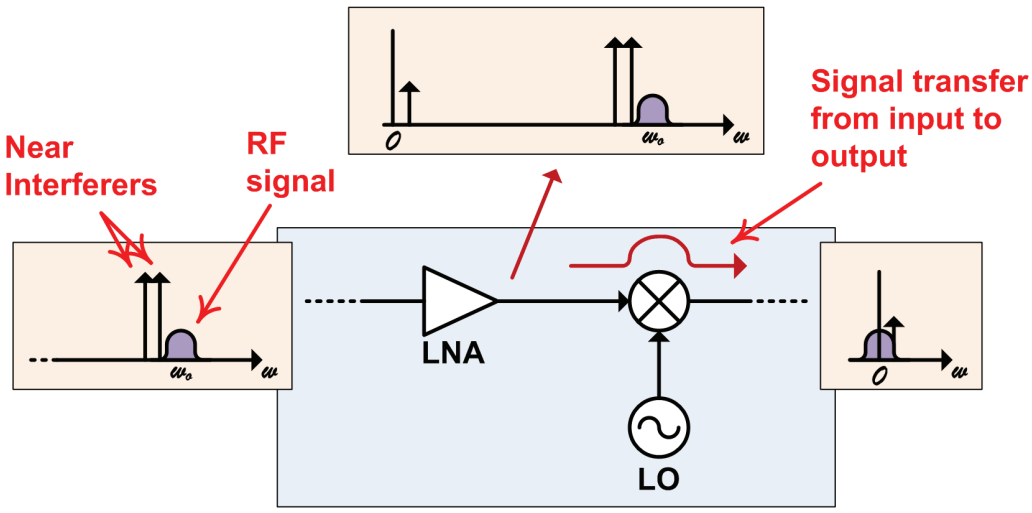

Figure 2.10 : The effect of even order distortion at the input of the Zero-IF receiver.

low frequency products of the even order distortion at the input are then transferred to the output with some loss by the mixer. They reside in the baseband where the desired actual signal exists [3]. Thus, these unwanted outcomes of the interferer signals cannot be eliminated by the LPF at the output. The effect of even order distortion on Zero-IF transceivers is shown in Figure 2.10.

2.2.4 Flicker Noise

In Zero-IF receivers, the Flicker Noise of the stages following the mixer is added directly to the signal band since the RF signal is converted directly to baseband in the mixer. Thus, the Flicker Noise of the stages following the mixer along with the gain of the LNA and the conversion gain of the Mixer become important.

This problem arises mostly in CMOS implementations. Using a technology like SiGe where the transistors are low noise devices relieves the problem. The precautions taken for the DC offset voltage problem also help decreasing the Flicker Noise since it is dominant near DC [3, 70].

2.2.5 LO Leakage

The radiation of the LO leakage via the antenna causes interfering signal to the other receivers. Since the LO frequency is equal to the carrier frequency, the LO leakage problem may cause considerable disturbance in Zero-IF receivers. The on-chip implementation of the local oscillator decreases this problem since the most important

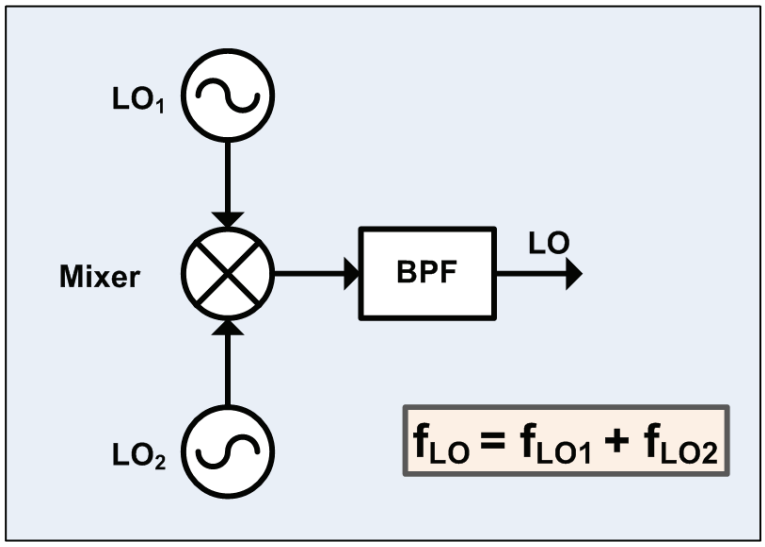

Figure 2.11 : Producing the actual LO signal from two different LO signal with different frequencies.

source of LO radiation is the bonding wires. As described in Section 1.4, using second harmonic mixing technique brings a fundamental solution to this problem even when the oscillator is implemented outside the chip [3].

2.2.6 LO Pulling

In Zero-IF transmitters, there exist a high power RF signal at the output of the PA. Since the frequency of this RF signal is equal to the LO signal, it may cause the output frequency of the voltage controlled local oscillator to change [3, 56]. This effect is called the LO pulling. To solve this problem, a technique which is shown in Figure 2.11 by producing the actual LO signal on-chip by mixing two external LO signals with different frequencies can be applied [3]. In [59], a single chip Zero-IF CMOS implementation is proposed using one-third frequency LO. Some other techniques to LO pulling resistant transmitters are introduced in [54–56].

Using second harmonic mixing technique as explained in Section 1.4 also helps to prevent the LO pulling problem of the Zero-IF transceivers. Since the LO frequency is the half of the carrier frequency, the high power RF signal at the PA output cannot change the frequency of the LO.

3. THEORY OF THE PROPOSED CIRCUIT

In this section, the building blocks of the proposed second harmonic Zero-IF receiver topology; low noise amplifier (LNA), second harmonic mixer and IF amplifier are examined separately. For the LNA and IF amplifier, differential circuit topologies are selected to be realized. The design and the realization of these block are done considering that it is aimed to obtain a receiver topology which is integrated on a single chip. The design considerations and details of the selected topologies for the LNA and the IF amplifier are given in Section 3.1 and Section 3.3 respectively.

A new second harmonically pumped mixer topology is proposed. The topology is explained in details in Section 3.2. Circuit analysis of the proposed mixer is performed and the proper operating conditions for second harmonic mixing is exhibited. Also the main contribution made to the Zero-IF receiver topology in order to solve the DC offset voltage problem is explained in this section.

3.1 Low Noise Amplifier (LNA)

As a front-end to the proposed Zero-IF receiver topology a wide band LNA is designed. Selected topology is a differential two stage amplifier. It is designed to operate within a wide frequency range to satisfy a receiver which can be utilized in different applications. The selected LNA topology is explained in details in Section 3.1.1.

3.1.1 LNA Topology

The LNA circuit schematic designed for the Zero-IF receiver is shown in Figure 3.1. For simplicity in the circuit schematic, some connections are shown with labeling. The nodes with same labels should be considered connected. The selected topology is suitable for wide band operations and it has single ended input and differential outputs. The LNA circuit is designed to operate within a wide range of 2-10 GHz. it consists of two gain stages and an emitter follower stage. The input matching of the circuit is achieved by the passive components, C1, C2, L1 and L2. L1 is also used to supply

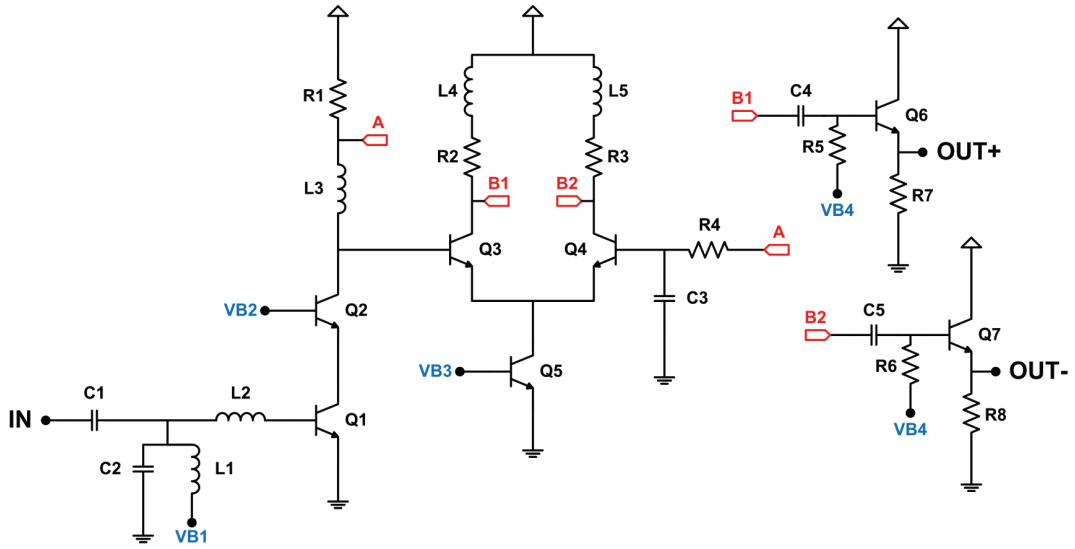

Figure 3.1 : LNA circuit schematic.

the input biasing voltage VB1 which is generated internally. The first gain stage is a common emitter cascode gain stage consisting of Q1 and Q2 transistors. The passive components L3 and R1 compose the load impedance of the first gain stage.

The second gain stage of the LNA is a differential pair stage composed of Q3 and Q4 transistors as the identical pair and the Q5 transistor as the biasing current source. Q5 transistor is biased with a constant voltage VB3 which is also generated internally. The load impedance of the differential pair consists of R2, R3, L4 and L5 components. The passive components on both sides of the differential pair is taken identical. L4 and L5 inductors are implemented as a center tapped single symmetrical inductor. Besides supplying gain in the signal path, the main purpose of this second gain stage to convert the single ended RF signal to a balanced differential signal. To achieve this purpose, signal ended RF signal coming out from the first gain stage is applied to one input of the differential pair, to the base of transistor Q3, and the other input of the differential pair, the base of transistor Q4, is biased with the DC voltage level of the same RF signal. A low pass filter consisting of R4 and C3 is used to obtain the DC voltage level of the RF signal.

Using a first order filter consisting of R4 and C3 to generate the DC voltage level of the RF signal is a simple and an effective solution. Arranging the cutoff frequency of the filter, the whole baseband can be passed through. Applying the baseband portion of the RF signal to the common port of the differential pair, base of Q4, eliminates

the unwanted components in the baseband in the following stages. As explained in the even order distortion problem in Section 2.2.3, the nonlinearity of the signal path may cause it to contain unwanted frequency components in the baseband. Some part of these components are directly transfered to baseband at the mixer output because of some unidealities. Therefore, using such a LPF helps also preventing the even order distortion problem in some sense while providing the necessary biasing to the second stage. The unwanted even order distortion products at the baseband originating from the nonlinearity the first stage then be prevented at the differential second stage. After that point, the overall Zero-IF receiver circuit maintains differential structure which makes it naturally immune to even order distortion.

As a further approach, the LNA circuit should be constructed as shown in Figure 3.2. In this configuration, the biasing of the Q4 transistor in the second stage is accomplished by a negative feedback from the outputs of the LNA. A simple operational amplifier can be used for the feedback. Even a single differential pair is sufficient. By placing a proper capacitance, the bandwidth of the feedback amplifier can be arranged to the baseband. Thus, all the unwanted signals somehow occur in the baseband is eliminated by equalizing the differential outputs within the relevant band. Thanks to this amplifier feedback, any baseband signals occurring at the RF inputs of the mixer for any reason is filtered out. However, for sake of simplicity in the overall structure, this approach is not utilized in the design of the LNA. The schematic using a first order LPF for the biasing of the second stage given in Figure 3.1 is used for the Zero-IF receiver topology.

At the outputs of the second gain stage, the balanced differential RF signal is generated and it is applied to the emitter follower stage at the output. Transistors Q6 and Q7 act as the emitter followers and they are biased via identical resistors R5 and R6. The biasing voltage of the emitter follower stages VB4 is also generated internally with a biasing circuitry. The load resistors of the emitter followers, R7 and R8, are also taken identical. By using the emitter followers at the output of the LNA, a low and almost constant output impedance within the target frequency range is obtained.

Since the LNA which is designed to be used in Zero-IF receiver is not connected to an IR filter at the output, the output impedance or the LNA is not matched to 50 Ω. In the Zero-IF receiver topology, the LNA is directly connected to the mixer and they

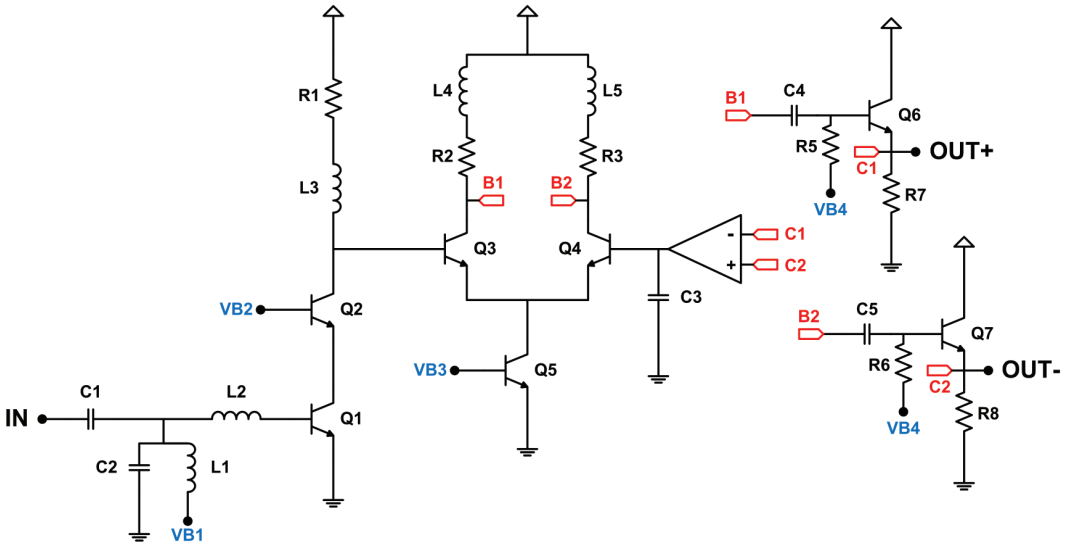

Figure 3.2 : The circuit schematic of the LNA with the negative feedback.

are planned to be integrated on a single chip. Thus, the low and almost constant output impedance of the LNA topology satisfy the requirements of the overall Zero-IF receiver topology.

3.2 Second Harmonic Mixer

A new second harmonically pumped mixer topology is proposed and the details of the topology are given in this section. A detailed circuit analysis is performed on the proposed topology. Proper operating conditions are determined depending on the circuit analysis and the principle contribution made for solving the DC offset voltage problem is explained. Biasing dependent performance alteration is also exhibited upon the analysis performed.

3.2.1 Proposed Mixer Topology

The proposed second harmonically pumped mixer topology is depicted in Figure 3.3. The input RF signal $v_{RF}(t)$ is assumed to be given by (3.1).

$$v_{RF}(t) = V_{RF} \cos \omega_{RF} t \tag{3.1}$$

In the proposed circuit, the balanced form of $v_{RF}(t)$ is applied to the input ports of the both primary and secondary differential pairs consisting of transistors Q1, Q2 and Q3, Q4 respectively. Here, V_{RF} is the amplitude and ω_{RF} is the angular frequency of the

RF signal. The balanced LO signal $v_{LO}(t)$ is applied to the inputs of the tail transistors Q5 and Q6 which act as the current sources of the primary differential pair. The LO signal $v_{LO}(t)$ is defined as in (3.2). Further definitions regarding $v_{LO}(t)$ signal is made in (3.3), (3.4) and (3.5) to be used in equations later on.

$$v_{LO}(t) = v_{LO}^{+}(t) - v_{LO}^{-}(t) \tag{3.2}$$

$$v_{LO}^{+}(t) = V_C + v_0(t) \tag{3.3}$$

$$v_{LO}^{-}(t) = V_C - v_0(t) \tag{3.4}$$

$$v_0(t) = V_0 \cos \omega_0 t \tag{3.5}$$

Here, V_C and V_0 are the DC voltage level and the amplitude of the $v_0(t)$, and ω_0 is the angular frequency of the LO. Transistor Q7 which act as the current source of the secondary differential pair is biased with constant V_B voltage.

Together with the Q5 and Q6 transistors, transistor Q7 compose a differential pair like structure with three transistors in the LO stage. This three transistor differential pair is driven by a constant current I_T via transistor Q8 which is biased with a constant voltage. The collector currents i_C^+ and i_C^- of transistors Q5 and Q6 respectively are combined to form i_C current which is the total biasing current of the primary differential pair. The collector current i_R of Q7 is formed as the residue current due to the three transistor differential pair structure. It is the remaining part of the subtraction of i_C from the total biasing current I_T of the LO stage. The residue current i_R is used as the biasing current of the secondary differential pair of the RF stage. The expressions of the biasing currents i_C and i_R are given in Section 3.2.2. By arranging the DC biasing levels of the three transistor differential pair structure in the LO stage properly, the circuit may be adjusted for the second harmonically pumped mixing. The proper biasing conditions and the effects of the biasing on the conversion voltage gain are also examined in Section 3.2.2.

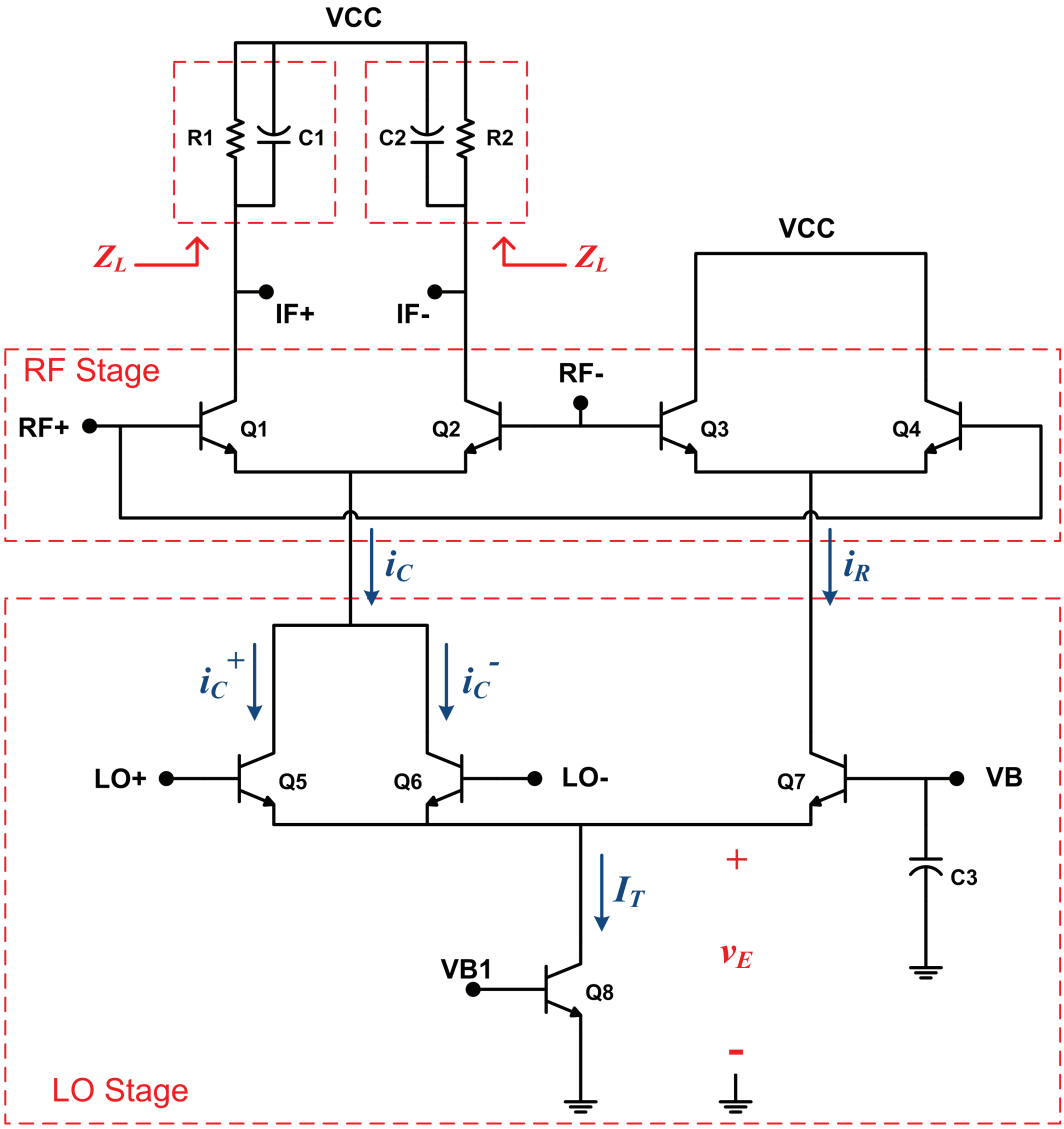

Figure 3.3 : The schematic of the proposed mixer circuit.

In the proposed topology, the primary differential pair at the RF stage which is loaded with Z_L load impedance performs the actual second harmonic mixing upon proper biasing. Load impedance Z_L on which the downconverted baseband output signal occurs is composed of parallel resistor and capacitor components. The baseband output signal which is conventionally called the intermediate frequency (IF) signal is defined as in (3.6).

$$v_{IF}(t) = V_{IF} \cos \omega_{IF} t \tag{3.6}$$

Here, V_{IF} is the amplitude and ω_{IF} is the angular frequency. The parallel R1 and C1 components for one branch and the parallel R2 and C2 on the other branch are

taken identical correspondingly for equivalent Z_L impedances on both branches. The secondary differential pair is placed as a dummy structure which is an identical copy of the primary differential pair.

Although the LO frequency is the half of the RF frequency in second harmonic mixers, there may still be an on chip leakage to RF inputs resulting in DC offset since the main pumping current i_C, as investigated in Section 3.2.2, contains the $f_{2LO} = 2 \times f_{LO}$ frequency component dominantly. Mainly via the base currents of the RF input transistors of the primary differential pair, Q1 and Q2, which are linearly a small fraction $\left({}^{1}/_{\beta}\right)$ of the biasing current and through other parasitic paths, the f_{2LO} component which is intentionally produced at the emitter ports of RF input transistors Q1 and Q2 may leak to the RF inputs. Compared to fundamental mixing mixers, the LO to RF leakage is less effective since it is limited to on chip paths. However, it is still a problem to be solved for the zero-IF mixers.

The proposed topology comprises a self balancing mechanism for the leakage resulting a noticeably high DC compression at the output. Considering that the sum of the tail currents, i_C and i_R, of the both differential pairs is constant I_T, it can be stated that the residue current i_R contains exactly the same frequency components with opposite signs with the tail current i_C of the primary differential pair. This statement is also approved with the Fourier analysis in Section 3.2.2. Thus, for all the frequency components of the pumping current leaking to RF inputs, there exist an opposite signed leakage due to the residue current and the dummy secondary differential pair. This opposite signed leakage encounters the same parasitic paths to the RF inputs with the leakage from the actual pumping current i_C due to the symmetrical structure and the layout. Therefore, the leakage of all the frequency components including the dominant f_{2LO} frequency which may result in DC offset voltage at the output is suppressed at the RF inputs.This is the main attribute of the proposed topology.

Nevertheless, the total current drawn from the supply voltage by the overall mixer circuit is the total DC current I_T which is determined by the current source transistor Q8. The pumping current i_C is split from this total current only locally to perform the mixing and then unite with the residue current at the supply terminal forming again the constant DC current I_T. Thus, the overall current drawn from the supply voltage and the power consumption of the mixer stays constant during the mixing operaiton.

The concept of flowing constant current through the supply lines satisfies an isolation between the noisy mixer and the rest of the integrated circuit in some sense. Since the fundamental LO frequency and its harmonic components do not flow through the supply and ground paths, the propagation of these frequency components to the other parts of the integrated circuit is somewhat prevented.

The theory of flowing a total constant current and splitting it into i_C and i_R currents such that i_C and i_R contain the same frequency components with opposite amplitude signs depends on the assumption that the transistor Q8 acts like an ideal current source with an infinite output impedance. It needs to be considered that the finite output impedance of the transistor Q8 may lead a minor alteration on the total biasing current I_T. To prevent this minor alteration, a current source with an improved output impedance may be used instead of the transistor Q8.

3.2.2 Circuit Analysis of the Proposed Mixer Topology

The expressions of i_C and i_R currents can be obtained from the large signal analysis of the three transistor differential pair at the LO stage. The expression of the collector currents i_C^+ and i_C^- of the transistors Q5 and Q6 driven by v_{LO}^+ and v_{LO}^- signals are given in (3.7) and (3.8) respectively. The expression of the collector current i_R of the transistor Q7 biased with the constant voltage V_B is given in (3.9).

$$i_C^+ = I_S \left(\mathrm{e}^{\frac{v_{LO}^+ - v_E}{V_T}} \right) \tag{3.7}$$

$$i_C^- = I_S \left(\mathrm{e}^{\frac{v_{LO}^- - v_E}{V_T}} \right) \tag{3.8}$$

$$i_R = I_S \left(\mathrm{e}^{\frac{V_B - v_E}{V_T}} \right) \tag{3.9}$$

Here, I_S is the saturation current, V_T is thermal voltage and the v_E is the emitter voltage of transistors Q5, Q6 and Q7. Since i_C is sum of the collector currents i_C^+ and i_C^- of Q5 and Q6, it can be written as in (3.12).

$$i_C = i_C^+ + i_C^- \tag{3.10}$$

$$i_C = I_S\left(e^{\frac{v_{LO}^{+}-v_E}{V_T}}\right) + I_S\left(e^{\frac{v_{LO}^{-}-v_E}{V_T}}\right) \tag{3.11}$$

$$i_C = I_S e^{\frac{-v_E}{V_T}}\left(e^{\frac{v_{LO}^{+}}{V_T}} + e^{\frac{v_{LO}^{-}}{V_T}}\right) \tag{3.12}$$

Depending on the fact that the sum of all the collector currents of Q5, Q6 and Q7 is equal to the total biasing current I_T, the expression for I_T can be evaluated as in from (3.13) to (3.15).

$$I_T = i_C^{+} + i_C^{-} + i_R \tag{3.13}$$

$$I_T = I_S\left(e^{\frac{v_{LO}^{+}-v_E}{V_T}}\right) + I_S\left(e^{\frac{v_{LO}^{-}-v_E}{V_T}}\right) + I_S\left(e^{\frac{V_B-v_E}{V_T}}\right) \tag{3.14}$$

$$I_T = I_S e^{\frac{-v_E}{V_T}}\left(e^{\frac{v_{LO}^{+}}{V_T}} + e^{\frac{v_{LO}^{-}}{V_T}} + e^{\frac{V_B}{V_T}}\right) \tag{3.15}$$

The expression for the term $I_S e^{\frac{-v_E}{V_T}}$ can be obtained from (3.15) as in (3.16).

$$I_S e^{\frac{-v_E}{V_T}} = \frac{I_T}{e^{\frac{v_{LO}^{+}}{V_T}} + e^{\frac{v_{LO}^{-}}{V_T}} + e^{\frac{V_B}{V_T}}} \tag{3.16}$$

When the expression for the term $I_S e^{\frac{-v_E}{V_T}}$ given in (3.16) and the expressions of v_{LO}^{+} and v_{LO}^{-} given in (3.3) and (3.4) respectively are used in the expression of the total pumping current i_C given in (3.12), the expression for i_C is obtained as in (3.21) upon evaluation from (3.17) to (3.21).

$$i_C = \frac{I_T}{e^{\frac{v_{LO}^{+}}{V_T}} + e^{\frac{v_{LO}^{-}}{V_T}} + e^{\frac{V_B}{V_T}}}\left(e^{\frac{v_{LO}^{+}}{V_T}} + e^{\frac{v_{LO}^{-}}{V_T}}\right) \tag{3.17}$$

$$i_C = \frac{I_T}{1 + \frac{e^{\frac{V_B}{V_T}}}{e^{\frac{v_{LO}^{+}}{V_T}} + e^{\frac{v_{LO}^{-}}{V_T}}}} \tag{3.18}$$

$$i_C = \frac{I_T}{1 + \frac{e^{\frac{V_B}{V_T}}}{e^{\frac{V_C}{V_T}}\left(e^{\frac{v_0(t)}{V_T}} + e^{-\frac{v_0(t)}{V_T}}\right)}} \tag{3.19}$$

$$i_C = \frac{I_T}{1 + \frac{e^{\frac{V_B - V_C}{V_T}}}{e^{\frac{v_0(t)}{V_T}} + e^{-\frac{v_0(t)}{V_T}}}} \tag{3.20}$$

$$i_C = \frac{I_T}{1 + \frac{A}{e^{\frac{v_0(t)}{V_T}} + e^{-\frac{v_0(t)}{V_T}}}} \tag{3.21}$$

Here $v_0(t)$ is as defined in (3.5) and A is a constant defined by the DC biasing conditions of the LO stage. As it can be seen from the definition of A given in (3.22), it is value is defined only by $V_B - V_C$ voltage difference.

$$A = e^{\frac{V_B - V_C}{V_T}} \tag{3.22}$$

The expression of i_C given in (3.21) can be rewritten as in (3.24) by applying the proper trigonometric transformation given in (3.23).

$$\text{sech(x)} = \frac{2}{e^x + e^{-x}} \tag{3.23}$$

$$i_C = \frac{I_T}{1 + \frac{A}{2}\text{sech}\left(\frac{v_0(t)}{V_T}\right)} \tag{3.24}$$

The final expression of the total pumping current i_C can be obtained as in (3.25) by using the definition of $v_0(t)$ given in (3.5).

$$i_C = \frac{I_T}{1 + \frac{A}{2}\text{sech}\left(\frac{V_0}{V_T}\cos\omega_0 t\right)} \tag{3.25}$$

Let a transfer function TF_C is defined for the transformation from the sinusoidal term of the LO signal $v_0(t)$ to the pumping current i_C as in (3.26). This transfer fucntion is used for further investigation of the generation of the pumping current i_C.

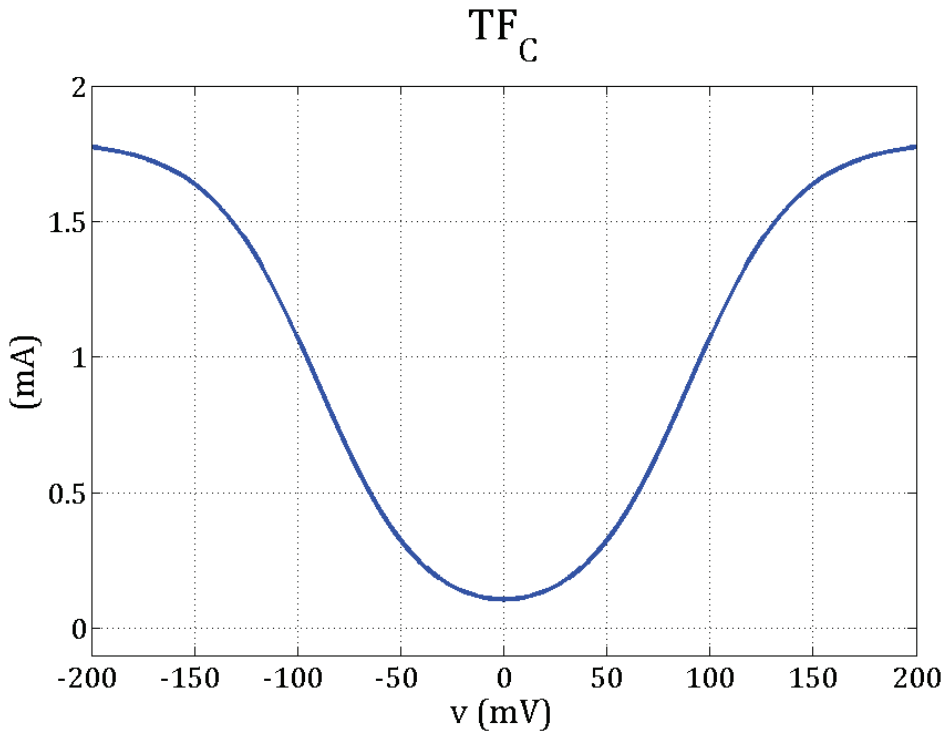

Figure 3.4 : Transfer function TF_C according to independent variable v.

$$i_C(t) = TF_C(v_0(t)) \Rightarrow TF_C(v) = \frac{I_T}{1 + \frac{A}{2}\text{sech}\left(\frac{1}{V_T}v\right)} \tag{3.26}$$

Here v is used as an independent variable for the transfer function TF_C. When the time varying signal $v_0(t)$ is applied, the transfer function TF_C converts it to time varying pumping current $i_C(t)$.

The obtained transfer function TF_C is an even function because of the hyperbolic trigonometric function sech it contains. As a result of this transfer function, i_C consists of only the even harmonics of the LO frequency f_0 which is $\omega_0/2\pi$. The curve of the transfer function TF_C according to the independent variable v is given in Figure 3.4. The illustration of conversion from the sinusoidal term of the LO signal $v_0(t)$ to pumping current i_C is shown in Figure 3.5. In this figure, the graph of the transfer function TF_C is given together with the graphs of $v_0(t)$ and $i_C(t)$. The axes of all three graphs in Figure 3.5 are scaled according to each other. It is shown that for a single period of the $v_0(t)$ signal, two periods of $i_C(t)$ current are produced as a result.

From Figure 3.5, the effects of the biasing dependent variables I_T and A on $i_C(t)$ can be observed. I_T is an upper limit for the amplitude of i_C while A is a parameter to decrease the lower rail for the $i_C(t)$ swing towards zero. While keeping the DC biasing

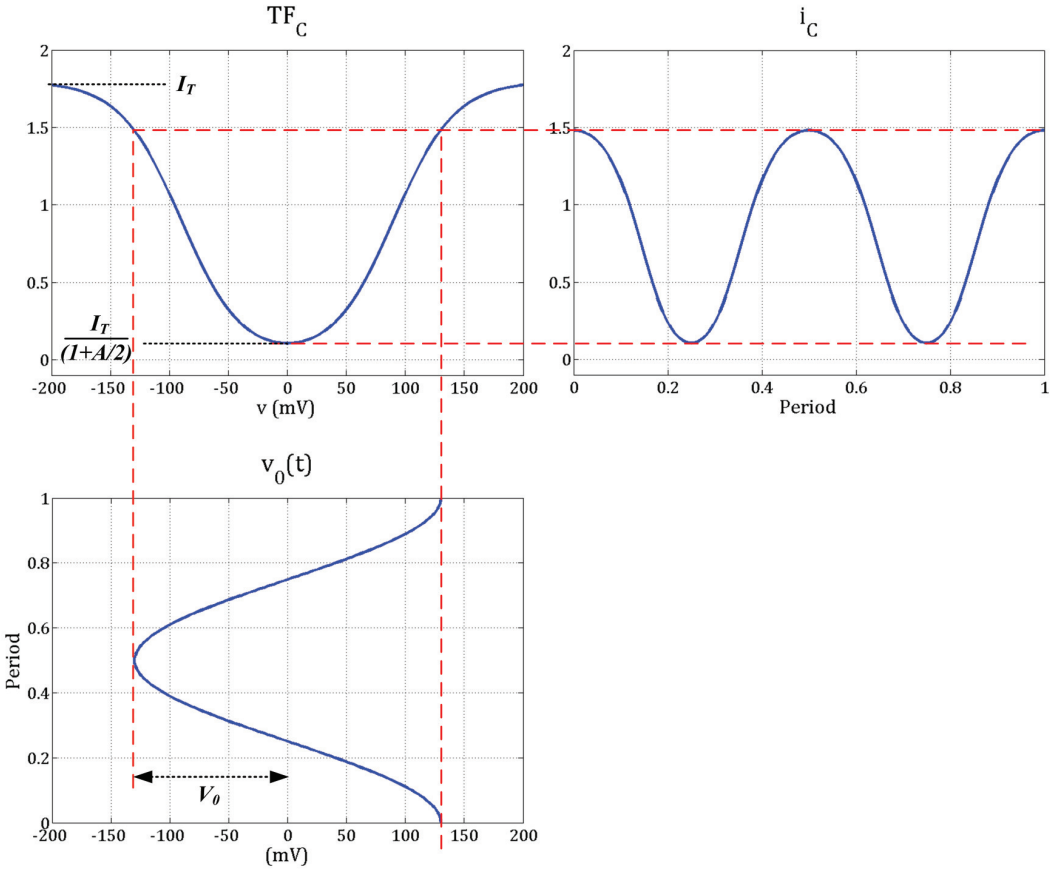

Figure 3.5 : Conversion from $v_0(t)$ to $i_C(t)$ via transfer function TF_C.

conditions suitable for proper functionality of the circuit, the values of both A and V_0 should be kept as large as possible. As A and V_0 are increased, they enlarge the amplitude of resulting pumping current where the value of A is directly determined by the voltage difference $V_B - V_C$.

The impact of the value of A on the linearity of the transfer function TF_C is observed in Figure 3.6. The Figure 3.6 contains plots of TF_C for different values of A. The voltage difference, $V_B - V_C$, is changed from 30 mV to 180 mV with 30 mV steps to obtain the values of A annotated in the legend of the graph. The other parameter, I_T, in the equation of TF_C given in (3.26) is kept constant at 1.8 mA, which is the value used for the circuit simulations.

To emphasize the effect of the value of A on the amplitude and linearity of the resulting i_C current, Figure 3.7 shows i_C currents generated from the same $v_0(t)$ signals with the same amplitudes V_0. For the $v_0(t)$ signals, V_0 is selected to be 110 mV, which is the value also used in the circuit simulations. From visual inspection on Figure 3.7, the best i_C current in linearity can be selected as the one plotted with black color which is

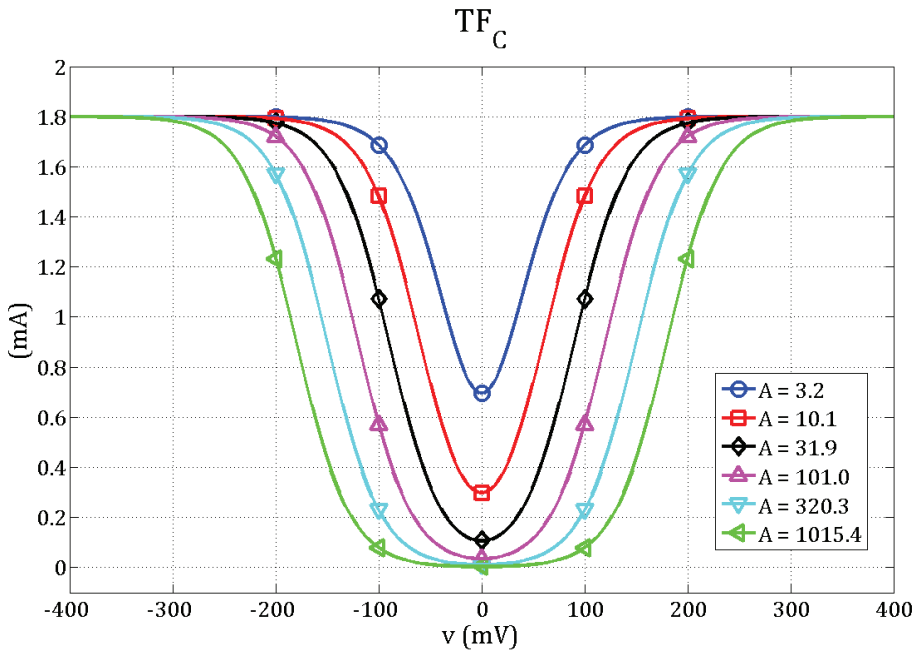

Figure 3.6 : The change of TF_C for different values of A.

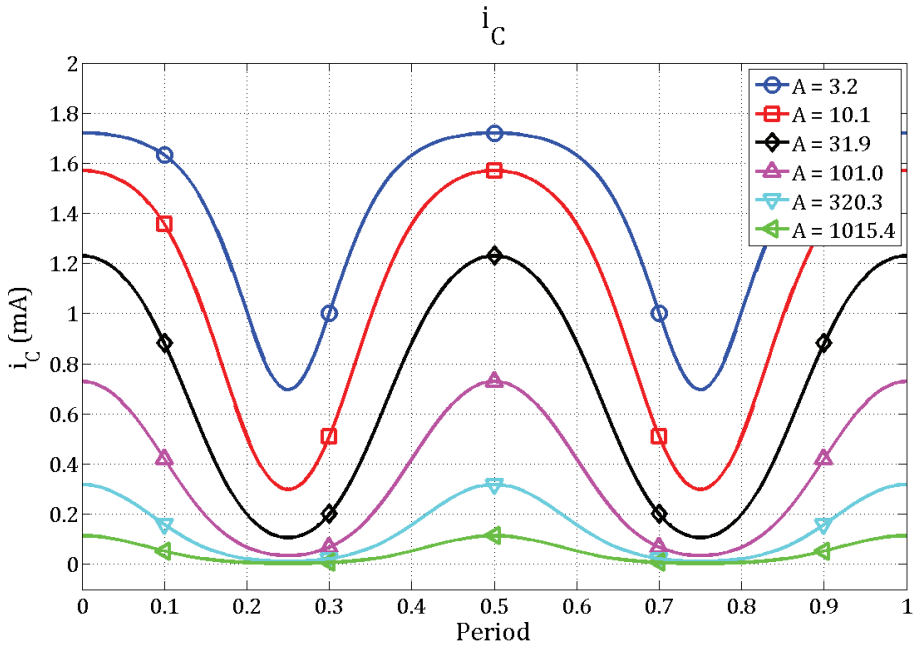

Figure 3.7 : Different i_C currents obtained form the same $v_0(t)$ for different values of A.

obtained for A=31.9. This result is interpreted such that there exists an optimum value of A regarding linearity for a given V_0.

When spectrum analysis of the i_C currents from Figure 3.7 is performed for three cases of A; A=3.2, A=31.9 and A=320.3, i_C for A=31.9 appears to be the most linear one with the largest second harmonic component and lowest other harmonics. The

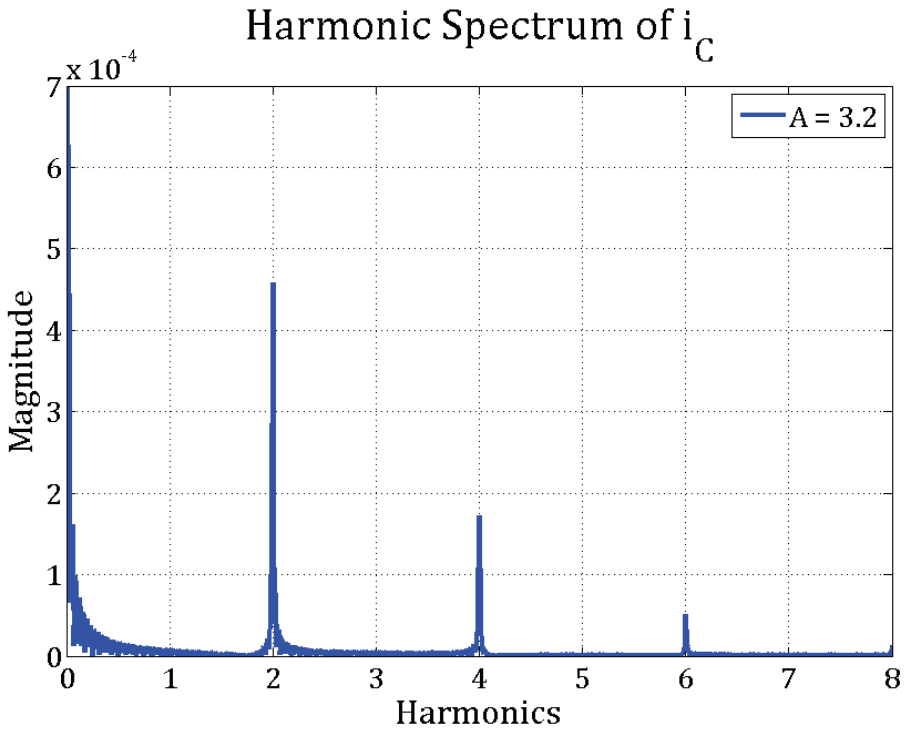

Figure 3.8 : Harmonic spectrum of i_C for A=3.2.

spectrum analysis of the three cases are shown in Figure 3.8, Figure 3.9 and Figure 3.10 respectively. In the Figures, the analysis are performed over one hundred periods of the LO signal and the harmonics up to eight are shown. As proposed, the total pumping current, i_C, does not include any odd harmonics of LO signal, it consists of even harmonics.

Similarly, the expression of the residue current i_R is evaluated from (3.9) by substituting the term $I_S e^{\frac{-v_E}{V_T}}$ with the equation obtained for it in (3.16). The evaluation of the expression of i_R is given in form (3.27) to (3.34).

$$i_R = \frac{I_T}{e^{\frac{v_{LO}^+}{V_T}} + e^{\frac{v_{LO}^-}{V_T}} + e^{\frac{V_B}{V_T}}} \left(e^{\frac{V_B}{V_T}} \right) \tag{3.27}$$

$$i_R = \frac{I_T}{1 + \frac{e^{\frac{v_{LO}^+}{V_T}} + e^{\frac{v_{LO}^-}{V_T}}}{e^{\frac{V_B}{V_T}}}} \tag{3.28}$$

When definitions of v_{LO}^+ and v_{LO}^- given in (3.3) and (3.4) respectively are used in (3.28), (3.29) is obtained.

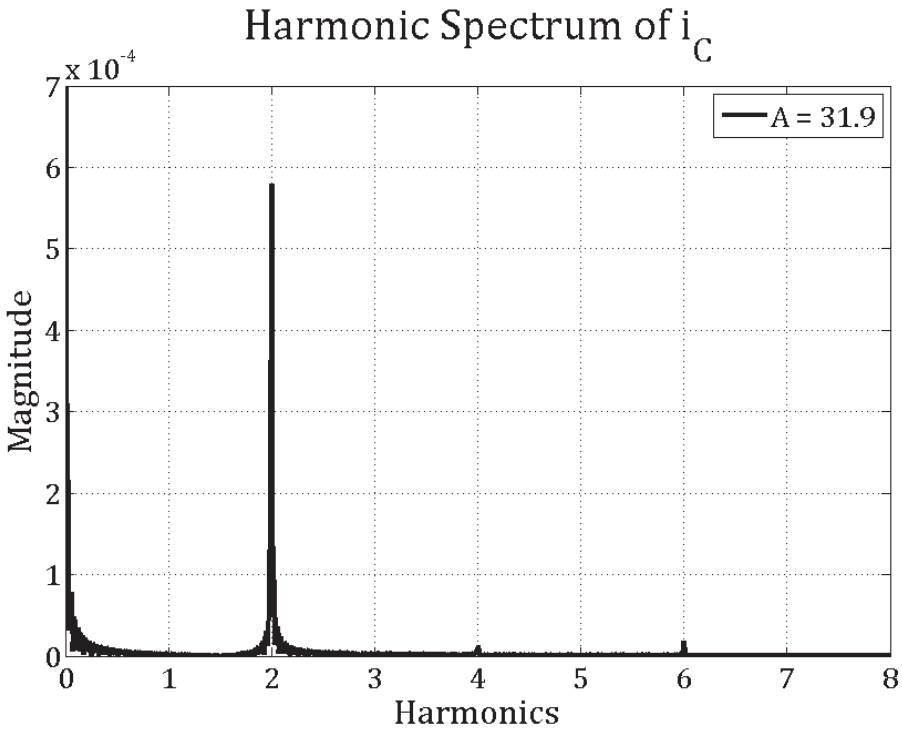

Figure 3.9 : Harmonic spectrum of i_C for A=31.9.

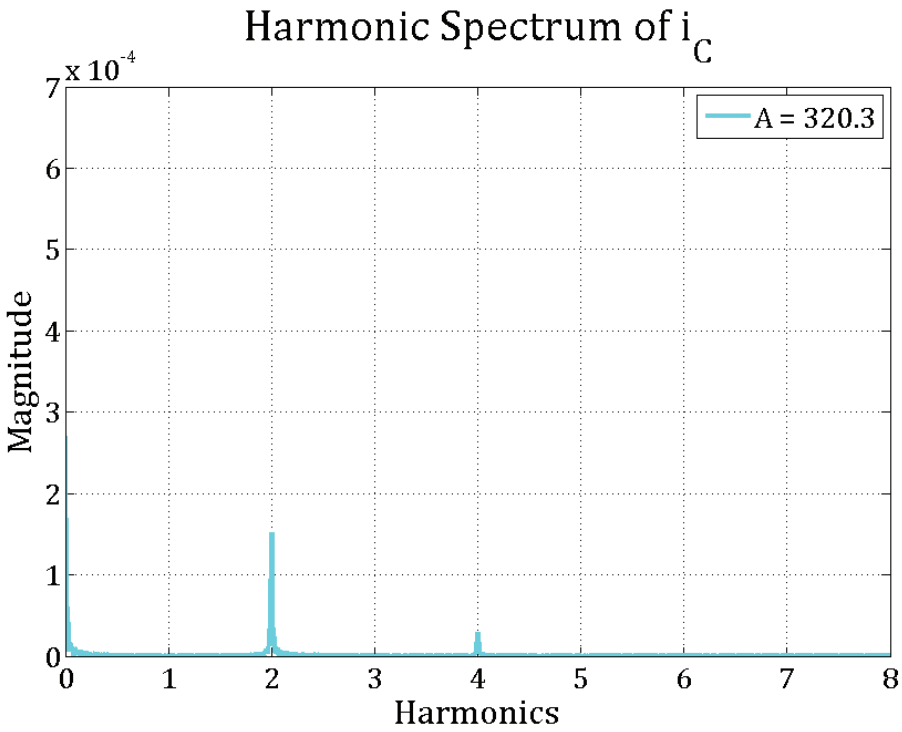

Figure 3.10 : Harmonic spectrum of i_C for A=320.3.

$$i_R = \frac{I_T}{1 + \frac{e^{\frac{V_C}{V_T}}\left(e^{\frac{v_0(t)}{V_T}} + e^{\frac{-v_0(t)}{V_T}}\right)}{e^{\frac{V_B}{V_T}}}} \tag{3.29}$$

$$i_R = \frac{I_T}{1 + \frac{e^{\frac{v_0(t)}{V_T}} + e^{\frac{-v_0(t)}{V_T}}}{e^{\frac{V_B - V_C}{V_T}}}} \tag{3.30}$$

$$i_R = \frac{I_T}{1 + \frac{e^{\frac{v_0(t)}{V_T}} + e^{\frac{-v_0(t)}{V_T}}}{A}} \tag{3.31}$$

Here, A is a bias dependent constant used for simplification in the expression. The definition of A is given in (3.22). It the same constant used in the expression of i_C current. When proper trigonometric conversion is applied to (3.31), the expression in (3.33) is obtained. The definition for the hyperbolic trigonometric function $\cosh(\mathrm{x})$ is given in (3.32).

$$\cosh(\mathrm{x}) = \frac{e^x + e^{-x}}{2} \tag{3.32}$$

$$i_R = \frac{I_T}{1 + \frac{2}{A}\cosh\left(\frac{v_0(t)}{V_T}\right)} \tag{3.33}$$

When the definition $v_0(t)$ given in (3.5) is used in (3.33), the final expression of the residue current i_R is obtained as in (3.34). From the final expression of the residue current i_R given in (3.34), it is concluded that the residue current i_R also is a result of an even transfer function. When the harmonic spectrum analysis of i_R is investigated, it is seen that the residue current contains only the even harmonics of LO signal, dominantly the second harmonic.

$$i_R = \frac{I_T}{1 + \frac{2}{A}\cosh\left(\frac{V_0}{V_T}\cos\omega_0 t\right)} \tag{3.34}$$

Let a transfer function TF_R is defined for the transformation from the sinusoidal term of the LO signal $v_0(t)$ to the residue current i_R as in (3.35) to investigate the generation of the residue current i_R.

$$i_R(t) = TF_R(v_0(t)) \Rightarrow TF_R(v) = \frac{I_T}{1 + \frac{2}{A}\cosh\left(\frac{1}{V_T}v\right)} \tag{3.35}$$

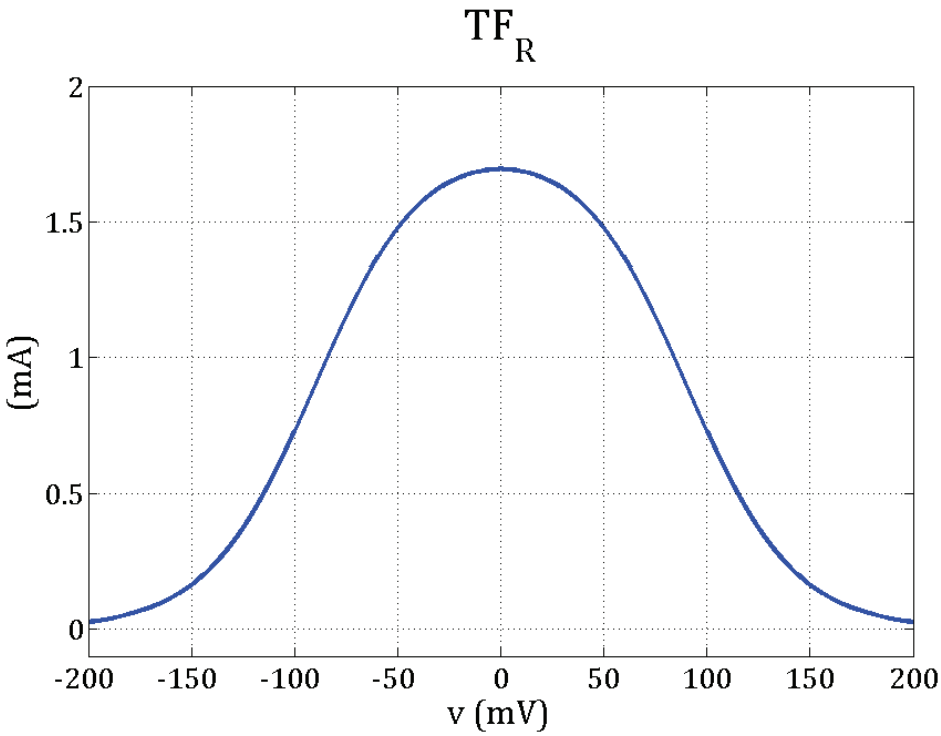

Figure 3.11 : Transfer function TF_R according to independent variable v.

Here v is used as an independent variable for the transfer function TF_R. When the time varying signal $v_0(t)$ is applied, the transfer function TF_R converts it to time varying residue current $i_R(t)$.

The obtained transfer function TF_R is an even function because of the hyperbolic trigonometric function cosh. The curve of the transfer function TF_R according to the independent variable v is given in Figure 3.11.

Figure 3.12 and Figure 3.13 are given to show the change of TF_R and i_R according to A. For comparison, the graphs are obtained with the same parameter values as they are done for TF_C and i_C in Figure 3.6 and Figure 3.7 respectively. The voltage difference, $V_B - V_C$, is changed from 30 mV to 180 mV with 30 mV steps to obtain for the annotated values of A and I_T in the equation of TF_R given in (3.35) is kept constant at 1.8 mA.

When the spectrum analysis is performed on i_R, the results given in Figure 3.14, Figure 3.15 and Figure 3.16 are obtained. These results are given for different values of A as annotated on the graphs. For comparison with the harmonic spectrum graphs obtained for i_C, The exact same biasing conditions are used upon analysis. It is seen that as proposed, the harmonics have the same magnitudes for the same biasing

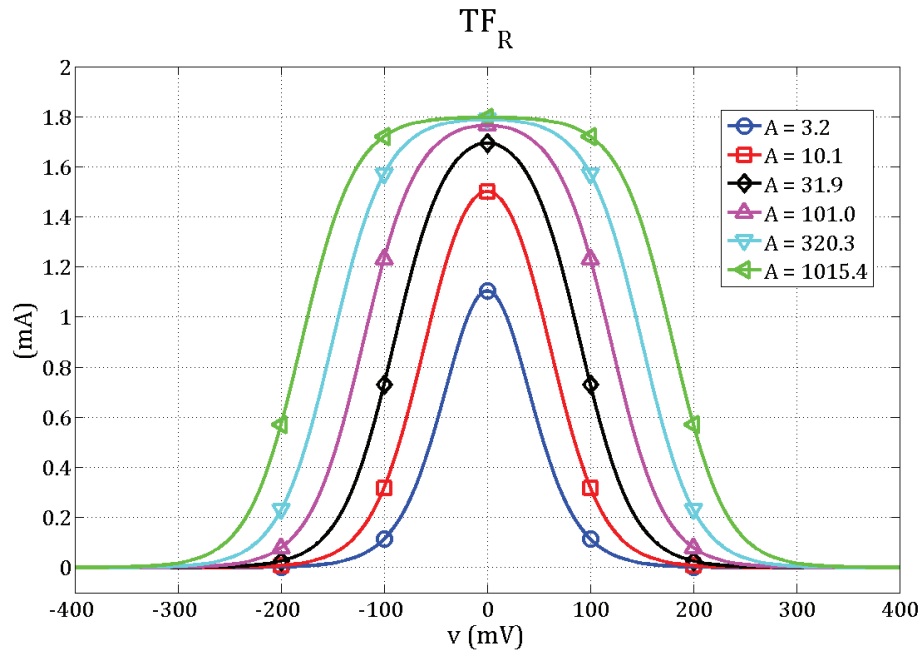

Figure 3.12 : The change of TF_R for different values of A.

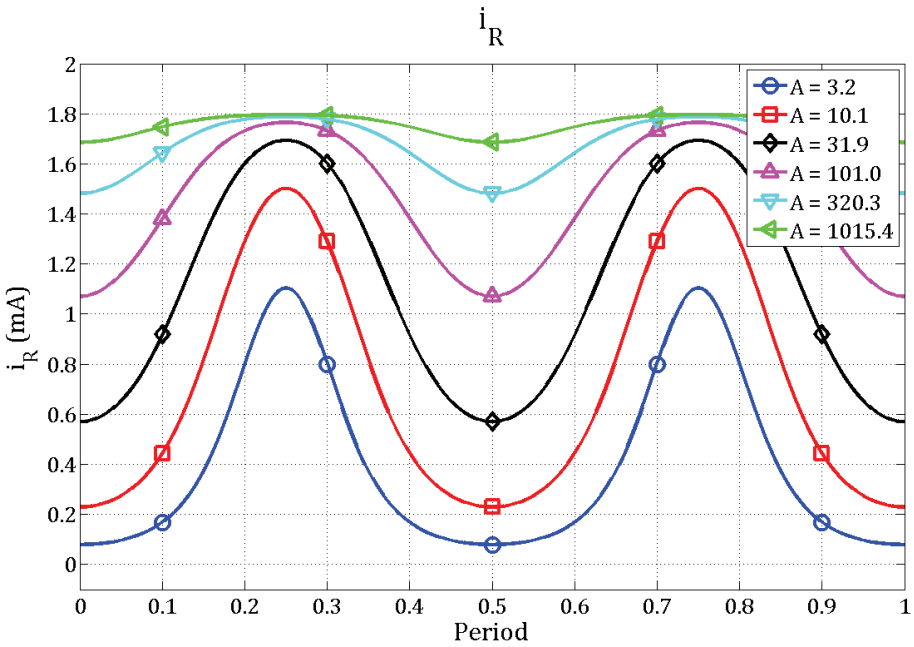

Figure 3.13 : Different i_R currents obtained form the same $v_0(t)$ for different values of A.

conditions for both i_C and i_R. However, from the spectrum analysis and also from the transient curves of i_C and i_R given in Figure 3.7 and Figure 3.13, it is observed that the DC levels of both currents are different when they are biased with the most efficient value of A. For the example case given in the graphs, the value of A at which the magnitude of second harmonic component of i_C and i_R is maximum and other

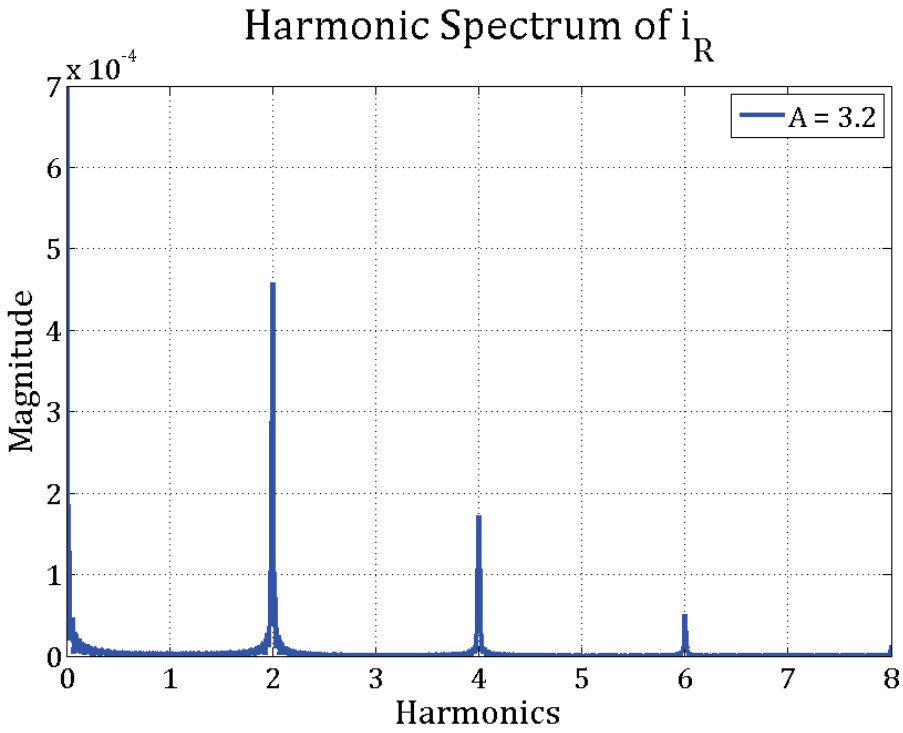

Figure 3.14 : Harmonic spectrum of i_R for A=3.2.

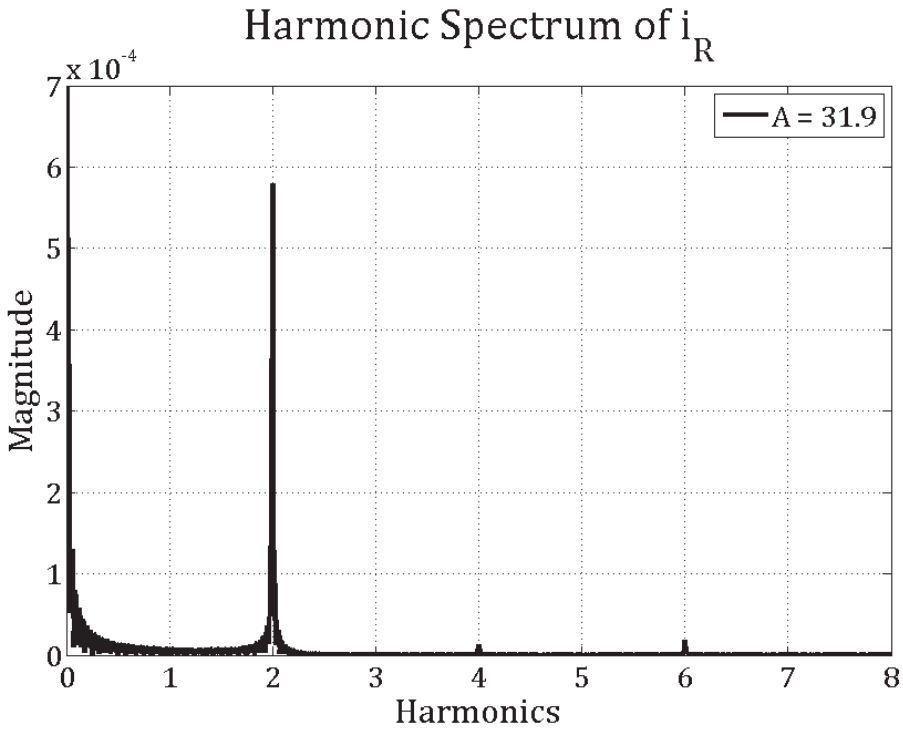

Figure 3.15 : Harmonic spectrum of i_R for A=31.9.

harmonic components are low is found to be 31.9. When I_T and V_0 are kept constant at 1.8 mA and 110 mV respectively, as it is done in all the graphics, the resultant i_C and i_R currents are obtained as in Figure 3.17.

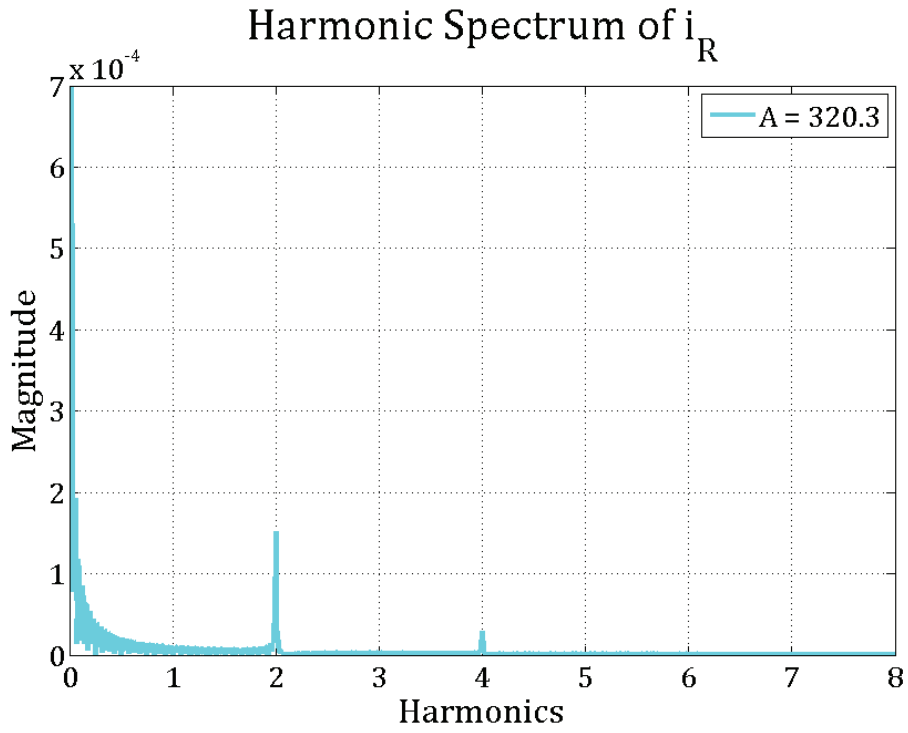

Figure 3.16 : Harmonic spectrum of i_R for A=320.3.

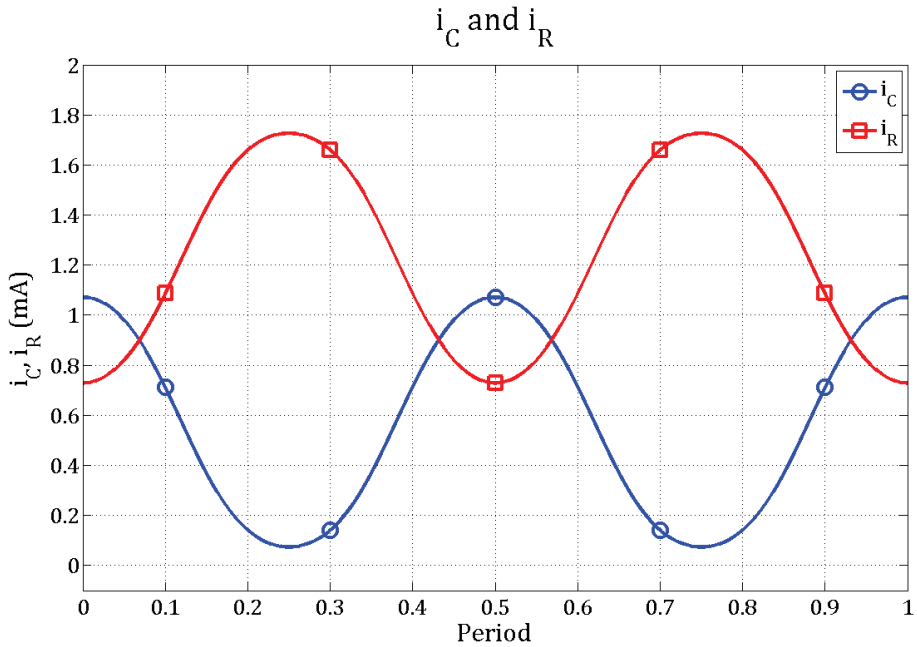

Figure 3.17 : i_C and i_R currents for A=31.9.

Since both i_C and i_R currents are even functions of time, they can be expressed by the Fourier series expansion for even functions given in (3.36). The equation for the Fourier series coefficients $i_{\{C,R\}n}$ is given in (3.37).

$$i_{\{C,R\}} = i_0 + 2\sum_{n=1}^{\infty} i_{\{C,R\}n}\cos n\omega_0 t \tag{3.36}$$

$$i_{\{C,R\}n} = \frac{1}{2\pi}\int_{-\pi}^{\pi} i_{\{C,R\}}\cos n\theta \mathrm{d}\theta, n = \{0,1,2,\dots\} \tag{3.37}$$

Here θ is defined as in (3.38).

$$\theta = \omega_0 t \tag{3.38}$$

When the expression of i_C and i_R given in (3.25) and (3.34) are used in (3.37) and evaluated, (3.39) and (3.40) are obtained for Fourier coefficients of i_C and i_R respectively.

$$i_{Cn} = \frac{I_T}{2\pi}\int_{-\pi}^{\pi} \frac{\cos n\theta}{1+\frac{A}{2}\mathrm{sech}\left(\frac{V_0}{V_T}\cos\theta\right)}\mathrm{d}\theta, n = \{0,1,2,\dots\} \tag{3.39}$$

$$i_{Rn} = \frac{I_T}{2\pi}\int_{-\pi}^{\pi} \frac{\cos n\theta}{1+\frac{2}{A}\cosh\left(\frac{V_0}{V_T}\cos\theta\right)}\mathrm{d}\theta, n = \{0,1,2,\dots\} \tag{3.40}$$

Calculation of (3.39) and (3.40) reveals more information about the harmonics of i_C and i_R currents. Figure 3.18, Figure 3.19 and Figure 3.20 show the change of DC component and second and fourth harmonics of i_C according to voltage difference $V_B - V_C$ respectively. Since the all the odd harmonics are suppressed and very close to zero no graphs for the odd harmonics are given. The given three graphs in Figure 3.18, Figure 3.19 and Figure 3.20 represents the harmonic components with the largest coefficients.

From Figure 3.19, it is seen that the second harmonic coefficient i_{C2} is maximized for an optimum value of $V_B - V_C$. Besides, the fourth harmonic coefficient, i_{C4}, passes from zero in the vicinity of the biasing point at which the second harmonic coefficient is at its maximum. Therefore, an optimum biasing voltage difference $V_B - V_C$ can be found from the graphics given in Figure 3.18, Figure 3.19 and Figure 3.20 for a maximum second harmonic and a minimum fourth harmonic considering the linearity and the efficiency. Due to the differential pair structure of the LO stage, the increase in the biasing voltage difference $V_B - V_C$ causes also the DC component of i_C to decrease.

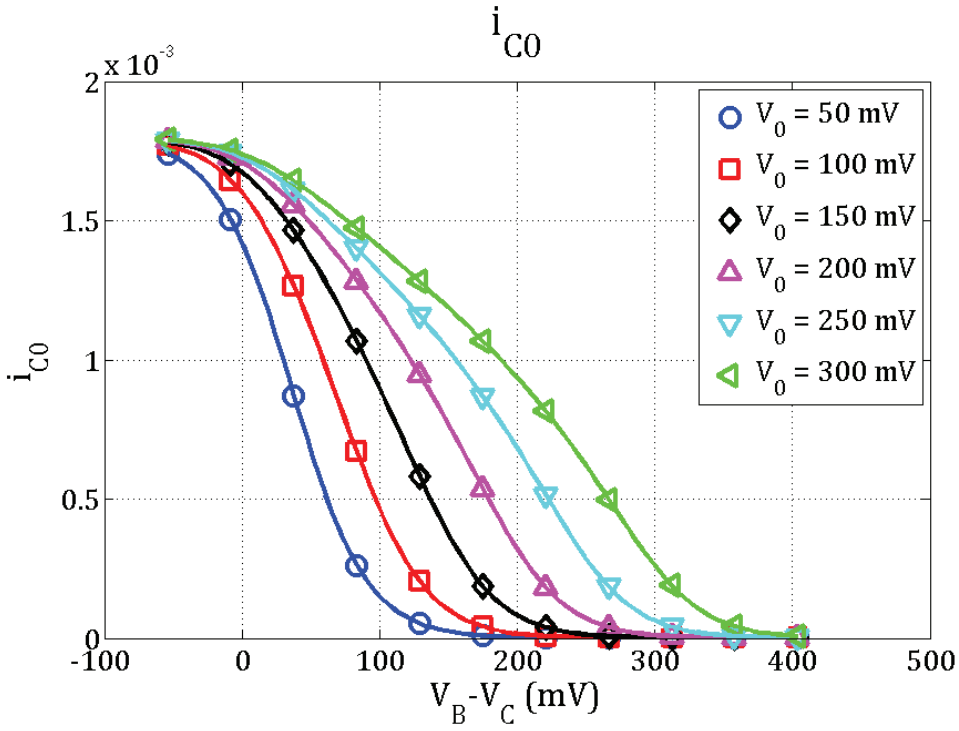

Figure 3.18 : The variation of the DC component coefficient of i_C current according to $V_B - V_C$ voltage difference for different values of V_0.

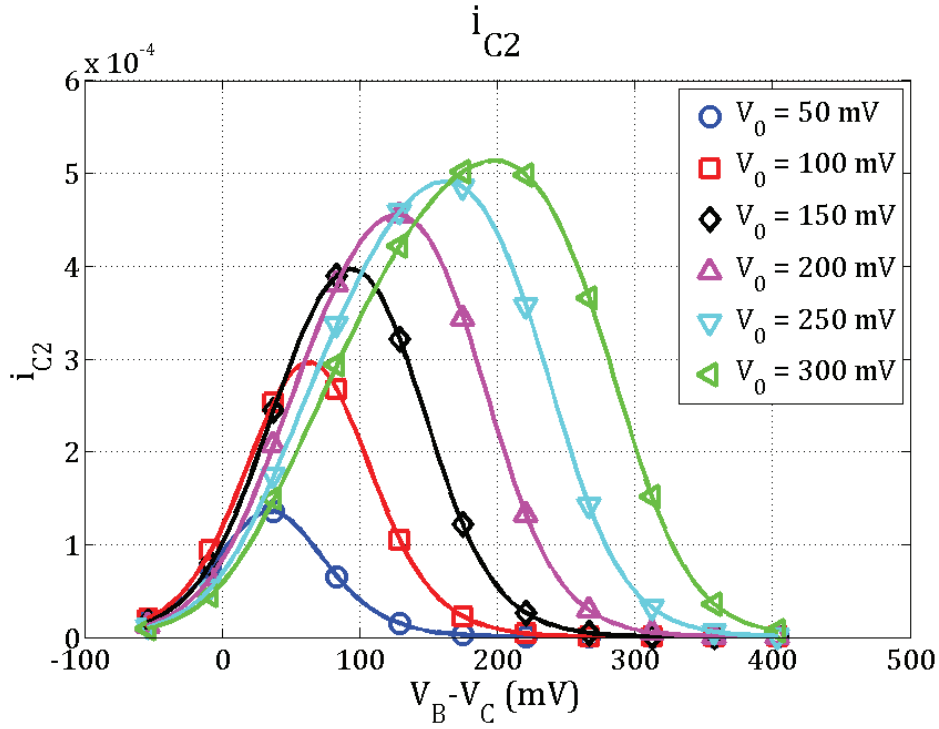

Figure 3.19 : The variation of the second harmonic coefficient of i_C current according to $V_B - V_C$ voltage difference for different values of V_0.

Similarly, Figure 3.21, Figure 3.22 and Figure 3.23 show the change of DC component and second and fourth harmonics of i_R according to voltage difference $V_B - V_C$

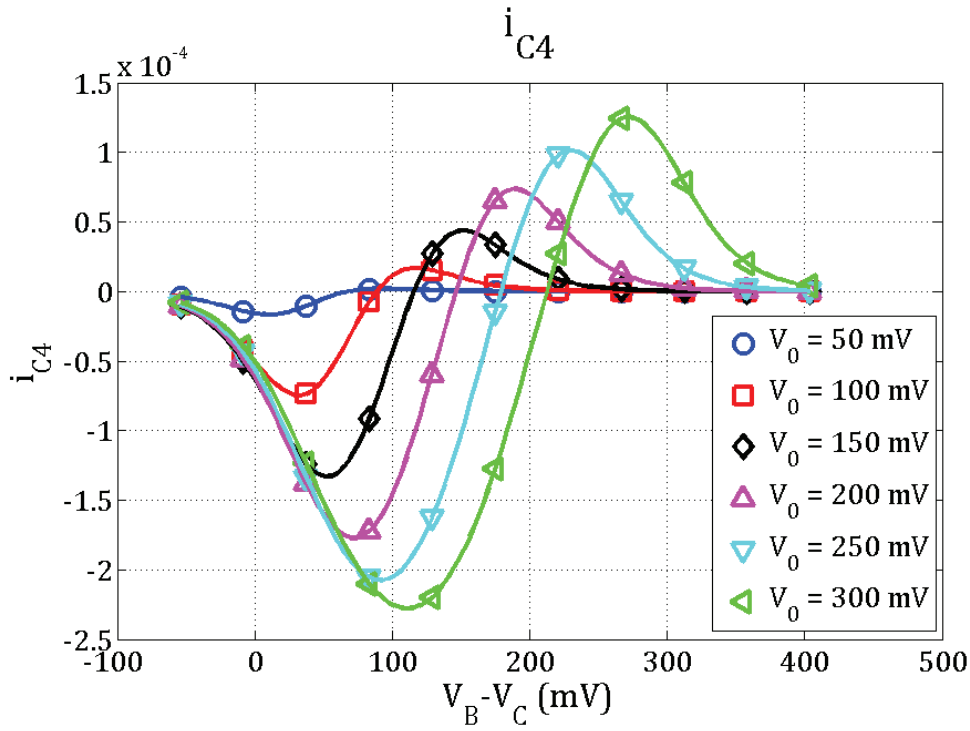

Figure 3.20 : The variation of the fourth harmonic coefficient of i_C current according to $V_B - V_C$ voltage difference for different values of V_0.

respectively. The sweep range and the parameter values for V_0 are taken same with the values used for the analysis of i_C. It is verified that under the same biasing conditions, the residue current i_R has exactly the same harmonic components with i_C with opposite signs.

As a result, in the proposed second harmonic mixer topology, the pumping current i_C is used to vary the input transconductance of the mixer to satisfy the desired mixing. To find the expression of the input transconductance g_m, the relation between the collector current and the transconductance of a transistor is used. There is a linear relation between the collector current I_C and the transconductance g_m of a bipolar transistor as given in (3.41).

$$g_m = \frac{I_C}{V_T} \tag{3.41}$$

Here, I_C is the collector current of a bipolar transistor and V_T is the thermal voltage. Since only the half of the i_C current flows through each of the RF input transistors of the primary differential pair Q1 and Q2, the collector currents of these transistors can

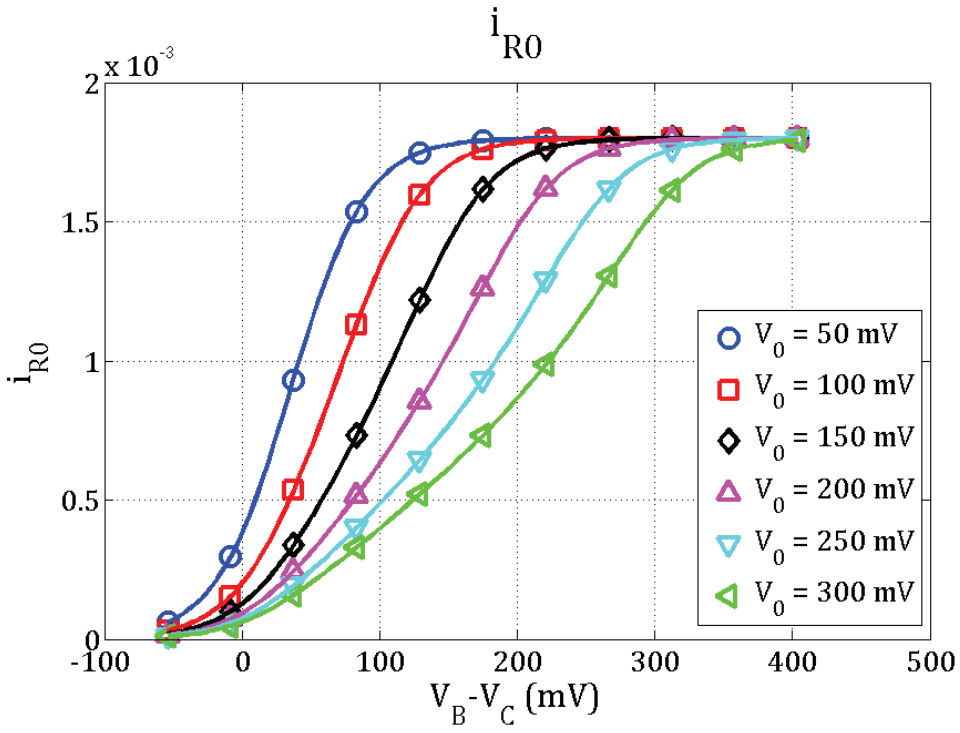

Figure 3.21 : The variation of the DC component coefficient of i_R current according to $V_B - V_C$ voltage difference for different values of V_0.

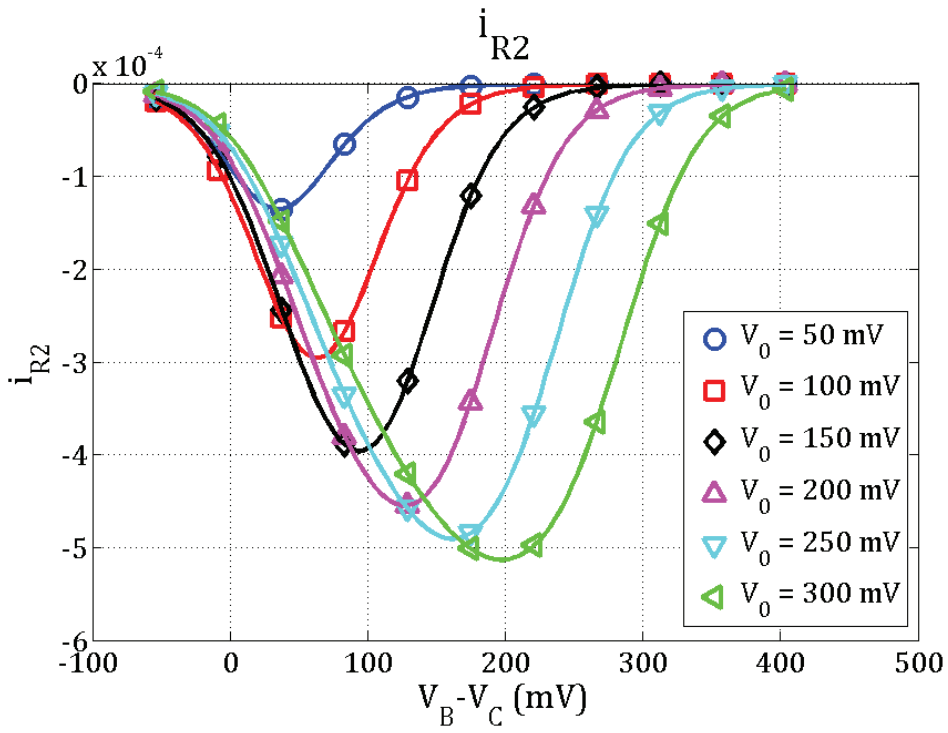

Figure 3.22 : The variation of the second harmonic coefficient of i_R current according to $V_B - V_C$ voltage difference for different values of V_0.

be shown as in (3.42). Therefore the transconductance g_m of the input transistors Q1 and Q2 can be expressed as in (3.43)

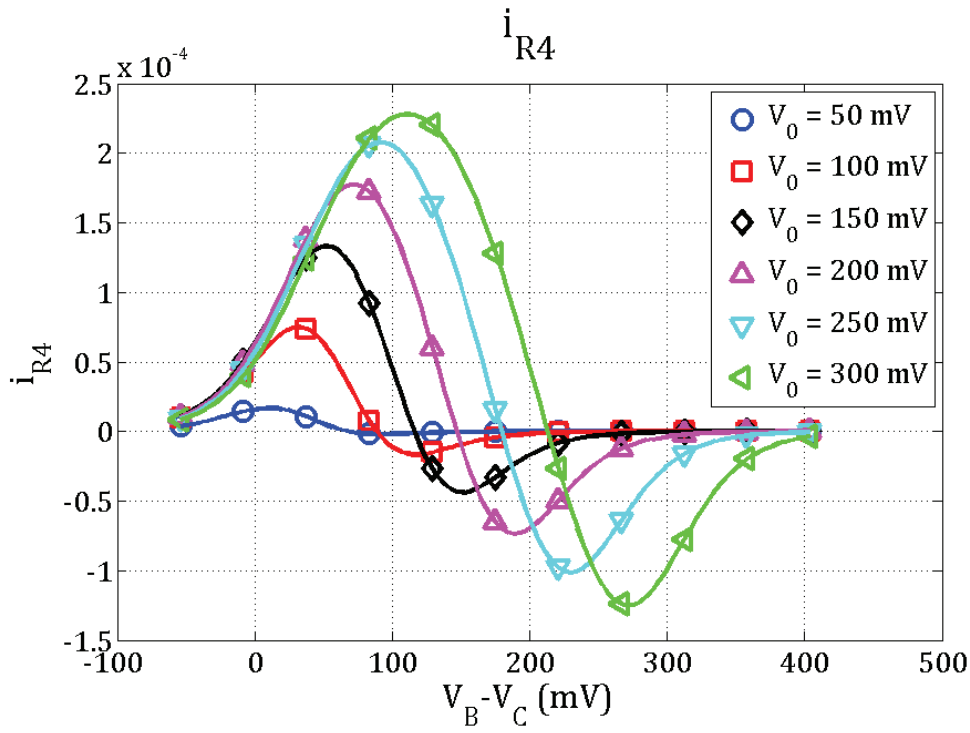

Figure 3.23 : The variation of the fourth harmonic coefficient of i_R current according to $V_B - V_C$ voltage difference for different values of V_0.

$$I_C = \frac{i_C}{2} \tag{3.42}$$

$$g_m = \frac{i_C}{2V_T} \tag{3.43}$$

By using the equation of i_C given in (3.25) in (3.43), the expression for the g_m of the RF input transistors is obtained as in (3.44). As it is mentioned previously, due to the linear relation between g_m and collector current, g_m contains exactly the same frequency components with i_C which means that the g_m is also an even function. Thus, the Fourier series expansion for even functions can be used to express the g_m as in (3.45).

$$g_m = \frac{I_T}{2V_T}\left(1 + \frac{A}{2}\text{sech}\left(\frac{V_0}{V_T}\cos\omega_0 t\right)\right)^{-1} \tag{3.44}$$

$$g_m = g_{m0} + 2\sum_{n=1}^{\infty} g_{mn}\cos n\omega_0 t \tag{3.45}$$

Here, A is defined as in (3.22) and the g_{mn} is the n^{th} Fourier coefficient. By using (3.44) in the general definition given in (3.46) for the calculation of the Fourier series coefficients, the equation given in (3.47) is obtained. θ in (3.46) and (3.47) is as defined previously in (3.38).

$$g_{mn} = \frac{1}{2\pi} \int_{-\pi}^{\pi} g_m \cos n\theta \, \mathrm{d}\theta, n = \{0, 1, 2, \dots\} \tag{3.46}$$

$$g_{mn} = \frac{I_T}{4\pi V_T} \int_{-\pi}^{\pi} \frac{\cos n\theta}{1 + \frac{A}{2}\operatorname{sech}\left(\frac{V_0}{V_T}\cos\theta\right)} \mathrm{d}\theta, n = \{0, 1, 2, \dots\} \tag{3.47}$$

From the Fourier analysis of the g_m of which expression is given in (3.44), it is verified that the transconductance is mainly composed of the even harmonics of the LO and does not contain any odd harmonics. The harmonic components of g_m is important since the RF signal is converted into baseband by being multiplied by the g_m of the RF input transistors. Therefore, the elimination of the odd harmonics from the total transconductance variation prevents fundamental mixing products at the output. The Fourier coefficients of the DC, second harmonic and fourth harmonic components of the g_m are plotted in Figure 3.24, Figure 3.25 and Figure 3.26. In the graphs, the variation of the coefficients according to the biasing voltage difference $V_B - V_C$ for different values of V_0 are shown. The sweep range and the parameter values are taken same with the values used for i_C and i_R analysis for convenient comparison.

The differential output IF current, i_{IF}, is directly proportional with the product of time varying transconductance $g_m(t)$, and the differential input RF voltage $v_{RF}(t)$, as given in (3.48). The definition of the RF input signal $v_{RF}(t)$, is given in (3.1).

$$i_{IF}(t) = v_{RF}(t) g_m(t) \tag{3.48}$$

When $v_{RF}(t)$ is substituted by its definition in (3.1) and $g_m(t)$ is replaced by the general Fourier expansion expression given in (3.45), through evaluation from (3.49) to (3.52), by performing the appropriate trigonometric conversion, (3.52) is obtained as the expression of the $i_{IF}(t)$ current at the output of the primary differential pair.

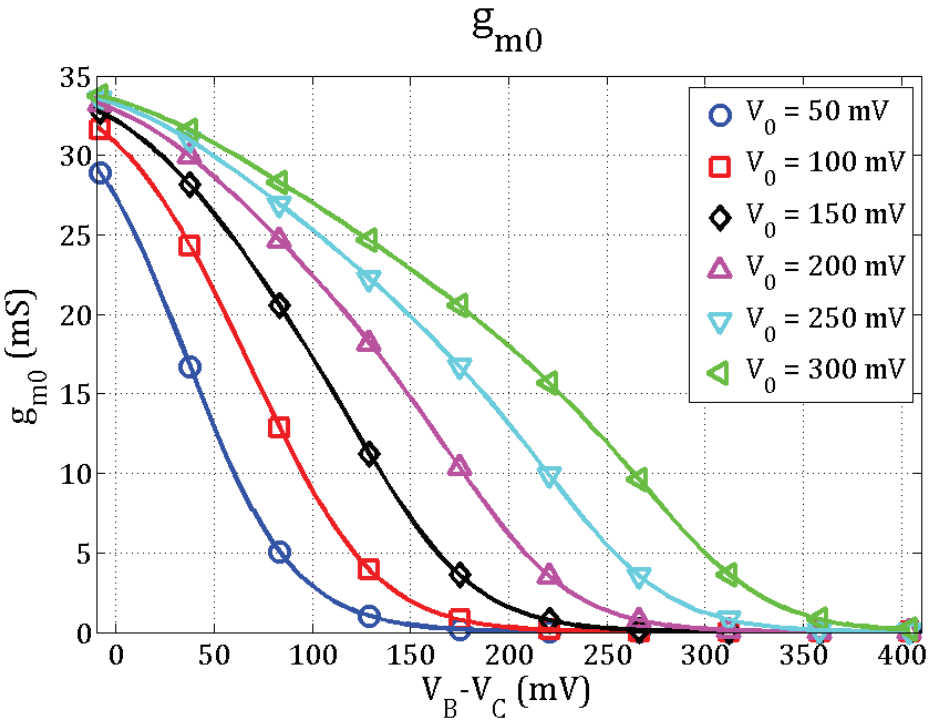

Figure 3.24 : The variation of the DC component coefficient of g_m according to $V_B - V_C$ voltage difference for different values of V_0.

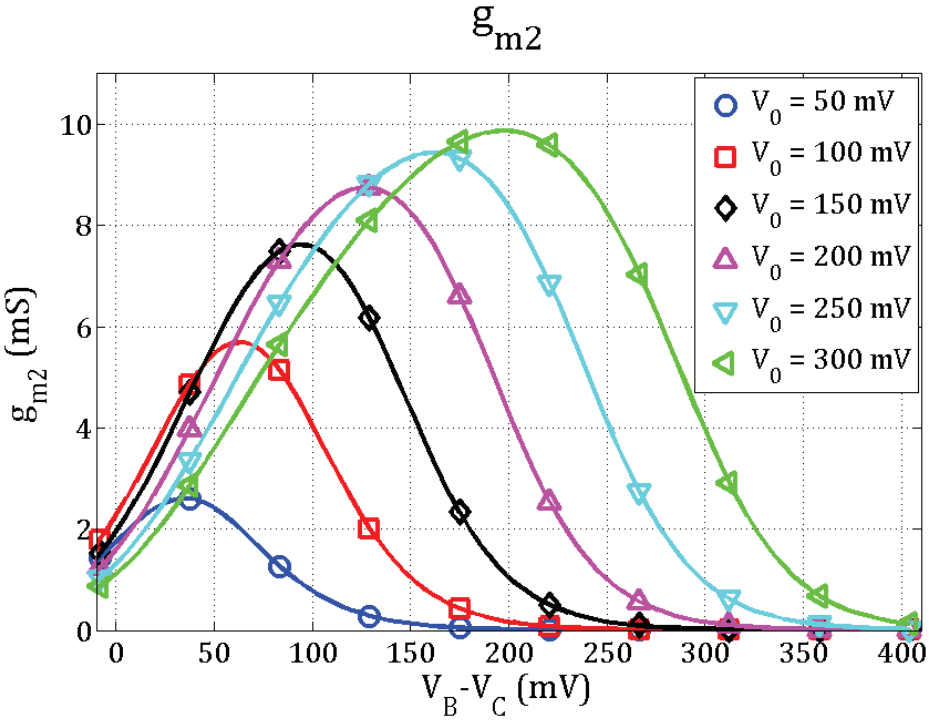

Figure 3.25 : The variation of the second harmonic coefficient of g_m according to $V_B - V_C$ voltage difference for different values of V_0.

$$i_{IF}(t) = (V_{RF}\cos\omega_{RF}t)\left(g_{m0} + 2\sum_{n=1}^{\infty} g_{mn}\cos n\omega_0 t\right) \tag{3.49}$$

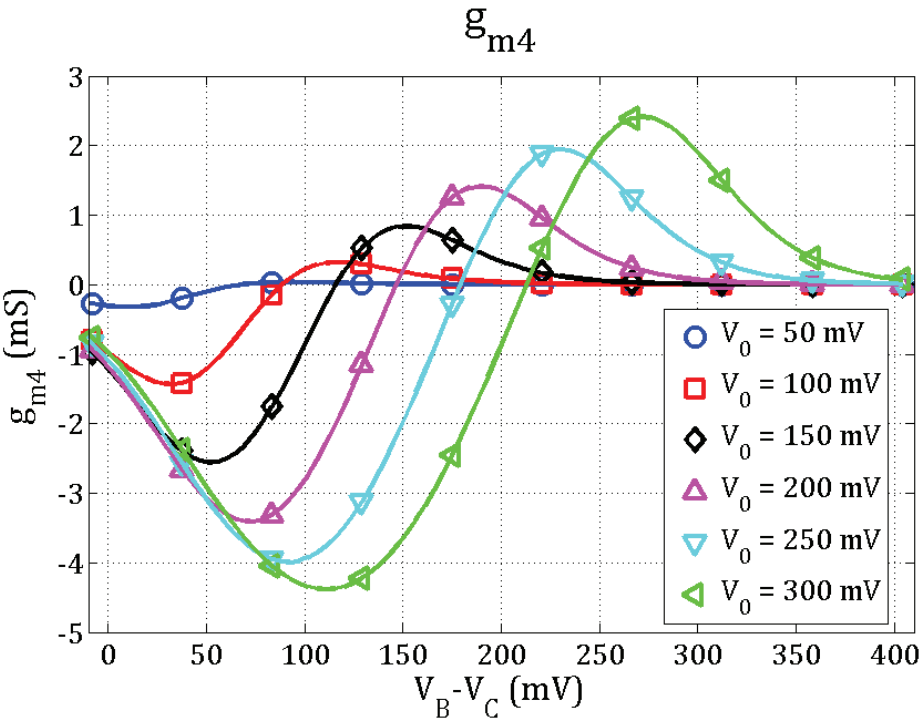

Figure 3.26 : The variation of the fourth harmonic coefficient of g_m according to $V_B - V_C$ voltage difference for different values of V_0.

$$i_{IF}(t) = g_{m0}V_{RF}\cos\omega_{RF}t + 2g_{m2}V_{RF}\cos 2\omega_0 t\cos\omega_{RF}t + 2g_{m4}V_{RF}\cos 4\omega_0 t\cos\omega_{RF}t + \cdots \tag{3.50}$$

$$i_{IF}(t) = g_{m0}V_{RF}\cos\omega_{RF}t + g_{m2}V_{RF}\cos\left(\underbrace{2\omega_0 - \omega_{RF}}_{\omega_{IF}}\right)t + g_{m2}V_{RF}\cos(2\omega_0 + \cos\omega_{RF})t + \cdots \tag{3.51}$$

$$i_{IF}(t) = g_{m0}V_{RF}\cos\omega_{RF}t + g_{m2}V_{RF}\cos\omega_{IF}t + g_{m2}V_{RF}\cos(2\omega_0 + \cos\omega_{RF})t + \cdots \tag{3.52}$$

As shown in the circuit schematic of the proposed mixer given in Figure 3.3, the primary differential pair of the mixer is loaded with Z_L load impedance. The resultant IF current is converted into the output IF voltage $v_{IF}(t)$ on the load impedance Z_L of the primary differential pair. The IF voltage $v_{IF}(t)$ is defined in (3.6). Because of the low pass characteristic of the load impedance Z_L, all the higher frequency terms of the $v_{IF}(t)$ is filtered out and only the IF term at the baseband exists. At the baseband frequency, the load impedance Z_L can be simplified into only the real resistive part of it which is the value of R1 and R2 resistors in the circuit.

$$v_{IF}(t) = i_{IF}(t) R_L \tag{3.53}$$

Here, R_L is the value of the R1 and R2 resistors at the load impedance Z_L. Since the higher frequency terms of the $i_{IF}(t)$ is filtered out at the output impedance Z_L, only the baseband term in (3.52) is substituted with $i_{IF}(t)$ in (3.53).

$$v_{IF}(t) = (g_{m2} V_{RF} \cos \omega_{IF} t) R_L \tag{3.54}$$

The definition of the IF voltage, v_{IF}, is given in (3.6). When (3.6) is used in (3.54), the equality in (3.55) is obtained. Consequently, the equality yields to the conversion voltage gain A_{VC} of the mixer as in (3.56).

$$V_{IF} \cos \omega_{IF} t = (g_{m2} V_{RF} \cos \omega_{IF} t) R_L \tag{3.55}$$

$$A_{VC} = \frac{V_{IF}}{V_{RF}} = g_{m2} R_L \tag{3.56}$$

It is clearly seen that the gain is totally determined by the second harmonic coefficient g_{m2} of the Fourier expansion (3.45) which can be obtained by the solution of the Fourier coefficient integral given in (3.47) for $n = 2$. The Fourier coefficient integral to be solved for the special case $n = 2$ is shown in (3.57).

$$g_{m2} = \frac{I_T}{4\pi V_T} \int_{-\pi}^{\pi} \frac{\cos 2\theta}{1 + \frac{A}{2} \operatorname{sech}\left(\frac{V_0}{V_T} \cos \theta\right)} \mathrm{d}\theta \tag{3.57}$$

The equation for g_{m2}, due to the definition of A given in (3.22), depends on the voltage difference $V_B - V_C$ and the magnitude of LO signal V_0. The voltage difference $V_B - V_C$ can be adjusted in such a way that the conversion voltage gain is maximized for a specific value of V_0. Therefore, in the expression of g_{m2}, $V_B - V_C$ may be viewed as a variable x and g_{m2} can be examined as a parametric expression in terms of variable x and parameter V_0 as in (3.58).

$$g_{m2} = g_{m2}(x, V_0). \tag{3.58}$$

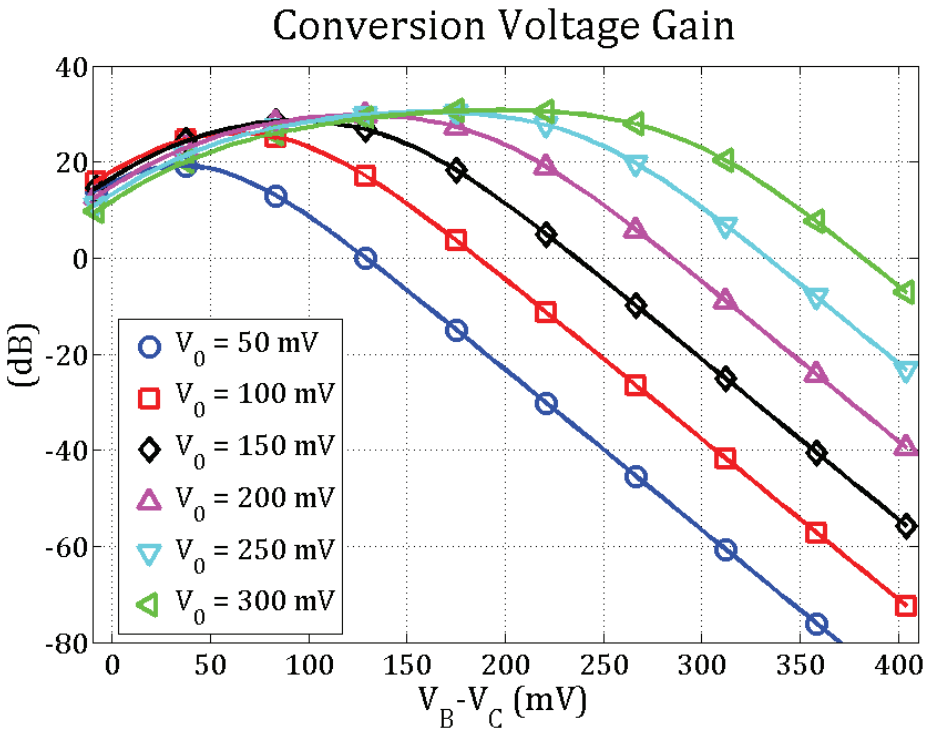

Figure 3.27 : Conversion voltage gain according to $V_B - V_C$ voltage difference for different values of V_0.

The graph of the parametric expression of g_{m2} is shown in Figure 3.25. According to the graph, the value of g_{m2} can be maximized by increasing the V_0 and finding the appropriate $V_B - V_C$ voltage difference. However, when selecting the voltage difference $V_B - V_C$, the biasing conditions for the proper functionality of the circuit should also be satisfied.

Besides the dependence of the second harmonic coefficient g_{m2} on $V_B - V_C$ and V_0, the linearity of the time varying transconductance $gm(t)$ is also strictly determined by the values of $V_B - V_C$ and V_0. Figure 3.26 shows the value of the forth harmonic coefficient g_{m4} which is the largest coefficient after g_{m2}. It is observed that at a specific biasing point for both $V_B - V_C$ and V_0, g_{m4} passes from zero, where at the same biasing point g_{m2} is almost at its maximum.

By using the obtained g_{m2} values in the conversion voltage gain expression given in (3.56), the graph of conversion voltage gain variation upon the same biasing range for $V_B - V_C$ and same values of V_0 can be plotted as in Figure 3.27. Here, the value of R_L is selected to be 3.5 kΩ depending on the biasing conditions on the actual circuit.

When the biasing conditions used in the circuit simulations, which are V_0=110 mV and $V_B - V_C$=90 mV, are also used in the circuit analysis, a conversion voltage gain of 21 dB is obtained.

3.3 IF Amplifier

A fully differential IF amplifier topology is selected to be realized as the back-end of the proposed receiver topology. The details of the FI amplifier circuit is explained in this section. A simple amplifier structure is considered for the integration with the overall topology.

3.3.1 IF Amplifier Topology

IF amplifier topology selected to be used as the back-end of the Zero-IF receiver is shown in Figure 3.28. The IF amplifier has a simple structure consisting of three identical differential pairs. All three differential pairs are biased with identical current source transistors Q9, Q10 and Q11. The first differential pair in the topology consists of transistors Q1 and Q2. The aim of this first differential pair is to supply an inverting unity gain. This is satisfied by loading this differential pair with the emitters of the transistors Q7 and Q8 which are identical to Q1 and Q2. Using identical transistors as load satisfies a negative gain almost equal to unity.

The differential input signal is applied to the first differential pair together with the second differential pair consisting of Q3 and Q4 transistors via transistors Q14 and Q15. The transistors Q14 and Q15 are connected as Darlington transistors to improve the performance of the IF amplifier by decreasing the input current. Using Q14 and Q15 decreases the current drawn from the outputs of the mixer which causes a significant loss on the resistor of the first order low pass filter placed between the mixer and the IF amplifier. Thus, using these Darlington transistors brings a great improvement such that they take place as a necessity. The third differential pair consisting of Q5 and Q6 transistors is driven by inverted signal from the outputs of the first differential pair. The outputs of the second and the third differential pairs are cross connected and loaded with R1 and R2 resistors.

The second and the third differential pairs are the actual gain stages of the IF amplifier. Input signal itself is applied to the second differential pair directly while the inverted

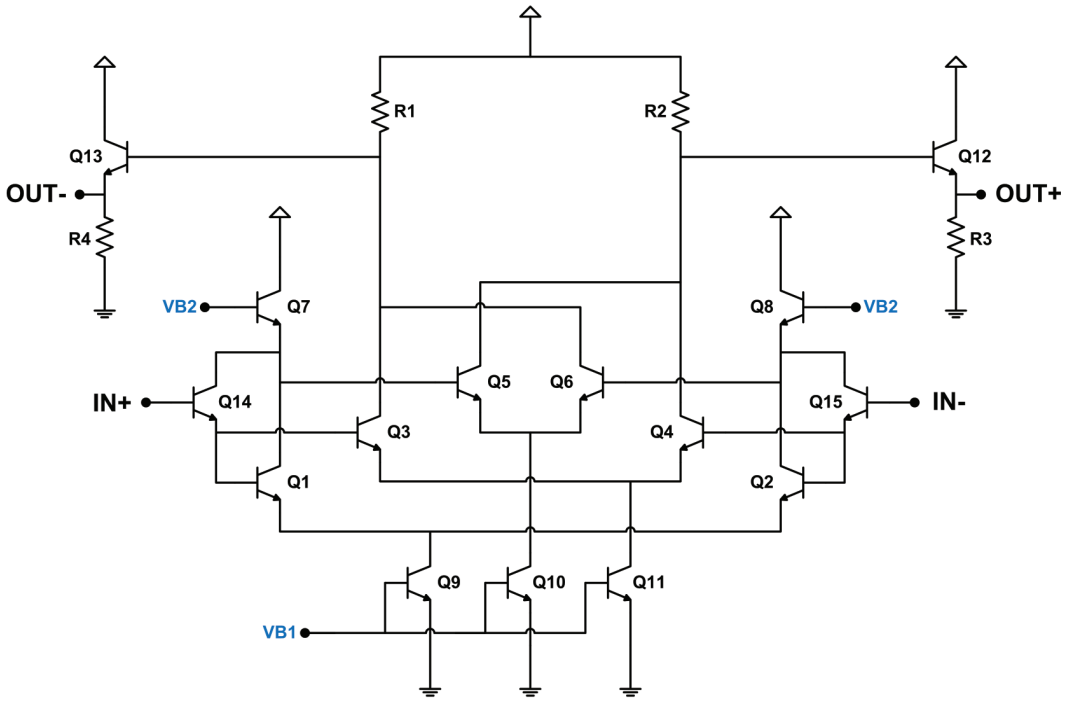

Figure 3.28 : IF amplifier circuit schematic.

input signal, which is the output of the first differential pair, is applied to the third differential pair. By this way, it is aimed to convert the differential inputs to a single ended output by subtracting two terminals from each other. Although a single ended output can be obtained form any side of these differential pairs, the same emitter follower stages are connected to the each sides to keep them as symmetrical as possible. Thus, the IF amplifier has differential outputs both of which can be used to sustain a higher gain and dynamic range. Nevertheless, any one of the outputs can be used alone as a single ended output.

Due to its single gain stage structure, the IF amplifier circuit originally have wide bandwidth. It is possible to limit the bandwidth of the IF amplifier to a desired value with a small capacitor by taking advantage of the miller effect. Small capacitors placed between outputs and the inputs with opposite polarities should satisfy a significant decrease in the bandwidth. Since the outputs of the Zero-IF receivers are the baseband signals generally with very low bandwidths, this property may be useful to satisfy such a low cutoff frequency. However, in the designed topology, the bandwidth of the IF amplifier is not limited and the filtering of the IF signal is left to the load impedance of the mixer and the first order passive filter used between the mixer and the IF amplifier.

4. SIMULATION RESULTS

The schematics of circuit blocks of the proposed Zero-IF receiver topology were built and simulated within a variety of configurations. For deeper investigation, they were tested under different conditions. The circuit schematics for the proposed receiver topology components; LNA, second harmonic mixer and IF amplifier are given in Figure 3.1, Figure 3.3 and Figure 3.28 respectively in Chapter 3. The schematics and corresponding layouts of the circuits which are shown in Chapter 5 were drawn in various design environments. Chapter 5 describes the prepared layouts for separate testing structures for the submodules of the receiver.

Most of the effort was spent on Cadence design environment to develop the proper layouts and detailed parasitic extracted netlists were obtained from these layouts to be used in the simulations. These post-layout netlists include all the parasitics related to the layouts, thus the simulations performed are supposed to give realistic results. Besides developing the layouts of the circuits in Cadence design environment, AWR Analog Office software tool was also used to benefit from its RF simulation capabilities and example testbenches. For the simulations performed, obtained post-layout parasitic netlists were connected to the suitable testbenches. Both the stand alone simulations of each block and the simulations performed on the combined schematics are included and investigated in this chapter.

The simulation results of the blocks of receiver are given and explained. The simulations are performed on the parasitic netlists of the circuits along with much of the expected external parasitics. These additional external parasitics mostly include the parasitics from the biasing of the circuit, namely the source and the ground parasitics. Since the circuits are designed to be integrated on a single chip, the bonding wire parasitics are also added to the external connections. With the added expected external parasitics, it is aimed to approach to more realistic simulation results that match the measurements.

4.1 Simulation Results of the LNA

As a front end to the Zero-IF receiver, a single input to differential outputs LNA topology is designed. The circuit schematic of the LNA is shown in Figure 3.1. The topology is explained in details in Section 3.1.1. The LNA topology is designed to operate within the target RF frequency range of 2-10 GHz. Operating within such a wide range of frequency makes the input matching challenging. The circuit schematic is connected to 50 Ω ports and S-Parameter simulation is performed on the circuit. The S11 parameter of the LNA given in Figure 4.1 and Figure 4.2 shows the performance of the input matching. According to the simulation result, the S11 of the LNA circuit stays below -12 dB within the whole RF range.

Regarding the gain of the LNA, S21 and S31 parameters are shown in Figure 4.3. According to the simulation results, an average gain of 22 dB is obtained from the LNA and it changes ± 1 dB within the band. The LNA topology is a single ended input to differential outputs converting topology as explained in Section 3.1.1. Due to the asymmetric parts of the topology, there exist a minor gain difference between to outputs. The difference in the gain traces of two outputs is maximum 0.5 dB as it is seen in Figure 4.3.

Regarding the linearity and the dynamic range of the LNA, a Harmonic Balance simulation is performed. In this simulation, the power of the input source is swept from -50 dBm to -10 dBm for a selected frequency of 2 GHz. The gain of the LNA and the resultant output power are given in the same graphic in Figure 4.4. It is seen from the graphic that both of the output powers increase linearly up to -28.35 dBm input power. For an input power of -28.35 dBm, the gain of the LNA decreases 1 dB due to saturation. The point is called the 1 dB compression point and the input power level at this point is input 1 dB compression point (I1dB). The I1dB value for the LNA is observed as -28.35 dBm for the LNA. The output power at this point is called output 1 dB compression point (O1dB) of which value is -7.6 dBm for the LNA.

Finally, the noise figure (NF) of the LNA circuit is shown in Figure 4.5. The noise figure of the LNA stays below 3.8 dB for the entire RF range. For the lower frequency range the noise performance of the LNA seems to be much better since the NF is much

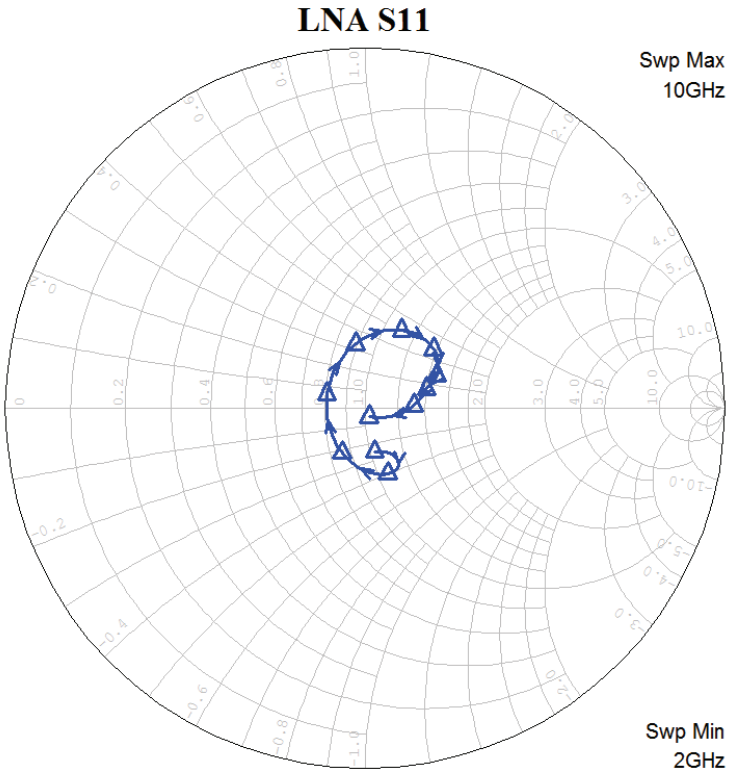

Figure 4.1 : The S11 parameter of the LNA shown on Smith Chart.

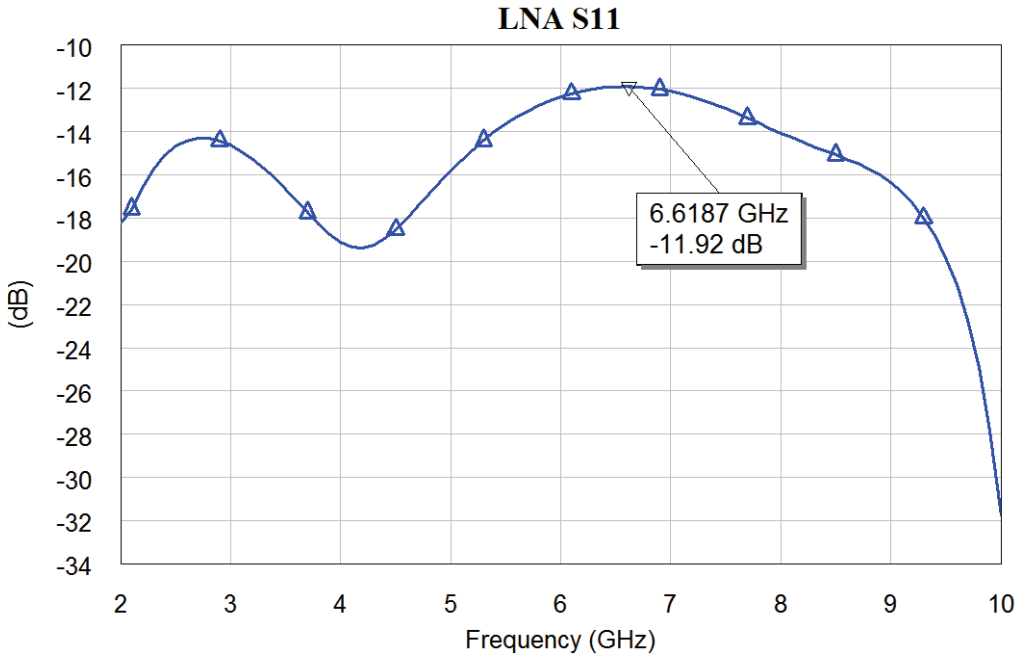

Figure 4.2 : Magnitude of the S11 parameter of the LNA shown on rectangular coordinates.

lower. However for higher frequencies, the NF of the LNA increases linearly up to 3.8 dB.

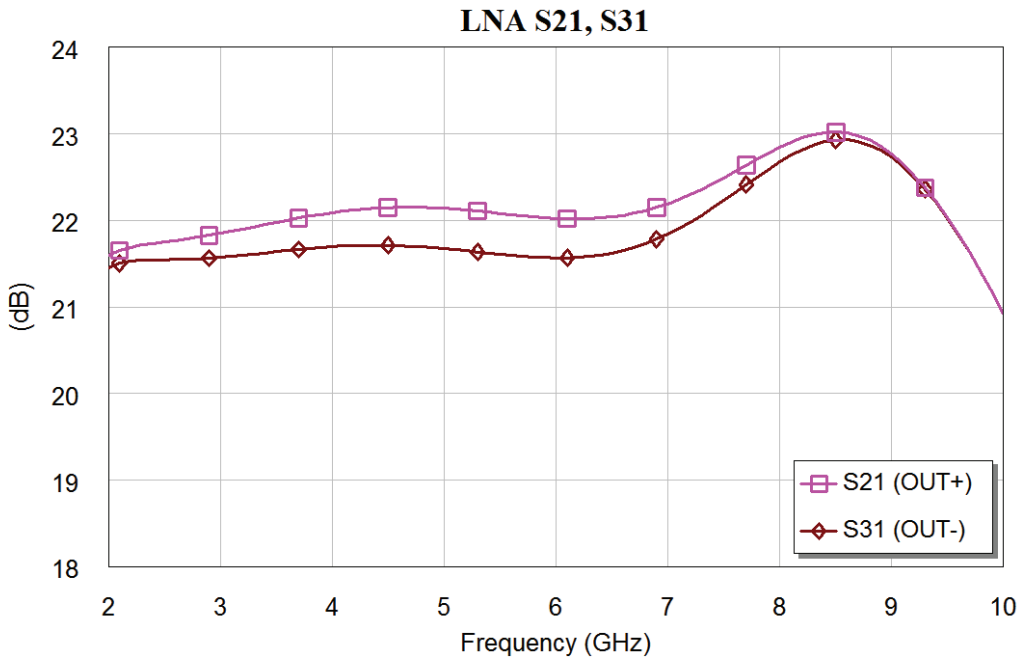

Figure 4.3 : S21 and S31 parameters of the LNA.

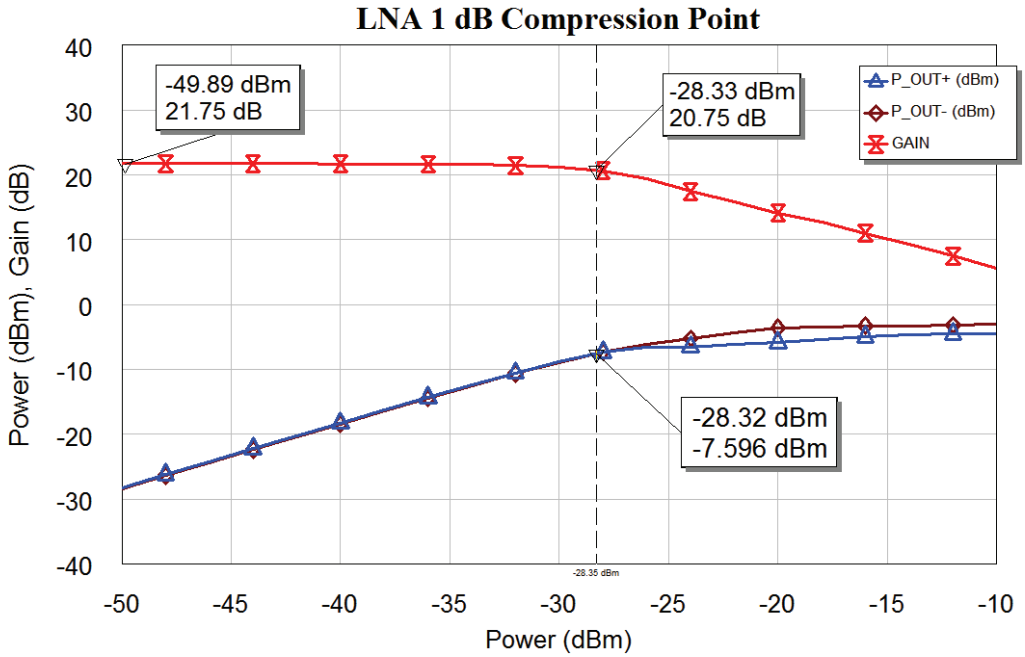

Figure 4.4 : 1 dB compression point of the LNA.

4.2 Simulation Results of the Second Harmonic Mixer

The proposed second harmonic mixer topology circuit schematic is shown in Figure 3.3. The circuit analysis of the proposed topology is performed and explained in details in Section 3.2. Since the proposed topology involves in the primary contribution

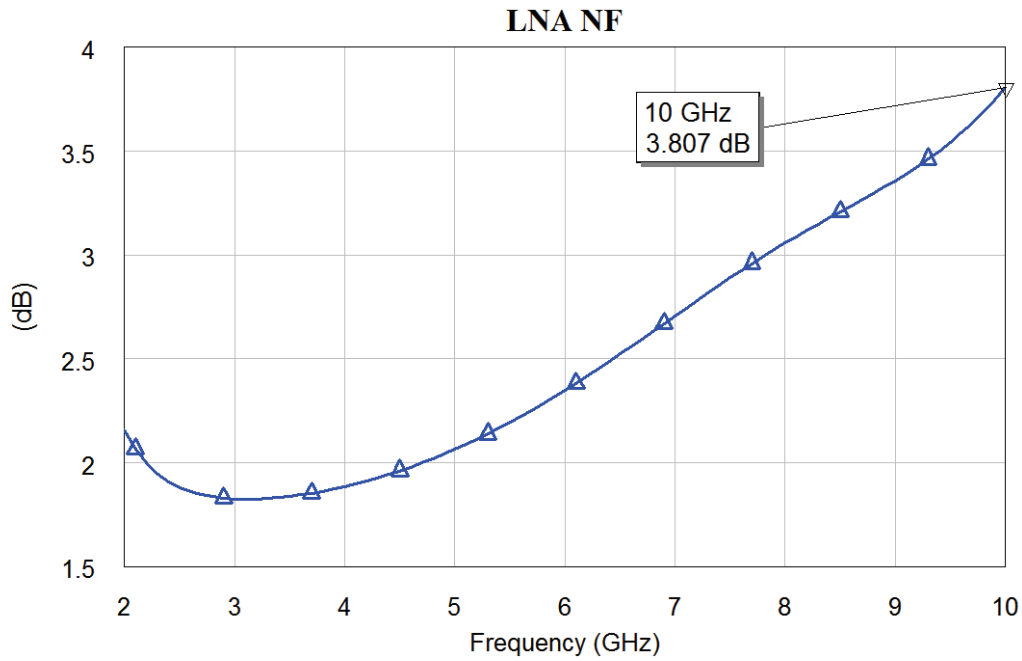

Figure 4.5 : Noise figure of the LNA.

to the overall Zero-IF receiver circuit, detailed simulations are performed on the circuit schematic shown in Figure 3.3 to support the analysis results.

In Section 3.2, the proper operating conditions and the generation of second harmonic pumping current is explained step by step by supporting equations. In following simulations, the same biasing conditions with the conditions used in the Section 3.2 are used to obtain comparable graphics.

The first simulation performed on the second harmonic mixer topology is Harmonic Balance simulation which is a nonlinear simulation technique using frequency domain calculations. The differential LO and the differential RF inputs are driven by single ended power sources over ideal baluns. The differential outputs are loaded with 50 kΩ high resistive loads since in the actual receiver circuit the mixer is connected to the inputs of the IF amplifier.

For the LO signal, a power source of -9 dBm is used and it is converted to differential signals via an ideal balun. The resultant differential LO signals are shown in Figure 4.6. In this graphic, the DC biasing level of the LO signal is neglected and only the time varying part is shown which corresponds to the $v_0(t)$ signal used in Section 3.2.2. The definition of $v_0(t)$ is given in (3.5). From Figure 4.6, it is seen that the amplitude of the time varying LO signals V_0 is obtained as 110 mV. It is the same value used in the

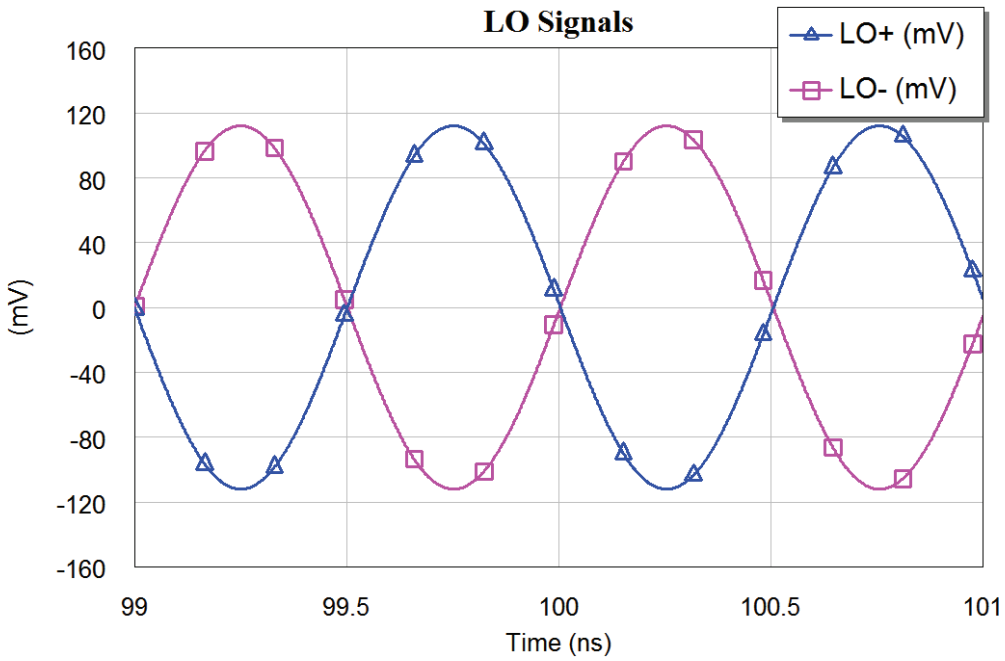

Figure 4.6 : The time varying part of the differential LO signals, $v_0(t)$.

circuit analysis in Section 3.2.2. For this simulation, the LO frequency is selected to be 0.995 GHz.

The biasing voltage difference $V_B - V_C$ which determines the value of A as explained in Section 3.2.2 is selected to be 90 mV. The definition of A is given in (3.22). For a biasing voltage difference of 90 mV, the value of A becomes 31.9. It is the value at which the pumping current i_C appears to be most linear for the biasing cases given in Section 3.2.2. Since the graphics of the analysis results given in Section 3.2.2 are obtained for $A = 31.9$, the same value is selected for the simulations. The total biasing current I_T is selected to be 1.8 mA which is also same with the value used in analysis in Section 3.2.2.

In Figure 4.7, the i_C^+ and i_C^- currents are shown separately. It is seen that due to the proper biasing, the transistors producing the i_C^+ and i_C^- currents turns on and off sequentially for every half period of the LO signal. Due to the turning on and off operation of the individual transistors producing the i_C^+ and i_C^- currents, the i_C^+ and i_C^- currents both contain the harmonic components of the LO signal. When combined together, the i_C^+ and i_C^- currents generate the total pumping current i_C of which the frequency is mainly the second harmonic of the LO signal. The total pumping current i_C and the residue current i_R are shown together in Figure 4.8. The graphics shown

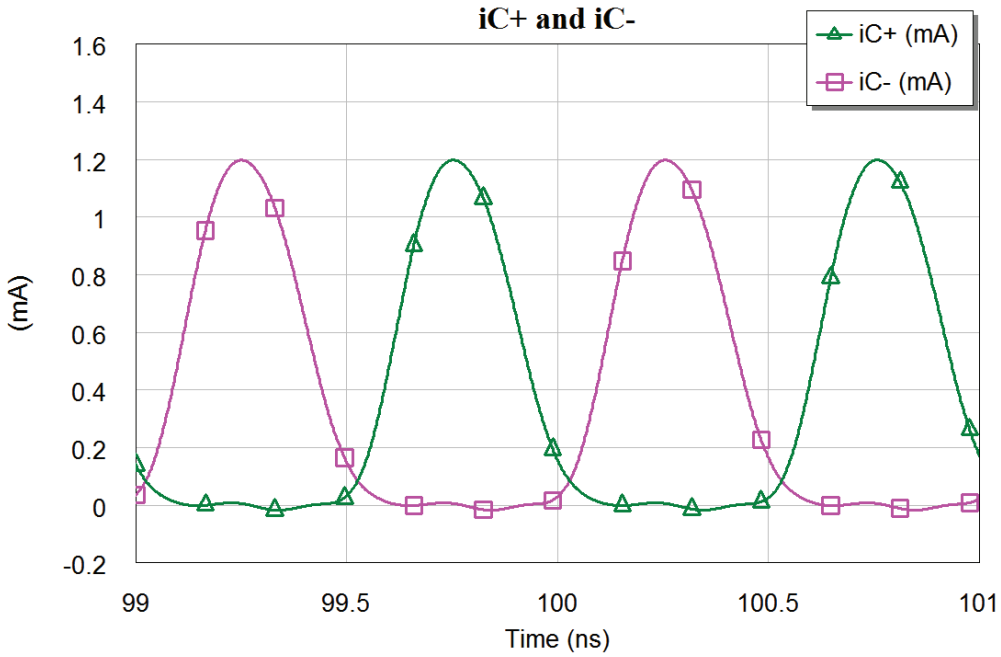

Figure 4.7 : i_C^+ and i_C^- currents.

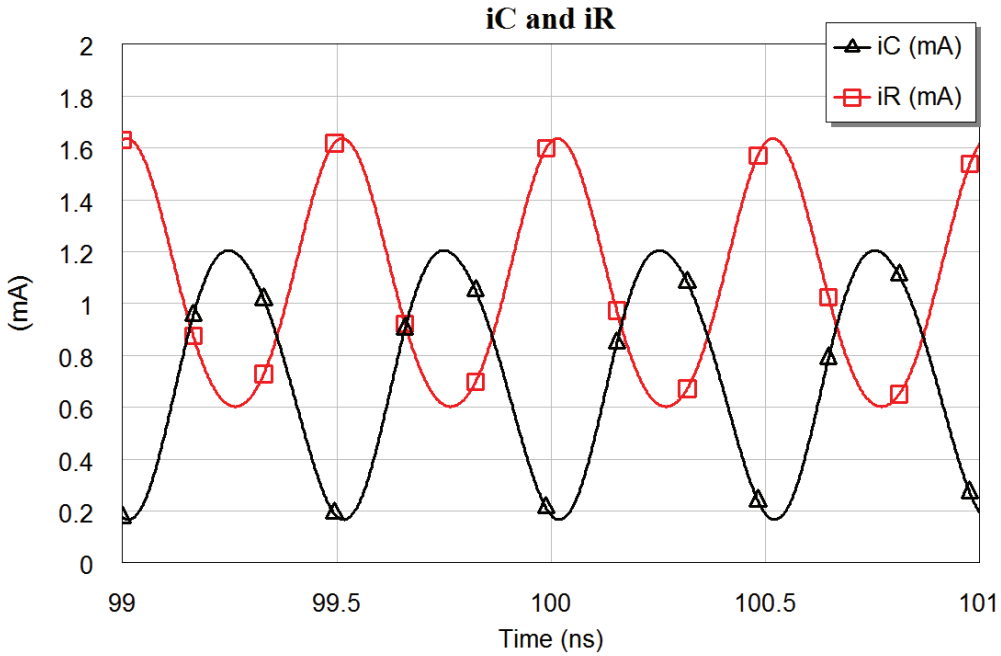

Figure 4.8 : The pumping current i_C and the residue current i_R.

in both Figure 4.7 and Figure 4.8 are obtained for the differential LO signals given in Figure 4.6.

In Section 3.2.2, when the circuit analysis of the proposed second harmonic mixer is being explaned, the total biasing current I_T is assumed to be constant since it is supplied by a transistor biased with a constant voltage. This transistor is assumed

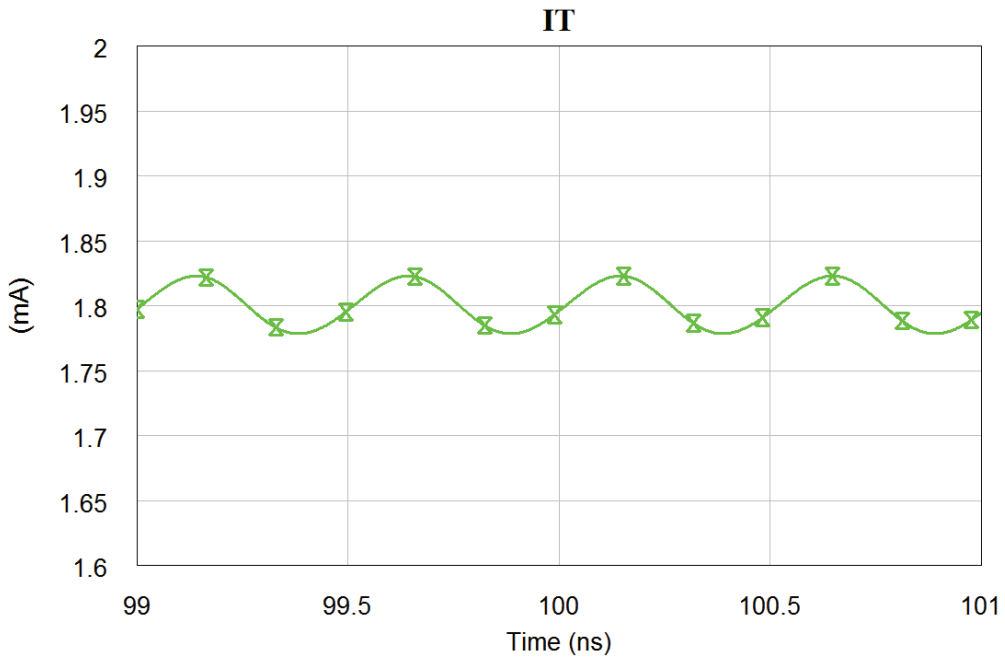

Figure 4.9 : The change of the total biasing current I_T .

as ideal and it is assumed that its collector current is not effected from the voltage change on its collector like an ideal current source. However, in realization, since the output impedance of the transistor is not infinite like an ideal current source, its collector current shows some minor dependence on the voltage change on its collector. Although this minor dependency can be neglected safely for the sake of simplicity of the analysis, it can be improved by using some more complex circuitry as the source of total biasing current I_T. The change of the I_T current effected from the voltage change on the collector of the transistor is shown in Figure 4.9. As it is seen from the graphic, the I_T contains a minor amount of second harmonic component of the LO signal.

The resultant i_C curves of an parametric simulation is given in Figure 4.10. Here, the value of A is changed as a parameter by arranging the biasing voltage difference $V_B - V_C$. This is achieved by keeping the DC biasing level of LO signal V_C constant and simply changing the biasing voltage V_B. The voltage difference is changed stepwise from 30 mV to 180 mV with 30 mV steps in accordance with the values which are given in the analysis in Section 3.2.2. The effect of A value on the resulting pumping current i_C is seen in Figure 4.10. It effects both the amplitude of the i_C variation and the linearity of it.

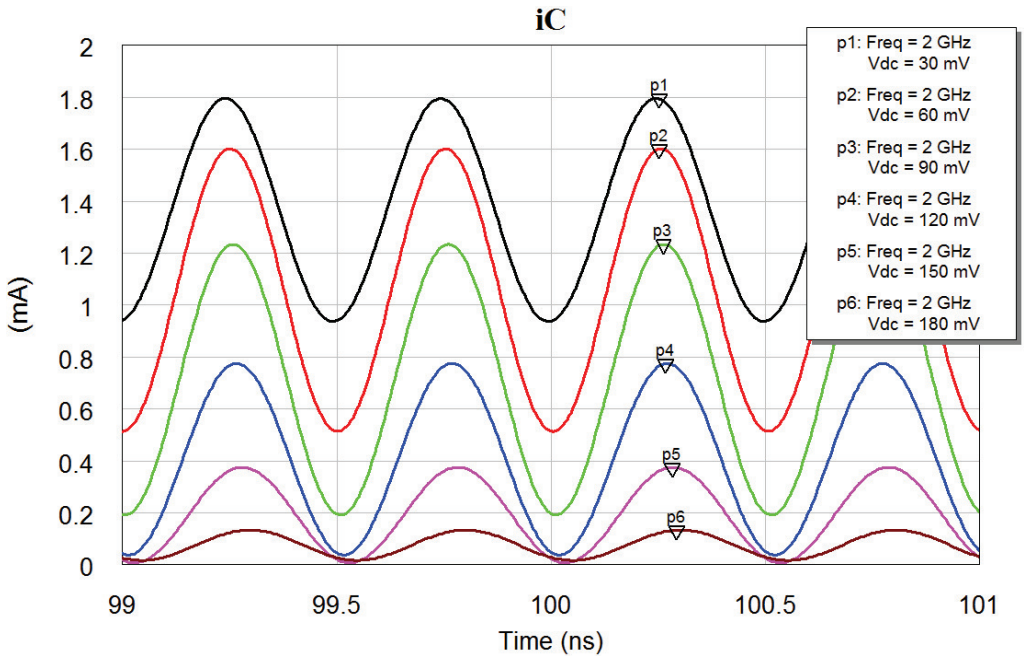

Figure 4.10 : The pumping current i_C for different values of biasing voltage difference $V_B - V_C$.

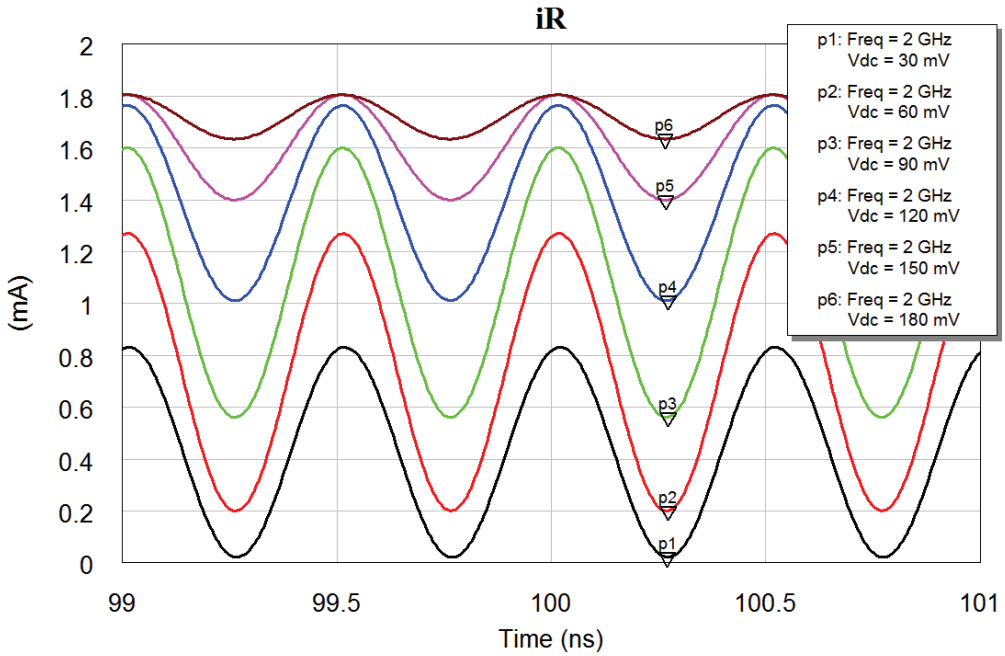

Figure 4.11 : The residue current i_R for different values of biasing voltage difference $V_B - V_C$.

Similarly with the same biasing conditions and parameter values, the change of the residue current i_R is obtained as in Figure 4.11. It is observed from both Figure 4.10 and Figure 4.11 that the effects of the value of A on i_C and i_R are in total correlation.

Another graphic given in Section 3.2.2 belongs to the transfer function TF_C defined in (3.26), to explain the conversion from LO signal $v_0(t)$ to pumping current i_C. The transfer function obtained from the analysis results is shown in Figure 3.4 and its change according to the value of A is shown in Figure 3.6 in Section 3.2.2. To verify the performed analysis, a DC simulation is performed on the circuit schematic of the second harmonic mixer. To obtain the similar graphics for convenient comparison, the DC voltage sweep form -400 mV to 400 mV is applied between the differential LO ports of the mixer by keeping the appropriate DC biasing level V_C at both LO ports. The resultant graphic shown in Figure 4.12 shows the transfer function TF_C. Again by changing the voltage difference $V_B - V_C$, thus the value of A, stepwise through the same values, the graphic in Figure 4.13 is obtained.

For the residue current i_R, another transfer function TF_R is defined in (3.35) in Section 3.2.2. It emphasizes the similarities in the generation of i_C and i_R currents. From the same DC simulation, the graphic for the transfer function TF_R is obtained as in Figure 4.14. The effect of the value of A shown in Figure 4.15. The corresponding graphics obtained form the analysis results in Section 3.2.2 are Figure 3.11 and Figure 3.12 respectively.

When the proposed second harmonic mixer is biased at the optimum operating conditions, it is expected to have a linear pumping current i_C of which dominant frequency component is $2f_{LO}$. All the odd harmonics of f_{LO} frequency should be suppressed in i_C as explained in analysis given in Section 3.2.2. To reveal all the frequency components of the pumping current i_C, a Harmonic Balance simulation is performed on the mixer schematic. The frequency spectrum of the i_C is obtained as shown in Figure 4.16. As it is seen from Figure 4.16, the total pumping current i_C is composed of only the even harmonics of the LO frequency f_{LO}. This result shows total agreement with the analysis results given in Section 3.2.2.

According to the analysis results given inSection 3.2.2, the residue current i_R contains the exact same frequency components with opposite signs with the pumping current i_C. In Figure 4.17, it is seen that the i_R is also composed of the even harmonics of the LO frequency f_{LO} with the same magnitudes with i_C. As expected, only the magnitude of the DC term of the i_R current differs from i_C.

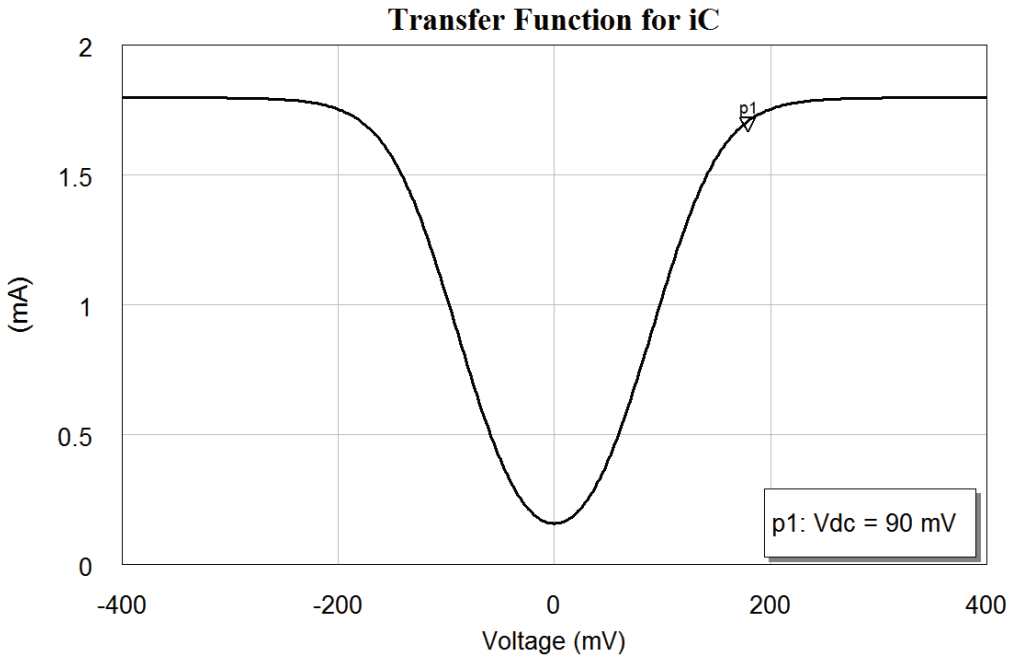

Figure 4.12 : Transfer function TF_C under proper biasing conditions.

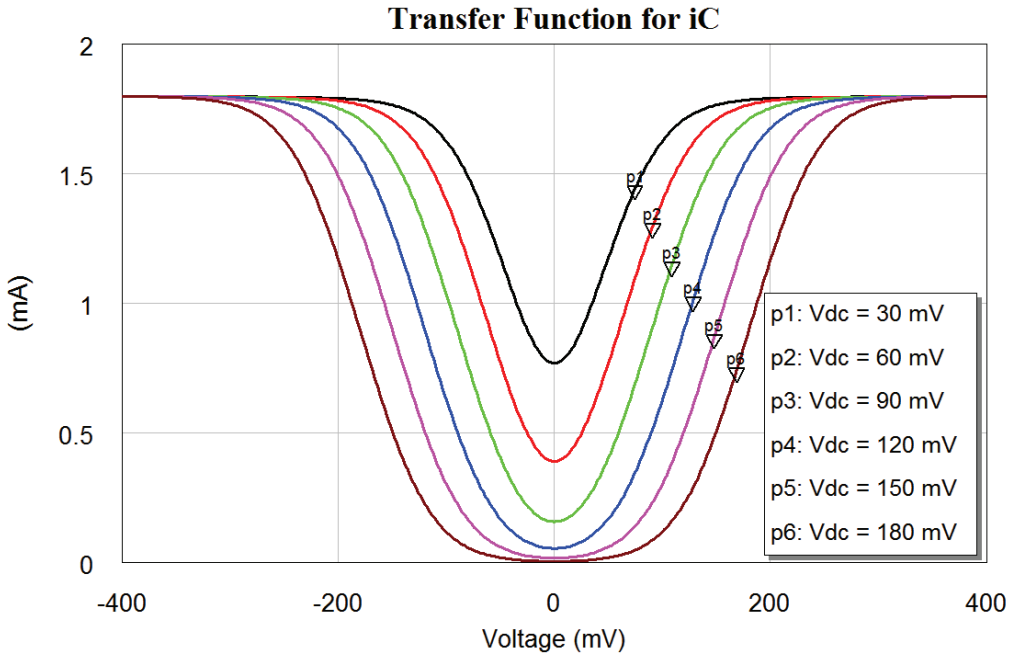

Figure 4.13 : Transfer function TF_C for different biasing voltage differences $V_B - V_C$.

In the simulation to investigate the conversion voltage gain of the proposed second harmonic mixer, the RF signal frequency f_{RF} is swept from 2 GHz to 10 GHz since it is target RF frequency range of the designed overall Zero-IF receiver topology. The frequency of the resultant IF signal f_{IF} is selected to be 10 MHz. The LO frequency is also swept accordingly to obtain an IF signal at 10 MHz at the outputs of the mixer.

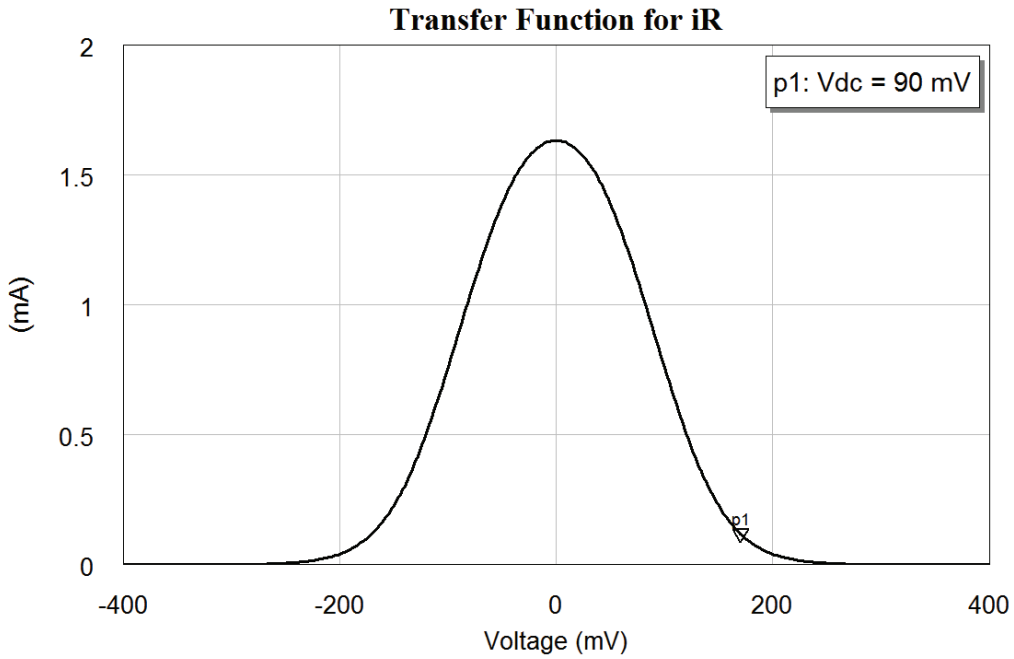

Figure 4.14 : Transfer function TF_R under proper biasing conditions.

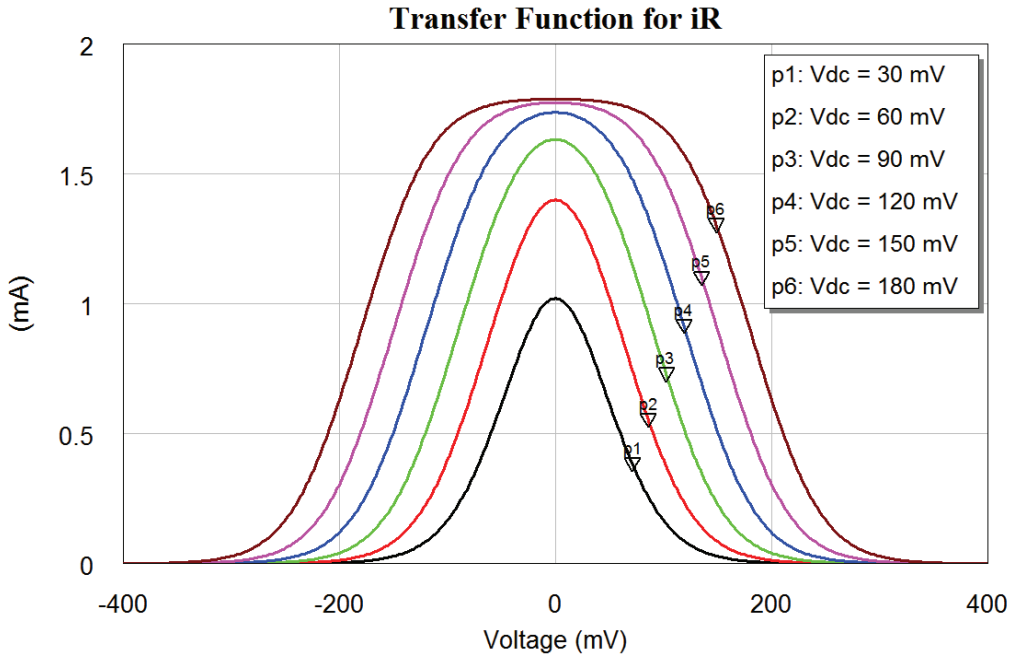

Figure 4.15 : Transfer function TF_R for different biasing voltage differences $V_B - V_C$.

$$f_{LO} = \frac{(f_{RF} - f_{IF})}{2} \tag{4.1}$$

The frequency of the LO signal is defined as in (4.1) for the simulation, thus for all the sweep points the IF signal occurs at 10 MHz. Therefore, in the simulation, the LO frequency f_{LO} is swept form 0.995 GHz to 4.995 GHz simultaneously with RF frequency f_{RF}. Within this RF frequency range the conversion voltage gain of the

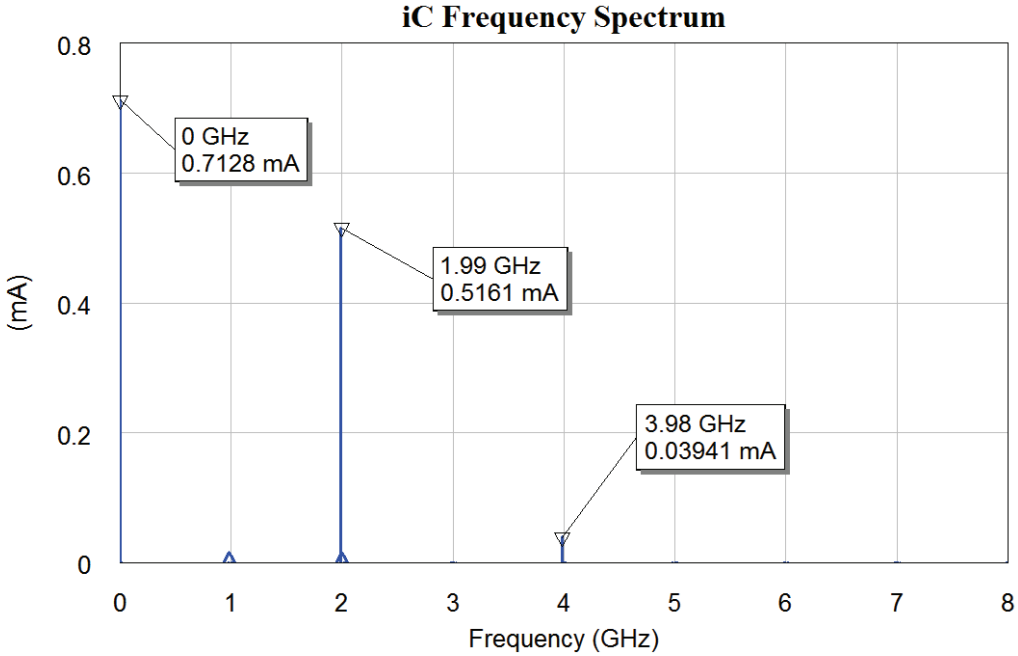

Figure 4.16 : Frequency Spectrum of the pumping current i_C under proper operating conditions.

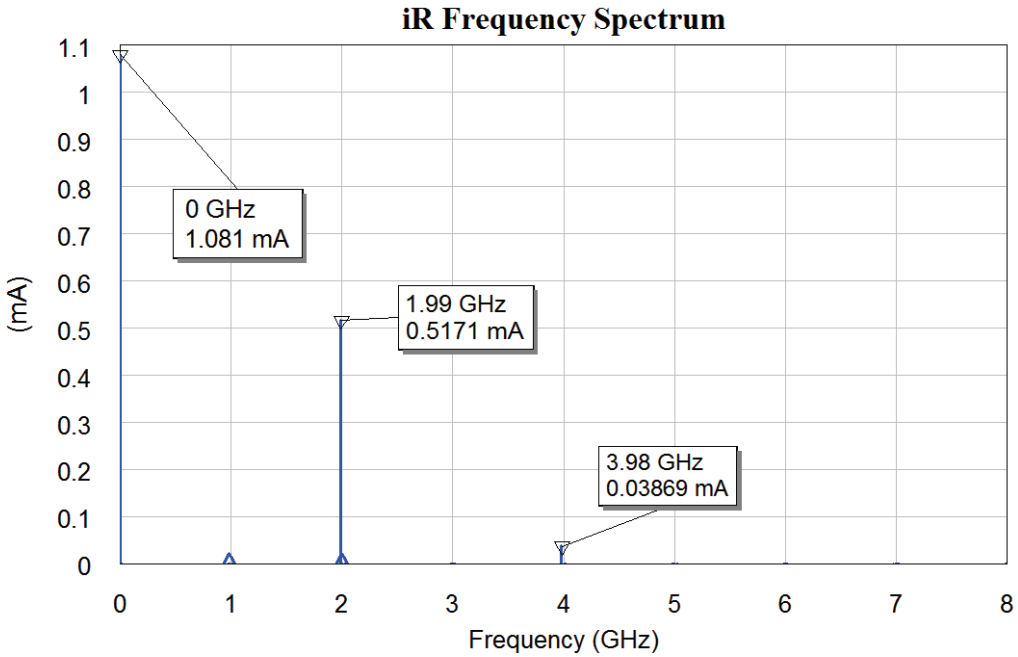

Figure 4.17 : Frequency Spectrum of the residue current i_R under proper operating conditions.

proposed second harmonic mixer is obtained as shown in Figure 4.18. According to the simulation result, the proposed mixer has a conversion voltage gain of 20 dB, it changes only 1.3 dB within the whole RF frequency range. This result shows that

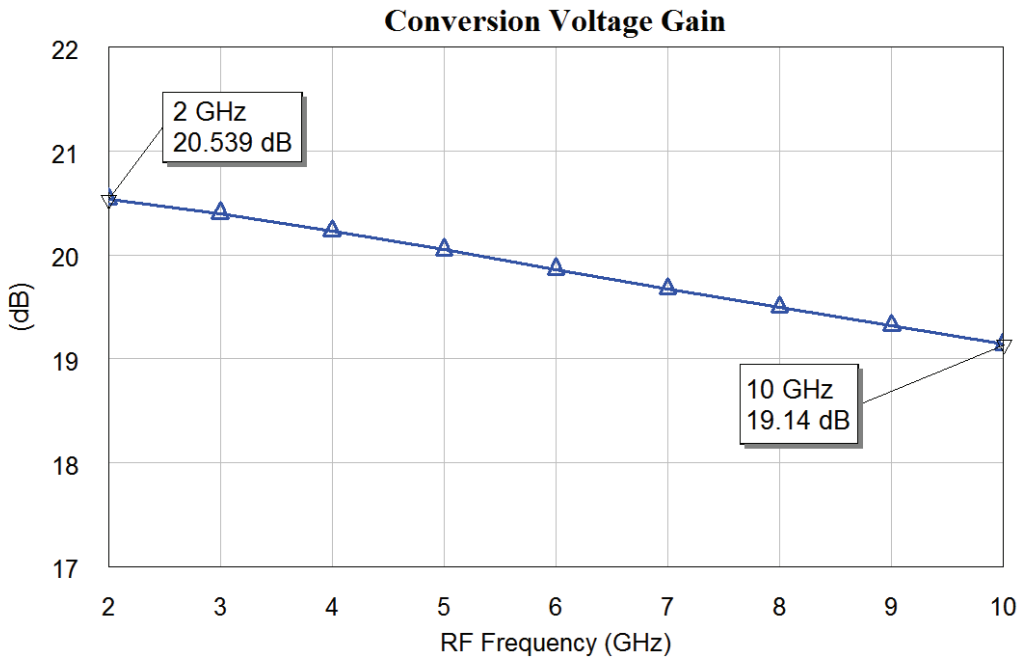

Figure 4.18 : The conversion voltage gain of the proposed mixer topology within 2-10 GHz RF frequency range.

the mixer topology is suitable for wide band operations can be used for a variety of applications.

As depicted previously, the proposed mixer topology is designed to be connected to an IF amplifier through a first order passive low pass filter. When connected with the IF amplifier according to the purpose of the topology, the overall conversion voltage gain becomes as in Figure 4.19. As seen in Figure 4.19, the conversion voltage gain is increased by 16 dB linearly for the entire RF frequency range. Figure 4.20 shows the total noise figure of mixer and IF amplifier together. It is seen that the noise figure stays below 14 dB for the entire band. The detailed simulation results regarding the IF amplifier is given in Section 4.3.

To investigate the dynamic range of the prosed mixer together with the IF amplifier following it, a Harmonic Balance simulation is performed with a swept input power source. The input power source is applied to the differential RF inputs of the mixer through an ideal balun. The differential outputs of the If amplifier is connected to 50 Ω loads and the both outputs are observed separately. The input RF power is swept from -40 dBm to -10 dBm for the selected RF frequency 2 GHz. The LO frequency f_{LO} is kept at 0.995 GHz through out the simulation to have the IF output component at 10 MHz. The power graphics of the obtained IF components at both output ports of

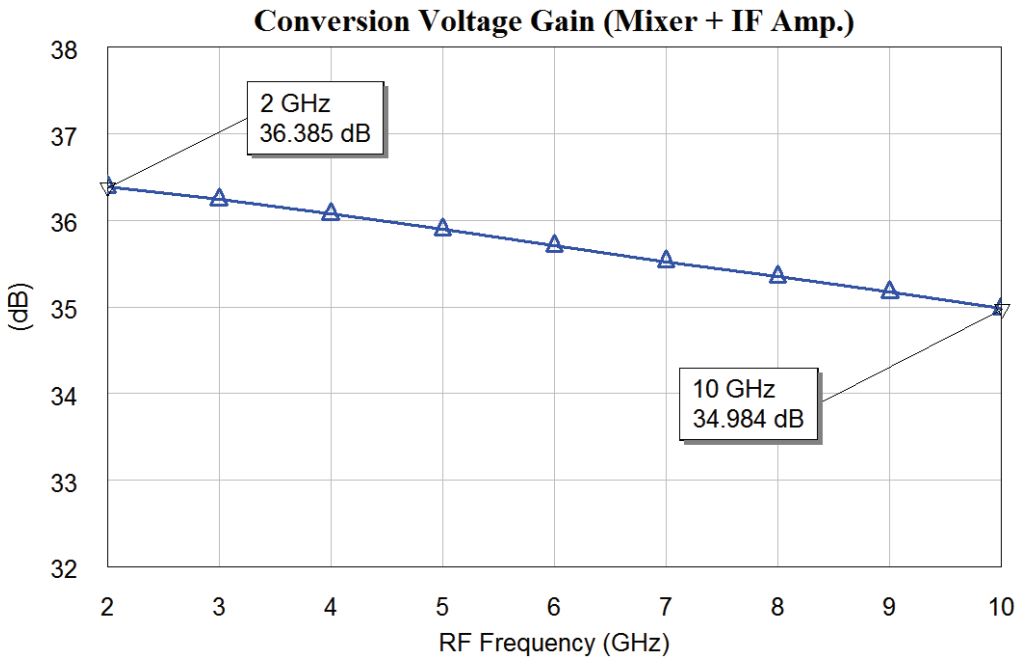

Figure 4.19 : Total conversion voltage gain within 2-10 GHz RF frequency range when the mixer and the IF amplifier is connected together.

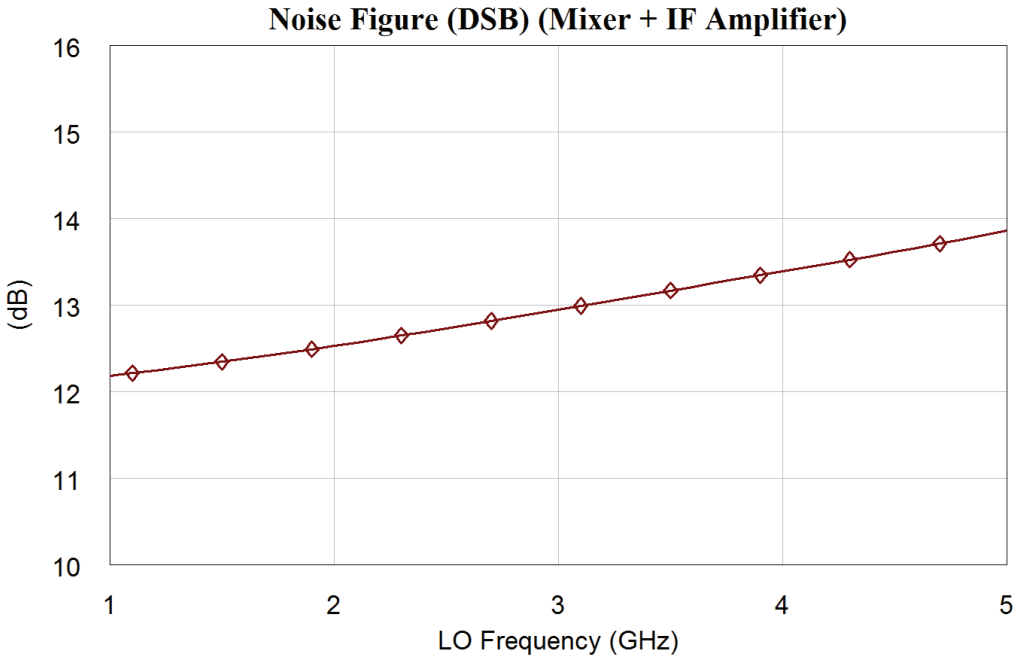

Figure 4.20 : Total noise figure within 1-5 GHz LO frequency range when the mixer and the IF amplifier is connected together.

the IF amplifier together with the conversion gain graphs are shown in Figure 4.21. As the input power is increased the both If outputs starts to saturate. The point where the gain is decreased 1 dB is called 1 dB compression point which used as a linearity metric. When the total gain is evaluated, it is found out that 1 dB compression occurs

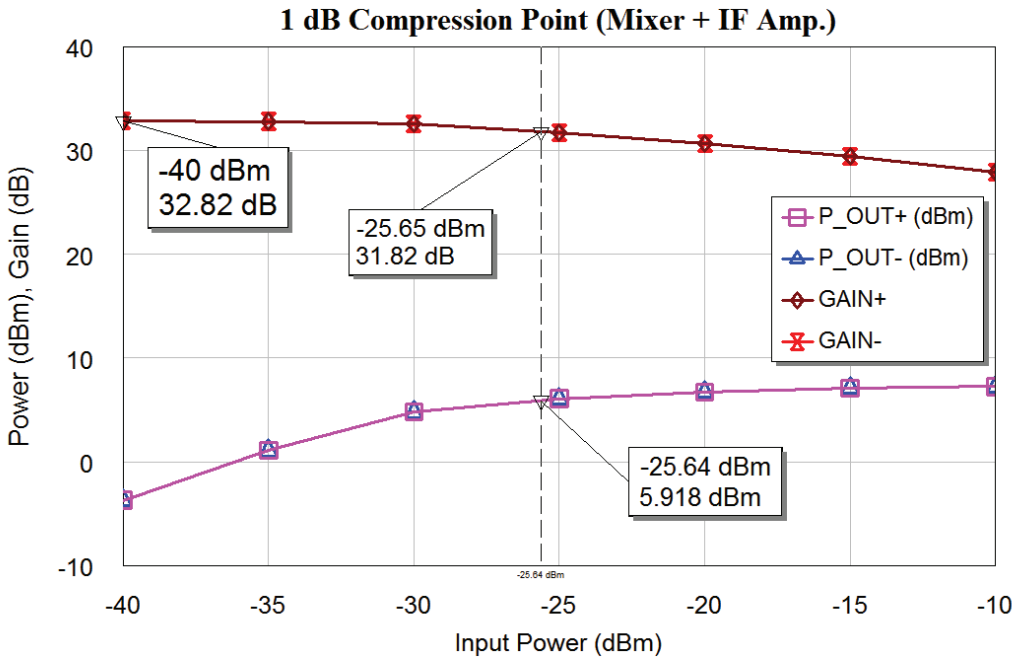

Figure 4.21 : 1 dB compression point when the mixer and the IF amplifier is connected together.

for an input power of -25.6 dBm. This value is called the input 1 dB compression point (I1dB). The output power at this point which is called the output 1 dB compression point (O1dB) is found as 5.9 dBm from the graphic.

The IF bandwidth of the combined mixer and the IF amplifier structure is exposed with an appropriate simulation. In the simulation, for a selected LO frequency f_{LO} of 1 GHz, the RF frequency f_{RF} is swept from 2.001 GHz to 3 GHz. Thus, the resultant IF signal frequency f_{IF} changes from 1 MHz to 1 GHz accordingly. The corresponding conversion voltage gain graphic is shown in Figure 4.22. The total IF filtering consists of the load impedance of the second harmonic mixer and a separate LPF placed between the mixer and the IF amplifier. Both the separate filter and the load impedance of the mixer are first order passive filters consisting of a single resistor and a capacitor. From Figure 4.22, the 3 dB cut-off frequency of the IF filtering is 10 MHz. Figure 4.22 represents the worst operating condition case since the RF signal frequency is selected to be 2 GHz thus the LO frequency is 1 GHz. This is condition at which the RF signal frequency and the LO frequency are closest to the IF bandwidth. As it is seen from Figure 4.22, the gain at 1 GHz is about -25 dB that means sufficient suppression can be satisfied even for the worst case.

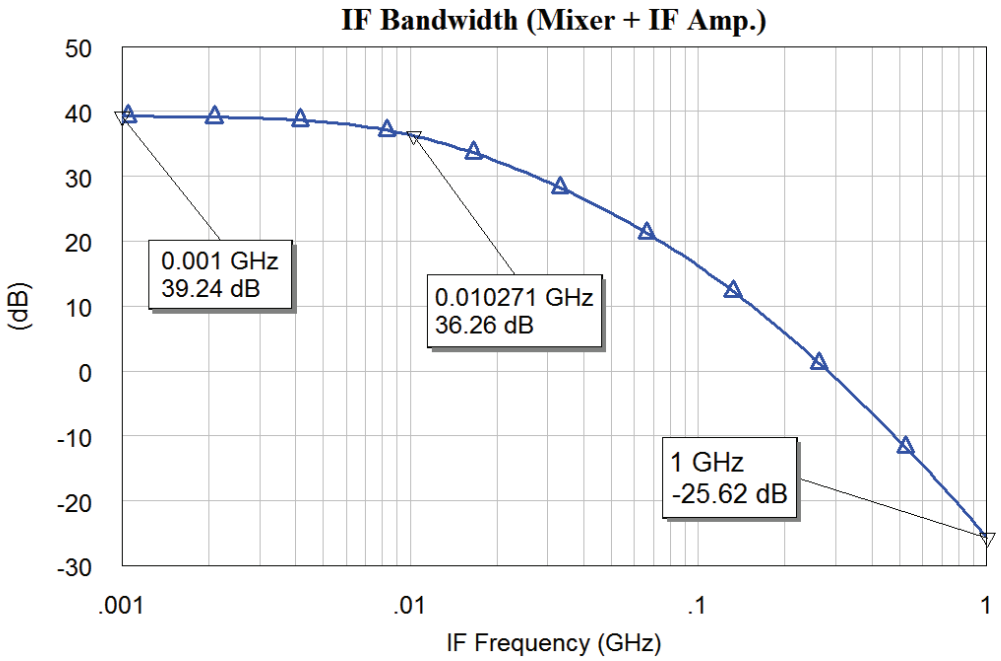

Figure 4.22 : IF bandwidth of the combined structure of the mixer and the IF amplifier.

To emphasize the conversion gain in the IF bandwidth and the out of band suppression, the frequency spectrum at both the output of the second harmonic mixer and the IF amplifier are given in Figure 4.23 and Figure 4.24 respectively. When two graphics are compared, it is noticed that the high frequency components existing at the mixer output are suppressed at the IF amplifier outputs. This elimination of the high frequency components is due to the passive LPF between the mixer and the IF amplifier. It is also observed that the fundamental mixing product $f_{RF} - f_{LO}$, which is 1.005 GHz in this example, does not occur at the mixer outputs, thus it is suppressed naturally by the second harmonic mixer.

The magnitudes of the IF component and the DC component at the outputs of both the second harmonic mixer and the IF amplifier for the whole RF signal frequency range is shown in Figure 4.25 and Figure 4.26. In the simulation, the RF signal frequency is swept from 2 GHz to 10 GHz and the LO frequency is swept simultaneously such that the IF signal frequency is kept at 10 MHz. The simulation results verify that no DC component appears at the output of the proposed mixer. The DC cancellation mechanism of the proposed second harmonic mixer topology efficiently eliminates the DC offset voltage.

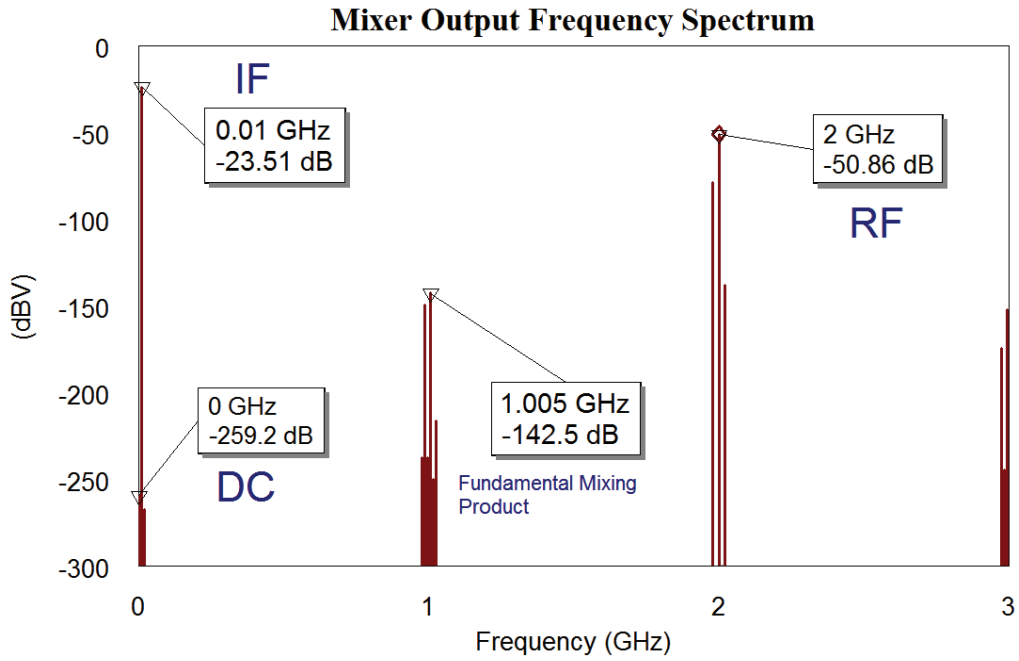

Figure 4.23 : Output frequency spectrum of the mixer.

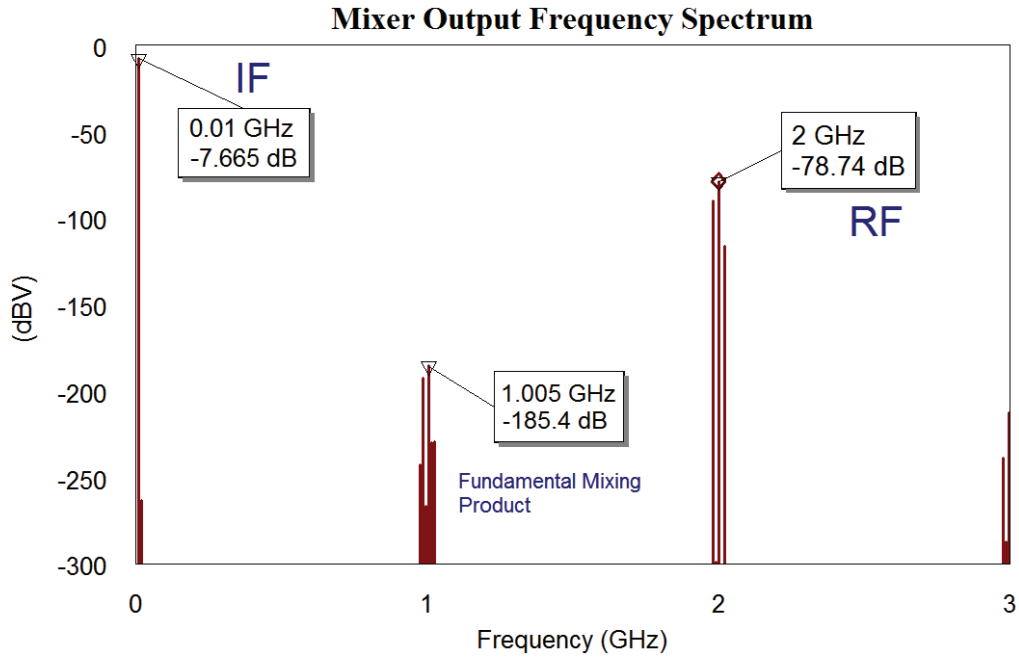

Figure 4.24 : Output frequency spectrum of the IF amplifier.

4.3 Simulation Results of the IF Amplifier

The IF amplifier circuit used at the back-end of the second harmonic receiver topology is shown in Figure 3.28. The given circuit schematic which is explained in details in Chapter 3 is constructed in the simulation environment. Several simulations are performed on the schematic to discover the performance and the limitations of the

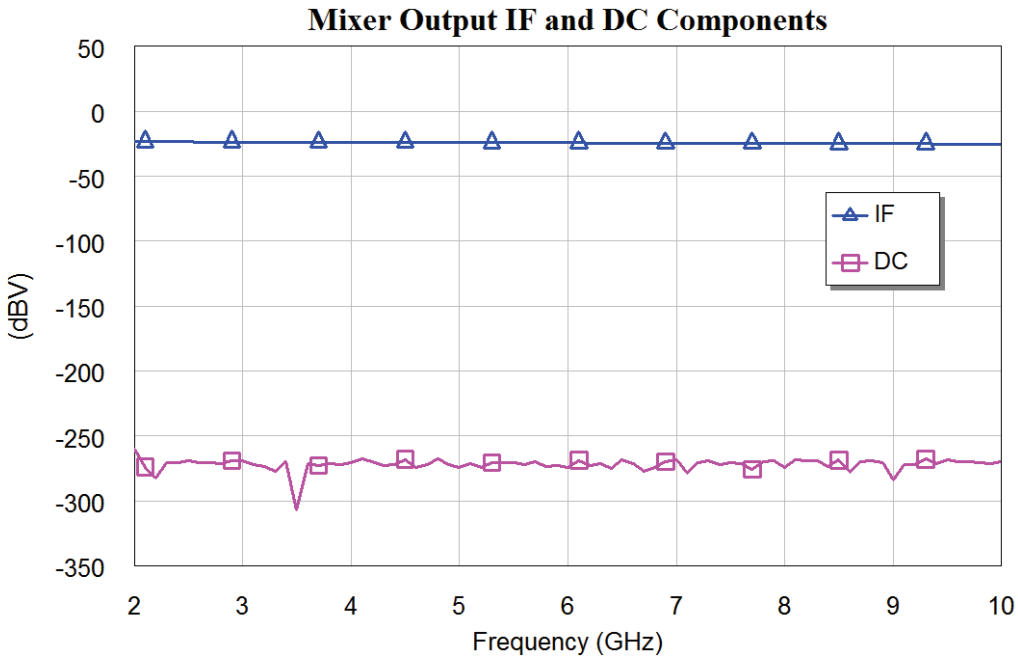

Figure 4.25 : IF and DC components at the mixer output for the whole RF frequency range.

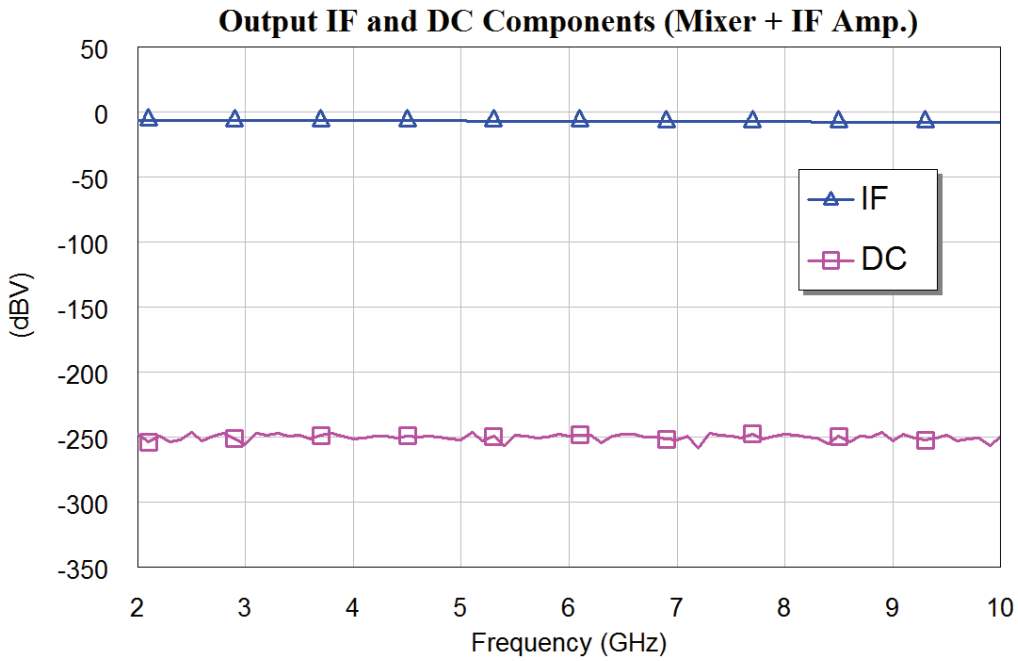

Figure 4.26 : IF and DC components at the IF amplifier output for the whole RF frequency range.

amplifier. The purpose of the amplifier is to be used at the baseband following the second harmonic mixer. Since the bandwidth of the baseband signal is chosen to be 10 MHz, the amplifier bandwidth should also satisfy just up to this frequency range. Although the IF amplifier should be designed to satisfy such a bandwidth and used also

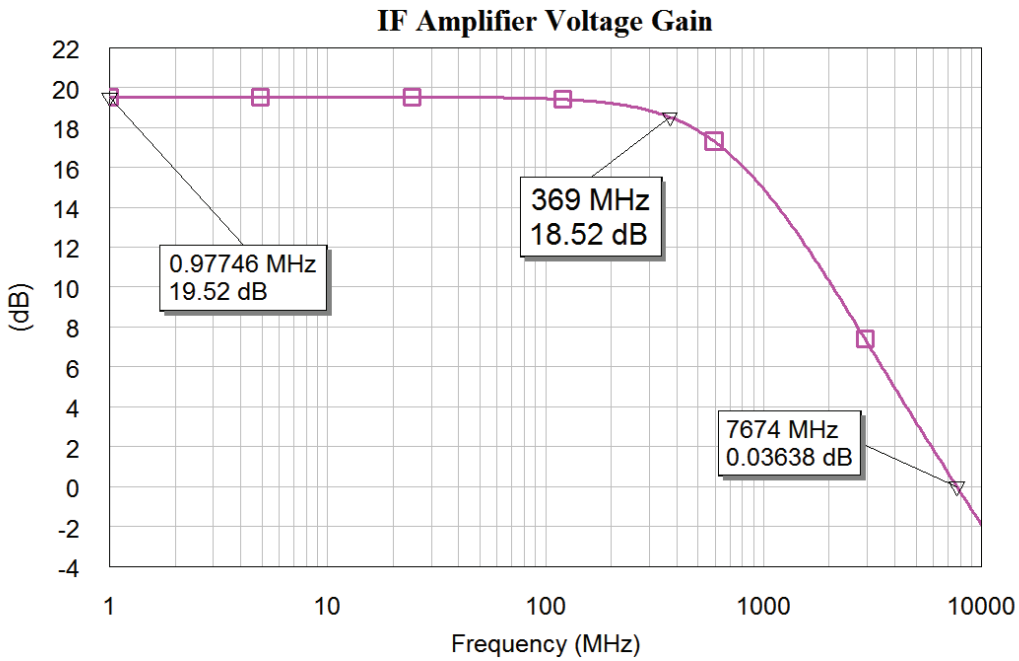

Figure 4.27 : IF amplifier voltage gain according to frequency.

as a baseband filter, for simplicity the bandwidth of the IF amplifier is not limited. The input signal of the IF amplifier is supposed to be filtered such as it contains only the baseband signal. In the overall receiver topology, the filtering of the baseband signal is achieved by the load impedance of the second harmonic mixer, which is actually a first order filter, together with another passive first order filter placed between the mixer and the IF amplifier.

The first simulation performed on the IF amplifier is the AC simulation. The differential inputs of the IF amplifier is driven by AC voltage source differentially. The AC voltage gain when the outputs are open is given in Figure 4.27. Here, the differential outputs are combined ideally. The frequency is swept from 1 KHz to 10 GHz. According to the simulation result, the voltage gain of the amplifier is 19.5 dB and the 3 dB cutoff frequency is 370 MHz. Since the amplifier consists of a single gain stage followed by emitter followers, The gain plot shows a single pole behavior. The gain bandwidth (GBW) of the amplifier is 7.67 GHz.

Upon the same frequency range, the phase shift of the If amplifier is plotted in Figure 4.28. The graph shows that the IF amplifier shows a phase shifting of less than 100 degrees. It has a phase margin of 87 degrees.

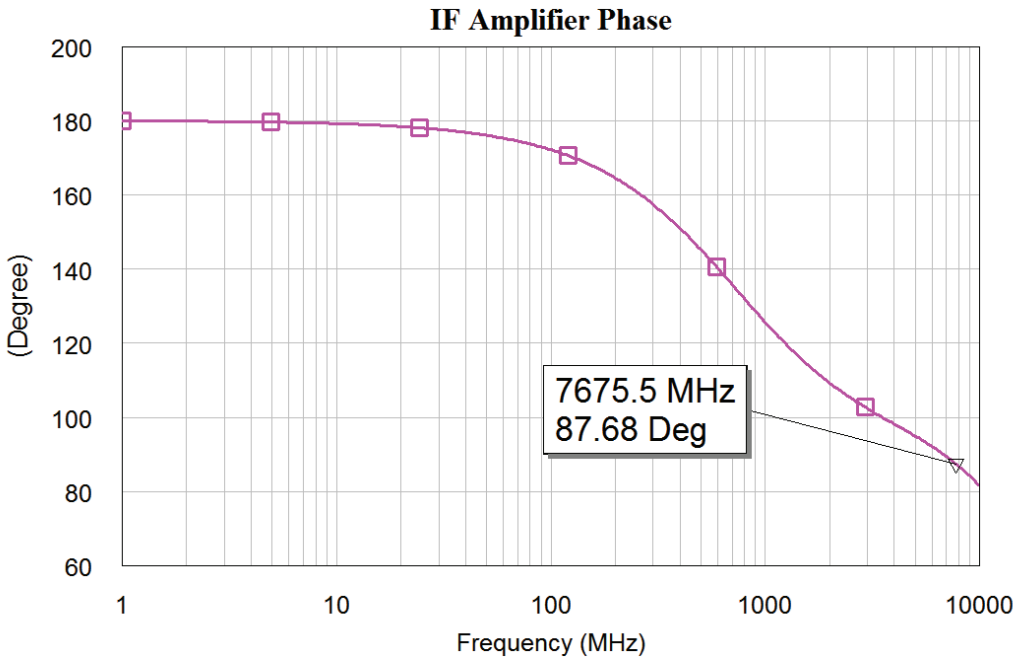

Figure 4.28 : IF amplifier phase shift according to frequency.

Another simulation performed on the IF amplifier circuit schematic is the noise figure (NF) simulation. The noise performance of IF amplifier has minor importance in the overall system noise performance. The noise figure of the IF amplifier is shown in Figure 4.29. The Flicker noise effect is seen at the low frequency range up to 1 MHz. Beyond 1 MHz the NF of the amplifier is tied up to a constant value of 12.4 dB upon the bandwidth. The IF signal bandwidth is supped to be 10 MHz thus the NF value at this frequency is marked at the graphic.

The differential inputs of the IF amplifier is combined with an ideal balun and a power source is connected to the input. The outputs of the IF amplifier are connected to 50 Ω ports to perform the Harmonic Balance simulation. The input signal power is swept from -40 dBm to 10 dBm and the output signal power is observed. The performed Harmonic Balance simulation reveals the linearity performance of the IF amplifier. In Figure 4.30, the power gain at the fundamental frequency is shown. The gain curves for the both outputs of the IF amplifier are shown separately. According to the results, the power gain of the IF amplifier is 17.64 dB. In Figure 4.31, the power gain is shown along with the output power. In both Figure 4.30 and Figure 4.31, the 1 dB compression point is marked. The output 1 dB compression point (O1dB) and the input 1 dB compression point (I1dB) are two related performance metrics for linearity. The I1dB shows the input power level and the O1dB shows the output power level at

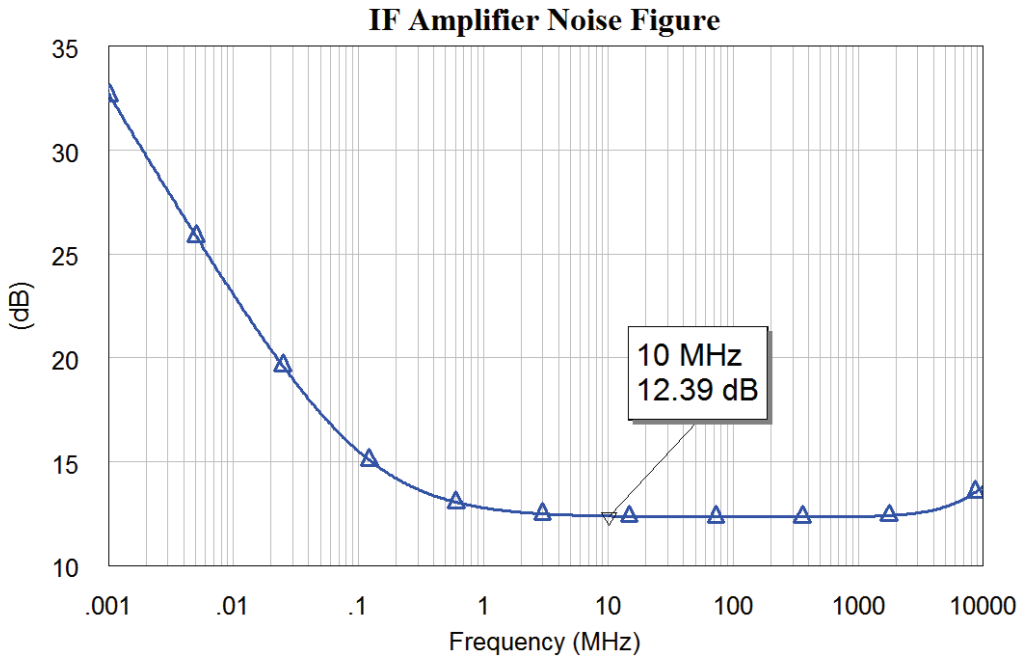

Figure 4.29 : IF amplifier noise figure according to frequency.

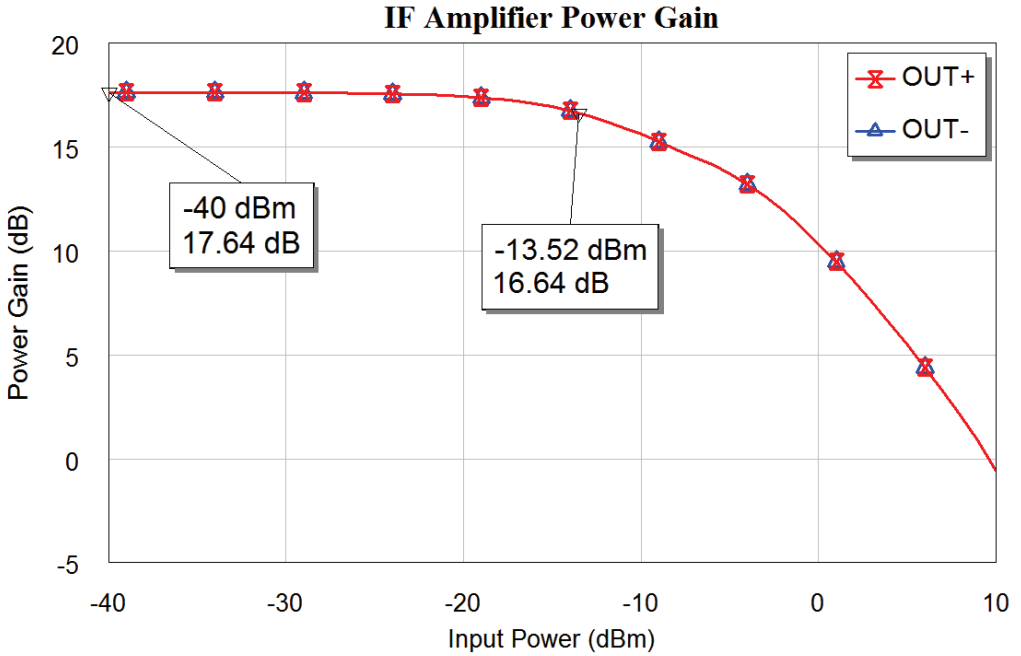

Figure 4.30 : IF amplifier power gain according to input power.

which the power gain decreases 1 dB. As shown in the graphics, the I1dB value of the IF amplifier is -13.5 dBm and the O1dB is 3.1 dBm. This result shows that a signal of up to 3.1 dBm can swing linearly at the both outputs of the If amplifier. It also means that the mixer can supply baseband signal to the IF amplifier up to -13.5 dBm.

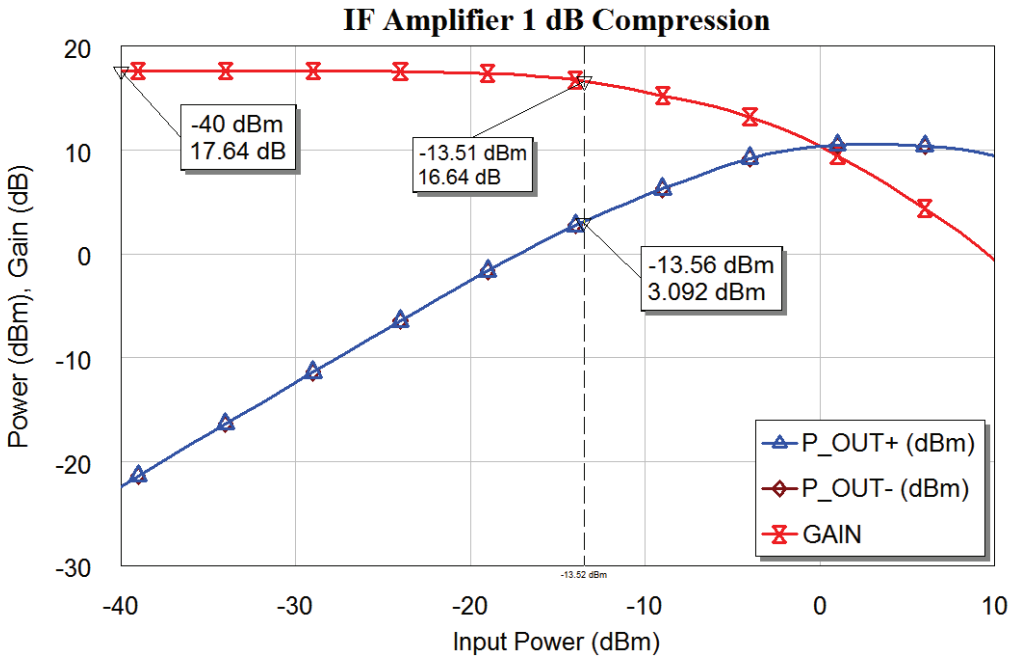

Figure 4.31 : IF amplifier output power and the 1 dB compression point.

4.4 Simulation Results of the Receiver

The building blocks designed and simulated separately are combined together to build the receiver circuit. Some simulations are performed on the whole structure to show the performance of the receiver topology. the first simulation performed on the receiver circuit is the Harmonic Balance simulation. In this simulation, the RF input is driven with a 50 Ω power source with -70 dBm signal power. This level of input signal power assures the signal not to be saturated through the topology. The input RF frequency is swept from 2 GHz to 10 GHz and the LO frequency is swept from 0.995 GHz to 4.995 GHz simultaneously. Thus, the IF signal frequency is kept constant at 10 MHz through out the simulation. The outputs of the receiver circuit is connected to 50 Ω loads.

Figure 4.32 shows the conversion gain graphics for both of the outputs separately. According to the simulation results, the overall receiver circuit supplies a conversion gain of around 61 dB within the target RF frequency range. The total conversion gain change within the range is about ±1.5 dB.

From the same simulation, The output frequency spectrum of the receiver is obtained as in Figure 4.33. Here, the IF ($f_{RF} - 2f_{LO}$) frequency component, the fundamental mixing product ($f_{RF} - f_{LO}$) component and the RF frequency (f_{RF}) component of the

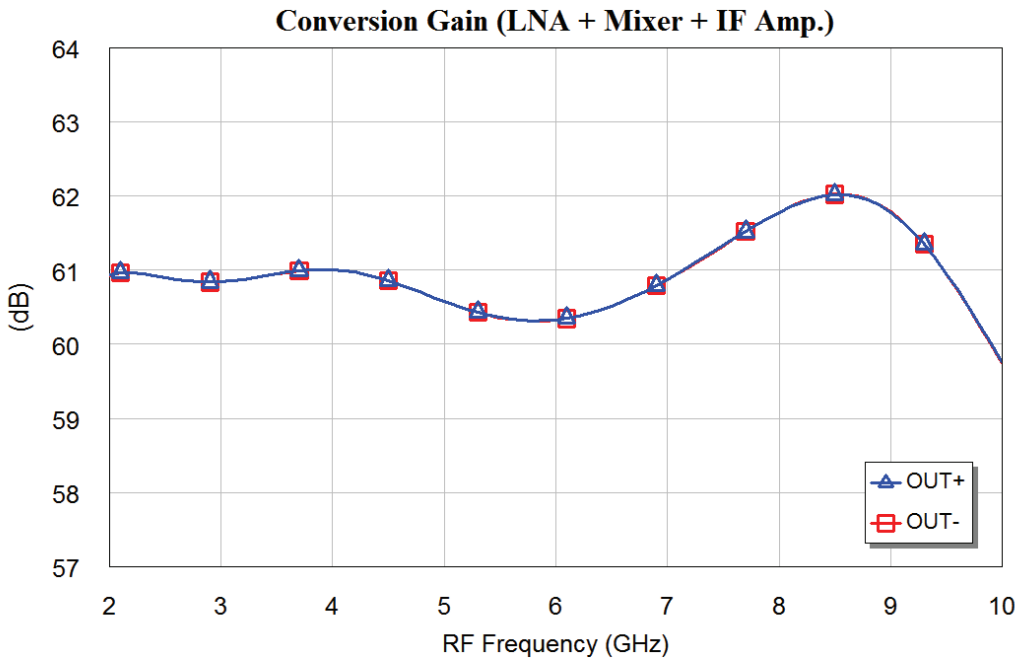

Figure 4.32 : The overall conversion gain graph of the receiver topology.

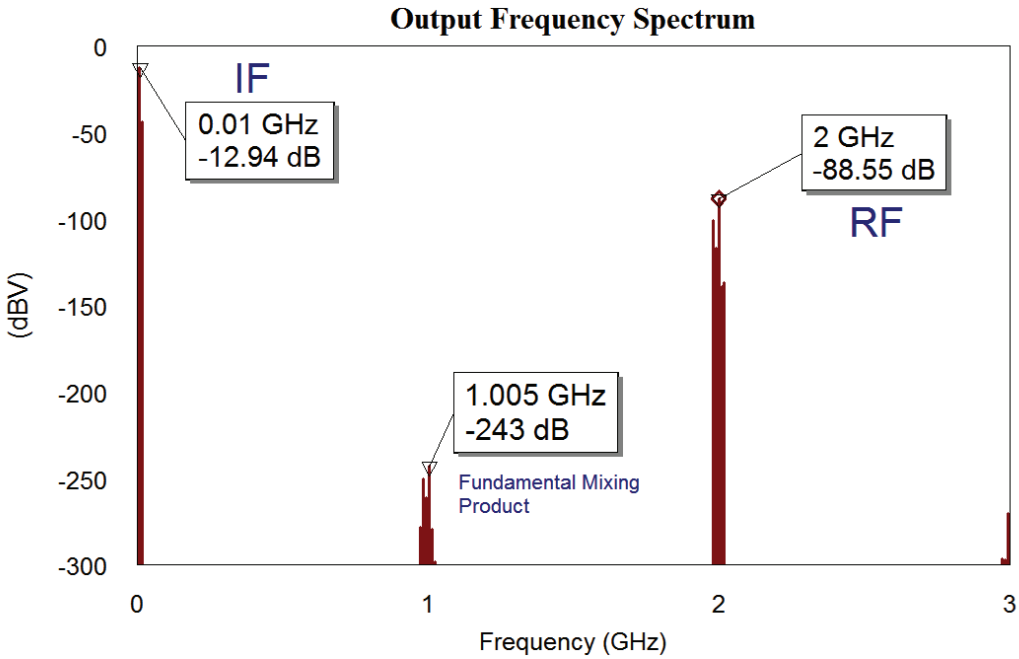

Figure 4.33 : The frequency spectrum of the IF signal.

output signal are marked on the graphic. The frequency spectrum belongs to a single output of the receiver. It is seen that even at a single output of the mixer, the DC offset voltage does not appear, the fundamental mixing product is suppressed and the higher frequency components are filtered out.

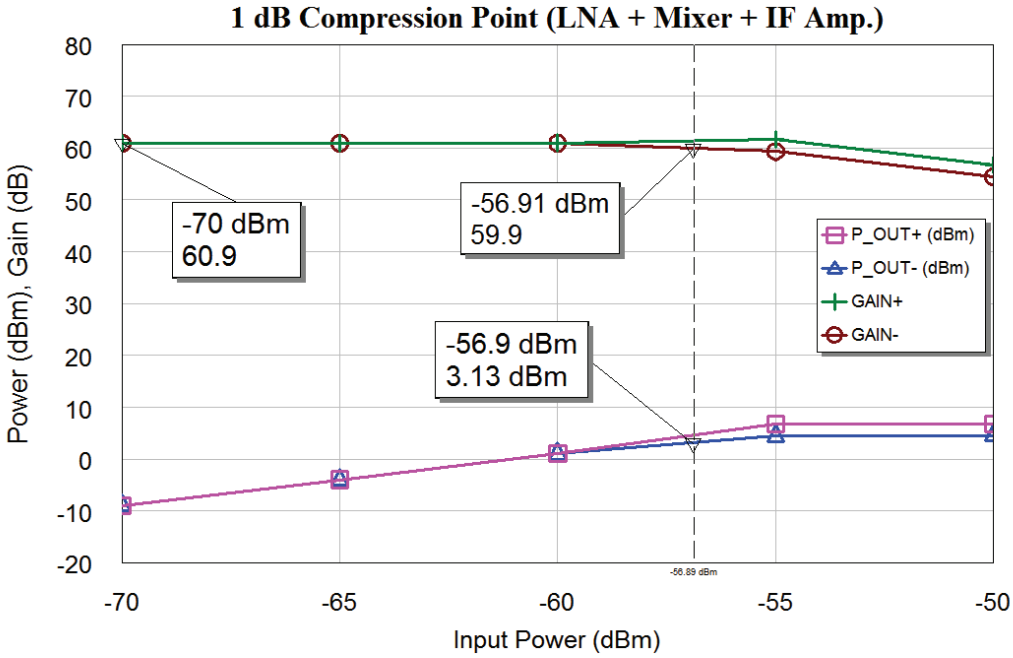

Figure 4.34 : 1 dB compression point of the overall receiver circuit.

For the evaluation of the dynamic range of the overall receiver topology, the Harmonic Balance simulation with a swept input power is performed on the circuit schematic. The input power is swept from -70 dBm to -50 dBm with 5 dBm steps at a single frequency of 2 GHz. The resultant output power graphics together with the conversion gain graphics are shown in Figure 4.34. On this graphic, the 1 dB compression point of the receiver circuit is marked. According to the simulation results, the O1dB of the receiver is 3.1 dBm for a single output and the I1dB is -57 dBm.

5. REALIZATION OF THE PROPOSED RECEIVER

The proposed second harmonic Zero-IF receiver topology is realized by using a 0.18 μm SiGe BiCMOS semiconductor processing technology. The utilized technology includes high frequency heterojuntion bipolar transistors (HBT) suitable for RF applications. There are also high Q passive components like on-chip spiral inductors, metal-insulator-metal (MIM) capacitors and polysilicon resistors available for the designers. Since it is a BiCMOS process, the technology also includes complementary metal oxide semiconductor (CMOS) transistors which are suitable for digital implementations.

The availability of the CMOS transistors on the same integrated circuit provides the possibility to implement some control circuitry and post processing circuitry on the same integrated circuit. As the target of the study is to develop a receiver topology which is suitable for integration, utilizing the advantages of such a process supports the achievement. Providing the capability of integrating the transceiver together with the digital control circuitry eases efforts of the IC manufacturers on efficiency in great extend.

In the study, the RFIC design of the topology is covered and the total layout of the proposed topology is prepared for manufacturing. For the manufacturing of the designed integrated circuit, a multi-project wafer (MPW) manufacturing method is targeted. In MPW manufacturing, the manufacturer provides predefined chip areas and collect the layouts of different researchers to put them together on the same wafer. Thus, supplying a possibility to manufacture very small amount of ICs for feasible prices which is an important chance for research and prototyping purposes.

Since in MPW production the chip area provided by the manufacturer is predefined, the layouts prepared should be suitable for placing in such an area. The chip area for the selected MPW production is 5 mm $\times$ 5 mm. The prepared layouts are arranged accordingly to use the available area efficiently. Different layouts of the receiver

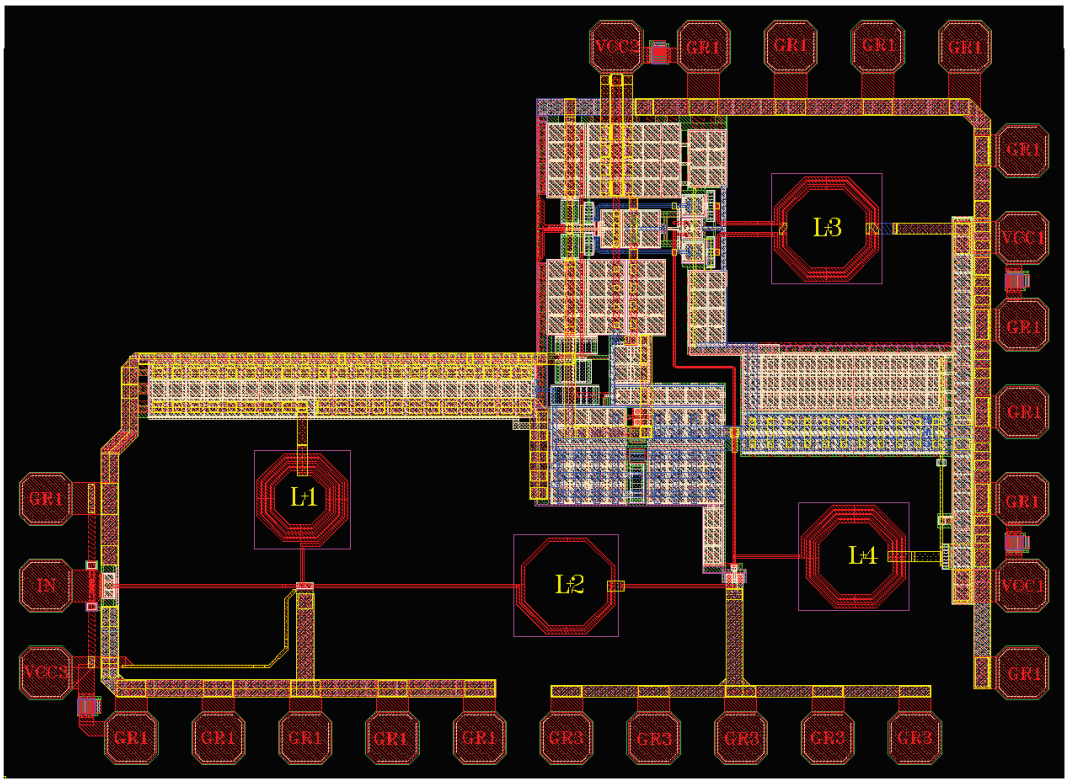

Figure 5.1 : Layout of the LNA.

topology, separate LNA circuit and separate mixer circuit is prepared and placed in the IC. In the following sections, the layouts prepared are explained.

5.1 Layout of the LNA

The layout of the LNA is the largest block in the overall receiver layout. It contains three single-ended and one differential inductors which cover the most area in the chip. Besides covering a large are themselves, the inductors should also placed apart carefully not to correlate each other. Thus, the required area for such a circuit extends larger by the number of inductors included. They are placed at the top metal layer of the process and the underneath is left blank. Structures that are not kept away in a sufficient distance can effect the inductor and decrease the quality factor of it drastically. Layout prepared for the LNA is shown in Figure 5.1.

In the layout, the inductors are kept at least 200 μm away from each other to satisfy sufficient isolation between them. The first stage of the LNA, which covers more than half of the area, is placed at the bottom side of the layout. The RF input is placed on the left side. The ground connections of the first stage and the rest of the circuit

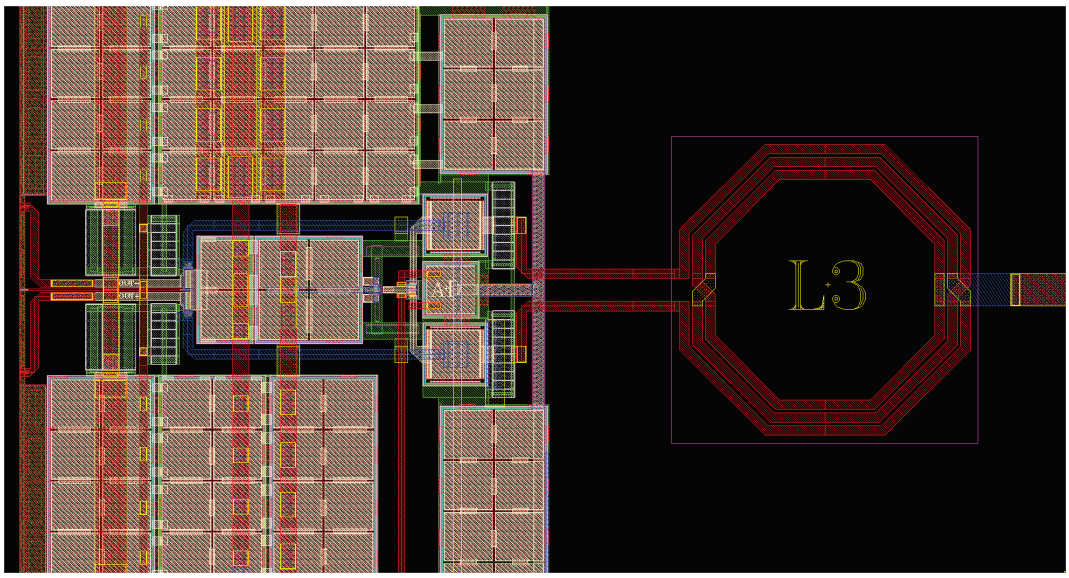

Figure 5.2 : Layout of the second stage of the LNA.

is separated. The ground connections of the input stage is place at the bottom side. Plural pads are used for the ground connection of input stage to minimize the parasitic inductance of the total bonding wires.

To isolate the first stage from the second stage of the LNA, the second stage is placed at a separate location at the upper side of the layout. The VCC and ground connections of the second stage are also separated from the first stage. The biasing pad of the second stage VCC2 is placed at the top side of the layout. the ground connection which is also biasing the overall substrate, GR1, is connected to a number of pads all around the layout to decrease the parasitic inductance thus for grounding the layout efficiently.

The second stage of the LNA is a differential pair which is used to convert the single-ended input signal to differential balanced signal. Thus, for proper performance the symmetry of this stage is important. As seen in Figure 5.2, a symmetric layout for this differential stage is satisfied. The layout of the LNA is prepared considering also space required for the layout of the other blocks. LNA part of the layout is tried to be isolated from the rest of the circuits by using substrate contacts and different type dopped wells. All the blank space are filled with coupling capacitors to stabilize the DC biases.

For testing purposes, the layout of the LNA is also placed alone in the integrated circuit. The layout of the separate LNA is shown in Figure 5.3. Since the total chip area is fixed, the DC biasing pads on the top side and right side of the layout are replaced to

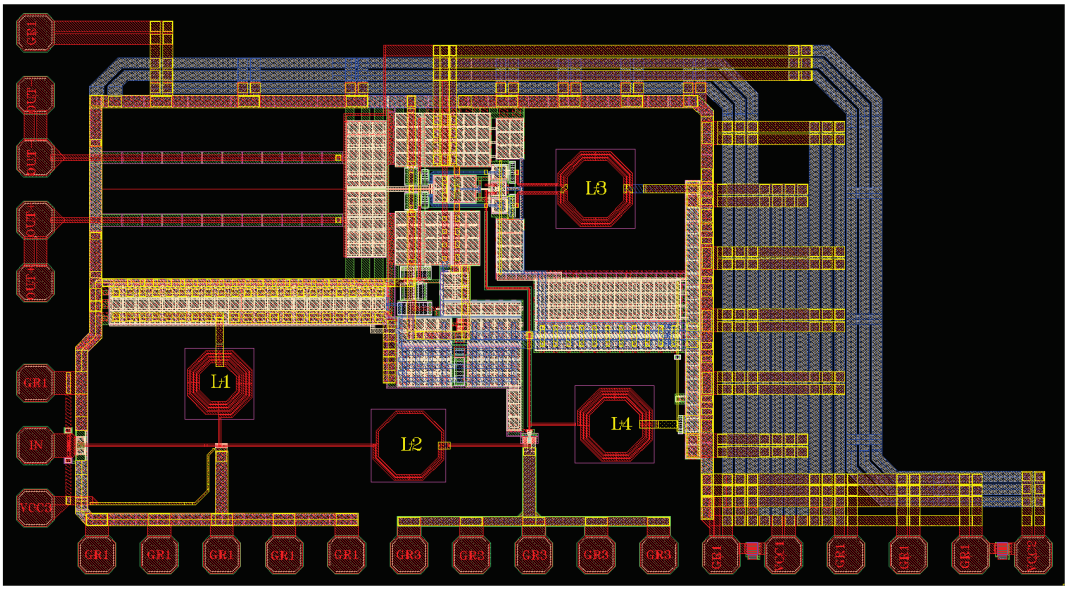

Figure 5.3 : LNA layout prepared for MPW placement.

the bottom side. This separate layout is place on the bottom left corner of the overall IC such as the pads stay near the sides of the IC. This placement is done to shorten the lengths of the bonding wires thus the parasitic inductances.

5.2 Layout of the Second Harmonic Mixer

The second harmonic mixer is directly connected to the outputs of the LNA in the proposed topology. The symmetric structure from the second stage of the LNA continues through the fully differential second harmonic mixer circuit. In the layout design of the mixer, the separation and isolation of the LO inputs and the RF inputs gain importance. Thus, they are kept away from each other as much as possible. The signal paths of both signals are also kept orthogonal to minimize the crosstalk.

The layout of the second harmonic mixer is seen in Figure 5.4 together with the IF amplifier and the passive LPF as a single block. The pads of the block layout are placed according to the MPW die placement requirements. In the actual receiver layout, the input RF connections of the mixer is connected to the LNA outputs directly, thus the pads for these connections are removed.

A symmetric path is prepared for both the differential LO signal and the differential RF signal. For isolation, a separate pad for the VCC biasing of the mixer is placed. For proper grounding, multiple pads as much as possible are placed around the layout.

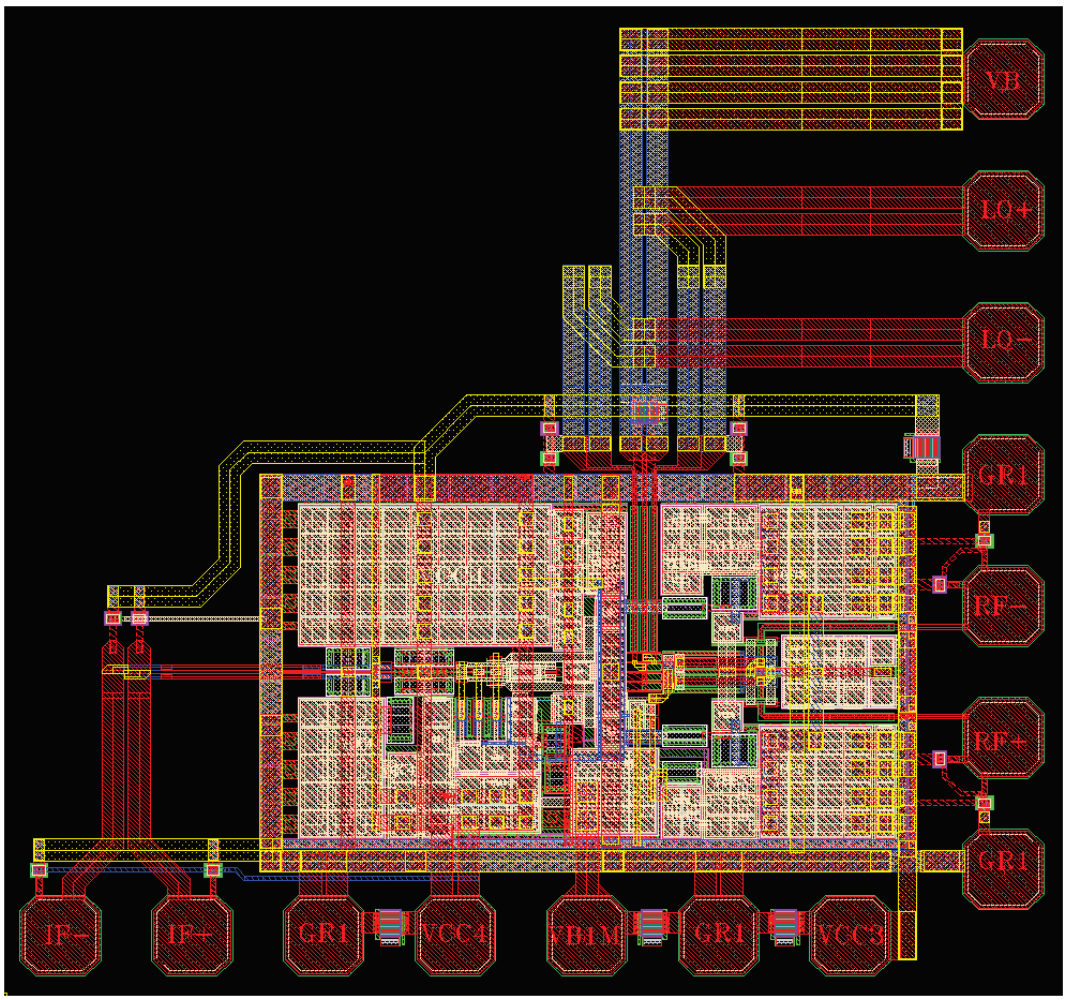

Figure 5.4 : Layout of the second harmonic mixer and the IF amplifier arranged for MPW placement.

Since the mixer circuit does not contain any on-chip inductors, the layout area of the mixer is much smaller compared to the LNA. Here, the advantages of the simple structure of the proposed topology and the second harmonic mixer is seen as the ease of integrability.

Two different layouts for the separate placements of the second harmonic mixer circuit are prepared with minor differences. One of the layouts including only the second harmonic mixer is shown in Figure 5.5. As a difference between these two layouts, only the pads for the differential LO signal inputs and the differential IF outputs are replaced. By placing the second harmonic mixer separately, it is aimed to be capable of testing the proposed structure alone without the effects of other blocks and verifying the effectiveness of the 2LO leakage suppression mechanism.

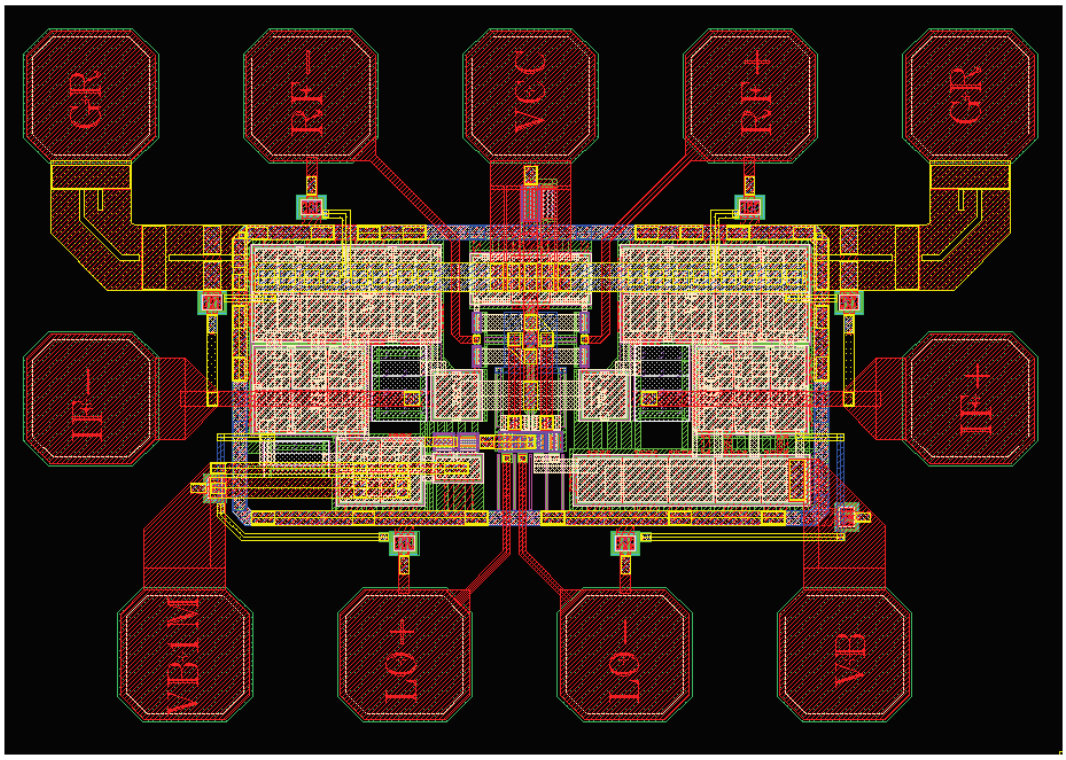

Figure 5.5 : Layout for separate placement of the proposed second harmonic mixer.

5.3 Layout of the IF amplifier

The layout of the second harmonic mixer is followed by the layout of the IF amplifier. The IF amplifier also has a fully differential structure thus the layout is drawn as symmetrical as possible. The IF amplifier has a simple structure and a small layout. Since it is designed to operate in the baseband, the preparation of the layout does not involve RF concerns. The outputs of the IF amplifier and the ground connections are placed at the left side of the overall layout. Between the IF amplifier and the second harmonic mixer, a symmetrical passive LPF also exists.

In Figure 5.4, the second harmonic mixer and the IF amplifier layouts are seen together. They are prepared together in such a way that their VCC and ground connections are laid together covering the both layouts. The signal path follows a straight line along the both structures. The available blank spaces are filled with coupling capacitors for proper DC biasing. The layout prepared for the mixer and IF amplifier covers almost one forth of the overall layout.Figure 5.4 shows the separate layout of the second harmonic mixer and the IF amplifier together to be placed on the MPW die as a test structure.

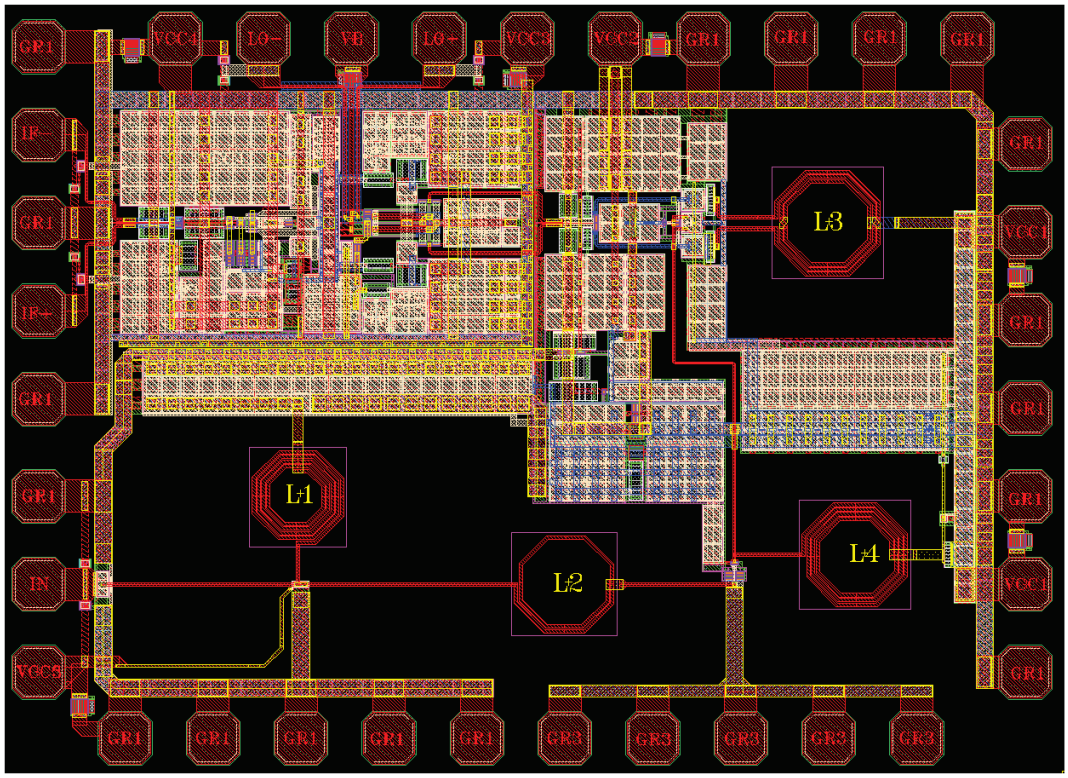

Figure 5.6 : Layout of the integrated receiver topology.

5.4 Layout of the Receiver

The layouts prepared for the circuit blocks are combined together as a single integrated circuit as shown in Figure 5.6. The overall receiver topology occupies a rectangular area of around 1800 μm $\times$ 1300 μm. The layout of which pads are rearranged for the MPW is shown in Figure 5.7. When rearranging the pads according to MPW die area, it is considered to move the DC pads towards two sides of the circuit. The connections between the moved pads and the circuit are done with multiple wide metal lines to prevent resistive loss.

5.5 Placement of the MPW Die

The placement of all the test structures for the receiver circuit blocks and the layout of the receiver itself is shown in Figure 5.8. In this figure, the whole 5 mm $\times$ 5 mm die area is seen. The test structures explained in the previous sections are placed close to the sides. Placing the layouts of the test structures close to the sides is necessary for easy accessibility of the pads for the bond wiring. The closer connections also shortens

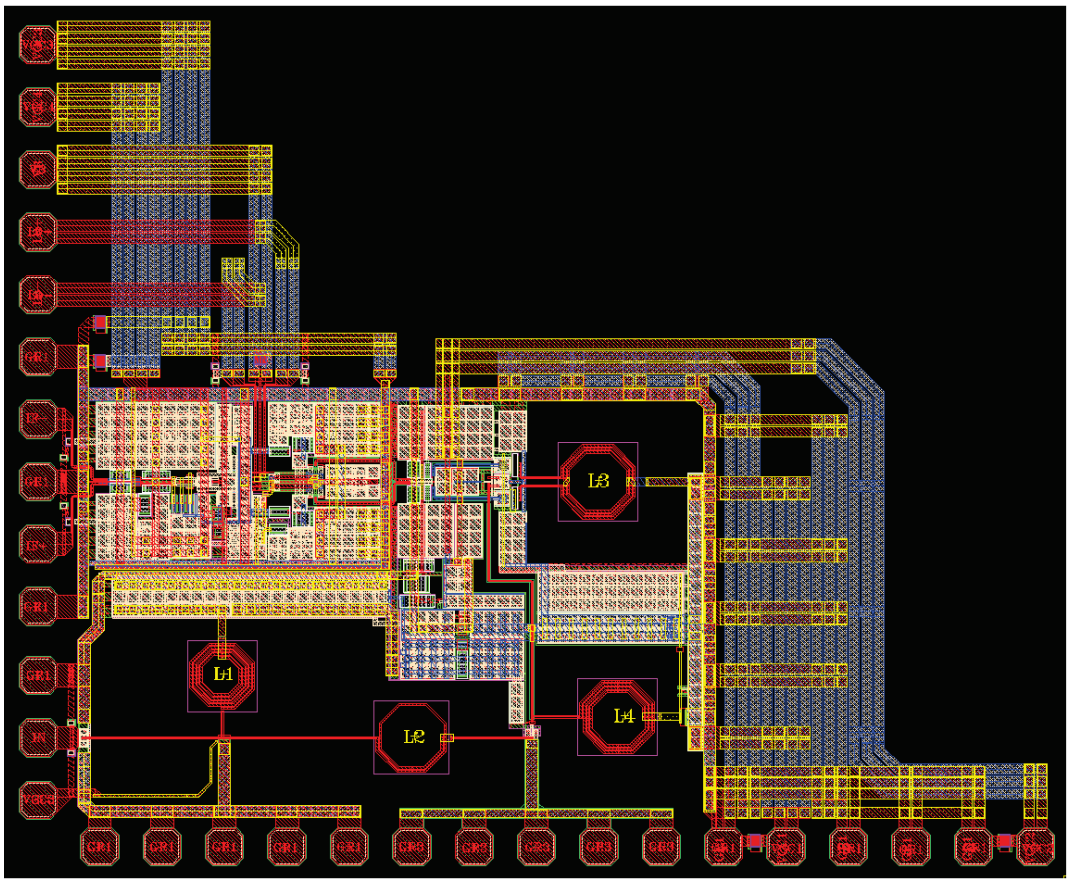

Figure 5.7 : Layout of the integrated receiver topology.

the length of the bond wires. Shorter the bond wires, the less parasitic inductances they present to the relevant connections.

In Figure 5.9, the final layout for the MPW manufacturing is seen. When the prepared test structures are placed in the overall die area, it is seen in Figure 5.8 that almost the half of the die area is covered. To utilize the remaining area, some other basic test structures are prepared. These test structures include the devices of the used technology like HBTs, inductors and MIMs. For testing these devices and verifying with the model files, the remaining area of the MPW chip is filled with the layouts of the devices. Since the testing of these devices are done with probe connections on probe station, the accessibility of their pads is not important.

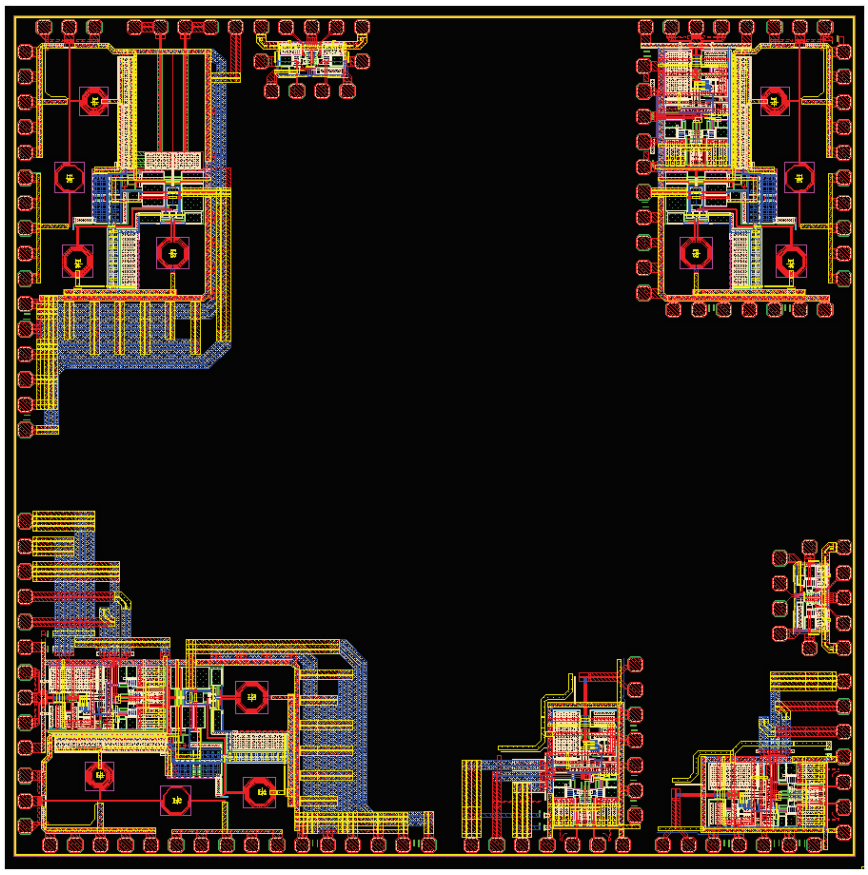

Figure 5.8 : Placement of the layouts of the test structures on the MPW die.

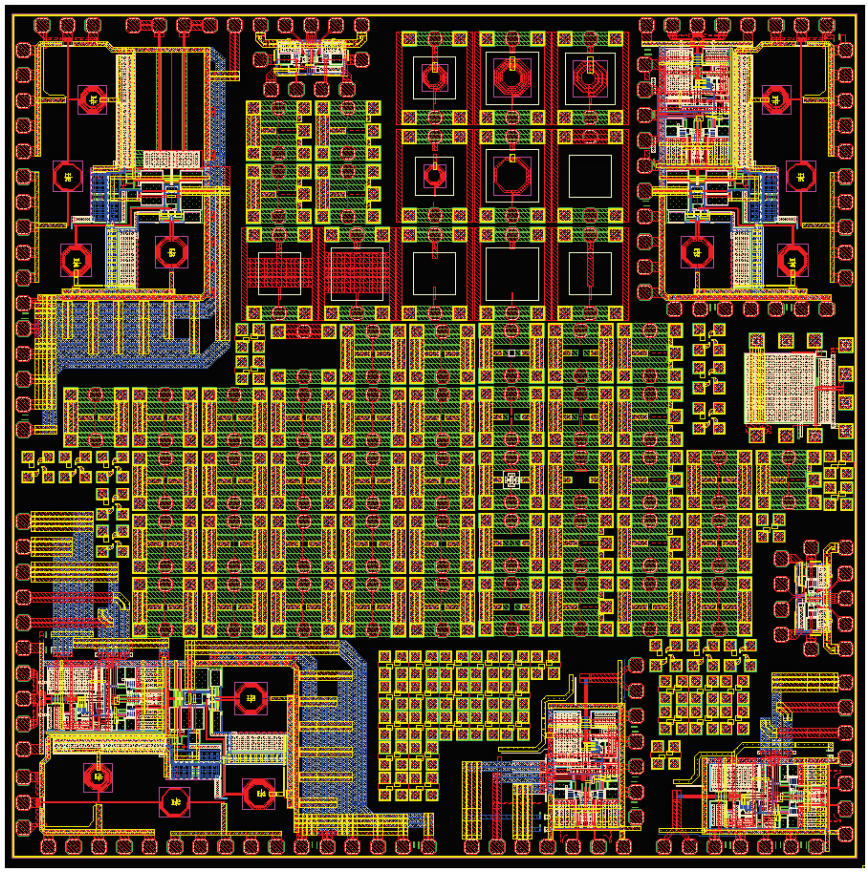

Figure 5.9 : Final layout of the MPW chip.

6. MEASUREMENT OF THE REALIZED TEST STRUCTURES

The realized second harmonic Zero-IF receiver topology and its test structures are manufactured with 0.18 μm SiGe BiCMOS technology. Photograph of the manufactured 5 mm $\times$ 5 mm IC is shown in Figure 6.1. Test chip includes the receiver topology and some separate sub-modules of it along with some other testing structures for the electronic components of the relevant technology. The layout of the test chip is given in Figure 5.9 in Section 5.5.

For measurement purposes, two separate test Printed Circuit Boards (PCB) are designed and manufactured with an appropriate board material. The board material for the testing PCBs is selected to support operating frequencies up to 10 GHz. Test chip is planned to be bonded directly to the test PCBs instead of placing it in a package, not to introduce extra parasitics from the package, effecting the performance of the IC. Therefore, to be able to directly bond the test chip to the PCBs, both of the PCBs are covered with gold and designed appropriately to match the dimensions of the IC and the coordinates of the corresponding bonding pads on the IC.

6.1 Printed Circuit Board for the Mixer + IF Amplifier Test Structure

The first test PCB is designed to measure the second harmonic Zero-IF mixer circuit in which the main contribution is made upon the study, thus, the separate testing structure which includes the mixer and the IF amplifier following the mixer is selected to be measured first. The layout of this test structure is shown in Figure 5.4. This target structure for the measurement is placed at the lower right corner of the test chip shown in Figure 6.1.

The PCB is designed to include minimum extra components for just satisfying the required biasing and operating conditions for an accurate measurement. All the biasing voltages are supplied externally by DC power supplies of which lines on the PCB include only coupling capacitors. The proposed second harmonic mixer topology has differential RF and LO inputs and the IF amplifier has differential IF outputs. In the

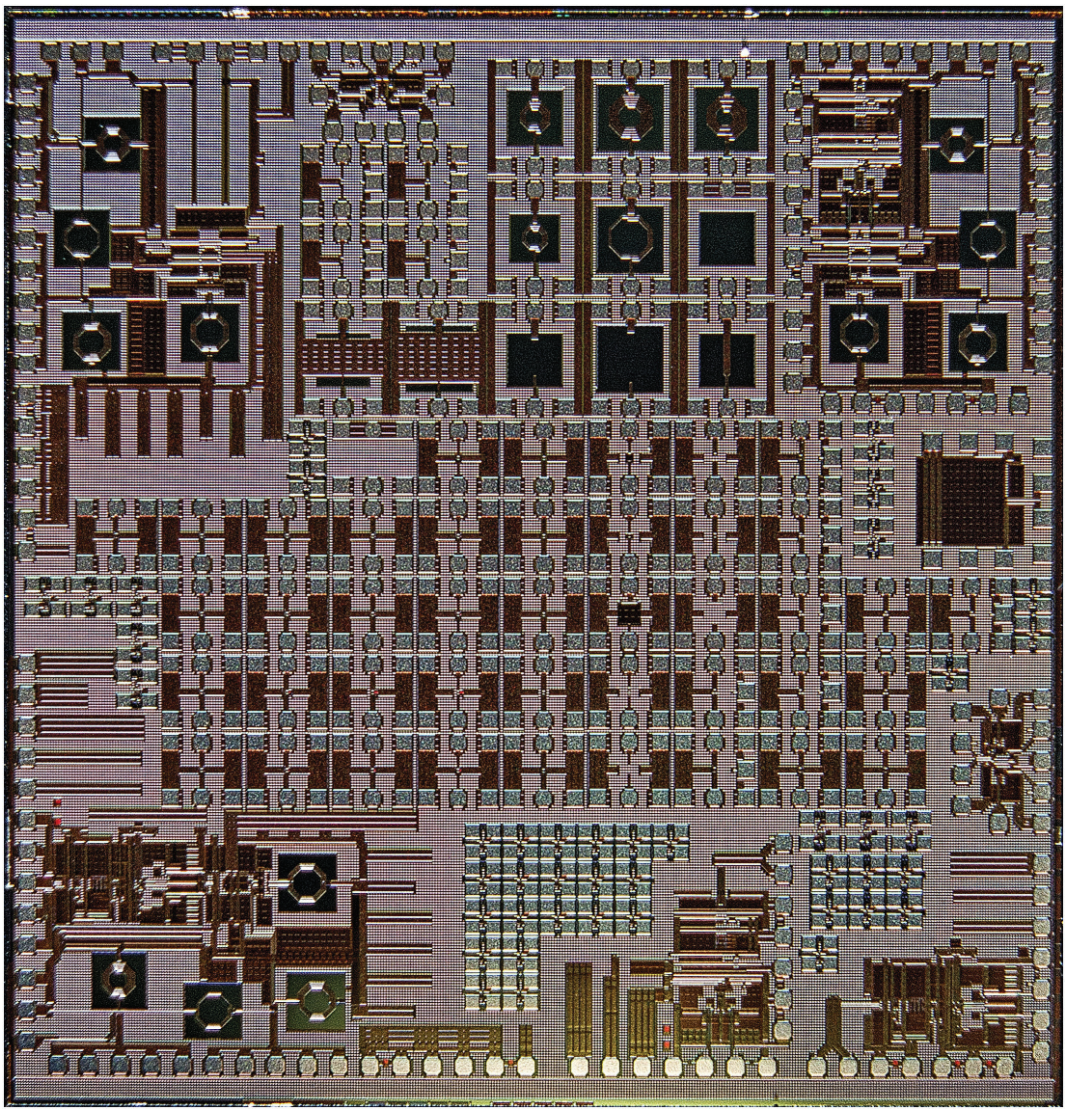

Figure 6.1 : Photograph of the manufactured test IC.

overall receiver topology, the mixer is driven by an LNA which is also supplying the required DC biasing voltage for the RF inputs, thus, in this separate test structure "Mixer + IF Amplifier", the mixer does not include biasing circuitry for the RF inputs. Therefore, a basic biasing circuitry for the RF inputs along with the biasing circuitry for the LO inputs is placed on the first test PCB.

In order to drive the differential RF and LO inputs properly from single ended signal generators, appropriate transformers are selected and placed on the PCB. The selected transformer for the LO signal is TCM4-452X+ which can be used between the frequencies 20 MHz and 4500 MHz, and the selected transformer for the RF signal is TCM1-63AX+ which is functional between the frequencies 10 MHz and 6000 MHz. Since, neither a single transformer which is functional within the whole operating band

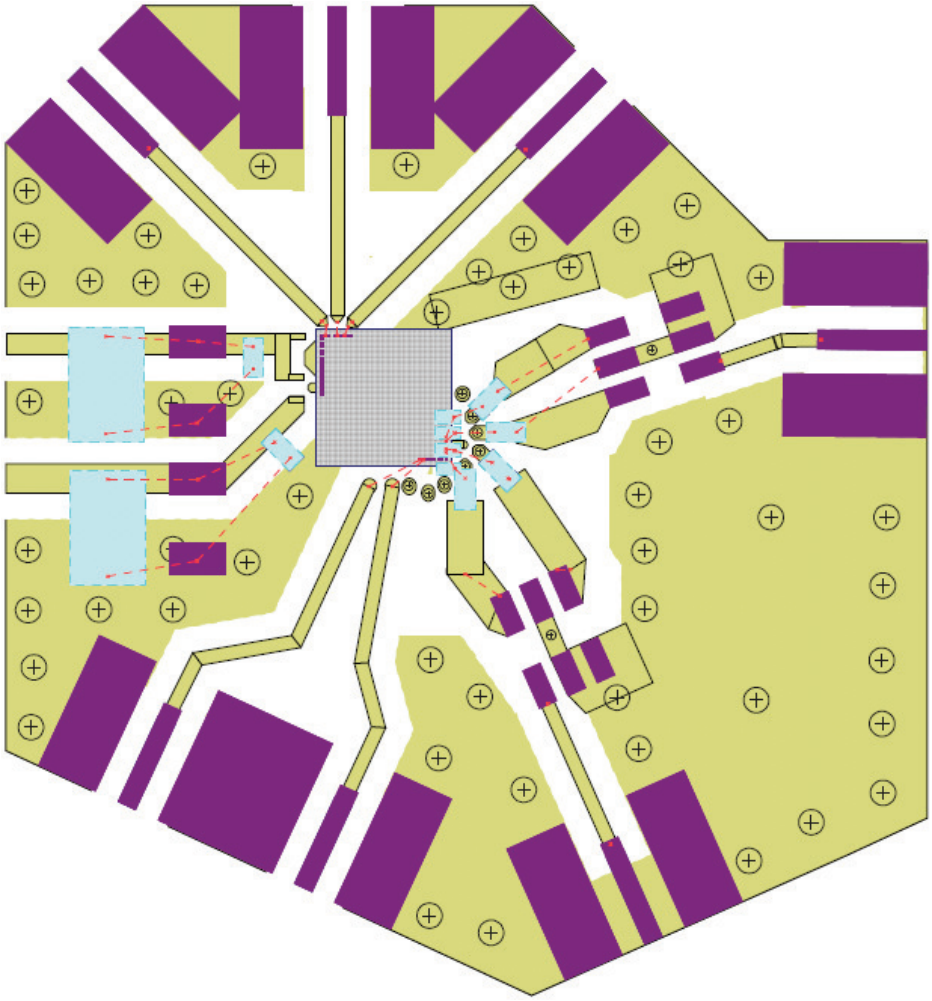

Figure 6.2 : Layout of the first test PCB.

of the mixer, nor multiple transformers with the same footprint of which operating frequencies cover the interested band together could not be found, the upper frequency limit for the measurements is set to be 6 GHz in the first step. It is decided to leave the measurement of the whole operation band to the second test PCB in which the overall receiver topology is subject to tests. The prepared layout of the first test PCB is shown in Figure 6.2.

6.1.1 Test Setup-1 for the Mixer + IF Amplifier Test Structure

It is aimed to verify the functionality of the proposed second harmonic mixer topology and measure the conversion gain upon the built test setup. Separate signal generators are used to supply the RF and LO signals, while the proper DC biasing is satisfied via external power supplies. Built testing setup for the measurement of conversion gain is given in Figure 6.3. DC biasing circuitry of the RF and LO differential inputs are

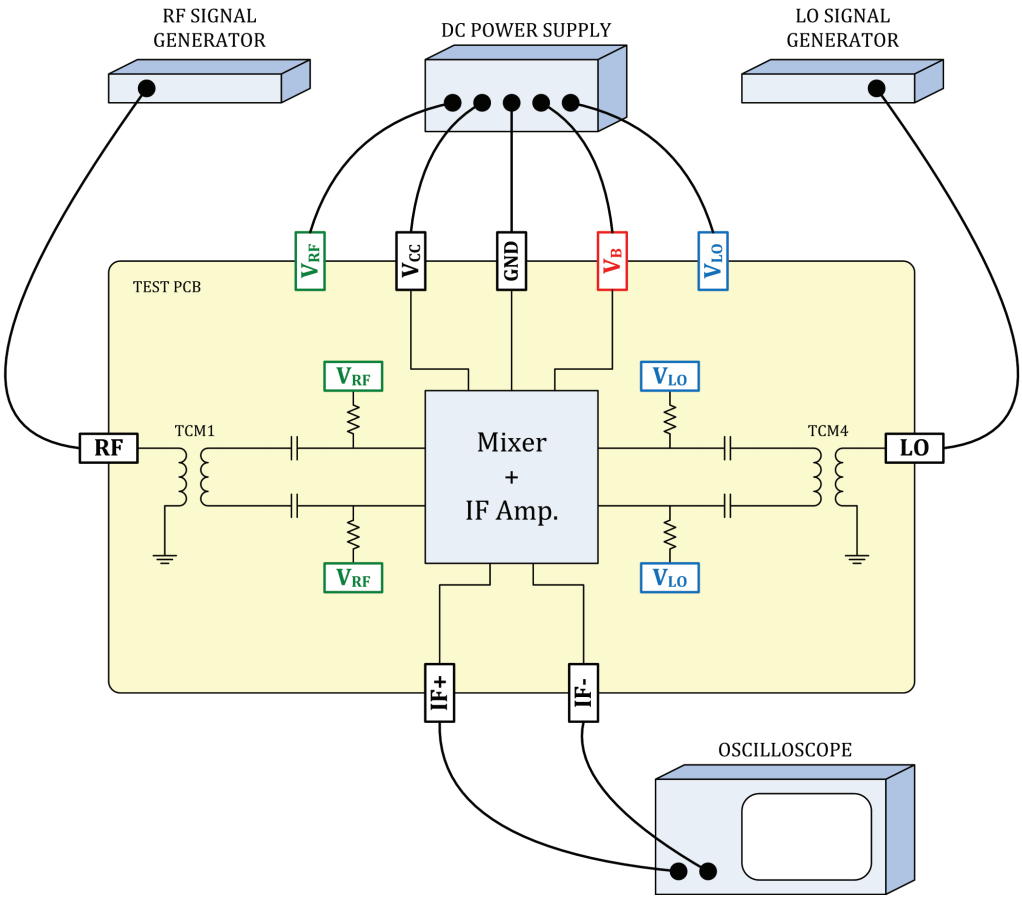

Figure 6.3 : Test setup for the conversion gain measurements of the Mixer + IF Amplifier test structure.

also shown in this basic schematic. An oscilloscope with 50 Ω inputs is used at the IF outputs to monitor the resultant IF signal.

Figure 6.4 shows the photograph of the prepared first test PCB connected to the testing equipment. The photographs of the actual testing environment, testing equipments along with the PCB, are given in Figure 6.5 and Figure 6.6.

For the measurements, the DC levels of the RF and LO inputs are set as 2.6 V and 1.75 V respectively as they are used in all the simulations through out the thesis. The V_{CC} of the circuit is supplied with 5 V. The biasing voltage V_B, which is one of the main factors determining the conversion gain and the linearity of the pumping current as described in Chapter 3, is set to 1.84 V and this biasing value results in $\Delta V = 90\,mV$, where ΔV corresponds to the voltage difference $V_B - V_C$ defined in Chapter 3. Since the value of the biasing voltage V_B has a considerable impact on the conversion gain, it is also used as a tuning mechanism to compensate the decrease in gain at higher

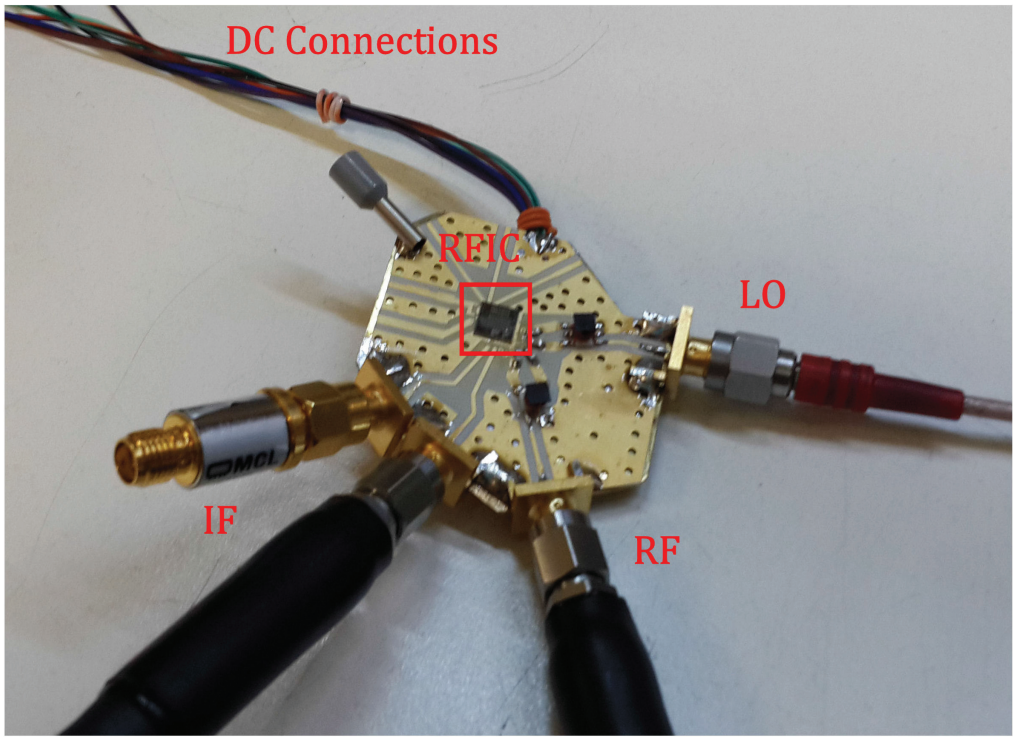

Figure 6.4 : Photograph of the first test PCB in the actual testing environment.

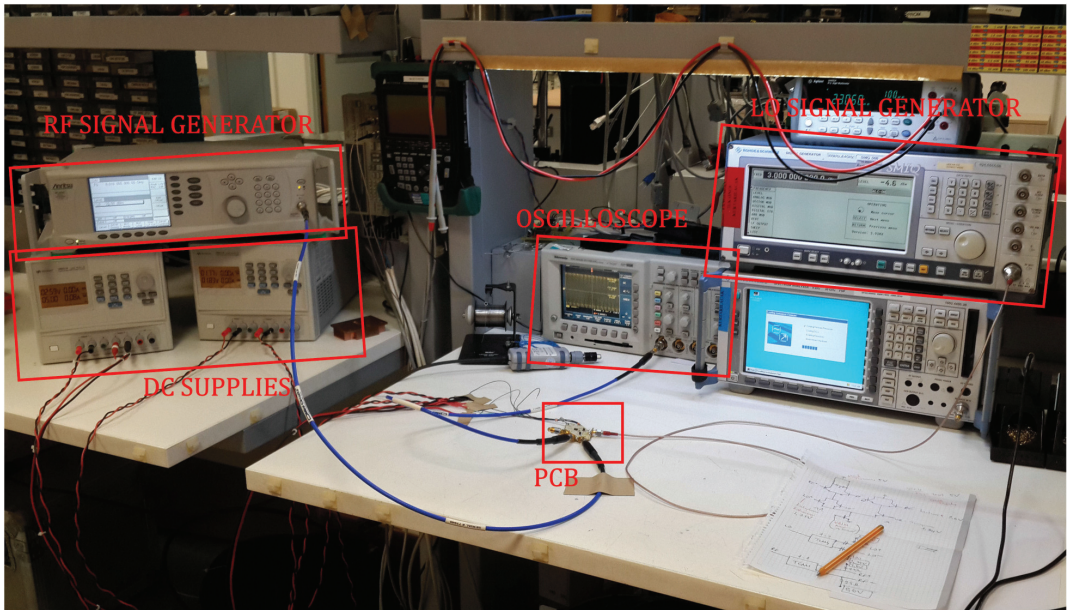

Figure 6.5 : Photograph of the actual testing environment.

frequencies due to PCB originated losses. Thus, the value of the V_B biasing voltage is decreased to 1.83 V for the RF frequencies above 5 GHz which results in $\Delta V = 80\ mV$.

For all the measurements performed, the power of the LO signal is kept as -2 dBm, the RF and LO signal frequencies are selected such as to keep the resultant IF signal frequency as 5 MHz. Results of the performed measurements are given in

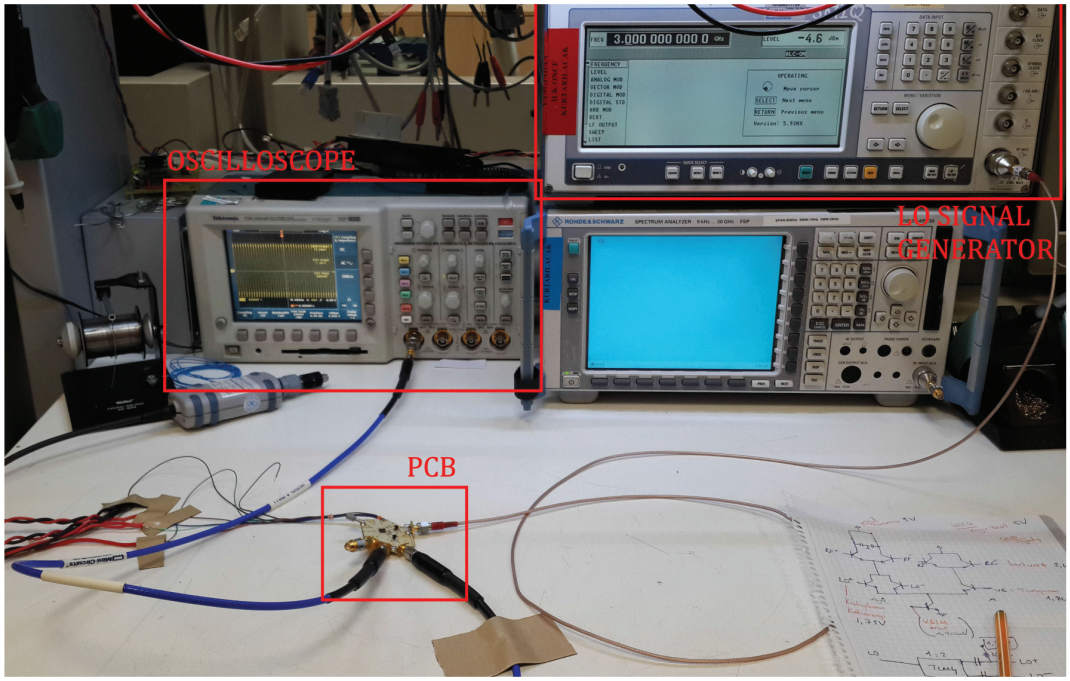

Figure 6.6 : Photograph of the actual testing environment.

Table 6.1 : IF measurements for $f_{LO} = 1\ GHz$, $f_{RF} = 2.005\ GHz$, $\Delta V = 90\ mV$.

P_{RF} [dB]	V_{PP} [mV]	P_{IF} [dBm]	Conversion Gain [dB]
-50	92	-6.745	43.255
-45	152	-2.384	42.616
-40	263	2.379	42.379
-35	462	7.272	42.272
-30	780	11.821	41.821
-25	1020	14.151	39.151
-20	1120	14.964	34.964
-15	1140	15.115	30.117

Table 6.1 through Table 6.5. Upon the measurements, peak-to-peak voltage amplitude of the resultant IF signal is measured for different RF power levels. Then, measured peak-to-peak voltage levels, V_{PP}, are converted into P_{IF} which is the signal power on 50 Ω load resistance in dBm. Therefore, the conversion gain column in the tables gives the difference between the output power P_{IF} and the input power P_{RF} in dB.

In order to visualize the results clearly, measurement results given in Table 6.1 through Table 6.5 are represented as graphics given in Figure 6.7 to Figure 6.10. Through out the measurements the LO frequency is changed such as to keep the IF frequency at 5 MHz.

Table 6.2 : IF measurements for $f_{LO} = 1.5\ GHz$, $f_{RF} = 3.005\ GHz$, $\Delta V = 90\ mV$.

P_{RF} [dB]	V_{PP} [mV]	P_{IF} [dBm]	Conversion Gain [dB]
-50	75	-8.519	41.481
-45	130	-3.742	41.258
-40	225	1.023	41.023
-35	402	6.064	41.064
-30	680	10.630	40.630
-25	980	13.804	38.804
-20	1070	14.567	34.567

Table 6.3 : IF measurements for $f_{LO} = 2\ GHz$, $f_{RF} = 4.005\ GHz$, $\Delta V = 90\ mV$.

P_{RF} [dB]	V_{PP} [mV]	P_{IF} [dBm]	Conversion Gain [dB]
-50	75	-8.519	41.481
-45	130	-3.742	41.258
-40	230	1.214	41.214
-35	412	6.277	41.277
-30	680	10.630	40.630
-25	970	13.715	38.715
-20	1070	14.567	34.567

Table 6.4 : IF measurements for $f_{LO} = 2.5\ GHz$, $f_{RF} = 5.005\ GHz$, $\Delta V = 80\ mV$.

P_{RF} [dB]	V_{PP} [mV]	P_{IF} [dBm]	Conversion Gain [dB]
-50	99	-6.108	43.892
-45	167	-1.566	43.434
-40	298	3.464	43.464
-35	510	8.131	43.131
-30	835	12.413	42.413
-25	1030	14.236	39.236
-20	1120	14.964	34.964

Table 6.5 : IF measurements for $f_{LO} = 3\ GHz$, $f_{RF} = 6.005\ GHz$, $\Delta V = 80\ mV$.

P_{RF} [dB]	V_{PP} [mV]	P_{IF} [dBm]	Conversion Gain [dB]
-50	80	-7.959	42.041
-45	140	-3.098	41.902
-40	240	1.584	41.584
-35	440	6.848	41.848
-30	730	11.246	41.246
-25	1020	14.151	39.151
-20	1140	15.117	35.117

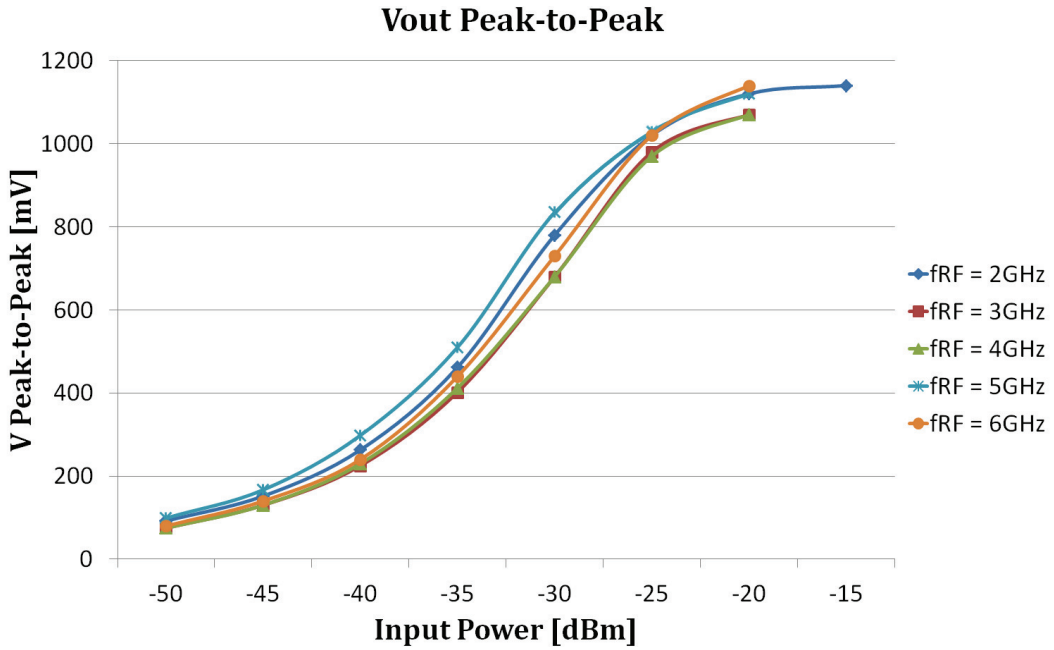

Figure 6.7 : Measured peak-to-peak IF amplitude, V_{PP}, according to the input RF power at different frequencies.

In Figure 6.7, peak-to-peak IF signal voltage values are shown according to input RF power for different frequencies. According to the graph, the output IF signal can swing about 1000 mV linearly. Figure 6.8 shows the same measurements represented as the power on a 50 Ω load resistance. From both graphics, it is seen that the input RF power can be increased up to -25 dBm for the Rf frequencies below 4 GHz and -30 dBm for the RF frequencies above 4 GHz without any degradation in the output IF signal and the conversion gain.

Calculated conversion gain values are given in Figure 6.9 and Figure 6.10. Figure 6.9 shows the degradation in conversion gain when the input RF power is increased while Figure 6.10 emphasizes the stability of the conversion gain according to frequency. According to Figure 6.9, input 1 dB compression point, I1dB, is about -27 dBm which is close to the simulation resuls of -26 dB. Figure 6.10 show that the conversion gain stays almost constant for the whole measured band as expected. Conversion gain of the "Mixer + IF Amplifier" test structure changes about $\pm$1 dB around 32 dB.

Total conversion gain of 32 dB shown in Figure 6.10 also includes some extra losses due to transformers used to convert the single ended signals to differential signals, and the connection cables, both of which are not included in the circuit simulations performed in Chapter 4. Therefore, transformer losses and the connection cable losses

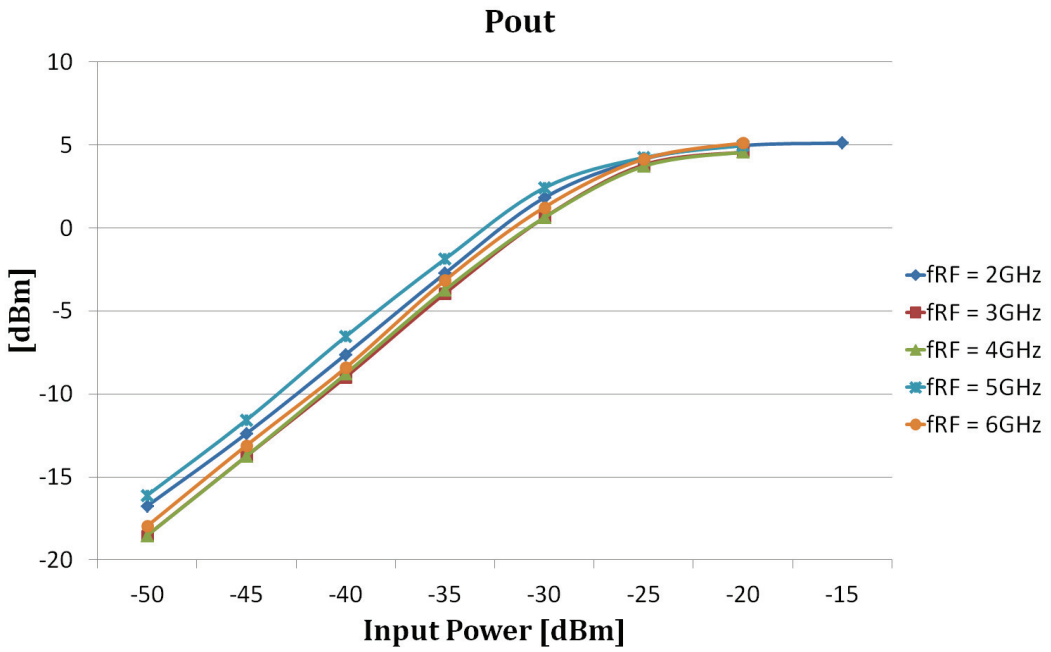

Figure 6.8 : Calculated IF power, P_{IF}, according to the input RF power at different frequencies.

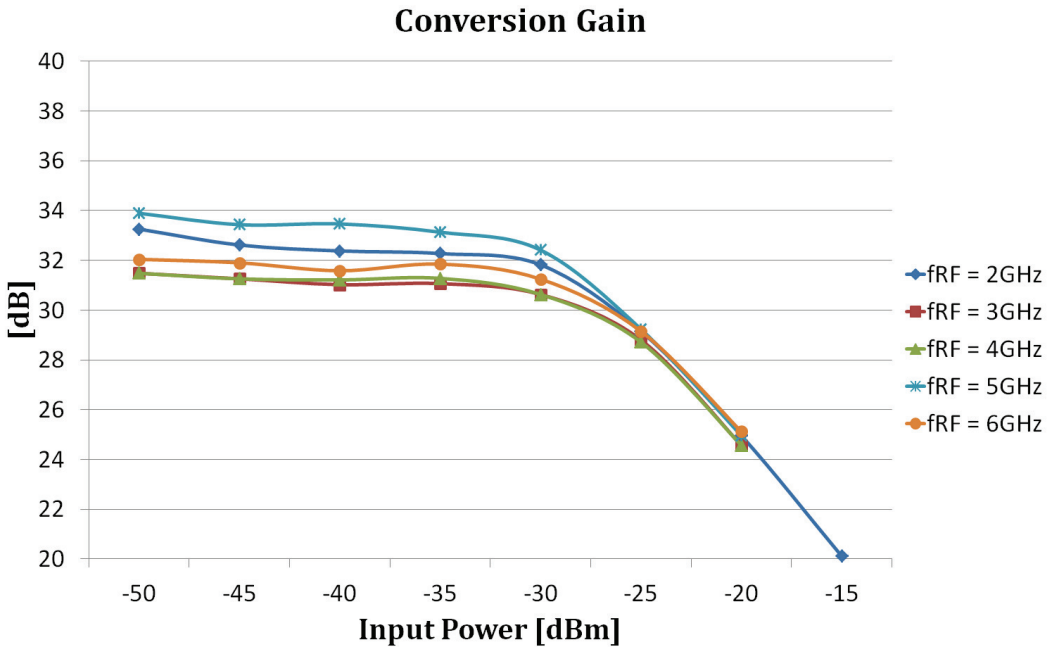

Figure 6.9 : Calculated conversion gain according to the input RF power at different frequencies.

according to frequency is measured and given in Figure 6.11 and Figure 6.12. TCM1 and TCM4 of which losses are given in Figure 6.11 are the transformers used on the RF and LO signal paths respectively. In Figure 6.12, losses originated form the connection cables of the RF and the LO signals are given respectively.

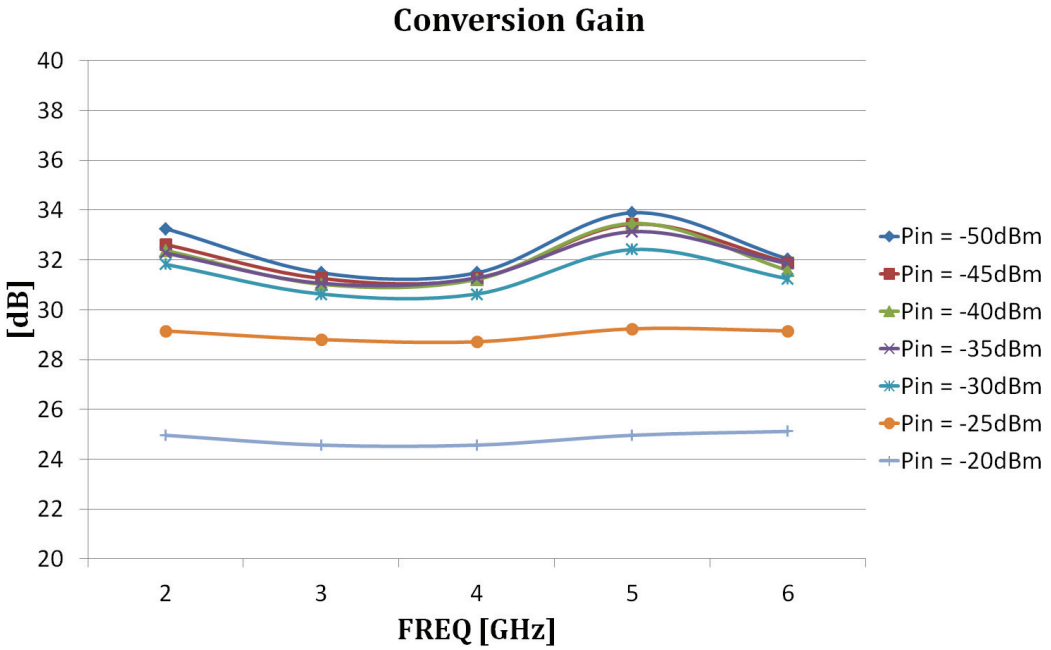

Figure 6.10 : Calculated conversion gain according to the input frequency.

In the measurements, in order to compensate the PCB and other peripheral losses in the LO path, the LO signal power is increased to -2 dBm. Losses on the RF signal path given in Figure 6.11 and Figure 6.12 are added to the measured conversion gain values and the obtained actual conversion gain graphics are given in Figure 6.13 and Figure 6.14. Figure 6.13 shows the compensated conversion gain according to input power, while Figure 6.14 represents the change of the compensated conversion gain according to the RF frequency. It is seen that when the transformer and cable losses are added to the measured conversion gain values, average conversion gain is obtained as 35 dB which is in agreement with the simulation results. The simulation result for the conversion gain of the mixer with IF amplifier structure is also plotted in the same graph to compare with the measurement results. The relevant simulation result is given in Figure 4.19 in Section 4.2 originally.

6.1.2 Test Setup-2 for the Mixer + IF Amplifier Test Structure

In the second test setup for the Mixer + IF Amplifier test structure, it is aimed to measure the leakage of the second harmonic component of the LO signal to the RF port. The setup for this measurement is illustrated in Figure 6.15. The IF outputs are terminated with 50 Ω load resistances. LO signal is applied to the LO port of the PCB

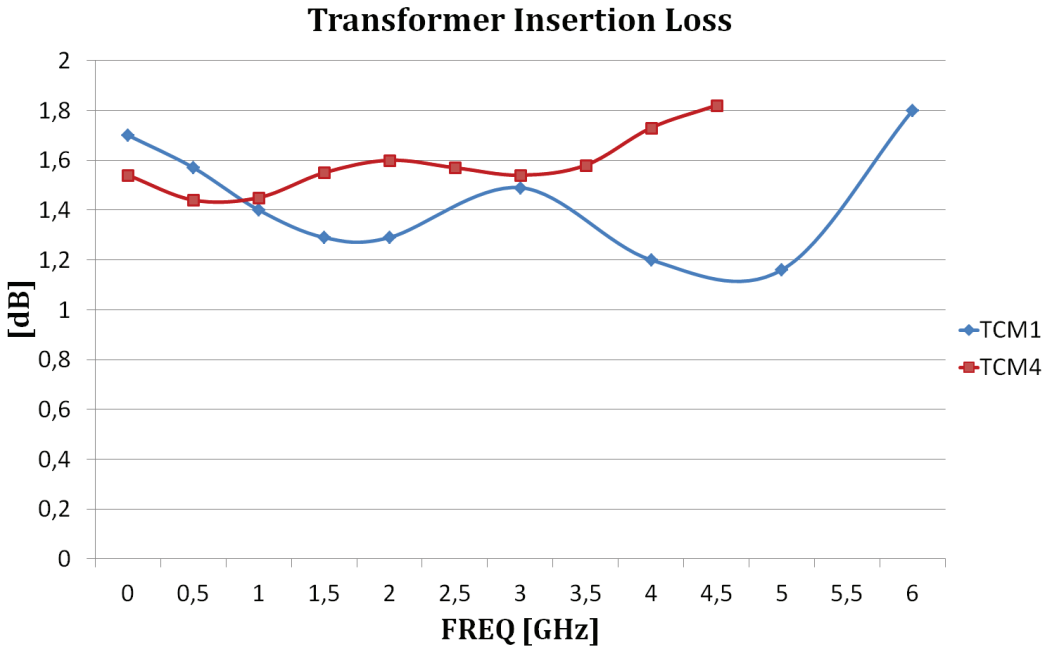

Figure 6.11 : Loss of the transformers used for RF and LO signal paths.

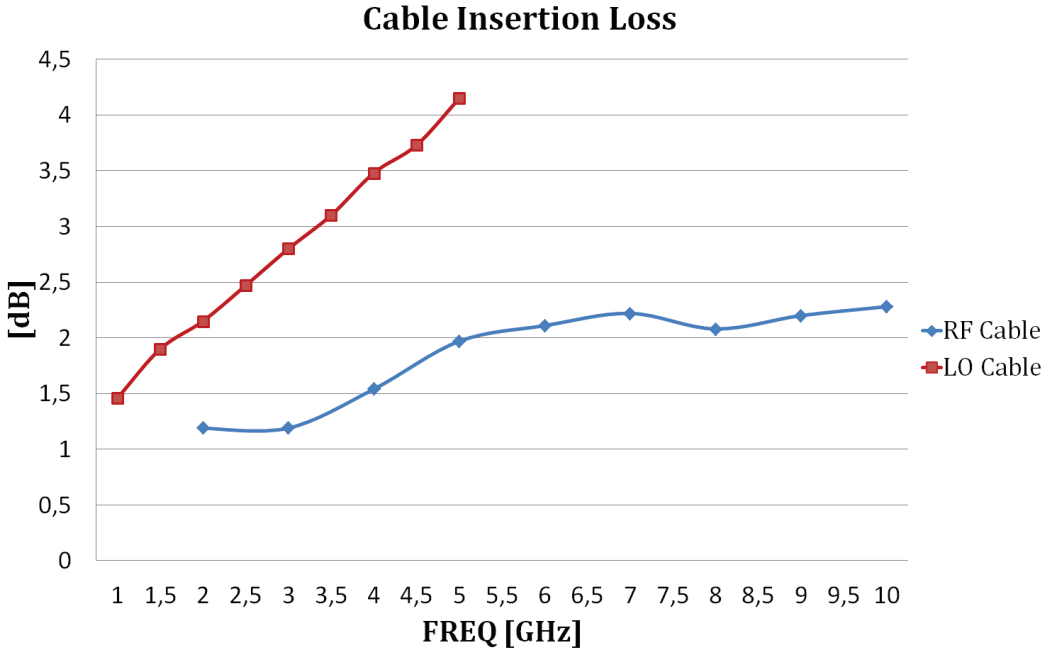

Figure 6.12 : Loss of RF and LO connection cables according to frequency.

from a signal generator and the signal power level at the second harmonic of LO signal is measured at the RF port by a spectrum analyzer.

For the measurements of the second test setup, the power level of the LO signal is set to -4 dBm and the V_B biasing voltage level is set to 1.84 V for which the maximum conversion gain is obtained. While biasing with this optimum biasing voltage, RF port is monitored for the leakage of second harmonic of the LO signal. The minimum

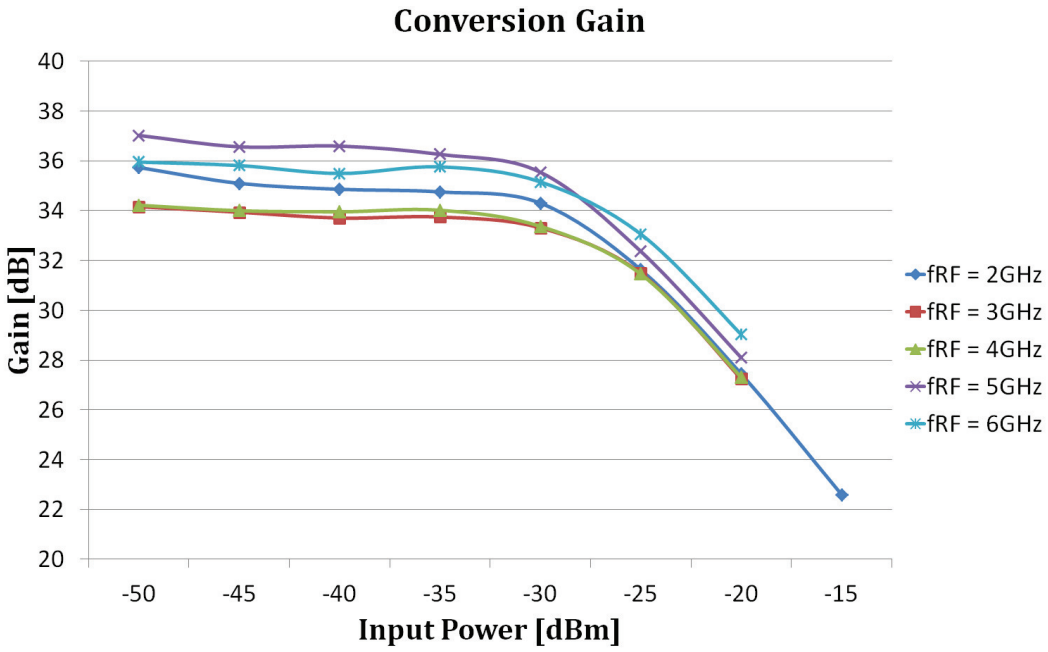

Figure 6.13 : Conversion Gain according to the input RF power at different frequencies when cable and transformer losses are added.

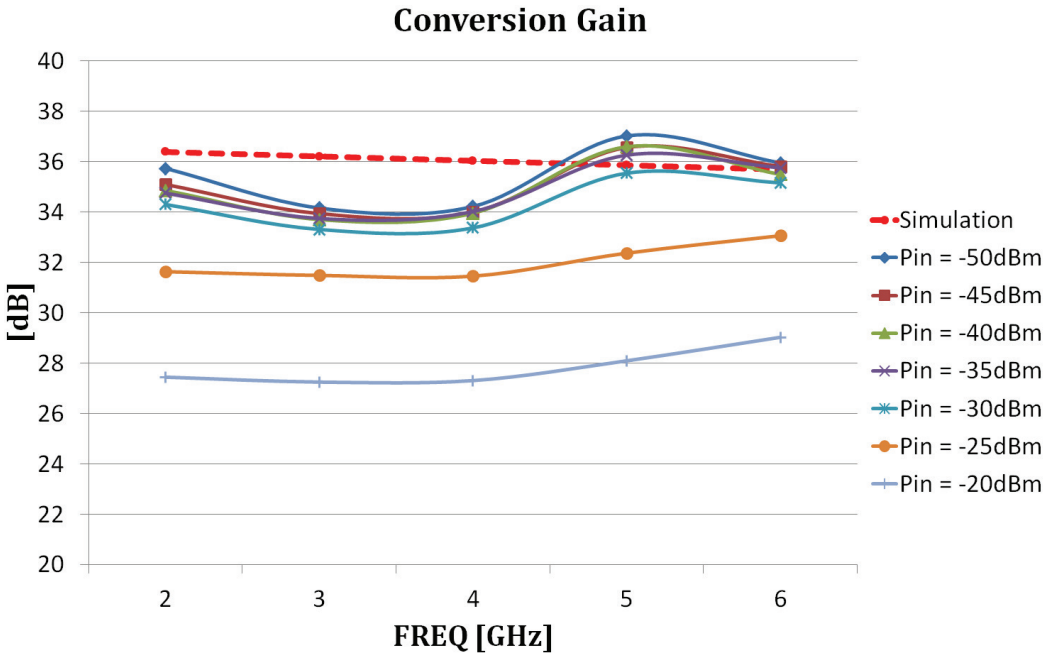

Figure 6.14 : Conversion Gain according to the input frequency when cable and transformer losses are added.

noise floor of the used spectrum analyzer is -70 dBm. According to the measurements with the spectrum analyzer, when the LO signal is applied, no recognizable second harmonic component occurs at the RF port. The obtained measurement results from

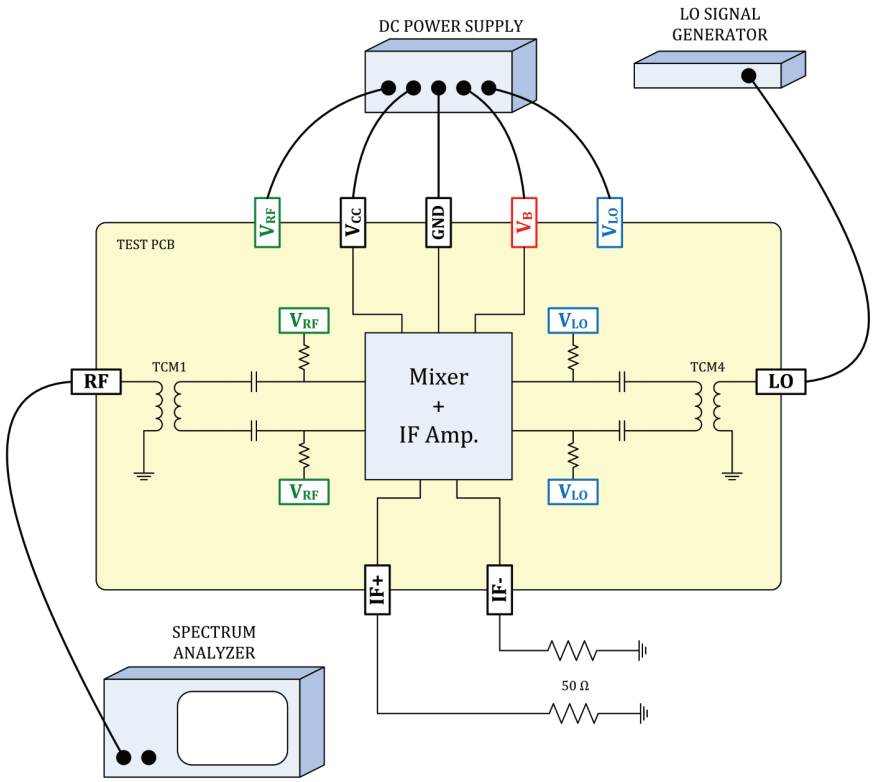

Figure 6.15 : Test setup for measuring the second harmonic component leakage of the LO signal to the RF port of the Mixer + IF Amplifier test structure.

this setup supports the effectiveness of the proposed structure in suppressing the second harmonic component leakage.

6.1.3 Test Setup-3 for the Mixer + IF Amplifier Test Structure

When the both IF outputs are monitored while the circuit is operating in the first test setup given in Section 6.1.1, it is seen that the DC voltage levels of both outputs slightly differ from each other. Observing such a DC offset at IF outputs in spite of the measurement results given in Section 6.1.2, points to a static DC offset voltage originated from component mismatches of either test IC or the PCB. In Figure 6.16, the static DC offset that occurs during the actual operation is seen. Both IF outputs swing around slightly different DC voltage levels.

To distinguish the origin of the DC offset, a third test setup shown in Figure 6.17 is built. In this setup, both RF and LO inputs are terminated with 50 Ω resistances, thus DC offset due to LO self mixing does not occur. Although it is expected to measure the DC offset due to component mismatches with this measurement setup under the actual biasing conditions, as a topological necessity, a different LO voltage level, V_{LO},

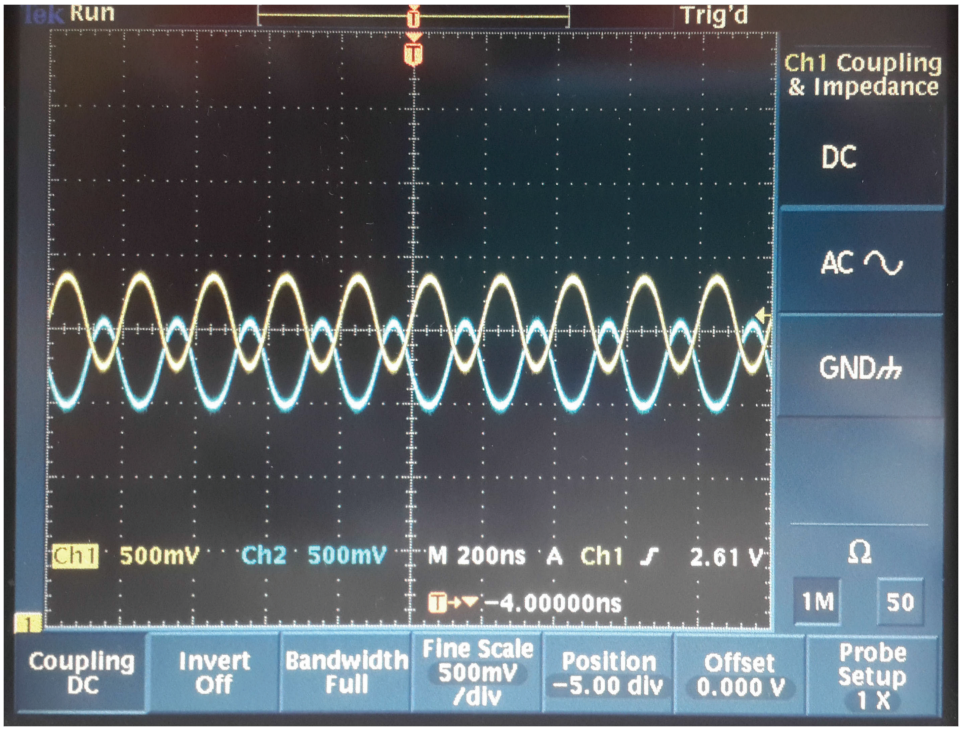

Figure 6.16 : The static DC offset seen at the IF outputs.

should be applied to the proposed mixer in order to acquire a proper measurement. Since the LO voltage level, V_{LO}, is lower than the V_B biasing voltage in the proposed mixer topology which is shown in Figure 3.3, under actual DC biasing conditions when no LO signal is applied, no DC current flows through the primary differential RF stage. Therefore, DC voltage level of the outputs of the mixer reaches the upper rail voltage and the inputs of the following IF amplifier is saturated due to this high input voltage level. As a result, no DC offset voltage can be measured at the outputs of the IF amplifier. In order to measure the static DC offset which is seen during the actual operation, a higher LO DC voltage level, V_{LO}, which is sufficient to steer the same biasing current from the primary differential RF stage, is applied to the mixer circuit. Under these biasing conditions, the actual average biasing current flows through the primary RF differential stage and the IF outputs voltage levels reach to their actual values with the same static DC offset voltage.

To steer the same biasing current, V_{LO} is set to 1.80 V which causes a static DC offset voltage of 360 mV. When the measured static DC offset voltage level is subtracted form the IF outputs, which corresponds to shifting the DC voltage level of one of the IF outputs towards the other, it is seen that both of the IF outputs swing around the

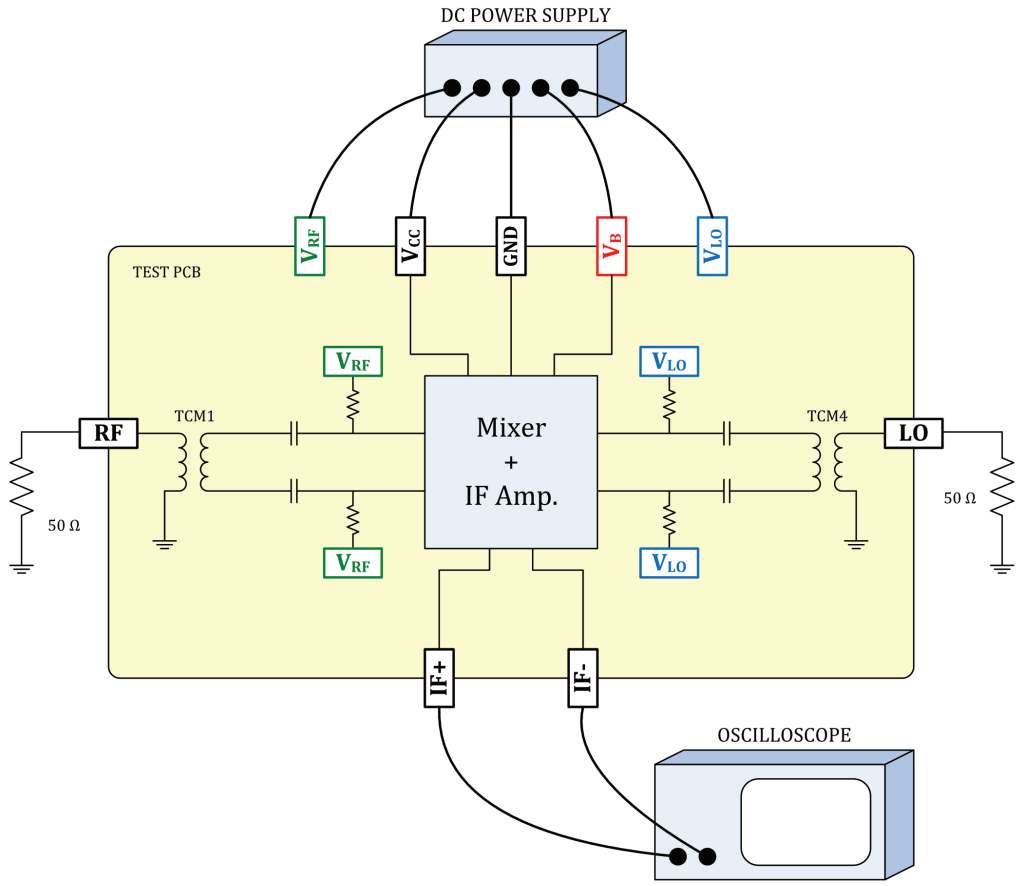

Figure 6.17 : Test setup for measuring the static DC offset due to component mismatches.

same DC voltage level during actual operation. Figure 6.18 shows the outputs from which the measured static DC offset is subtracted.

6.2 Printed Circuit Board for the LNA + Mixer + IF Amplifier Test Structure

The second test PCB is designed to measure the whole receiver circuit designed in the study, consisting of LNA, second harmonic mixer and the IF amplifier. The layout of relevant test structure is shown in Figure 5.7. This target structure for the measurement is placed at the lower left corner of the test chip shown in Figure 6.1.

Since the whole designed circuit is measured with the second PCB, the PCB includes only a transformer to convert single ended LO signal to differential signals, and the required biasing circuitry for the LO inputs. The RF input of the LNA is biased internally, thus, it can be driven directly by a signal generator. All the biasing voltages are supplied externally by DC power supplies of which lines on the PCB include only coupling capacitors.

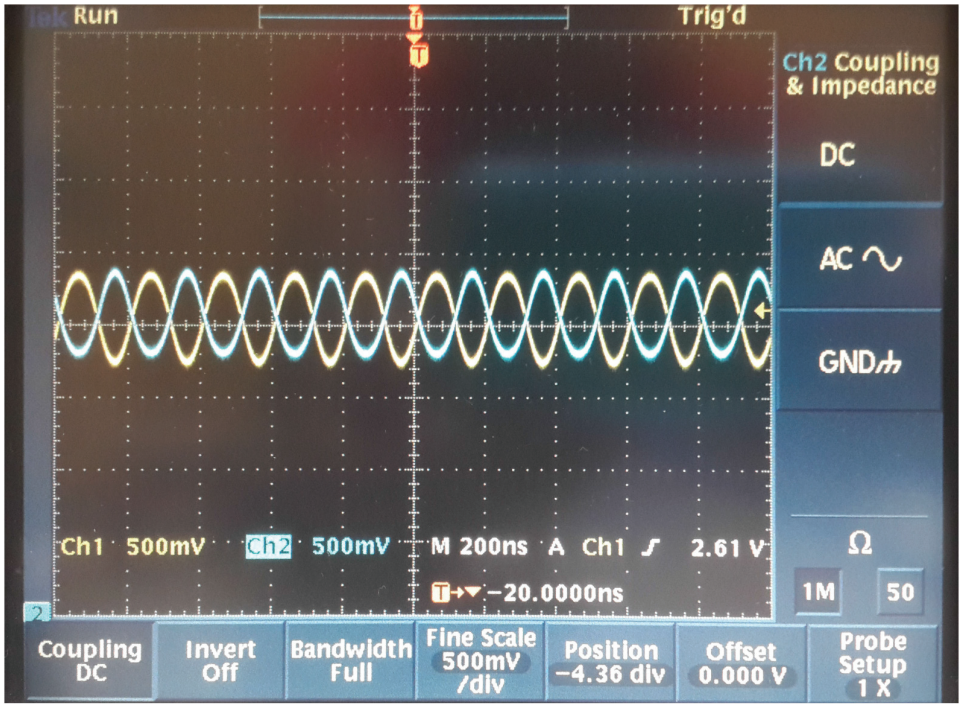

Figure 6.18 : IF outputs from which the measured static DC offset is subtracted.

The selected transformer for the LO signal is TCM4-452X+ which can be used between the frequencies 20 MHz and 4500 MHz. The prepared layout of the second test PCB is shown in Figure 6.19.

6.2.1 Test Setup-1 for the LNA + Mixer + IF Amplifier Test Structure

In this test setup, it is aimed to verify the functionality of the overall designed receiver structure consisting of LNA, mixer and the IF amplifier, and measure the conversion gain upon the built test setup. Separate signal generators are used to supply the RF and LO signals, while the proper DC biasing is satisfied via external power supplies. Built testing setup is illustrated in Figure 6.20. An oscilloscope with 50 Ω inputs is used at the IF outputs to monitor the resultant IF signal.

Figure 6.21 shows the photograph of the prepared second test PCB connected to the testing equipment. The photograph of the actual testing environment, testing equipments along with the PCB, is given in Figure 6.22.

For the measurements, LO inputs DC level is set to 1.75 V respectively as they are used in all the simulations through out the thesis. Two different supply voltages, V_{CC1} and V_{CC2}, are arranged to be 3.3 V and 5 V respectively. The biasing voltage V_B is set

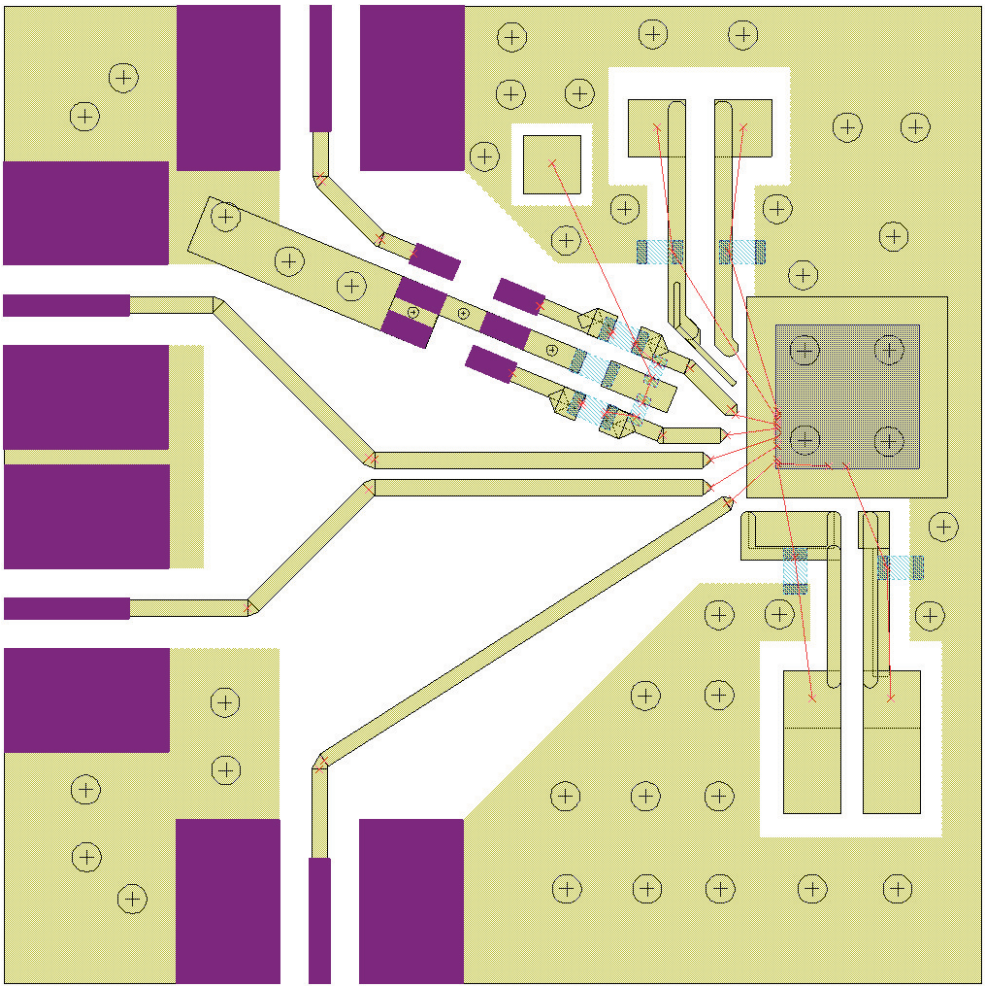

Figure 6.19 : Layout of the second test PCB.

appropriately to obtain the maximum gain. Since the value of the biasing voltage V_B has a considerable impact on the conversion gain, it is also used as a tuning mechanism on the conversion gain of the receiver structure.

For all the measurements performed, the power of the RF signal is kept as -55 dBm, the RF and LO signal frequencies are selected such as to keep the resultant IF signal frequency as 5 MHz. Since the upper frequency limit for the LO transformer is 4500 MHz, RF signal frequency is swept up to 9 GHz for three different values of LO power, P_{LO}, -2 dBm, -4 dBm and -6 dBm. Results of the performed measurements are given in Table 6.6 through Table 6.8. Upon the measurements, peak-to-peak voltage amplitude of the resultant IF signal is measured for different RF frequencies. Then, measured peak-to-peak voltage levels, V_{PP}, are converted into P_{IF} which is the signal power on 50 Ω load resistance in dBm. Therefore, the conversion gain column in the

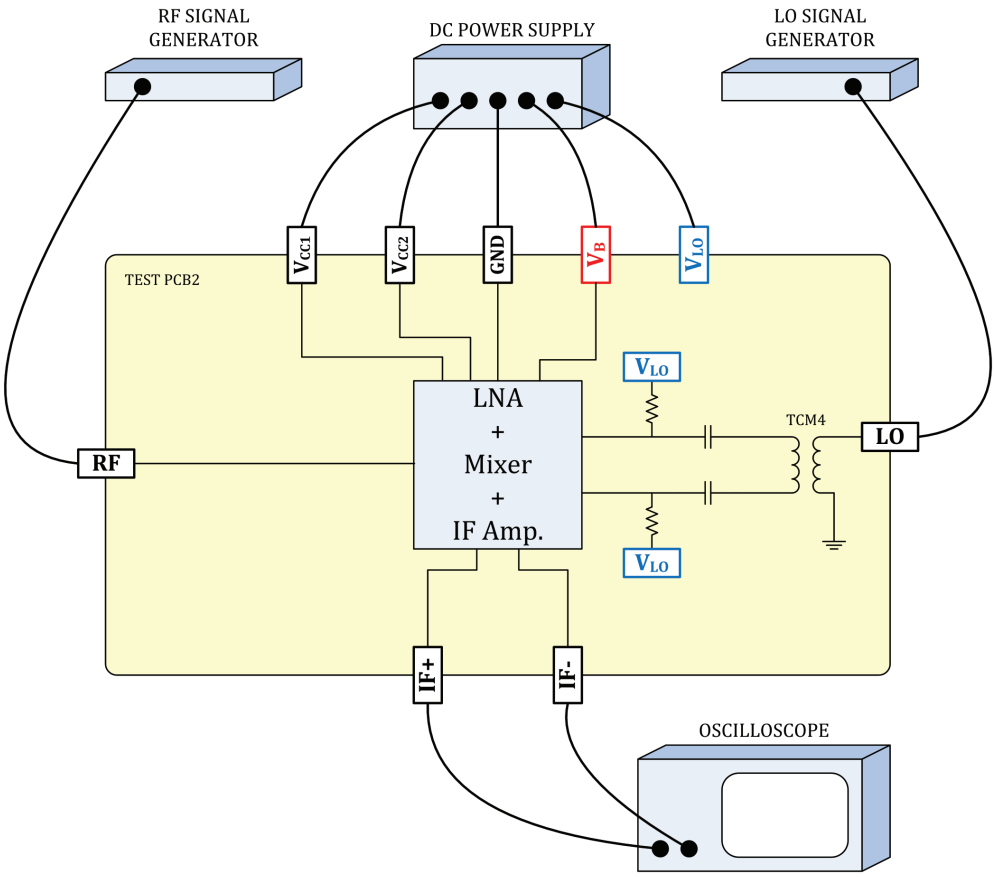

Figure 6.20 : Test setup for the conversion gain measurements of the LNA + Mixer + IF Amplifier test structure.

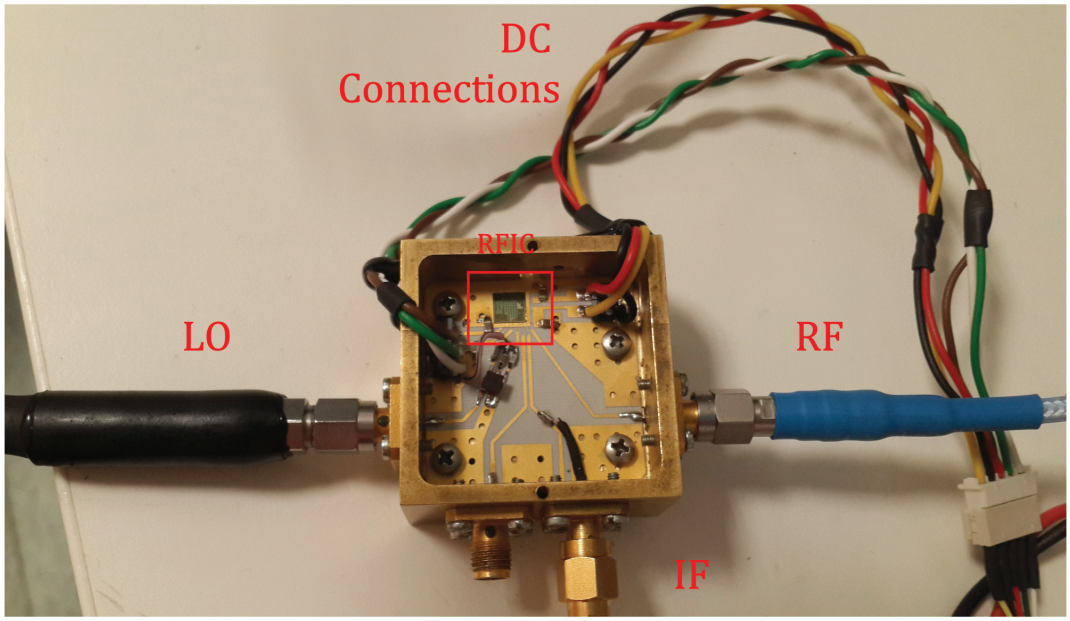

Figure 6.21 : Photograph of the second test PCB.

tables gives the difference between the output power P_{IF} and the input power P_{RF} in dB.

Table 6.6 : IF measurements for $P_{LO} = -2\ dBm$, $P_{RF} = -55\ dBm$.

f_{RF} [GHz]	V_{PP} [mV]	P_{IF} [dBm]	Conversion Gain [dB]
2	890	2.967	57.967
3	940	3.442	58.442
4	790	1.932	56.932
5	885	2.918	57.918
6	340	-5.391	49.609
7	840	2.465	57.465
8	424	-3.473	51.527

Table 6.7 : IF measurements for $P_{LO} = -4\ dBm$, $P_{RF} = -55\ dBm$.

f_{RF} [GHz]	V_{PP} [mV]	P_{IF} [dBm]	Conversion Gain [dB]
2	803	2.074	57.074
3	808	2.128	57.128
4	962	3.643	58.643
5	864	2.710	57.710
6	400	-3.979	51.021
7	872	2.790	57.790
8	548	-1.245	53.755
9	136	-13.350	41.650

Table 6.8 : IF measurements for $P_{LO} = -6\ dBm$, $P_{RF} = -55\ dBm$.

f_{RF} [GHz]	V_{PP} [mV]	P_{IF} [dBm]	Conversion Gain [dB]
2	560	-1.057	53.943
3	824	2.298	57.298
4	760	1.596	56.596
5	725	1.186	56.186
6	490	-2.217	52.783
7	758	1.573	56.573
8	585	-0.677	54.323

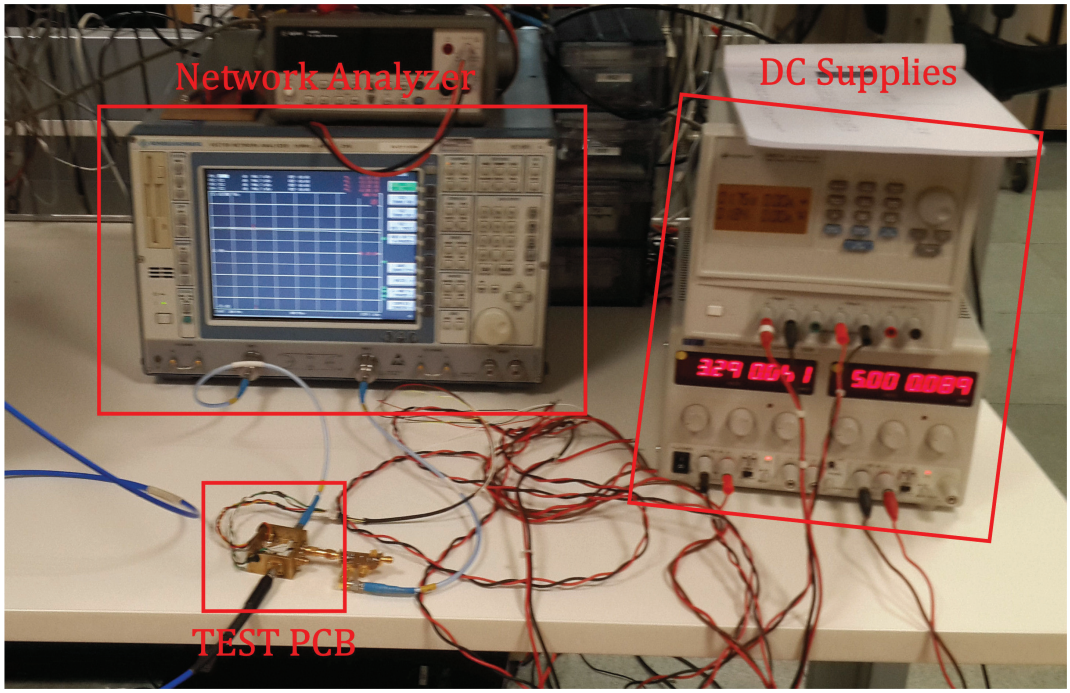

Figure 6.22 : Photograph of the actual testing environment.

In order to visualize the results clearly, measurement results given in Table 6.6 through Table 6.8 are represented as a graphic given in Figure 6.23. When losses due to RF cable is added to the calculated conversion gain values, the graph given in Figure 6.24 is obtained. From Figure 6.24, it is seen that the overall conversion gain of the LNA + Mixer + IF Amplifier test structure is about 59 dB for the RF frequencies up to 5 GHz. Between 5 GHz and 7 GHz, the conversion gain drops to 56 dB and then at about 7 GHz it increases to 59 dB level again. For higher frequencies, the conversion gain decreases sharply above 8 GHz.

The drop of the conversion gain around 6 GHz RF frequency relates to inaccurate impedance matching of the RF input port for these frequencies as it is shown in Section 6.2.2. It is believed that the major effect for the decrease at higher frequencies is the frequency response of the transformer used on the LO path. The upper frequency limit for the used transformer, TCM4, is 4500 MHz which corresponds to 9 GHz RF frequency because of the second harmonic operation. Close to this frequency limit and above, the loss of the transformer increases dramatically thus decreases the overall conversion gain. Therefore, the measurement for the conversion gain is performed upto 9 GHz RF frequency.

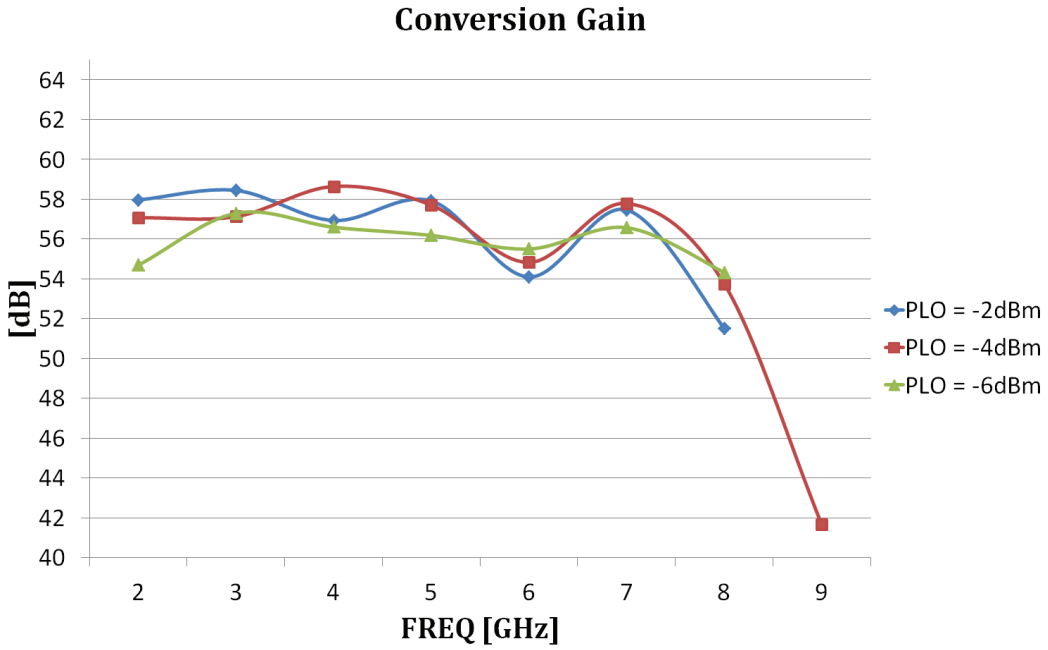

Figure 6.23 : Conversion gain according to RF frequency.

When compared to conversion gain graph obtained from the simulation results given in Figure 4.32, except the decreased regions at around 6 GHz and frequencies higher than 8 GHz, the measured conversion gain graph is close to the simulation results. The simulation results graphs is also plotted together with the measurements results in Figure 6.24 to show the accordance. The simulation result graph changes around 61 dB within a $\pm 1.5\ dB$ range and the measured average conversion gain is about 59 dB.

6.2.2 Test Setup-2 for the LNA + Mixer + IF Amplifier Test Structure

Prepared second test setup for the LNA + Mixer + IF Amplifier test structure is shown in Figure 6.25. Here, all input and output ports of the second PCB is terminated with 50 Ω resistances except the RF port. RF port is connected to a network analyzer. Via the network analyzer, the input matching of the receiver is examined by S11 measurement.

The result of the S11 measurement of the RF port is given in Figure 6.26. Figure 6.26 shows that the S11 of the RF port is below -10 dB between 2 GHz and 5 GHz and around 7 GHz, while it increases up to -5 dB level between 5 GHz and 7 GHz and above 8 GHz. The simulation result for the S11 of the RF port, which is originally given in Figure 4.1, is also plotted in order to compare with the measurement results.

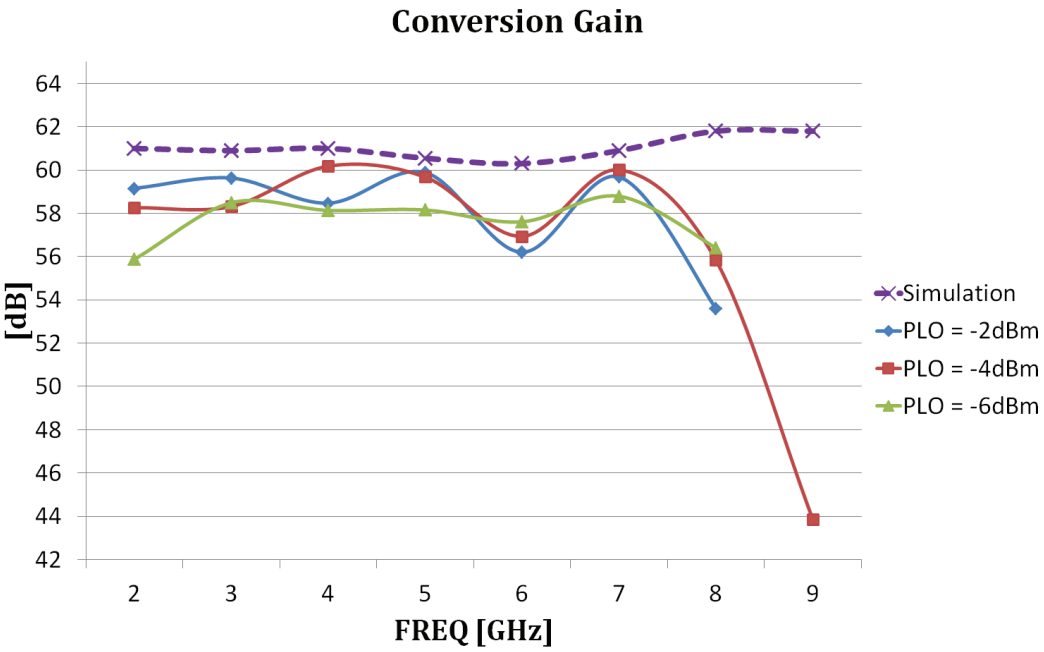

Figure 6.24 : Conversion gain according to RF frequency without the RF cable losses.

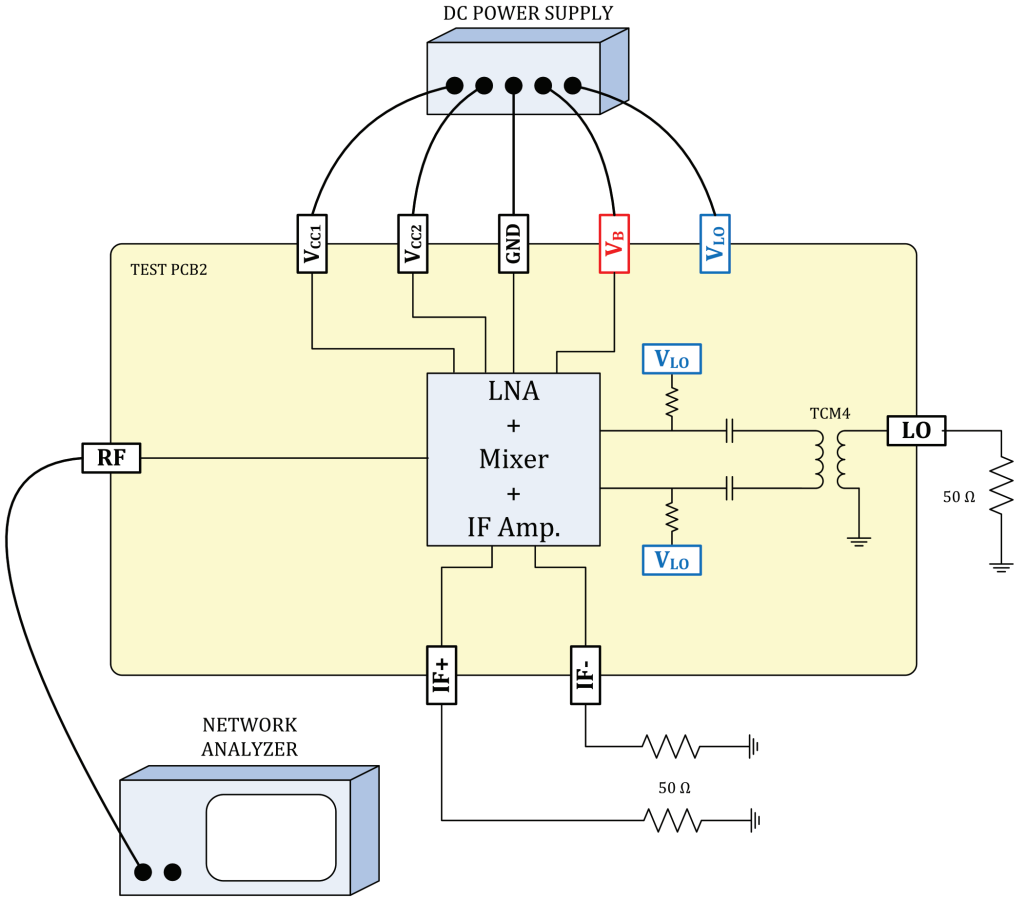

Figure 6.25 : Test setup for the measurement of S11.

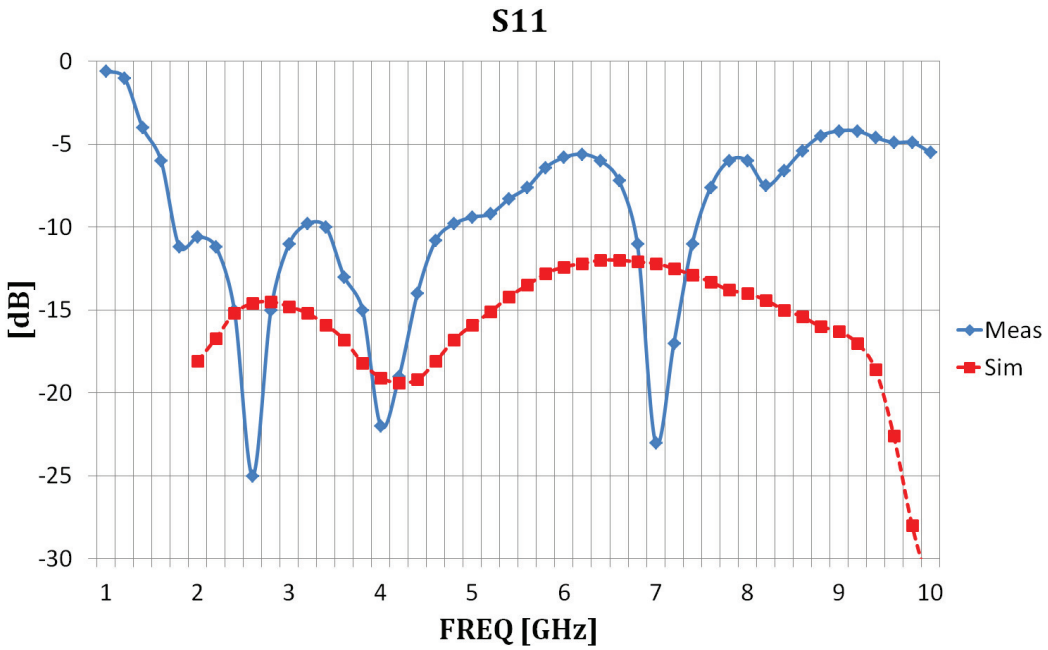

Figure 6.26 : Measurement and simulation results for S11.

It is seen that the actual measurement results does not show strong correlation with the simulation results.

It is concluded that the inaccuracy in the input impedance matching between 5 GHz and 7 GHz correlates with the conversion gain results given in Figure 6.24. The overall conversion gain given in this graphs drops where S11 increases.

7. CONCLUSION

In this study, it is targeted to propose a compact and fully integrated transceiver architecture for the use of rapidly developing wireless communication systems. For this purpose, transceiver topologies are investigated and their advantages and disadvantages are considered. Upon a literature review about the topic, the Homodyne, namely the Zero-IF transceiver architecture is selected to realize the best embodiment for a simple and integrated receiver solution. Yet, the selected architecture brings serious problems besides that researchers prefer to stay away in most applications. The evaluation of the transceiver architectures are summarized in Chapter 2.

A Zero-IF receiver topology is proposed in the study. To overcome the serious problems of the Zero-IF architecture, second harmonic mixing technique is utilized. Since the LO frequency is the half of the carrier frequency in second harmonic mixing technique, a fundamental solution to the most of the problems of Zero-IF receivers which arise from the equality of the LO and the carrier frequency is provided naturally.

For the realization of the proposed receiver topology, SiGe BiCMOS semiconductor processing technology is selected. Providing the proper devices as high speed HBTs, high quality passive components and CMOS transistors together, the SiGe technology is a rising technology especially for RFIC applications. By utilizing such a technology, it is aimed to obtain an integrated receiver solution with an easily accessible and low cost technology.

An LNA, a second harmonic mixer and an IF amplifier are designed as the building blocks of the Zero-IF receiver. A fully differential structure is built through out the topology. The overall topology is designed to operate within an RF frequency range of 2-10 GHz. The LNA circuit is converting the single ended RF signal to differential signal and driving the second harmonic mixer circuit directly. The fully differential second harmonic mixer circuit is followed by a differential IF amplifier.

A new second harmonically pumped mixer topology is proposed for the Zero-IF receiver topology. The circuit analysis of the topology is performed and equations regarding the generation of the pumping current and the conversion gain of the mixer is derived from the analysis. Proper biasing conditions for the efficient second harmonic mixing is determined. The effects of the biasing conditions on the performance of the mixer is investigated. The new second harmonic Zero-IF mixer topology provides an adequate mechanism to suppress the DC offset voltage at the output of the mixer. The proposed mixer operates with a constant total DC current. The total DC current is split into two, locally, to produce the pumping current which contains the second harmonic of the LO frequency component. After performing the second harmonic mixing operation, the pumping current reunites with the residue current to form again the total DC biasing current. This unique mechanism of drawing constant current from the supply and ground lines provides an isolation between the noisy mixer circuit and the rest of the integrated circuit. Thus, the propagation of the second harmonic of the LO signal to the RF signal path is prevented. The leakage from the locally generated pumping current to the RF inputs of the mixer is also prevented by replicating the RF input stage of the mixer and biasing it with the residue current, which is the remaining part of the total DC current from the pumping current. Since the residue current contains the same frequency components with opposite amplitude signs with the pumping current, for all the frequency components leaking of pumping current to the RF inputs, an oppositely signed leakage is supplied by the replica input stage. Thus, the local leakage of the second harmonic of the LO frequency to the RF inputs of the mixer is also suppressed by the mixer topology. The detailed analysis results regarding the harmonic components of the pumping and the residue currents are given in Chapter 3.

The schematics of the building blocks are built separately within the design environment and various simulations are performed. According to the simulation results, the LNA has a gain of 22 dB within the RF range. The gain of the LNA changes only ± 1 dB. The S11 of the LNA obtained from the S-parameter simulation is below -12 dB for the whole RF range. For the investigation of the dynamic range of the LNA, the input signal power is swept. The 1 dB compression point for the output (O1dB) is found as -7.6 dBm while the input 1 dB compression point (I1dB)

is -28.35 dBm. The noise figure of the LNA circuit is below 3.8 dB for the whole RF range.

The simulations of the proposed second harmonic mixer topology is performed not only to exhibit the performance of the circuit but also to verify the analysis results. By using the same biasing conditions with the analysis, the similar graphics regarding the operations of the circuit are obtained. The generated pumping and residue currents and their harmonic components are shown. It is seen that the expected results are also obtained from the simulations results. It is verified that the analysis and the simulations results are in agreement. According to the simulation results, the mixer has a conversion voltage gain of about 20 dB and it changes only 1.3 dB within the RF frequency range.

When the IF amplifier circuit is simulated alone, it is seen that it has a voltage gain of 19.5 dB wiht a 3 dB cutoff frequency of 370 MHz. The phase margin of the IF amplifier is 87 degrees. From the noise figure simulation, it is seen that the Flicker noise effect at the output lasts up to 1 MHz and then the noise figure of the IF amplifier is tied up to 12.4 dB. Another simulation is performed on the IF amplifier by sweeping the input power range. It is observed that the output power saturates 1 dB for an input power of -13.5 dBm and the O1dB is 3.1 dBm.

When the second harmonic mixer circuit is simulated with the IF amplifier and the first order passive low pass filter in between them, the O1dB of the combined structure becomes 5.9 dBm and I1dB becomes -25.6 dBm. Due to the first order passive low pass filter used between the mixer and the IF amplifier, the IF bandwidth of the combined structure is obtained as 10 MHz. The output frequency spectrum of the combined structure show that the circuit performs outstanding DC voltage suppression. This verifies the effectiveness of the proposed topology.

The simulations of the total receiver topology is performed and a conversion gain of 61 dB is obtained with a change of $\pm$1.5 dB within the RF frequency range. From the output frequency spectrum of the receiver, it is observed that the fundamental mixing product is suppressed and the IF signal regarding the mixing with the second harmonic of the LO signal exist in the baseband. The overall O1dB is obtained as 3.1 dBm and I1dB is -57 dBm.

The Zero-IF receiver topology of which building blocks are designed and simulated is realized with the 0.18 μm SiGe BiCMOS technology. Several layouts for both the overall receiver circuit and the building blocks of the receiver separately are prepared and placed on a 5 mm $\times$ 5 mm MPW die. Two separate PCBs are prepared for two test structures; "Mixer + IF Amplifier" and "LNA + Mixer + IF Amplifier". Selected test structures are directly bonded to the PCBs and several test setups are prepared for measurements.

By measuring "Mixer + IF Amplifier" test structure, it is aimed to verify the analysis results and the effectiveness of the proposed second harmonic mixer topology in which the main contribution is made. Measurements are performed upto 6 GHz which is the limit for the selected transformers on the RF and LO signal paths.

First, the conversion gain of the test structure is measured by arranging the IF frequency as 5 MHz for different input signal powers. According to measurements, the test structure performs 35 dB of conversion gain which is close to the simulation result, 36 dB. I1dB of the structure is about -28 dBm, which is found as -25.6 dBm according to simulations. The leakage of the second harmonic of the LO signal to RF input port is also measured since the it gives the merit for the DC offset due to LO self mixing. A spectrum analyzer with -70 dBm noise floor is used yet no leakage at the second harmonic frequency of the LO signal is detected at the RF port. This isolation performance shows the effectiveness of the proposed topology in suppressing the DC offset due to LO self mixing. By measuring the output DC offset when no RF and LO signals are applied, it is shown that the static DC offset between two IF outputs of the topology is originated from the component mismatches. The measured results for the proposed mixer is compared with other subharmonic mixer embodiments given in the reference in Table 7.1.

The overall receiver circuit, "LNA + Mixer + IF Amplifier" test structure, is also measured on a separate PCB. Conversion gain graphs for the receiver is plotted upto 9 GHz and compared with simulation results. An average of 59 dB conversion gain is measured where the conversion gain according to the simulation results is about 61 dB.

The proposed second harmonic mixer which is utilizing a unique method to suppress the second harmonic leakage of LO to RF path is manufactured and the theory

Table 7.1 : Comparison of the proposed mixer with the subharmonic mixers given in references.

Ref.	CG	2LO-RF	NF	I1dB	RF Freq.
[20]	9.5	48	NA	-20	5
[23]	10.2	68	13	-2	2.1
[30]	15.18	NA	16.33	-16.3	2.4
[32]	17.2	75.6	9.8	NA	2
[34]	25	NA	6.8	NA	5
[35]	3.2	>60	10	-12.7	24
[36]	12.5	>75	7.4	-17.5	24
[37]	8.01	NA	5.96	-12	5.6
[38]	13.71	NA	11.98	-15	2.4
[41]	11.61	NA	12	NA	2
[42]	9.3	>35	NA	-15.7	5.25
[43]	19	38	NA	-19.5	2.4
This Work	35	>70	14	-28	2-10

is verified upon simulations and relevant measurements. A paper presenting the proposed mixer topology is prepared for the Istanbul University Journal of Electrical and Electronics Engineering with the title "Zero-IF Second Harmonic SiGe Mixer with DC Offset Cancellation".

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