ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

LAYOUT TECHNIQUES FOR ANALOG BUILDING BLOCKS AND APPLICATION TO AN ADAPTIVE OUTPUT BUCK CONVERTER

M.Sc. THESIS

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Faik Mevlut DURMAZ, a M.Sc. student of ITU Graduate School of Science Engineering and Technology 504111244 successfully defended the thesis entitled **"Layout Technıques For Analog Building Blocks And Applıcation To An Adaptive Output Buck Converter"**, which he/she prepared after fulfilling the requiremnts specified in the associated legistlations, before the jury whose signatures are below.

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To my wife, family and friends

FOREWORD

This thesis cannot be finished without endless support and encouragement of my beloved wife, Gizem. She endured all my misery and gave hope at all times.

My family, mother, grandmother and grandfather, I thank you all. You made me what I am now.

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May 2016 Faik Mevlut DURMAZ

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ABBREVIATIONS

IC	**:** Integrated Circuit
CMOS	**:** Complementary Metal Oxide Semiconductor
CAD	**:** Computer Aided Design
PMOS	**:** P channel Metal Oxide Semiconductor
NMOS	**:** N channel Metal Oxide Semiconductor
MOSFET	**:** Metal Oxide Semiconductor Field Effect Transistor
MIMCAP	**:** Metal-Insulator-Metal Capacitor
MOSCAP	**:** Metal Oxide Semiconductor Capacitor
MOMCAP	**:** Metal On Metal Capacitor
STI	**:** Shallow Trench Isolation
LOCOS	**:** Local Oxidization of Silicon
TOX	**:** Thick Oxide
FOX	**:** Field Oxide
R3D	**:** Resistive 3-Dimensional Extraction
RDL	**:** Re-Distribution Layer
CBM	**:** Capacitor Bottom Metal
CTM	**:** Capacitor Top Metal
RCX	**:** Resistive Capacitive Extraction
SOI	**:** Silicon on Insulator
RHBD	**:** Radiation Hardened by Design
ELT	**:** Enclosed Layout Transistor

LIST OF SYMBOLS

$\bar{J}$	**:** Current Density
E	: Electric field
ρ	: Resistivity of material (Ωm)
σ	: Conductivity (S/m)
μ	: Micron, 10^{-6} meter
Ω	: Ohm
V	: Voltage
I	: Current
l	: length
w	: width
h	: height
$\mathbf{t_{ox}}$	: gate oxide thickness
$\mathbf{C_{ox}}$	: oxide capacitance
$\mathbf{V_T}$	: threshold voltage
$\mathbf{V_{BG}}$	: Bulk-gate voltage
D	: Drain
S	: Source
B	: Bulk
G	: Gate

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ANALOG LAYOUT TECHNIQUES AND APPLICATION TO AN ADAPTIVE OUTPUT BUCK CONVERTER

SUMMARY

Integrated circuits (ICs) have become an essential part of our daily lives. Different kind of chips called Application Specific Standart Product (ASSP) is being used in specific part of a system. Chip creation contains analog, digital and layout designs. Each design step is important to succesfully fabricate desired chips.

There is a need for power management circuitry in ICs, in order to power each and every device. Today's trend of mobile technology increases the need of power management. LDOs, DC-DC converter or buck converter and buck-boost converters must be utilized. Inside ICs, power management circuit design is an active research area and there are many publications in the literature about this topic. This thesis focuses on basic layout, layout strategies and layout of buck converter.

This thesis is organized as follow. In chapter 1, the fabrication process of. MOSFET devices are explained. Then basic layout structures are described in detail, starting from CMOS layout structures to diode, BJT layout and layout of passive components. Isolation structures are explained in chapter 4. These isolations are both contain process related isolation and layout design isolations. Issues coming from layout are given in detail in chapter 5 which affects block performance significantly. Layout matching is explained and demonstrated in chapter 6. These layout structures and strategies are very important in layout design.

In chapter 7, analog blocks of adaptive output buck converter is explained in detail. The layout designs are analysed in detail to show what kind of layout structure is used. Most important part of buck converter is the pass device which is explained in detail with layouts. Resistive extraction tool is used to extract metallization resistance for spotting the weak parts in pass device metal structure. Moreover, this tool gives the total on resistance of pass device which can be given feedback to analog designer to modify their buck converter simulations.

Total laid out pass device area is 800µ x 650µ while total buck converter design occupies 800µ x 940µ. Buck converter is designed in a 0.25µ process with 1 poly 5 metal process.

ANALOG SERIM TEKNIKLERI VE UYARLANABILEN CIKIS ALCALTICI DÖNÜŞTÜRÜCÜYE UYGULANMASI

ÖZET

Otuz yılda teknolojinin gelişmesi ile hayatımız değişmiş, teknoloji büyük yer kaplamaya başlamıştır. Bunun arkasında tümdevre tasarımı ve üretimi önemli bir yer kaplamaktadır. On sekiz ayda bir tümdevrenin boyunun yarıya inmesi veya işlem gücünün iki katına çıkması mottosu gelişimi hızlıandırmıştır. Tümdevrelerin temel yapı taşı olan yongalar bu harekete ayak uydurma adına giderek küçülmekte veya bir yonganın tek başına gerçekleştirdiği işlem yapabilme kabiliyeti artmaktadır. Yonga tasarımı temelinde analog tasarım, sayısal tasarım ve serim içermektedir. Bunlar ayrı ayrı gibi gözüksede bir yonga içinde bunları barındarmaktadır.

Analog tasarım ve sayısal tasarım bilgisayar destekli tasarım programları ile simülasyonları yapılmakta ve yapılan tasarım doğrulanmaktadır. Daha sonra bu tasarımların yonga içerisinde yerleştirilmesi, farklı amaç için tasarlanmış devreler daha sonra birbirleri ile gerekli bağlantıların yapılması suretiyle, uygulamanın ihtiyaç duyduğu belli bir amaca sahip yonga üretilmektedir. Devrelerin, transistörlerin ve diğer yapıların yerleştirilmesi, birbirleri ile gerekli bağlantılarının yapılması noktasında serim denmektedir. Analog ve sayısal tasarımlarda kullanılan transistor boyutu küçüldükçe tasarlanan devrelerde yaşanabilecek sorunlar artmaktadır. Özellikle kullanılan transistör, direnç ve kapasitörlerin boyutu küçüldükçe üretiminde kaynaklanabilecek ve serim aşamasında sorun yaratma durumları artmaktadır.

Günümüzde eğilim teknolojik ürünlerin düşük çalışma enerji özellikleri ile batarya ömrünün uzun olması yönündedir. Bunun olmasını sağlayan unsurlardan biri yongaların düşük enerji tüketmesi için ihtiyaç duydugu gerilim ve akım değerlerinin azaltılması, diğer unsur ise bataryaların teknolojisi geliştirilip aynı boyutlarda daha yüksek enerji depolanmasıdır. Yongaların ihtiyaç duyduğu düşük gerilim değerlerini bataryanın sağladığı gerilim değeri ile sağlamak mümkün değildir. Çünkü bataryanın enerjisi azaldıkça, sağladığı gerilim değeri ihtiyaç duyulan sabit gerilim sağlayamamaktadır.

Bu nedenle güç yönetimi yongaları kullanılmaktadır. İçinde bulundurduğu elemanlar ile bataryadan aldığı gerilim ve akım değerlerini düzenleyip, sistemde bulunan her yonganın ihtiyaç duyduğu, her yongaya özel gerilim ve akım değerlerini sağlayarak sisteme iletmektedir.

Güç yönetimi yongası içinde kullanılan en önemli elemalardan biri çıkış alçaltıcı dönüştürücü elemanıdır. Bu elemanın amacı, bataryadan gelen değişken gerilim değerini, gerekli gerilim ve akım değerine regüle ederek ve bunu yaparkan verimlilik yani enerji kaybını en az seviyede tutarak yapan elemandır. Günümüzde çıkış alçaltıcı dönüştürücü elemanlarının verimlilik değeri %95 ler civarındadır. Bu sayede gerilim ve akım regüle edilirken enerji seviyesi en az seviyede tutulmaktadır.

Tezin amacı, çıkış alçaltıcı dönüştürücü elemanına serim teknikleri bakımından incelenmesi ve uygulanınca daha iyi sonuçlar veren serim teknik ve özelliklerine odaklanmıştır.

Tezin giriş kısmından sonra ikinci bölümünde transistörün üretim aşamaları anlatılmıştır. Daha sonra endüstride yaygın olarak kullanılan N katkılı transistör ve P katkılı transistörlerin birlikte kullanıldıgı birbirini tamamlayan metal oksit yarı-iletken üretim teknolojisi detaylı bir şekilde anlatılmıştır.

Üçüncü bölümde en temel serim yapıları aktarılmıştır. N katkılı transistor, P katkılı transistörlerin serim yapıları ve özellikleri gösterilmiştir. Sonrasında diyot yapısının serimi anlatıldı, çift kutuplu transistör yapısı gösterildi. Tasarlanan yongalarda kullanılan direnç yapısı ve direnç çeşitleri aktarıldı. Aynı şekilde kullanılan kapasite çeşitleri, birbirlerine göre üstünlükleri şekiller yardımıyla detaylı bir şekilde anlatıldı. Transistörleri, yarı-iletken olmayan elemanları ve devrelerin bağlanması için kullanılan metallerin kullanım sonucu aşınarak düşük dirençli olması istenirken, iç direncinin artmasi durumu anlatıldı. Fiziksel etkilerin buna neden olması durumları açıklanmistir.

Tasarlanan devrelerin tasarlanma durumlarına göre yüksek gürültülü olma durumunun izolasyon teknikleri ile nasıl birbirlerin ayrılabileceği detaylı bir şekilde açıklandı. Bu izolasyon yapıları üretimde özel teknikler ile sağlanabildiği yapılar ile serim aşamasında uygulanabilecek izolasyon stratejileri anlatılmistir.

Beşinci bölümde serimden kaynaklanabilecek sorunlar detaylı bir şekilde açıklandı. Doğru yaklaşım yapılmamış bir serimin bütün yongayı ve dolayısıyla tümdevreyi yakma durumu anlatıldı. Sorunlarında bir diğeri N katkılı transistörlerin ve P katkılı transistörlerin birbirlerine fazla yakın yerleştirmesi sonucu iki yapınında analog tasarımda yapılan simülasyondaki modelinden çok daha farklı davranma durumu anlatıldı. Bu olası sorunların serim aşamasında nasıl dikkate alınması gerektiği, analizinin nasıl ve hangi temelle yapılması gerektiği dolayısıyla bu sorunların çözümleri gösterilmistir.

Devre tasarımında yapılan simülasyon ile serimde yongaya konan transistörlerin aynı gerilim, akım davranışlarının sergilememesi durumu anlatıldı. Bunu nedenleri detaylı bir şekilde verildi. Çözüm olarak farklı serim teknikleri ve bunların avantajları, serime dolayısıyla devreye etkileri açıklandı. En önemli etmenin birbirleri ile belirli bir hassaslık derecesine sahip olması gereken tasarımlarım serim teknikleri, yerleştirme stratejisi, serimde birim eleman kullanmanın yarattığı iyileştirme, serimde transistörlerin kenarlarına konulan fazla transistörlerin birbirleriyle hassaslık gerektiren tranistör yapılarında yarattığı iyileştirme etkileri detaylı ve açıklayıcı bir şekilde anlatıldı. Metal bağlantılarda uygulanabilecek simetrinin avantajları gösterildi. Transistörlerin simetrik yerleştirilme şekilleri ve bu yerleştirme çeşitlerinin birbirlerine göre üstünlükleri anlatılmistir.

Yedinci bölümde, önceki bölümlerde anlatılan tüm yapıların, stratejilerin, göz önüne alınması gerekn durumların hepsi dikkate alınarak ve alçaltıcı dönüştürücü yonga tasarımında uygulanması detaylı bir şekilde anlatıldı. Alçaltıcı dönüştürücü tasarımının sahip oldugu alt analog devrelerin seriminin yapılış figürlerle ve açıklayıcı anlatımla aktarılmıştır.

Alçaltıcı dönüştürücünün en önemli yapı elemanı olan ve alçaltıcı dönüştürücünün mantığı olan yüksek akım sağlamayı sağlayan bu devre, serimi ve üzerine gerekli metallerin konmasından sonra yapılan 3 boyutlu direnç çıkarımı ve analizi yapan program ile analiz yapıldı. Bu programın görsel avantajı resimlerle detaylı bir şekilde aktarıldı. Bu programın transistör modeli arassındaki yaklaşım farkı örneklerle gösterildi. Alçaltıcı dönüştürücü üzerinde geçen yüksek akımın davranış özellikleri de anlatılmistir.

Son olarak serimi yapılmış alçaltıcı dönüştücü resimlerle gösterildi, yonga içerisinde kapladığı alan hesaplandı ve kullanılan transistörün yapıiçi direnci üzerine eklenen metallerin yarattıgı fazladan direnç değeri 3 boyutlu direnç çıkarım programı sayesinde bulunarak alçaltıcı dönüştürücünün üretildiğinde sahip olacağı toplam direnç bulundu. Tezin daha ileriye götürülebilmesi adına yapılabilecek adımlar hakkında bilgi verilmiştir.

1. INTRODUCTION

Layout design is a part of chip design and production. It sits between circuit design phase and produced/real world chip architecture. Circuit design contains analog and digital design. All together builds a system and addition of mixed-signal creates chip required in real life. Circuit design is drawings of transistor-level or gate-level design of transistors. This is not real world representation of a chip. Thus, layout design is the physical representation of the circuit.

CMOS ICs are made using an extremely complicated process that in the end results in tiny transistors and metal wires being constructed and connected on a silicon substrate. Layout design is the art of drawing these transistors and wires as they look like in silicon.

The CMOS circuit design process consists of defining circuit inputs and outputs, hand calculations, circuit simulations, circuit layout, simulations including parasitics, reevaluation of circuit inputs and outputs, fabrication, and testing.

The task of laying out the IC is often given to a layout designer. Parasitics are the stray capacitances, parasitic resistances of wiring the nets, PN junctions, and bipolar transistors which cause latch-ups. Layouts of all these devices are explained in this thesis [1].

Power management IC are one of today's important and necessary part of technological devices because trend is being more mobile. Inside power management chips, buck converter occupies a large and important function. The thesis focused on layout basics, advanced layout strategies and layout of a buck converter.

1.1 Organisation of Thesis

Thesis is organized and summarized as below:

Chapter 2 covers production flow of a chip and explaines how a transistor is fabricated. Process steps are briefly covered.

In Chapter3, basic layout structures are given. Layouts of CMOS, diode, BJT and passive devices are explained with cross-sections of related devices.

Chapter 4 covers isolation schemes regarding layout. Isolation can be maintained in fabrication step and layout structures when designing layout. Various types of isolation strategies are explained in detail.

In Chapter 5 issues relating layout design are explained. These problem might cause serious functionality problem of chip. How these issues emerge and how to prevent or minimize them are given.

Chapter 6 dives into layout design. Most important type of layout design is matching between devices. This chapter explaines how matching can be done from basic to advance styles.

In Chapter 7 analog blocks of buck converter are explained briefly and layouts of these blocks given in detail with applies layout strategies explained in previous chapters.

Chapter 8 explains a specific tool used to analyse metallization of buck converter in detail.

Finally, Chapter 9 summaries the overall work done in this thesis and suggests future works to improve more.

1.2 The Purpose of Thesis

The aim of this thesis is to create an idea of what “layout” is, why it is needed and how to do as correct and best as possible. This includes basic principles of production flow which produces IC. Production limitations, unwanted side-effects of process, offsets which can be systematic or random will all be covered and solutions to minimize or get rid of these effects will be explained. At the end, techniques to solve these issues will lead to a proper and advanced layout knowledge.

2. MANUFACTURING OF A MOSFET

2.1 Fabrication

CMOS integrated circuits are fabricated on thin circular slices of silicon called wafers. Each wafer contains hundreds or even thousands of individual chips or "die" (Fig. 1.1). For production purposes, each die on a wafer is usually identical. Wafer sizes also differ from 150mm – 300mm. The most common wafer size (diameter) in production is 300mm (12 inch) and 200mm (8 inch) is in second place. In addition to existing wafer sizes, 450mm wafer size production is projected to come alive in following years [2].

The production of silicon wafers constitues only the first step in the fabrication of ICs. Many of the remaining steps deposit materials on the wafer or etch them away. A technique called photolithography allows photographic reproduction of patterns that can be used to selectively block depositions or etches. IC fabrication makes extensive use of photolithography.

A CMOS integrated circuit is fabricated by repetitively applying photolithography to build the necessary structural layers which creates the layout and at the end the chip. Photolithography begins with the application of a photosensitive emulsion called a photoresist (PR). PR is sensitive to certain wavelengths of light. First, the wafer is coated with PR then mask which defines a particular area is applied on PR with using ultraviolet light. Areas on PR exposed to UV can become polymerized depending on the type of PR applied. When the wafer is flooded with solvent, desired areas wash away and other areas remain coated with PR. This technique allow certain areas to be implanted while protecting undesired area with PR [3]

Every layer in the fabrication is done on the same basis by applying PR, exposing UV light, Repetation of this process builds the necessary structural layers.

2.2 CMOS Fabrication Process

Different type of production flows exit but this thesis will consider state of art techniques to fabricate CMOS.

If we analyze CMOS processes, we find that there are four basic layer types [3-13]:

1-Conductors: These layers are conducting layers in that they are capable of carrying signal voltages or currents. Diffusion areas, metal and polysilicon layers, and well layers fall into this category.

2-Isolation layers: These layers are the insulator layers that isolate each conductor layer from each other in vertical and horizontal directions. This isolation is required in both the vertical and horizontal direction to avoid “short circuits” between separate electrical nodes.

3-Contacts or vias: These layers define cuts in the insulation layer that separates conducting layers and allow the upper layer to contact down through the cut or “contact” hole. If this cut connects two same material of conductor then it is called “via”. If cut connects different type of conductor material, it is called contact. For example, connection between metal1 to metal2 is called “via” if metal1 and metal2 is made up of copper. Openings in the passivation layer for pads are called “contact” because it connects copper to aluminium. At the end, both “via” and “contact” serve the same purpose, connecting one layer to another.

4- Implant layers: These layers do not explicitly define a new layer or contact, but customize or change existing conductor propriety. For example, diffusion or active areas for PMOS and NMOS transistors are defined simultaneously. A P+ mask is used to create P+ implant areas that define certain diffusion areas to P-type by the use of a P-type implant.

Using a combination of these four types of layers, transistor devices, resistors, capacitors, and interconnections are created.

Fabrication process can be summarized briefly as below:

Well formation stage: Implants n-type impurities into the wafer followed by diffusing the impurities deep into the substrate to form the N-Wells. For CMOS process, the silicon substrate is usually p-type. (Figure 2.1)

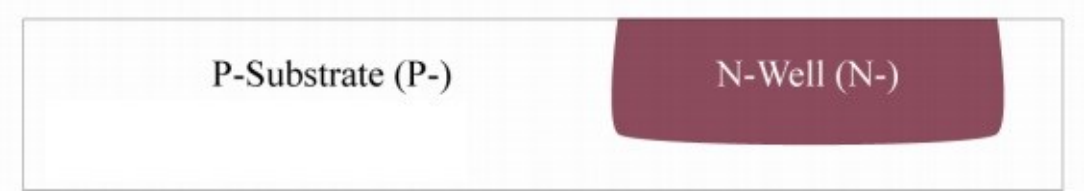


Figure 2.1 : Well formation stage [14].

Active & isolation stage: Thick oxide is grown outside the active areas. Active areas are defined as areas where the CMOS transistors are fabricated. Thick oxide (TOX) is also known as field oxide (FOX). Field oxides isolate the transistors from one another. (Figure 2.2)

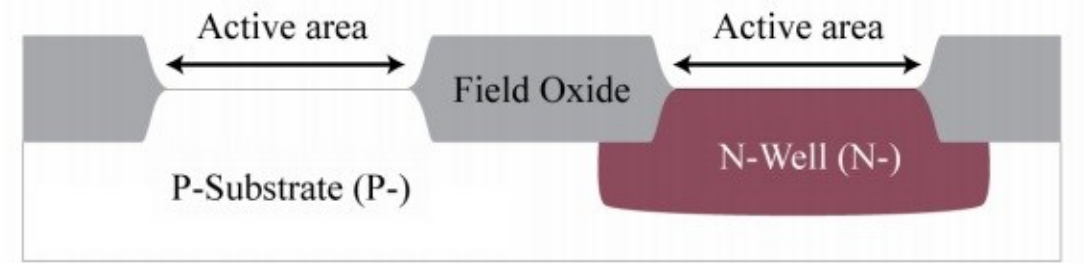


Figure 2.2 : Active and isolation stage [14].

The first two steps describe a formation of a conventional well. The depth and doping profile of a conventional well are controlled by the diffusion drive-in at high temperature. A better way to form the well is usually used in 0.25µm and smaller process technologies (A process technology of 0.25µ means that the shortest channel length (L) of a transistor is 0.25µm.). It is called ion implamentation. It is done by very high energy implantation. The depth and doping profile of a well are controlled by implantation energy and impurity dose. This is formed after the field oxide. Since this does not require diffusion drive-in, it has smaller lateral diffusion and a more ideal doping profile.

Gate oxide formation stage: A thin gate oxide is grown across the wafer. Gate oxide of only tens of silicon oxide atoms thick is created during the fabrication process with the current technology. Gate oxide is the insulator between the transistor's gate

and its channel. Gate oxide refers to the “O” in “MOS” which stands for Metal-Oxide Semiconductor. (Figure 2.3)

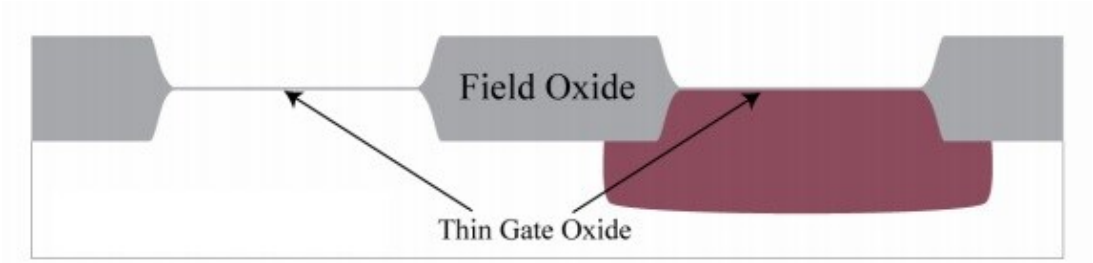


Figure 2.3 : Gate oxide formation stage [14].

Gate formation stage: Poly (i.e. poly-silicon) is deposited on the wafer. The poly that are deposited on the gate oxides are the gates of the transistors which are usually known as gate poly. The gate poly will incline upward when it extends over the field oxide. The gate oxide in the active area that are not covered by the gate poly will be etched away to form the source and the drain of the transistor. (Figure 2.4)

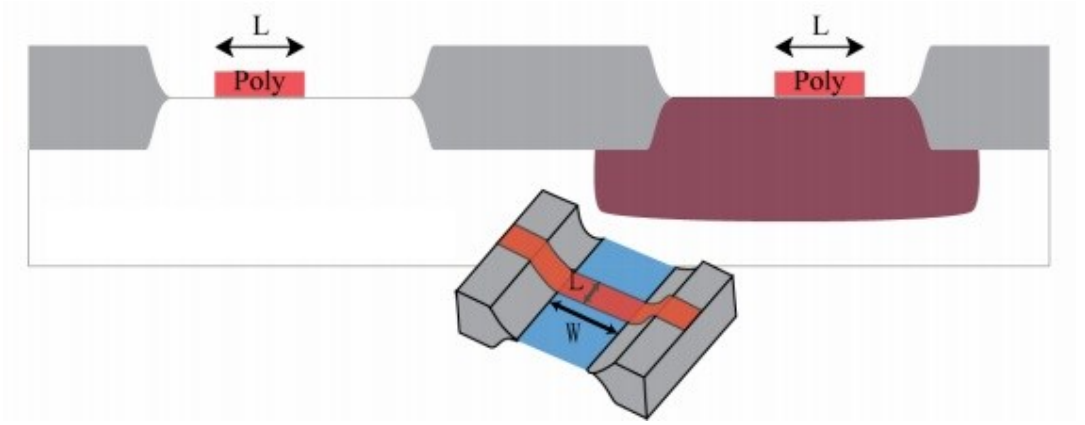


Figure 2.4 : Gate formation stage [14].

Source and drain formation stage: P-type and n-type impurities are implanted into the active areas. The impurities are diffused into the silicon to form the source terminals and the drain terminals. As the impurities diffuse both vertically and laterally, the gate poly will slightly overlap the sources and the drains which will result in gate overlap capacitances. The diffusions for the sources and the drains of NMOS and PMOS are N-diffusion (N-diff) and P-diffusion (P-diff) respectively. (Figure 2.5)

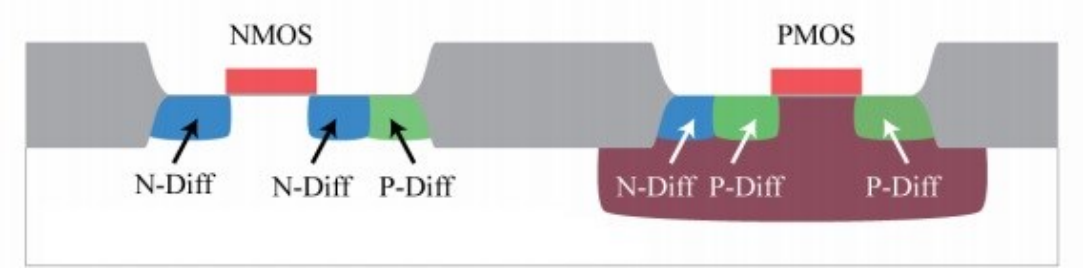


Figure 2.5 : Source drain formation stage.

P-diff in p-substrate is known as p-tap, while n-diff in N-well is known as n-tap. Connections from the metal routings to the substrate and the Nwells are made through the p-tap and the n-tap. This is necessary to ensure the wells are properly tied down and the transistors are isolated. The p-substrate should be biased to the lowest voltage potential while the N-well should be biased to the highest voltage potential. In this way, all the P-N junctions are reverse biased and hence the transistors are electrically isolated from one another

Isolating the transistors with the thick field oxide is commonly found in 0.35µm and larger process technologies. For 0.25µm and smaller process technologies, shallow trench isolation (STI) shown in the diagram below is more commonly used to isolate the transistors. (Figure 2.6) In STI fabrication, trenches are etched into the wafer and filled with silicon oxide to isolate the islands of transistor active area.

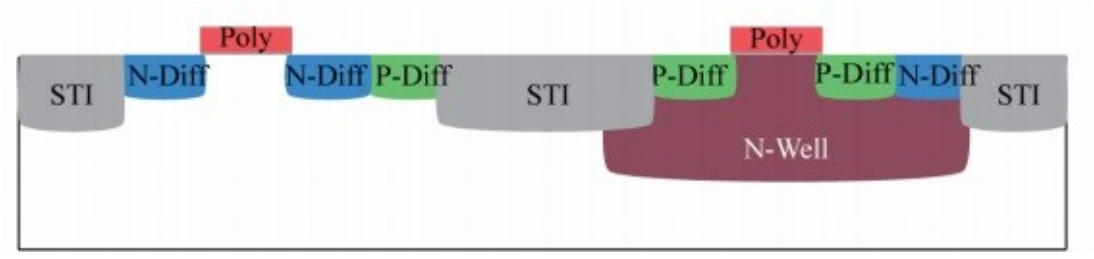


Figure 2.6 : Shallow trench isolation.

Following the basic process steps, it can be concluded that the drain and the source are fabricated in the same way. In Figure 2.7, overall CMOS layout structure which contains NMOS and PMOS can be observed. With this observation, The bulk of all the NMOS are connected together. The bulk of all the PMOS in the same N-well are connected together.

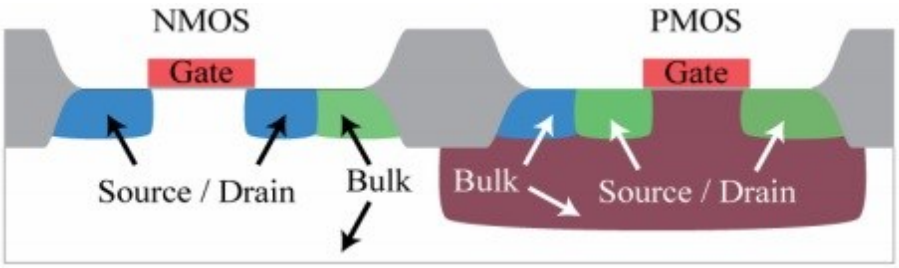


Figure 2.7 : NMOS and PMOS layout cross section.

Figure 2.8 shows simple mask steps that creates an inverter.

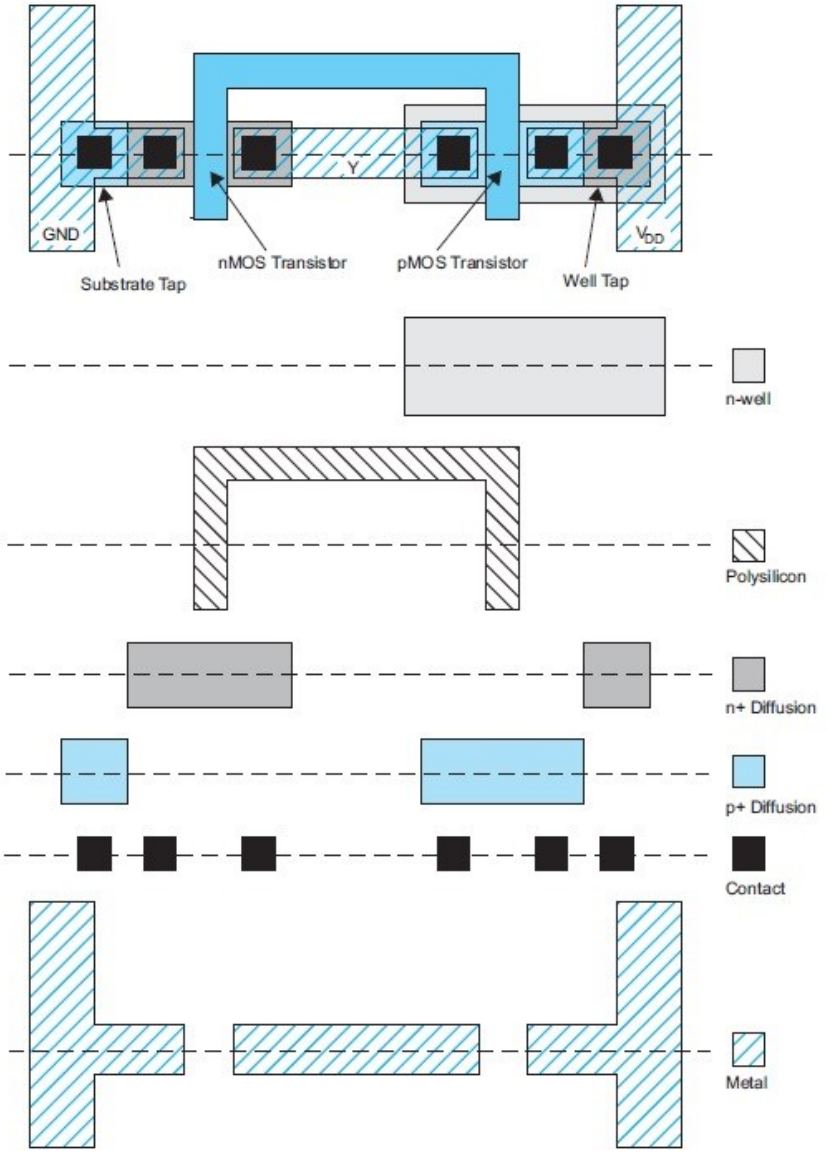


Figure 2.8 : Six masks that basically define an inverter.

3. BASIC LAYOUT STRUCTURES

3.1 CMOS Layout Structure

In a schematic view of a basic inverter, with its input, output, substrate, supply and ground pins. Input pin means that a signal is entering the designated circuit or block. Output is the result of the circuit after it does its job. Substrate pin is generally serves same as ground pin. In contrast, its purpose is separation of ground and substrate paths, so any parasitics do not couple through ground. Ground is the lowest potential in the circuit, block or chip. In general its notations are VSS, AVSS (Analog VSS), DVSS (Digital VSS), GND. Supply pin is the highest potential in the circuit, block or chip. Its notations vary differently but most common types are VDD, AVDD (Analog VDD), DVDD (Digital VDD) or small letters of same notations. Naming convention of ground and supply pins should be consistent all over chip and sub-blocks but depending on purpose, more than one supply or ground can exist.

3.2 PN Diode Layout

Two types of PN junctions can be formed in a standart CMOS technology: one in the p-substrate and another in an n-well in Figure 3.1. PN junction done by using p-substrate itself is not possible to use as diode. To allow current to flow, PN diode needs to work in forward biased mode. Forward biased PN diode in p-substrate means current is injected to substrate. This will cause substrate potential to rise which leads to unexpected, uncontrolled malfunctions in chip [7].

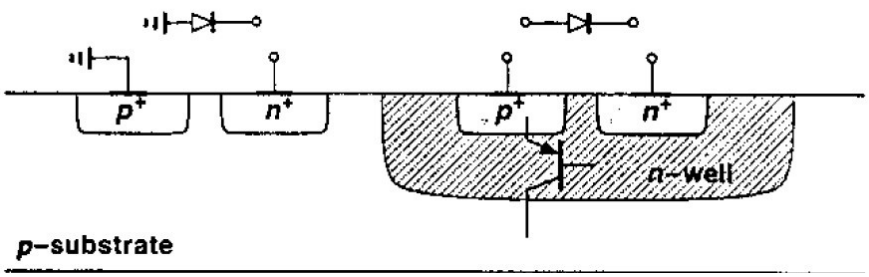


Figure 3.1 : Pn-diode structures.

The diode formed in an n-well also faces difficulties if forward biased. P^+ region in the n-well, the n-well itself, and the p-substrate constitute a bipolar pnp transistor whose collector is typically grounded. Thus, if the pn junction in the n-well is forward biased, substantial current flows from the p^+ terminal to the substrate. In other words, the structure must not be viewed as merely a two-terminal floating diode.

3.3 BJT Layout

Since this thesis only considers CMOS technology, other types of transistors are not explained. However, it is good to have brief layout knowledge about BJT since BJT and MOSFET have similar but not identical operational behaviours. In Figure 3.2, top-view of BJT and cross-section of it can be analysed. Structure heavily relies on pn structures as one level of layer on top of other.

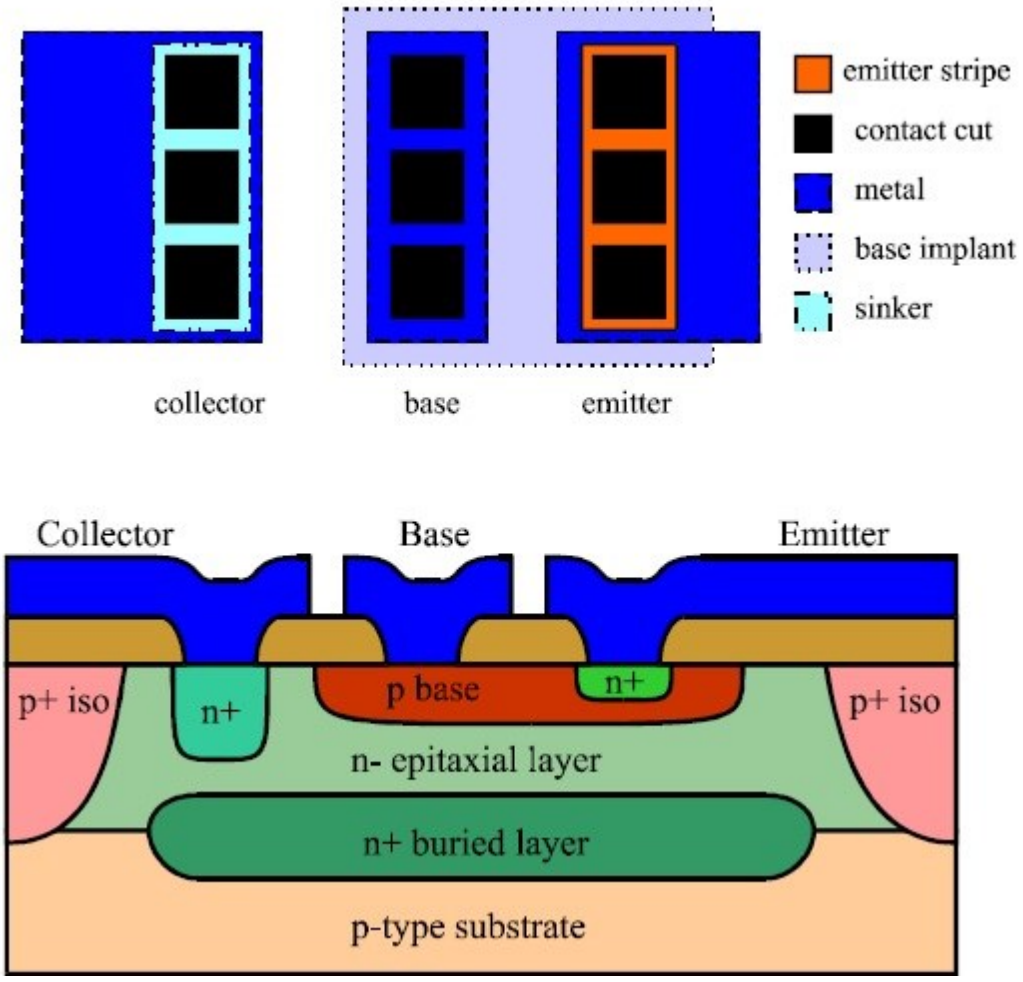


Figure 3.2 : Top view and cross-section of BJT layout.

3.4 Resistor Layout

A CMOS process may be modified so as to provide resistors suited to analog design. A common method is to selectively "block" the silicide layer that is deposited on top of polysilicon, thereby creating a region having resistivity of the doped polysilicon, in Figure 3.3. This means the fabrication requires an additional mask and corresponding lithography sequence [15]

The use of silicide on the two ends of the resistor results in a much lower contact resistance than that obtained by directly connecting the metal layer to doped polysilicon. Also polyresistors typically exhibit much less capacitance to substrate than other types.

Other types of resistor structures are double poly resistor (which is not used in modern fabrication process because only one poly options are available), metal resistor which relies on sheet resistance of metal line hence having low resistance values compared to poly resistor. Nwell resistor is also available but its resistivity may vary large with process so not used in applications where resistor value is critical. Depletion region formed between n-well and p-substrate, nwell resistors suffer from large parasitic capacitance

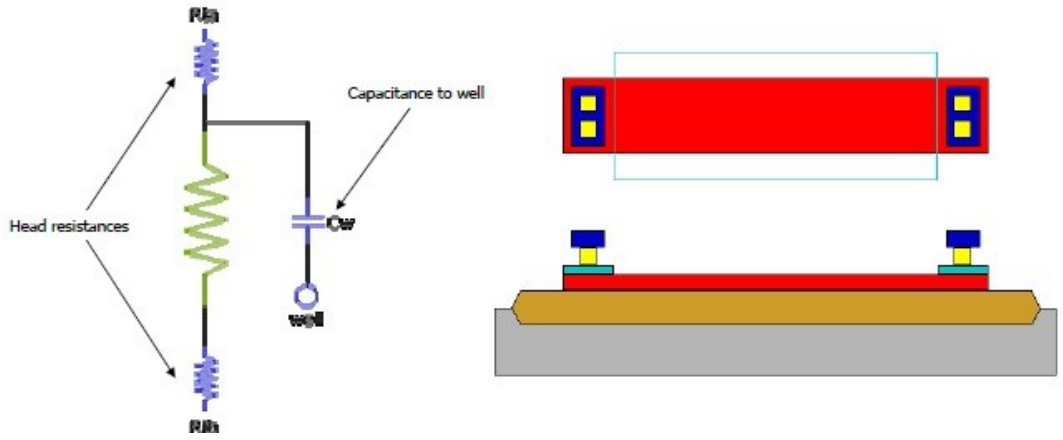


Figure 3.3 : Resistor model (left), top-view (top) and layout (bottom) of a resistor.

3.5 Capacitor Layout

Capacitors prove indispensable in most of today's analog CMOS circuits. Several parameters of capacitors are critical in analog design: nonlinearity (voltage dependence), parasitic capacitance to the substrate, the series resistance and capacitance per unit area (density). In CMOS technologies modified for analog design, capacitors are fabricated as metal-insulator-metal capacitor (MIM), metal-on-metal capacitor (MOM) and mosfet's used as capacitor by drain and source are connected together to form one side plate and gate forms the other side plate.

3.5.1 MOS capacitor

Metal-oxide semiconductor capacitor (MOSCAP) as name implies made by using either PMOS or NMOS transistors. It is done by connecting drain and source to same net and voltage and gate to another. Thin oxide under polysilicon (gate) and channel that it formed underneath it by drain and source side can be used as a capacitor. In order to form channel, transistors has to be biased in accumulation or strong inversion mode [16].

MOS capacitor has a structure that drain, source and bulk (D, S, B) of a PMOS transistor tied together (D=S=B) corresponds to one plate, while the polysilicon gate creates the other plate. This structure depends on the gate-bulk voltage V_{BG}. The MOS capacitor is shown in Figure 3.4. In the case of PMOS capacitor, an inversion channel with mobile holes builds up for $V_{BG} > |V_T|$, where $|V_T|$ is the threshold voltage of the transistor. $V_{BG} >> |V_T|$ guarantees the MOS capacitor works in the strong inversion region. However, for the value of the voltage $V_G > V_B$, the device enters the accumulation region, where the voltage at the interface between gate oxide and semiconductor is positive and high enough to allow electrons to move freely. The value of the MOS capacitance, CMOS in the strong inversion and accumulation region is at its maximum, and is equal to

$$C_{ox} = \varepsilon_{ox}\left(\frac{L.W}{t_{ox}}\right) \quad \textbf{(3.1)}$$

where LxW is the transistor channel area and t_{ox} is the gate oxide thickness.

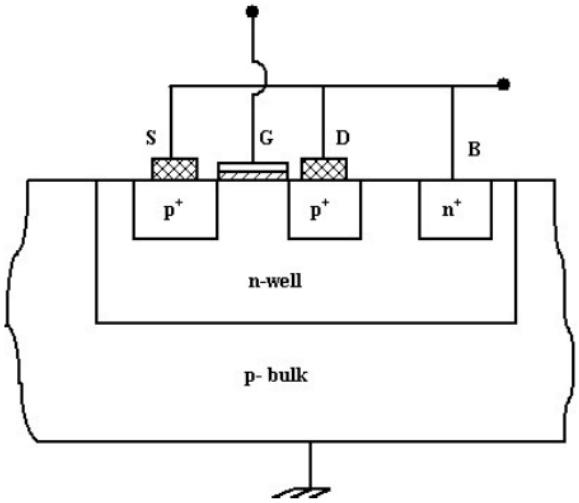


Figure 3.4 : MOSCAP layout cross-section [16].

Three more regions exist for the intermediate values of V_{BG}: moderate inversion, weak inversion, and depletion. In these regions there are few or very few mobile carriers at the gate oxide interface that decreases the capacitance of the MOS device. Capacitive versus V_{BG} characteristics of a MOS capacitor is shown in Figure 3.5.

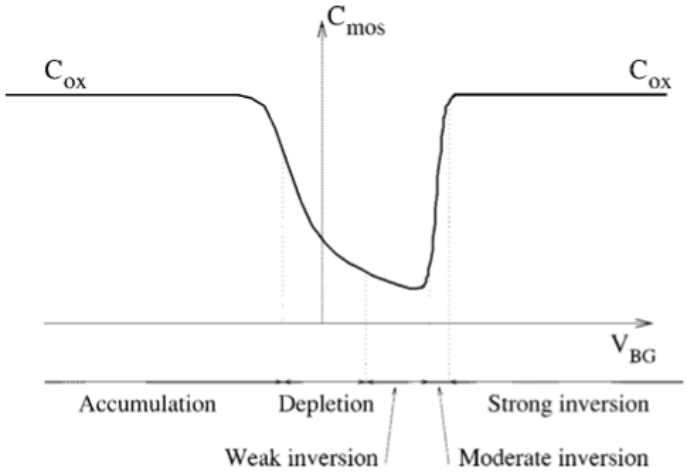


Figure 3.5 : Capacitive versus V_{BG} characteristics of a MOS capacitor [16].

Benefit of using MOSCAP is; process does not require additional masks to produce so makes it cost effective and can be placed everywhere as it does not need any special care in contrast to analog block layouts.

Downside of using MOS transistor as a capacitor is MOS capacitors have high parasitic resistance. This resistance comes from both channel resistance and the resistance of the metal plates. Other drawback of using MOS cap is as explained before; in order to achive a capacitance value, MOS transistor has to be biased in

accumulation or strong inversion modes and design should guarentee that these biasing does not change.

3.5.2 MIM capacitor layout

A MIM capacitor consists of two metal layers (plates) separated by a deposited dielectric layer. A cross section of a MIM capacitor is shown in Figure 3.6. A thick oxide layer is typically deposited on the substrate, reducing the parasitic capacitance to the substrate. The parasitic substrate capacitance is also lowered by utilizing the top metal layers as plates of a MIM capacitor. The capacitance density can be increased by reducing the dielectric thickness and employing high-k dielectrics [17-19].

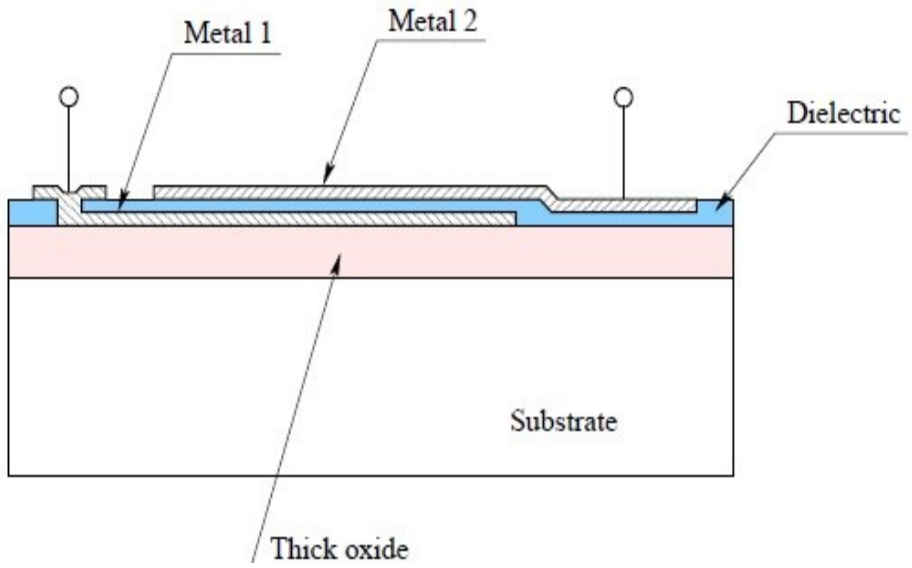


Figure 3.6 : Cross section of a MIM capacitor [17]

In today's IC fabrication, MIM capacitors are done on top metal and one metal below top metal, to reduce substrate capacitance which is undesired. In addition to this, by using extra process steps and masks MIM cap is created in to special layers which are not used as metal in design. They are called Capacitor Top Metal (CTM) and Capacitor Bottom metal (CBM). In order to do that additional process step and masks are required which increases the fabrication cost of a chip. Figure 3.7 and Figure 3.8 depicts widely used MIM capacitor cross-section.

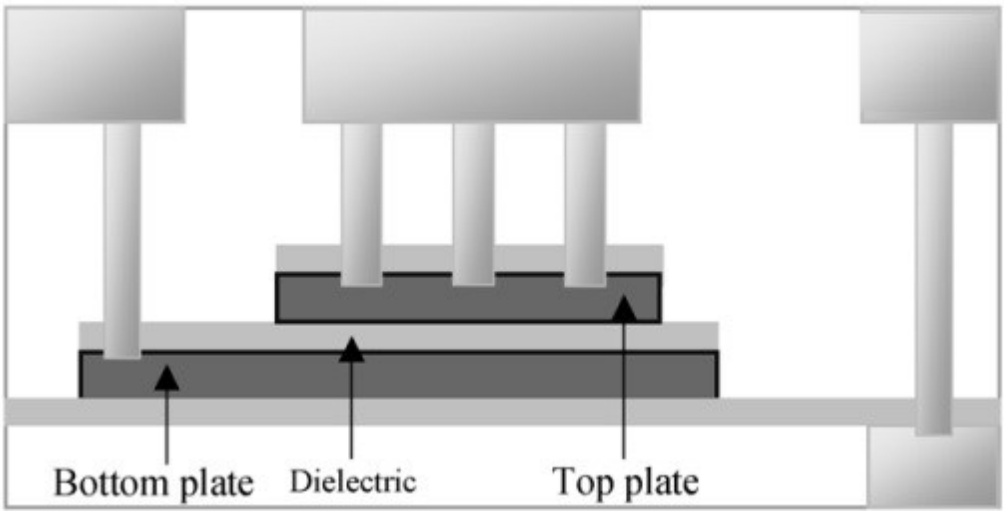


Figure 3.7 : MIM capacitor consisting of CTM and CBM layers [18]

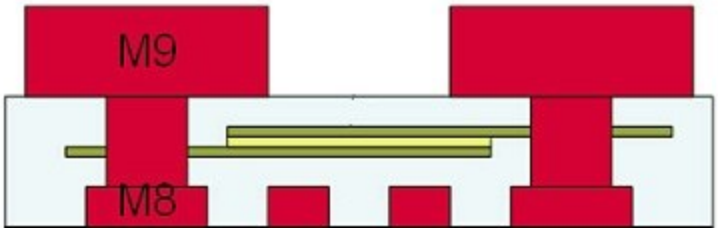


Figure 3.8 : Another view of MIM capacitor.

3.5.3 Metal - on - metal (MOM) capacitor layout

The total capacitance per unit area can be increased by using more than one pair of interconnect layers. Current technologies offer up to ten metal layers, increasing the capacitance nine times with a sandwich structure. The capacitance is further increased by exploiting the fringe capacitance between the adjacent metal lines within a special interconnect layer. In scaled technologies, the adjacent metal spacing (on the same level) shrinks faster than the spacing between the metal layers (on different layers), resulting in substantial lateral coupling. It is same in vertical capacitance between two metal layers, Figure 3.9 gives top and angled view of MOM capacitors.. By using fingered and stacked metals from bottom to allowed top metal, we can increase capacitance as much as possible.

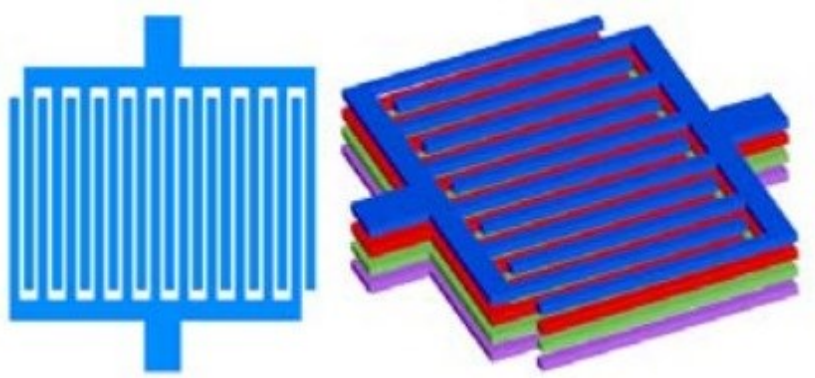


Figure 3.9 : MOM capacitor view [20].

3.6 Electromigration

Electromigration is the gradual displacement of metal atoms in a semiconductor. It occurs when the current density is high enough to cause the drift of metal ions in the direction of the electron flow, and is characterized by the ion flux density. This density depends on the magnitude of forces that tend to hold the ions in place, i.e., the nature of the conductor, crystal size, interface and grain-boundary chemistry, and the magnitude of forces that tend to dislodge them, including the current density, temperature and mechanical stresses [21]

In another way, under the conditions of high current densities and high temperatures in metals, there is momentum transfer between conducting electrons and diffusing metal atoms. This causes gradual drift of the ions in the metal in the direction of electron flow and result in mass transport. This process of material transfer is called Electromigration(EM).

The effect of EM in integrated circuits is open circuit(void) or short circuit(Hillock) failures shown in Figure 3.10.

The mean time to failure(MTTF) of an interconnect is the expected time that it will operate before the first failure. MTTF of the interconnect under constant current stress and temperature, subjected to EM affects, is given by Black's equation as

$$\text{MTTF} = \frac{A}{J^n} e^{(\frac{E_a}{kT})} \qquad \textbf{(3.2)}$$

where

E_a →Activation energy for failure(0.5 to 0.7 eV for Al)

A →Constant based on the cross-sectional area of the interconnect

J →Current density in the metal interconnect

n →Constant vary between 1 ~ 7 (usually set to 2 acording to Black)

k →Boltzmann constant

T →Temperature in Kelvin (K^o)

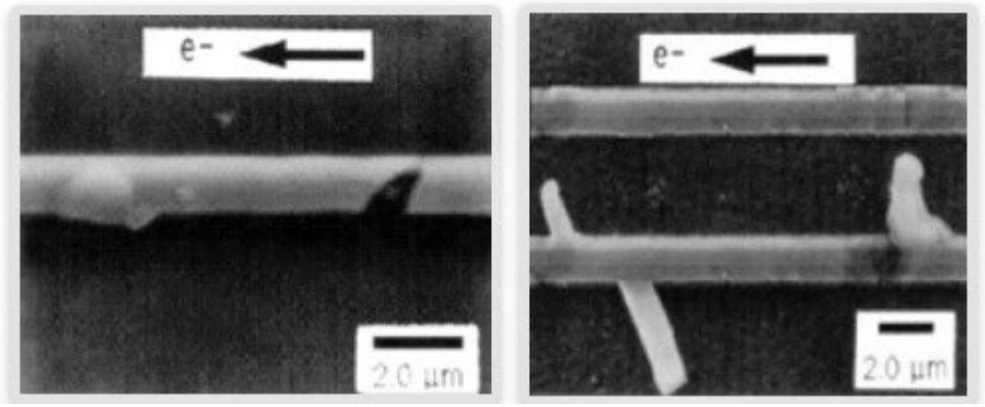


Figure 3.10 : EM failure types, open circuit (left), short circuit (right) [21].

The formula indicates that temperature and current density are the key factors that contribute to electromigration mechanism. The temperature of the conductor appears in the exponent, i.e. it strongly affects the MTTF of the interconnect. For an interconnect to remain reliable as the temperature rises, the maximum tolerable current density of the conductor must necessarily decrease.

Electromigration, eventually determines the current capability of an interconnect metal in process. A quote taken from one of the foundaries' design rule document states that "I_{max} is the maximum DC current allowed for metal lines, vias,, or contacts. Imax is based on 0.1% point of measurement data at a 10% resistance increase after 100K hours of continuous operation at 110^0C." [22].

To explain more in depth, failure level of an interconnect is set to 10% increase in resistance and this must be achieved at least 100.000 hours of continuous operation with temperature in 110^0C. If design requires a working temperature more or less than 110^0C, then foundary gives a rating factor to convert standart 110^0C I_{max} value to desired temperature.

Rating factor of I_{max} → 2.33 (at $\leq 85^0$C), 1.38 (at 100^0C), 1.17 (at 105^0C), 1 (at 110^0C), 0.735 (at 120^0C), 0.633 (at 125^0C)

For instance: I_{max} (at 125^0C) = 0.633xI_{max}(at 110^0C)

There is also a term called I_{peak} exits. I_{peak} is the current at which a metal line undergoes excessive Joule heating and can begin to melt. Thus, I_{peak} should not be a limit to current density as reaching I_{peak} value means interconnect metal will not work and cause vital errors. I_{peak} value can vary 30 – 60 mA per width. Detailed information about this can be found in foundary's design rule document.

The I_{peak} rule applies to periodical AC or pulsed DC signals that has a pulse width of less than 1msec.

I_{peak} of contact and vias are not included because the heating in contacts and vias is negligible and is usually determined by metal or substrate.

3.7 Electromigration Dependency On Physical Effects

3.7.1 Temperature

From Black's equation, it is clear that failure due to electromigration is dependent on temperature; however, there is a more sinister dependence on temperature that accelerates failures due to voids. Figure 3.11 highlights a cyclical positive feedback loop that ultimately ends in failure

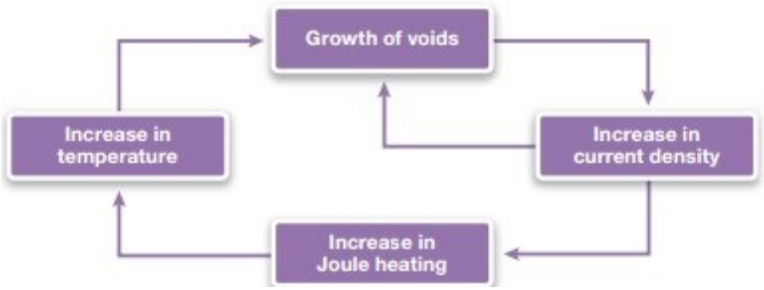


Figure 3.11 : Electromigration dependency on temperature [21].

Once a void begins to develop in a metal wire, the wire itself becomes narrower at that point. Due to the reduction in width, the current density increases and, therefore, the interconnect temperature increases due to Joule heating. Joule heating is a result of root-mean square (RMS) current. As the temperature of the wire increases, the growth of the void accelerates, and eventually an open circuit occurs. This is why it is critical to also take RMS current into account when performing EM analysis

3.7.2 Wire width and current density

Current density is the primary factor influencing electromigration. Wider metal lines have lower current density for the same current, hence have high resistance to electromigration. There is one exception to this rule and that is when the wire width falls below the average grain size of the interconnect material. This apparent contradiction is caused by the position of the grain boundaries (Figure 3.12), which in such narrow wires lie perpendicular to the width of the whole wire. Because the grain boundaries in these so-called "bamboo structures" are at right angles to the current, the boundary diffusion factor is excluded, and material transport is correspondingly reduced (Figure 3.13) [23].

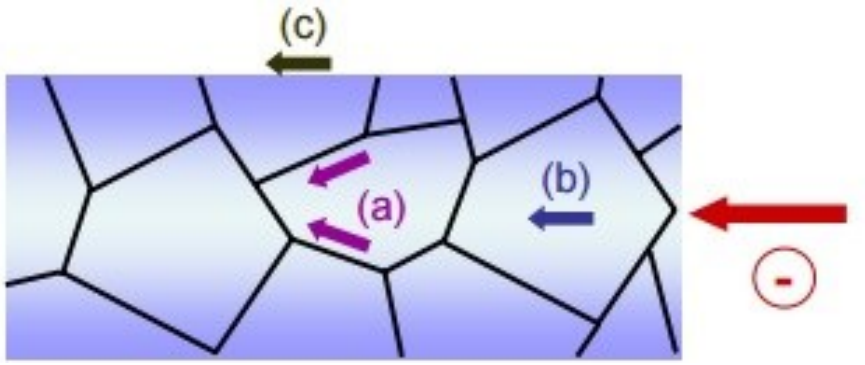


Figure 3.12 : Illustration of various diffusion processes within the lattice of an interconnect: **(a)** grain boundary diffusion, **(b)** bulk diffusion, and **(c)** surface dissusion [23]

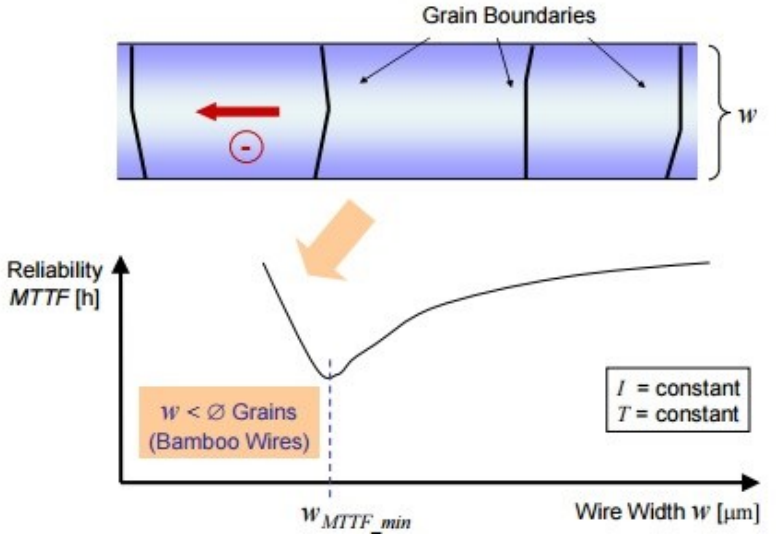


Figure 3.13 : Reduced wire width below the avarage grain size increases the reliability of the wire with regard to electromigration [23]

So-called bamboo wires are characterized by grain boundaries which lie perpendicular to the direction of the electron wind and thus permit only limited grain boundary diffusion.

However, the maximum wire width possible for a bamboo structure is usually too narrow for signal lines of large-magnitude currents in analog circuits or for power supply lines. In these circumstances, slotted wires are often used, whereby rectangular holes are carved in the wires. Here, the widths of the individual metal structures in between the slots lie within the area of a bamboo structure, while the resulting total width of all the metal structures meets power requirements.

3.7.3 Wire length

There is also a lower limit for the length of the interconnect that will allow electromigration to occur. It is known as “Blech length”, and any wire that has a length below this limit (typically in the order of 10-100 μm) will not fail by electromigration. Here, a mechanical stress buildup causes a reversed migration process which reduces or even compensates the effective material flow towards the anode. Specifically, a conductor line is not susceptible to electromigration if the product of the wire’s current density J and the wire length l is smaller than a process technology-dependent threshold value (J·l)

3.8 IR Drop

The Power supply in the chip is distributed uniformly through metal layers (Vdd & Vss) across the design. These metal layers have finite amount of resistance. When voltage is applied to this metal wires current starts flowing through the metal layers and some voltage is dropped due to that resistance of metal wires and current. this drop is called as IR drop. Highest and one below highest metal are used for power and ground routing in chip level layout. These metals are thicher and wider than lower metals thus reducing metal resistance for power rails or inductors.

IR drop is an unwanted drop in voltage caused by current through a metal wire. It is so named because voltage (V) = current (I) * resistance (R). An unexpected voltage drop on an instance or a device can cause a functional failure because the lowered voltage supply may not be strong enough to switch the instance, or may switch it too slowly.

IR drop is signal integrity (SI) effect caused by wire resistance and current drawn off from power(Vdd) and ground (Vss) grids. According to ohms law, V=IR. If wire resistance is too high or the current passing through the metal layer is larger than the predicted, an unacceptable voltage drop may occur. Due to this unacceptable voltage drop, the power supply voltage decreases. That means the required power across the design is not reaching to the cells. This results in increased noise susceptibility and poor performance.

The design may have different types of gates with different voltage levels. As the voltage at gate decreased due to unacceptable voltage drop in supply voltage, the gate delays are increased non-linearly. This may lead to setup time and hold time violations depending on which path these gates are residing in the design.

As technology node shrinking, there is decreased in the geometries of the metal layers and the resistance of this wire increased which lead to decrease in power supply voltage during CTS, the buffers and inverters are added along the clock path to balance the skew. The voltage drop on the buffers and inverters of clock path will cause the delay in arrival of clock signal, resulting hold violation.

Signal carries both voltage and current, however depending on signal type, voltage value or current might be more important than other might. This affects the layout of the circuit. If current is more crucial, layout need some calculations whether metal line that carries current is enough wide to handle that much of current. If voltage is critical than IR drop is needed to be taken into consideration, Figure 3.14. Note that voltage equals current times resistance (V= I*R). In addition to that if signal is sensitive some shielding strategies should be applied. These will be explained later in thesis.

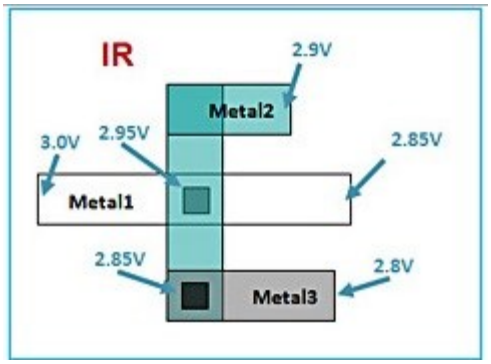


Figure 3.14 : IR drop in layout.

4. ISOLATION SCHEMES

Isolation techniques protect circuit from noise or prevents noise to couple other blocks or devices. First part is isolation of device itself. In that part, isolation is achieved on fabrication process.

As different circuits/blocks behave differently and prone to different effects, an isolation strategy should be build to protect them which is explained in second part, isolation in layout

4.1 Isolation of Device in Fabrication Process

To avoid electrical shorts between the closely placed MOS transistors, the electrical isolation of the MOS from all sides is a must.Usually, silicon dioxide (SiO2) is used for this purpose. SiO2 has the advantage that it can be easily etched, besides being process compatible; and it can be grown or deposited easily compared to other dielectric materials. There are many oxide-based isolation schemes, but the three most popular oxide isolation schemes, namely, thick oxide isolation, Local Oxidation of Silicon (LOCOS) isolation and shallow trench isolation.

Thich Oxide isolation suffers from high vertical oxide step at the edge of the field-oxide and active areas. This sharp vertical oxide step creates proclems for subsequent MOS fabrication steps. In additon, the silicon area is more consumed then other two schemes. Furthermore, in the thick oxide isolation scheme, the transistrs are isolated from the top of the wafer surface, but not from bottom of the silicon wafer. For these reasons, the thick oxide isolation scheme is not used in MOS fabrication process.

4.1.1 Local oxidation of silicon (LOCOS)

LOCOS has been used extensively for 0.35μ or larger minimum linewidth CMOS technologies.

A thick oxide layer is grown by the oxidation process [24]. The thick oxide is called Field Oxide (FOX). These FOX areas are used for MOS isolation. By laying nitride film on top of active areas, oxygen atoms cannot diffuse through the nitride film;

thus, no oxide is formed in the active areas. This eventually leads to the local oxidation of the silicon wafer. That is why process called local oxidation of silicon (LOCOS). FOX is not sharp vertical, but slanted inside the active.

In the LOCOS isolation scheme, the MOS transistors are isolated form the top as well as bottom of the wafer to some extend. The LOCOS oxide has gentle slope between the FOX and the active areas with less oxide height [25].

Unfortunately, the LOCOS scheme suffers from loss of silicon due to a "bird's beak" formation, Figure 4.1. The bird's beak is formed due to lateral diffusion of oxygen atoms inside the active regions, resulting in the oxidation of the silicon. The bird's beak encroaches into the active area, thereby reducing the achievable circuit packing density. The effective channel width of the transistor is affected by the bird's beak. Moreover, LOCOS requires a long, high-temperature process, which can result in significant diffusion of previously introduced dopants.

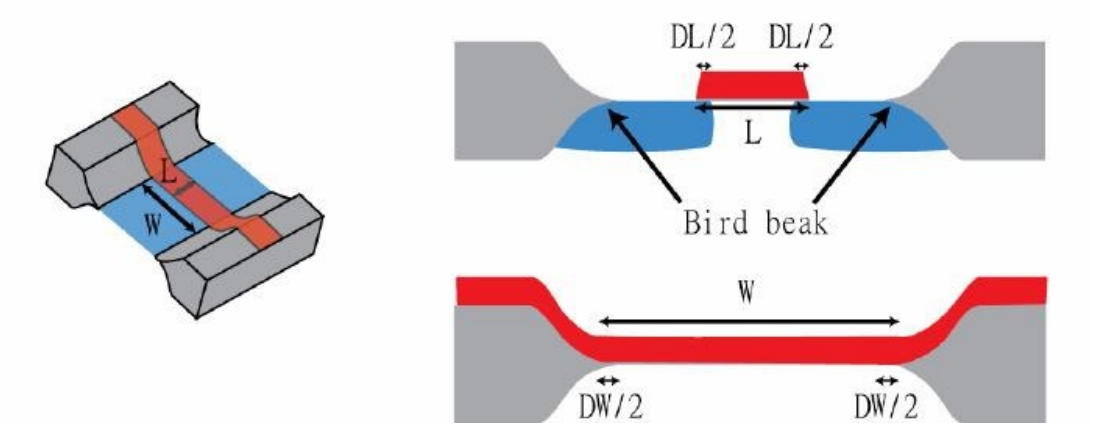


Figure 4.1 : Bird's beak and its effect on device width [14].

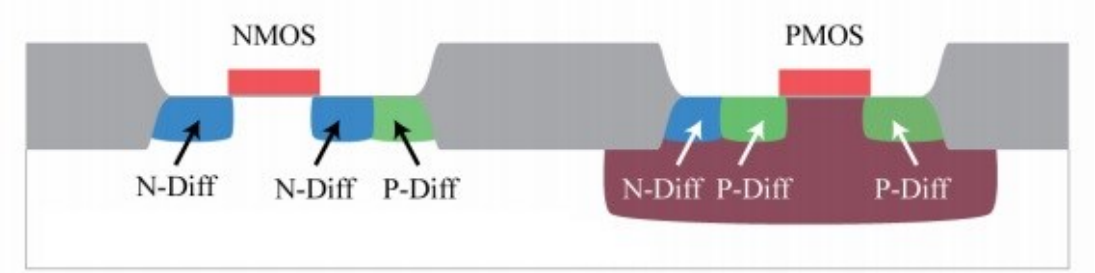


Figure 4.2 : LOCOS formation in NMOS and PMOS cross-section.

In Figure 4.1 can be seen that due to oxide growth in LOCOS, expansion is upwards and downwards through substrate and Figure 4.2 shows FOX with NMOS and PMOS layout cross-section.

4.1.2 Shallow trench isolation

Shallow trench isolation (STI), is an integrated circuit feature which prevents electric current leakage between adjacent semiconductor device components. STI is generally used on CMOS process technology nodes of 0.25µ and smaller [26-31].

STI is created early during the semiconductor device fabrication process, before transistors are formed. The key steps of the STI process involve etching a pattern of trenches in the silicon, depositing one or more dielectric materials (such as silicon dioxide) to fill the trenches, and removing the excess dielectric using a technique such as chemical-mechanical planarization (CMP).

Advantage of using STI is deeper isolation between devices. Filled trenches also called Field oxide. Disadvantage of STI is mechanical stress on device which affects the performance. This effect is called STI Proximity effect or Length of Diffusion (LOD) effect which will be explained in further chapters.

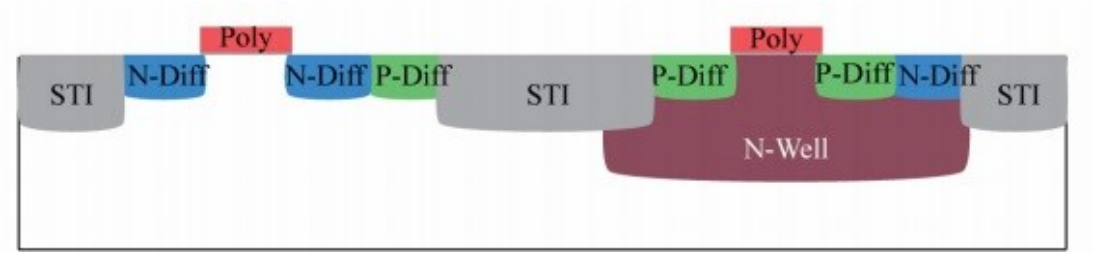


Figure 4.3 : STI formation of NMOS and PMOS cross-section.

The mechanical stress of STI on device is first noticed in 0.13µ node and later on smaller nodes this became a dominant factor, in order to to balance or minimize STI proximity effect some layout structures are used. These will be explained in further chapter.

Figure 4.3 shows STI formation, this formation has more planar surface than LOCOS formation with help of CMP.

4.2 Isolation in Layout

Analog design performances are sensitive to electrical disturbance as known as noise. Disturbance (noise) in the substrate should be minimized as much as possible. Two common types of substrate disturbance are

- Disturbance from minority carrier
- Substrate coupling noise

Above subject discusses about noise in terms of layout and further subjects are explained to reduce noise susceptibility.

There are different types and structures for isolation. Nearly all of them can be utilized in layout to achieve best protection, however applying all types and structures come with a cost in either area consumption or additional mask need in fabrication which means more expensive production cost

4.2.1 Disturbance from minority carrier

Minority carriers are injected into substrate from source diffusion and the drain diffusion when

- The source potential or the drain potential of NMOS is below the subtrate potential
- The source potential or the drain potential of PMOS is above the N-well potential

There are several possibilities for the above conditions to happen. Examples are

- Inductive ground path causes the ground in the substrate to bounce
- Resistive power and ground path from the power pins to the subtrate and the n-well
- Fast switching with significant overshoot

The drifting of the minority carriers in the substrate and the n-well create a potential difference that can affect the performance of the circuit or trigger a latch-up.

4.2.2 Substrate coupling noise

A reverse biased diode has the electrical properties of a capacitor. Circuit signals can be coupled through the substrate as illustrated in the diagram below, Figure 4.4.

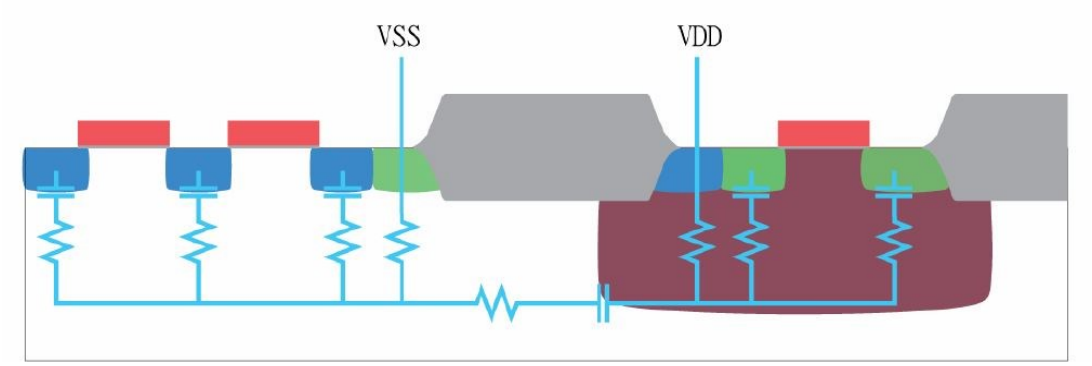


Figure 4.4 : Substrate coupling noise.

To prevent this coupling guard rings should be utilized. Below, how they work explined and configuration to implement showed.

4.2.3 Guard rings

To reduce substrate coupling noise, one may use guard ring in the following configuration around critical transistors.

- Surround NMOS in the p-substrate with p-tap guard ring that is connected to ground.
- Surround PMOS in n-well with n-tap guard ring that is connected to VDD.

To reduce disturbances from minority carrier, one may use guard ring in the following configuration around noisy transistors.

- Surround NMOS in the p-substrate with n-well guard ring. Tie the n-well guard ring to VDD. The n-diffusions from the NMOS could inject stray electrons into substrate. These stray electrons could be collected efficiently by the n-well guard ring that is biased to VDD to attract the electrons.
- Surround the PMOS in the n-well with p-diffusion guard ring. Tie the p-diffusion guard ring to ground. P-diffusions from the PMOS inject stray holes into the n-well. These stray holes could be collected efficiently by the p-diffusions guard ring that is biased to ground to attract the holes.

For the guard rings to be effective, the resistance in the path from noise source to the guard ring and then to the voltage source (either VDD or VSS) must be kept as low as possible. Hence guard ring should be made as wide as possible to decrease resistance. Wider guard ring helps to reduce ~5dB extra isolation [76]. Ideally, the guard rings should be placed as closely to the noise sources as possible, closer the guard ring better noise isolation achieved (~7dB better isolation) [76]. The guard rings are also placed around the critical transistors to minimize stray electrons and stray holes from affecting the critical transistors [32]

An important layout practice is to ensure that there is no (or very little) current flowing through any part of the guard ring. Consider the layout in the diagram below. A current flowing in the p-type guard ring raises its potential above VSS. If the potential of the n-diffusion next to the ptype guard ring (shaded in the diagram) is at VSS, the PN junction potentially becomes forward biased, and results in holes injected from the guard ring into the substrate, Figure 4.5.

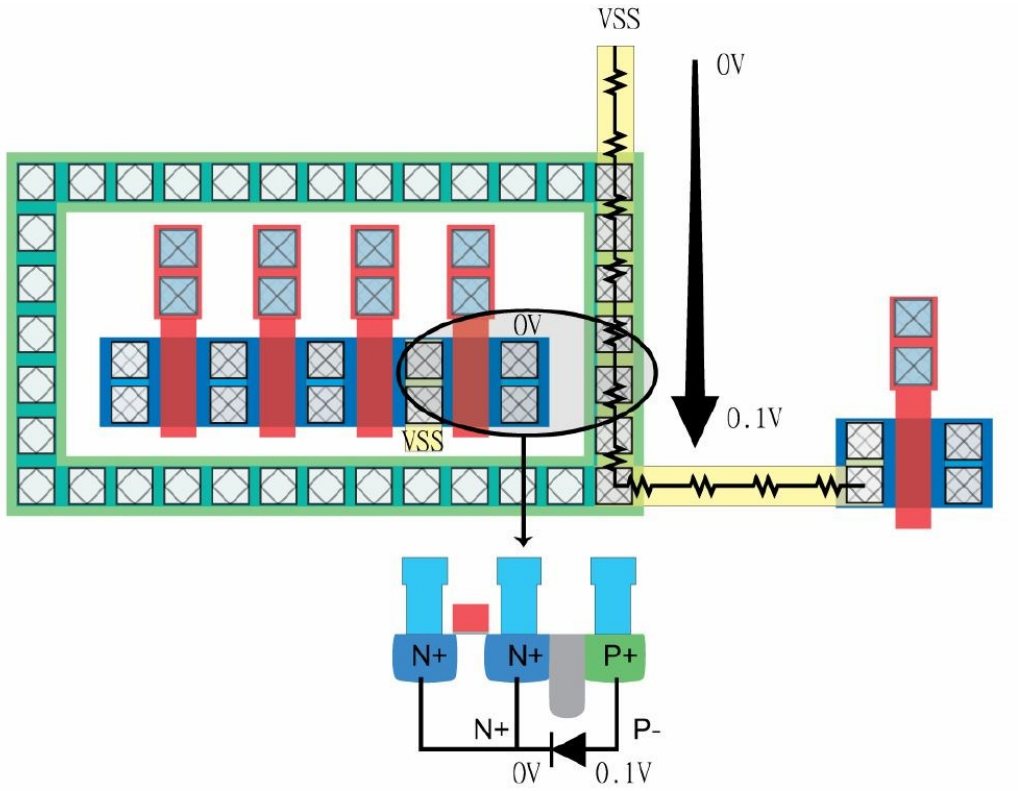


Figure 4.5 : Guard ring path.

4.2.3.1 Nwell guard ring

By nature of PMOS device, it sits inside an nwell area and nwell rings are used to bias the bulk (or body) connection of PMOS device. This nwell area needs to be

biased to the highest potential in the chip. Generally, the highest potential is named as VDD, AVDD, DVDD, vsupply etc. To bias this nwell area, nwell guard rings are used around PMOS devices. Nwell guard ring can also be called ntap guard ring.

This connection should be done in a smooth transition. Because nwell area has high ohmic resistance while metal that will bias nwell has low ohmic connection. This is achieved by using a medium which has lower ohmic resistance then nwell area whilst higher ohmic resistance than metal. This medium is n+ diffusion in nwell guard ring. So, this prevents schotthy diode in connection.

Another purpose of guard ring is to attenuate noise coming from surface of wafer or noise coming from below the surface. As biasing is higher potential noise cannot go through nwell ring, instead it travels down on substrate. As substrate doping concentration is high on surface and getting lower in deeper creating a more resistive field in middle and bottom of subsrate. By forcing noise to go deeper to pass nwell, noise gets attenuated which is a benefit for device and overall circuit to be less effected by noise.

4.2.3.2 Ptap guard ring

NMOS device sits on p-substrate itself and device bulk (or body) needed to be biased also. In order to do that, ptap guard ring is used. Ptap guard ring is created by p+ diffusion in p-substrate, this is similar in concept which is explained in nwell guard ring section.

Purpose of this rings are to collect minority carriers (which can be also called “noise”). Noise is injected into substrate and can travel and disturb working conditions of the circuit or it may alter the resulting outcome. Ptap rings help to collect these noise before reaching circuit or device itself. By doing so, noise sensitivity of the circuit is improved.

4.2.3.3 Double guard ring concept

This concept uses both ntap and ptap in conjucture with each other. Order of the rings change depending on which device it protects.

NMOS transistors can be surrounded by first (inner ring) p+ connection to lowest potential (VSS, AVSS or DVSS etc.) then again surrounded by (outer ring) n-well

guard ring with n+ connection to vdd, Figure 4.6 and Figure 4.7 show same but PMOS version.

PMOS transistors surronded by n+ ring then p+ ring surrounding the sutructure again.

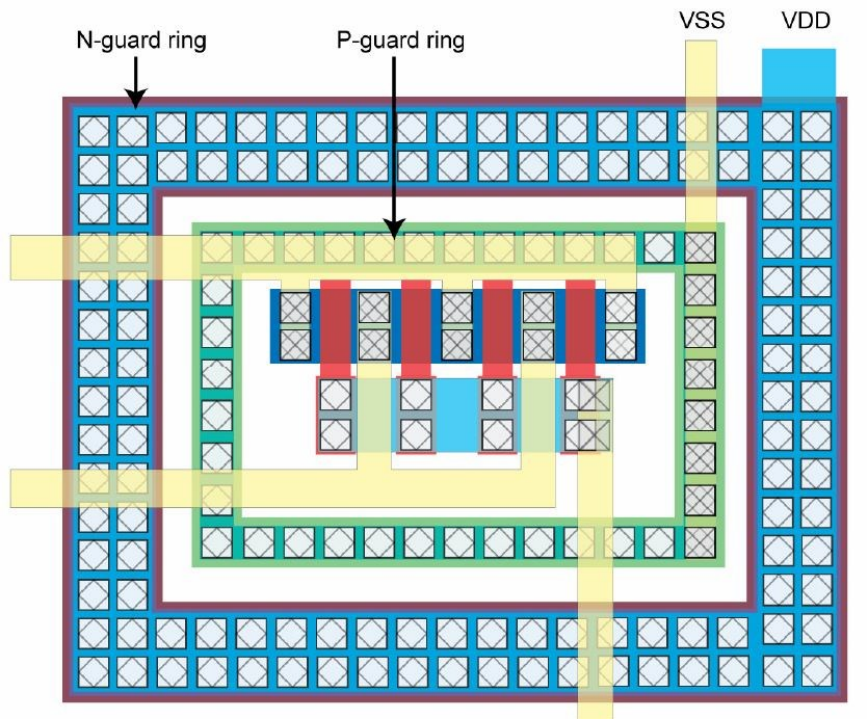


Figure 4.6 : Double guard ring structure for NMOS [14].

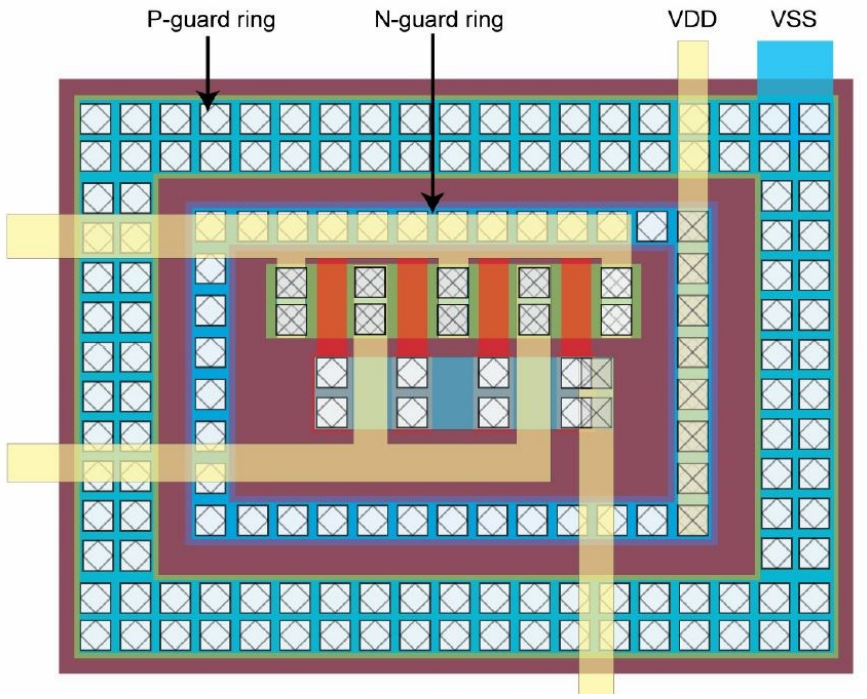


Figure 4.7 : Double guard ring structure for PMOS [14].

Double guard ring increase noise protection to some extend but there will be still uncaptured noise coming from deeper sides in substrate because these ring has a certain and not much depth in substrate.

Following subjects covers how to deal with isolation in a greater extend.

4.2.4 Deep n-well structure

Substrate noise caused by minority carrier injection into the substrate and well can be collected by the use of well taps and/or guard rings. An additional problem exists in that capacitive coupling of noise from the well to the substrate means more noise reaches the supply. In digital circuitry this is usually not a problem owing to the relatively high noise immunity of logic gates. However in analog design, for example a 12 bit ADC, noise can be a serious problem. A variety of techniques can be used to minimise this noise, for example by keeping analog devices surrounded by guard rings, or using a separate supply for the substrate/well taps. However guard rings alone cannot prevent noise coupling deep in the substrate, only surface currents [33].

Another problem is that it is not possible to isolate NMOS devices. So relatively noisy digital logic cannot be isolated completely from more sensitive analog areas.

A solution is to isolate the NMOS devices by using an extra well – a ‘deep N well’. So in Figure 4.8 the NMOS device is fabricated in a P well or substrate completely surrounded by an N type diffusion

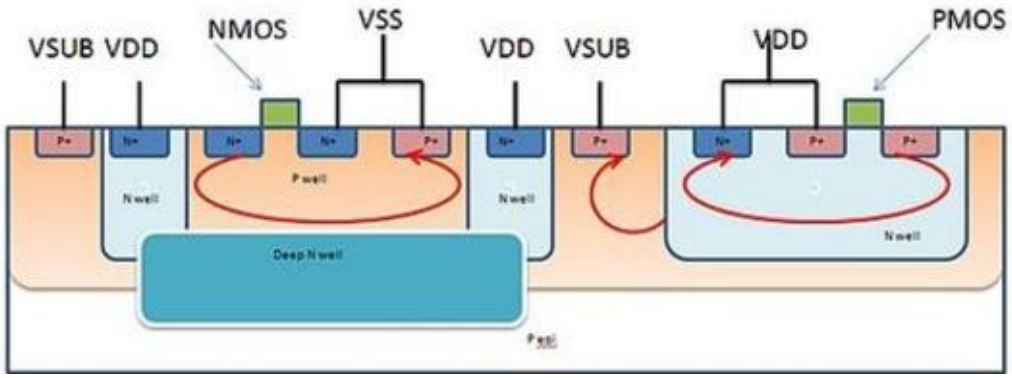


Figure 4.8 : A deep N well CMOS inverter cross section. Substrate noise currents are shown as red lines [33].

In this case, the deep N well is formed by a high energy ion implantation to give peak impurity concentration deep enough to un-affect the NMOS device performance. Connection to the deep N well is formed by a N well ring that is

connected to VDD. The deep N well has the effect of decreasing the noise coupling through it to the substrate and giving the advantage of fully isolated NMOS devices – which can in theory be at a different potential from ground.

The implications on layout are of course larger area for nmos devices due to the extra N well rings used to connect to the deep N well. However the noise performance improvements justify this for sensitive analog design.

Deep nwell isolation is also called Triple well isolation. Below is a summary of DNW isolation

- Used to isolate noisy NMOS devices.
- The MOS sits within a standard pwell doped silicon region, labeled as Pwell, and isolated from the rest of the P-type substrate.
- The isolation is the NW ring in contact with the DNW base which forms a barrier of N-type doped material.
- It is imperative the Pwell substrate is star-connected back to the ground pad and not connected to the local ground substrate. Doing this will effectively short out the DNW region and all noise isolation will be lost.
- It's also important to note DNW is an extra mask and therefore would incur extra cost.

In summary, the use of deep N well devices can significantly reduce noise coupling between sensitive analog areas and more noisy digital regions in mixed-signal designs.

4.2.5 Deep trench isolation

Deep trench Isolation uses a series of isolating trenches that bury deep into the IC substrate, Figure 4.9; effectively creating on-chip "pockets" where noise and power supply parameters are carefully controlled.

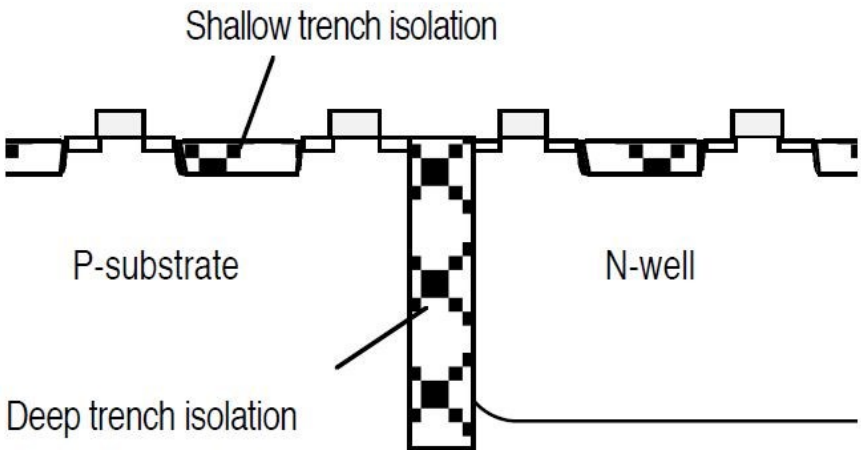


Figure 4.9 : Deep trench isolation [24].

Disadvantage of utilizing deep trench is it's area requirement. Design rule of deep trench is larger than having STI or guard rings. However, on top of its protection skills, the deep trench technology also helps to minimize die area by allowing dense packing of high-voltage analog pockets with low-voltage regions. You can obtain improvements in die area of 10 to 60 percent over designs that use standard junction isolation techniques.

Another drawback is added mask which means cost in production because deep trench isolation needs seperate mask to identify planned areas.

4.2.6 NT_N (native) layer (as known as moat isolation)

This layer is used for mask making rather than process requirements. It is defined as a non-PWell and a non-Nwell region. In other words, the area covered by NT_N will NOT get doped either P or N.

This is important to understand because typical CMOS design takes place on heavily doped P-Substrate (Psub). Heavily doped Psub has low resistivity. The reason being, Psub that is low in resistance will provide good latch up protection. The flip side to this is that it's bad for noise isolation [34].

However if we cover an area of Psub with NT_N, this area won't get doped and will therefore resemble intrinsic silicon

Intrinsic silicon by its very nature is highly resistive. It should also be noted the N_TN drawn layer adds no process cost and does not consist of an extra mask.

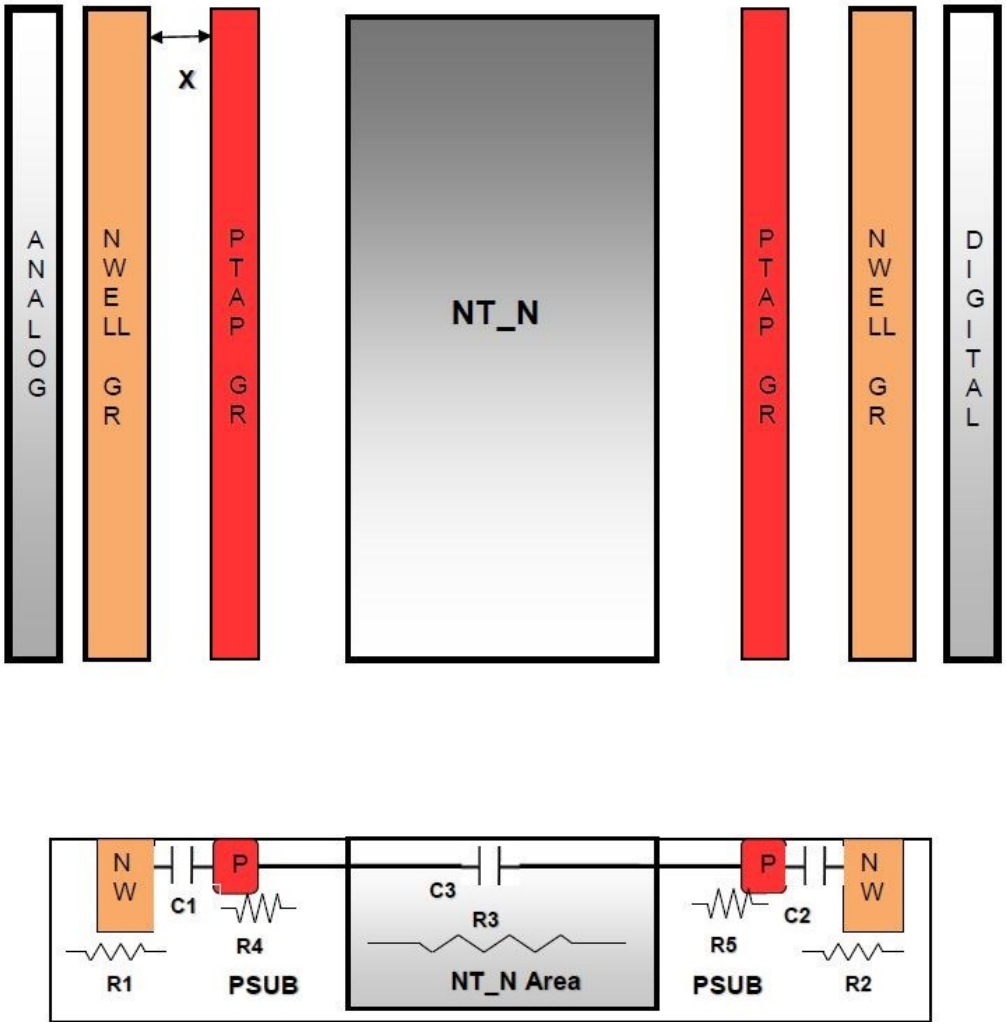


Figure 4.10 : Moat guard ring isolation (top) overview, (bottom) cross section [34].

Below is explanation of Moat guard ring theory with Figure 4.10:

- The Nwell guard rings are used to provide noise attenuation.
- However the worst case scenario is some noise will still get through.
- The Ptap guard rings placed beside the Nwell guard ring can now do their job and collect any stray noise.
- Capacitors C1&C2 provide an added benefit because they act as shorts at high frequencies. Therefore noise from the Nwell guard ring gets directed injected into the Ptap rings. This is an excellent added bonus in our noise isolation strategy.
- Again the worst case scenario would be the Ptap GR's don't get all the noise. Now the un-doped substrate comes into play.

- As we've said, intrinsic silicon is highly resistive and therefore provides excellent noise attenuation. Any stray noise at this point will be further dissipated .

Drawback of Moat guard ring configuration is that ring consumes a lot of space but provides one of the best isolation between analog and digital domains in same chip area.

5. ISSUES RELATING LAYOUT

As larger fabrication processes all dominant effects in layout were solved in different ways either in fabrication process change or layout techniques. However, technology nodes shrink in fabrication, some 2nd, 3rd effects in layout becomes dominant, this new effects damage design/layout and chip when fabricated. These effects are explained in following subjects.

5.1 Latch-up

If care is not taken when laying out CMOS circuits, the parasitic devices present can cause a condition known as latch-up.Parasitic devices are by nature of NMOS and PMOS structure are parasitic lateral NPN and vertical PNP bipolar transistor in CMOS. It can be best described in inverter design which basicly contains both NMOS and PMOS. Figure 5.1 show the cross-section of an inverter with its lateral NPN and vertical PNP bipolar transistor.

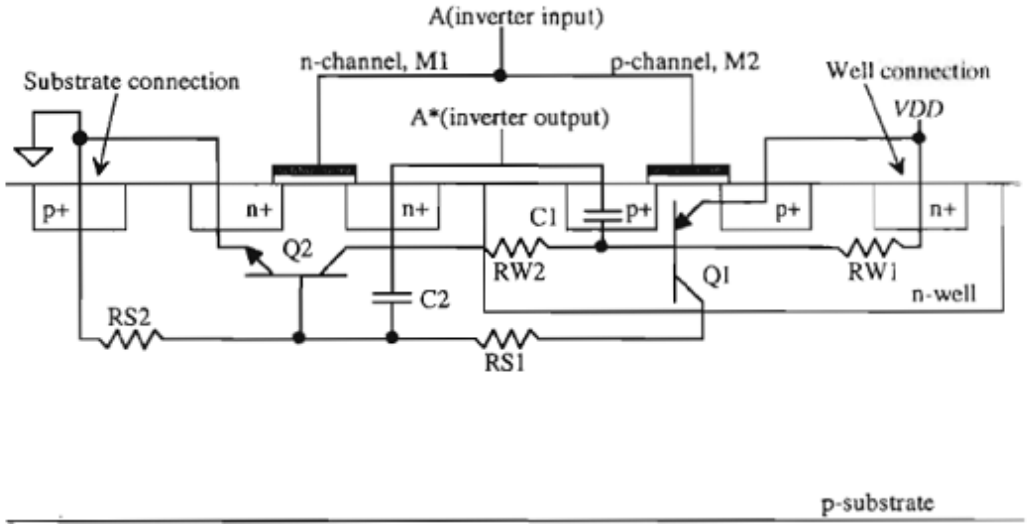


Figure 5.1 : Inverter cross-section showing lateral NPN and vertical PNP.

The parasitic structure is usually equivalent to a thyristor (or silicon controlled rectifier ”SCR”), a PNPN structure [36] which acts as a PNP and an NPN transistor

stacked next to each other. So, in some text books or other sources latch-up is called PNPN structure.

A Latch-up can be triggered in various ways:

- If there is a voltage at the input or output of a circuit that is more positive than the supply voltage, or more negative than the ground connection (or, to be precise, more negative than the connection to the substrate), current flows into the gate of the thyristor. If the amplitude and duration of the current are sufficient, the latch-up is triggered. The transit frequency of the parasitic transistors is only about 1 MHz. For this reason, overvoltages and undervoltages with durations of only a few nanoseconds, usually are not able to trigger the latch-up. However the probability that the latch-up might be triggered must be taken into account. This applies also at the interfaces between a circuit and the outside world; unacceptable overvoltages also often occur at this point.
- An electrostatic discharge can trigger the parasitic PNPN structure. Even if the electrostatic discharges have a duration of only a few tens of nanoseconds, when this happens, the complete chip may be flooded with charge carriers, which then flow away slowly, resulting in the triggering of latch-up.
- The parasitic thyristor can be triggered by a rapid rise of the supply voltage. This effect often was observed in earlier generations of CMOS circuits.
- Additionally, latch-up might be triggered by a high supply voltage – far higher than the value given in data sheets.
- Also, latch-up can be initiated by ionizing radiation. This is important with components that operate close to a source of high-energy radiation.

Figure 5.2 shows equivalent circuit of the SCR formed from parasitic bipolar transistors.

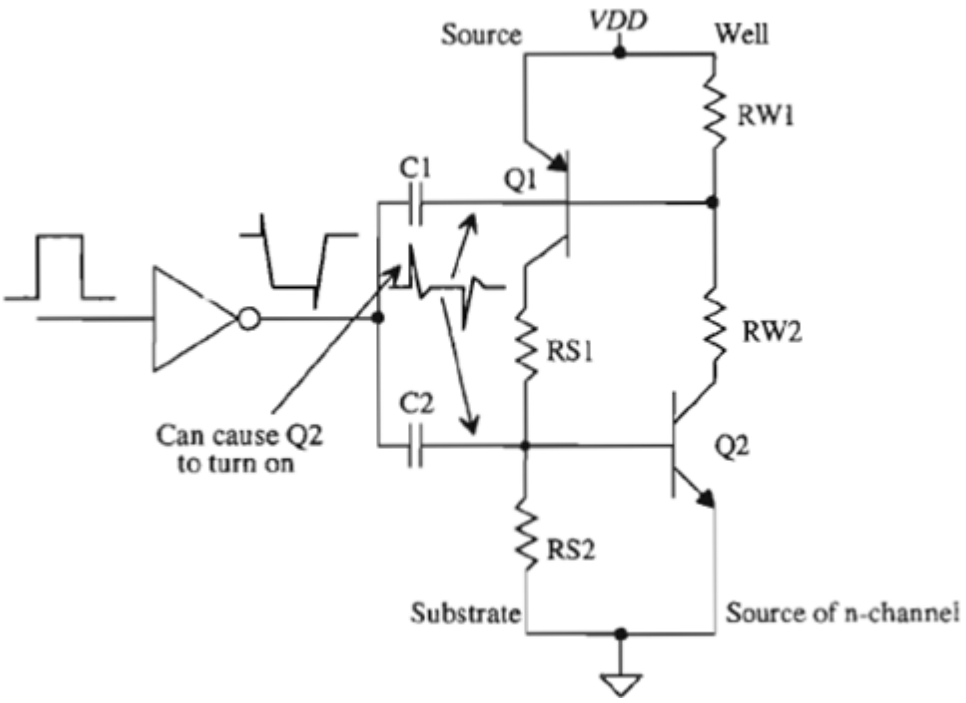


Figure 5.2 : Inverter cross-section showing lateral NPN and vertical PNP.

The emitter, base, and collector of transistor Ql are the source of the PMOS, n-well, and substrate, respectively. Transistor Q2's collector, base, and emitter are the n-well, substrate, and source of the NMOS transistor. Resistors RW1 and RW2 represent the effects of the resistance of the n-well, and resistors RSI and RS2 represent the resistance of the substrate. The capacitors Cl and C2 represent the drain implant depletion capacitance, that is, the capacitance between the drains of the transistors and the n-well (for Cl) and substrate (for C2).

If the output of the inverter switches fast enough, the pulse fed through C2 (for positive-going inputs) can cause the base-emitter junction of Q2 to become forward biased. This then causes the current through RW2 and RW1 to increase, turning on Ql. When Ql is turned on, the current through RSI and RS2 increases, causing Q2 to turn on harder. This positive feedback will eventually cause Q2 and Ql to turn on fully and remain that way until the power is removed and reapplied. A similar argument can be given for negative-going inputs feeding through Cl, VDD bouncing upwards, or ground bouncing downwards.

Method of reducing latch-up effects is to reduce the parasitic resistances RW1 and RS2. If these resistances are zero, Ql and Q2 never turn on. The value of these resistances, is a strong function of the distance between the well and substrate contacts. Simply put, the closer these contacts are to the MOSFETs used in the inverter, the less likely it is that the inverter will latch up. These contacts should be plentiful as well as close. Placing substrate and well contacts between the PMOS and NMOS devices provides a low-resistance connection to VDD and ground, significantly helping to reduce latchup. Placing guard rings between and/or around circuits reduces the amount of signal reaching a given circuit from another circuit.

Another method to minimaze latch-up risk is to increase RS1 and RW2 resistances. These resistances corresponds the distance between NMOS and PMOS device. To increase them, devices should be placed as far as possible but in a shrinking world trend in IC, this is practically impossible.

5.2 Well Proximity Effect (WPE)

An NWell is formed by bombarding the wafer with N+ dopants. Photo-resist controls these dopants to only implant the areas which should become NWell, any area not doped will become PWell. However due to an effect known as scattering, the edges of an NWell tend to become more heavily doped than the centre, this scattering also causes light N+ doping to spill into the PWell regions directly adjacent to NWell Figure 5.3. The result is that in these boundary regions, neither the NWell or PWell characteristics are exactly as required. Figure 5.4. Design rules are defined to help place devices away from these areas of maximum deviation to minimise the effect that well variation has on transistor performance. Nevertheless to minimise the effect of well variation in critically matched devices it is important that the whole array is as far from a well edge as practical [37-39].

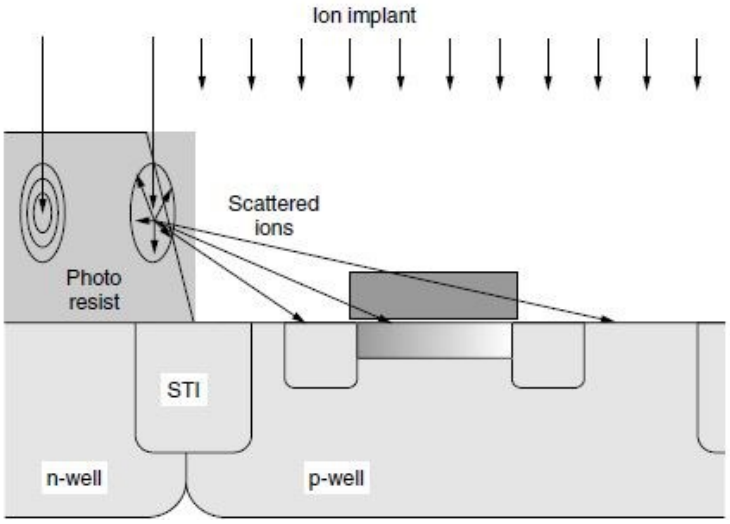


Figure 5.3 : Scattering ions at the edge of Nwell region.

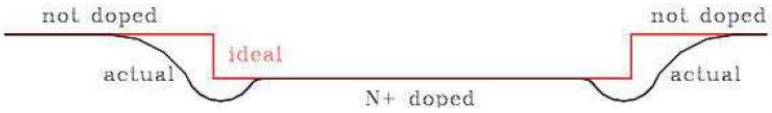


Figure 5.4 : Doping concentration of scattered ions.

bulk doping concentration is one of the key physical parameters than controls the operation of MOS transistors. Therefore it should be apparent that the proximity of a transistor to a well edge, which changes its bulk doping, can affect its behavior significantly. Prior to about the 0.25 µm technology node the overall size of transistors meant they could not be placed close enough to a well edge for the enhanced doping level to affect their behavior. For technology nodes below that WPE has become an important issue

WPE can effect threshold voltage of MOSFETs around 50mV-90mV which might be critical for sensitive circuits. In order to minimize WPE , NMOS and PMOS devices should be placed more than 2µ further away from the nwell edge.

5.3 STI Proximity Effect/Length of Diffusion (LOD)

STI (shallow trench isolation) is the oxide formed wherever diffusion is absent, the isolation between diffusions, its creation causes a mechanical stress to the gate poly edge of a transistor in direct proportion to its distance from it, LOD (length of diffusion), the greater the distance the less the effect. The LOD on one side of a transistor is “SA”, on the other side “SB”. Values for SA, SB and the STI effect are calculated at schematic entry as a function of the parameters “multiplicity” and

"number of fingers" and added to the simulation data. Layout deviation from the schematic defined parameters will change these values and hence the circuit performance. Figure 5.5 shows LOD and SA/SB parameters for each finger.

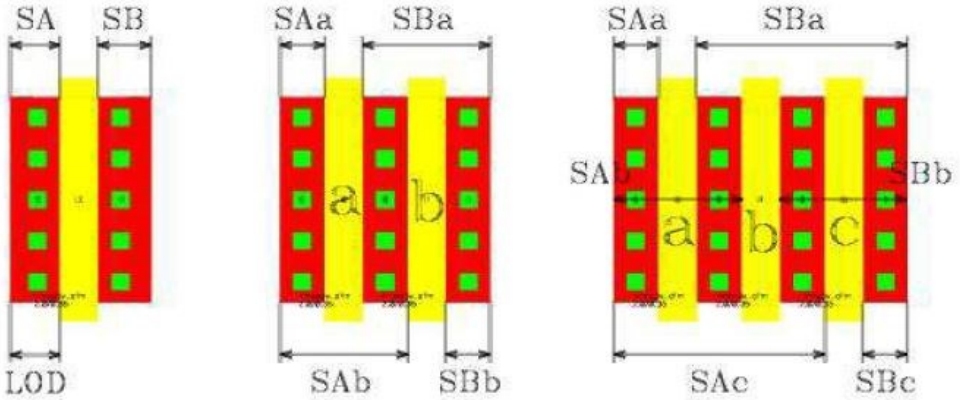


Figure 5.5 : SA and SB representation in MOSFET.

Due to the different thermal expansion coefficients between Si and STI (which is SiO_2), there exists biaxial compressive residual stress in the active region after processing, Figure 5.6. STI-stress generally increases PMOS current and decreases NMOS current, Figure 5.7. Stress relaxes exponentially with increased distance from Si/STI boundary.

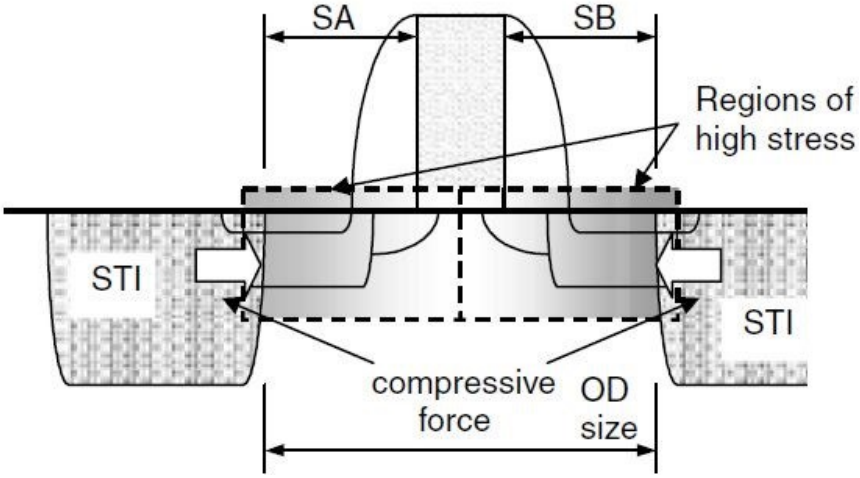


Figure 5.6 : STI stress in cross-sectional view.

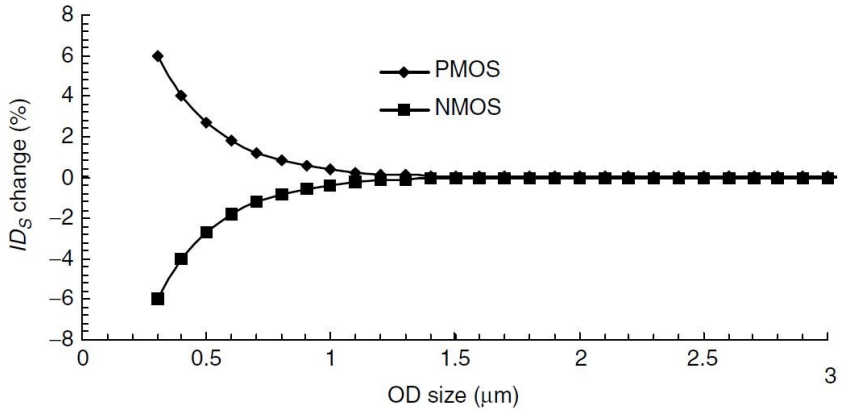


Figure 5.7 : $I_{d\ sat}$ variation for an advanced process (0.13μm and beyond).

5.4 Antenna Effect

Antenna effect or "plasma induced gate oxide damage" is a manufacturing effect. This is a type of failure that can occur solely at the manufacturing stage. This is a gate damage that can occur due to charge accumulation on metals and discharge to a gate through gate oxide.

In the manufacturing process, metals are built layer by layer. First, metal1 is deposited, then all unwanted portions are etched away, with plasma etching. The metal geometries when they are exposed to plasma can collect charge from it. Once metal1 is completed, via1 is built, then metal2 and so on. So with each passing stage, the metal geometries can build up static electricity. The larger the metal area that is exposed to the plasma, the more charge they can collect. If the charge collected is large enough to cause current to flow to the gate, this can cause damage to the gate oxide. This happens especially in long metal lines connected to gate. This failure impacts fabrication yield. Thus should be taken precautions in layout.

There are two ways to prevent antenna effect. One is creating a metal bridge (jumper) near gate of MOS device so that while fabrication, metal connencting to gate will be small but the rest of the long metal line is after the jumper. This jumper should be done to the highest metal allowed in fabrication Figure 5.8 shows the implementation of a jumper.

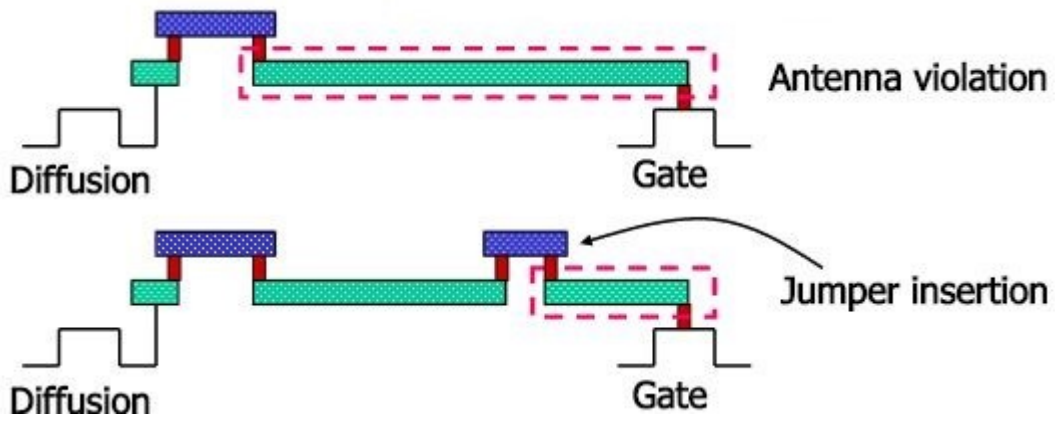


Figure 5.8 : Antenna violation and jumper insertion [40].

Second way of prevention is to place a reverse biased diode near gate. Using diode provides a discharge path to the substrate by contact to a diffusion area. If possible, connect this diode to gate with metal1 so that prevention starts right with metal1 fabrication. During normal operation this reverse biased diode will not effect functionality, Figure 5.9.

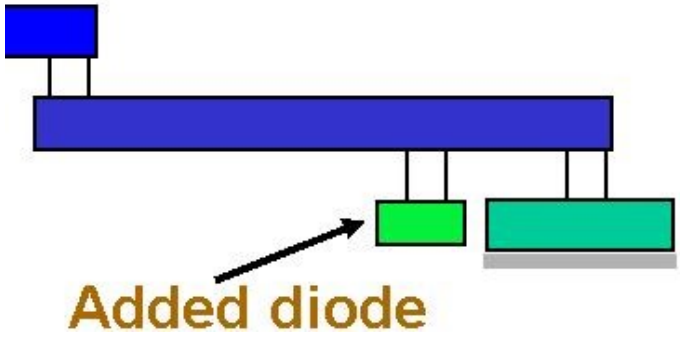


Figure 5.9 : Diode insertion to prevent Antenna effect.

6. MATCHING IN LAYOUT

Mismatch is an effect that arises in IC fabrication and is a limiting factor of the accuracy and reliability of many analog and digital integrated circuits. Due to mismatch two equally designed (drawn) transistors display different electrical behavior due to mismatch. The main reason for the differences is the non-uniformity of process parameters across the wafer. Mismatch affects electrical parameters of the transistor, which in turn differ between two identically drawn devices. Consequently the operating point and other circuit characteristics differ from their desired values [41-44].

Mismatch in a certain component can be defined as the variation in the value of identically designed components. Mismatch can be divided into two categories: random and systematic. Systematic mismatch is that part of the total mismatch where a deterministic trend can be observed in the mismatch values of the various transistors. The remainder of the mismatch, in which no apparent trend is observed, falls under the category of random mismatch [45].

Mismatch types are lot-to-lot, wafet to wafer, die to die, and device to device. Extensive research are done to understand and minimize all of these kind of mismatchs.

Mismatch has a gaussian distribution behaviour, so Figure 6.1 and Figure 6.2 will help to better understand the systematic and random mismatch difference and their behaviour.

Systematic mismatches caused by process biases, contact resistances, nonuniform current flow, diffusion interactions, mechanical stresses, temperature gradients. Systematic mismatches are generally occurred in schematic design and layout design. Can usually be avoided or minimized by good design and good layout practice.

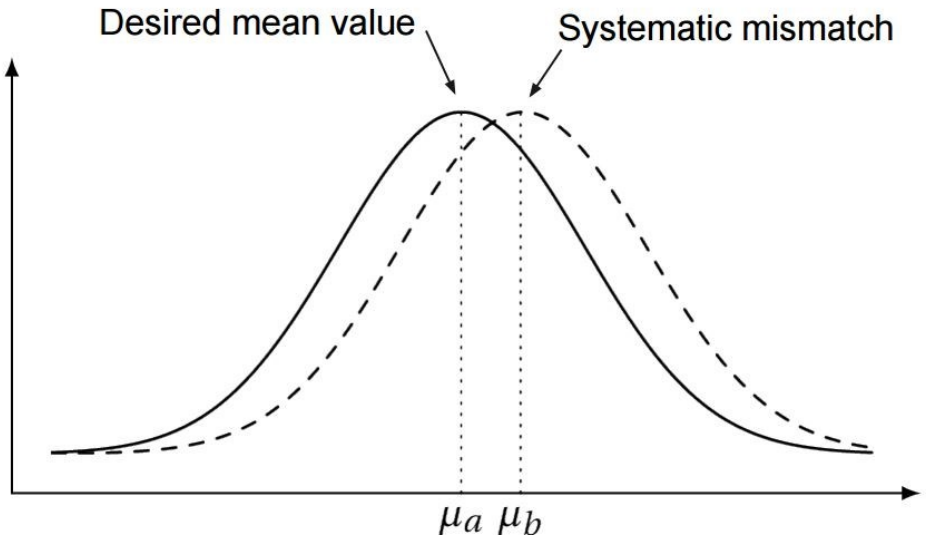


Figure 6.1 : Systematic mismatch behaviour representation.

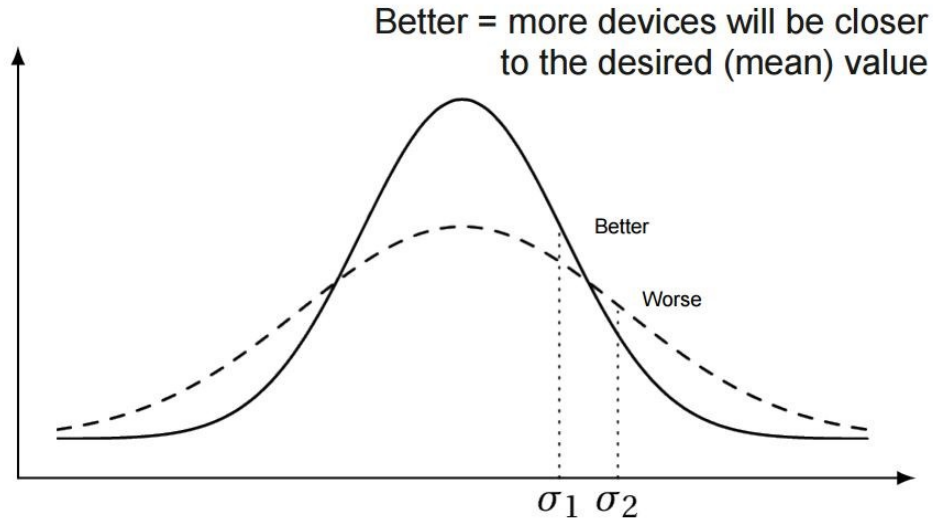


Figure 6.2 : Random mismatch behaviour.

Fluctuations in dimensions, dopings, oxide thicknesses and other parameters that influence component values result in random mismatch Examples of random mismatch are device length, channel doping, oxide thickness, sheet resistance, capacitance. Good layout practice can minimize these mismatch in greater extend.

.

6.1 Matching Techniques in Layout

As explained before to reduce and minimize the systematic and random mismatches matching techniques should be applied. These techniques are applicable to MOSFET's and passive devices like resistors, capacitors etc [45-59].

Below are subjects that defines matching when all of them taken care of. Thus, applying all these criterias are important to achieve close to perfect layout.

- Orientation of devices
- Placement of devices, location
- Unit size device usage
- Dummy device usage
- Routing Symmetry
- Symmetrical Placement
    - Interdigitation
    - Common-Centroid
    - 1-D Symmetry placement
    - 2-D Symmetry placement

Now, all these sub-subjects will be explained.

6.2 Orientation of Devices

Different oriented MOSFETs that like in Figure 6.3, will have mismatch due to crytalline structure difference. This different crystalline structure effects the transconductance of MOS transistors which depend on carrier mobilities and these in turn exhibit orientation-dependent stress sensitivity.

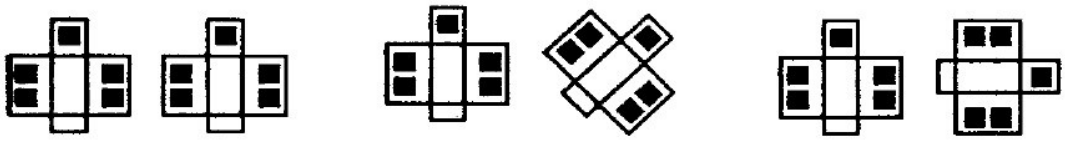


Figure 6.3 : Orientation of devices [7].

The first MOSFETs appeared in Figure 6.3 has same orientation compared to others. Second one has one placed vertically the other placed 45^0 angle. The last placement has one vertical and one horizontal device. Current flow of these three examples are: 1) from one side to other which means horizontal current flow. 2) in modern fabrication processes rotated mosfets are not supported so even it is wanted to placed like tilted, process will not allow. 3) Current flow is horizontal in first and vertical in second placement. Thus, if a sensitive matching is needed, this misoriented placement will create mismatch.

Orientation is not only placing all matching needed devices in vertical or horizontal position but also making current direction of vertically or horizontally placed devices same. Imagine there are two vertically placed transistors exist but the direction of current flow is different. In one transistor it is from right to left, the other is from left to right. This difference also effects matching, so current directions of matched devices should be in same direction as much as possible.

6.3 Placement (Location) of Devices

Placement of devices are also critical to achieve matching. Devices that need matching should see gradient effects as same as possible. These gradient effects can be thermal gradient or stress gradient. Figure 6.4 shows an example.

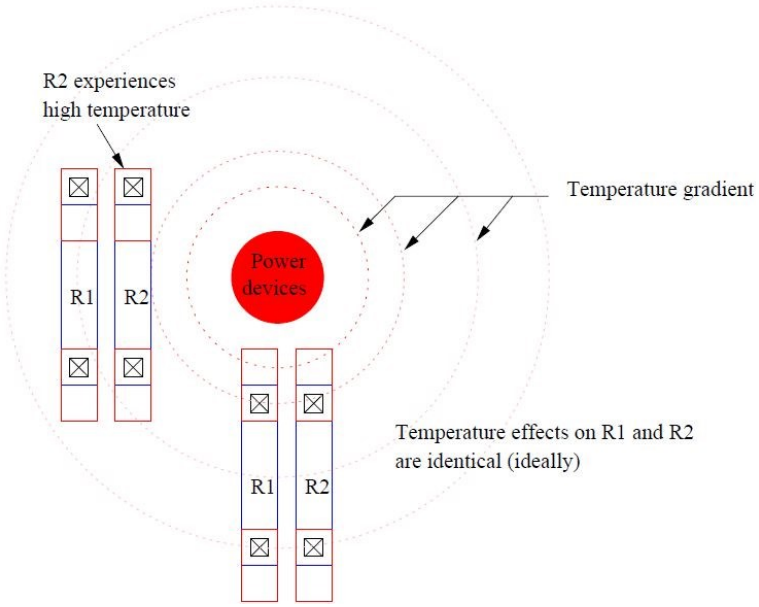


Figure 6.4 : Temperature gradient and mismatch on devices [10].

In addditon to Figure 6.4, the input and output of devices should be in same environment or at least if they are differential pair, inputs and outputs of two differential nets should be close to each other and should be in the same environment (Figure 6.5).

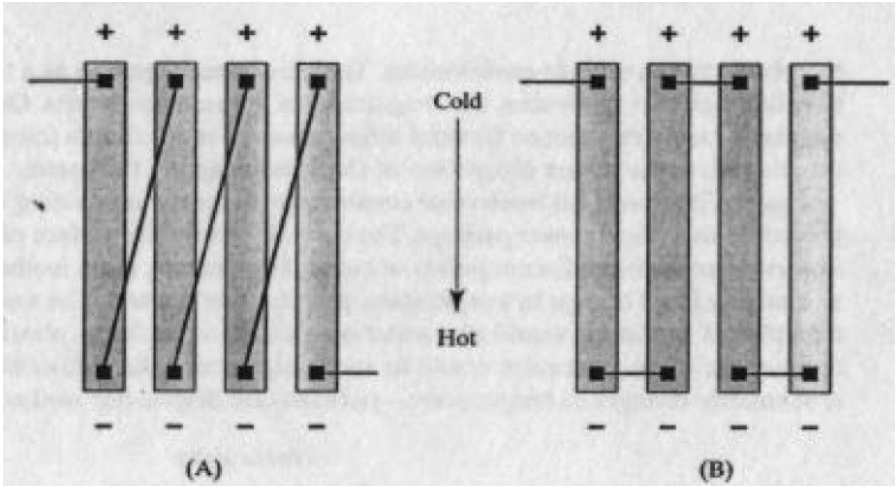


Figure 6.5 : Input-output difference [7].

In Figure 6.5, first resistor will see thermal difference between its input and output due to placed in different thermal area. Second resistor have input and output in same thermal area so will have better matching.

Stress distribution varies over the die, so matched devices should placed as close as possible to minimize the difference in stresses between them. Thus, devices will see similar stress effects on them.

6.4 Unit Size Device Usage

Large transistors or passive devices match more precisely than small ones. On the other hand, large or very large devices are not desired depending on design requirement. In addition, some devices might not be same size but requires matching.

In order to achieve better matching, a unit size should be decided to use for all different size devices. So that, they can be build up with more than one but same size devices.

For example, assume we need to match two current mirror transistors with different sizes. One has W=20µ/L=2µ and the other, diode connected one has W=2µ/L=2µ. If these transistor laid out as one instance than one will be bigger than the other which create mismatch in its current branch. A unit size should be found and applied for

both of transistors to achieve same size for all of them. Unit size can be chosen as W=2µ/L=2µ. In this particular example, diode connected transistor will have one unit device while the other one will have ten unit device of W=2µ/L=2µ. These 10 unit device in paralel to each other will create the W=20µ/L=2µ device. Eleven instances will be used to layout this current mirror.

Dividing both matched devices into segments of the same size will help to avoid mismatch caused by process biases. In other words, make your devices in unit size and reach your desired value by adding more unit size of device. This is applicable to all transistors and passive devices.

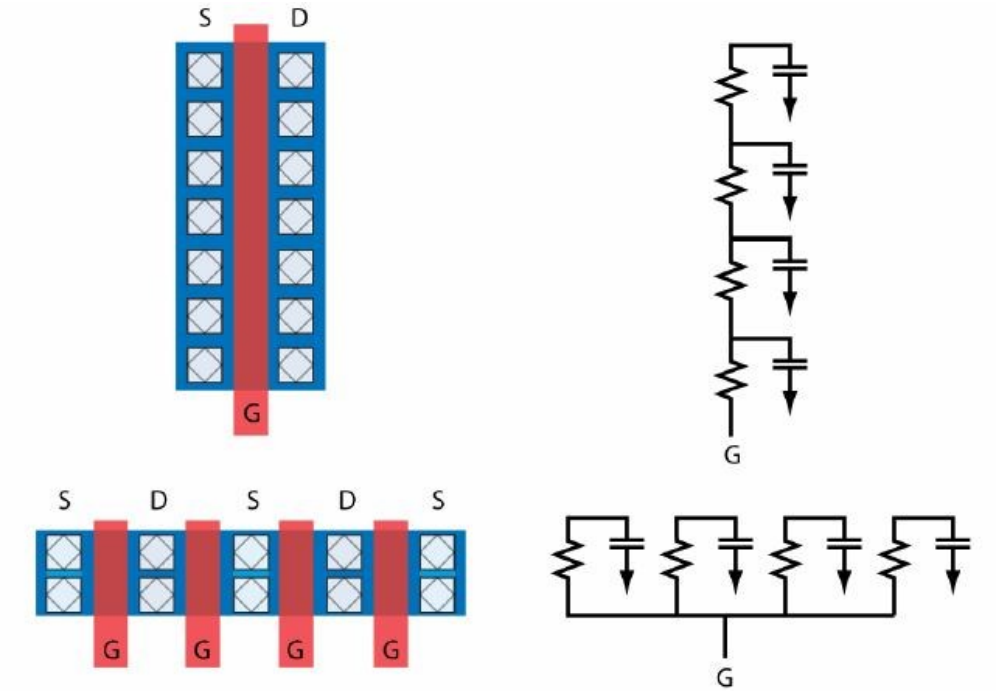


Figure 6.6 : Breaking a device into unit sizes.

Breaking a device into unit sizes also benefits to share drain and sources. So that parasitic capacitance of drain and sources can be reduces significantly. This also reduces the parasitic gate resistance as shown in Figure 6.6.

Usage of unit device will also benefit us to place them in a more matched arrays to minimize any kind of gradient effects. These will be explained in Symmetry section.

6.5 Dummy Device Usage

In fabrication process, devices will get different etch rate which results in different device which should be matched. Especially, etch difference creates different values for two closely placed transistor or passive device.

If etchant have free space, it will etch more than etching an opening that has limited space. Imagine we placed three resistors next to each other, the outer edges of the resistors have free space that etchant can etch more resulting in overetching while inner opening between two resistor has more limited space for etchant to etch away.

By placing dummy devices at the end of array of devices, we create a uniform etching both inside and outer edges of devices. Overetching will effect the dummy devices but as name implies, they are placed as not a part of design itself but protection for matched devices. Dummy will be effect while they don't have any purpose to serve design it is not important. The spacing between dummy and actual devices should be equal to the spacing between the array of devices, Figure 6.7.

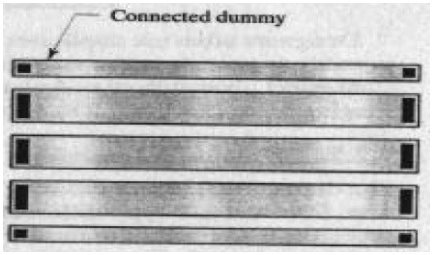


Figure 6.7 : Dummy resistors at the edges of array [7].

In other words, to get a better matching environment of matched devices should be as same as possible. This can be done by adding as much dummy device as possible on matched devices. This means adding dummies to right and left side of matched devices migt not be enough so add dummies on top and bottom of device array to get a better same environment. Drawback of placing dummies on four sides is consumed area which means bigger layout. Careful thinking must be done whether 4 side of dummies are actually needed or just 2 side of dummies is enough to achieve desired matching.

6.6 Routing Symmetry

Matched decives should have as similar routing as possible inside matched devices, input/output of matched devices and if possible same routing along the chip (Figure 6.8). Metal routing over critically matched resistors will influence the stress on the devices and capacitively couple noise into devices.

In addition to these, electric field will modulate the conductivity of the resistance material (called conductivity modulation). If it is a must to route over the critically matched devices, instead of using first level of metal layer routing, second or more level of metal layer should be used. This will reduce the electrical field and reduce the conductivity modulation. Same applies to matched MIM caps. If routing is needed under MIM caps, it should be on lower metals to reduce coupling to capacitors, or a shielding layer should be added on top of routing channel.

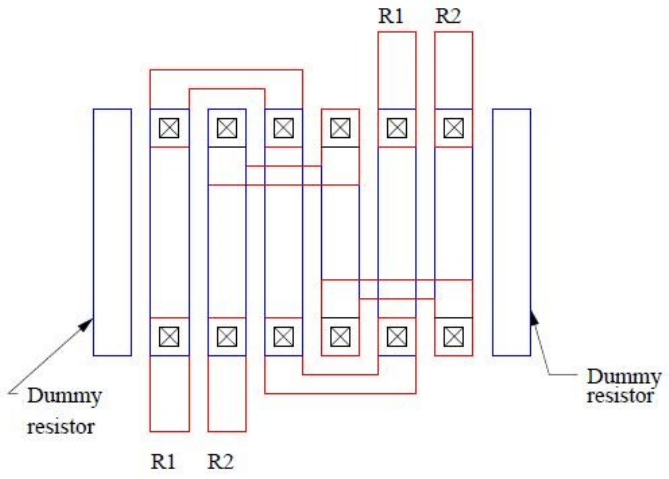


Figure 6.8 : Layout of matched resistors.

6.7 Symmetrical Placement

Symmetrical placement of devices, especially using unit devices are one of the most important feature to create matching. Symmetrical placement can be achieved in many ways. These techniques are:

- Interdigitation
- Common centroid
- 1-D Symmetry

- 2-D Symmetry

Interdigitation is a way to spread two different devices using unit devices into each other. Imagine we call one mosfet as A and other is B. Interdigitation is laying out A and B unit devices one next to other: Like following:

ABAB BABA ABBA BAAB

Assuming we need more than 2 devices to layout then it can be

ABCABC ACBACB CABCAB ABCCBA

All above placements uses interdigitation.

Common-Centroid technique is making all A,B and C unit device devices in the same axis of symmetry. So that all devices will have same center for the symmetry.

Different placements can be:

ABC|CBA CAB|BAC BCA|ACB

But in ABCABC configuration, they are interdigitated but not have same central symmetry. $AB|_AC|_BA|_CBC$ centre symmetry of all A,B and C devices are shown as "$|_X$" and they are not coincide with each other.

1-D Symmetry is actually used in both interdigitation and common-centroid. It is a way to layout these unit devices in only one row like ABCABC (interdigitation) or ABCCBA (interdigitation & common-centroid). This can be feasible if matching needed devices are small in number and do not be placed too far away from each other. 1-D Symmetry does not mean common centroid but common-centroid also includes 1-D symmetry by its nature

Figure 6.9 : 1-D symmetry layout structures [54]

(a) in Figure 6.9 is the very basic structure while (b) has more device that are laid out in one row. Note that centroid of device 1 and centroid of device 2 share same common point which makes than common-centroid too.

On the other hand, some designs might need to utilize many devices themselves or many unit devices of actual devices. In that case 1-D symmetry layout can be too long even it is done in interdigitation and common-centroid.

2-D Symmetry comes handy in these situations where laying out in a one row will be too long and not feasible.

Figure 6.10 : 2-D symmetry examples [54].

Figure 6.10 shows a simple version of 2-D symmetry layout. This kind of layout structure is the most useful one because it eliminates gradient factors in every direction. More complex version of 2-D symmetry is in Figure 6.11. Notice that (a) and (b) of Figure 6.11 are interdigitated when 1 row is considered and have common centroid of both device 1 and device 2. This kind of structure is one of the best to layout but structure increases the

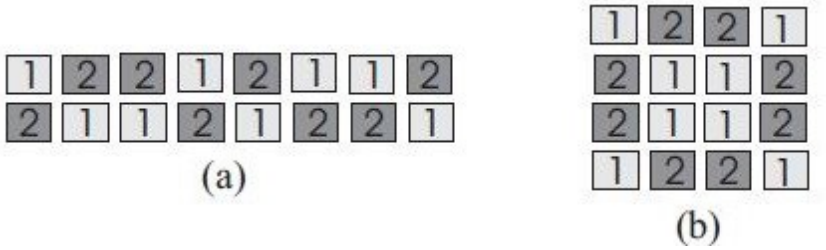


Figure 6.11 : Complex 2-D layout structures [54]

2-D symmetry is also called quadratic common centroid if it has square shape or just common centroid but common-centroid term has a general meaning than saying 2-D symmetry. If devices are too much to place only by two row, they can be placed as 3 row or 4 row like (b) on the right in Figure 6.10.

Structures explained above can be used for any device in the chip. FETs, resistors, capacitors or any other kinds.

7. LAYOUTS OF ADAPTIVE OUTPUT BUCK CONVERTER BLOCKS

All these layout techniques are applied to an adaptive output stage buck converter. This section will briefly explain the analog blocks and pass device and demonstrate designed layouts in detail. System level schematic representation of adaptive output stage buck converter is shown in Figure 7.1.

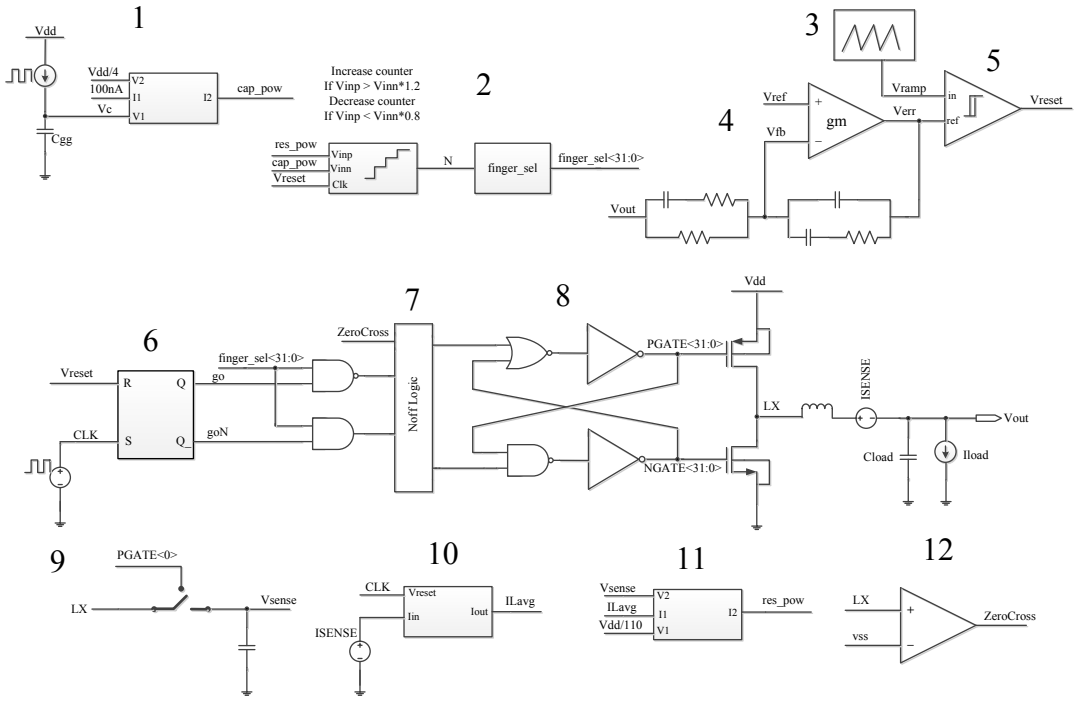


Figure 7.1 : Adaptive output buck converter system model [60].

The system level setup is composed of an adaptive capacitive gm block, a current comparator, a ramp generator, an error amplifier with its compensation network, a PWM latched comparator, a SR Flip Flop (SRFF), a N_{off} Logic, an adaptive stage pre-driver and driver, a vSense sample and hold circuit, a current sense block, an adaptive resistive gm block, and an active diode comparator.

All these blocks are explained very briefly in terms of analog design point. However, layouts of all of them will be presented in a detailed way.

1st block is adaptive capacitive gm block which generates the capacitive current.

Number 2 is current comparator and implemented by using Verilog A code which is digital not analog so will not be explained in terms of layout.

3rd block is ramp generator.

4th block is error amplifier and compensation network.

5th block is PWM comparator.

6th component is SRFF block.

N_{off} Logic is number 7th component.

Adaptive output stage pre-driver is number 8th component.

vSense sample and hold circuit is number 9th .

10th block is the output current sense block.

11th block is adaptive resistive gm block.

12th block is the active diode comparator also known as zero cross comparator block

7.1 Adaptive Capacitive G_m and Adaptive Resistive G_m blocks

These two block serve to calculate the capacitive and resistive power losses of the switching converter. Then compares to find the optimum output stage size. Schematic of Adaptive capacitive Gm block is shown in Figure 7.2

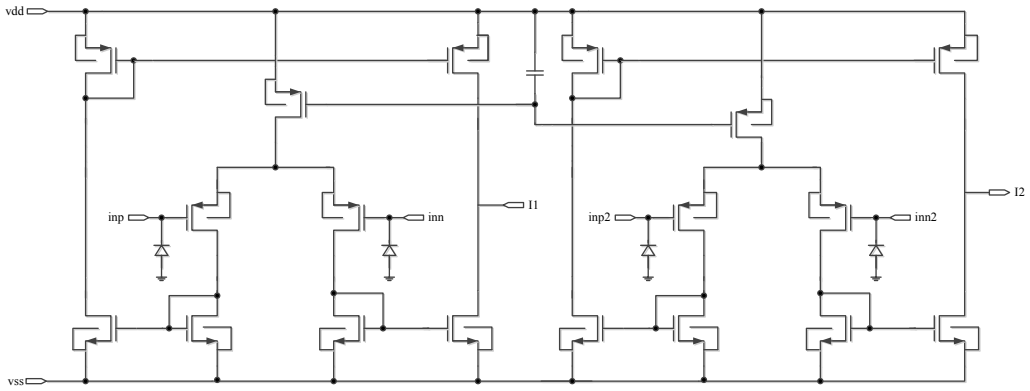


Figure 7.2 : Adaptive Capacitive g_m schematic [60]

An overall layout of adaptive capacitive Gm is shown in Figure 7.3. Later on, detailed layout snapshots and their explanations will be given.

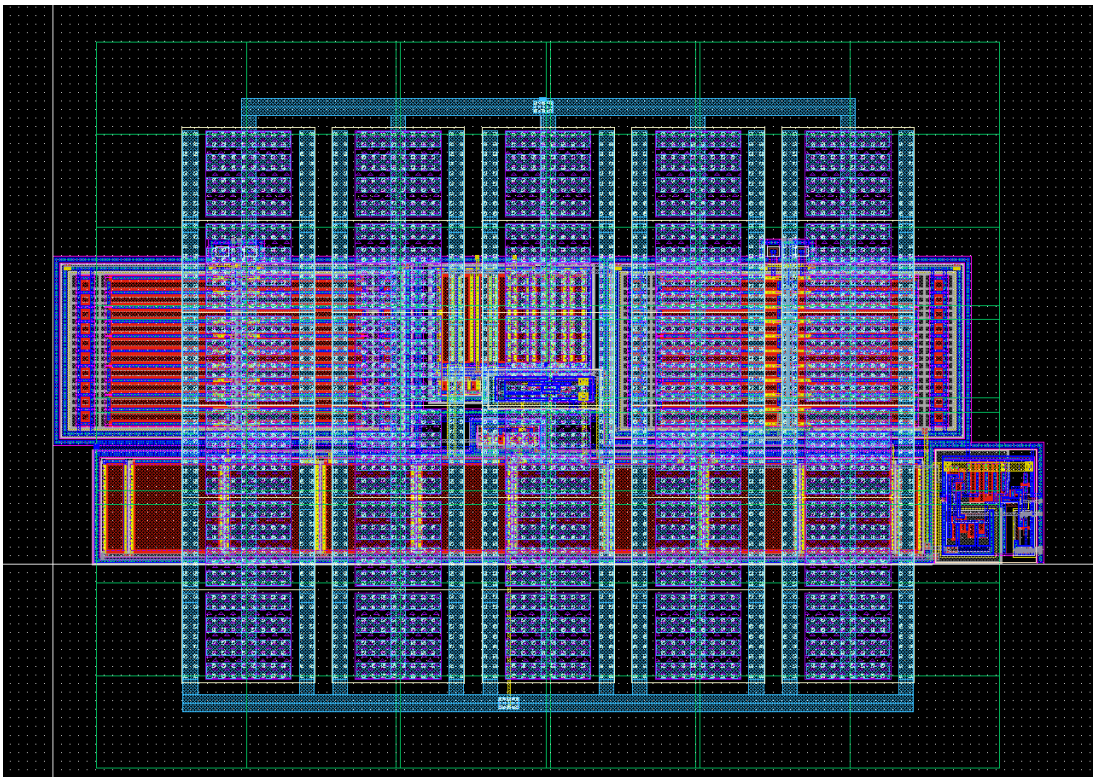


Figure 7.3 : Overall layout of Adaptive Capacitive Gm block.

A simplified layout snapshot is in Figure 7.4. In this picture, MIM caps are turned off to see the circutry under them. Two differential PMOS block is highlighted on right and left side in layout block. In the middle PMOS current mirrors placed and below that differential pairs' tail current PMOS is placed. At bottom, NMOS current mirrors placed as closed as possible.between NMOS current block and PMOS current block NMOS cascode transistors instentiated. On the very left side, logic block is placed which its connections are digital so placement of digital block is less important than analog blocks.

Note that all differential pairs and current mirrors regardless of transistor types have dummy transistors on both edges. Since cascode and tail current transistors do not need matching, they don't have dummies.

In Figure 7.5, differential input pairs zoomed more to analyse in detail. The distance between dummy and actual transistor is as same as between two transistors. Also, nwell guard ring is circulating all around differential pair, then substrate ring (noted as ptap guard ring) is around the block. To connect antenna diodes which are to prevent antenna effect in fabrication, in metal 1 nwell guard ring and substrate guard ring cut enough to allow connection to diodes.

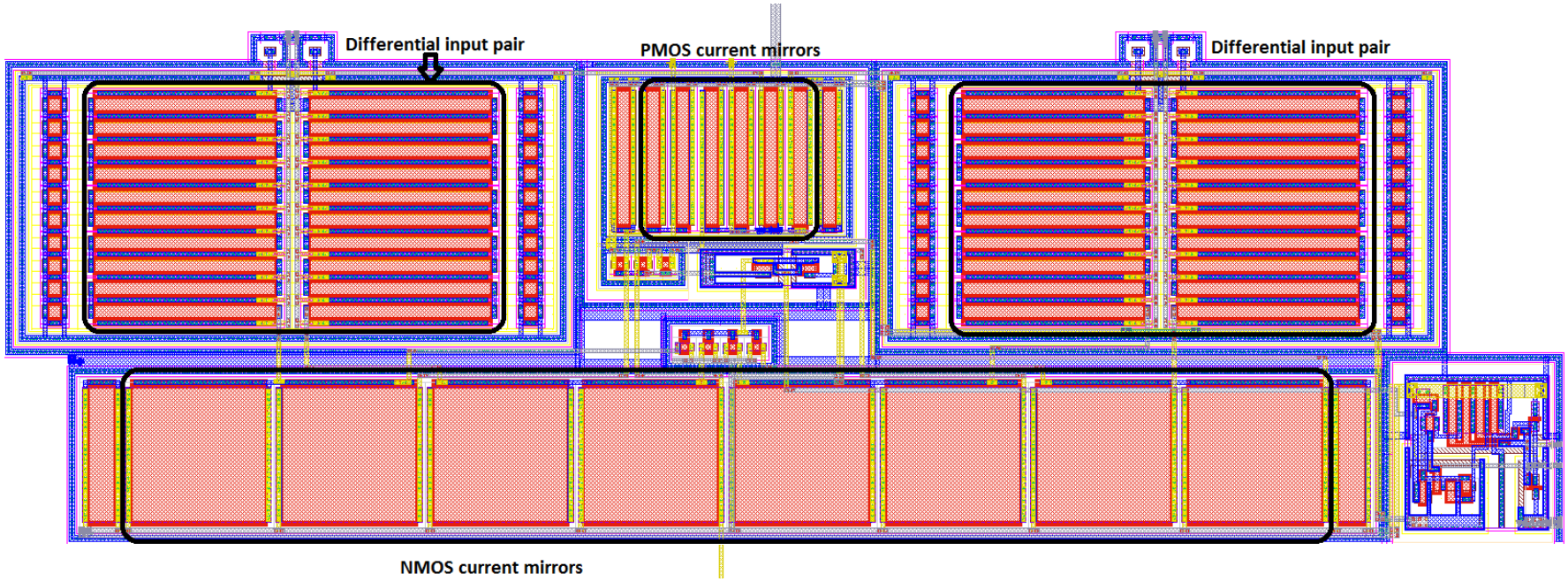


Figure 7.4 : Simplified Layout of Adaptive Capacitive Gm block

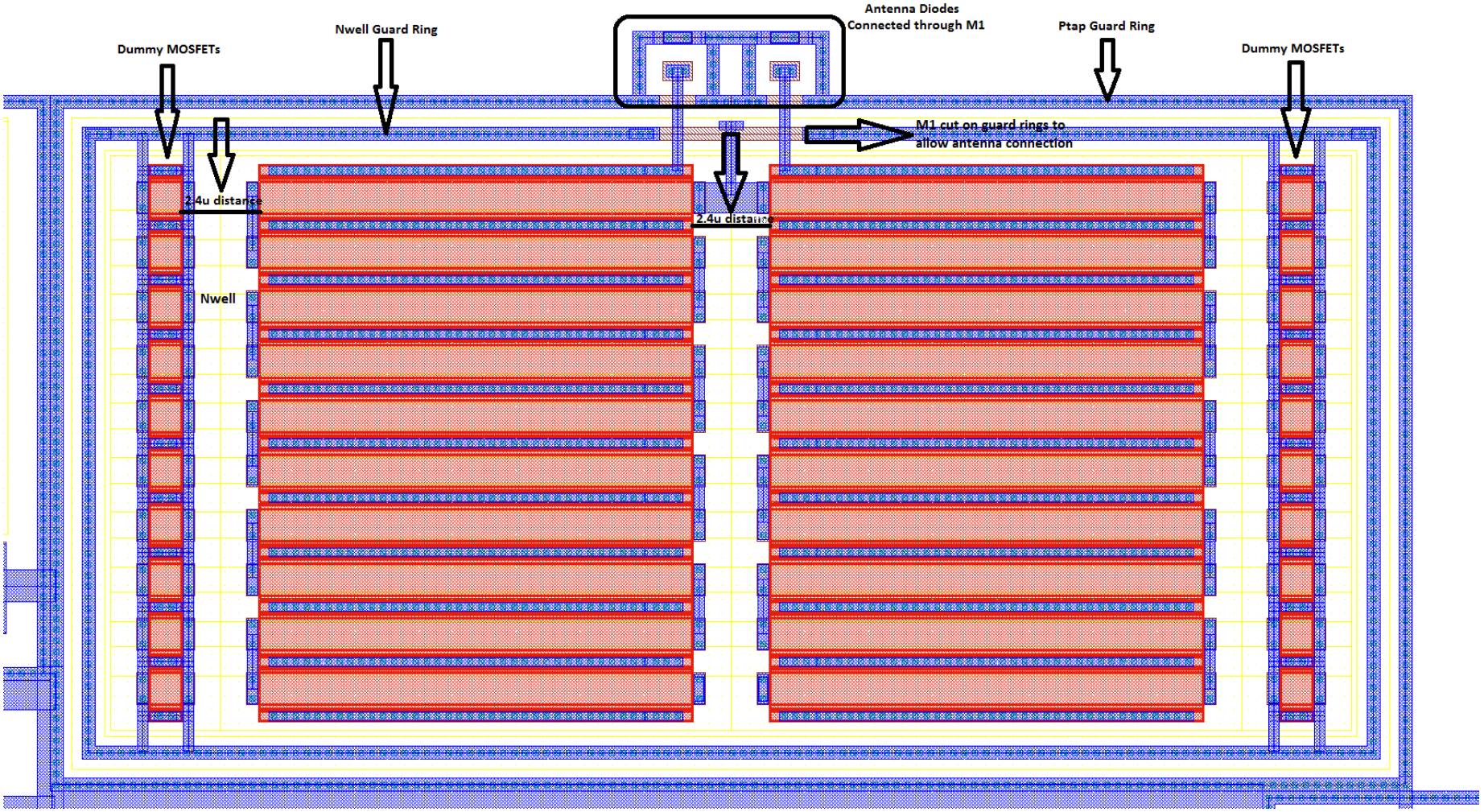


Figure 7.5 : Differential input pairs with detailed explanation.

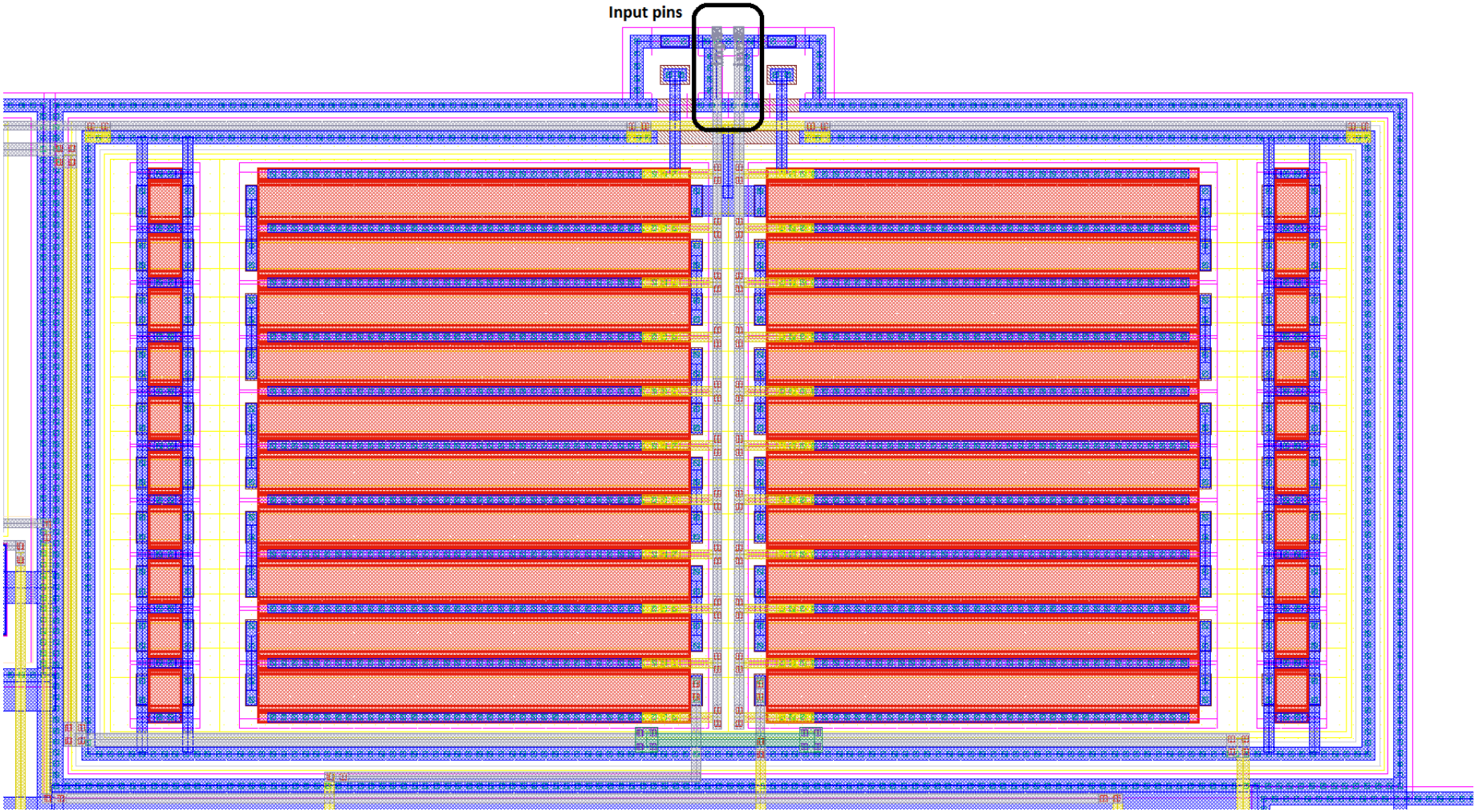


Figure 7.6 : Layout with metal routing connections.

To see differential block's metal routings, Figure 7.6 is shown. In this figure, input pins are located on top of block and output nets are on bottom. Metal 1 is used in everywhere for transistors themselves and guard rings. Thus, routing of nets can not be possible by metal 1. Metal 2 and metal 3 is used to connect nets between transistors and other devices (passive devices). Metal 2 is selected for vertical routing and Metal 3 is used mainly for horizontal routing. Very small routings are exceptional to this rule. This strategy of routing is to ease the block's routing in general also this will help wiring on higher level in integrating other blocks too.

Moving on to the adaptive resistive gm circuit, schematic structure is very similar as shown in Figure 7.7 but structure is upside down. So layout is also laid out similarly.

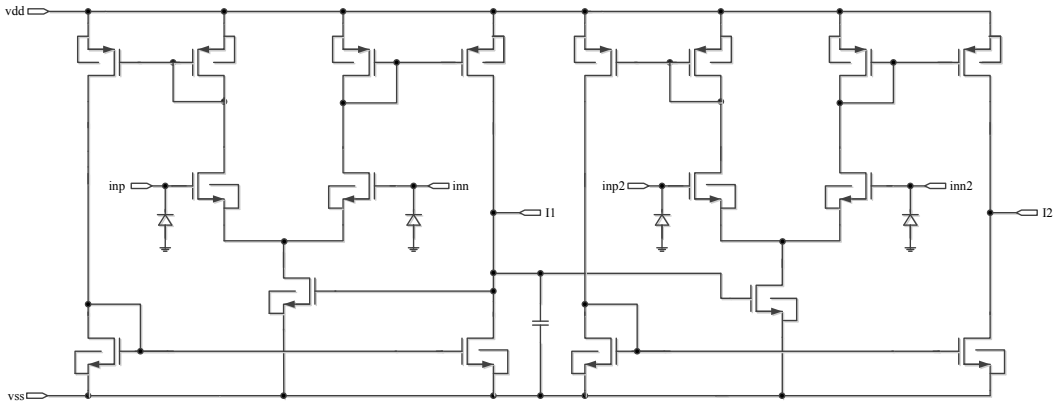


Figure 7.7 : Schematic of adaptive resistive g_m circuit [60]

Overall layout can be seen in Figure 7.8 with MIM caps on top of circutry. On top, PMOS transistor block is placed and at bottom, NMOS block is placed. On the left, logic circutry is placed.

In Figure 7.9, MIM capacitors turned off to see the circuit more clear. Dummy transistors are highlighted at both ends of differential pairs and current mirrors. In addition to this, antenna diodes placed in schematic can be seen on both ends. Notice that antenna diodes are placed as close as possible to differential pairs through metal 1 routing. To see MIM capacitor block, other layers are turned off in Figure 7.10. MIM capacitor have 2 ports and in layout one output is on the left and the other is on right. All these MIM capacitors are placed as closed as possible that DRC allows.

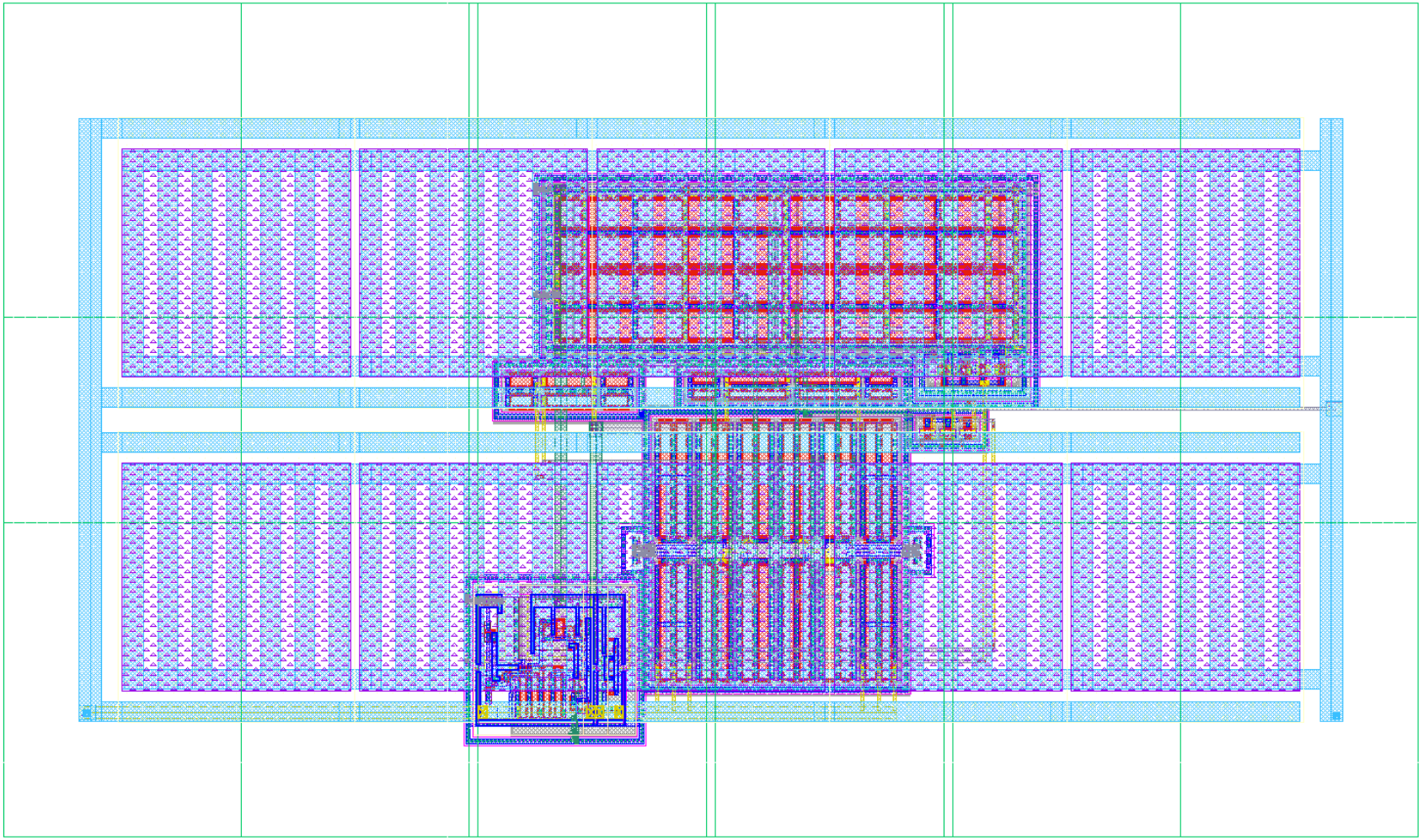


Figure 7.8 : Overall layout of adaptive resistive g_m block.

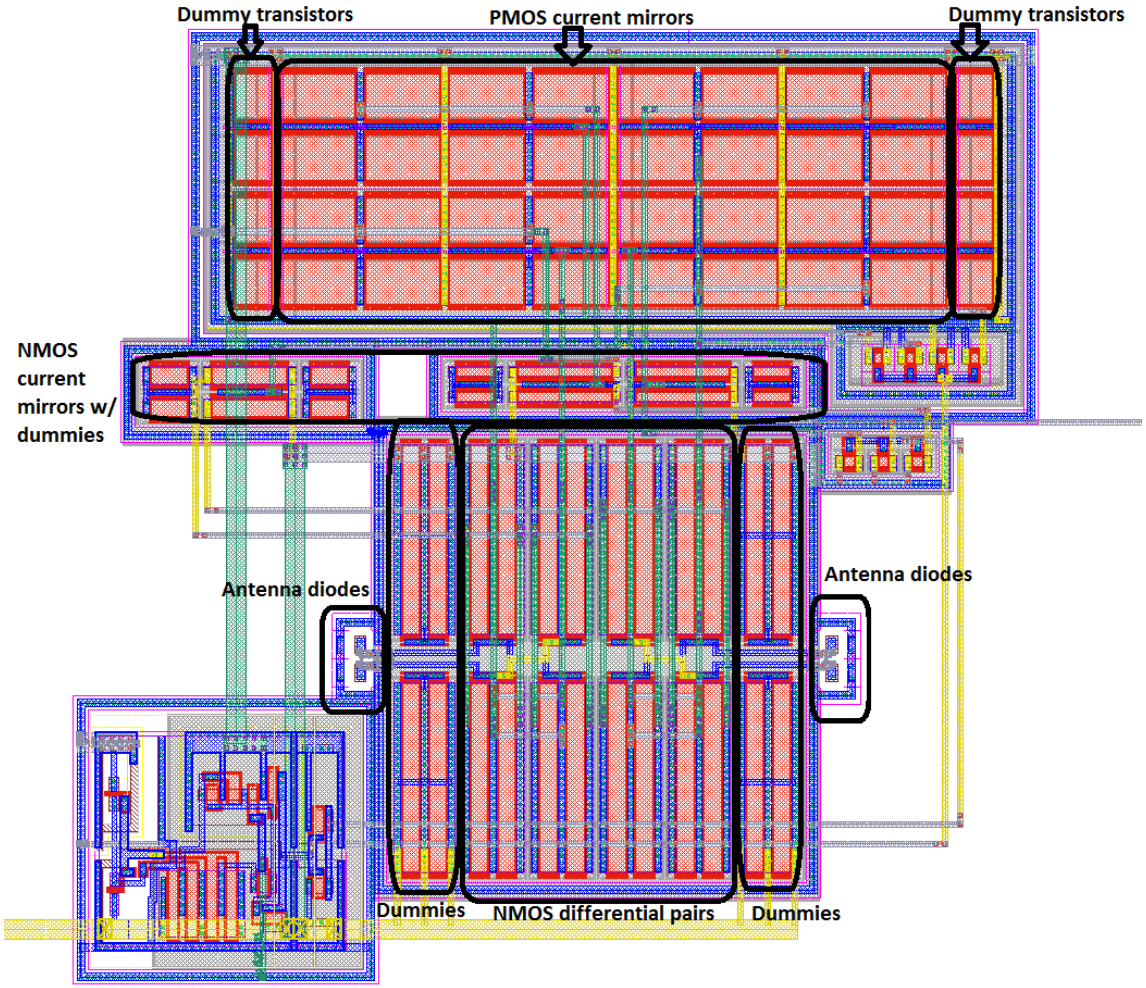


Figure 7.9 : Layout of adaptive resistive g_m block in detail.

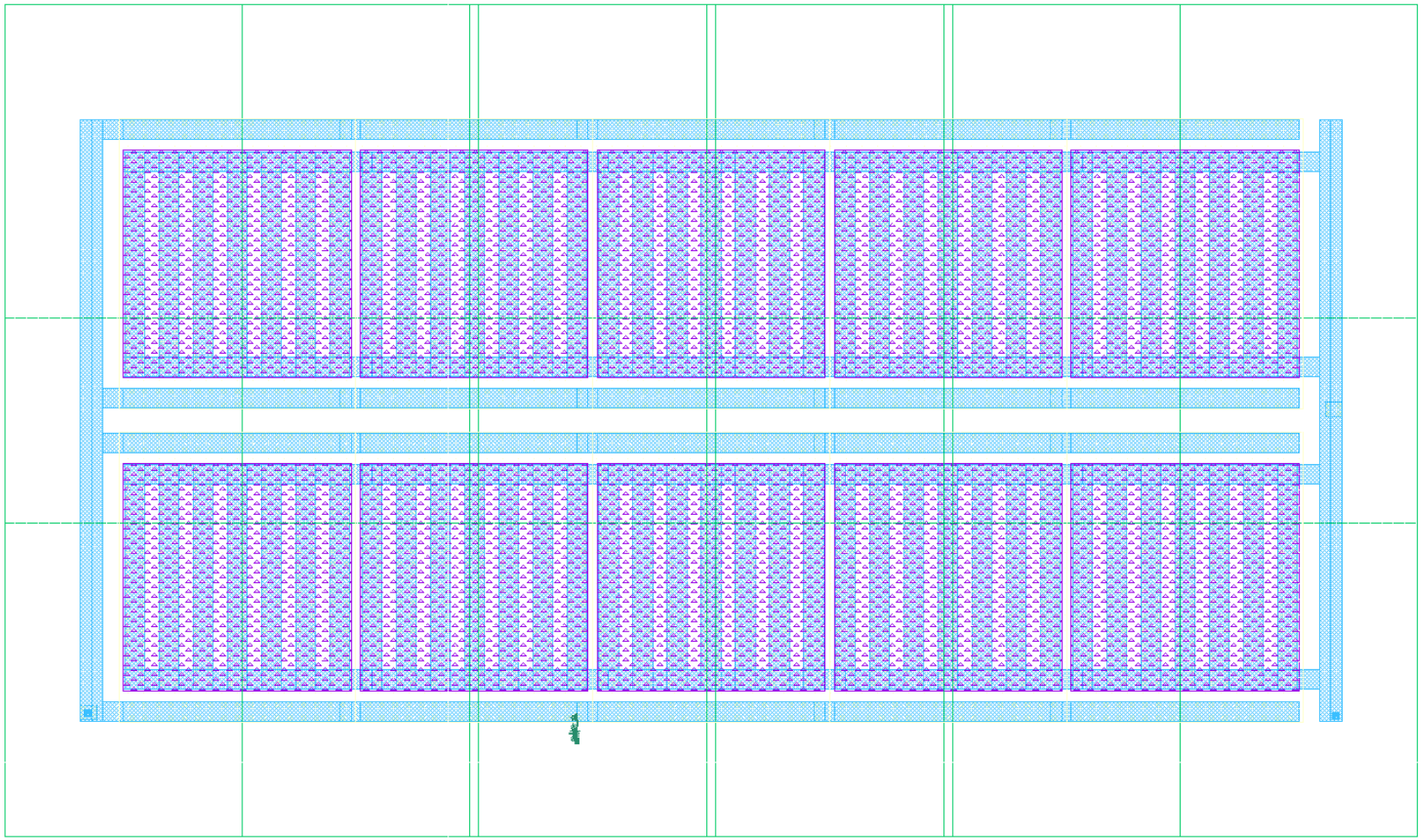


Figure 7.10 : MIM capacitor block.

Metal routings are decided as metal 1 internal routing, metal 2 vertical routing, metal 3 horizontal routing and metal 4 again vertical routing. Routing starts with metal 1 but as all devices use metal 1 as default, it is hard to route with metal 1. That is why higher metal layers are used. In this particular layout, metal 2 is vertical, metal 3 is horizontally routed. As block gets bigger or more complex, metal 2 and metal 3 routings may not enough to build circuit, so one more metal layer is used which is metal 4 for this block. Power and ground routings are on metal 4 with wider width routings.

7.2 Error Amplifier Block

Error amplifier consists of basic differential input stage and one stage NMOS amplifier. Compensation block is done seperately so no compensation inside the block. Circuit level representation can be seen in Figure 7.11.

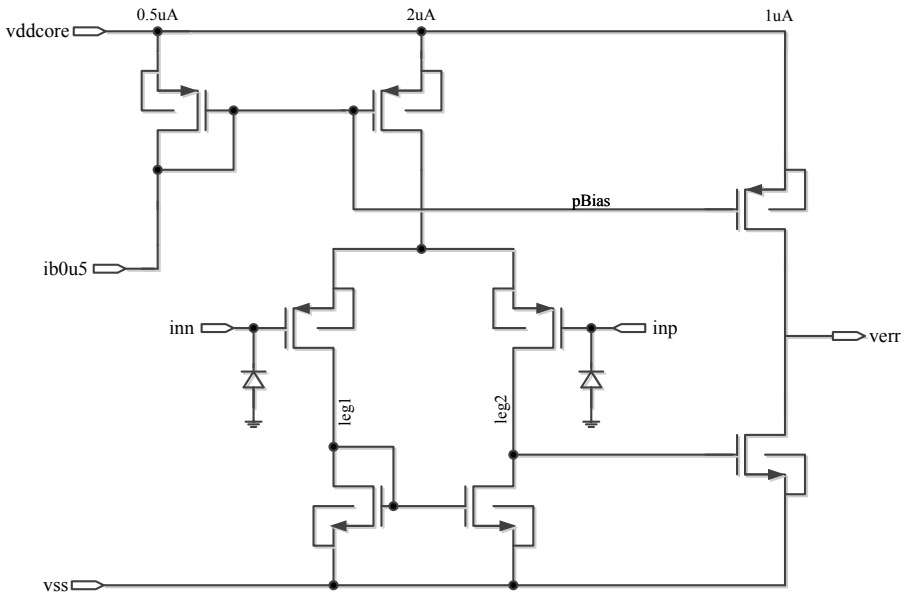


Figure 7.11 : Schematic of error amplifier. [60]

Finished layout is in Figure 7.12. As explained in previous paragraph, this block is small and has fewer devices. Pmos current mirrors are on top while Nmos part is on bottom. Between them, pmos differential block is placed and some logic devices on right and left side.

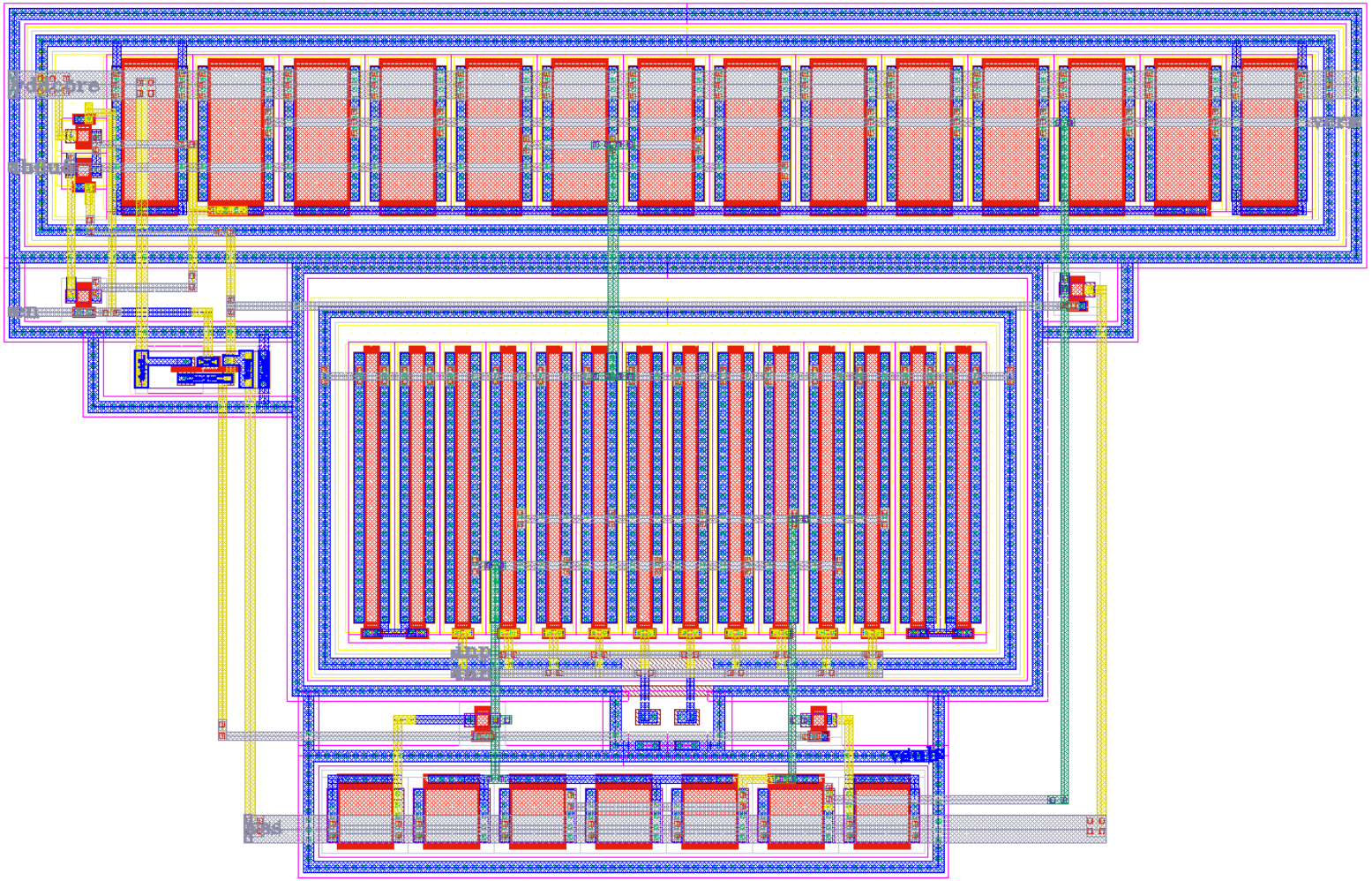


Figure 7.12 : Layout of error amplifier.

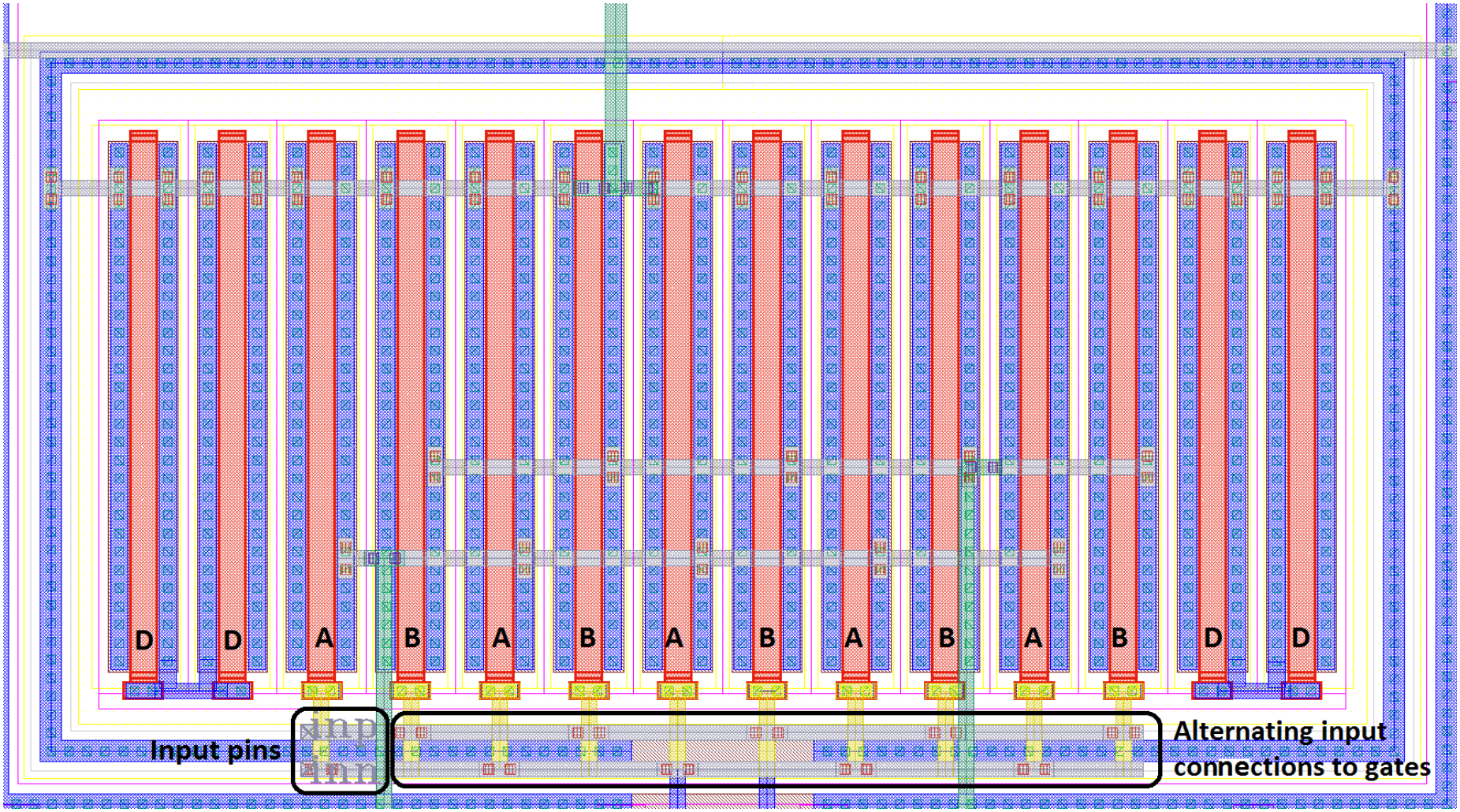


Figure 7.13 : Detailed pmos differential pair.

Figure 7.13 shows the pmos differential pair in detail. To reduce WPE, edge of nwell to actual pmos differential pairs are sufficient enoguh by more than 2µ. To get this more than 2µ, two dummy transistors per edge is used. Note that distance between A to B is same with distance between dummy transistors.To realize interdigitation, mosfets placed one another and their gates are connected by alternative connections.

Same metal routing strateqy is used. Metal 1 is internal metal for devices, metal 2 and metal 4 vertical, metal 3 horizontally used. Power and ground rails are in metal 3 layer and on top and bottom with their pins at edge.

7.3 PWM Comparator

The PWM comparator is a latching comparator. A two stage comparator is designed to implement it with a digital latching functionality. Schematic of block is in Figure 7.14.

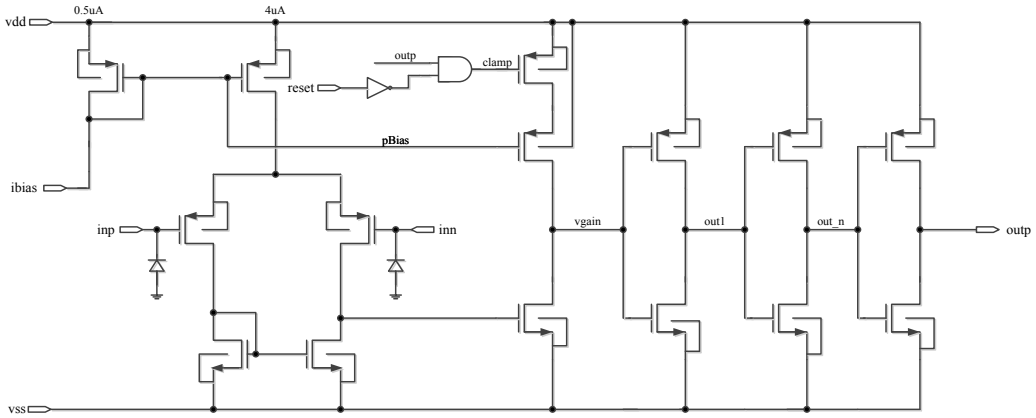


Figure 7.14 : Schematic of PWM comparator [60]

General layout view of PWM comparator is in Figure 7.15. Differential pmos pairs are placed bottom left side, pmos current mirrors are on top while nmos block at bottom. Between them, logic blocks are placed.

Let's have a detailed view for differential pmos pairs in Figure 7.16. Input pins are at the edge of block on left and antenna diodes are on right side. Differential pair is laid out as common-centroid structure explained in previous chapters. It can be seen that dummy transistors are at both edges with same distance asactual transistors. Around the block nwell guard ring and ptap guard rings placed.

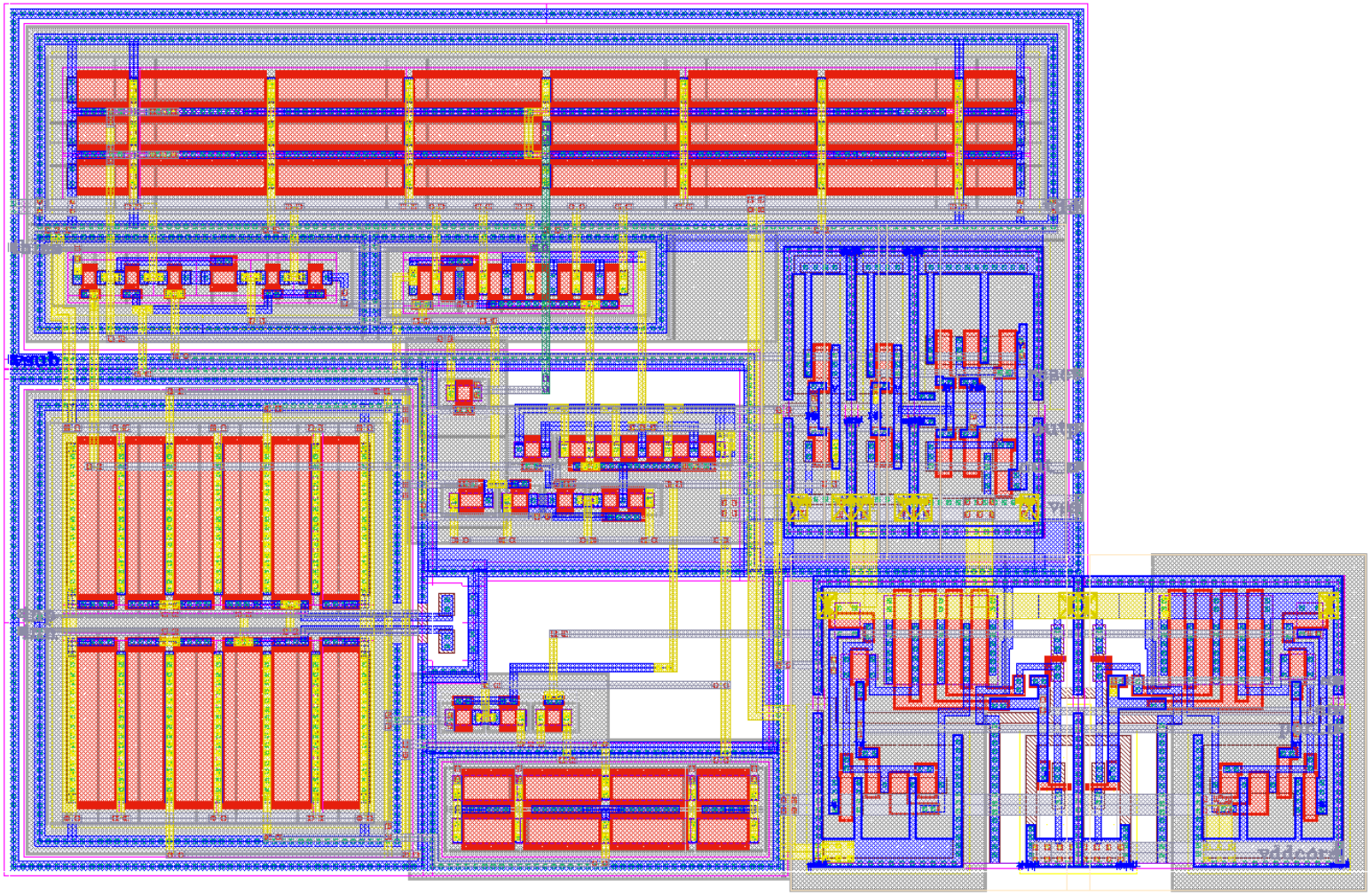


Figure 7.15 : General layout of PWM comparator.

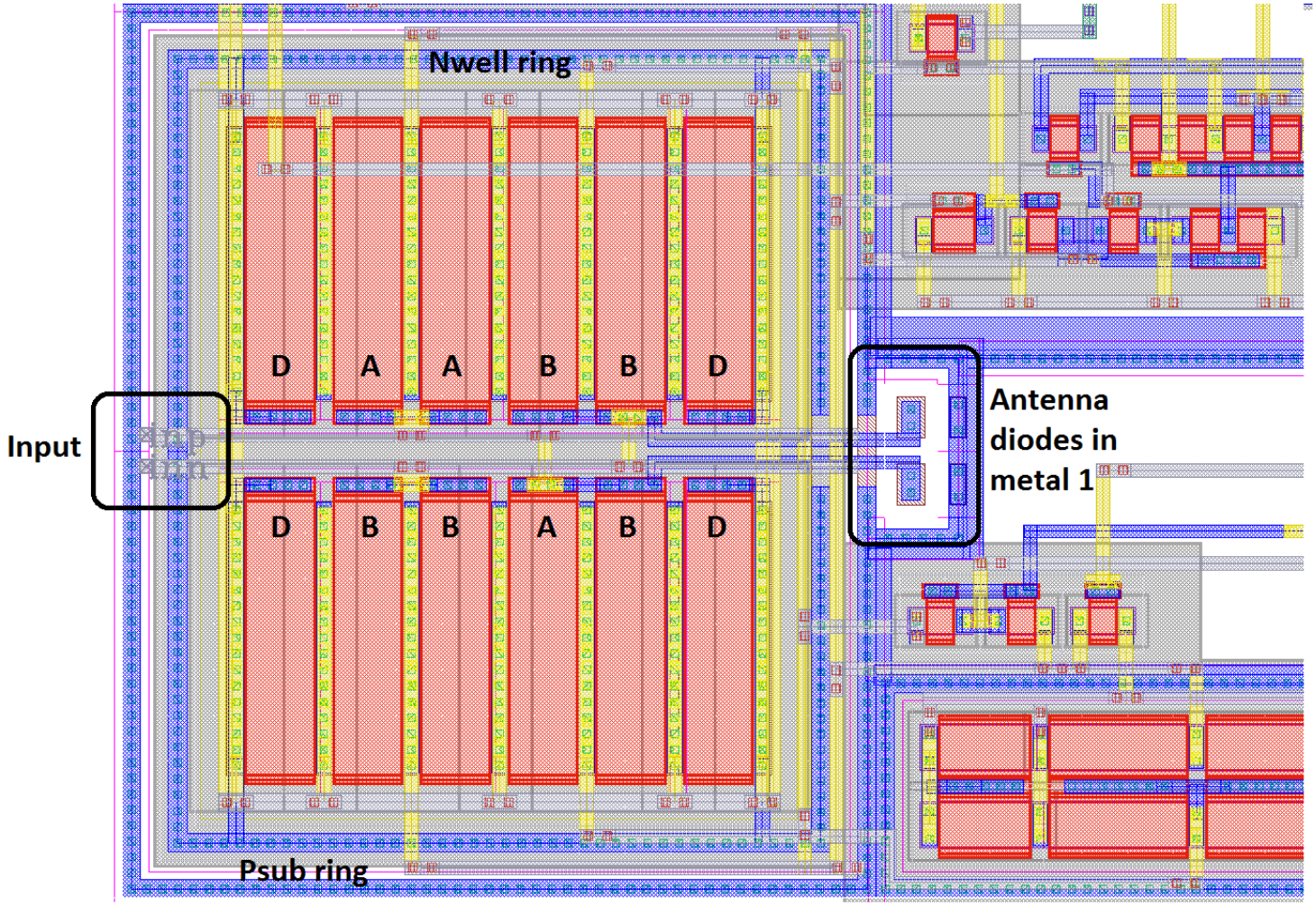


Figure 7.16 : Differential pair zoomed.

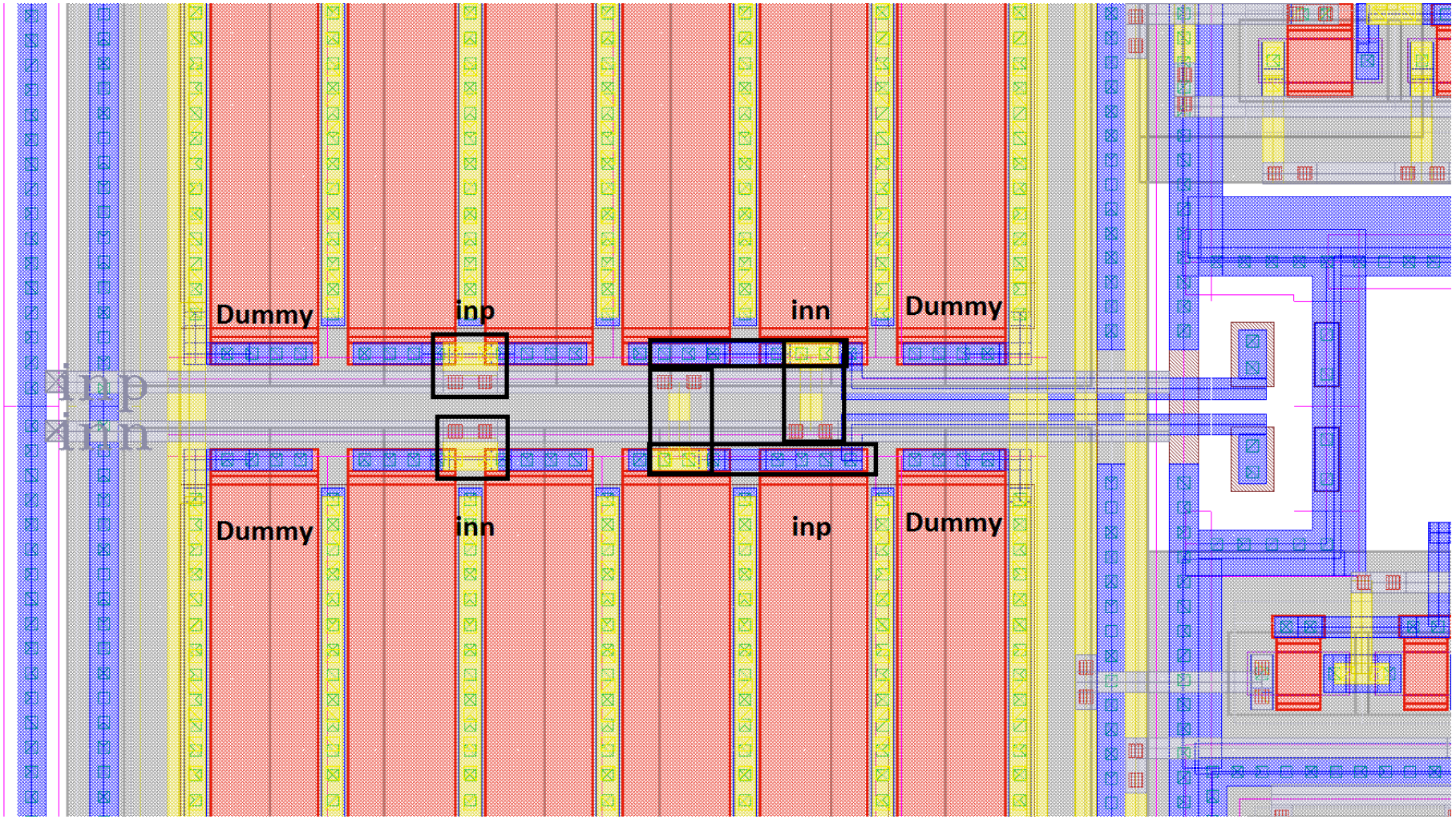


Figure 7.17 : Gate connections of common-centroid differential pmos pairs.

In Figure 7.17, gate connections are shown in detail. As it is seen, it is common-centroid and cross quad structure so connections get more complex. First inn and inp nets can easly connect to first two same mosfets but the other part they had to be cross conencted. This cross connection increases the parasitic capacitance between two nets. On the other hand, these two nets enters the differential pair, differential pair structure is immune to parasitic nets between inputs which is a benefit for inputs and layout connections.

As usual, vertical metal 2 and horizontal metal 3 routings are used in the block. Wider metal 3 routing on top and bottom represents vdd and ground path.

7.4 Ramp Generator

The ramp generator is a circuit specified with trimmable ramp voltage, switching frequency and the output ramp voltage range between certain voltages. The schematic design of ramp generator is demonstrated in Figure 7.18.

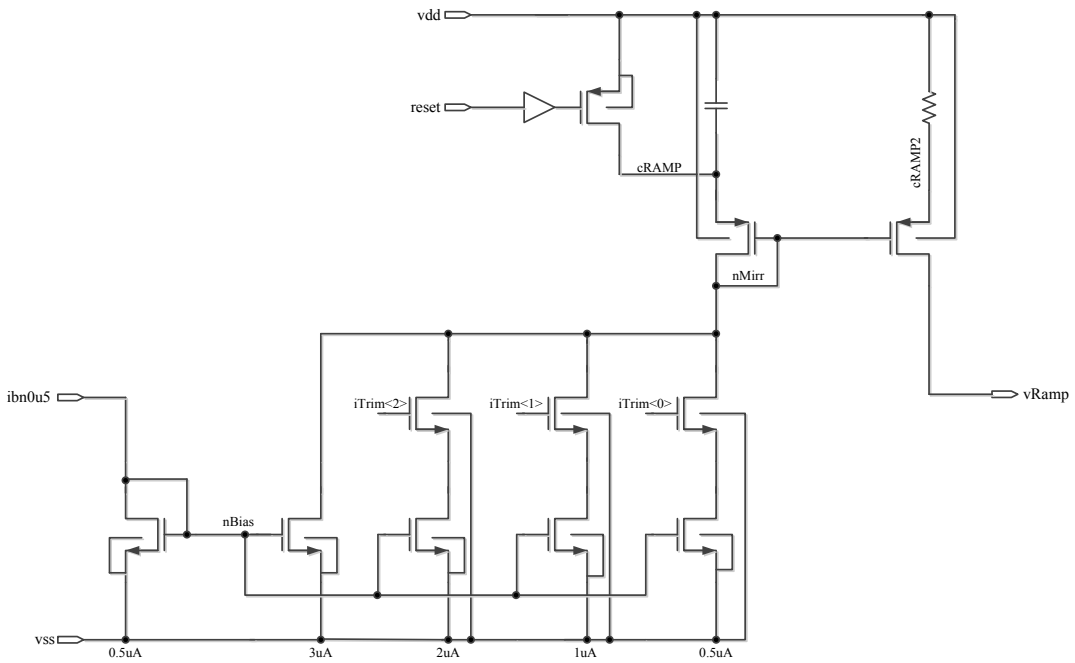


Figure 7.18 : Schematic of ramp generator [60]

Moving on the layout of block, general representation, simplified layout without MIM capacitors are shown in Figure 7.19 and Figure 7.20, respectively.

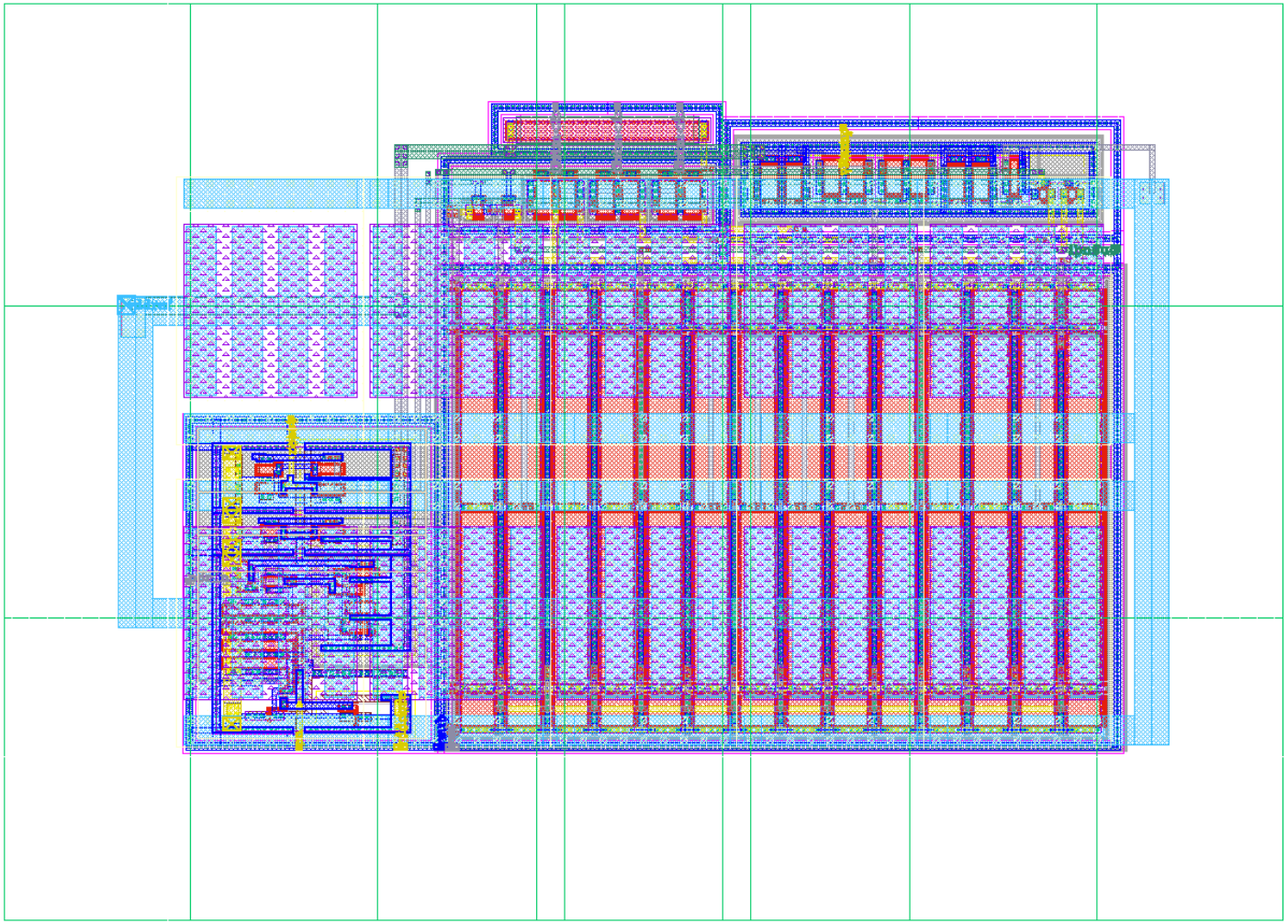


Figure 7.19 : General layout of ramp generator.

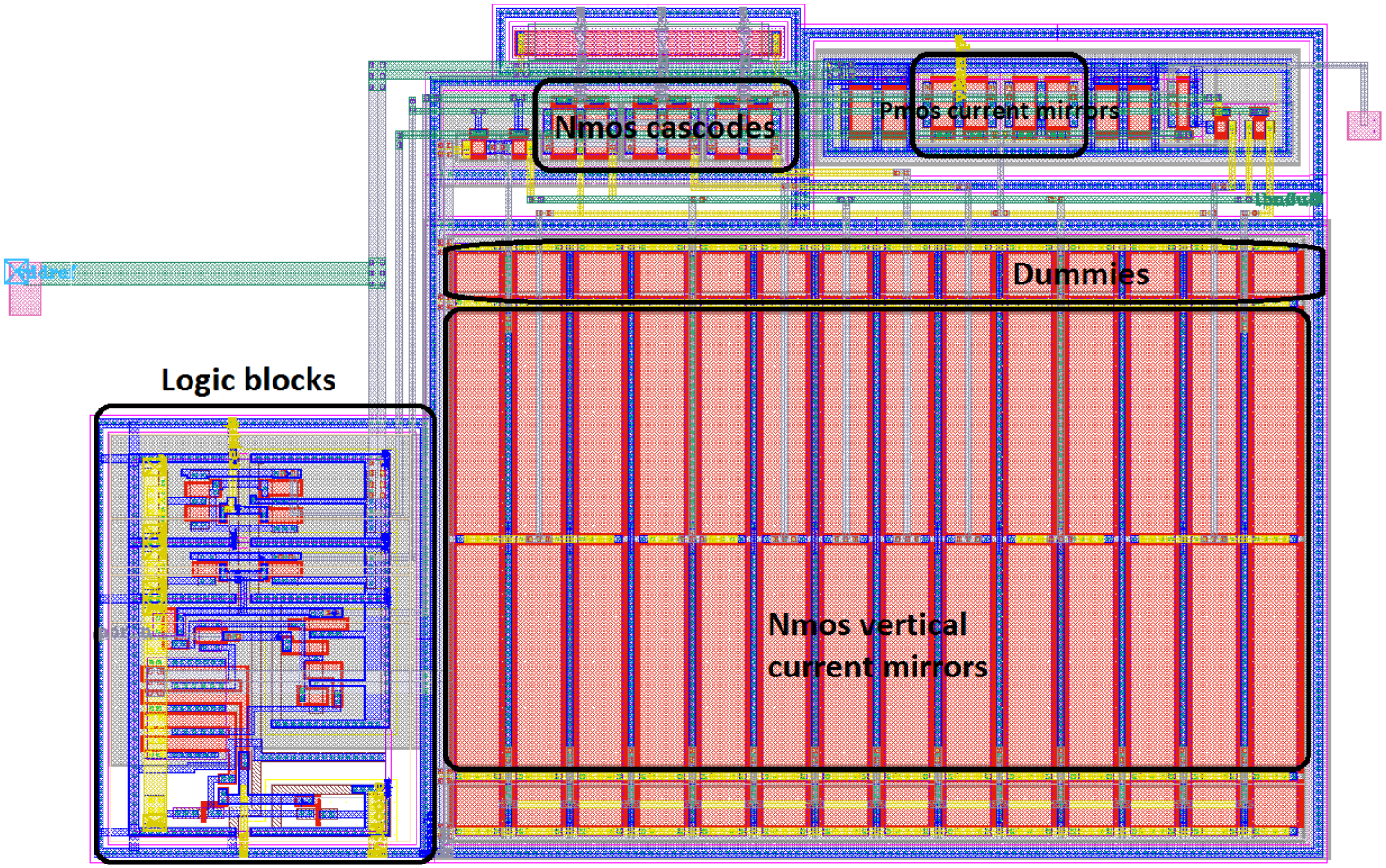


Figure 7.20 : Simplified layout without MIM capacitors on top.

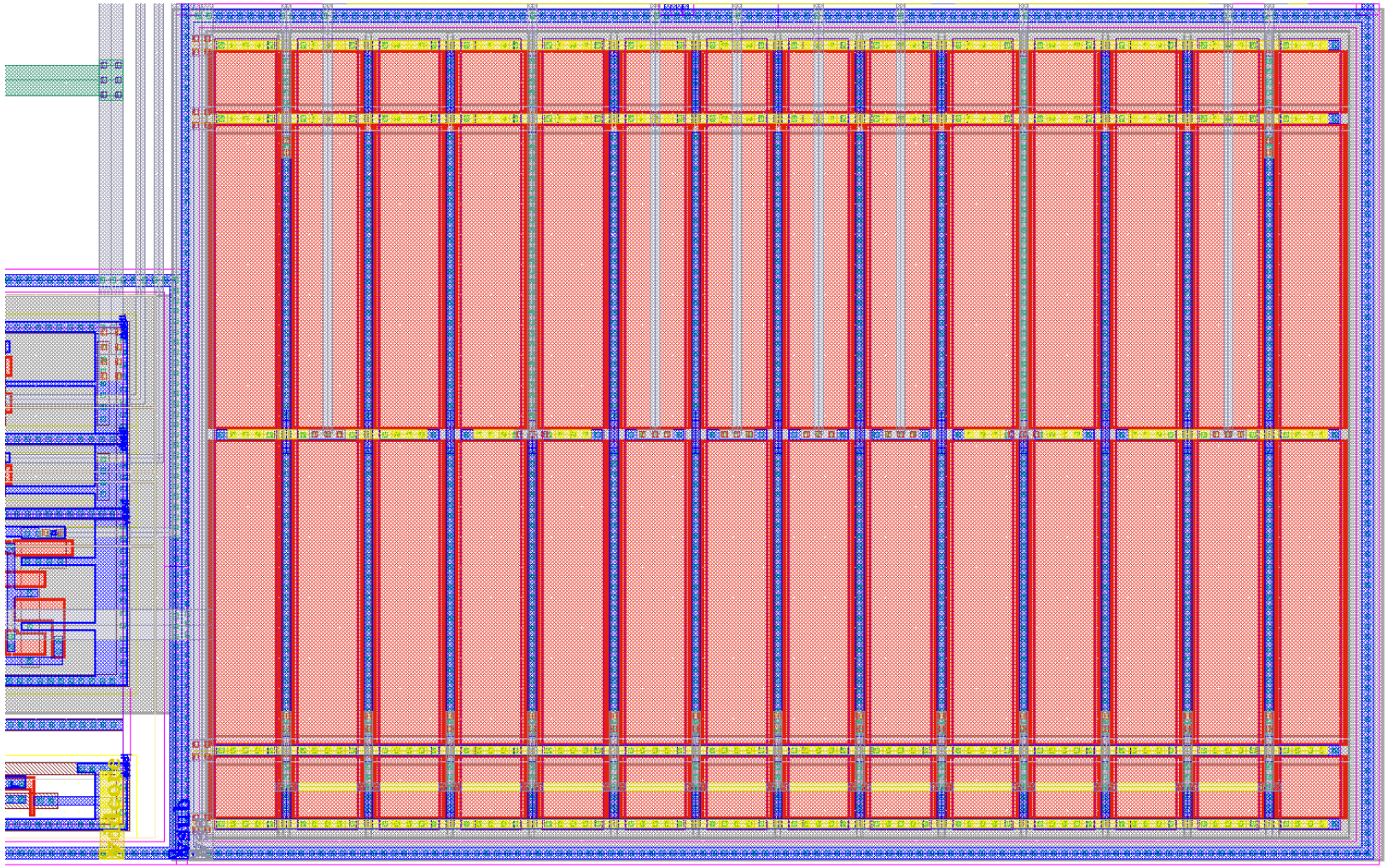


Figure 7.21 : NMOS current mirror connections.

7.5 vSense Sample and Hold Block

The vSense sample and hold block is designed to sense the LX voltage in correct point, sample it and hold in the sample point for the other cycle which the LX goes to zero. The design consists of basic NMOS and PMOS switches connected together and a sampling capacitor at the output in Figure 7.22. Two switches are used as PMOS and NMOS and the switches are driven with inverted signals to minimize charge injection.

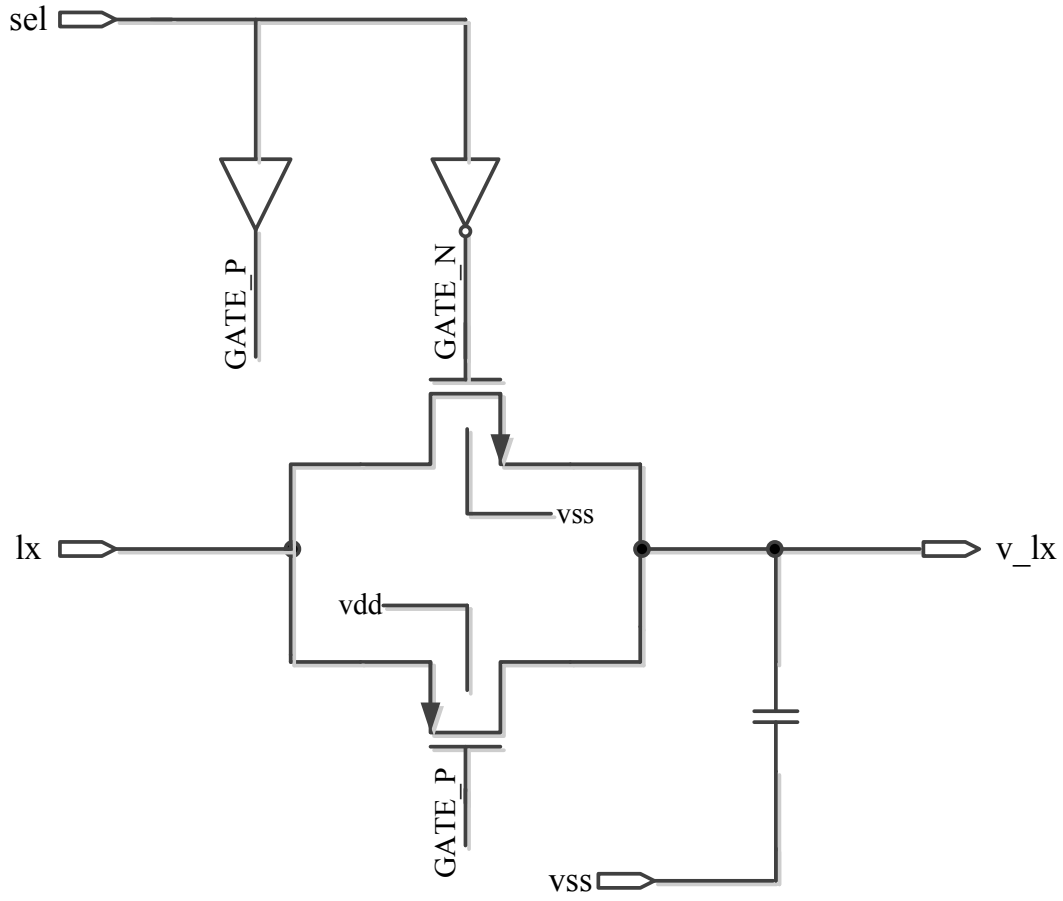


Figure 7.22 : Schematic design of vSense sample&hold block [60]

Since this block has very simple structure, layout is also simlpy laid off (Figure 7.23). Block consists of MIM capacitors, one pmos and one nmos with their gates are diriven and controlled by logic inverters.

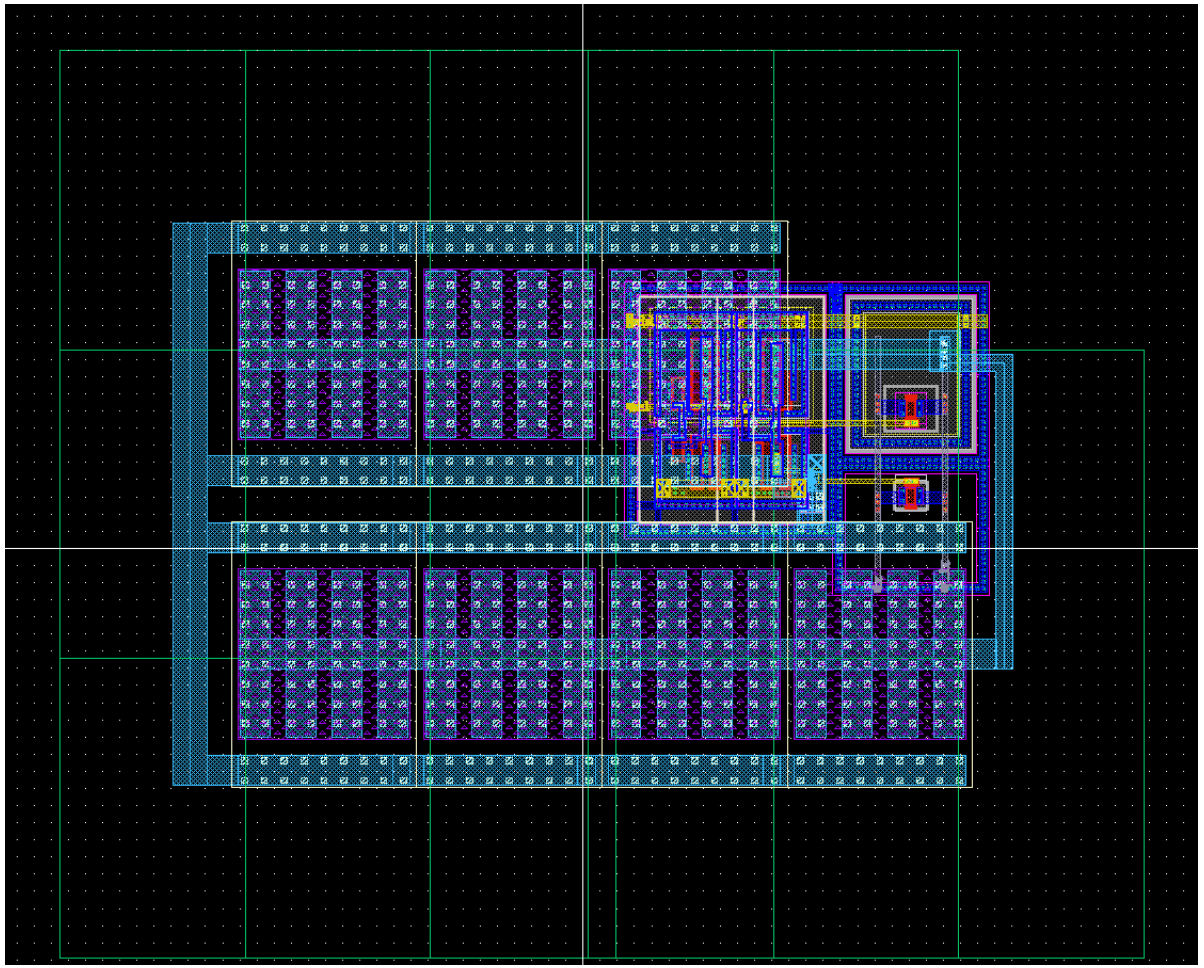


Figure 7.23 : Overall layout of vSense sample&hold.

7.6 Active Diode Comparator

The active diode comparator detects the condition that the inductor current crosses zero Ampere. A resistor string is used in the input stage to implement the trimmability in the input offset. The NMOS devices are used as switches to select different values of the resistors to create both positive and negative input offset. The same sized NMOS devices are put to the resistor string as well to compensate the switch resistances. The second stage is for only amplification. The output signal voltage domain is changed from 1.5V to 5V to be an input for zero crossing logic. Schematic of active diode is in Figure 7.24.

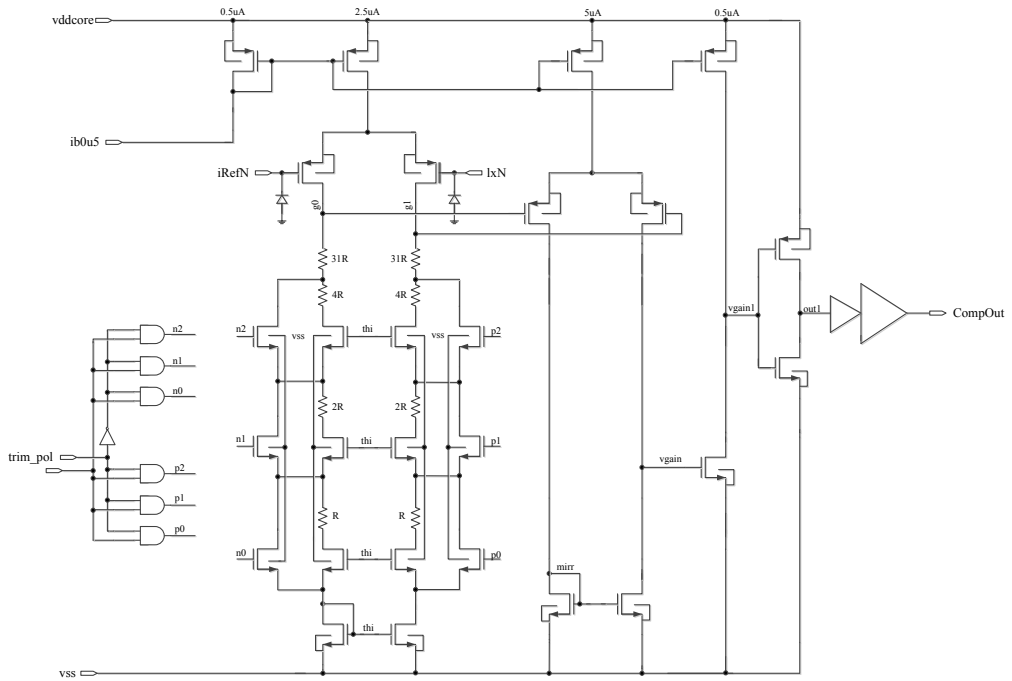


Figure 7.24 : Schematic of active diode comparator [60]

Finished layout of active diode comparator is shown in Figure 7.25. All current mirrors, differential pairs, serial resistors, its mosfet devices for switching, first and second stages and logic circuitry can be seen in Figure 7.26. Differential pair of first stage is shown in Figure 7.27 in detail. Note that differential pair blocks is laid out as sharing diffusions and dummies at both ends. It is laid out as A-B-A-B order.

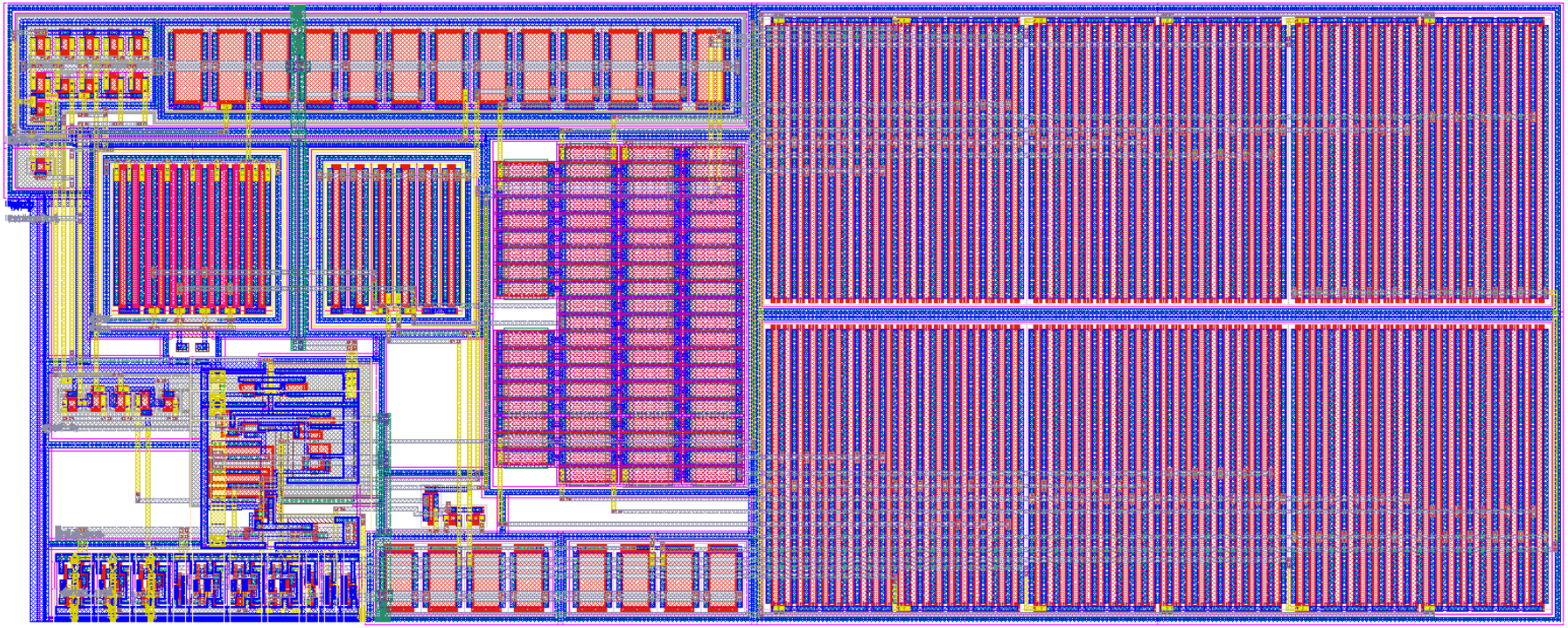


Figure 7.25 : Layout of active diode comparator.

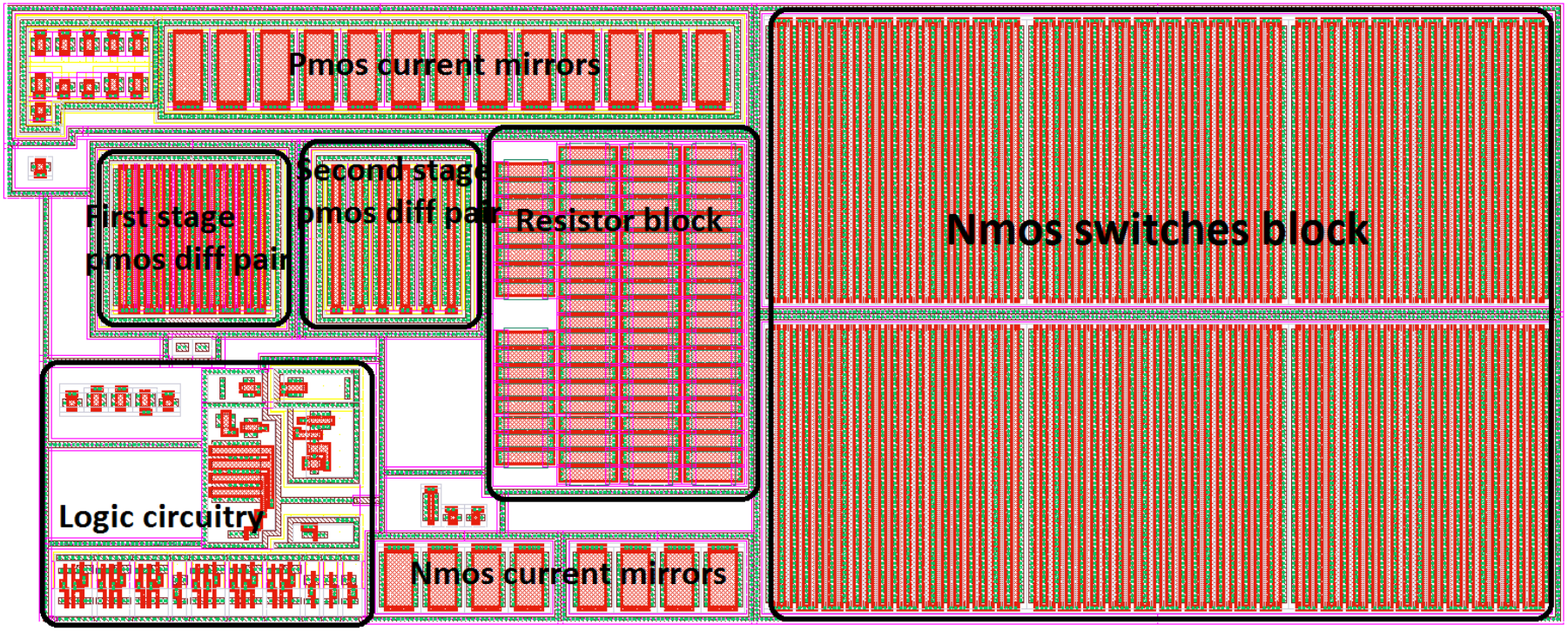


Figure 7.26 : Detailed blocks inside active diode with only base layers shown.

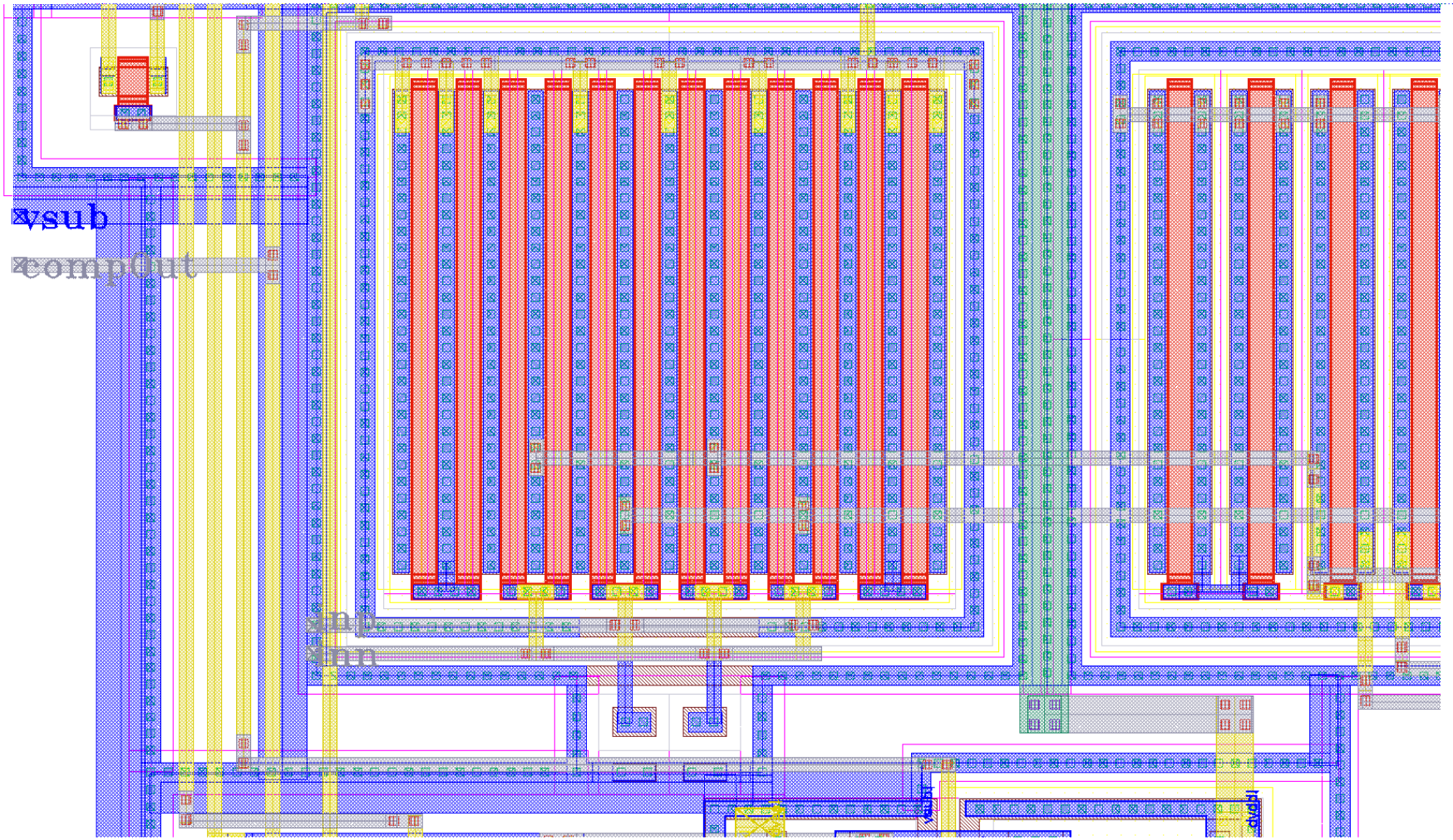


Figure 7.27 : First stage pmos differential pair and its conenctions.

7.7 Pre-Driver and Driver

The adaptive pre-driver and driver are among the critical circuit blocks for adaptive buck converter topology since they are the main units to drive various output loads and the efficiency of the buck converter is directly related to their unit sizes. In this study 5.6A maximum load current is decided. Peak efficiency of converter is generally $1/3^{th}$ of maximum load current. First PMOS device size is determined from that point NMOS device size is calculated. There is a small replica of the PMOS driver to sense the load current. Unit driver schematic is shown in Figure 7.28.

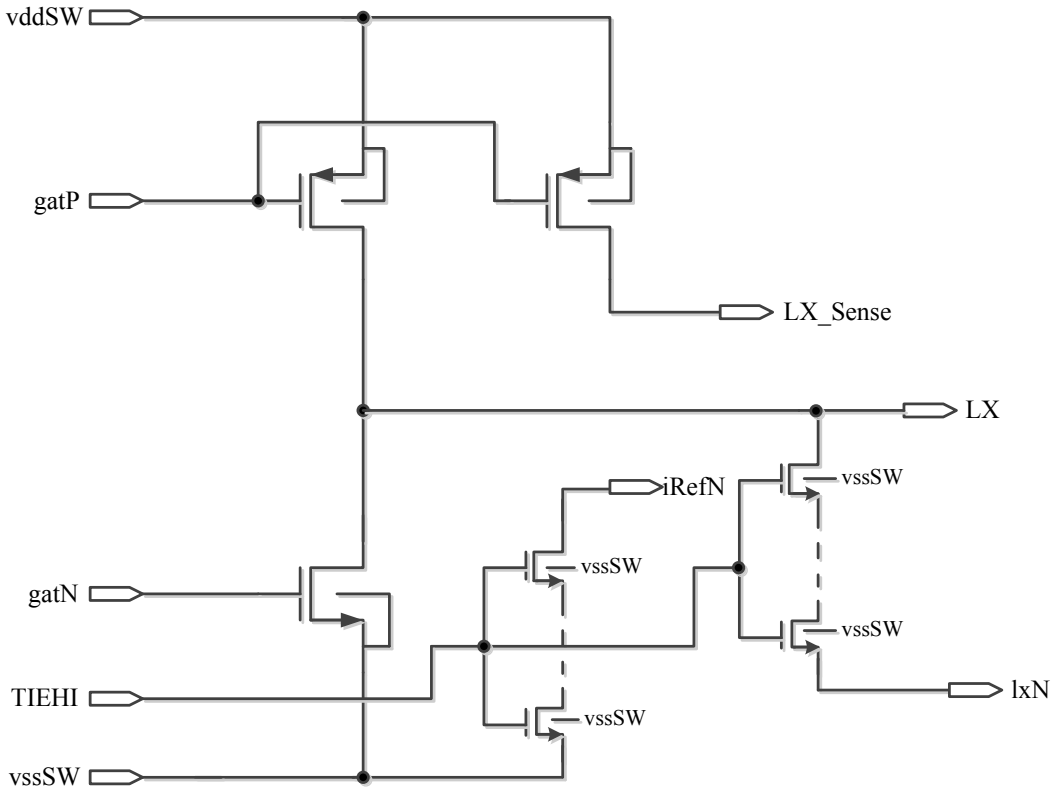


Figure 7.28 : Schematic of unit driver/pass device [60]

If the PMOS and NMOS conducts in the same time, short circuit current is an immense issue since it affects efficiency directly. Therefore, a non-overlapping logic is implemented to prevent short circuit current flowing on pass transistors as much as possible. The implementation is done inside pre-driver, Figure 7.29.

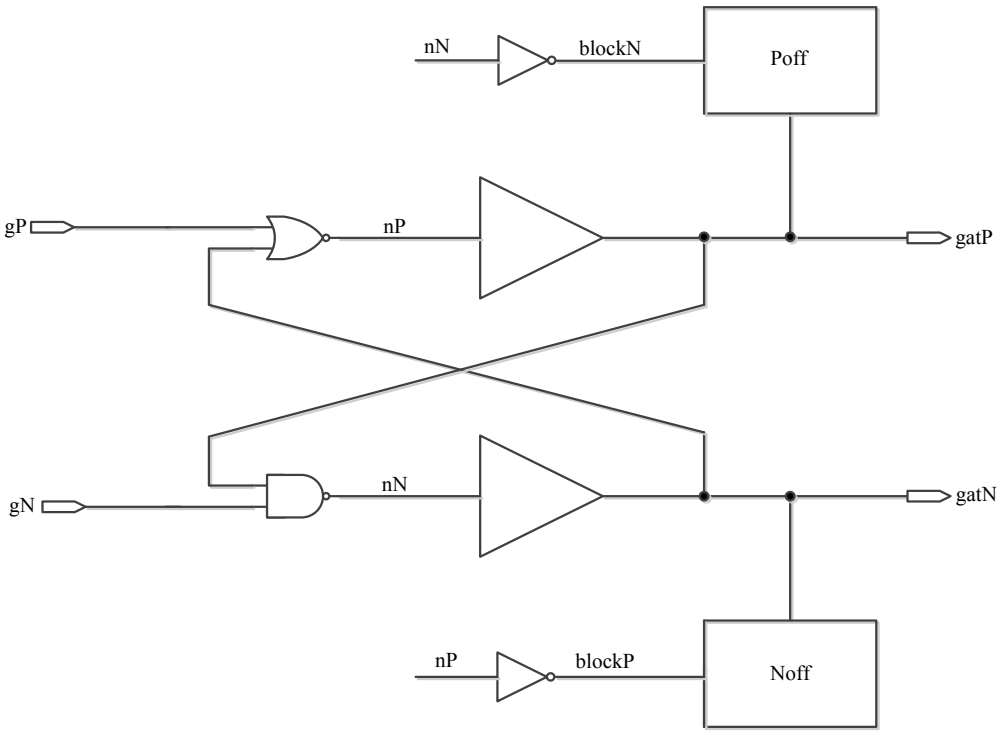


Figure 7.29 : Schematic of unit pre driver [60]

The Poff and Noff block seen in schematic diagram are designed to compensate a phenomenon called dv/dt induced turn on phenomenon [61]. Figure 7.30 shows inside of P_{off} logic while Figure 7.31 shows schematic diagram of N_{off} logic.

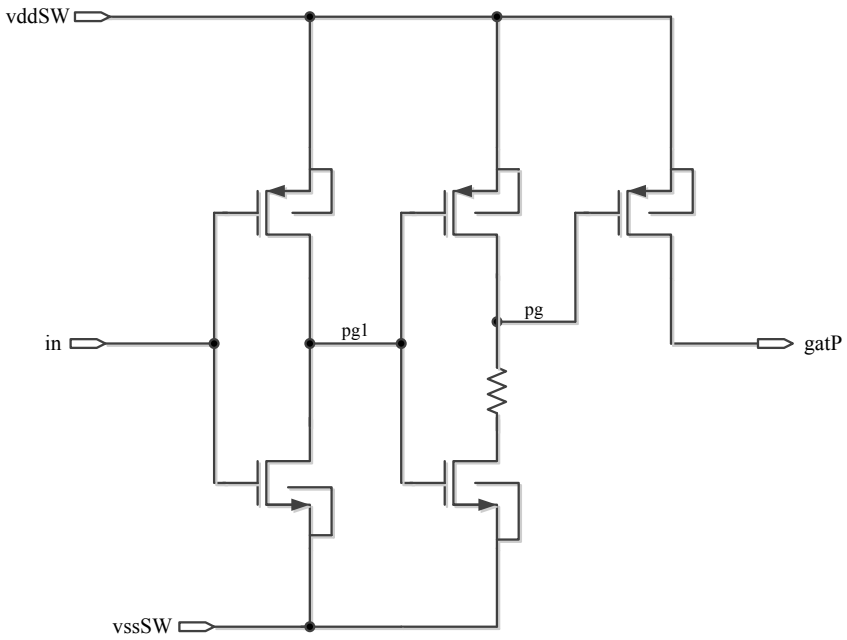


Figure 7.30 : Schematic design of P_{off} logic [60]

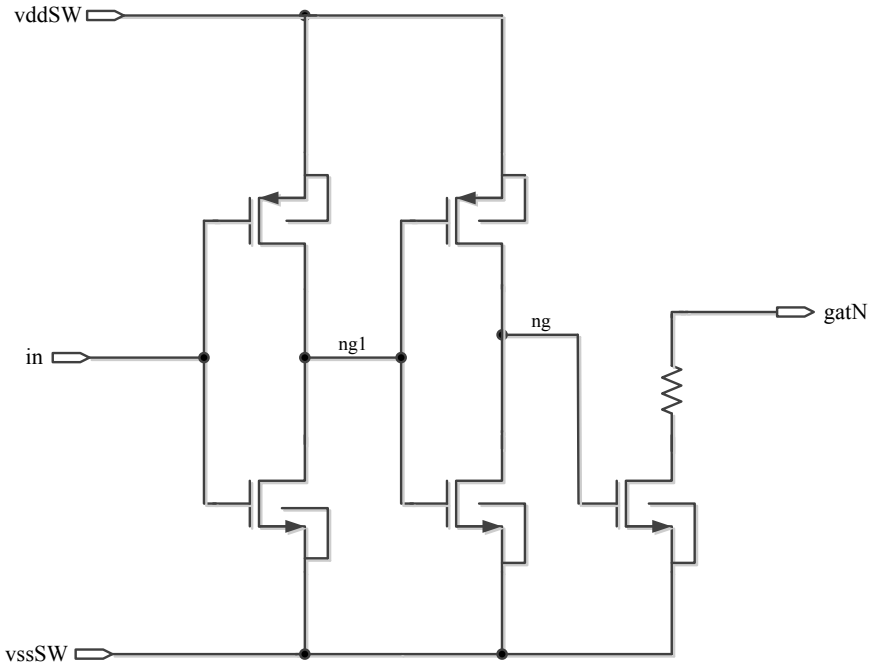


Figure 7.31 : Schematic design of N_{off} logic [60]

Let's start to have a look at to smaller blocks. Noff and Poff block layouts are shown in Figure 7.32 and Figure 7.33. These blocks have few instances to layout. Together with them buck unit drive block is done, Figure 7.34. A detailed representation of buck unit drive with Noff and Poff block are in Figure 7.35.

As this unit drive block is one unit, it is instantiated more in upper levels of schematic to control every unit pass device. So this unit drive might look small but doing upper levels we will see that this block will consume more area.

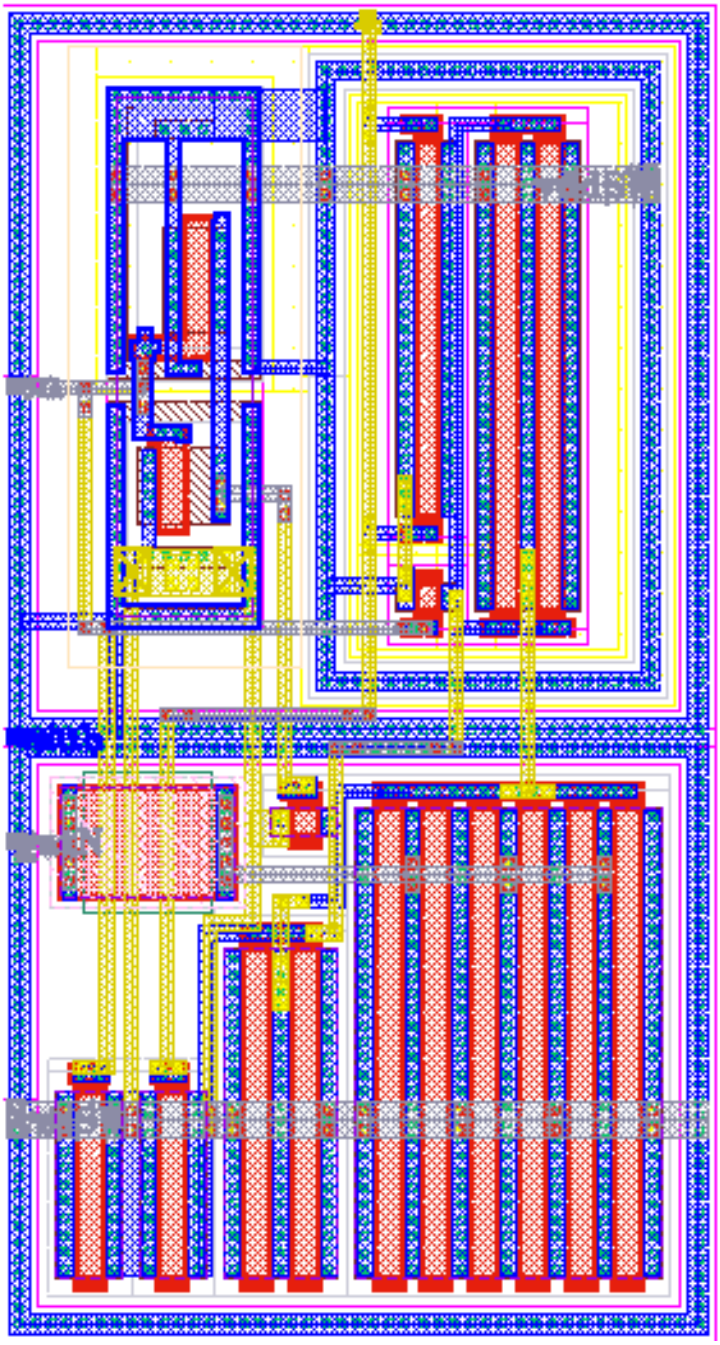


Figure 7.32 : Layout of N_{off} block.

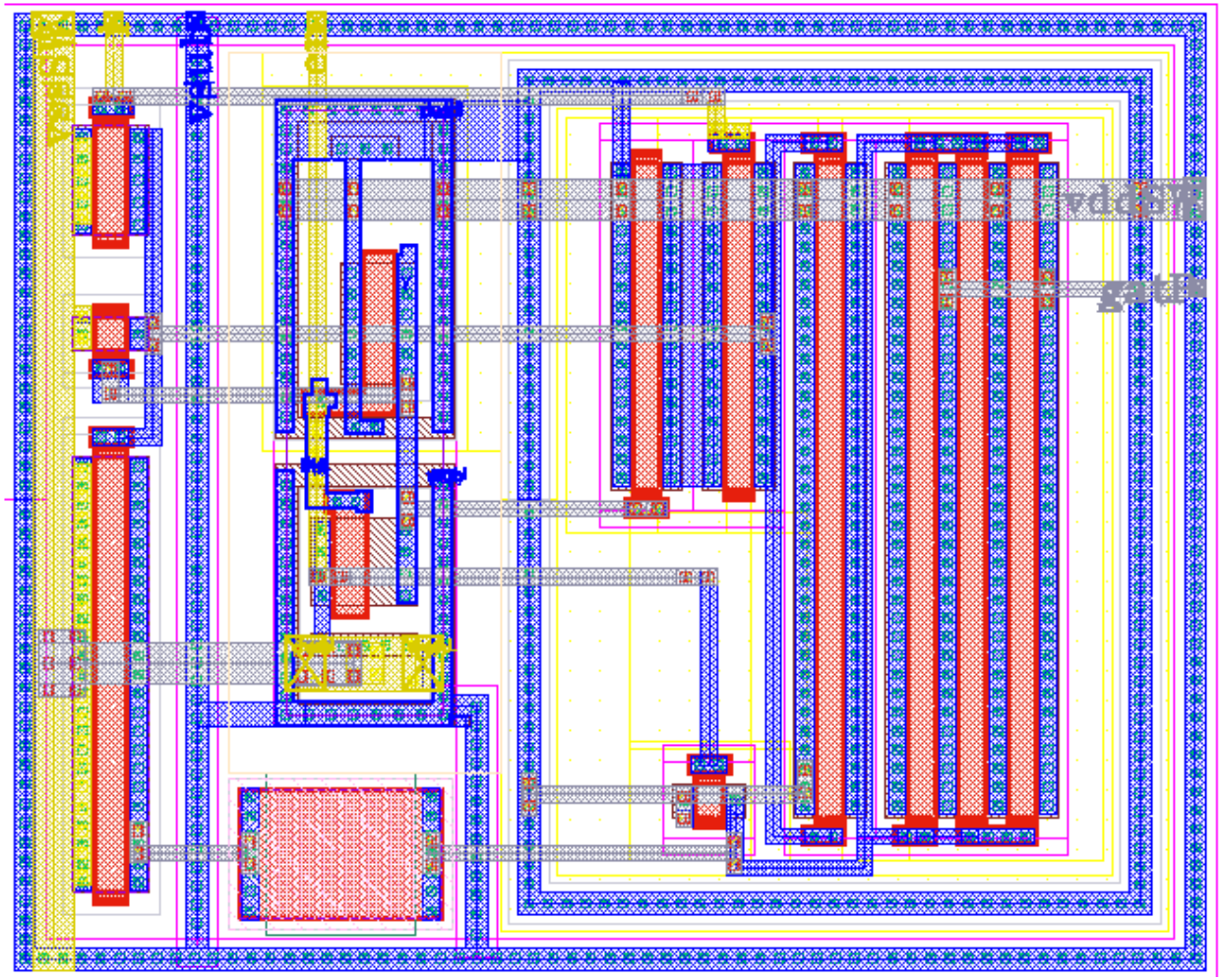


Figure 7.33 : Layout of P_{off} block.

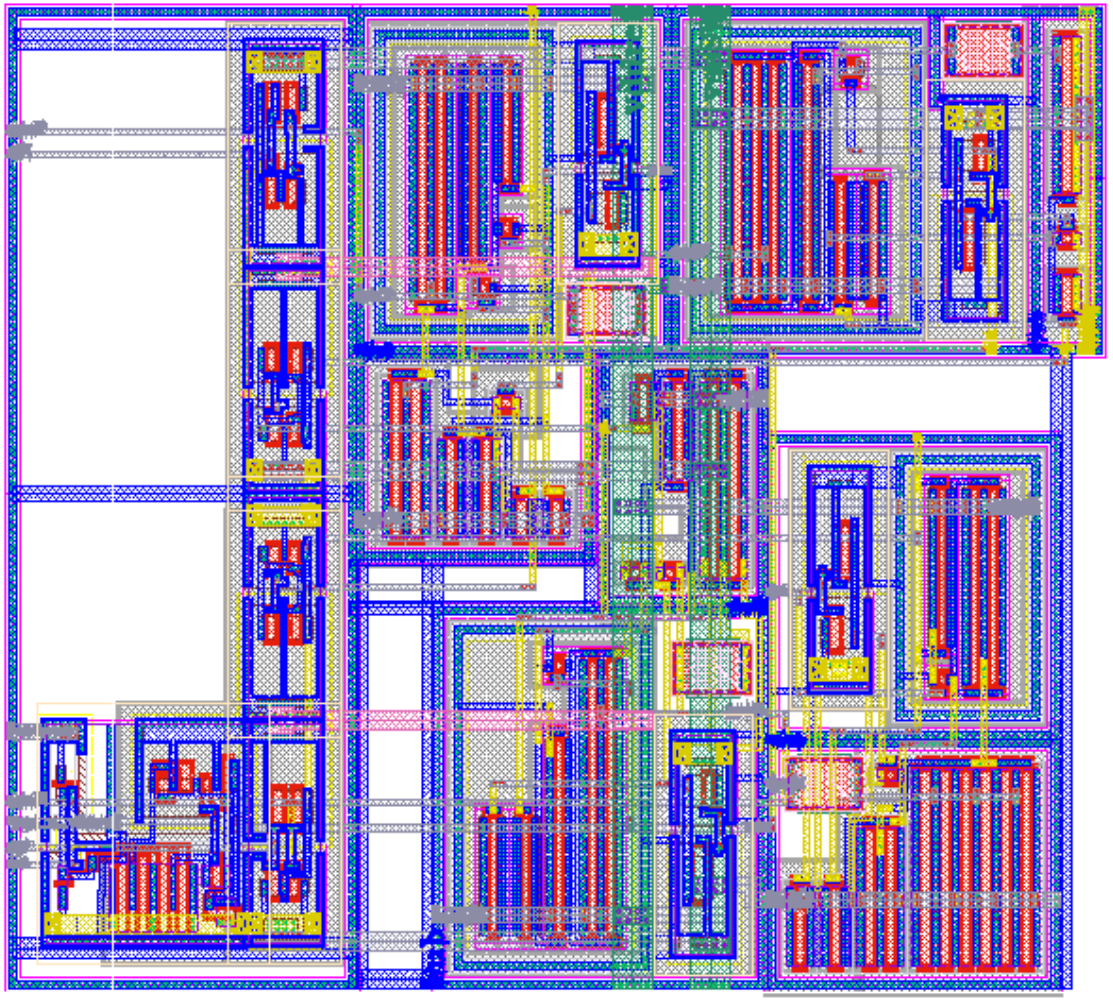


Figure 7.34 : Layout of buck unit drive block.

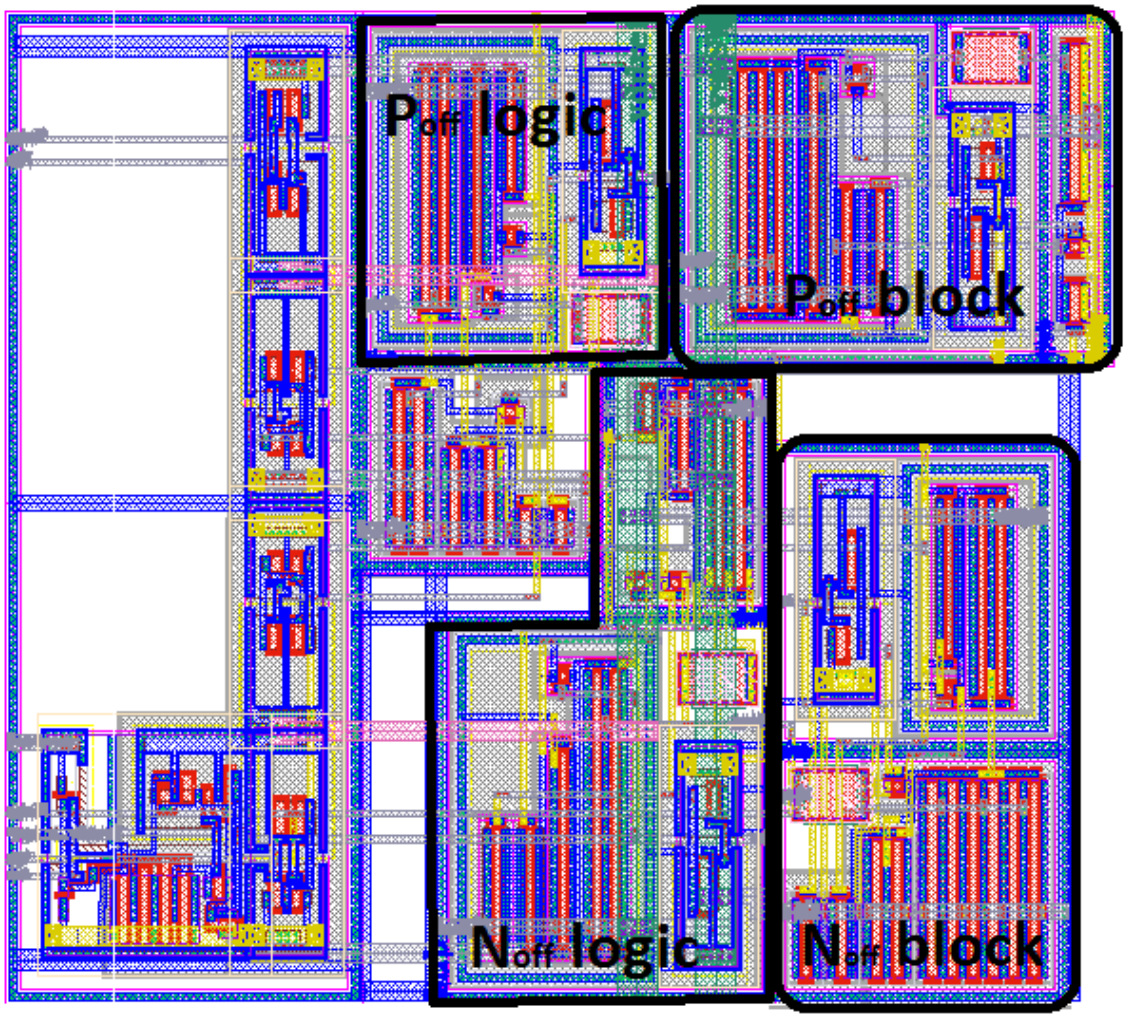


Figure 7.35 : Buck drive unit and its sub blocks.

Regulating ampers of current creates stress on layout. Therefore layout structure is very crutial for buck converters. Designed pass device or can be also called driver needs to handle lots of current. Metal connections should be as wide as possible and as lots of branches as possible should be used.

In order to roughly hand calculate whether metal line can sufficiently handle designed current value, Table 7.1 shows data for metal and contacts. Table 7.1 also shows metals sheet resistances. In some cases, signal's resistance can be important, so calculating metal routing and then sheet number and looking up the related metal's sheet resistance, it can be calculated by multiplying metal's sheet resistance with calculated sheet number. Therefore, resistance of metal routing can be deduced [62-63]

Generally, values for 110^0C is the standart calculation data. However, if designed chip operates more than standart temperature value, 125^0C data value should be used to calculate current capability of metal then layout should be laid out concerning 125^0C.

Placing as much contacts as possible while moving up or down on metal routing will help reduce contacts' resistance. Drawing metal line as wide as possible will also help reduce resistance of metal line while wide metal line will have more parasitic capacitance due to large metal.

Now move on the unit pass device layout. Since pass device itself occupies a very large area, it has to be laid out slice by slice. Because they are repetition of one slice to another, doing one slice and placing it more than one, we can have opportunity to layout whole pass device in a more convenient and faster way.

Table 7.1 : Metals and contacts/via sheet resistance and current density.

0.25µ BCD Process

	Rsh (Ohms/sq. or Ohms/ct.)	Current Density (mA/um or mA/ct.) @110°C	@125°C
CONT	7,4	0,71	0,48
M1	0,0841	1,00	0,67
VIA12	4	0,40	0,27
M2	0,0711	1,00	0,67
VIA23	4	0,40	0,27
M3	0,0711	1,00	0,67
VIA34	4	0,40	0,27
M4	0,0711	1,00	0,67
VIA45	4	0,71	0,47
M5_8K	0,0338	1,60	1,07
M5_30K (UTM)	0,00897	6,00	4,03

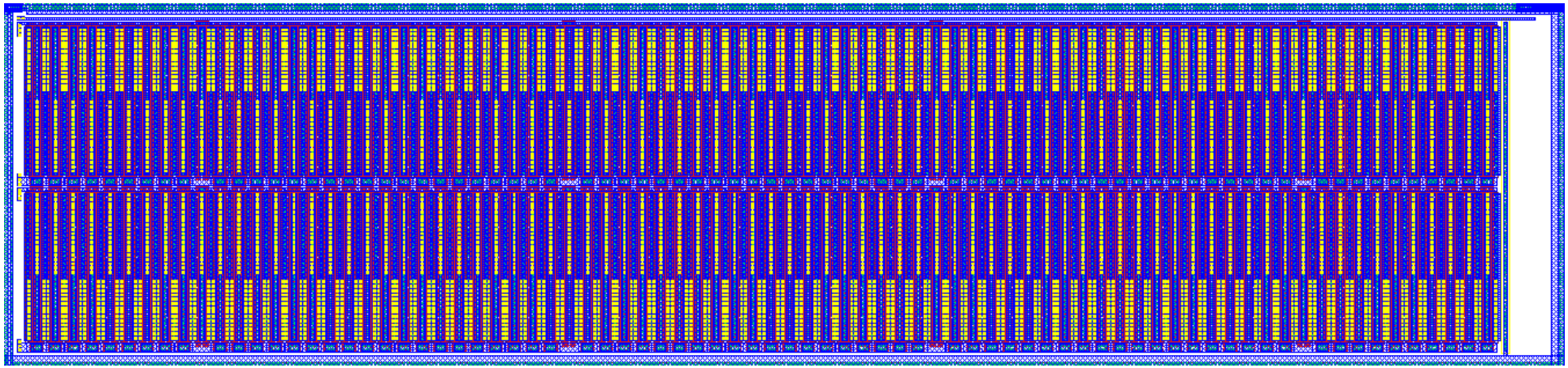


Figure 7.36 : NMOS unit pass device layout with base layers and metal 1.

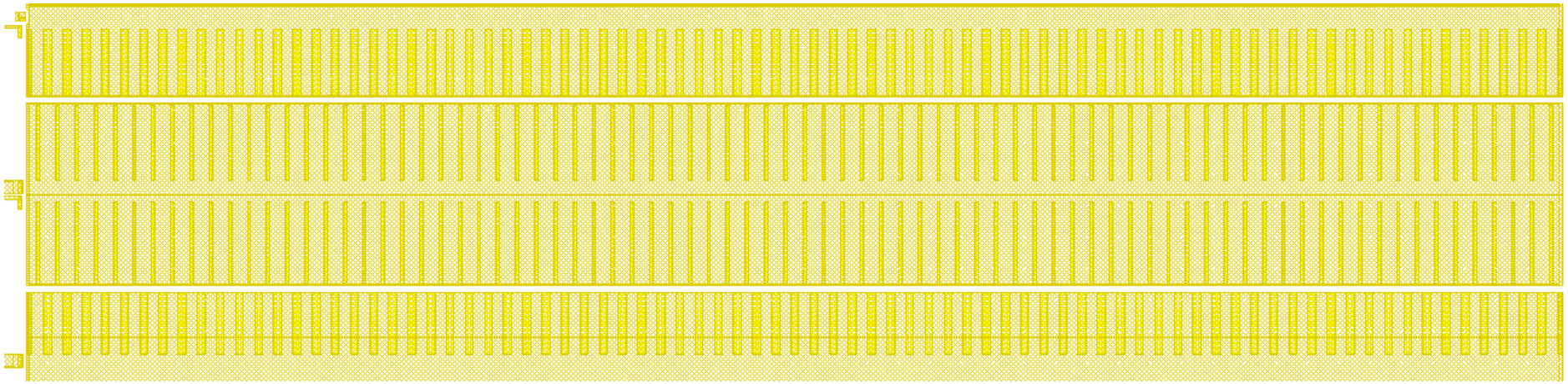


Figure 7.37 : NMOS unit pass device with metal 2.

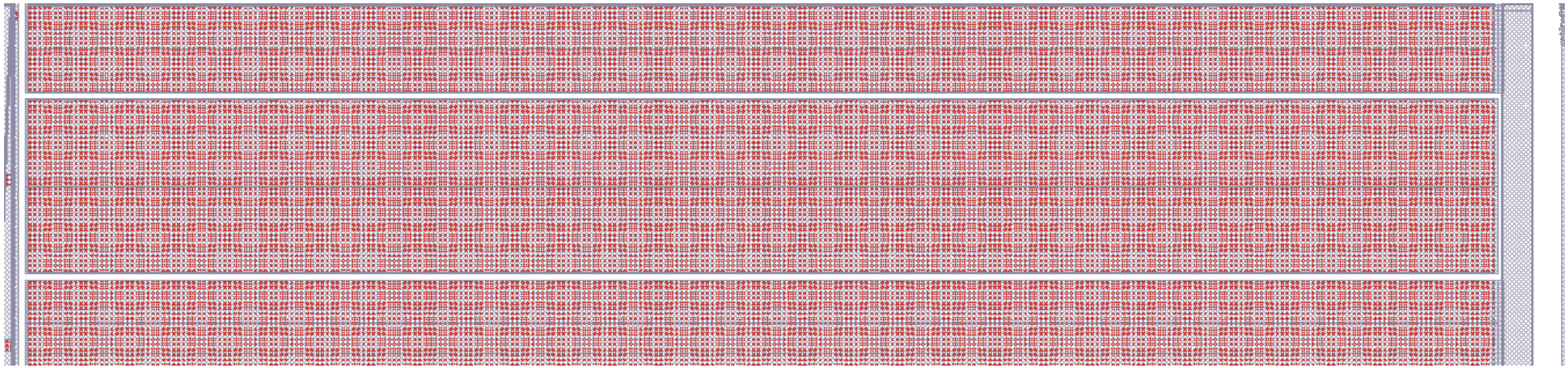


Figure 7.38 : NMOS unit pass device with metal 3.

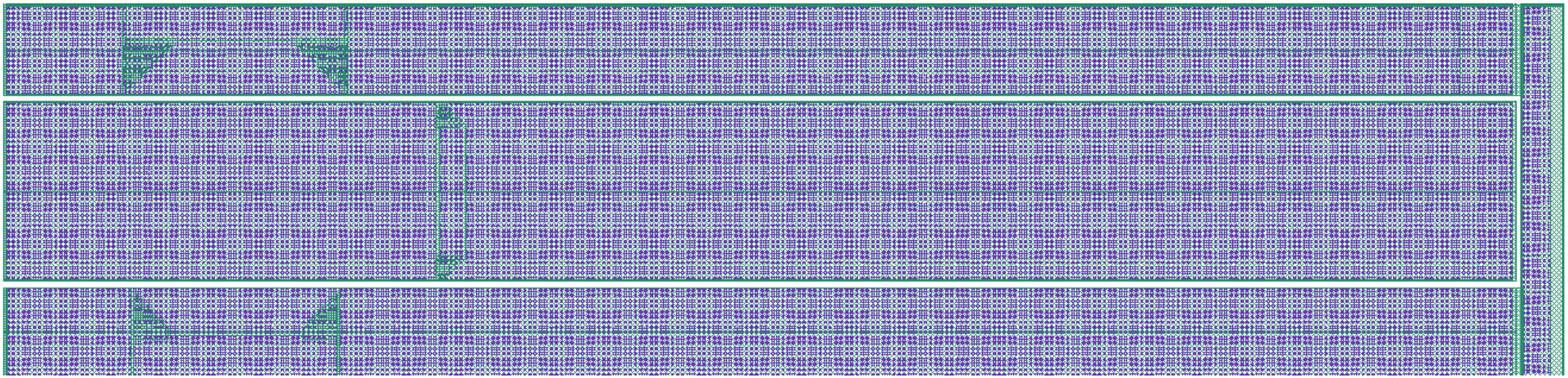


Figure 7.39 : NMOS unit device with metal 4.

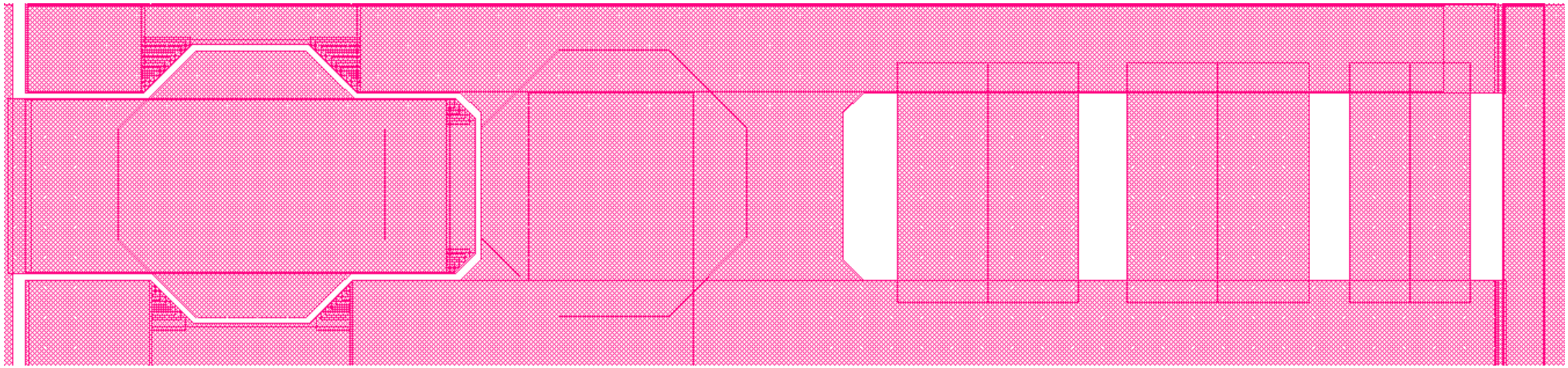


Figure 7.40 : NMOS unit pass device metal 5.

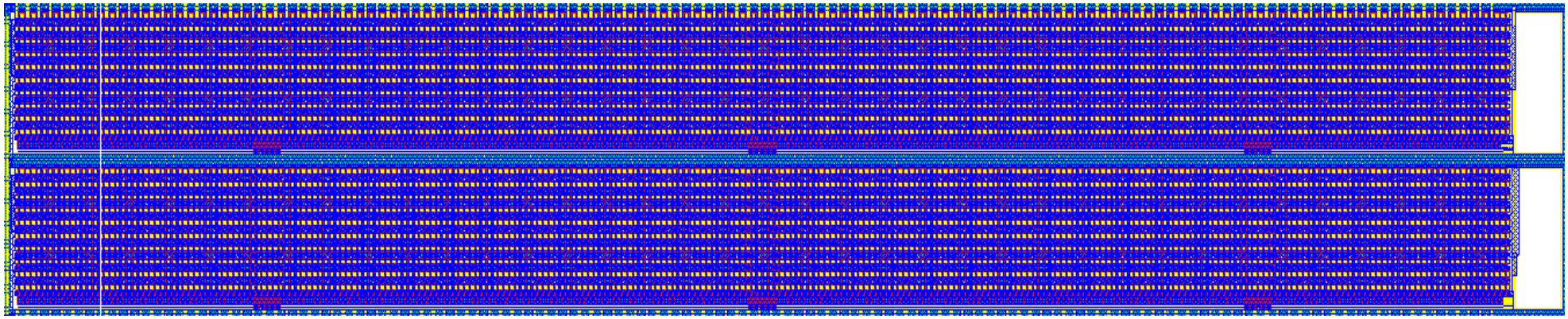


Figure 7.41 : PMOS unit pass device base layer and metal 1.

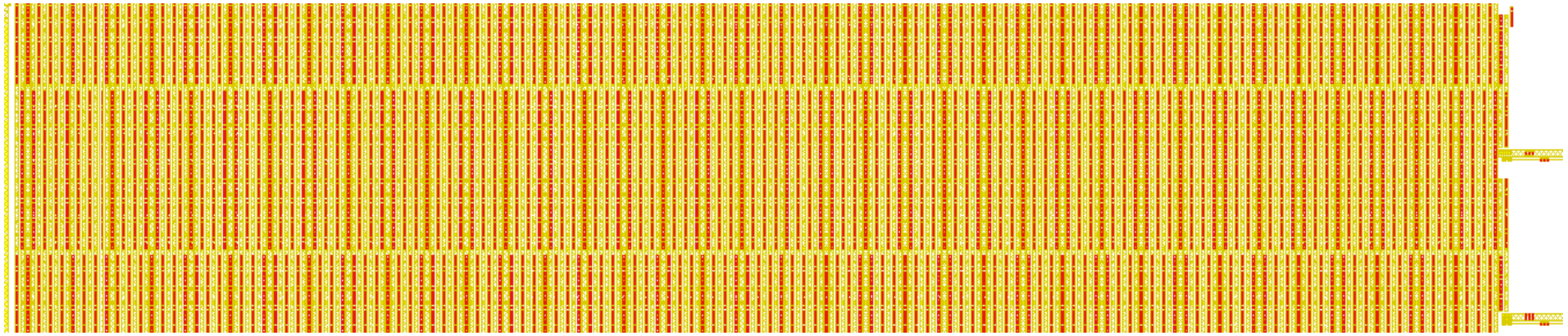


Figure 7.42 : PMOS unit pass device with metal 2.

Figure 7.43 : PMOS unit pass device with metal 3.

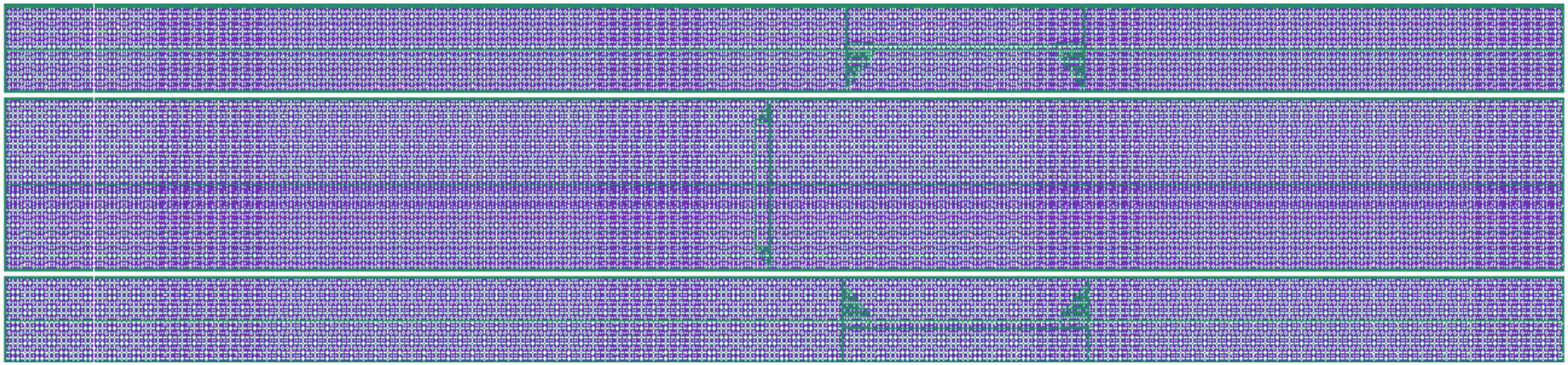


Figure 7.44 : PMOS unit pass device with metal 4.

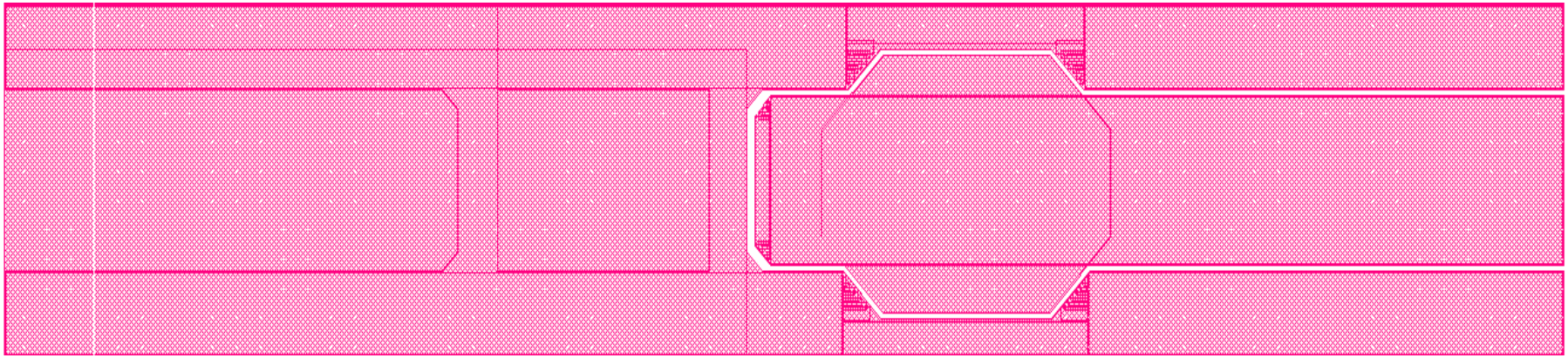


Figure 7.45 : PMOS unit pass device with metal 5.

Figure 7.36, Figure 7.37, Figure 7.38, Figure 7.39 and Figure 7.40 shows unit pass device for NMOS from metal 1 to metal 5, respectively. Due to unit pass device size, contacts are hard to recognize from figures. Contacts are placed as much as possible and from one end to another with width same as metal lines. It can be seen metal 5 (Figure 7.40) line has a bit weird shape, it is because there is an opening for outside connection for chip. This opening has one for each unit device with one end for vss in NMOS part and vdd for PMOS part. Also, there is an opening for node called LX which goes to inductor that is outside of chip.

Having large metal lines might create metal density errors. Workaround solution of this error is to open some metal slots in metal lines. This metal slots can be easily seen in Figure 7.40. Distance between two metal line space might not be enough to satisfy density error, then metal slots should be created.

Metal structures for PMOS part is shown in figures between Figure 7.41 to Figure 7.45. Height of unit pmos part is structured as same with NMOS part to allign the unit device block. This also helps to cascade units to create whole pass device.

Figure 7.46 shows completed buck pass device layout with unit size pass device and their pre-driver block in the middle of NMOS and PMOS pass device. It is designed with 10 unit pass device cascaded one below other. Total area of whole pass device consumes around 800µ x 650µ.

Pass device units are surrounded by wide guard rings both ntap and ptap rings one surrounds other. This is done for NMOS part with wide ptap ring then wide ntap ring, again wide ptap ring to prevent or reduce noise to effect other analog block that are close to pass device.

NMOS and PMOS pass device parts are isolated by deep n-well structure explained in previous sections. This structure greatly reduce noise of pass device also protects pass device of buck converter.

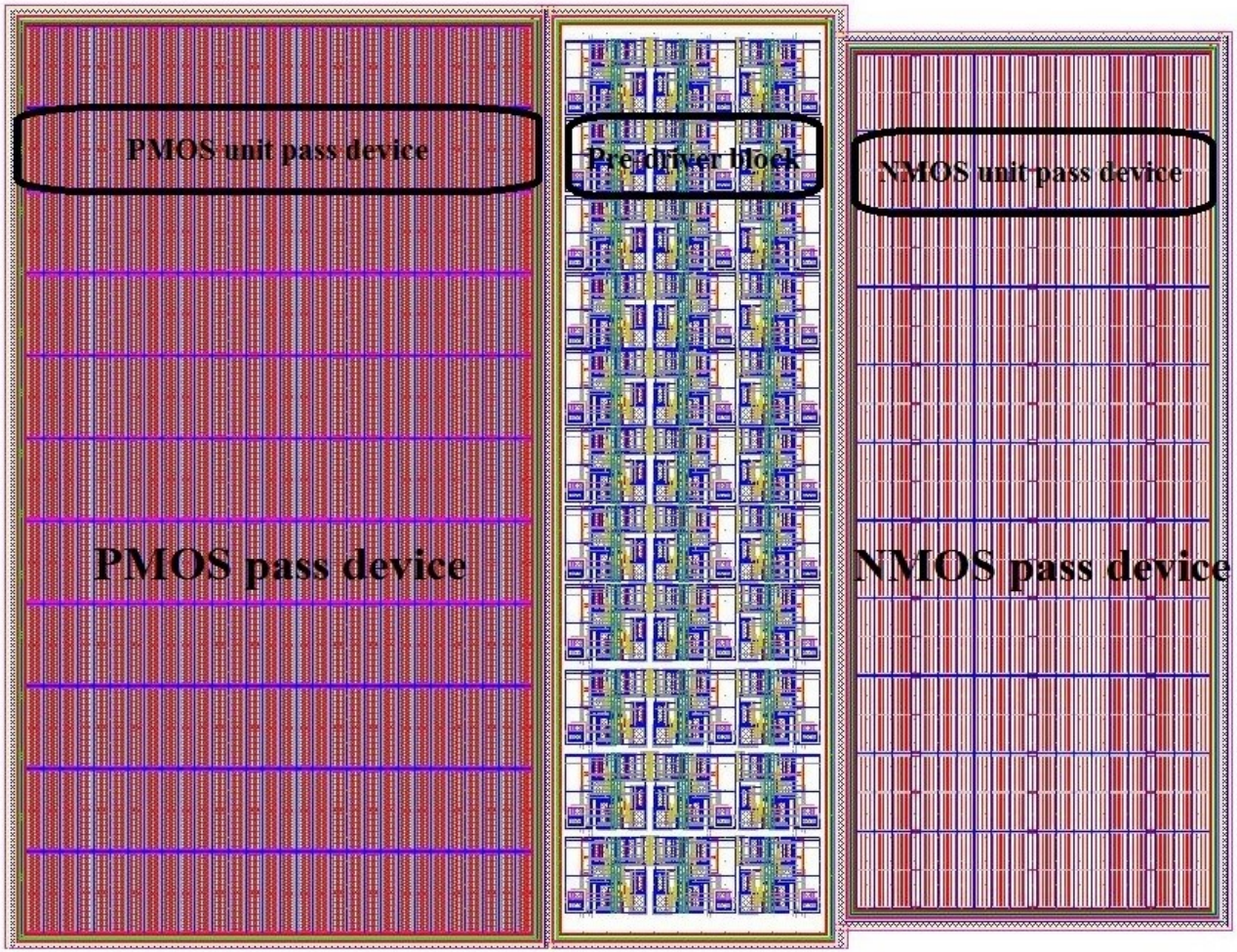


Figure 7.46 : Pass device layout with its drivers.

7.8 Current Sense Block

Current sense is one of the blocks which need to be designed together with output stage/pass devices. The basic principle is the following; a small replica of the main PMOS pass device is realized and current sense block senses the current on this small replica which replicates the coil current information, Figure 7.47. Therefore, it is also important to have a matching between the main pass device and the small replica of it to be able to have good sense ratio

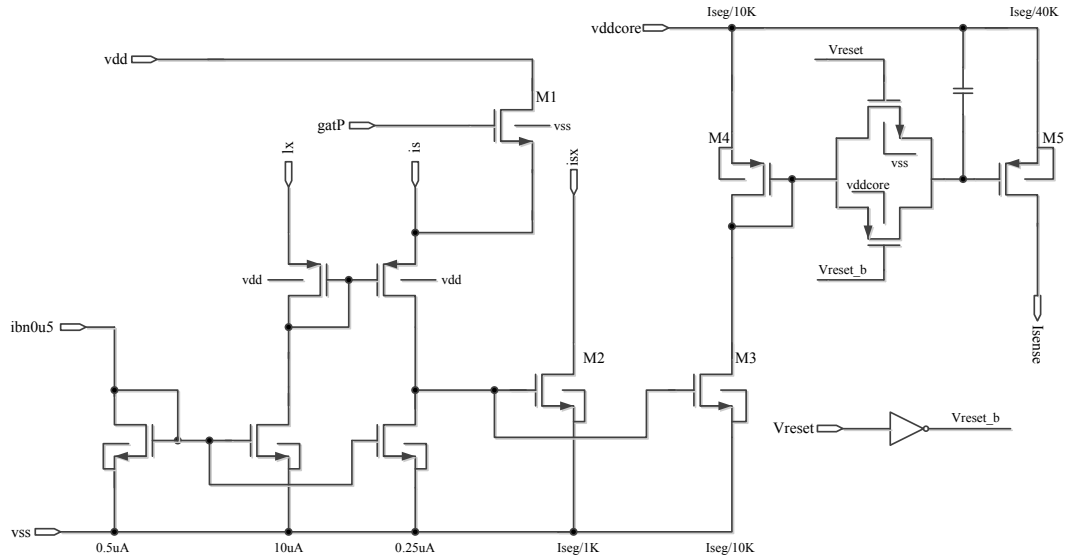


Figure 7.47 : Schematic of current sense block [60].

Since sence device replica mosfet devices are integrated into pass device, rest of devices in schematic is placed after deep n-well ring. Because of seperated parts, layout current sense block is not possible with figures.

7.9 Buck Converter Layout

All sub blocks that builds up buck converter is explained and demonstrated. Blocks are analyzed in terms of layout strategies. Differential pairs, current pairs, sensitive blocks and pass device.

Now let's look at the buck converter in total. Finished layout of buck converter is 800µ x 870µ. As from previous section, pass device itself covers 2/3rd of total buck converter layout.. This again shows the importance of layout of pass device.

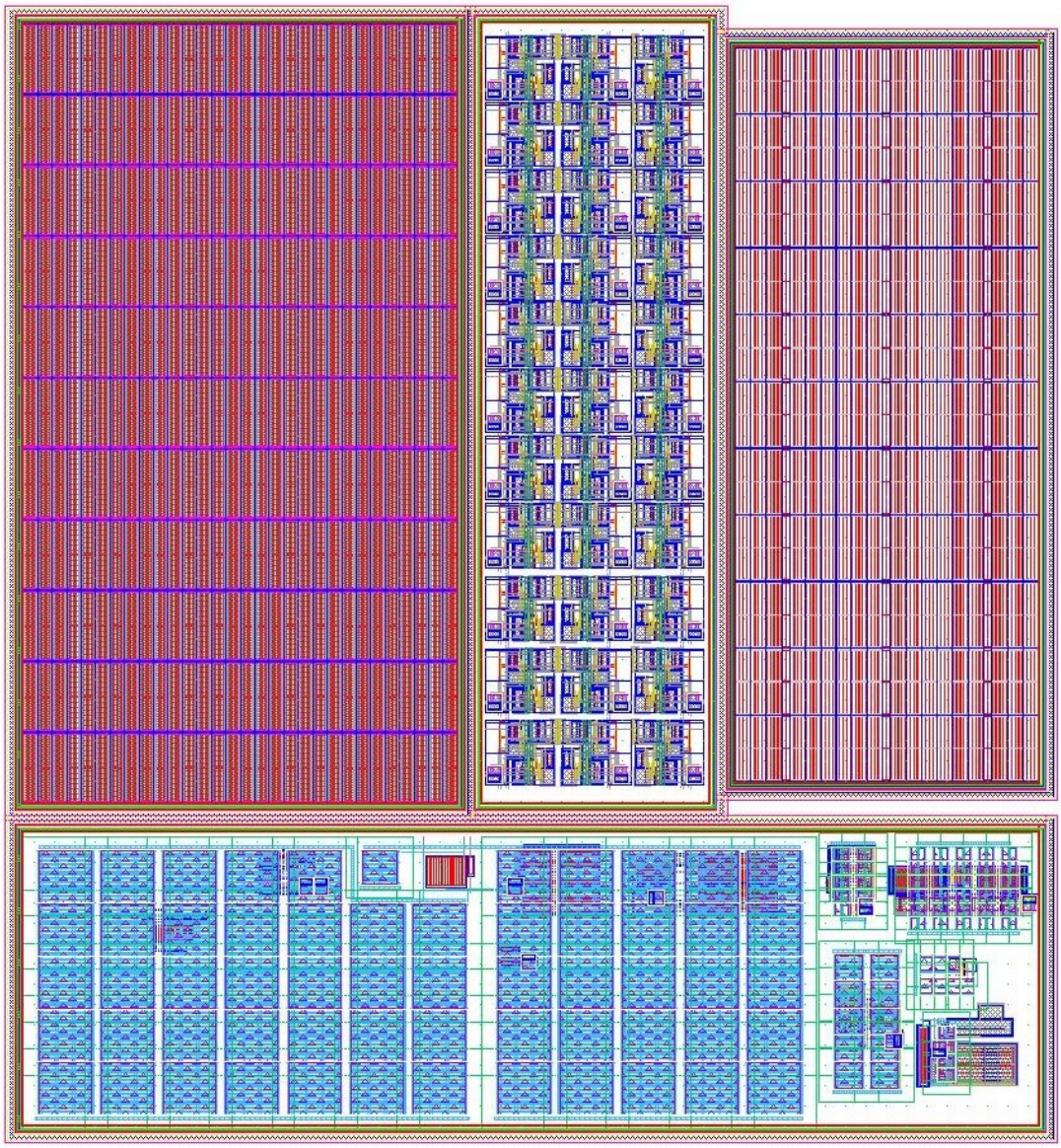


Figure 7.48 : Complete layout of buck converter.

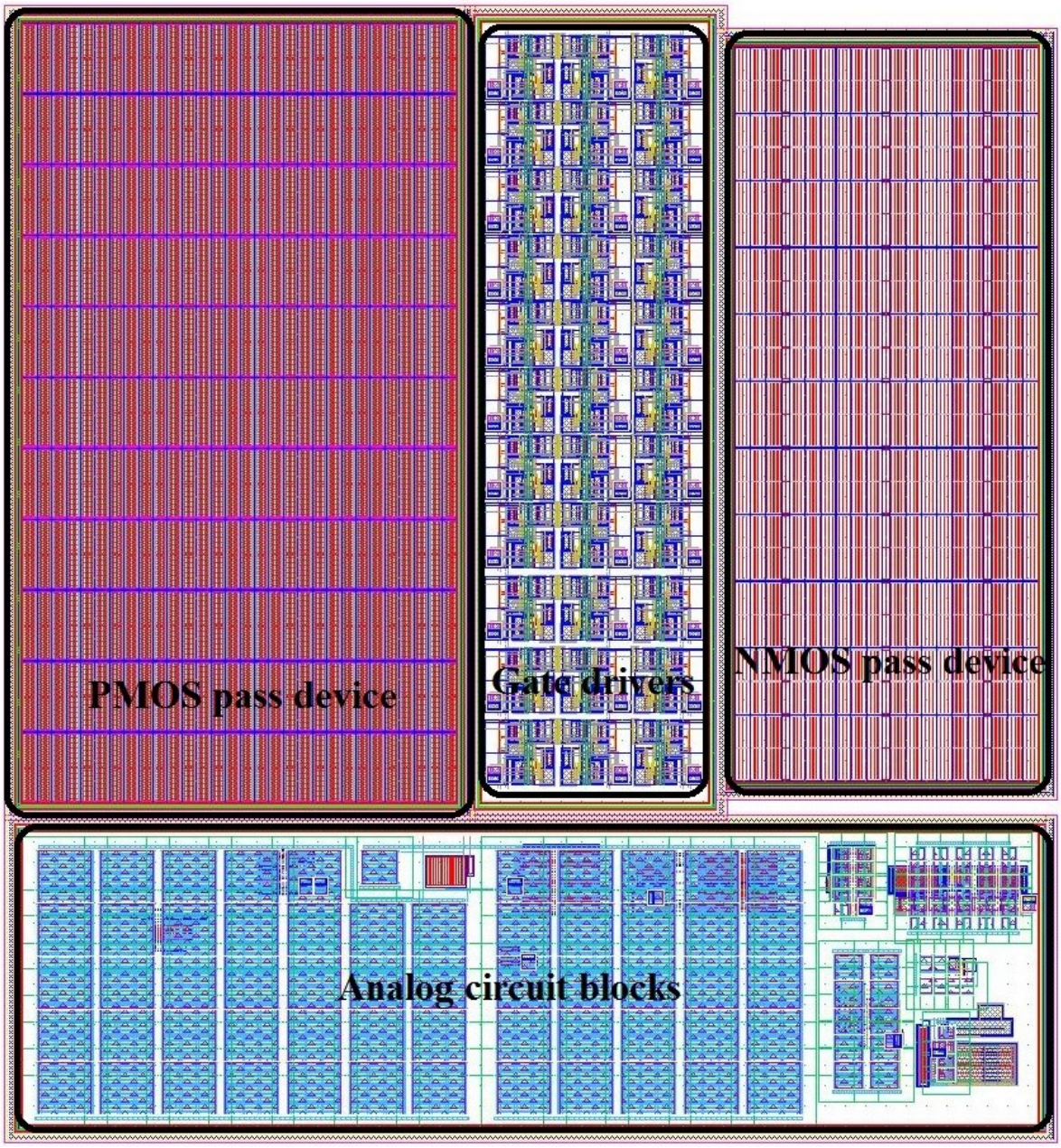


Figure 7.49 : Buck converter blocks.

Figure 7.48 shows the pass device of buck converter and all other blocks stated as analog control blocks. As seen in Figure 7.49, pass device consists a major area with its pass device mosfets and metallizations.

8. ANALYSIS AND OPTIMIZATION OF METAL INTERCONNECTS IN LARGE-AREA POWER MOSFETs

The layout of a pass device contains a huge number of small components such as metal lines, vias, contacts, bond-pads, wirebonds and devices. Since there exist series and distributed resistive components in the interconnects between the silicon and its package, a power device will experience undesired parasitic effects as it carries high current. These parasitic effects are IxR voltage drop, current crowding, metal debiasing effect, and high on-resistance ($_{Rds,on}$) [64-67]. Furthermore, the uneven current distribution in a power device can result in localized heating, electromigration, and other reliability concerns [68]. The parasitic resistances in the interconnect becomes more critical in a large-area power device, which is designed to carry a large amount of current with a very low $R_{ds,on}$ value.

In standard IC design, SPICE device models provided by fabrication foundries are essential to simulating circuit behavior. However, SPICE device models cannot be solely used when simulating a large-area power device because the parasitic resistances in the interconnect are not included in the device models. There exist commercial tools for RC parasitic extractions for post-layout simulations, such as Assura QRC, Calibre PEX and Star RCX. Nevertheless, they are not capable of handling the layout of power interconnects due to complexities of size and geometry of the layout, and multi-dimensional nature of the current flow [69]. There are also Technology Computer-Aided Design (TCAD) tools which are widely used to develop and optimize semiconductor processing technologies and devices. The size and the complexity of geometry in the power interconnects make the TCAD simulation tools unsuitable for large-area power device simulations. Therefore, the performance degradation due to parasitic effects should be thoroughly analyzed by using customized layout modeling methods in the case of designing a large-area power device.

8.1 Physics of Current Flow in Interconnects

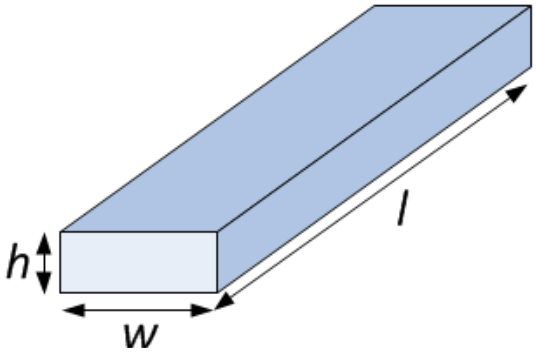
The physics of current flow in interconnects simply follows the Ohm's law. In linear media, the conduction current density is proportional to the applied electric field:

$$\bar{J} = \sigma . \boldsymbol{E} = \frac{\boldsymbol{E}}{\rho} \; [A/m^2] \qquad \textbf{(8.1)}$$

where $\bar{J}$ is the current density, $\boldsymbol{E}$ is the electric field, $\sigma = 1/\rho$ is the conductivity and ρ is the resistivity of the material. A table of resistivity and conductivity of most common materials used in metal interconnects are as listed in Table 8.1

Table 8.1 : Resistivity and Conductivity of materials used in metal interconnects.

Material	ρ [Ω.m]	σ [S/m]
Aluminium	2.83×10^{-8}	3.53×10^{7}
Copper	1.69×10^{-8}	5.8×10^{7}
Nickel	7.24×10^{-8}	1.38×10^{7}



$$R = \rho \cdot \frac{l}{w \cdot h}$$

Figure 8.1 : Resistance of a straight piece of metal.

Consider a straight piece of metal with a cross section area, *A* (w x h), and length, *l*, as shown in Figure 8.1. If a voltage, *V*, is applied between the ends of the metal, a uniform electric field of $\boldsymbol{E}=V/l$ exits in the conducting material and generates a current density, $j=E/\rho$. Then, the total current, *I*, through the material is:

$$I = \int_A \vec{j} \cdot ds = j \cdot w \cdot h = \frac{V \cdot w \cdot h}{\rho \cdot l} \qquad \textbf{(8.2)}$$

Also, the resistance is defined as follows:

$$R = \rho \cdot \frac{l}{w \cdot h} \tag{8.3}$$

Where R is the resistance of the metal piece.

Calculating the resistance of a metal piece is trivial, when the assumption of uniform current flow is made as seen in current equation above. However, the geometrical complexity of the metal interconnects introduces difficulties in accurately modeling the parasitic resistances. Moreover, the uniform current density assumption cannot be applied to a large piece of metal due to the current crowding effect. For example, when the current exits from the metal to a contact, current crowding around the contact occurs. The current then bends upward to exit through the surface of the metal, and it crowds toward the inside edges of the contact (see Figure 8.2). This current crowding produces a slight increase in the overall resistance. Therefore, when modeling the metal interconnects, the assumption of uniform current density should be made only for small pieces of metals.

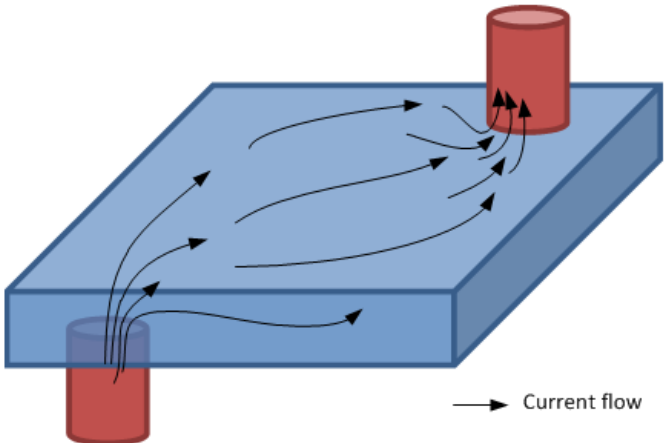


Figure 8.2 : Current crowding effect near the contacts [64].

For more accurate modeling of current flow in the metal interconnects, finite element analysis should be used for solving the basic charge conservation equation:

$$\nabla \cdot \left(\sigma(x,y,z)\nabla V(x,y,z)\right) = 0 \tag{8.4}$$

Where σ is the conductivity of the media, and V is the electrostatic potential at location (x,y,z). In order to apply finite element analysis, the device regions must be

divided into units (elements) using a 3D mesh (or grid). Figure 8.3 shows a 3D mesh of a metal interconnect generated by Synopsys TCAD tools. The potential values at the nodes of each element are approximated with an elemental interpolation and a user-specified potential as a boundary condition [70]. The current density at each node of elements is then solved by using finite deference method with the aid of a computer program.

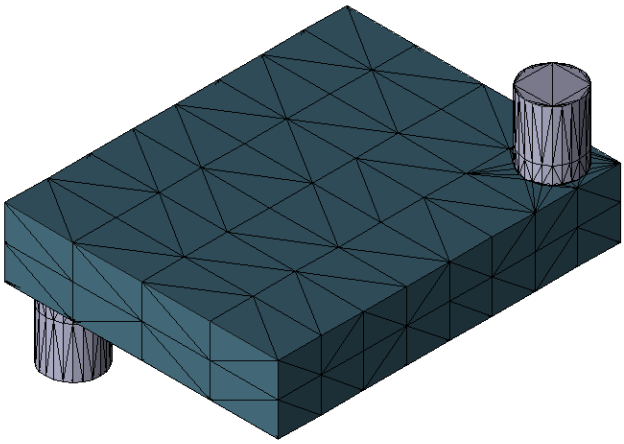


Figure 8.3 : 3D mesh of a metal interconnect (Synopsys TCAD tool).

8.2 SPICE Lumped-Element Layout Modelling

Although power MOSFETs are specifically designed for carrying a large amount of power, the same finger layouts used to construct small-signal transistors serve equally well for power applications. Figure 8.4 shows a MOS finger and a basic MOS multi-finger layout that are most frequently used to construct a large gate width transistor. Scalable SPICE models for MOS transistors are typically provided by fabrication foundries, but the parasitic resistances and capacitances from the interconnect are not included in the models. Because the automatic parasitic extraction followed by the post-layout SPICE simulation is not a viable solution for designing large-area power MOSFETs, the parasitic resistances of the interconnects should be identified manually with an assumption of uniform current flow in a small piece of metal. Then, the resistance value for each parasitic component can be calculated by using the sheet resistance table, which is provided by the foundry.

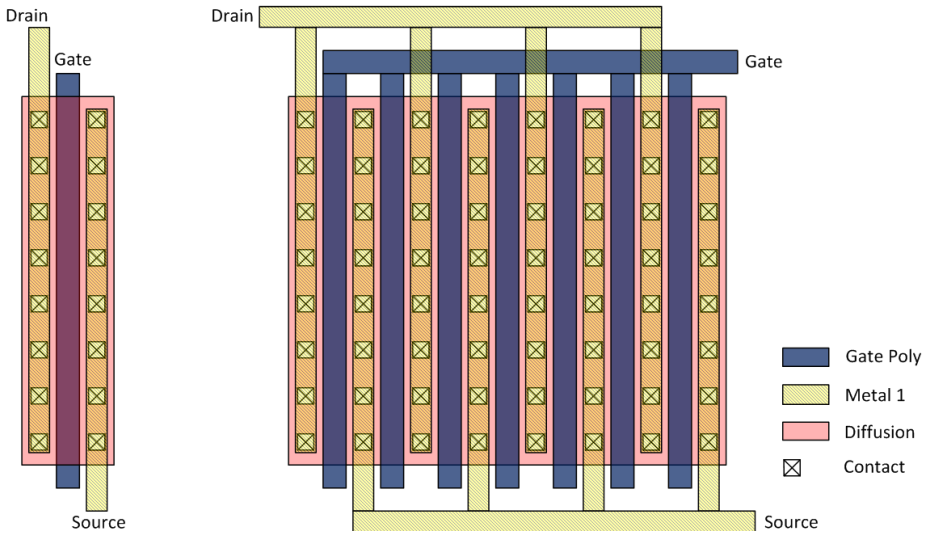


Figure 8.4 : Single MOS finger layout (left), basic MOS multi-finger layout [64].

Figure 8.5 shows an example of a SPICE lumped-element model with parasitic resistances in its contacts and metal 1 source/drain runners. A MOS transistor finger is partitioned into many small unit transistors with one contact for each source and drain. Then, the resistive parasitic components are manually inserted into the SPICE netlist.

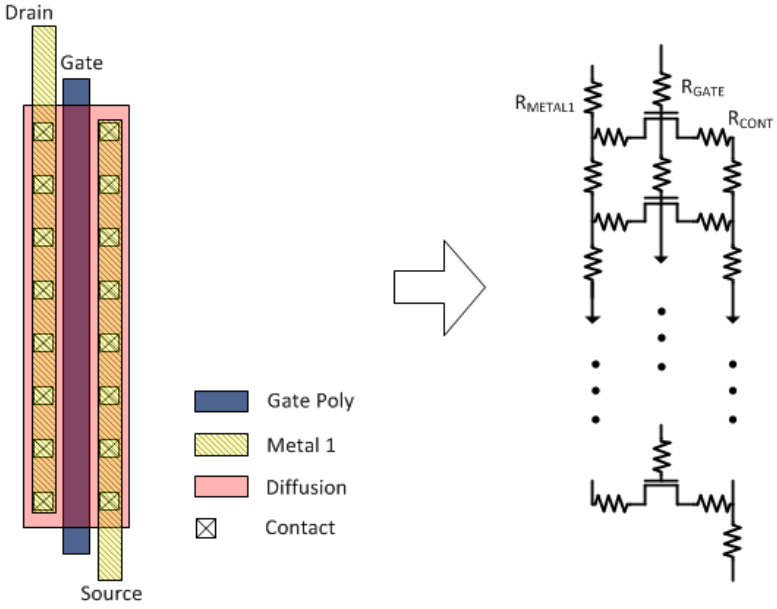


Figure 8.5 : SPICE lumped-element model for a MOS finger with parasitic resistive components.

Using this SPICE lumped-element model, several different circuit simulations have been performed to understand the effects of parasitic interconnect resistances. In this thesis, 0.25 μm BCD technology is used, and standard 5V MOS transistors are used in the simulations.

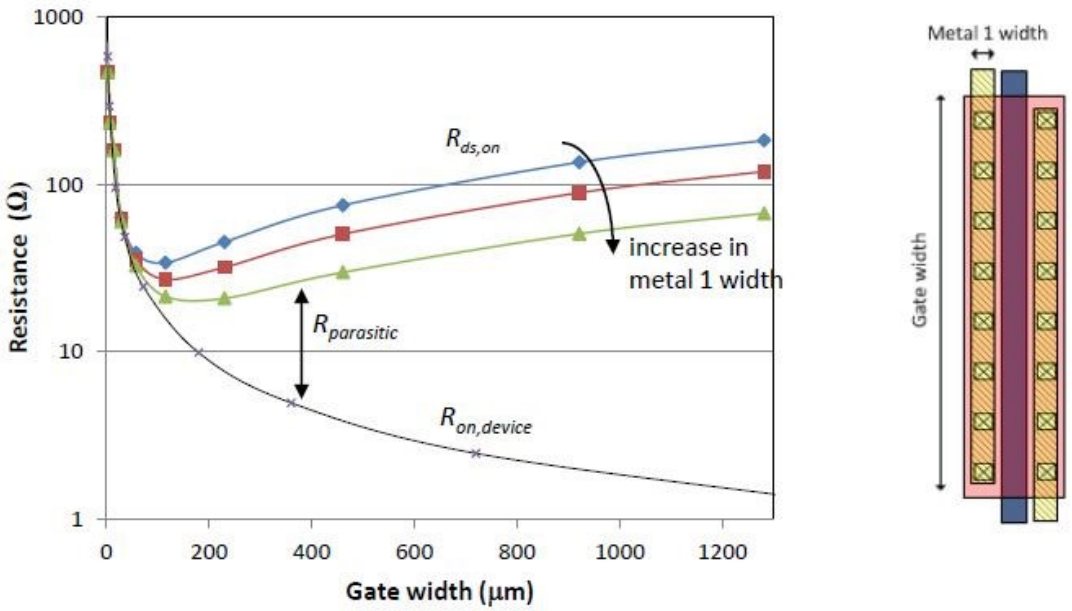


Figure 8.6 : Simulation results of $R_{on,device}$, $R_{ds,on}$ and $R_{parasitic}$ of standard 5V MOS finger using SPICE lumped-element model and layout of it.

Figure 8.6 shows the contribution of parasitic resistance due to contacts and metal-1 source drain runners in a 5 V MOS finger layout. As the gate width increases, the intrinsic device on-resistance ($R_{on,device}$) and the total on-resistance ($R_{ds,on}$) decrease because the intrinsic channel resistance are inversely proportional to the gate width [71]. The parasitic interconnect resistance ($R_{parasitic}$) corresponds to the difference between $R_{ds,on}$ and $R_{on,device}$. When the gate length is below 100 μm, the plot of $R_{ds,on}$ and $R_{on,device}$ are almost identical because $R_{parasitic}$ is relatively small compared to $R_{on,device}$. However, when the gate length increases beyond 100 μm, $R_{ds,on}$ starts to increase gradually while $R_{on,device}$ continues to decrease. This indicates that the parasitic resistance begins contributing more to $R_{ds,on}$. The domination of $R_{parasitic}$ is more pronounced in the longer gate width region.

SPICE lumped-element layout modeling had been used to simulate power MOSFET layouts. However, this method requires designers to manually identify the resistive components in the layout and insert them to the SPICE netlist. Since the width of a power MOSFET can be as large as 100,000 μm or larger depending on applications, the SPICE netlist can easily involve millions of components. Therefore, the simulation time and the accuracy of this simulation largely depend on clever optimization of the SPICE netlist by its designers. This modeling method can be effective when the size of power MOSFETs is small with a few metal layers. Otherwise, it requires a very long and tedious process of setting up the simulation,

which can take up to several days. In addition, SPICE is not optimized for handling such a huge number of components interconnected in a 3- dimensional mesh, thus, the simulation can often result in convergence failures.

In SPICE-based layout modeling, a corner is normally represented with two resistors connected in series. However, due to the current crowding effect, the current density tends to concentrate in the sharp corner which is shown in red in Figure 8.7(b). This produces a slightly higher value of resistance than the simple SPICE model. In addition to the discrepancies in the resistance value due to simplified models, identifying the high current density regions is very important because they are common sources of serious reliability issues. As shown in Figure 8.7(c), the high current density at the corners can be mitigated by using diagonally cornered interconnect. Moreover, the output data of SPICE simulations do not allow easy visualization of the current and voltage information at each node. This visualization is particularly important because it allows the designers to optimize the interconnect layout for more even distributions of the current density over the device area.

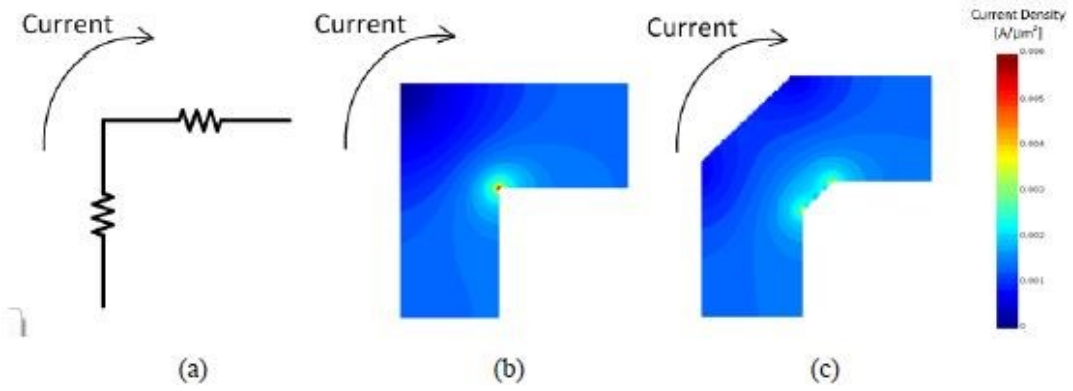


Figure 8.7 : SPICE lumped-element model of a cornered metal interconnect (b) Current density distribution of a cornered metal interconnect (c) Current density distribution of a diagonally cornered metal interconnect.

SPICE-based layout modeling had been previously used in some academic literature because it was the only available approach to analytically investigate the parasitic effects in different power device layouts. However, it encompasses many handicaps, such as the complexity in the process of setting up the simulation, the time and accuracy of simulation, which largely depend on the designer's clever optimization of the SPICE netlist, and the difficulty in processing and visualizing the output data. Therefore, this method is not adopted widely for industrial use.

8.3 R3D Resistive Extraction and Analysis

R3D is a resistance extraction and analysis software developed by Silicon Frontline in 2009. This tool is equipped with a highly efficient iterative matrix solver, which is specifically designed for extraction, simulation, analysis, and optimization of metal interconnects of power semiconductor devices. Figure 8.8 is an illustration of the simulation flow of R3D. R3D reads in a standard layout file (GDSII), process technology files, and generates a 3D model representing all resistive elements of the structure (metal layers, vias/contacts, wire bonds/balls, and device cells). R3D's capability to read GDSII standard data files speeds up the process of setting up the simulation, while the SPICE-based layout modeling requires a large amount of the designer's effort to setup the simulation. R3D also helps minimize human errors which can be possibly associated with the process of setting up the simulation [72].

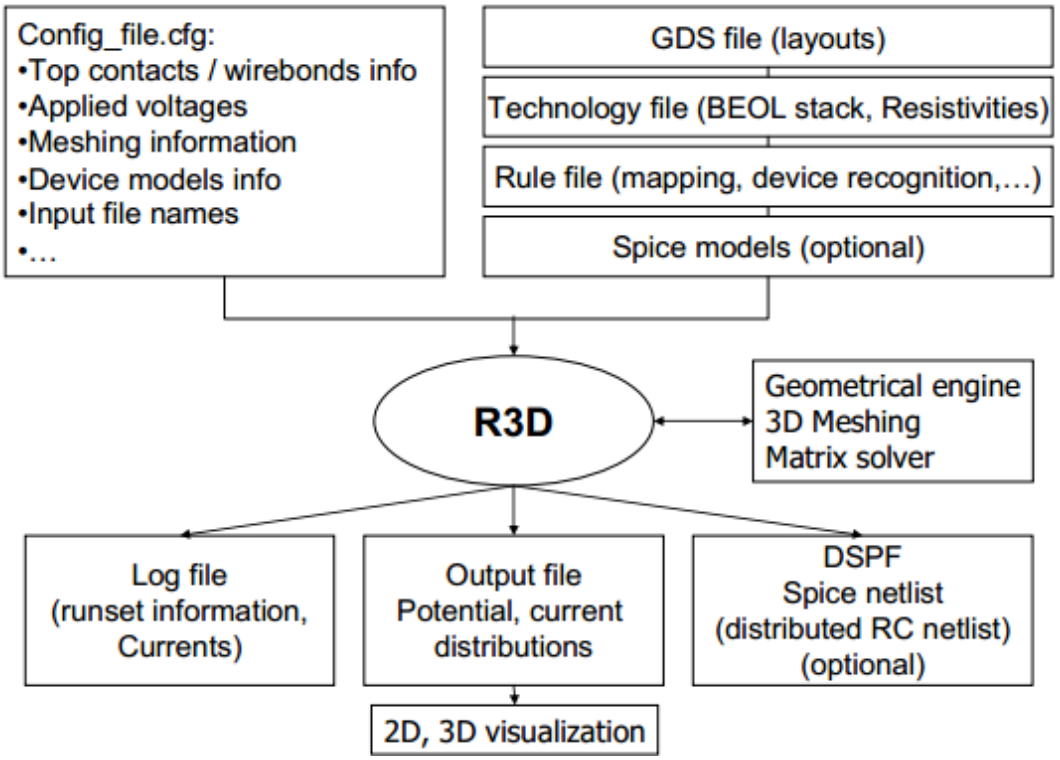


Figure 8.8 : R3D simulation flow diagram.

The layout in the GDSII file is then sub-divided using a 3-dimentional mesh, and current transport equations are solved at each point in the mesh using a finite difference method. The user-specified voltages applied to wire bonds or bond pads are used as boundary conditions in the calculations. R3D is capable of computing the distributions of potential and current densities in all metal layers, vias, contacts, and

devices. In addition, it provides an effective 2D and 3D visualization of the simulated data, and Rds,on value of the power device as the final result.

there exist complicated trade-offs for the performance of power MOSFETS depending on the layout of power MOSFETs, the metal interconnects and the size of the devices. In particular, the effects of parasitic resistances in the interconnects vary greatly depending on the layout techniques, thickness of metal layers, the number of metal layers, termination of source and drain pads, and so on. Therefore, when designing power MOSFETs, the effect of interconnects has to be thoroughly analyzed and optimized. R3D simulation tools also provide visual aid to analyze and optimize metal interconnect layouts.

The usefulness and effectiveness of the R3D simulator has been demonstrated. Layout of pass device of buck converter is simulated by using R3D simulations. The standart metal process option and total 5 metal layers were used. Then, R3D simulations were performed to investigate the difference in the contribution of parasitic resistances on $R_{ds,on}$ due to their structural differences. Since the R3D simulator produces $R_{ds,on}$ values as the final result of simulation from the input GDSII layout files, comparisons between designated $R_{ds,on}$ in schematic (which is $R_{on,device}$ actually) and $R_{on,device} + R_{parasitic}$ which in total $R_{ds,on}$ in layout.

Figure 8.9 shows the R3D result of NMOS pass device. On the right side scale is from 0 to 1.4mA which is a little bit higher than the maximum current that metal 1 can handle. This is because maximum current capability can fall on the orange color scale rather than red color range. Figure 8.10 shows current distribution of metal 2 layer. As it can be seen, in the middle of metal 2 row current gets crowded creating possibility of hotspot. Metal 3 and metal 4 layers in Figure 8.11 and Figure 8.12 also follow the same trend as of metal 2 result. In Figure 8.13, metal 5 layer has less current hotspot possibility. It is because there is RDL (Re-Distribution Layer, which is outside of this thesis scope) routing on top of metal 5 that RDL actually carries current rather than metal 5. So we see less current stress on metal 5. In R3D simulation, threshold can be set for every layer.By setting threshold value, R3D highlights areas where current density exceeds that particular threshold value, Figure 8.14.

Same applies to PMOS pass device part. Figure 8.15 shows metal 2 R3D result. Figure 8.16 shows metal 3 and Figure 8.17 for metal 4, Figure 8.18 for metal 5. Figure 8.19 again shows threshold areas for metal 5 that are more than metal 5 can handle. Threshold highlight may look much but when zoomed in, it can be seen that it is actually point error which is known. This is because of cornered metal interconnect. Even it is done as 45^0 angled routing there are still corner errors on the point of corner. At the end, threshold highlights must be carefully checked to decide whether it is a real hotspot or just point error.

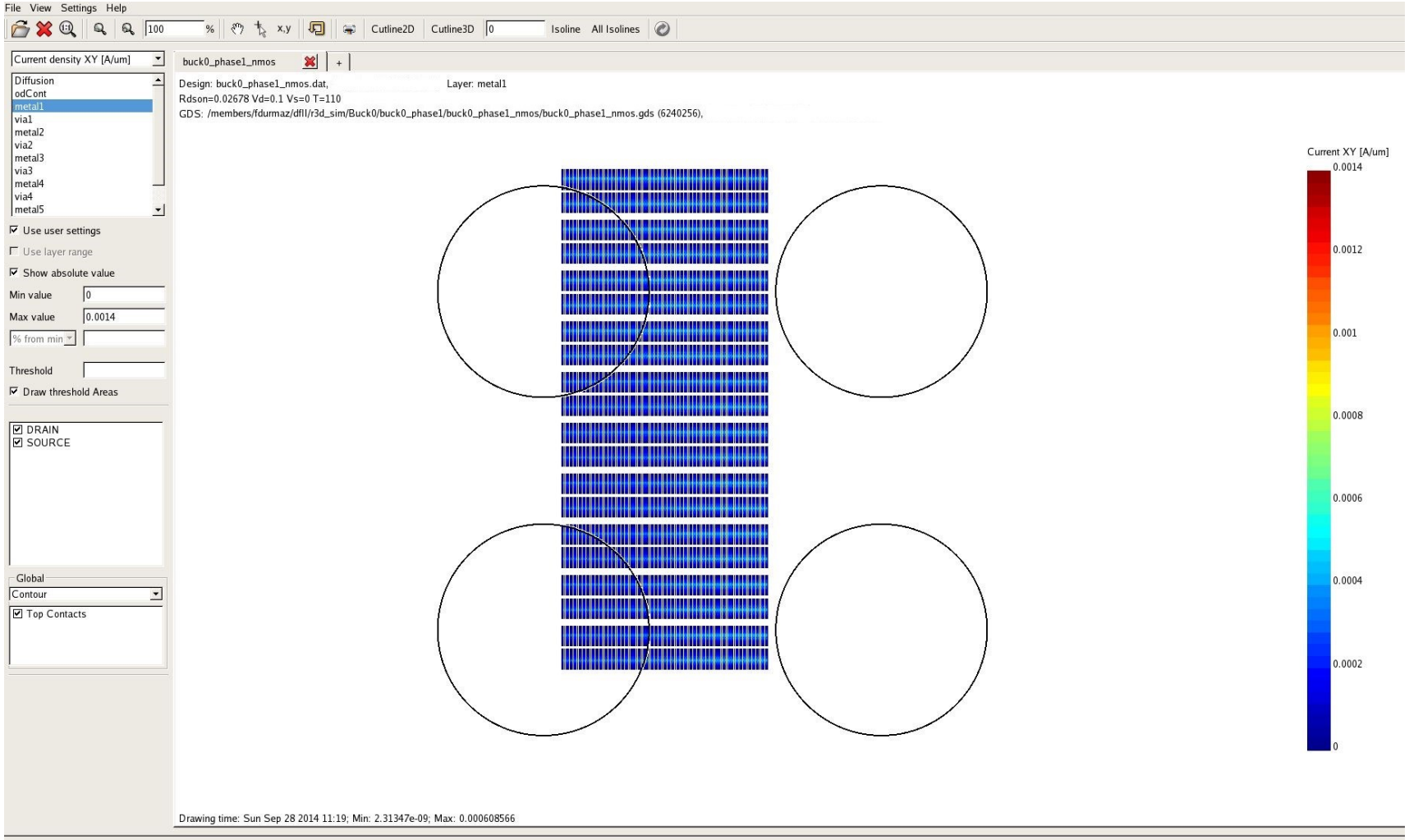


Figure 8.9 : R3D Current distribution of NMOS pass device in metal 1.

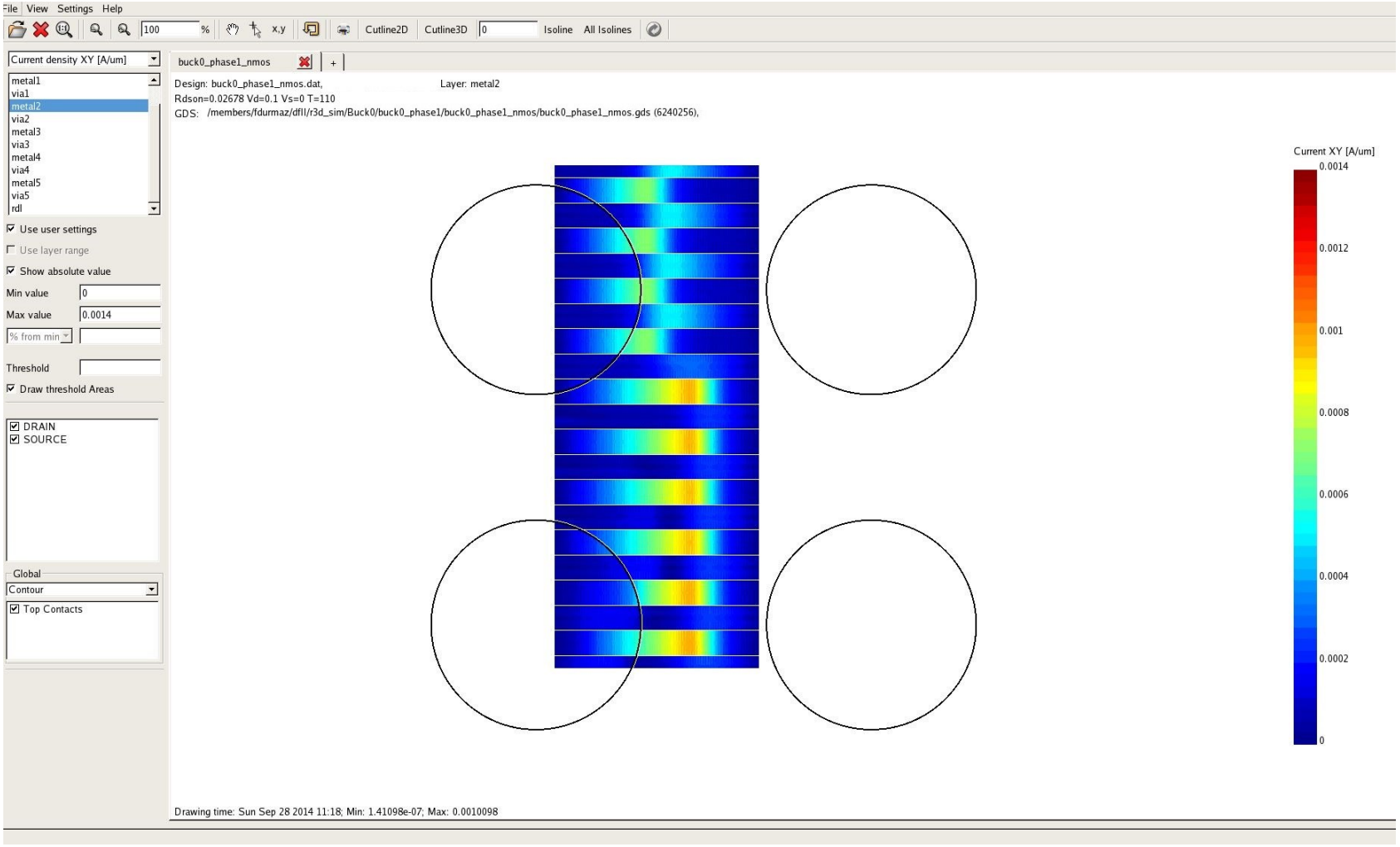


Figure 8.10 : R3D Current distribution of NMOS pass device in metal 2.

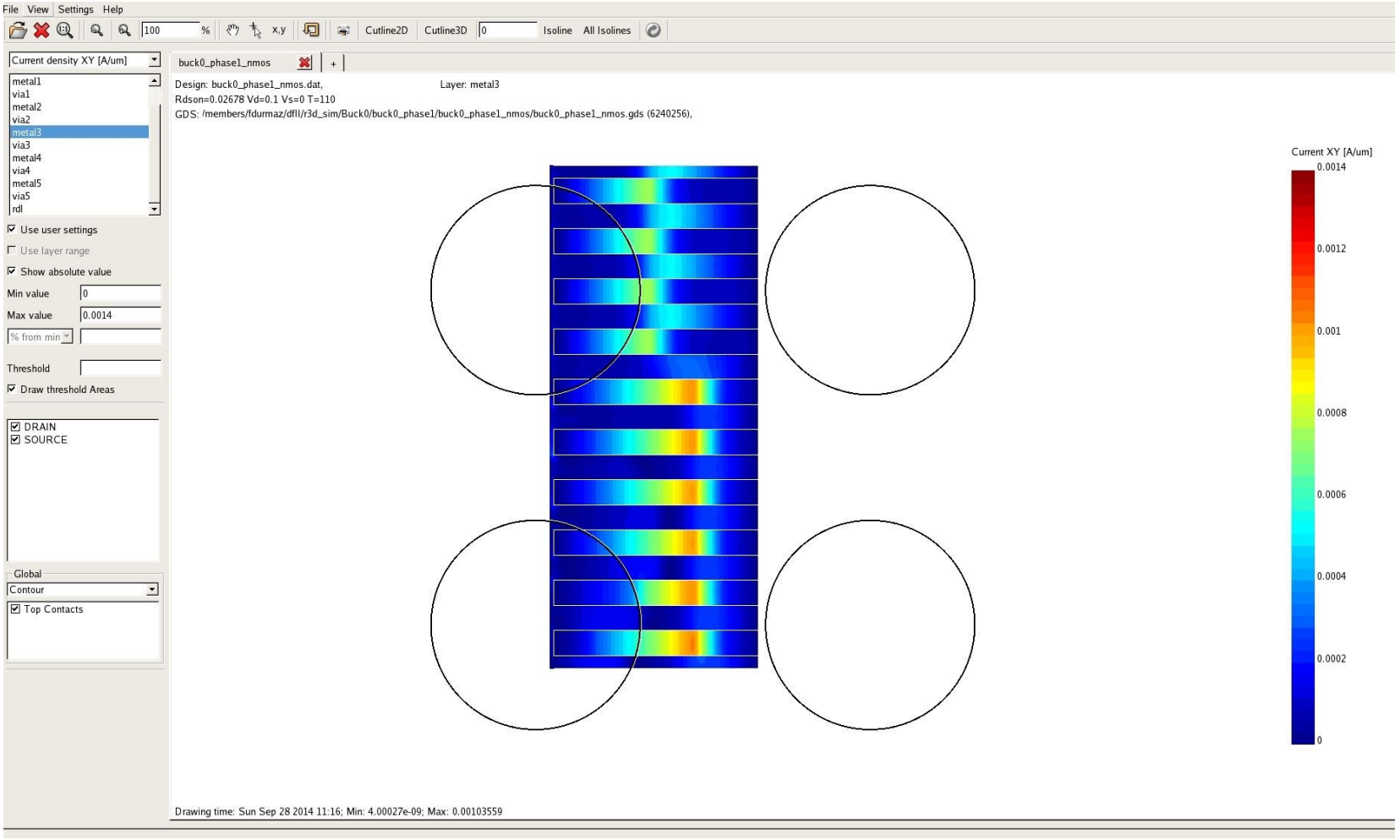


Figure 8.11 : R3D Current distribution of NMOS pass device in metal 3.

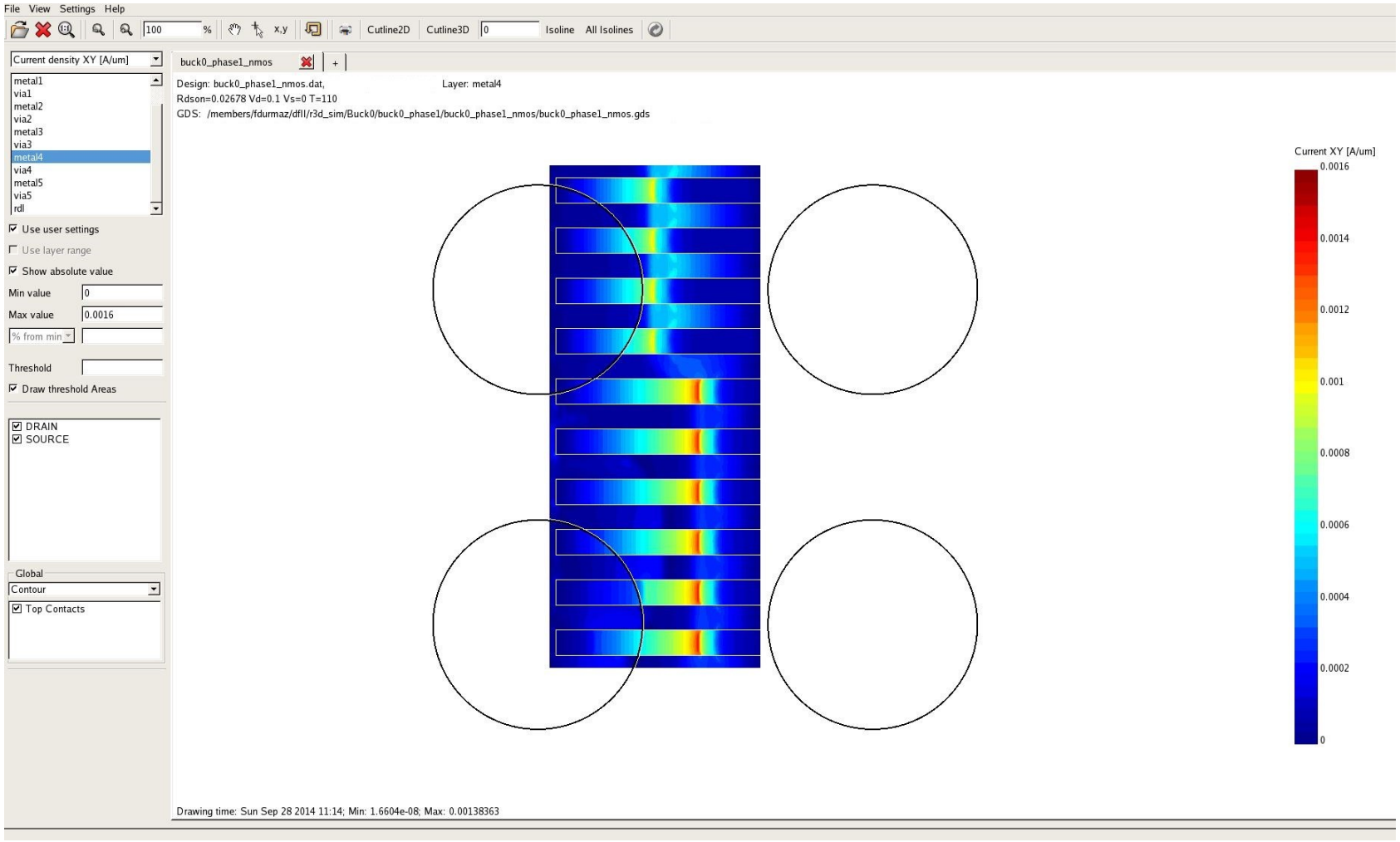


Figure 8.12 : R3D Current distribution of NMOS pass device in metal 4.

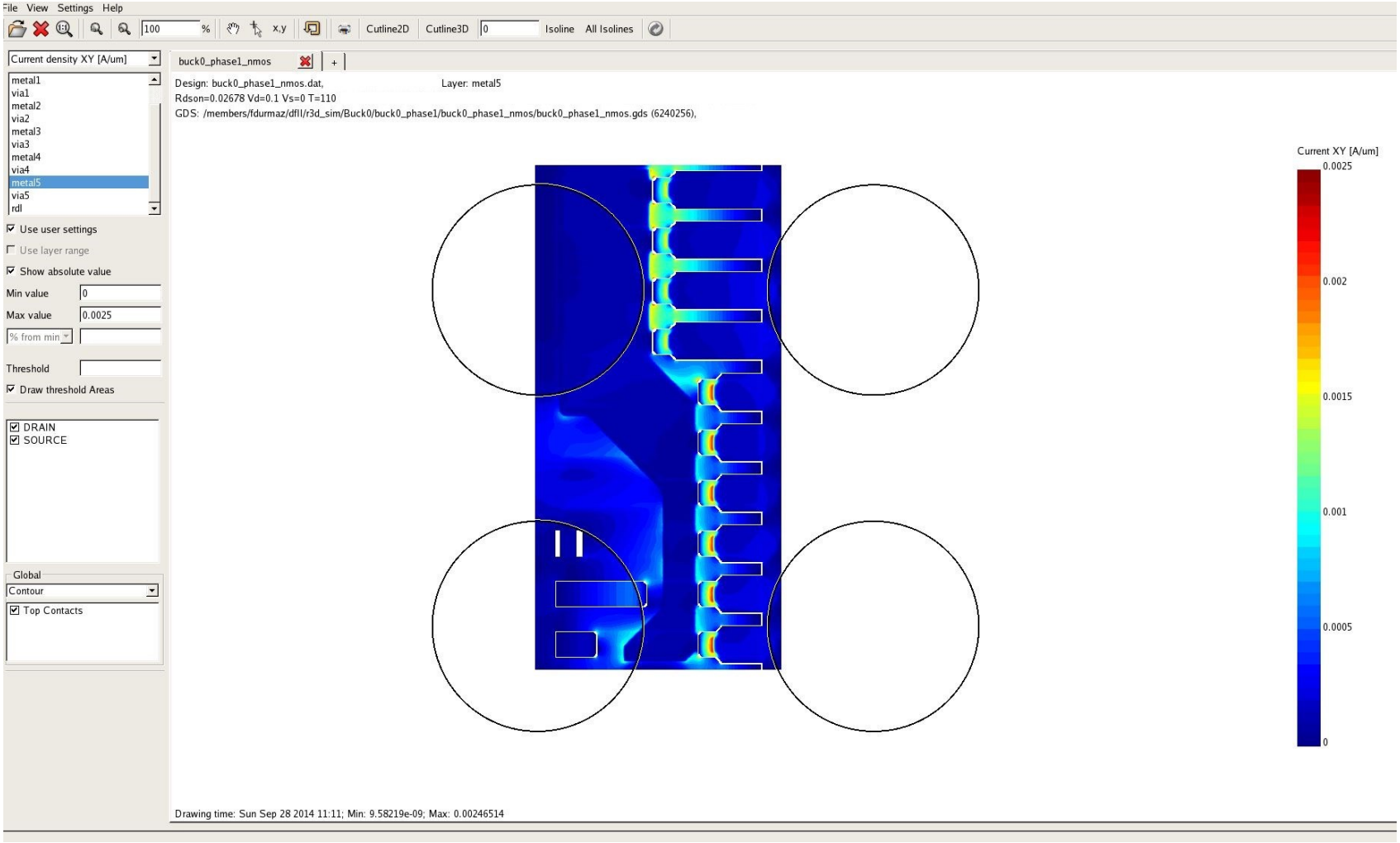


Figure 8.13 : R3D Current distribution of NMOS pass device in metal 5.

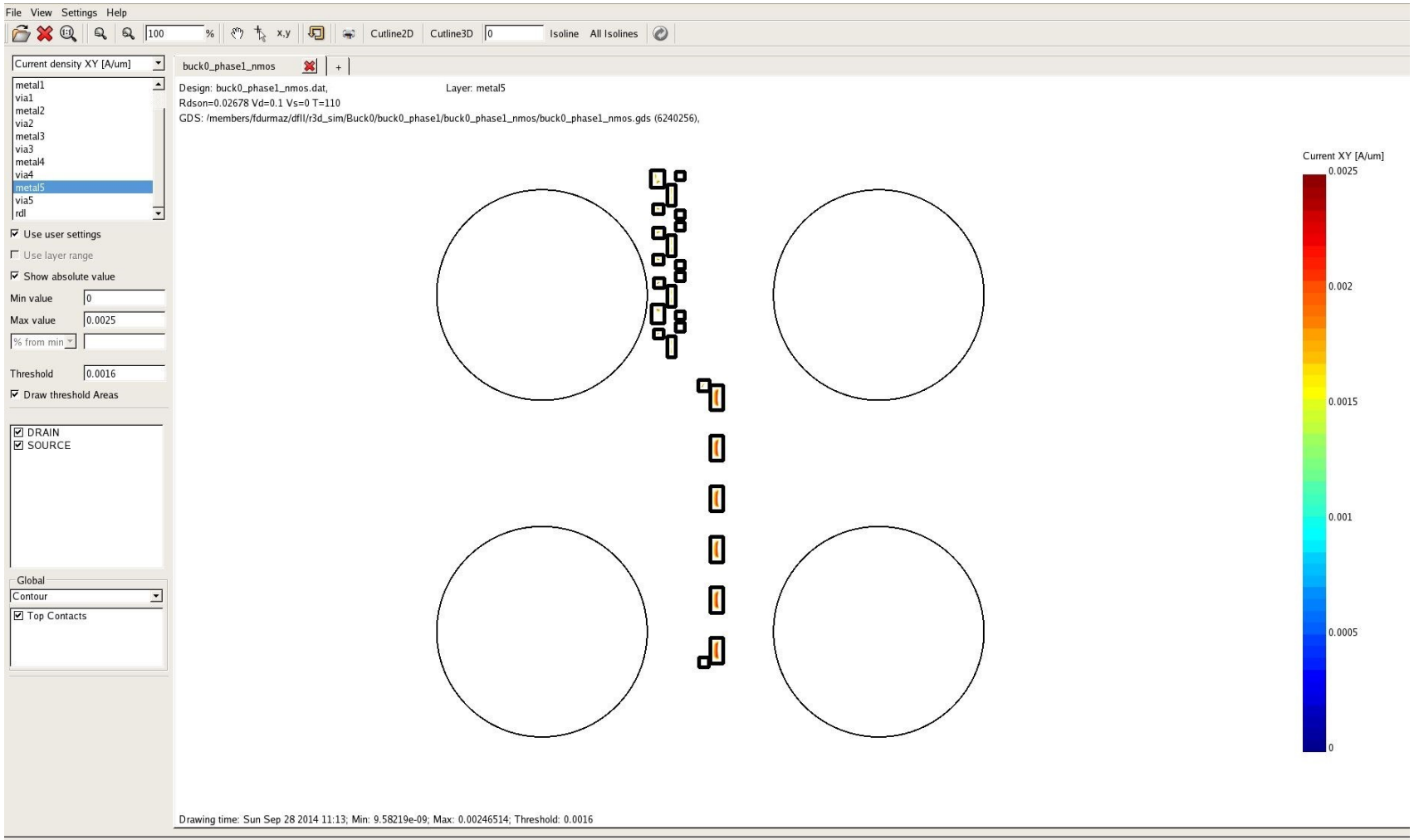


Figure 8.14 : R3D Potential hotspots of NMOS part in metal 5.

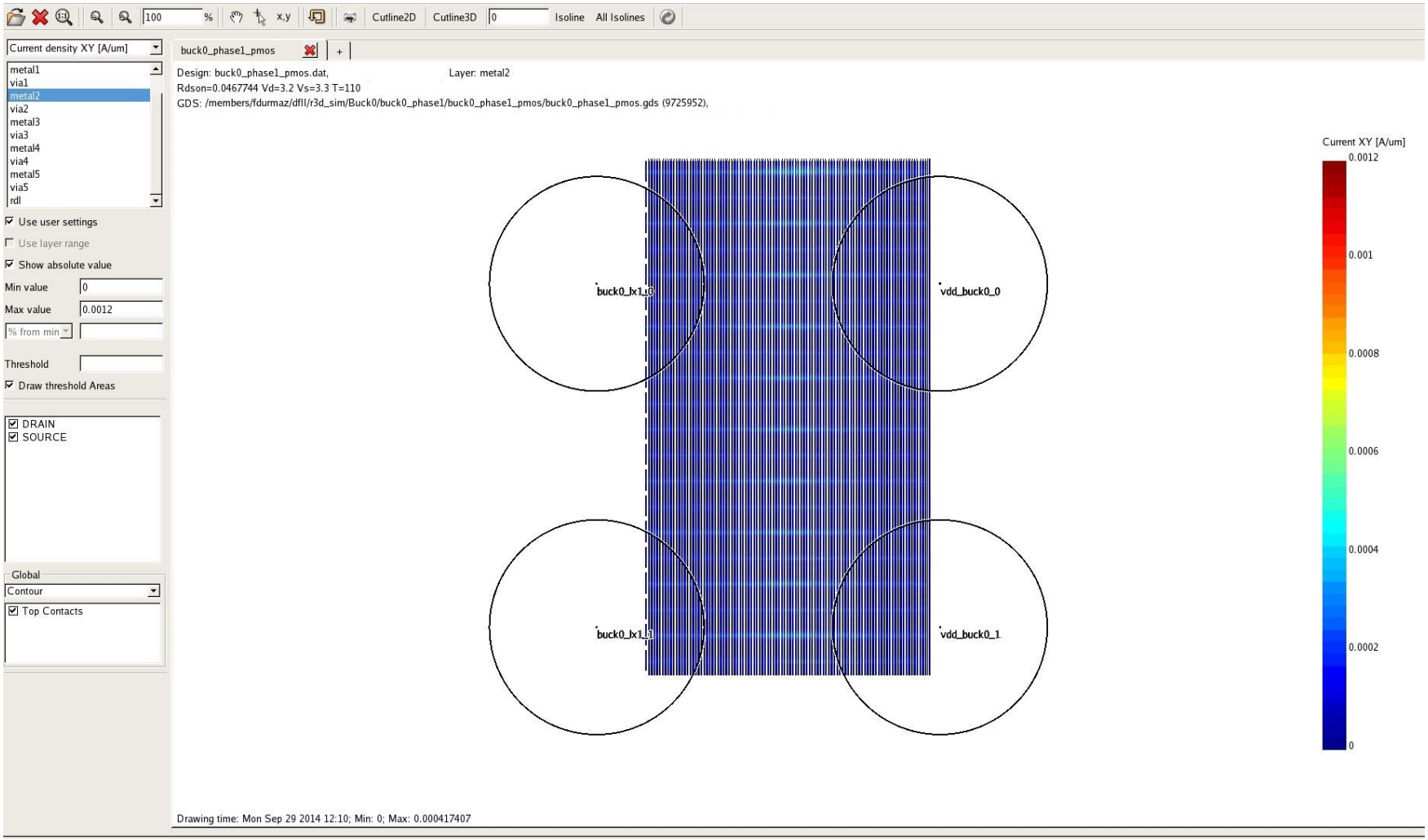


Figure 8.15 : R3D Current distribution of PMOS pass device in metal 2.

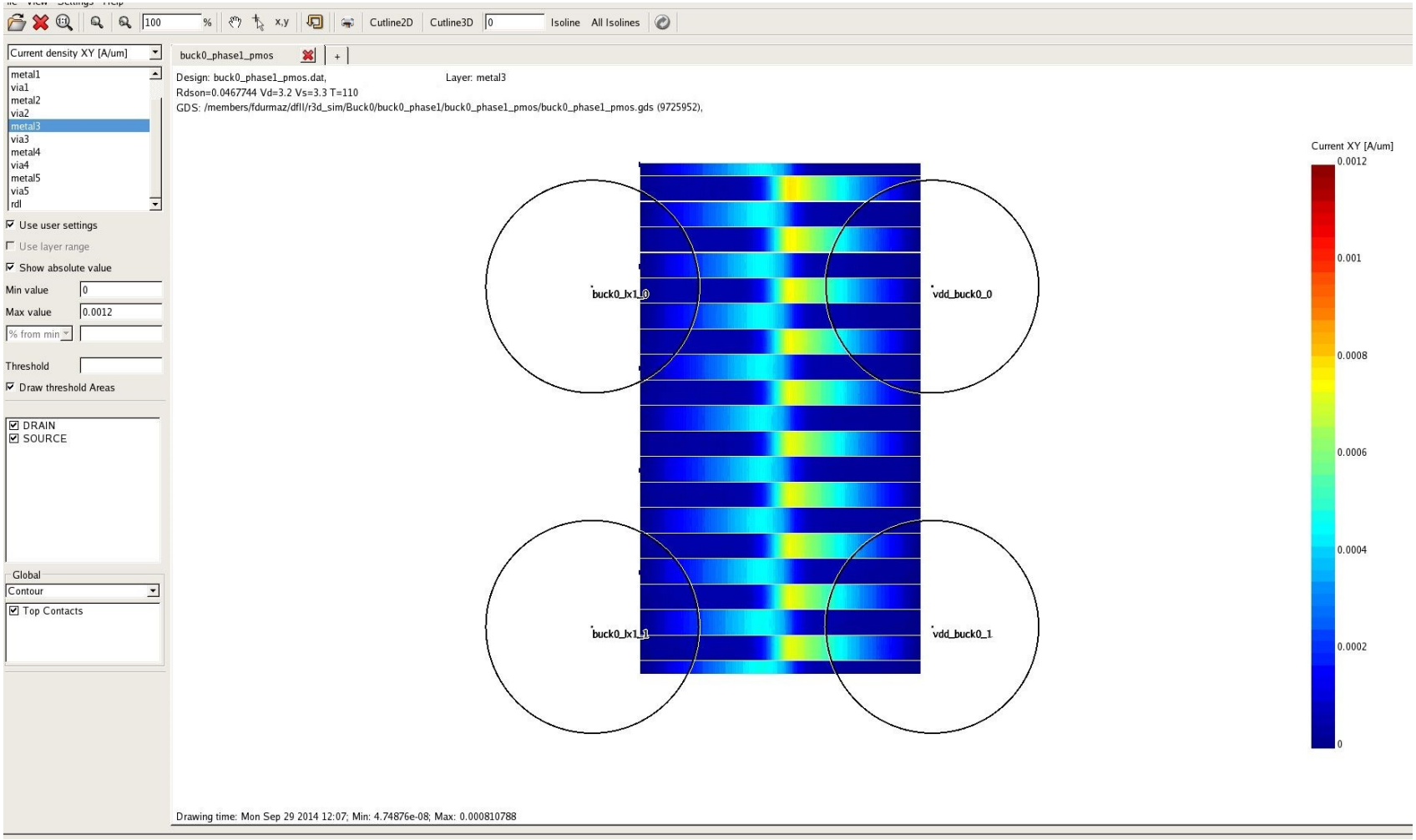


Figure 8.16 : R3D Current distribution of PMOS pass device in metal 3.

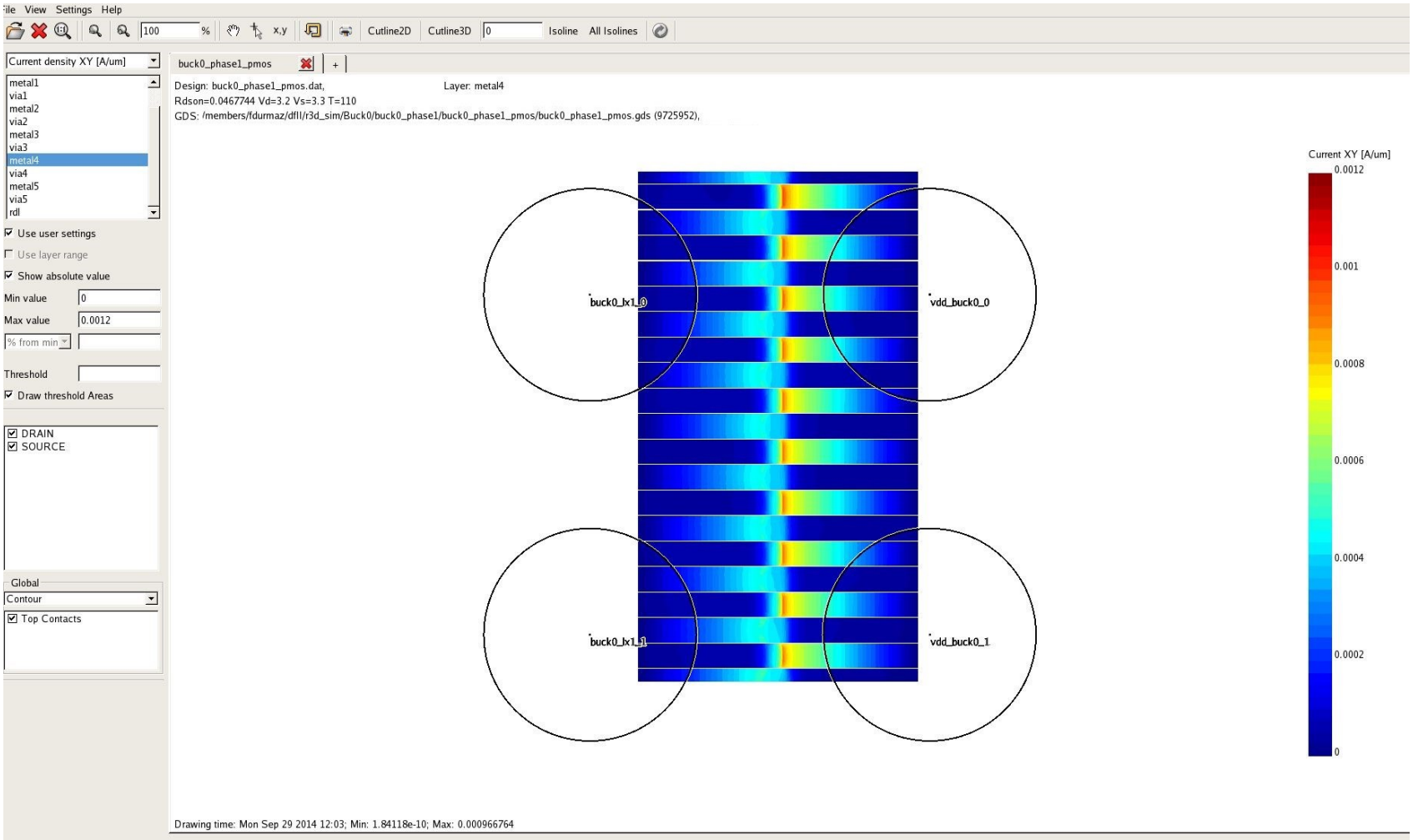


Figure 8.17 : R3D Current distribution of PMOS pass device in metal 4.

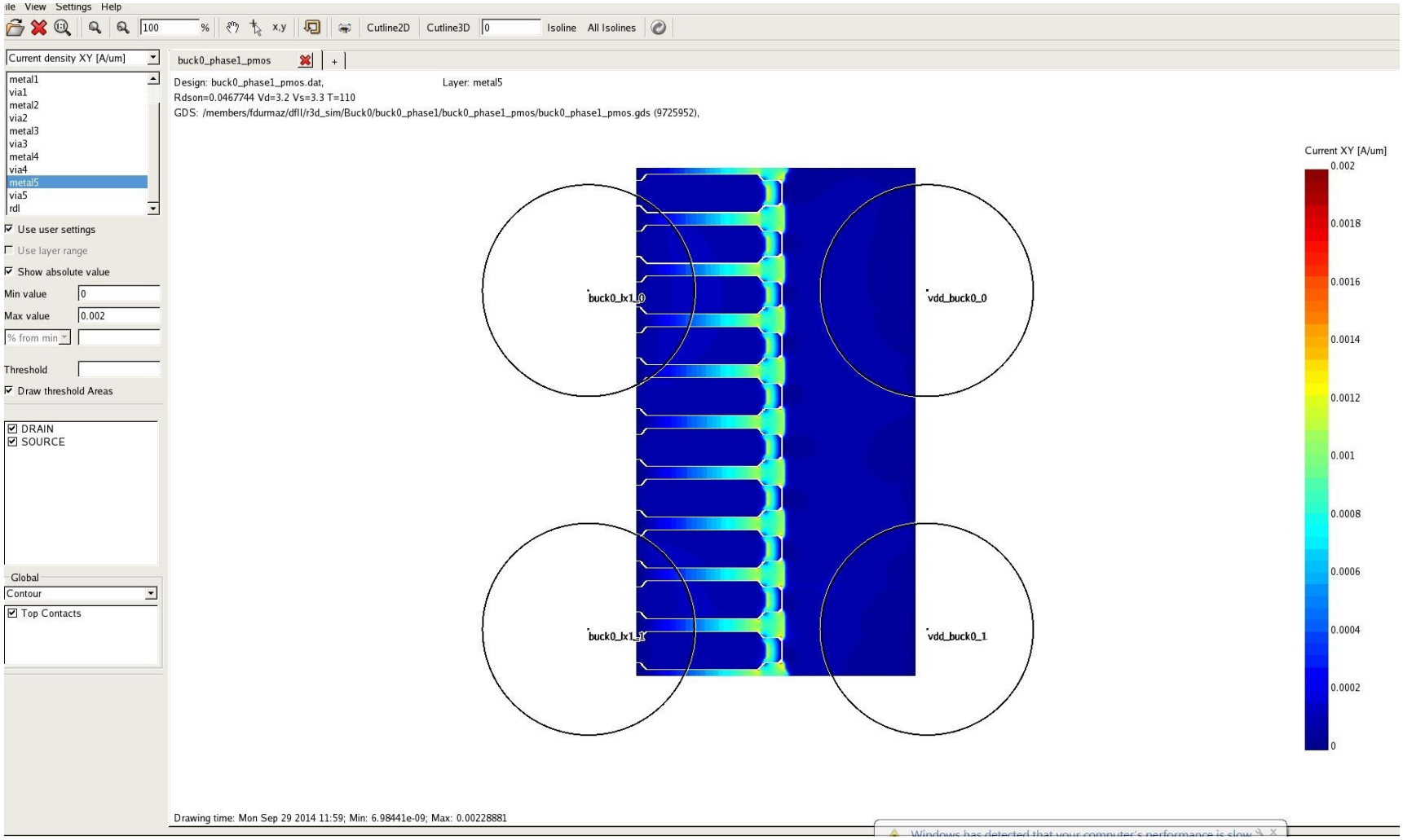


Figure 8.18 : R3D Current distribution of PMOS pass device in metal 5.

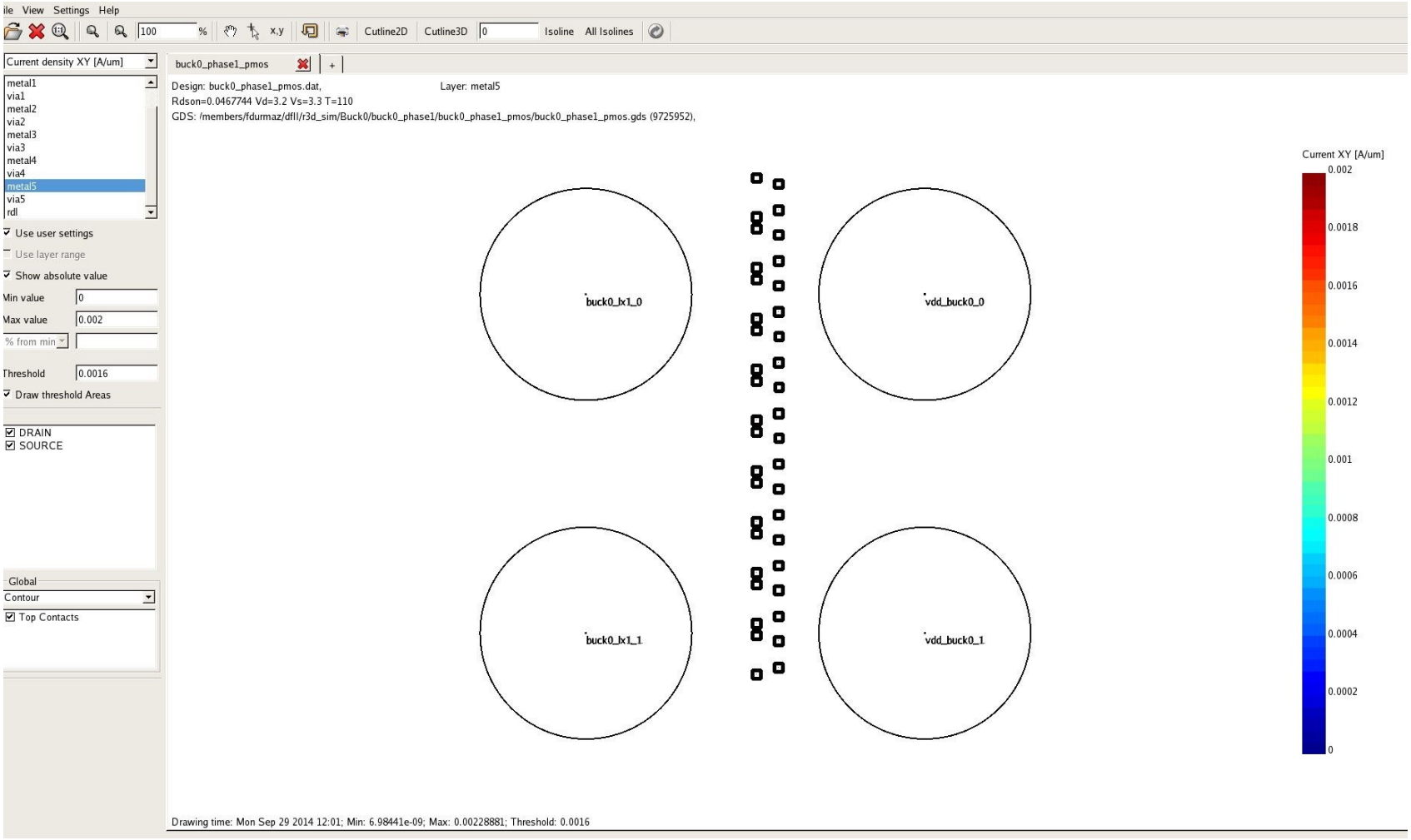


Figure 8.19 : Potential hotspots of PMOS part in metal 5.

Table of resistive components contributions to Rdson (in Ohms)

Component	Type	Res_[Ohm]	Source_[Ohm]	Drain_[Ohm]
Diffusion	MET	7.90494e-05	5.78582e-05	2.11912e-05
metal1	MET	0.000194448	0.000106988	8.74598e-05
metal2	MET	0.000796647	0.000146034	0.000650613
metal3	MET	0.000821863	0.000155977	0.000665886
metal4	MET	0.000897383	0.000178607	0.000718776
metal5	MET	0.000920041	0.000736214	0.000183827
rdl	MET	0.00336642	0.0025176	0.000848822
odCont	VIA	0.00039585	0.000265958	0.000129892
via1	VIA	0.000284476	0.000110566	0.000173911
via2	VIA	0.000115074	5.44186e-05	6.0655e-05
via3	VIA	0.000152209	6.20882e-05	9.01207e-05
via4	VIA	0.000274994	9.75964e-05	0.000177398
via5	VIA	3.90881e-05	1.59006e-05	2.31875e-05
vss_buck0	TC	0.000705176		
buck0_lx0_1	TC	0.000159336		
buck0_lx0_2	TC	0.00019411		
Interconnects	ALL	0.00939616	0.00521098	0.00418518
channel	DEV	0.020563		
Total Rdson		0.0299592		

Extracted channel/gate width [um]: 80000
Average channel resistivity [Ohm*um]: 1645.04

Figure 8.20 : R3D resistance result for NMOS part.

Table of resistive components contributions to Rdson (in Ohms)

Component	Type	Res_[Ohm]	Source_[Ohm]	Drain_[Ohm]
Diffusion	MET	1.44276e-06	7.21363e-07	7.21399e-07
metal1	MET	0.00015385	9.03054e-05	6.35445e-05
metal2	MET	0.000137275	6.52107e-05	7.20642e-05
metal3	MET	0.00135992	0.000417283	0.00094264
metal4	MET	0.00142171	0.000433691	0.000988022
metal5	MET	0.000788864	0.000634285	0.000154579
rdl	MET	0.000976841	0.000378119	0.000598723
odCont	VIA	0.000143652	7.18234e-05	7.18289e-05
via1	VIA	0.000398036	0.000189757	0.000208279
via2	VIA	0.000194436	9.83762e-05	9.60599e-05
via3	VIA	9.7461e-05	4.31962e-05	5.42648e-05
via4	VIA	0.000202954	6.7537e-05	0.000135417
via5	VIA	3.39805e-05	1.55572e-05	1.84234e-05
vdd_buck0_0	TC	0.000220087		
vdd_buck0_1	TC	0.000135853		
buck0_lx0_0	TC	0.000220108		
buck0_lx0_1	TC	0.000135835		
Interconnects	ALL	0.00662231	0.0028618	0.00376051
channel	DEV	0.0401503		
Total Rdson		0.0467726		

Extracted channel/gate width [um]: 150989
Average channel resistivity [Ohm*um]: 6062.25

Figure 8.21 : R3D resistance result of PMOS part.

As stated before, R3D gives metal resistance of every layer and also gives resistance of drain and source sides of MOS device. Figure 8.20 gives NMOS R3D results while Figure 8.21 gives PMOS results.

Total R_{dson} of NMOS is 29.9mΩ. This total resistance is divided to device channel resistance and interconnect metal resistance. R3D gives R_{device} as 20.5mΩ and 9.4mΩ resistance coming from metallization. This interconnect metallization resistance is divided to source and drain resistance. They are 5.2mΩ for source and 4.2mΩ for drain side.

Figure 8-20 shows resistance values of PMOS pass device. Total Rdson is 46.7mΩ. Rdevice is 40.1mΩ and interconnect resistance contribution is 6.6mΩ. This metallization resistance is divided as 2.8mΩ for source and 3.7mΩ for drain side.

With these outcomes, designer can adjust schematic of pass device by adding necessary parasitic resistances' both for drain and source sides of PMOS and NMOS parts. So that, schematic simulations will match layout and therefore more close to real world performance of the chip.

To better understand the benefit of R3D, different pass device top metal metallizations are shown in Figure 8.22 and Figure 8.23. In these figures, it is clear that there are more hotspots in top metal. Feedback from R3D resulted in a better metal layout optimization.

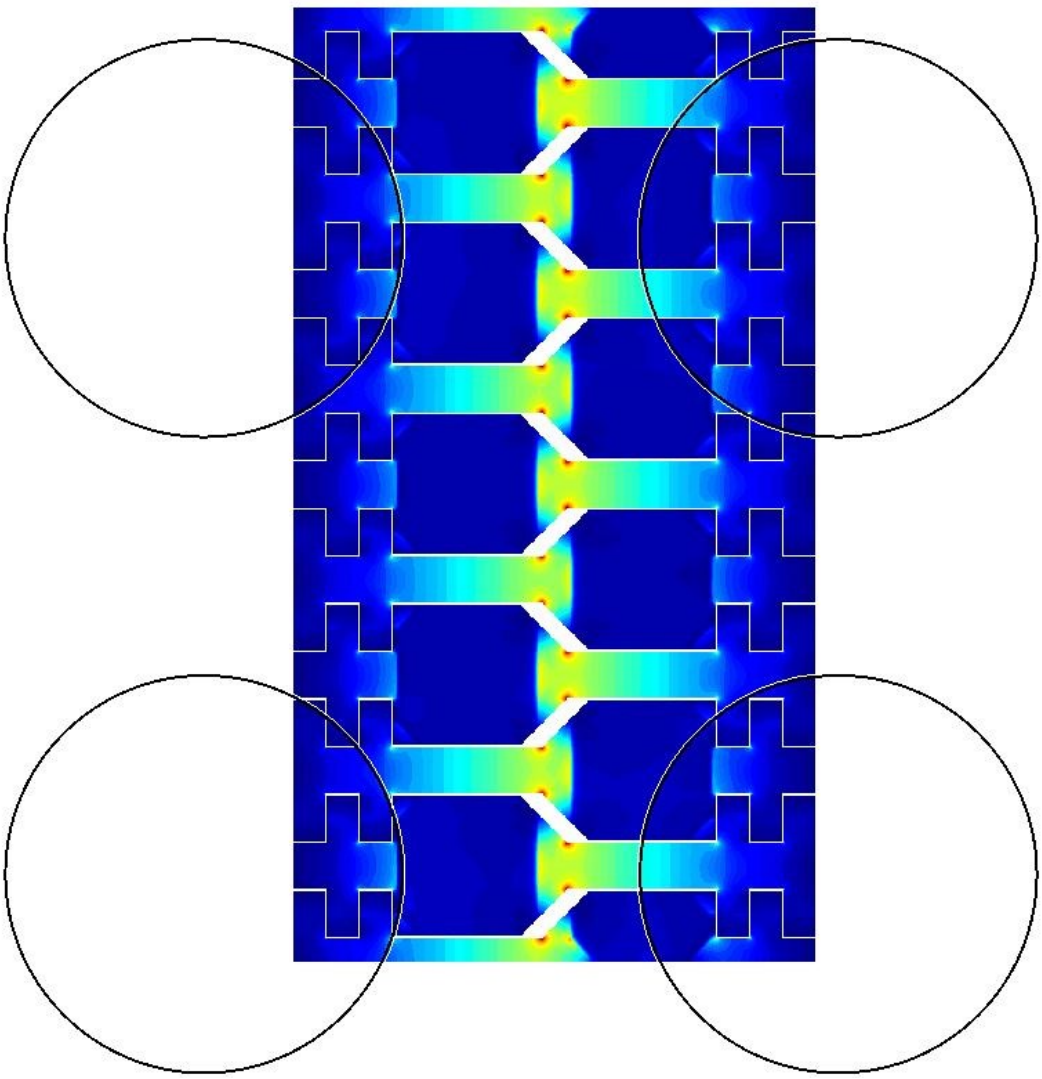


Figure 8.22 : R3D result of different metallization - 1

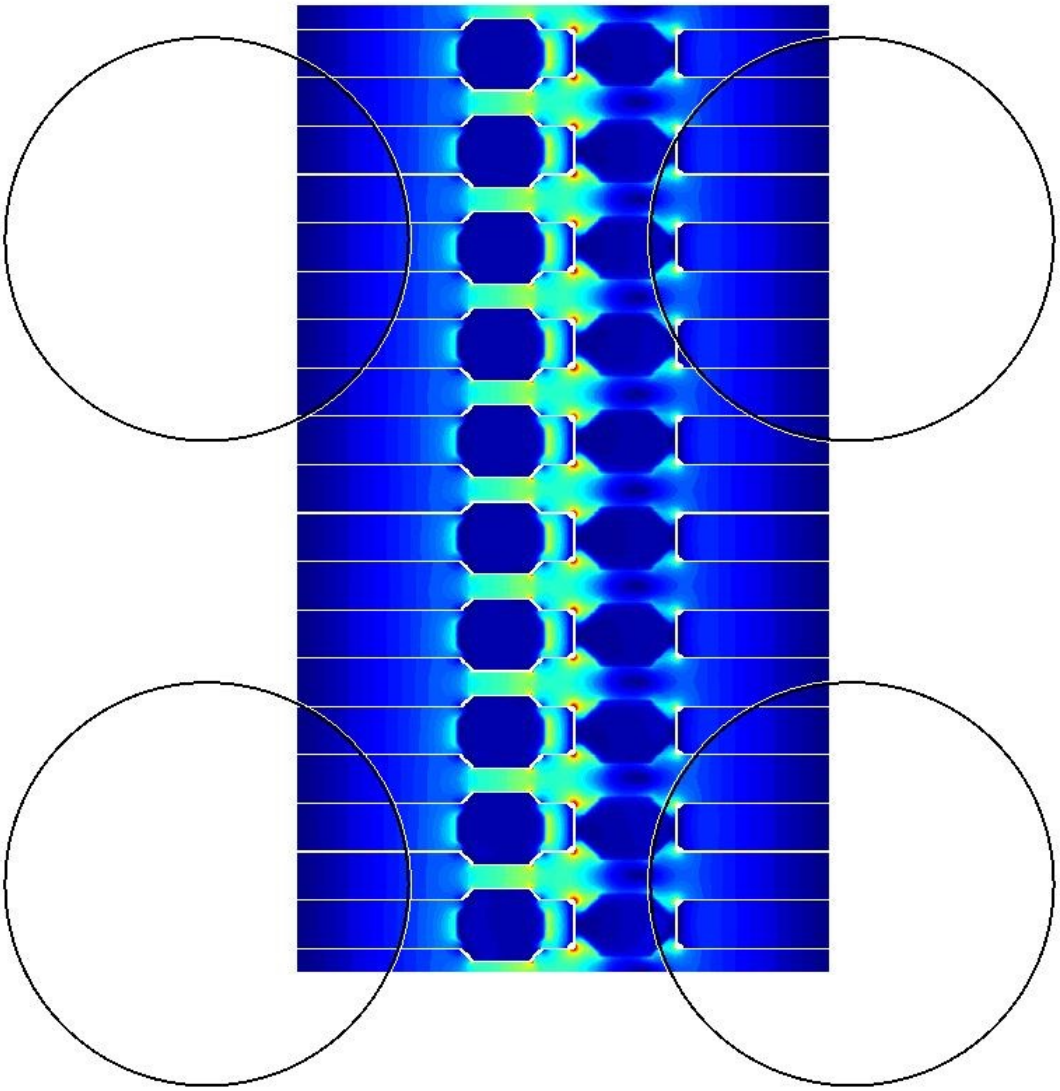


Figure 8.23 : R3D result of different metallization - 2

9. CONCLUSION AND FUTURE WORK

In this thesis, layout design of adaptive buck converter is implemented using 0.25µm BCD process with 1p5m (one poly, 5 metal layer) option. Basics of layout design are explained. Issues coming from layout effecting performance of chip are explained. Solutions regarding these issues are given in detail. Suggested layout structures are explained to minimize negative effects. Furthermore, advanced layout structures and methodology are demosntrated.

The layout design of sub blocks controlling NMOS and PMOS pass device parts are demosntrated in detail. Followed layout strategies and layout structures applied to blocks are given in detail. After these, layout of pass device of buck converter is shown. Total area that pass device occupies is 800µ x 700µ. Resulting buck converter area is 800µ x 870µ.

Furthermore to laying out buck converter, R3D simulations are done to analyze metallization over pass device. This R3D simulation gives potential hotspots on buck converter. So that, metal optimization can be done to reduce metallization resistance of PMOS and NMOS pass device parts. Outcomes of R3D for NMOS are $R_{metallization}$ = 9.4mΩ, R_{device} = 20.5mΩ and total Rdson = 29.9mΩ. Outcomes for PMOS are $R_{metallization}$ = 6.6mΩ, R_{device} = 40.1mΩ and total Rdson = 46.7mΩ. By help of these outcomes, schematic design can be simulated better with feedback from R3D.

Future improvements for layout design of buck converter can be using more metal layer by choosing process that supports more metals. Pass device are realized by standart MOSFETs, asymmetric MOSFETs can be used to reduce pass device area. In addition to asymmetric device, power MOSFET's that support high current capability by less device resistance can also be instantiated inside pass device. To determine the metallization of pass device other tool programs can be used to analyse. Furthermore, different process types like silicon-on-insulator (SOI) can be used to get better noise isolation of buck converters. Different analog design techniques can also applied to get same performance with less area consumption.

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APPENDICES

APPENDIX A: Metal routings of sub blocks of buck converter.

APPENDIX B: Silicon-on-insulator (SOI)

APPENDIX C: Enlosed layout transistor (ELT)

APPENDIX A

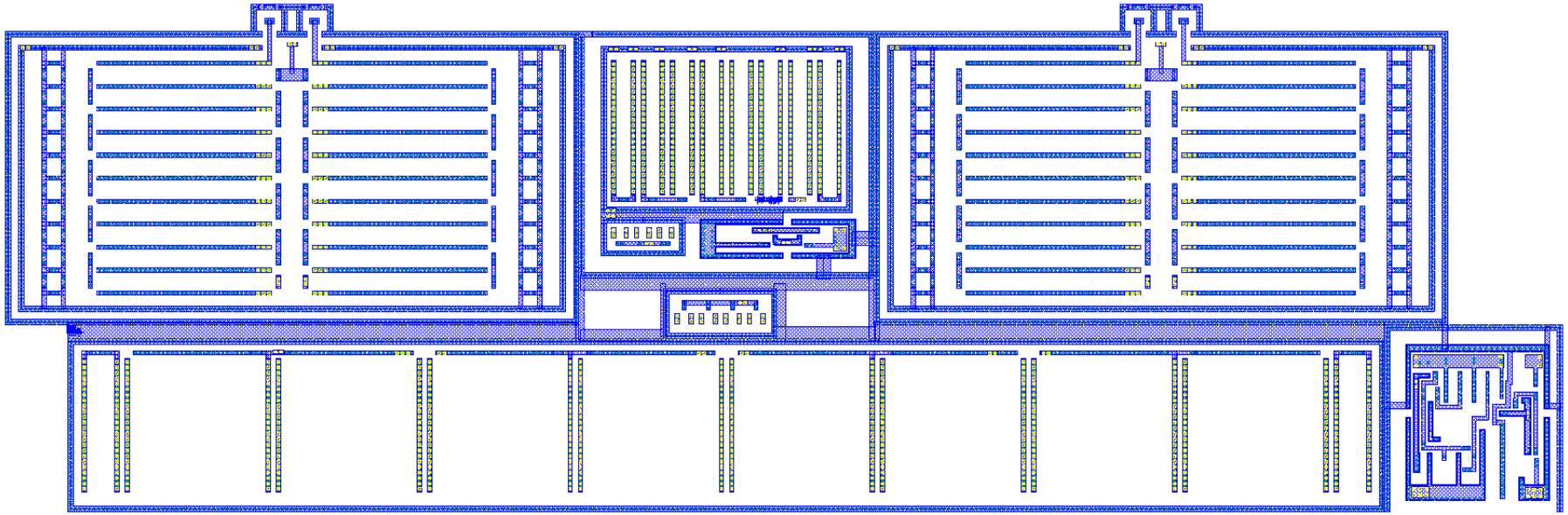

Figure A.1 : Adaptive Capacitive Gm block, metal 1 routings.

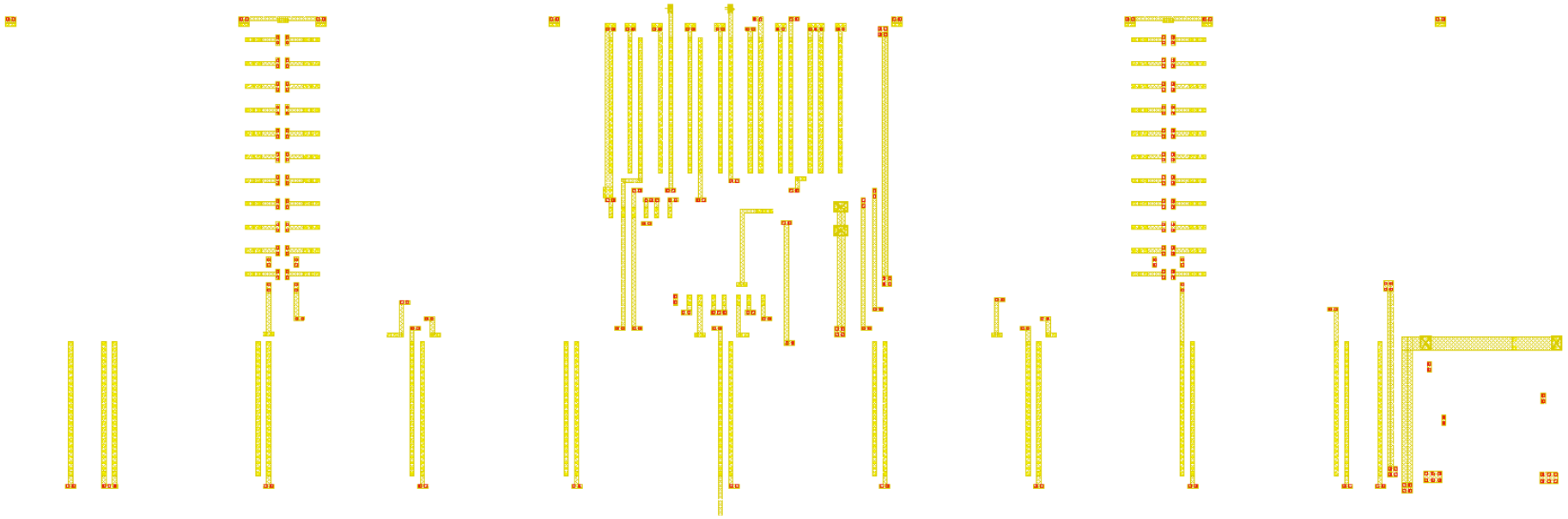

Figure A.2 : Adaptive Capacitive Gm block, metal 2 vertical routings.

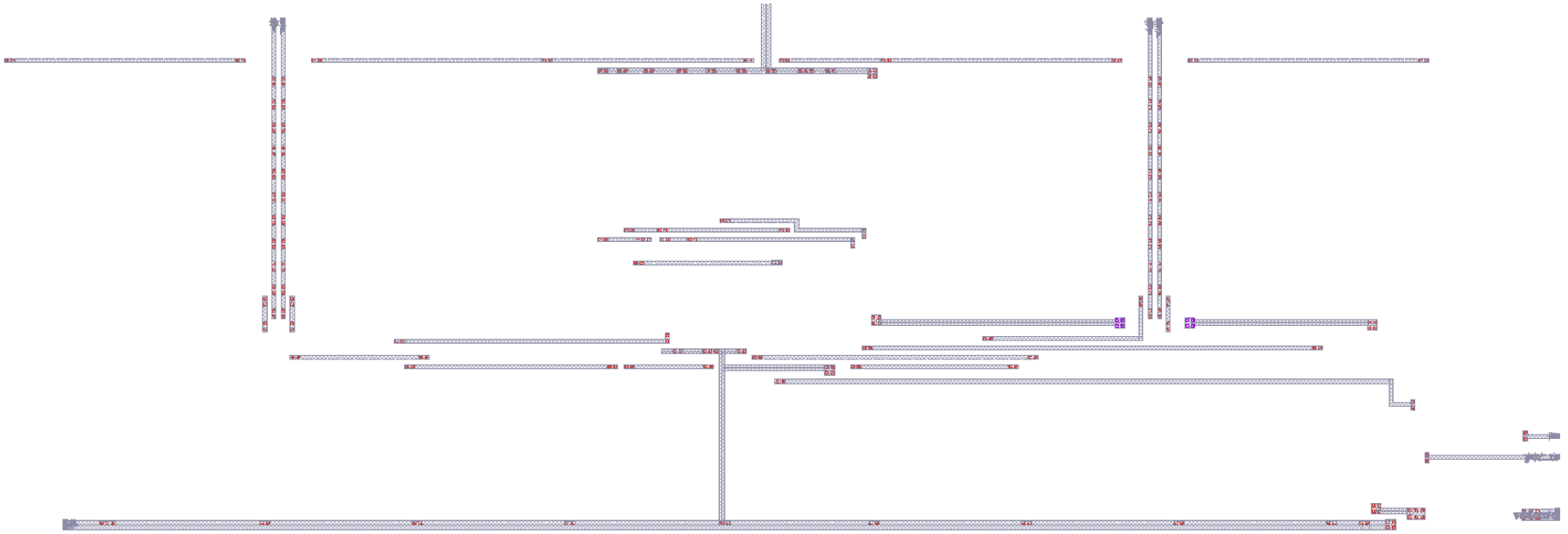

Figure A.3 : Adaptive Capacitive Gm block, metal 3 horizontal routing.

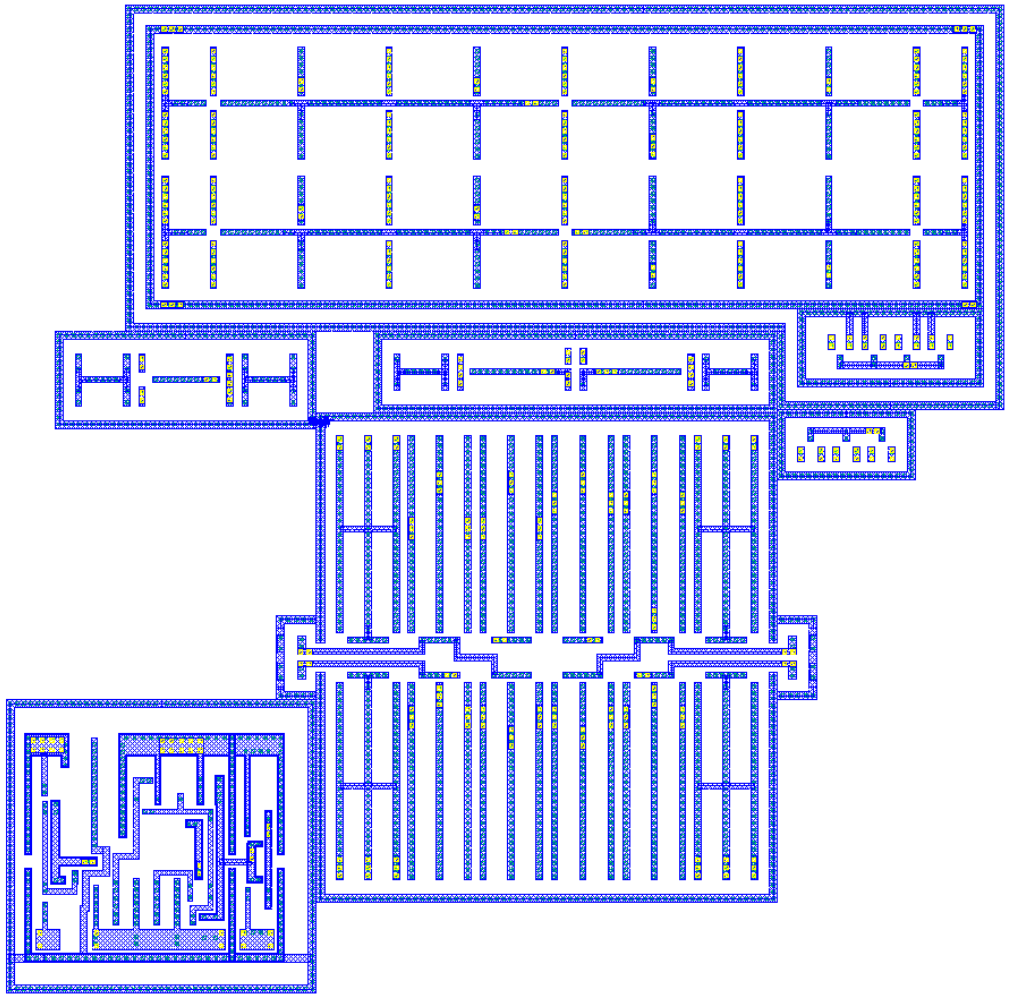

Figure A.4 : Adaptive Resistive Gm block, metal 1 routings.

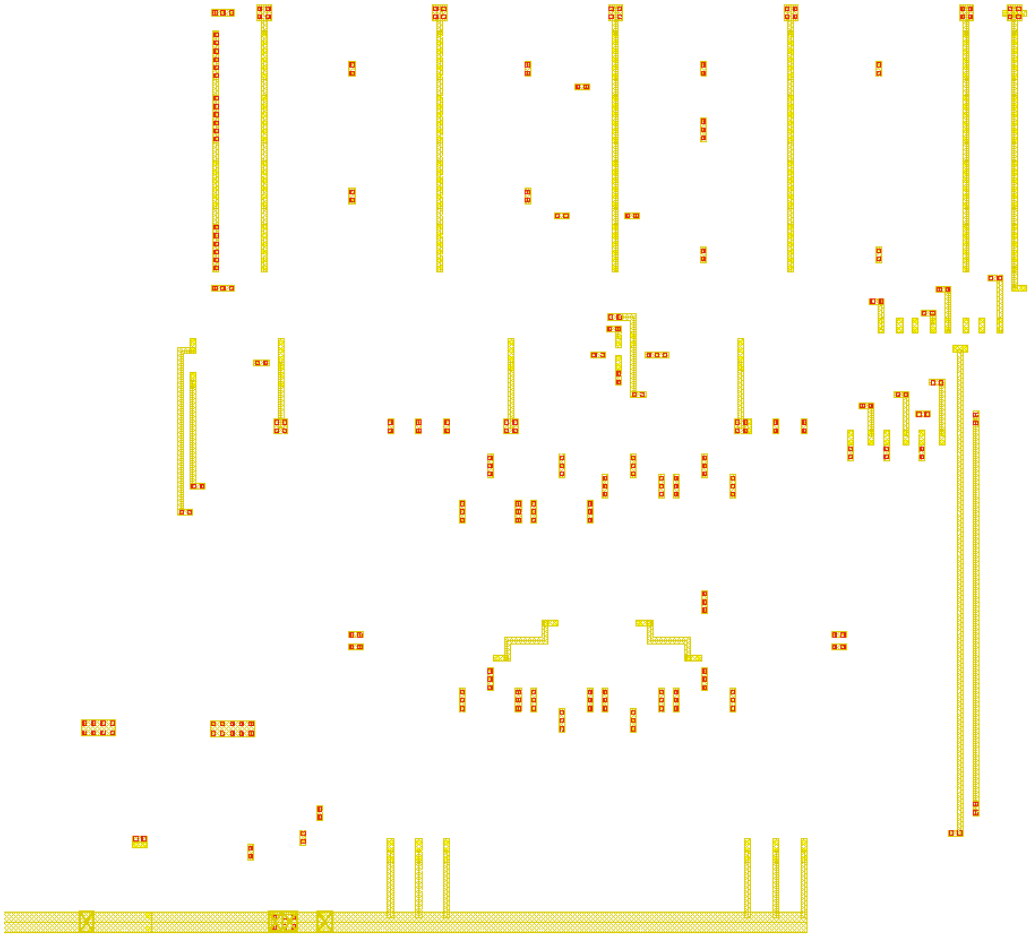

Figure A.5 : Adaptive Resistive Gm block, metal 2 vertical routings.

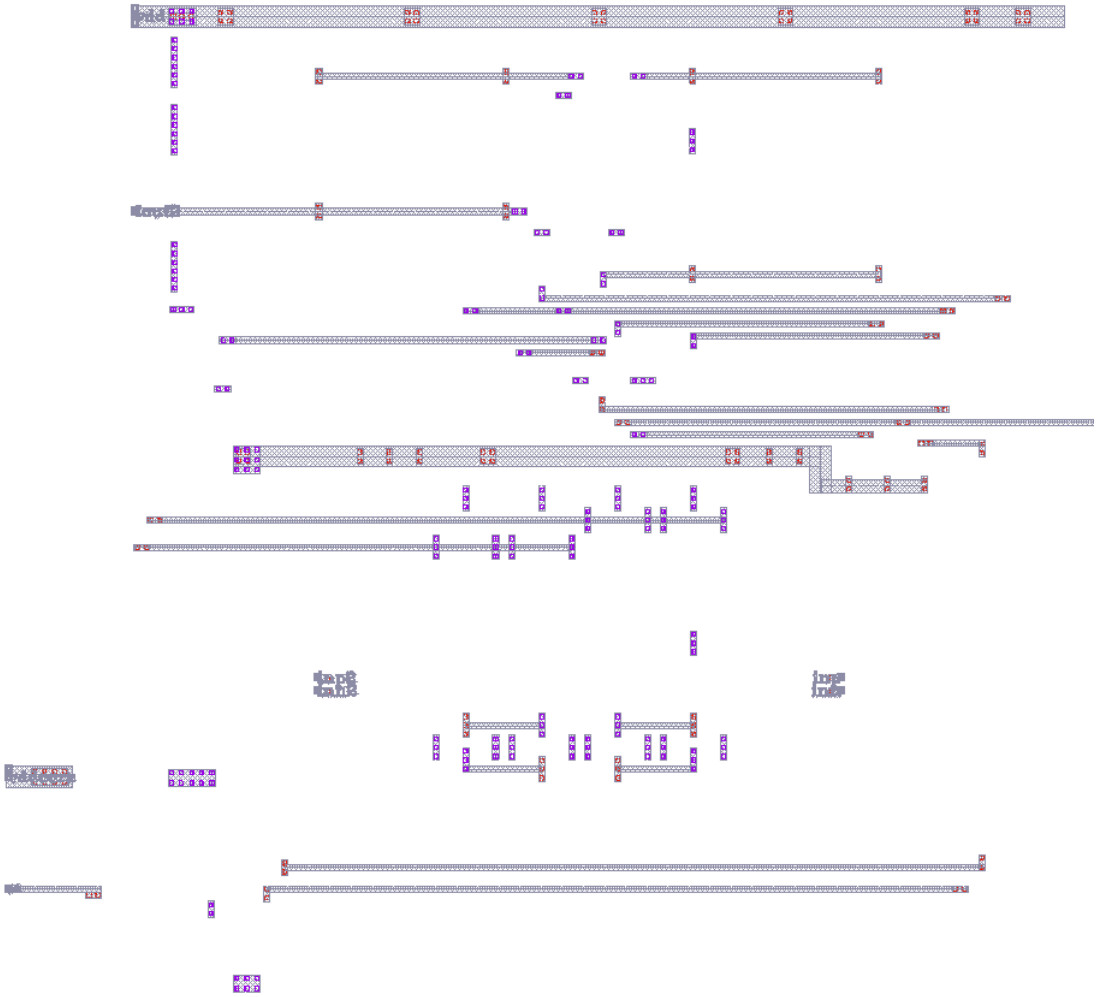

Figure A.6 : Adaptive Resistive Gm block, metal 3 horizontal routings.

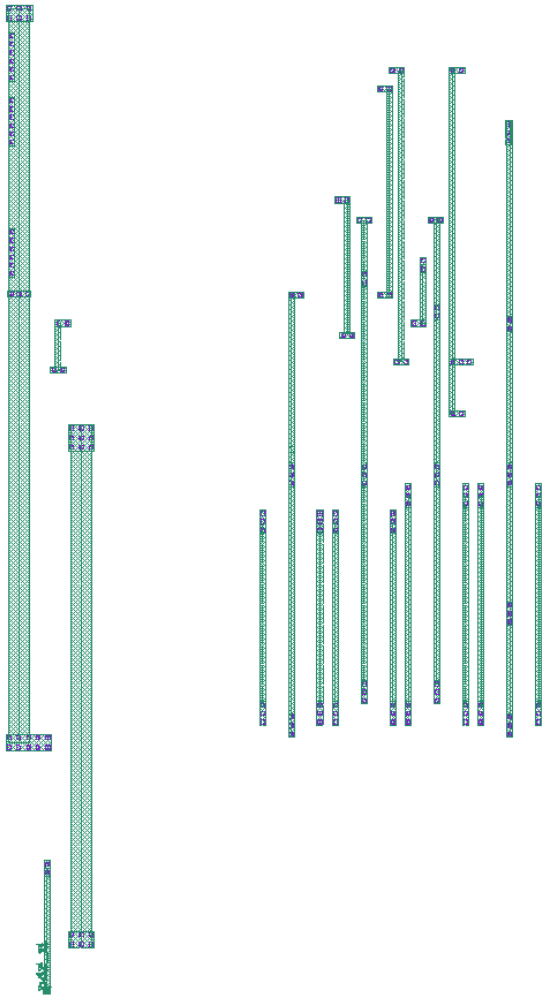

Figure A.7 : Adaptive Resistive Gm block, metal 4 vertical routings.

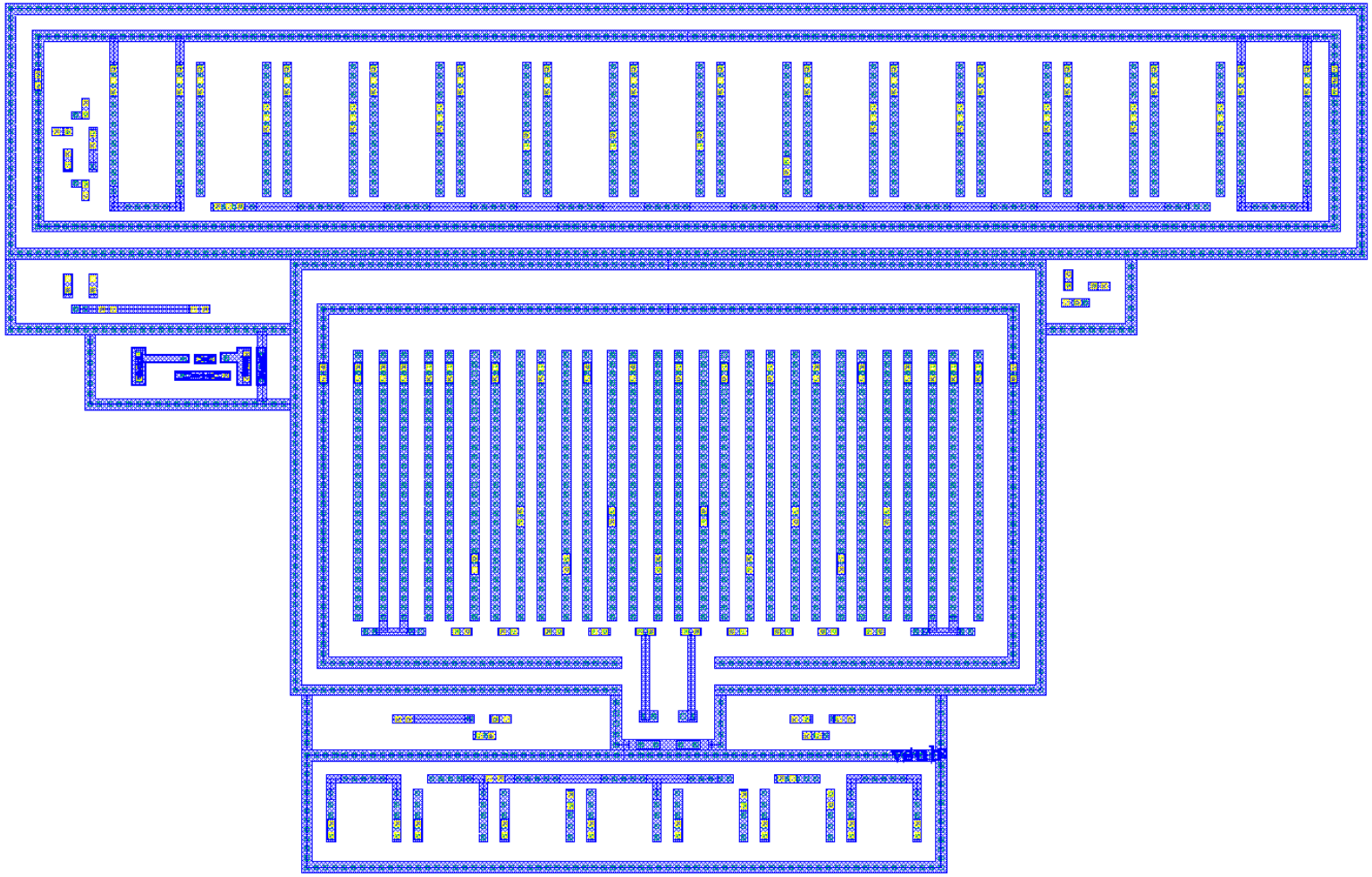

Figure A.8 : Error amplifier, metal 1 routings.

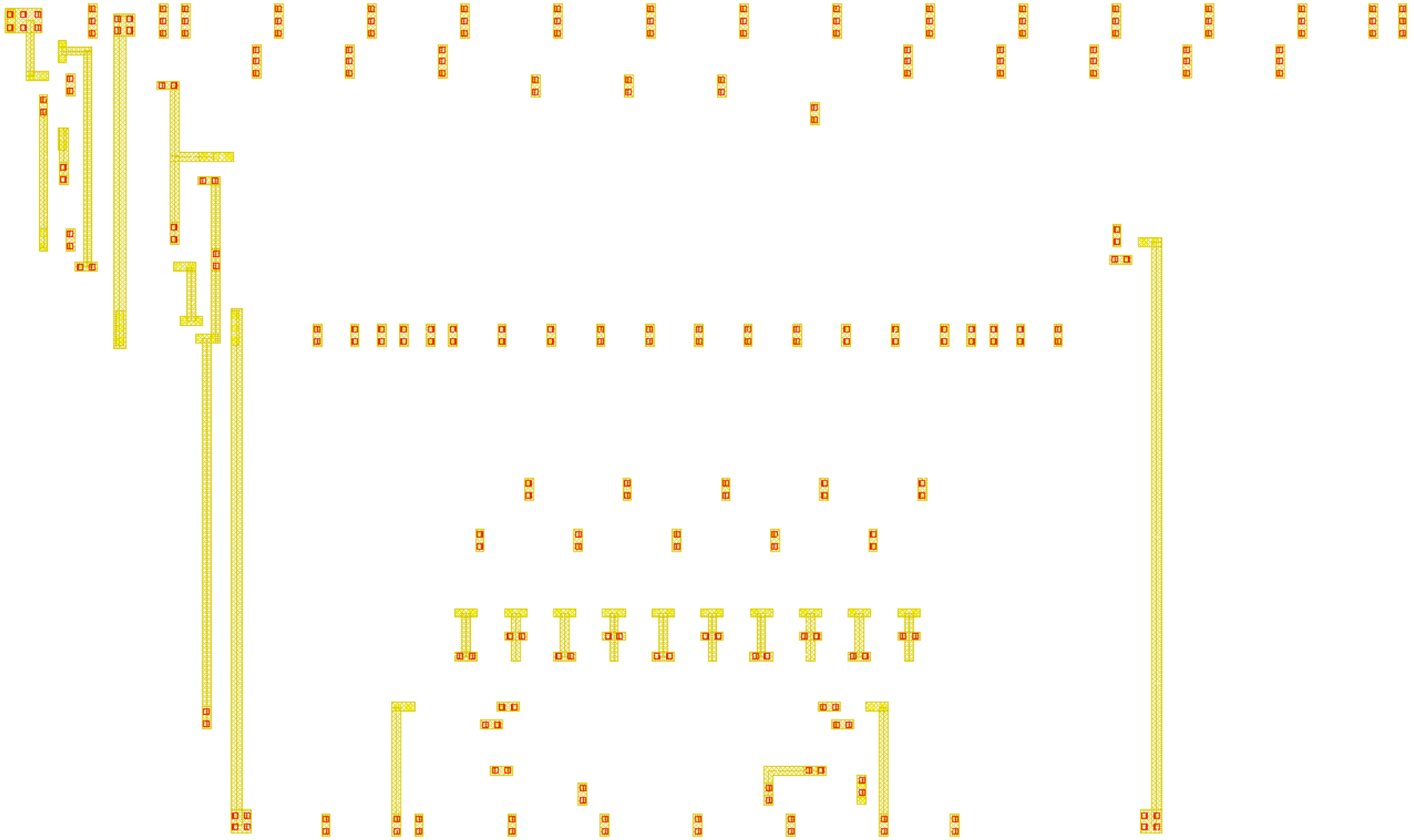

Figure A.9 : Error amplifier, metal 2 vertical routings.

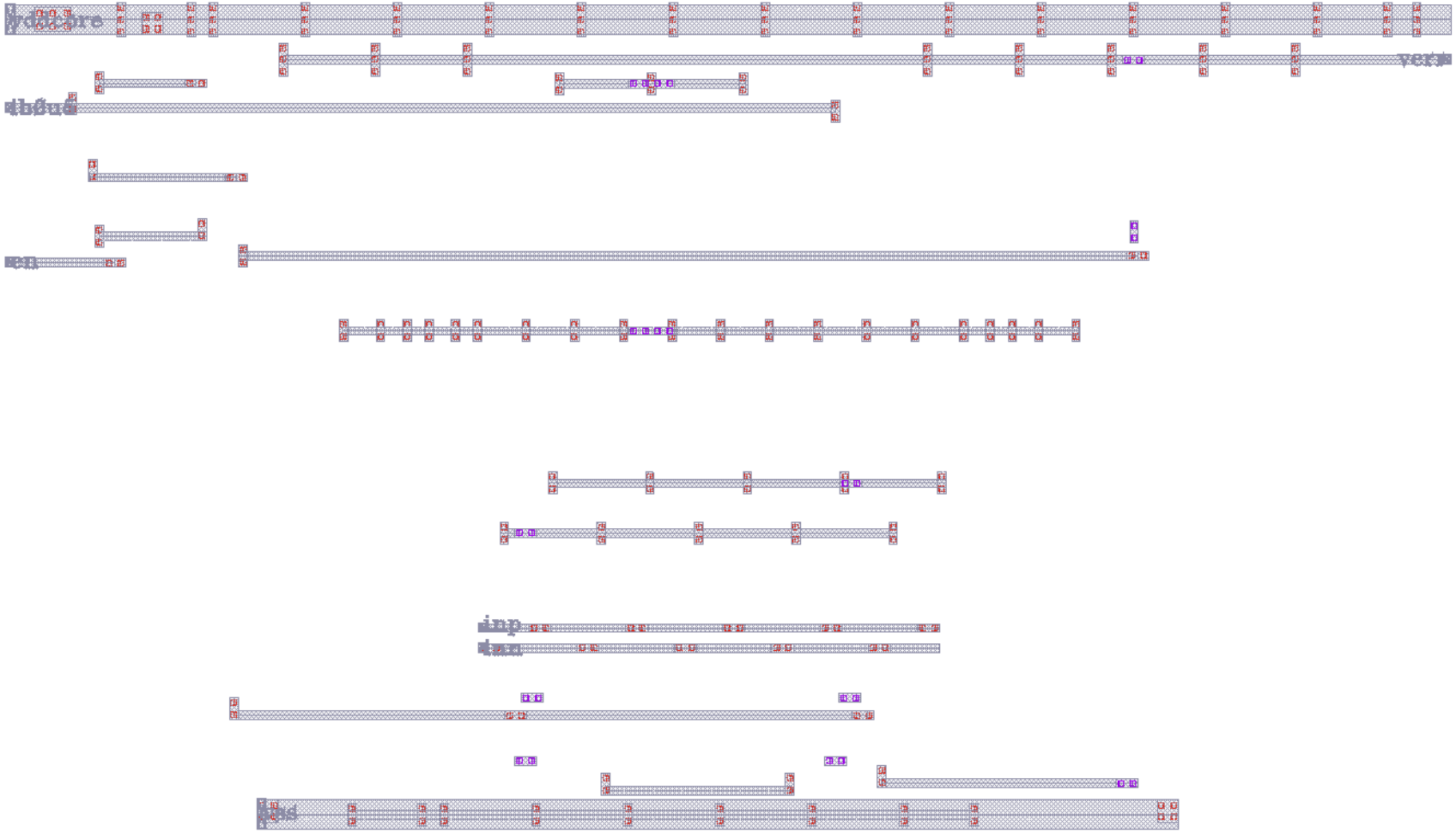

Figure A.10 : Error amplifier, metal 3 horizontal routings.

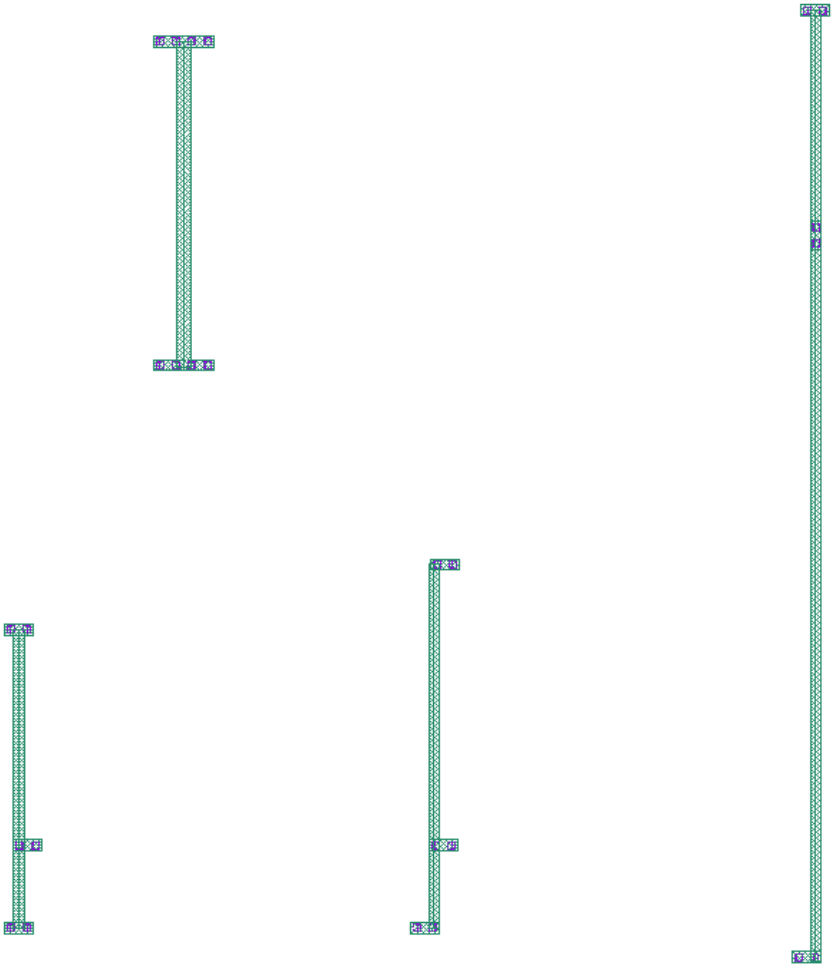

Figure A.11 : Error amplifier, metal 4 vertical routings.

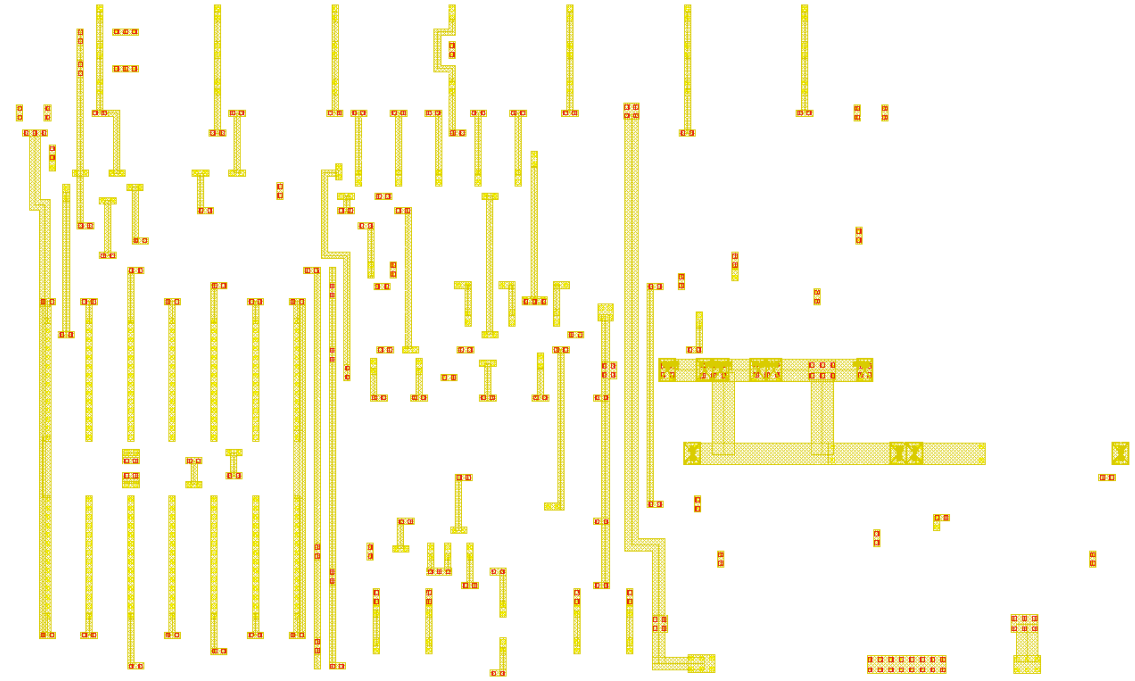

Figure A.12 : PWM comparator, metal 2 vertical routings.

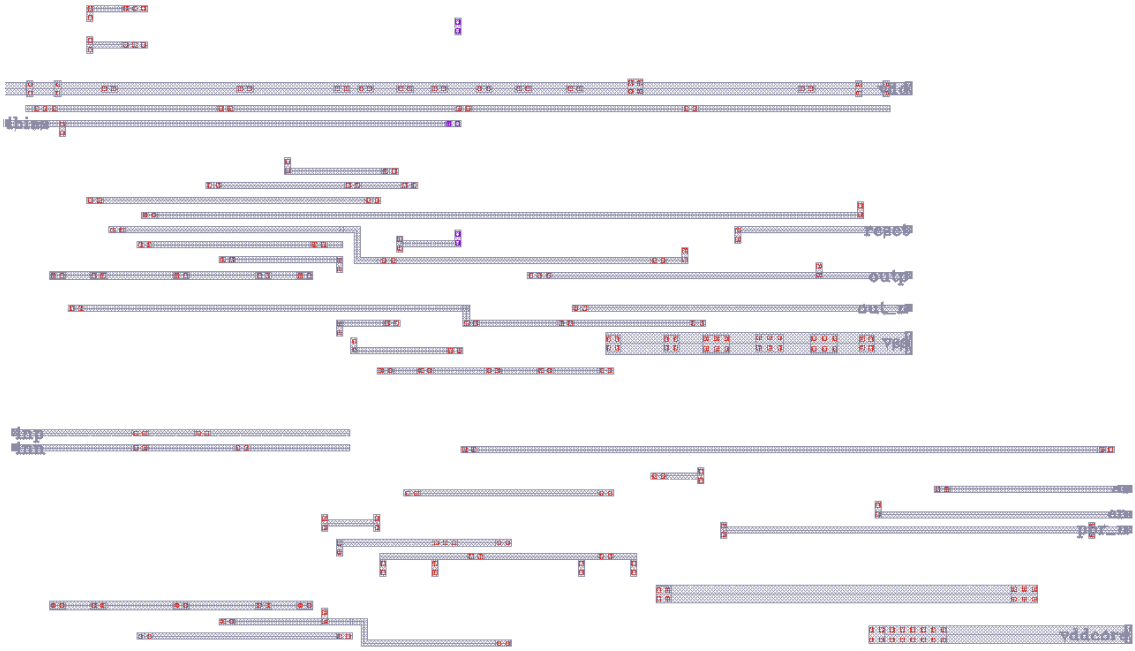

Figure A.13 : PWM comparator, metal 3 horizontal routings.

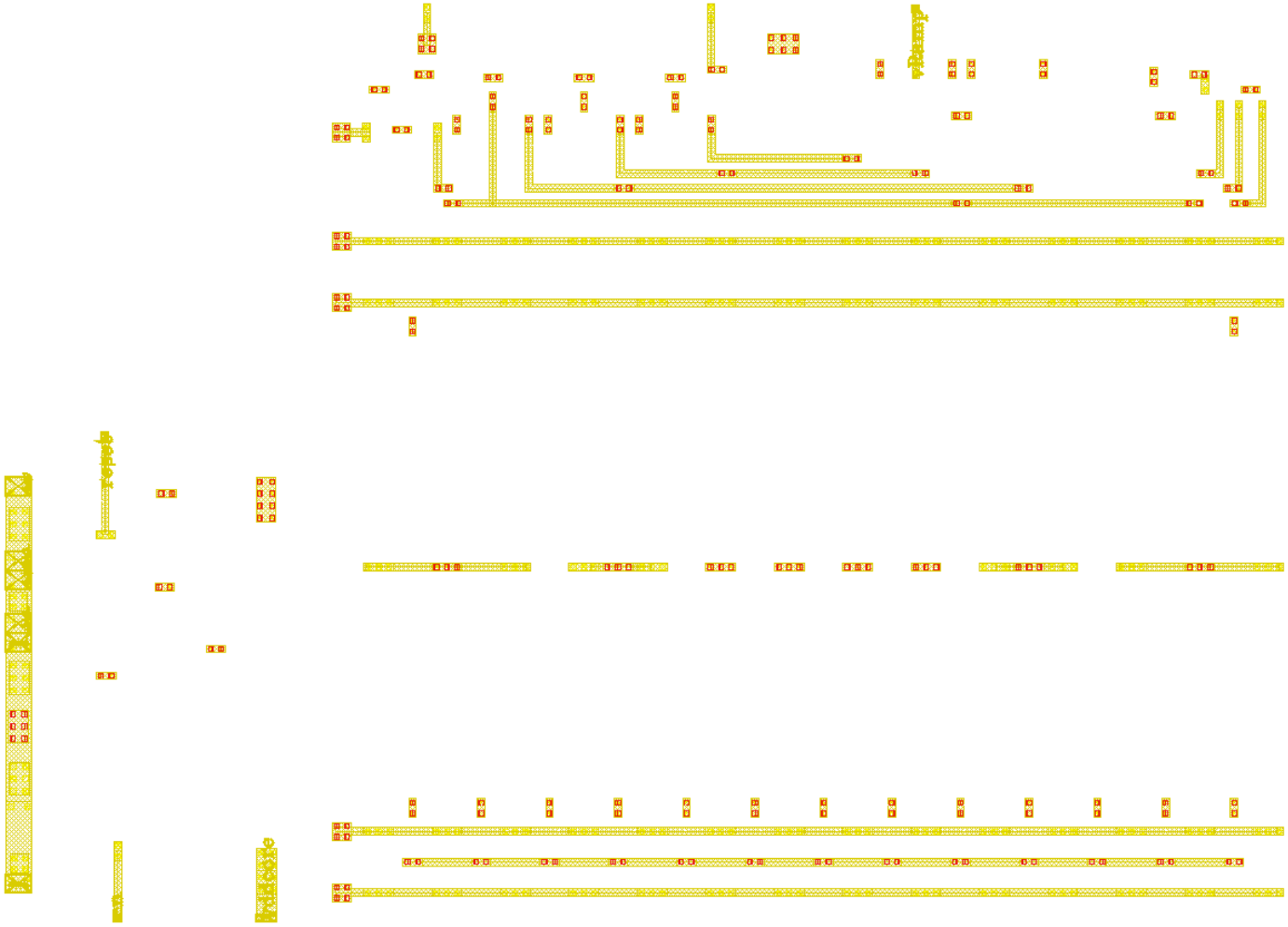

Figure A.14 : Ramp generator, metal 2 horizontal routings.

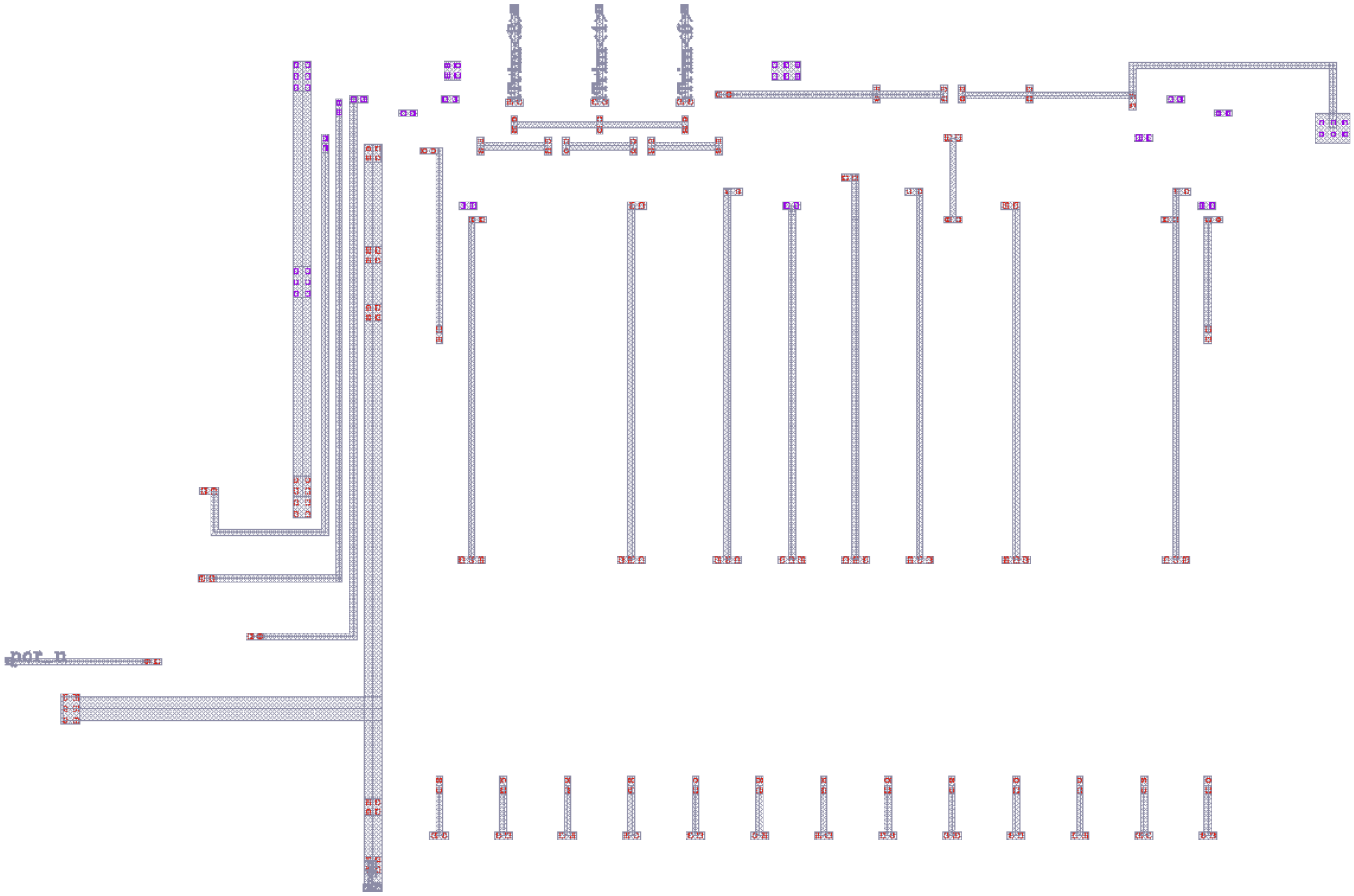

Figure A.15 : Ramp generator, metal 3 vertical routings.

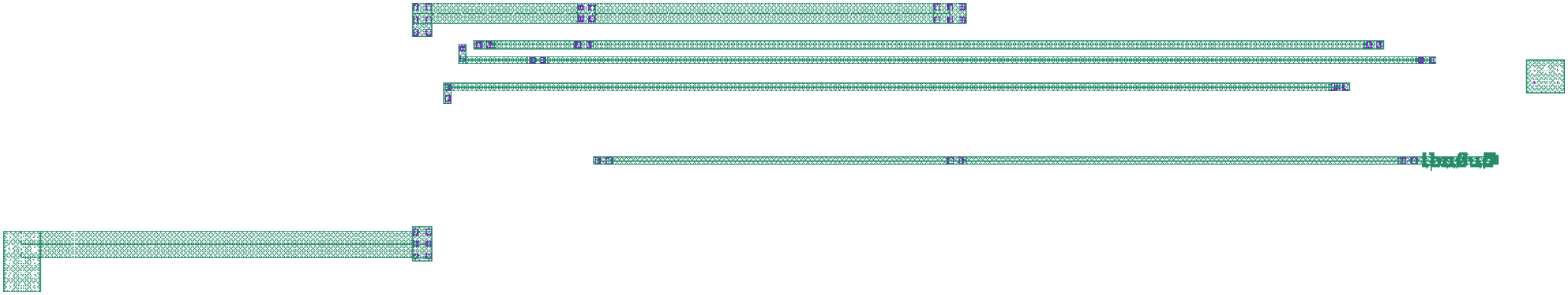

Figure A.16 : Ramp generator, metal 4 horizontal routings.

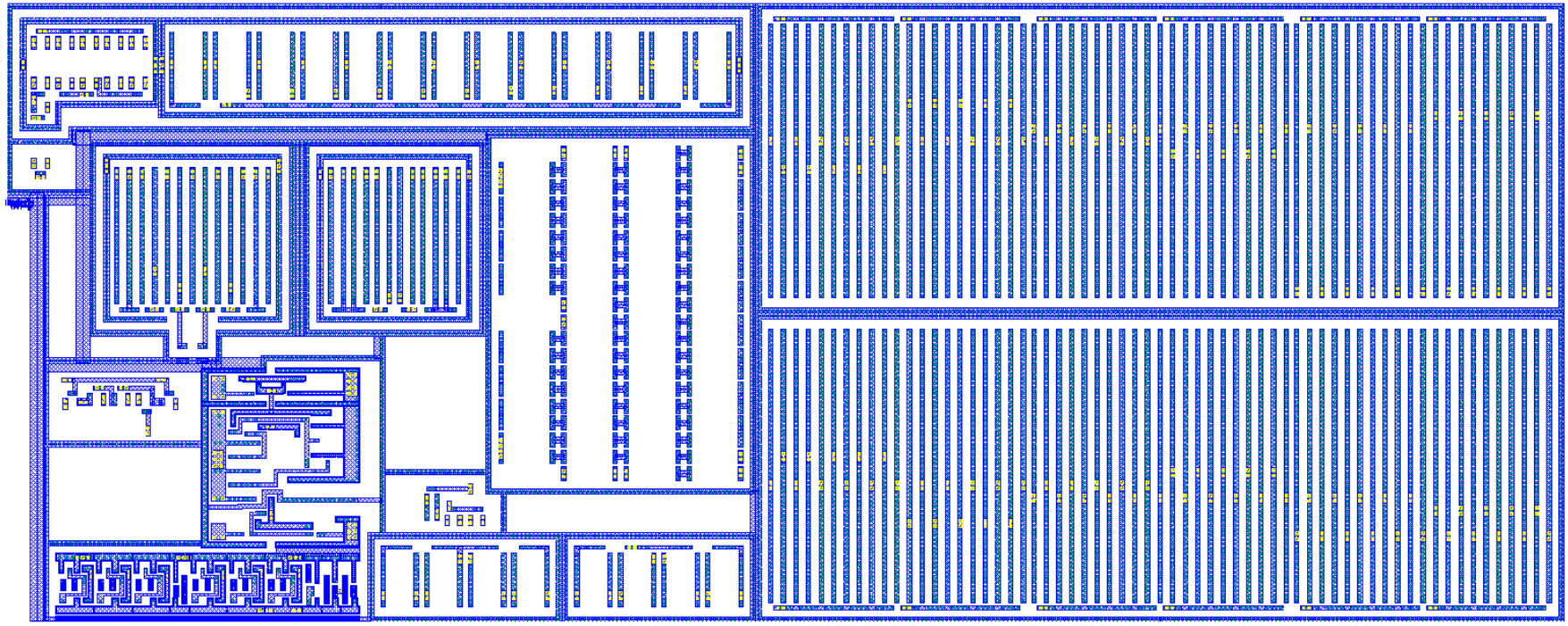

Figure A.17 : Active diode comparator, metal 1 routings.

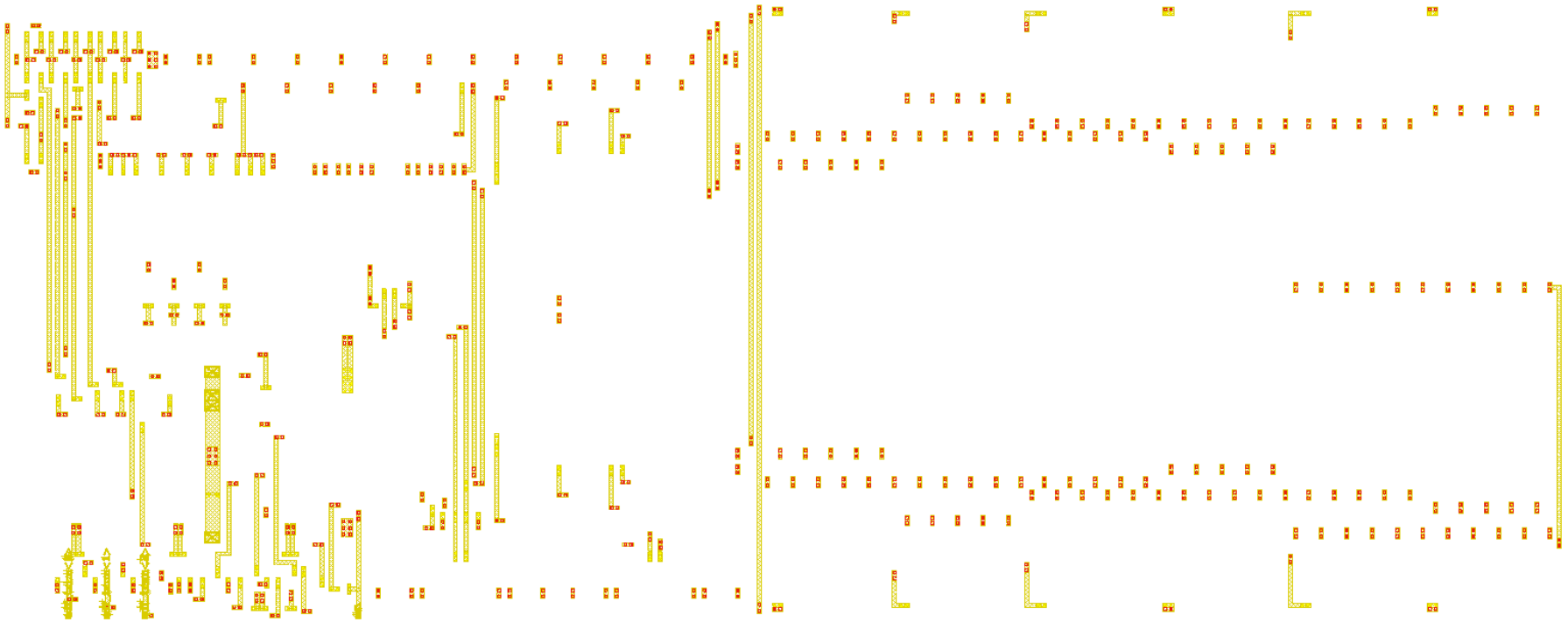

Figure A.18 : Active diode comparator, metal 2 vertical routings.

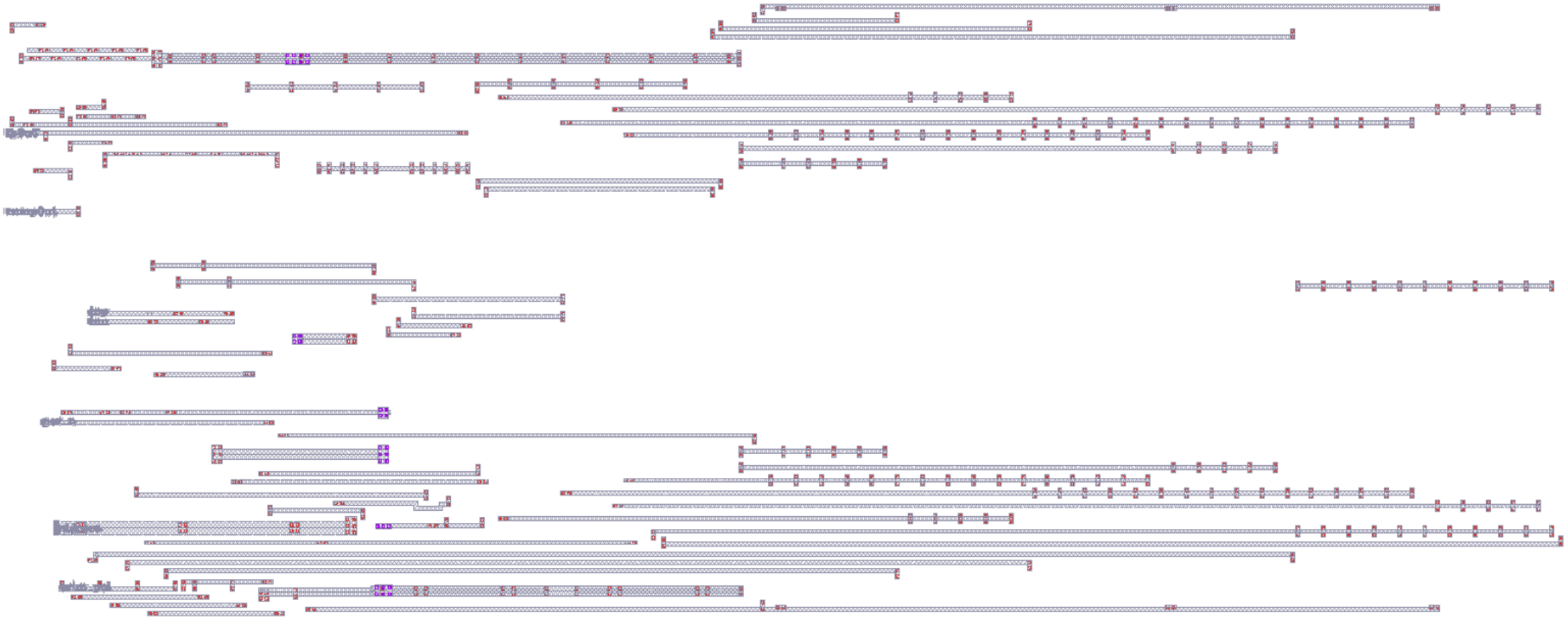

Figure A.19 : Active diode comparator, metal 3 vertical routings.

APPENDIX B

Silicon on Insulator

Silicon on insulator (SOI) technology refers to the use of a layered silicon–insulator–silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, to reduce parasitic device capacitance, thereby improving performance [73]. SOI-based devices differ from conventional silicon-built devices in that the silicon junction is above an electrical insulator, typically silicon dioxide or sapphire (these types of devices are called silicon on sapphire, or SOS). The choice of insulator depends largely on intended application, with sapphire being used for high-performance radio frequency (RF) and radiation-sensitive applications, and silicon dioxide for diminished short channel effects in microelectronics devices [74]. The insulating layer and topmost silicon layer also vary widely with application [75].

Benefits of SOI technology relative to conventional silicon (bulk CMOS) processing are :

- Lower parasitic capacitance due to isolation from the bulk silicon, which improves power consumption at matched performance.
- Resistance to latchup due to complete isolation of the n- and p-well structures.
- Reduced antenna issues
- Lower leakage currents due to isolation thus higher power efficiency.
- Inherently radiation hardened

APPENDIX C

Enclosed Layout Transistor (ELT)

Low-power microelectronic circuits including computers, communication devices and monitoring systems in space shuttle and satellites are very different from what we use on earth. They are radiation (high-speed atomic particles like proton and neutron, solar flare magnetic energy dissipation in Earth's space, energetic cosmic rays like X-ray, gamma ray etc.) tolerant circuits. These special electronics are designed by applying very different techniques using radiation-hardened-by-design (RHBD) MOSFETs to ensure the safe space journey and proper working of devices/ vehicles.

Radiation strikes near the silicon oxide region cause the channel inversion at the corners of the standard MOSFET due to accumulation of radiation induced trapped charges. If the charges are large enough, the accumulated charges affect STI surface edges along the channel near the channel interface (gate) of the standard MOSFET. Thus the device channel inversion occurs along the channel edges and the device creates off-state leakage path, causing device to turn on (Figure C.1). So the reliability of circuits degrades severely.

One of the design approaches for making a RHBD device is Enclosed-Layout-Transistor (ELT). Advantage of ELT is improved reliability by reducing unwanted surface inversion at the gate edges that occurs in the standard MOSFET. That is done by placing gate in between drain and source. In the center, there is drain or source, then gate surrounds it, outer is surrounded by source or drain (Figure C.2). By using this structure there is no STI stress on top or bottom of MOSFET when compared to conventional device.

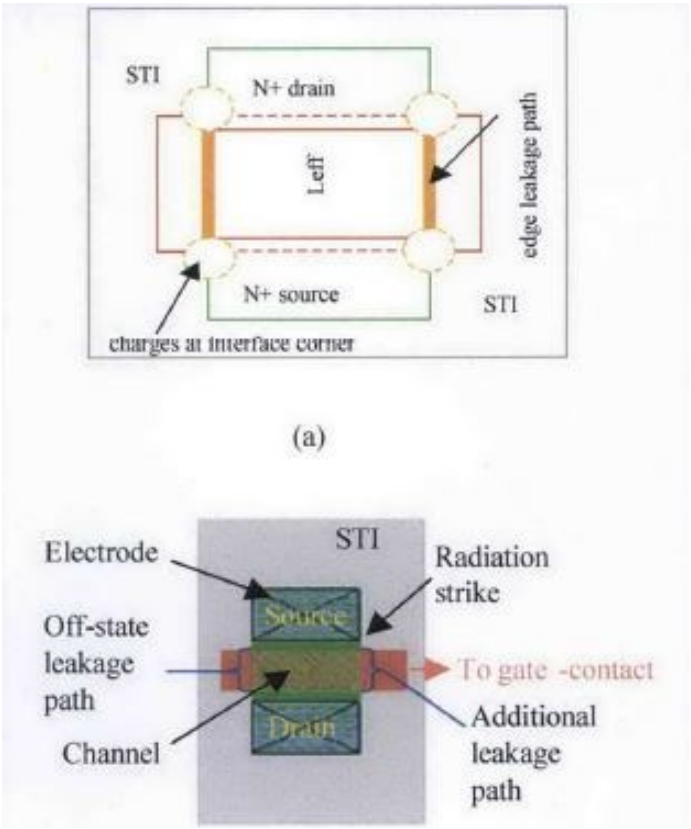

Figure C.1 : (a) Radiation effects mechanism and (b) illustration of off-state leakage path in the 2-edge standart MOSFET [77].

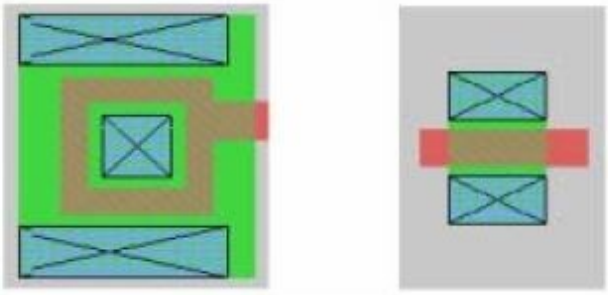

Figure C.2 : An ELT (left) and a simple MOSFET (right) [78].

Advantage of ELT can be summarized below;

- High radiation tolerance, suitable for high-energy physics domains like the Large Hadron Collider (LHR), space and satellite applications.
- Little to no leakage current with respect to radiation induced charge density.
- The additional advantage of improving the hot-carrier reliability of CMOS circuits by reducing the drain/source electric field compared to conventionally designed transistors [82]

Disadvantages that prevents ELT to be used widespread in commercial applications;

- W/L restriction due to fabrication limitations leading large area consumptions.
- Due to large area consumtion, expensive production.
- L of ELT is not constant because gate makes turns at the corners where the gate length (L) changes slightly due to the existence of the "corner device" [79-80].
- Difficulty in modelling ELT. Extraction of effective W/L is hard with existing methods. The foundry-provided tool for extracting the effective W/L is targeted toward the two-edged transistor and needs significant adaptation when applying to the enclosed-gate transistors [79].
- The output conductance in the saturation region is different if the inner or outer diffusion region is chosen as the drain. clear asymmetry in the channel length modulation, which is lower when the drain is outside the gate [81].
- Gate and drain or source capacitances are larger than in the standard transistors [83].

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