İSTANBUL TECHNICAL UNIVERSITY « INSTITUTE OF SCIENCE AND TECHNOLOGY

AN ALL CMOS WIDEBAND VARIABLE GAIN AMPLIFIER WITH LINEAR-IN-dB CONTROL

M.Sc. Thesis by

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Program : Electronics Engineering

JUNE 2008

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DOĞRUSAL-dB KONTROLLÜ GENİŞ BANTLI CMOS DEĞİŞKEN KAZANÇLI KUVVETLENDİRİCİ

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TABLE OF CONTENTS

LIST OF TABLES

Page No.

LIST OF FIGURES

Page No.

AN ALL CMOS WIDEBAND VARIABLE GAIN AMPLIFIER WITH LINEAR-IN-dB CONTROL

SUMMARY

In this study, the theory and the topologies of CMOS VGA (Variable Gain Amplifier) are examined and the design of the proposed VGA is completed. Linear in dB gain characteristic, wide tuning range, wide and constant bandwidth, IIP_3, IP_{1dB} and NF are the most important specifications of the VGA. The bandwidths of CMOS VGA topologies in the literature change with control voltage because variable gain is obtained by changing the output impedance of the amplifier. Thus, first of all, a VGA core is designed to obtain constant bandwidth with respect to the control voltage using the folded Gilbert cell. In this structure, gain is controlled by the transconductances of the input transistors. On the other hand, the output impedance does not change so the bandwidth of the VGA is constant. The MOS-L structure as a bandwidth extension load is used to increase bandwidth of the circuit. In CMOS technology, devices do not have an exponential characteristic. Therefore, pseudo exponential or Taylor series approximation functions are used to obtain the exponential characteristic. Taylor series approximation method is used to obtain linear-in-dB gain characteristic. An exponential current generator circuit is designed using Taylor series approximation method of exponential function. VGA core of the proposed VGA is folded Gilbert cell, so maximum gain of this core is not high. Therefore, to increase the gain level of the proposed VGA, three post amplifier circuits are used. Spectre circuit simulator was used as the simulator. Circuit was verified by using UMC 0.13µm CMOS process. The designed VGA has 21 dB-in-linear gain range and 3 GHz constant 3-dB bandwidth.

DOĞRUSAL-dB KONTROLLÜ GENİŞ BANTLI CMOS DEGİŞKEN KAZANÇLI KUVVETLENDİRİCİ

ÖZET

Bu çalışmada, CMOS VGA (Değişken Kazançlı Kuvvetlendirici) devrelerinin teorileri ve yapıları incelenmiştir ve önerilen VGA devresinin tasarımı ve analizleri tamamlanmıştır. VGA'nın en önemli tasarım parametreleri doğrusal-dB kazanç karakteristiği, geniş ayarlama aralığı, geniş ve sabit bant genişliği, IIP_3, IP_{1dB} ve NF dir. Literatürdeki CMOS VGA devre yapılarının bant genişliklerinin kontrol gerilimi ile değişmektedir çünkü değişken kazanç çıkış empedansının değiştirilmesiyle elde edilmektedir. Bu yüzden ilk olarak, katlanmış Gilbert hücresi kullanılarak sabit bant genişlikli CMOS VGA hücresi tasarlanmıştır. Bu yapıda kazanç giriş transistörlerinin geçiş iletkenlikleri ile kontrol edilmektedir. Diğer bir yandan çıkış empedansı değişmemektedir bu yüzden de VGA'nın bant genişliği sabittir. Bant genişliğini artırmak için MOS-L yapısı kullanılmıştır. CMOS teknolojilerde transistorlar üstel karakteristiğe sahip değillerdir. Bu yüzden, sözde üstel veya Taylor serisi yaklaşımı fonksiyonları üstel karakteristik elde etmek için kullanılır. Doğrusal-dB kazanç karakteristiği elde etmek için Taylor serisi yaklaşım metodu kullanılmıştır. Taylor serisi yaklaşım metodu kullanılarak bir üstel akım üretici devresi tasarlanmıştır. Önerilen VGA devresinin ana kısmı katlanmış Gilbert hücresidir, bu yüzden bu kısmın maksimum kazancı yüksek değildir. Bu yüzden önerilen VGA devresinin kazanç seviyesini artırmak için üç tane kuvvetlendirici kullanılmıştır. Devre gerçeklemesi Spectre devre simülatörü kullanılarak yapılmıştır. Benzetimler UMC 0.13µm CMOS teknolojisi model parametreleri temel alınarak yapılmıştır. Tasarlanan VGA 21 dB doğrusal kazanç aralığına ve 3 GHz sabit 3-dB band genişliğine sahiptir.

1. INTRODUCTION

The VGA (Variable Gain Amplifier) is an important block of many systems such as medical equipment, disk drives and wireless communication systems etc. The VGA is commonly used in analog gain control (AGC) loops to obtain high dynamic range. High gain is required to get low noise characteristics in RF (Radio Frequency) systems however high gain decreases the linearity of the system. Such that, when the input signal level is high, some blocks saturate due to the high gain and decrease the linearity. In these systems, gain is controlled according to the input signal level to obtain constant output signal level.

There are two ways to design the VGA. One of them is the digital VGA and other is the analog VGA. Digital VGA's gain is controlled with digital control signal and the gain of the analog VGA is controlled with an analog control signal [1]. In general, digitally controlled VGA's gain is controlled by binary weighted arrays of resistors

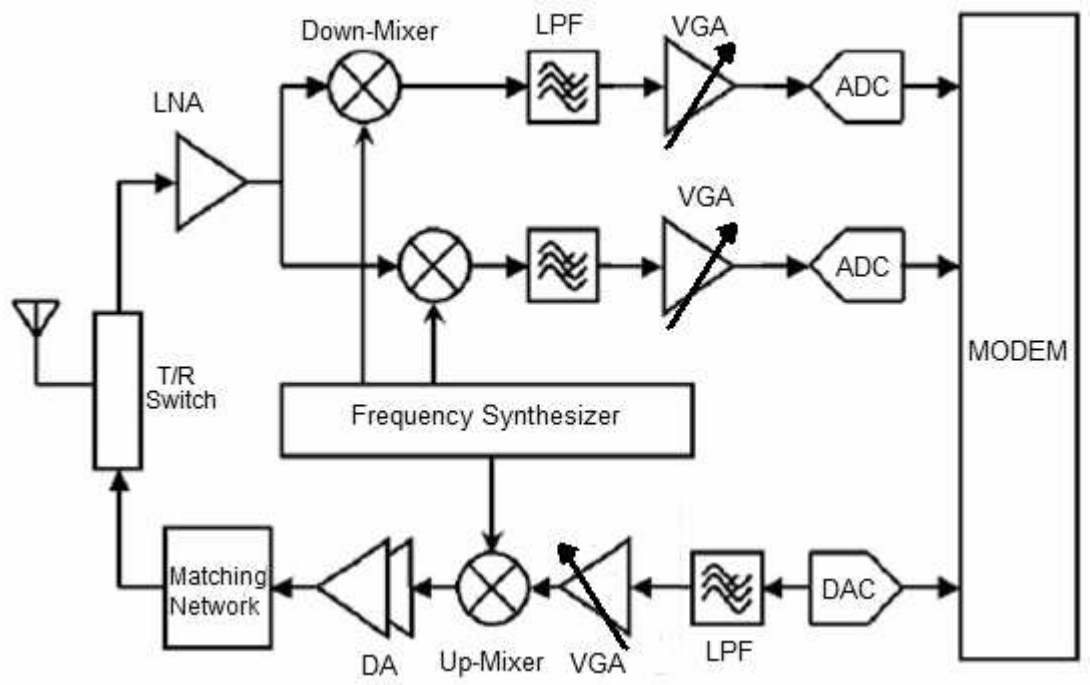

Figure 1.1: Transceiver architecture for DS-CDMA UWB systems [4]

or capacitors [2], and the analog VGA's gain is controlled by variable transconductance or resistance stages. The analog VGA is commonly preferred because of fewer control signals [3].

VGA can be used in different stages in receiver blocks. In Figure 1.1, an example of a transceiver architecture is shown. The VGA in receiver chain of the transceiver comes after mixer and LPF (Low Pass Filter). A signal, which is an RF signal, is received from the antenna and passed to the LNA (Low Noise Amplifier), and then it is amplified by the LNA. After that, down conversion mixer decreases the carrier frequency from RF to IF (Intermediate Frequency). Thus, the VGA in this system operates at intermediate frequencies.

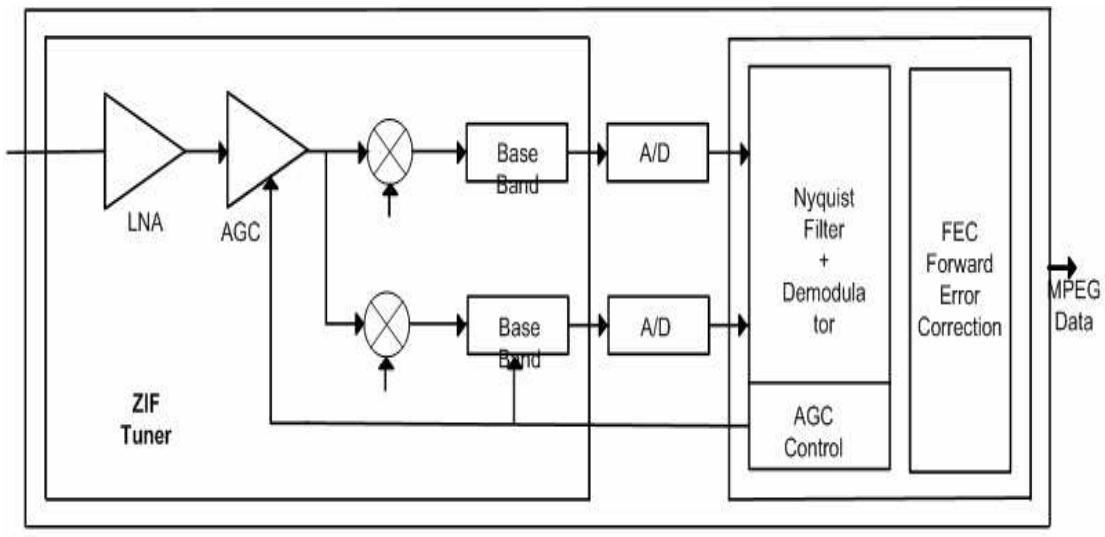

Figure 1.2: Block diagram of RF tuner for digital satellite broadcasting [5]

In Figure 1.2, an RF tuner architecture for digital satellite broadcasting is shown. There are two VGAs in this system, RF and IF VGA. Optimum SNR (Signal to Noise Ratio) is obtained by a 2-stage gain-controlled amplifier. The RF-VGA comes after the LNA and it amplifies or attenuates signal before the mixer. Thus, this VGA operates in radio frequency. This stage has a 24 dB gain control range at RF input and allows optimizing the dynamic range at the mixer [5]. IF VGA is used in base band block, which comes after the mixer. The VGA of this system helps to obtain specs of mixer, IIP_3 and IIP_2, and also increases reverse-isolation and decreases LO (Local Oscillator)-leakage.

Gain control range, input third order intercept point (IIP_3), NF (Noise Figure) and wide bandwidth are important specifications of the VGA.

Chapter 2 includes different CMOS VGA topologies and methods to obtain linear-in dB gain characteristic, and also challenges of the VGA.

Chapter 3 presents the proposed VGA and complete theoretical analysis of the blocks of the proposed VGA.

Chapter 4 presents the simulation results of the proposed VGA using UMC 0.13µm CMOS process.

Chapter 5 includes a review of the thesis and conclusion.

2. CONCEPTS AND CHALLENGES OF THE VGA

2.1 Concepts of the VGA

In this chapter, the different CMOS VGA topologies in literature are reviewed to understand methods to obtain variable gain characteristic using CMOS devices. Pseudo exponential and Taylor series approximation methods are introduced to understand how to get an exponential function using CMOS devices. And then, challenges and important specifications of the VGA are clarified.

2.1.1 The VGA Circuit-1

In CMOS technology, devices do not have an exponential characteristic so the exponential signal generation is not realized directly. Pseudo exponential or Taylor series approximation functions are used to obtain the exponential characteristic and these functions are respectively given by

$$e^{2ax} \cong \frac{(1+ax)}{(1-ax)} \tag{2.1}$$

$$e^{2ax} \approx 1+\frac{2a}{1!}x+\frac{(2a)^2}{2!}x^2 = \frac{1}{2}\left[1+(1+2ax)^2\right] \tag{2.2}$$

where a is a constant and x is an independent variable, respectively. These approximations are valid for $|2ax| << 1$ [3].

Figure 2.2 and Figure 2.3 shows the amplifying and control circuit of the VGA in [3]. In this circuit, a new exponential approximation equation is realized, which is expressed as

$$e^{2ax} = \frac{e^{ax}}{e^{-ax}} \cong \frac{\left[k + (1+ax)^2\right]}{\left[k + (1-ax)^2\right]} \qquad \textbf{(2.3)}$$

where k is a constant. The numerator and the denominator of equation (2.3) are the second-order Taylor series approximation of the exponential function for $k = 1$. As shown in Figure 2.1, the dB-in-linear range of equation (2.3) can be extended, for k less than unity. When k is equal to 0.15, the dB-in-linear range is more than 60 dB and also linearity error is less than ± 0.5 dB. Furthermore, the new approximation of the exponential function has more input range of x than that of the Taylor series approximation and pseudo-exponential functions as shown in Figure 2.1 [3].

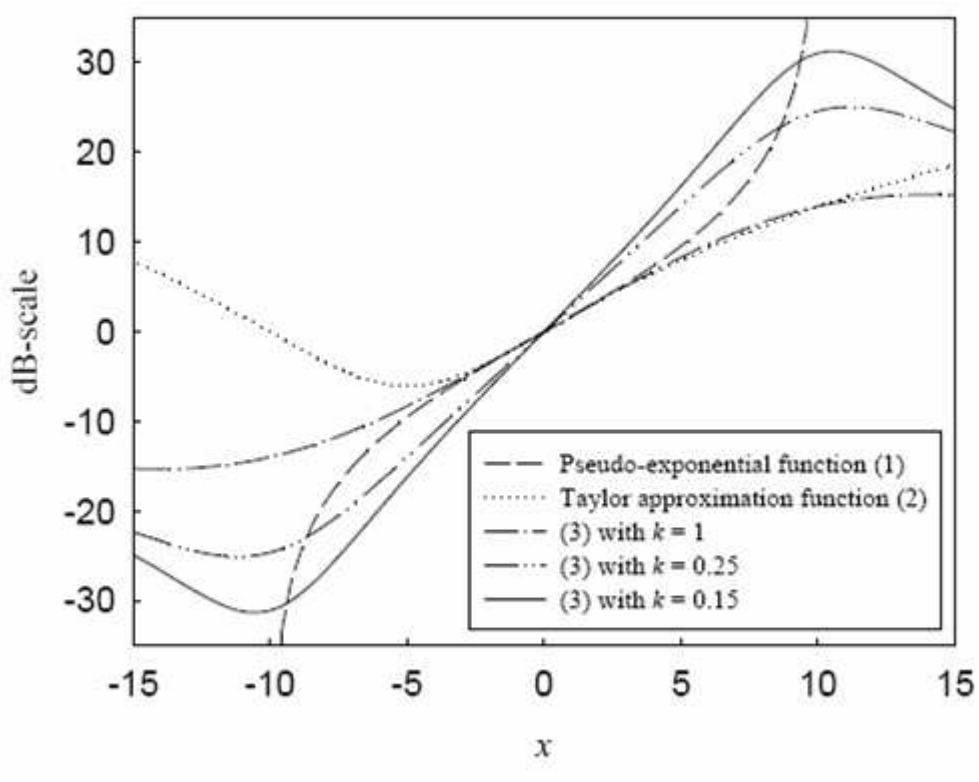

Figure 2.1: Plots of various functions on dB-scale [3]

The new exponential approximation function can easily be implemented in CMOS technology because long channel CMOS transistors have a square-law characteristic in saturation region [3].

The circuit in Figure 2.3 generates the numerator and the denominator of equation (2.3) when all transistors operate in saturation mode. To overcome the second order effects, the lengths of the transistor M_1 and M_2 should be chosen long enough. To

hold M_1 and M_2 in saturation region, the control voltage must not exceed a range of $(V_{SS} + V_{THn})$ - $(V_{DD} - |V_{THp}|)$. In saturation region, the drain current can be expressed as

$$I_{D1} = \beta_p \left(V_C - V_{DD} + |V_{THp}|\right)^2 / 2 \quad \textbf{(2.4)}$$

$$I_{D2} = \beta_n \left(V_C - V_{SS} - V_{THn}\right)^2 / 2 \quad \textbf{(2.5)}$$

where $\beta_p = \mu_p C_{ox} W / L$ and $\beta_n = \mu_n C_{ox} W / L$, which are constant process parameters, and V_{THp} and V_{THn} are the threshold voltages of the P-MOS and N-MOS

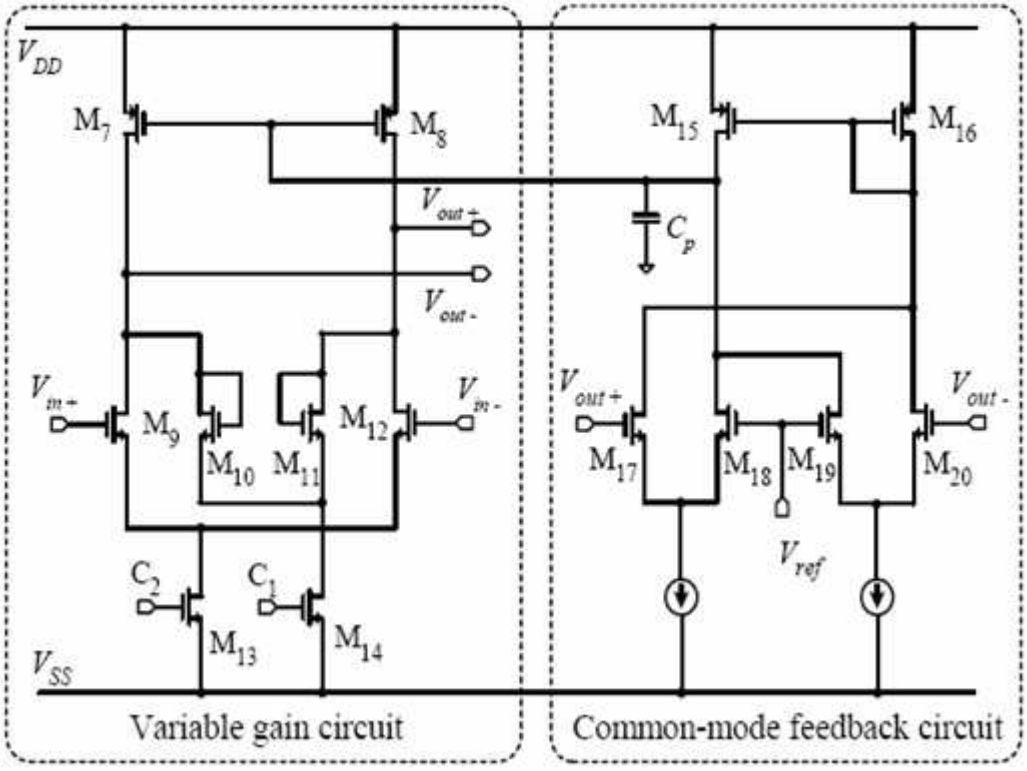

Figure 2.2: Amplifying block of the VGA Circuit-1 [3]

transistors, respectively. I_0 is a constant bias current and this current is added to drain currents of M_1 and M_2. These overall current I_{C1} and I_{C2} flow through M_5 and M_6. I_{C1} and I_{C2} can be expressed as [3]

$$I_{C1} = \beta_p \left(V_{DD} - \left|V_{THp}\right|\right)^2 \left\{ \frac{I_0}{\beta_p \left(V_{DD} - \left|V_{THp}\right|\right)^2 / 2} + [1 - \frac{V_C}{\left(V_{DD} - \left|V_{THp}\right|\right)}]^2 \right\} \Big/ 2 \qquad \textbf{(2.6)}$$

$$I_{C2} = \beta_n \left(V_{SS} + V_{THn}\right)^2 \left\{ \frac{I_0}{\beta_n \left(V_{SS} + V_{THn}\right)^2 / 2} + [1 - \frac{V_C}{\left(V_{SS} + V_{THn}\right)}]^2 \right\} \Big/ 2 \qquad \textbf{(2.7)}$$

Under the condition $\beta_p = \beta_n = \beta$ and $V_{DD} = -V_{SS}$ and $V_{THn} = \left|V_{THp}\right| = V_{TH}$, the ratio of the drain currents of the M_6 and M_5 can be given by [3]

$$\frac{I_{C2}}{I_{C1}} = \frac{\dfrac{I_0}{\beta\left(V_{DD} - \left|V_{TH}\right|\right)^2 / 2} + \left(1 + \dfrac{V_C}{(V_{DD} - \left|V_{TH}\right|)}\right)^2}{\dfrac{I_0}{\beta\left(V_{DD} - \left|V_{TH}\right|\right)^2 / 2} + \left(1 - \dfrac{V_C}{(V_{DD} - \left|V_{TH}\right|)}\right)^2} \qquad \textbf{(2.8)}$$

$$= \frac{\left[k + (1 + ax)^2\right]}{\left[k + (1 - ax)^2\right]}$$

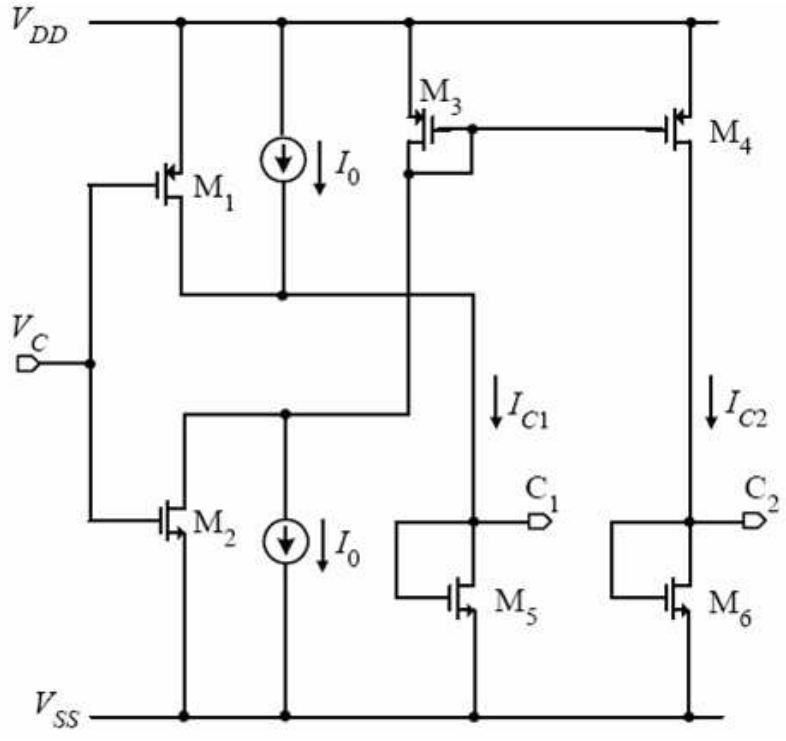

Figure 2.3: Control block of the VGA Circuit-1 [3]

where $k = 2I_0 / \beta(V_{DD} - |V_{TH}|)^2$, $a = 1/(V_{DD} - |V_{TH}|)$, and $x = V_C$. k factor of the new approximation function can be adjusted to obtain different dB-in-linear ranges using the bias current I_0 [3].

Figure 2.2 shows the schematic of the amplifying block and the common-mode feedback circuit. The output current I_{C1} and I_{C2} of the control circuit are mirrored by M_{13} and M_{14} to variable gain circuit. Gain of this circuit is given by

$$A_v = \frac{g_{m-input}}{g_{m-load}} = \sqrt{\frac{(W/L)_{input} I_{C2}}{(W/L)_{load} I_{C1}}} \quad \textbf{(2.9)}$$

where $g_{m\text{-input}}$ and $g_{m\text{-load}}$ are transconductance of the input transistors (M_9 and M_{12}) and diode connected loads (M_{10} and M_{11}) respectively, where I_{C1} and I_{C2} are given by Equation (2.8) [3]. From Equation (2.8) and (2.9), gain can be calculated as an exponential function of control voltage V_C.

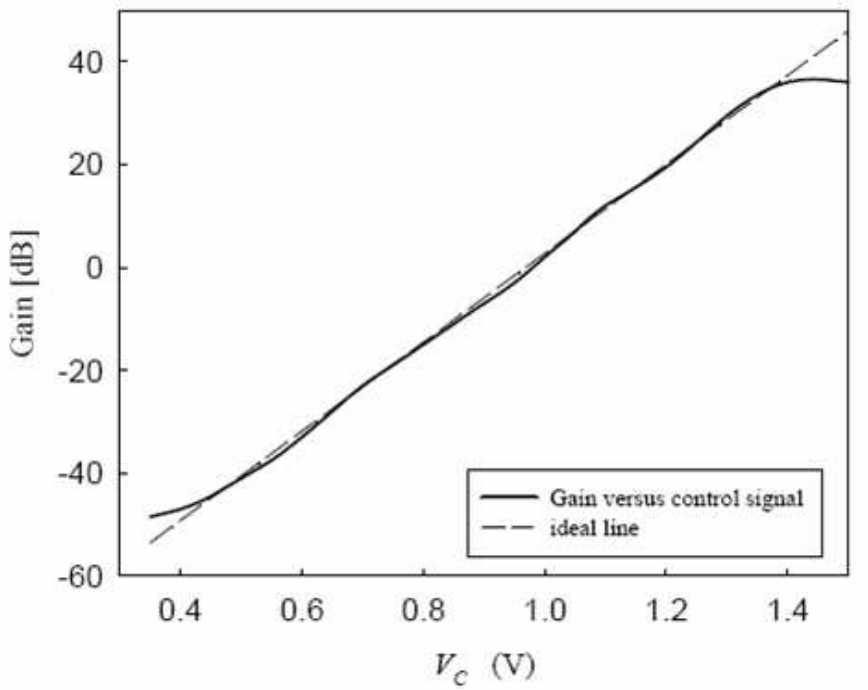

Figure 2.4: Measured gain versus control voltage V_C of the circuit in Figure 2.2 [3]

The output node capacitance and impedance determine the bandwidth of the circuit. The output impedance of the circuit can be approximated as $g_{m\text{-load}}$ which is controlled by I_{C1}. The bandwidth of the VGA has different values for high and low

gain modes because I_{C1} is changed with the square root of the control voltage V_C. Therefore, the bandwidth of the circuit varies with control voltage V_C [3]. Figure 2.4 shows the measurements of gain versus control voltage of the circuit in Figure 2.2.

2.1.2 The VGA Circuit-2

Schematic of the core pseudo-exponential approximation-based VGA is shown in Figure 2.5. This VGA is composed of a differential amplifier ($M_{1,2}$) and diode-connected loads ($M_{3,4}$). Differential gain of this circuit is product of the transconductance of the input differential transistors ($M_{1,2}$) and the output impedance. The output impedance is likely equal to $1/g_{m-M3,4}$, where $g_{m\text{-}M3,4}$ is the transconductance of the diode connected load transistors. The gain can be changed via controlling bias current of the differential input pair and the diode-connected loads because the transconductance is a function of the bias current [6]. The gain of the VGA core in Figure 2.5 is expressed as [6]

$$A_v = \frac{g_{m-M1,2}}{g_{m-M3,4}} = \sqrt{\frac{(W/L)_{M1,2} I_{M1,2}}{(W/L)_{M3,4} I_{M3,4}}} \qquad \textbf{(2.10)}$$

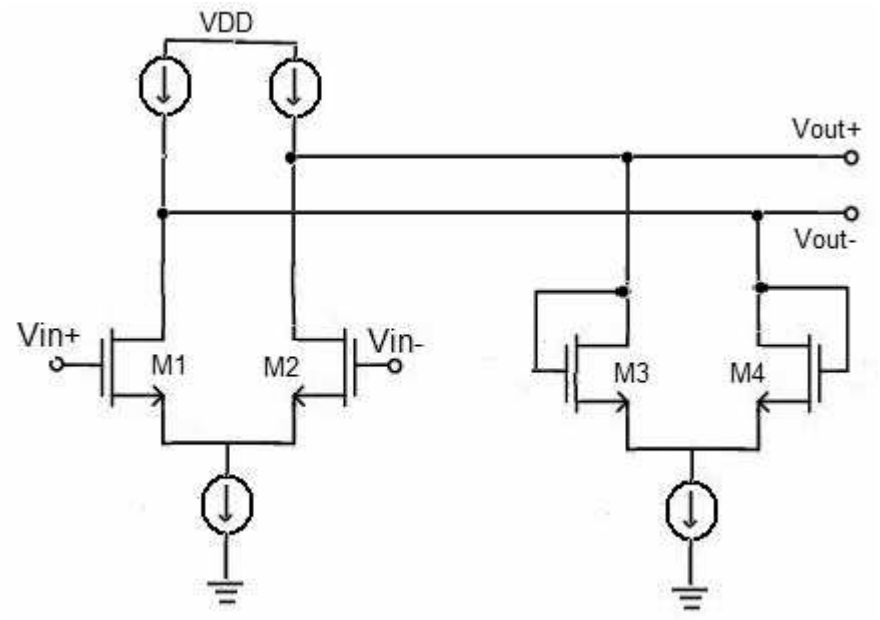

Figure 2.5: Schematic of the core pseudo-exponential approximation-based VGA [6]

The input and output poles limit the bandwidth of the VGA in Figure 2.5. The output pole impedance is dominated by the diode connected transistors, so the bias current of these transistors changes the output pole frequency. The bandwidth is wide when the gain is low. On the other hand, if the gain increases, the bandwidth decreases [3]. The input capacitance determines the input pole. In Figure 2.5, the overall capacitance at the input node of the input transistor is equal to C_{GS}, which is gate-source capacitance of the input transistor, plus Miller multiplication of C_{GD}, which is gate-drain capacitance of the input transistor. From this process, input capacitance: $C_{GS} + (1 + |A_v|)C_{GD}$, where A_v is as expressed in Equation (2.10). The input capacitance increases significantly because of Miller multiplication when the gain is high and this limits the bandwidth of the circuit [6].

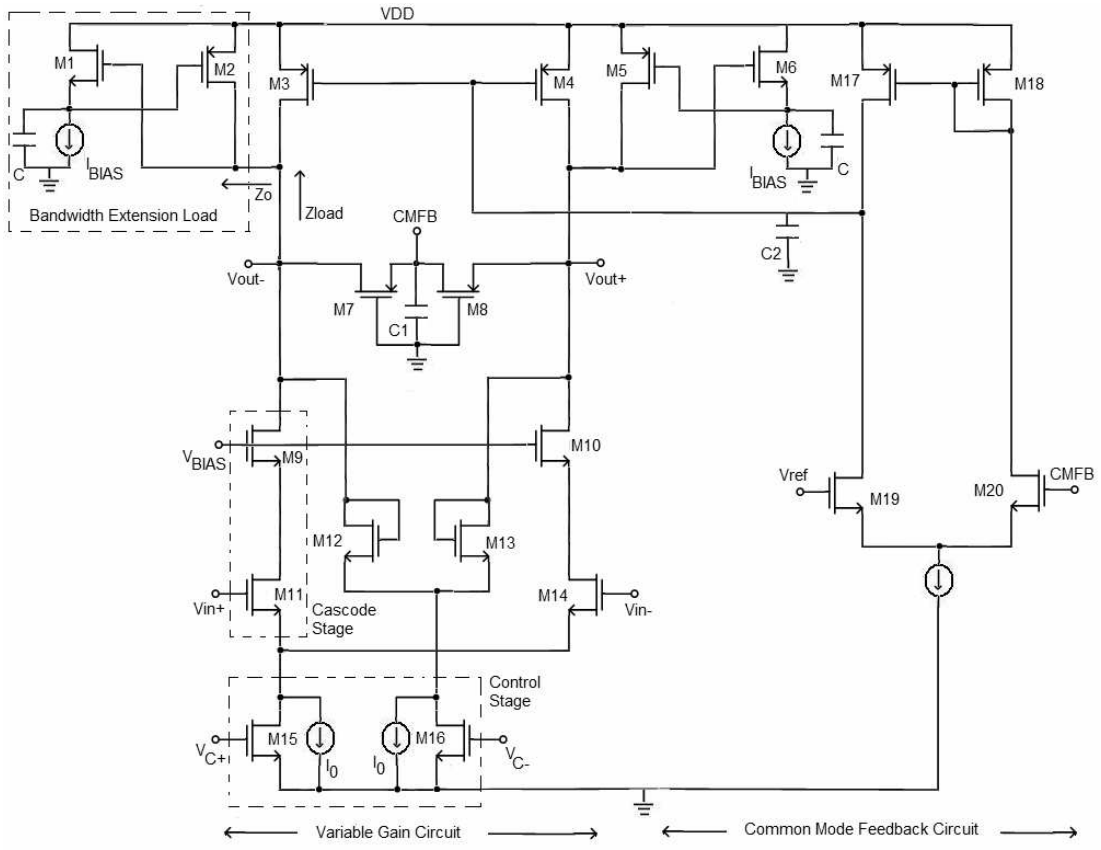

Figure 2.6: Schematic of the complete VGA in [6]

In Figure 2.6, cascode transistors ($M_{9,10}$) and active inductive load extend the bandwidth of the VGA. Miller multiplication can be reduced by giving same size to M_9 (M_{10}) and M_{11} (M_{14}) because the gain from input to drain of transistor M_{11} is

equal to $g_{m-M11} / g_{m-M9} = 1$ when the size of the input and cascode transistor are same. As a result, wider bandwidth is achieved by transferring the input pole to a higher frequency [6]. The load impedance, Z_{load}, is equal to $Z_0 // Z_{M13} \sim Z_0$ in Figure 2.6. The input impedance of the bandwidth extension load can be expressed as [7]

$$Z_0 \cong \frac{1}{g_{m-M2}}\left(1+\frac{s}{g_{m-M1}/C}\right) \qquad \textbf{(2.11)}$$

As shown from Equation (2.11), a "zero" comes to the output node from this extension load, and this increases the bandwidth [6]. In Figure 2.7, bandwidth extension and bandwidth extension load are shown. Z_{load} does a peaking because of bandwidth extension load and this increases the bandwidth.

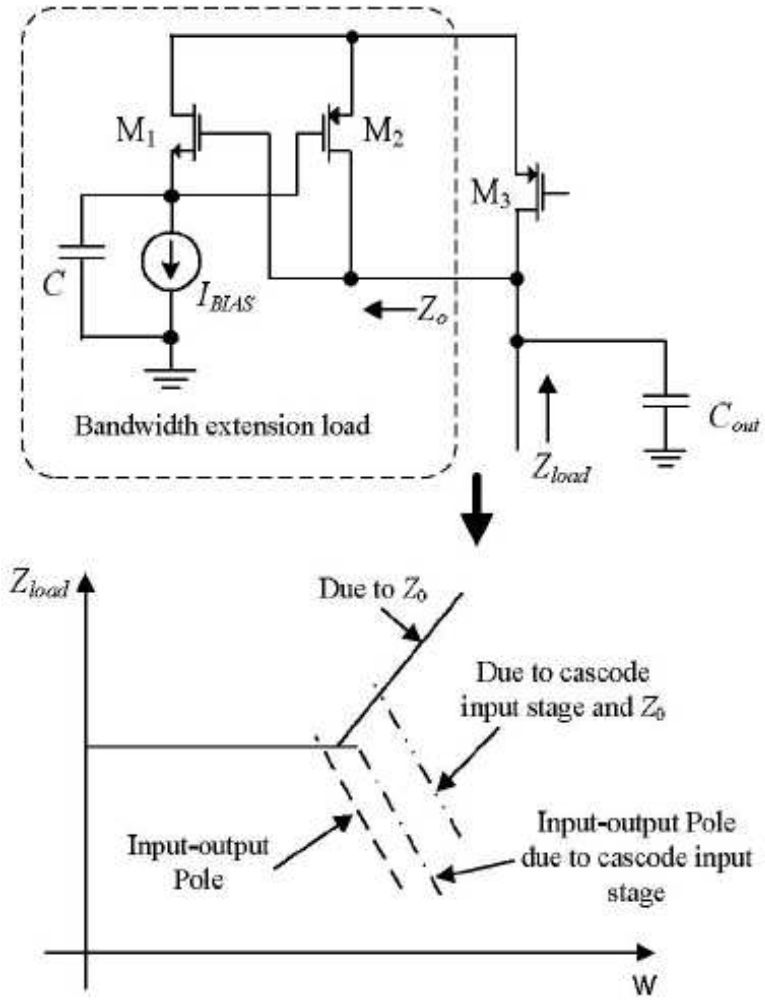

Figure 2.7: Bandwidth extension and bandwidth extension load [6]

The control stage in Figure 2.6 has a differential control signal, $V_{C+} = V_{BIAS} + V_C$ and $V_{C-} = V_{BIAS} - V_C$, where V_{BIAS} is the bias voltage and V_C is the differential control voltage. The control transistors, M_{15} and M_{16}, operate in saturation mode. The bias current of the input transistors ($M_{11,14}$) and loads ($M_{12,13}$) can be expressed as [6]

$$I_{M11,14} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{BIAS} + V_C - V_{TH}\right)^2 + I_0 \tag{2.12}$$

$$I_{M12,13} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{BIAS} - V_C - V_{TH}\right)^2 + I_0 \tag{2.13}$$

where V_{TH} represents the threshold voltages of NMOS transistors and I_0 is the bias current. From Equations (2.10), (2.12) and (2.13), the overall gain of the VGA can be given by [6]

$$A_v = \frac{g_{m-M11,14}}{g_{m-M12,13}} = \sqrt{\frac{(W/L)_{M11,14} I_{M11,14}}{(W/L)_{M12,13} I_{M12,13}}} \tag{2.14}$$

Under the condition $(W/L)_{M11,14} = (W/L)_{M12,13}$, from Equations (2.12), (2.13) and (2.14), the gain of the VGA in Figure 2.6 is expressed as [6]

$$\begin{aligned} A_v &= \left(\frac{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{BIAS} + V_C - V_{TH}\right)^2 + I_0}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{BIAS} - V_C - V_{TH}\right)^2 + I_0}\right)^{1/2} \\ &= \left(\frac{\frac{I_0}{\beta(V_{BIAS} - V_{TH})^2/2} + \left(1 + \frac{V_C}{V_{BIAS} - V_{TH}}\right)^2}{\frac{I_0}{\beta(V_{BIAS} - V_{TH})^2/2} + \left(1 - \frac{V_C}{V_{BIAS} - V_{TH}}\right)^2}\right)^{1/2} \\ &= \left(\left[\frac{k + (1+ax)^2}{k + (1-ax)^2}\right]\right)^{1/2} \end{aligned} \tag{2.15}$$

where $k = 2I_0 / \beta(V_{BIAS} - V_{TH})^2$, $a = 1/(V_{BIAS} - V_{TH})$ and $\beta = \mu_n C_{ox} W / L$.

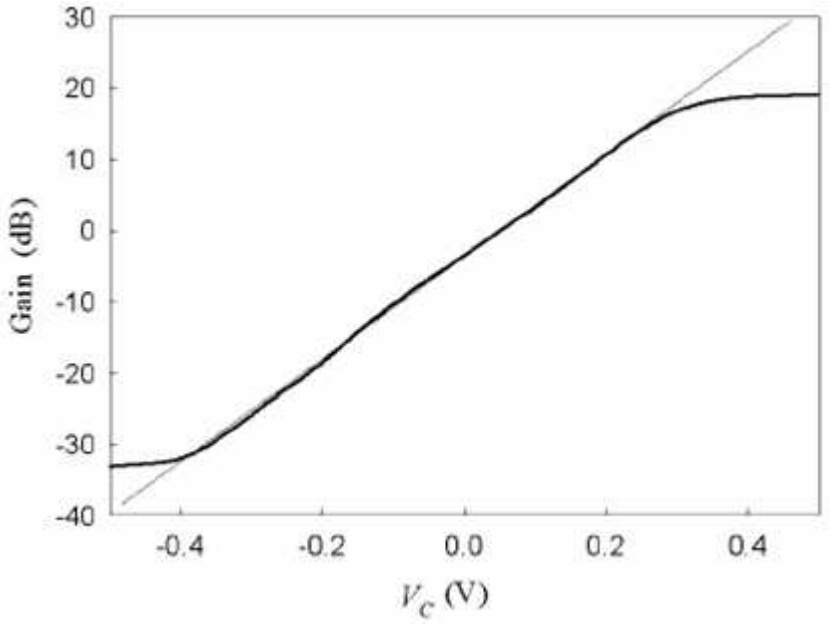

Figure 2.8: Simulated gain versus the control voltage of the VGA shown in Figure 2.6 [6]

Figure 2.8 and Figure 2.9 show the simulation results of the VGA in Figure 2.5 and Figure 2.6. As shown in Figure 2.9, the bandwidth of the VGA increases as a result of the extension load but it is not constant.

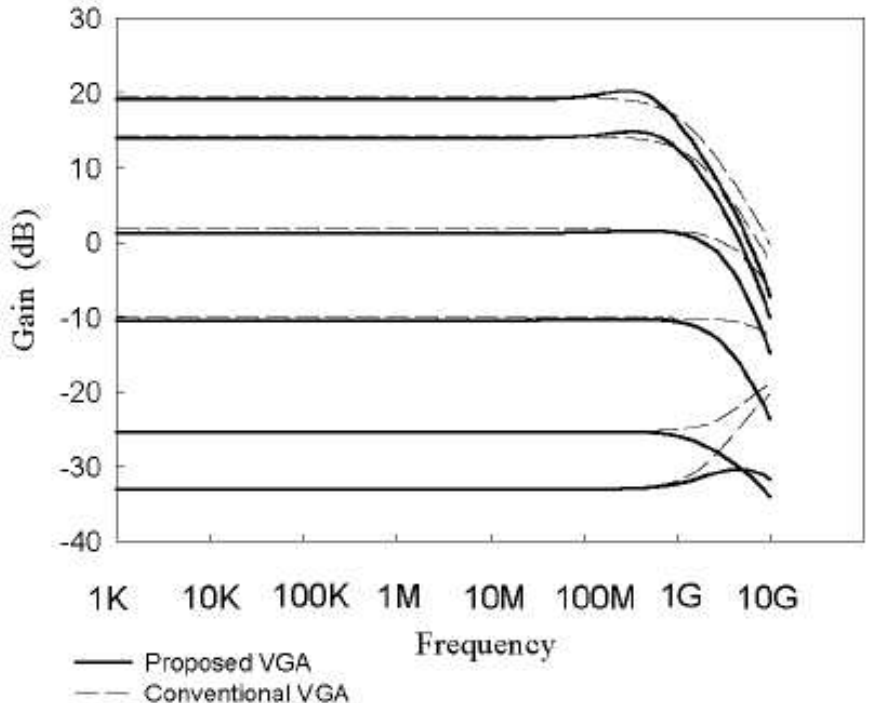

Figure 2.9: Simulated gain versus frequency at the different gain setting of the VGA shown in Figure 2.6 [6]

2.1.3 The VGA Circuit-3

Figure 2.10 and Figure 2.11 show the unit cell and whole circuit of the VGA in [4], respectively. The output resistance of the cascode configuration is higher, so is the gain. Moreover the input capacitance is lower because of small Miller multiplication than that of the simple common source amplifier. Thus, this configuration is commonly used to obtain a wideband VGA [4]. The circuit in Figure 2.10 is composed of a common-source transistor M_1, a common-gate transistor M_2, and a source load transistor M_3. The output resistance and the gain of this circuit are expressed as

$$R_o = [r_{o2}(1 + g_{m2} r_{o1})] // r_{o3} \quad \textbf{(2.16)}$$

$$A_v \approx -g_{m1}[(r_{o2}(1 + g_{m2} r_{o1})) // r_{o3}] \approx -g_{m1} r_{o3} \quad \textbf{(2.17)}$$

where, g_{m1}, g_{m2} and g_{m3} are the transconductance and r_{o1}, r_{o2} and r_{o3} are the output resistance of M_1, M_2 and M_3, respectively. As shown in Equation (2.17), gain can be controlled via g_{m1} by controlling the gate voltage of M_2, V_{GG2} [4].

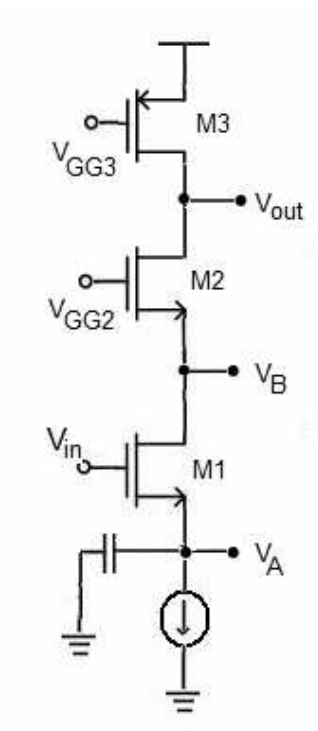

Figure 2.10: A cascode configuration [4]

When the input transistor M_1 is in triode region, the drain current and g_{m1} of M_1 can be given by

$$I_{DS1} = \frac{\mu_n C_{ox} W}{L}\left((V_{GS1} - V_{TH}) - \frac{V_{DS1}}{2}\right)V_{DS1} \quad \textbf{(2.18)}$$

$$g_{m1} = \beta . V_{DS1} \quad \textbf{(2.19)}$$

where, $0 < V_{DS1} < (V_{GS1} - V_{TH})$ and $\beta = \mu_n C_{ox} W / L$.

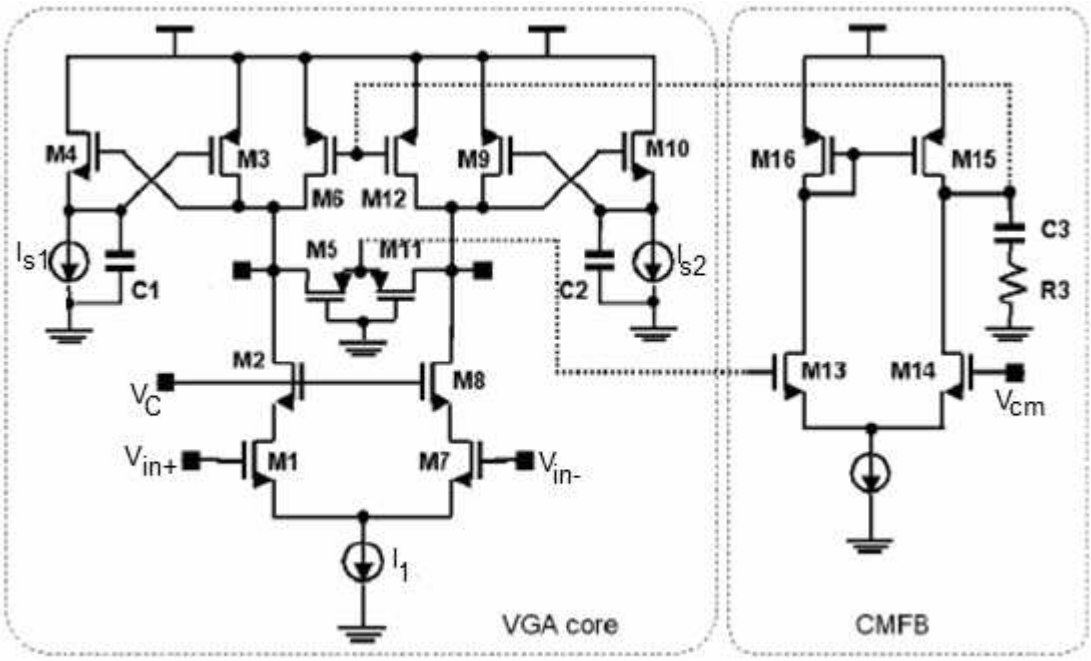

Figure 2.11: The VGA based on cascode configuration in Figure 2.10 [4]

When the input transistor M_1 is in saturation region, the drain current and g_{m1} of M_1 can be given by

$$I_{DS1} = \frac{\mu_n C_{ox} W}{2L}(V_{GS1} - V_{TH})^2 \quad \textbf{(2.20)}$$

$$g_{m1} = \beta(V_{GS1} - V_{TH}) = \sqrt{2\beta . I_{DS1}} \quad \textbf{(2.21)}$$

where, $V_{DS1} > (V_{GS1} - V_{TH})$.

When the input transistor operates in triode region, the transconductance of M1 can be controlled by the drain-source voltage of M_1. From Equations (2.18) and (2.20), the drain-source voltage of M_1 can be expressed as [4]

$$\frac{V_{DS1}}{\sqrt{2A}} = V_x + \sqrt{V_x^2 + 1} \tag{2.22}$$

where, $A = \frac{2I_{DS}}{\beta}$ and $V_x = \frac{V_{GG2} - V_{TH2} - (V_{in} - V_{TH1})}{\sqrt{2A}} - \frac{1}{\sqrt{2}}$. From Equation (2.17), that result can be obtained; the gain of the circuit can be controlled via controlling V_{DS1} when input transistor is in triode region. Right side of Equation (2.22) is in the form of an inverse hyper-tangent function. Its Taylor's series can be given by [4]

$$V_x + \sqrt{V_x^2 + 1} = 1 + \frac{1}{1!}V_x + \frac{1}{2!}V_x^2 + ... \approx e^{V_x} \tag{2.23}$$

20 dB linear-in-dB gain can be obtained using Equation (2.22) for $|V_x| \leq 1$. Thus, the overall gain characteristic can be obtained as linear in dB.

The VGA in Figure 2.11 is a differential pair which is adopted from cascode block in Figure 2.10. An active inductive load is used for wide bandwidth, and cascode configuration also increases the bandwidth [4]. In this circuit, M_1 and M_7 operate in triode region and M_2 and M_8 operate in saturation region. The gain of the VGA in Figure 2.11 can be calculated as [4]

$$A_v \approx -2g_{m1}\frac{C_1}{g_{m\_M3}g_{m\_M4}}\left(s + \frac{g_{m\_M4}}{C_1}\right) \tag{2.24}$$

The dominant pole comes from the output node. The output impedance and capacitance are nearly constant. Therefore, the bandwidth of the VGA is constant with respect to the control voltage.

2.1.4 The VGA Circuit-4

Figure 2.12 shows the architecture of the VGA in [1]. This architecture consists of three VGA cells, a fixed gain amplifier at the output, an exponential control voltage generator and a dc offset canceller. To obtain a dB-in-linear gain characteristic, the

external control voltage V_{EXT} must be changed to internal V_C, which has an exponential characteristic. The control voltage generator circuit inverts an external control voltage to an internal control voltage.

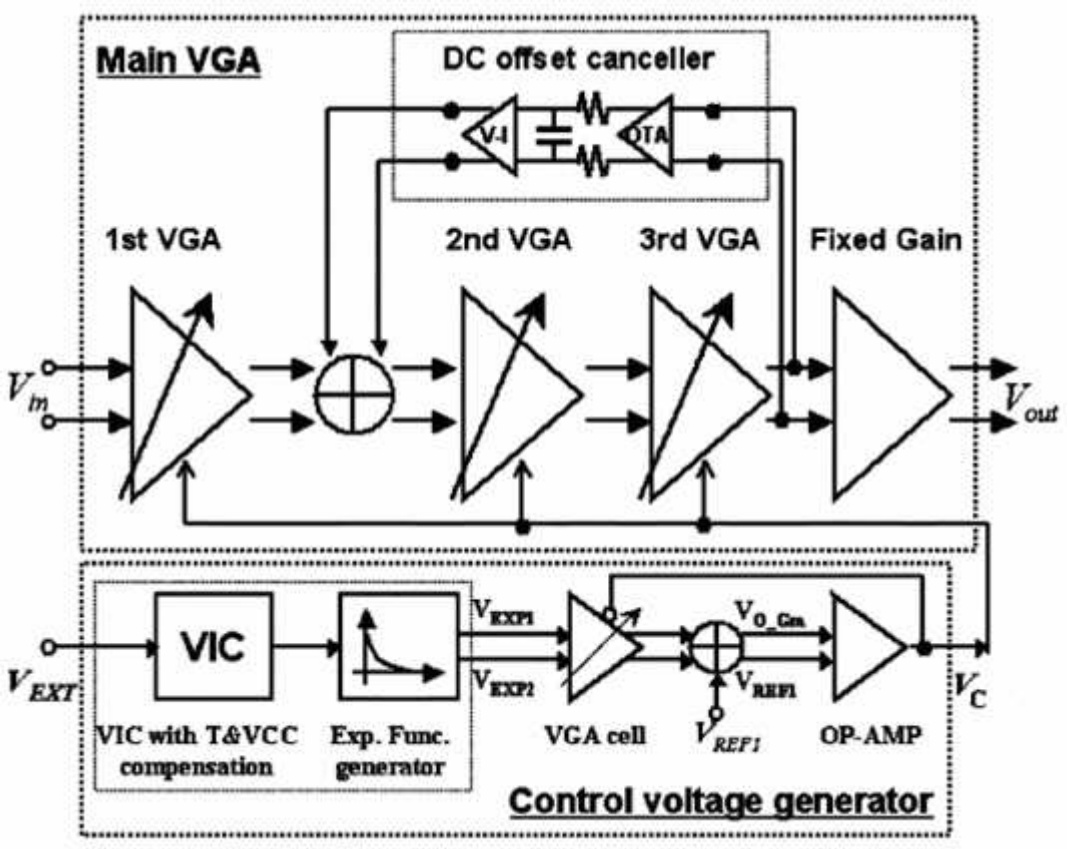

Figure 2.12: Architecture of the VGA [1]

The VGA cell is shown in Figure 2.13. This circuit is composed of a cascode topology, which reduces the Miller effect and increases the bandwidth. And also, the bandwidth extension load is used to increase the bandwidth. The input transistors, M1 and M6, operate in triode or saturation region depend on internal control voltage V_C. When these transistors operate in saturation region, a high gain is get. If the input transistors are in triode region, a low gain is get. The variable gain is obtained via the transconductance of the input transistors, g_{m1} and g_{m6}. The transconductance in triode and saturation region of the input transistors can be given by Equations (2.19) and (2.21), respectively.

A load network is composed of active loads (M_3, M_8, R_1, C_1), bleeding current sources (M_4, M_9), and dc level sensing transistors (M_5, M_{10}) [4]. The dc level sensing transistors and Common Mode Feedback (CMFB) circuit bias the bleeding current

source transistors. The output impedance of the bleeding current sources and dc level sensing transistors are high enough to ignore when calculating the load impedance. Therefore, the output impedance is determined by the output impedance of the active load [1].

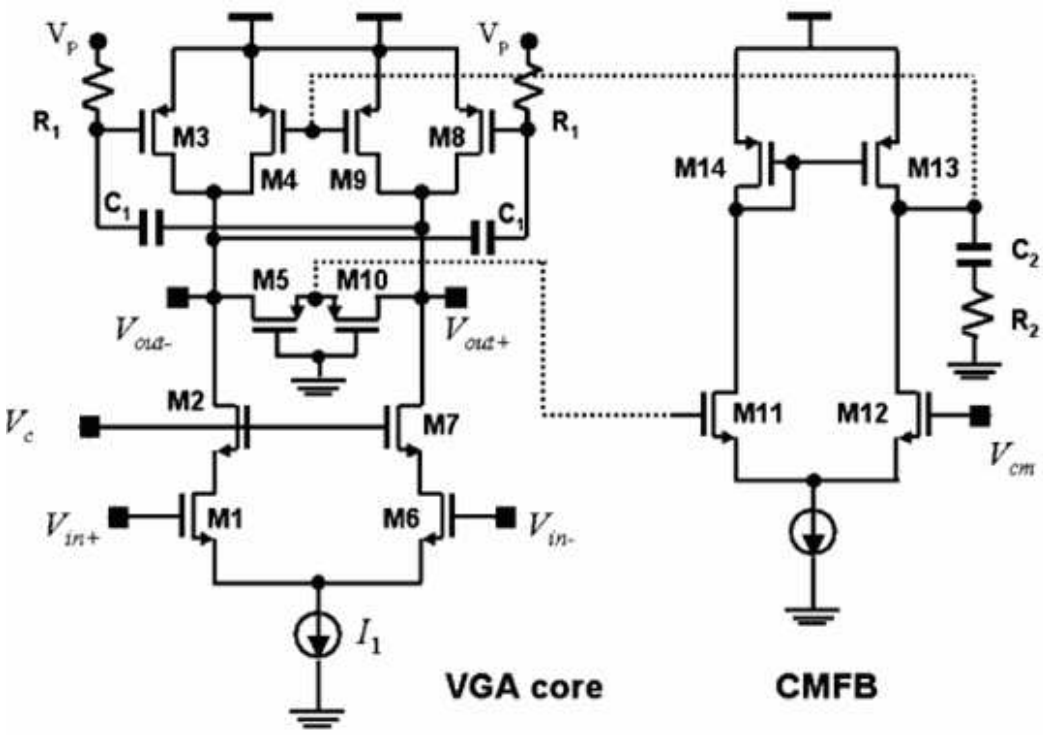

Figure 2.13: The VGA schematic in [1]

The small-signal equivalent circuit of the bandwidth extension load of the VGA in Figure 2.13 is shown in Figure 2.14. From the small signal equivalent circuit, the output impedance can be given by [1]

$$
\begin{aligned}
Z_O &\cong \frac{2r_o\left[1+sR_1\left(C_1+C_{GD}+C_{GS}\right)\right]}{D(s)} \\
D(s) &= 1+s\left[R_1\left(C_1+C_{GD}+C_{GS}\right)+r_o\left(C_1+C_{GD}-C_1 g_m R_1+C_{GD} g_m R_1\right)\right] \\
&\quad + s^2 r_o R_1\left[4C_1C_{GD}+\left(C_1+C_{GD}\right)C_{GS}\right]
\end{aligned}
\qquad \textbf{(2.25)}
$$

where g_m is the transconductance, r_o is the output resistance, C_{GD} is the gate-drain capacitance, and C_{GS} is the gate-source capacitance of M_3 or M_8. From Equation (2.25), the output impedance is nearly equal to $2r_o$ at the low frequency region. In the high frequency region, the output impedance does the peaking like an inductance load. This load has a zero point at the frequency $\omega_z = 1/R_1\left(C_1+C_{GD}+C_{GS}\right)$ [1].

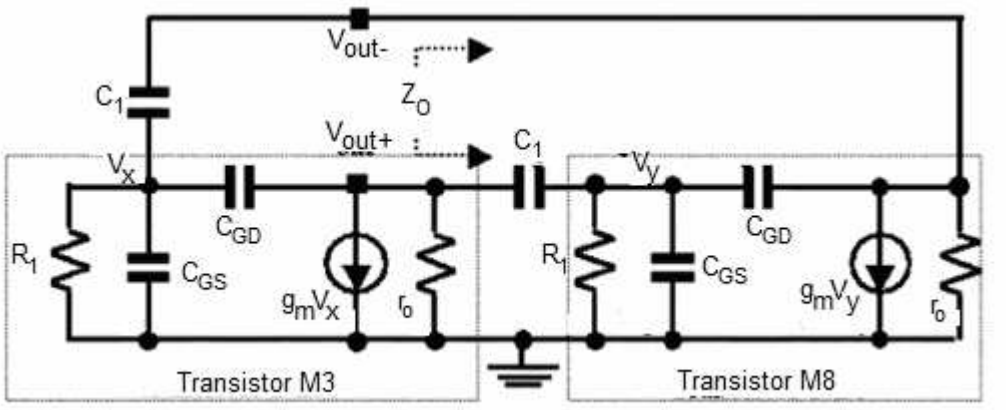

Figure 2.14: Small-signal equivalent circuit of the bandwidth extension load of the VGA in Figure 2.13 [1]

As shown in Figure 2.15, the active load acts like an inductance at the high frequency, and boosts the gain. As shown in Figure 2.15, 3-dB frequency can be extended using the value of the capacitor C_1 [1].

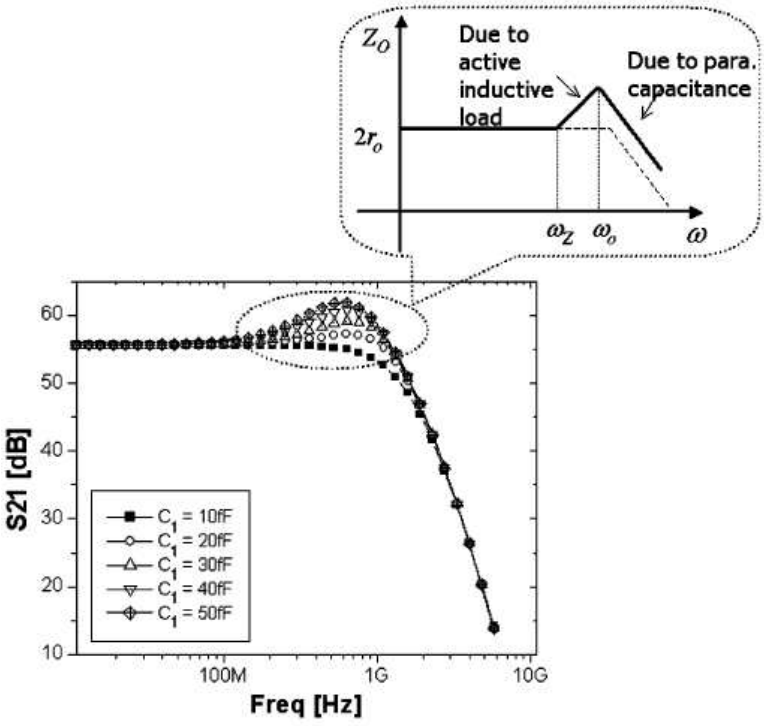

Figure 2.15: Frequency response of the VGA using a gain boosting technique with various C_1 values (10~50 fF)

The overall gain of the VGA cell can be expressed as [1]

$$A_v \approx -g_{m1} Z_O \qquad \textbf{(2.26)}$$

Figure 2.16 shows the measured and simulated gain characteristics of the circuit in Figure 2.12.

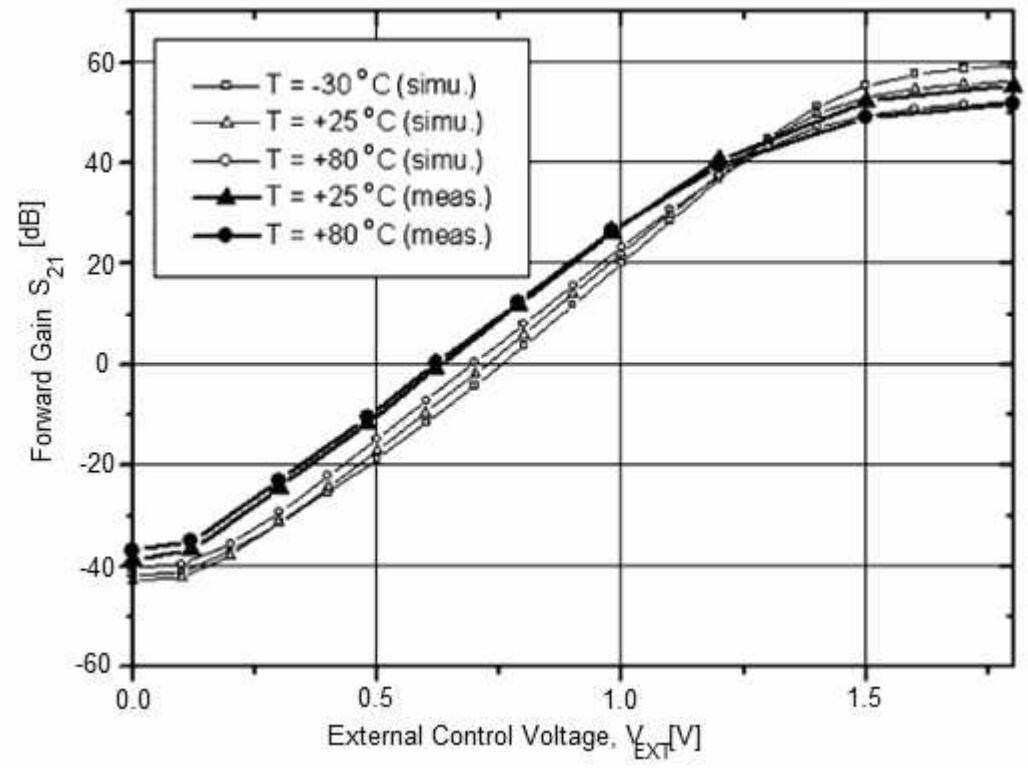

Figure 2.16: Measured and simulated gain characteristics with temperature variation of the circuit in Figure 2.12 at a test frequency of 100 MHz [1]

2.1.5 The VGA Circuit-5

In Figure 2.17, low voltage VGA topology and subcircuit schematic are shown. This topology is composed of a VGA cell, five post amplifiers, an offset extraction circuit and an output buffer. The post amplifiers are required to get sufficient gain to increase sensitivity. To overcome the dc offset voltage, which occurs because of device mismatch, the dc offset canceling feedback circuit is needed. This circuit is a low pass filter. A high-speed output buffer is used to drive off-chip loads [8].

In the post amplifier stage, MOS-L is used for bandwidth extension [9]. MOS-L has an inductive characteristic at the high frequency. A post amplifier stage has 6 dB

voltage gain and a bandwidth higher than 10 GHz. The low pass filter in dc offset cancellation circuit consists of a PMOS transistor operating in triode region, acts as resistor, and an NMOS transistor as a capacitor. Its drain, source, and body are connected to ground. The output buffer consists of two stages to drive off-chip loads. The last stage has 5 mA tail current and inductive loads [8].

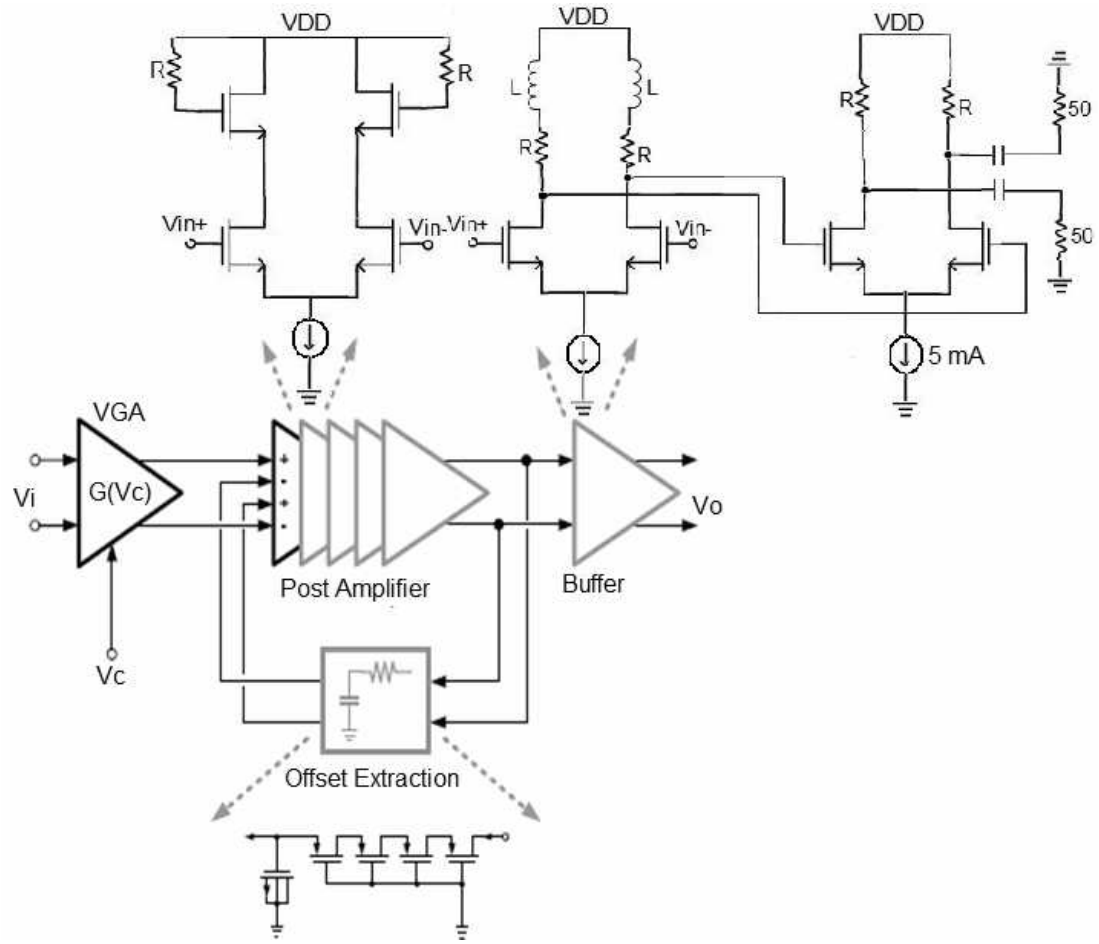

Figure 2.17: Low voltage VGA topology and subcircuit schematic [8]

Figure 2.18 (a) shows the Gilbert type four-quadrant multiplier which is used to obtain a linear gain characteristic with respect to the control voltage V_C because the product of the two inputs gives its output [10]. The output signal can be given by [8]

$$\begin{aligned} V_{o+} - V_{o-} &= \left(g_{m3,4} - g_{m5,6}\right) R\left(V_{in+} - V_{in-}\right) \\ &= \sqrt{\frac{\beta}{2I_{ss}}}\, g_{m1,2}\left(V_{C+} - V_{C-}\right)\left(V_{in+} - V_{in-}\right) \end{aligned} \qquad \textbf{(2.27)}$$

where, $g_{m3,4}$ and $g_{m5,6}$ are the transconductance of the input transistors, $g_{m1,2}$ is the control transistor's transconductance and I_{ss} is the tail current. All transistors operate in saturation region and these three differential pairs act as linear transconductors. The conventional cascode Gilbert cell structure implementation has two difficulties. It needs a high supply voltage and it has a low tuning range of the control voltage because the gain polarity is not constant with the control voltage [8]. The gain polarity is different when $g_{m3,4}$ is lower than or higher than $g_{m5,6}$. When the control voltage changes, difference of $g_{m3,4}$ and $g_{m5,6}$ causes the polarity changes of the voltage gain.

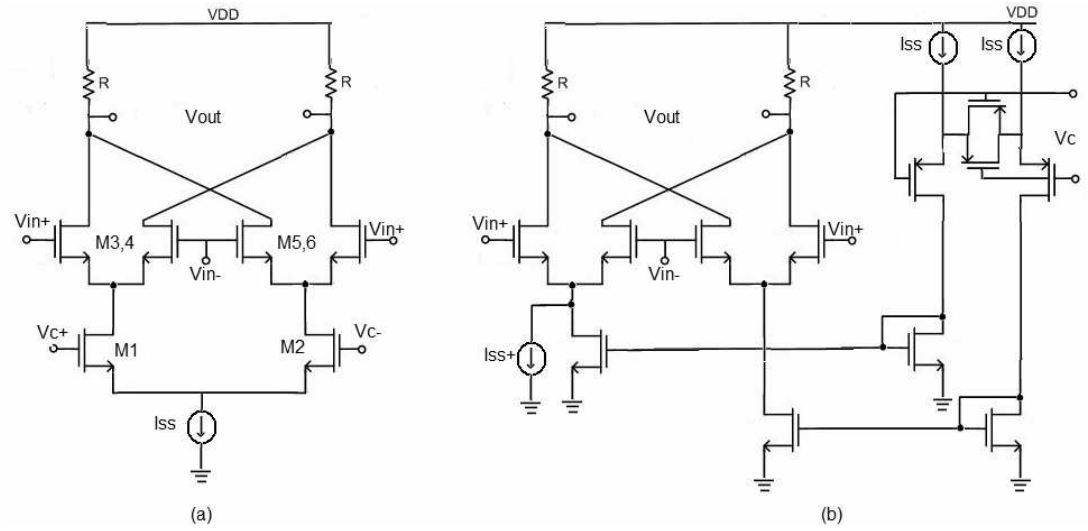

Figure 2.18: (a) Conventional Gilbert cell (b) Folded VGA structure [8]

Figure 2.18 (b) shows the proposed VGA in reference [8] to solve the drawbacks. To solve the high voltage requirement of the cascode structure, the folded structure is used instead of bottom differential pair of the original Gilbert cell. A constant current source which is greater than I_{ss} eliminates the polarity change. Using this current source, one of the differential pair's transconductance is always greater than the others', within entire control voltage range. Thus, this increases the tuning range of the VGA with respect to the control voltage [8].

The voltage gain; A_v, can be obtained from S-parameters as Equation (2.28) [8].

$$A_v = \frac{2S_{21}}{(1+S_{11})(1-S_{22})+S_{21}S_{12}} \qquad \textbf{(2.28)}$$

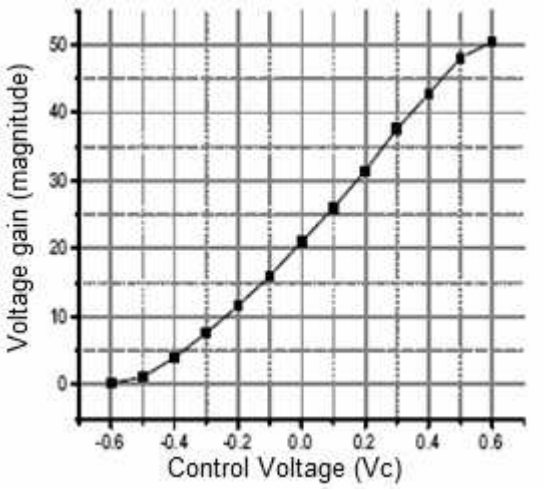

Figure 2.19: Voltage gain versus control voltage V_C [8]

The measured voltage gain versus control voltage is shown in Figure 2.19. The voltage gain of this circuit is linear-in-magnitude. The control circuit of the folded VGA in Figure 2.18 (b) is a differential pair with a linearization technique. Tail current is followed to one of the input differential pair by the control circuit's differential pair, and the variable gain is obtained. This control circuit does not generate an exponential function. It generates a linear function. Thus, the variable gain has a linear-in magnitude characteristic.

2.2 Challenges of the VGA

CMOS processes are widely used for analog and mixed signal application circuits because of low price and high integration for digital circuits. Linear in dB gain control is an important challenge in the analog VGA because of CMOS transistors. An exponential control voltage is required to obtain linear in dB gain characteristic but CMOS transistors do not have an exponential characteristic so this is the most important challenge in CMOS processes. In spite of the facts that, in subthreshold region CMOS transistors have an exponential characteristic, it is commonly not preferred because of poor noise and bandwidth performance [11]. Thus, parasitic bipolar transistor, pseudo-exponential function generation, or second order approximation of Taylor's series are widely used to overcome this challenge.

Wide tuning range is required to achieve high dynamic range. Approximation methods of the exponential function generation in CMOS technology are not valid in a wide range, so another challenge of the VGA is the wide tuning range. To extend the tuning range, two or three VGA cores are used as cascade, but this increases power dissipation.

Bandwidth is another important specification for many applications. The bandwidth of many of the VGA concepts in CMOS technology is not high and constant. Gain of the VGA is controlled by the output impedance in many VGA circuits, but the dominant pole comes from the output node. Thus, the bandwidth is changed by the control voltage.

IP_3 (Third Order Intercept Point) of the VGA is significant for many systems because this affects linearity and dynamic range of the systems. The VGA's IIP_3 (Input Third Order Intercept Point) must increase when gain decreases and decrease when gain increases to get constant OIP_3 (Output Third Order Intercept Point) and constant output power.

Noise figure is another important specification for the VGAs, especially RF VGAs. Generally, RF VGA comes after the LNA at a receiver. Noise figure of the systems can be given by Friis equation

$$NF = 10\log(F) \tag{2.29}$$

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... \tag{2.30}$$

where F_1,F_2 and F_3 are the noise figure of the first, second and third stage, respectively. G_1 and G_2 are the power gain of the first and second stage, respectively. From this equation, noise figure of the receiver can be roughly equal to LNA's noise figure plus that VGA's noise figure divided by LNA's gain if LNA's gain is high enough. As a conclusion, VGA's noise figure can be high when LNA's gain is high enough.

3. PROPOSED VGA

3.1 Introduction

The folded VGA structure in Figure 2.18 (b) has a linear-in magnitude (not in dB) gain by control voltage because the control circuit generates a current that is linear function of the control voltage. To get a linear-in dB gain characteristic with respect to the control voltage, an exponential current that is an exponential function of the control voltage is required for the input differential branches because the gain of the folded VGA structure in Figure 2.18 (b) is changed by difference of these two branch's transconductance. This difference is related to the tail current of the input differential branches, so an exponential gain characteristic can be get using an exponential tail current. The same result can be achieved from Equation (2.27). From Equation (2.27), if the control voltage has an exponential characteristic, a liner in dB gain characteristic is achieved. The same result can be obtained with an exponential transmission characteristic between two differential branches' currents and the control voltage. Taylor series approximation is used for the exponential current generation.

This structure has an advantage to get a constant bandwidth. The output node has the dominant pole and this node's capacitance and impedance are not dependent to the control voltage so the bandwidth is constant by the control voltage. The output resistance limits the bandwidth of this circuit. Using MOS-L structure instead of resistance can extend the bandwidth.

3.2 Block Diagram of the Proposed VGA Structure

The proposed VGA block diagram is shown in Figure 3.1. This circuit consists of a VGA core, post amplifiers and an exponential current generator as a control circuit.

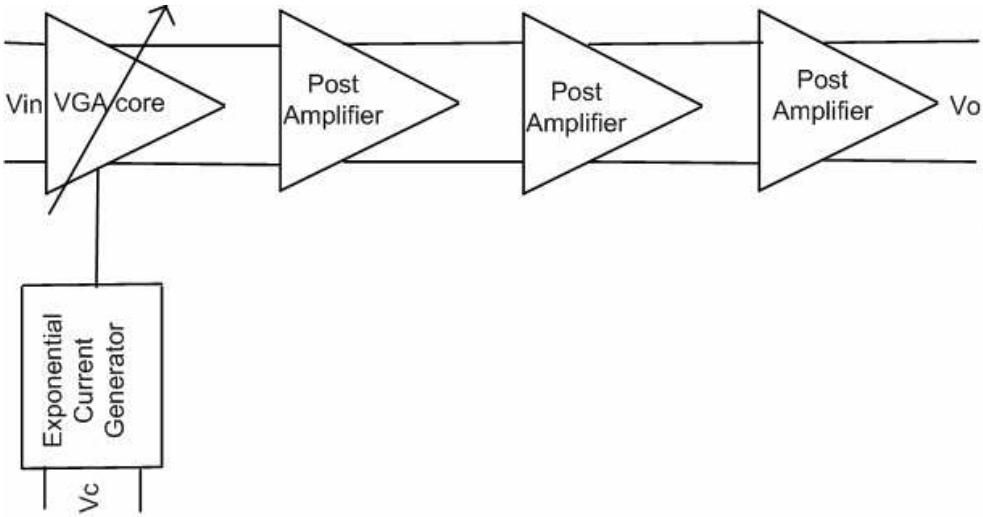

Figure 3.1: Block diagram of the proposed VGA structure

3.2.1 The Proposed VGA Core

Schematic of the VGA core is shown in Figure 3.2. This circuit's main core is the folded Gilbert cell. R_1 and M_{15} generate a constant bias current I_{ss}. And I_{exp} current comes from the exponential current generator. These two currents are used to control gain.

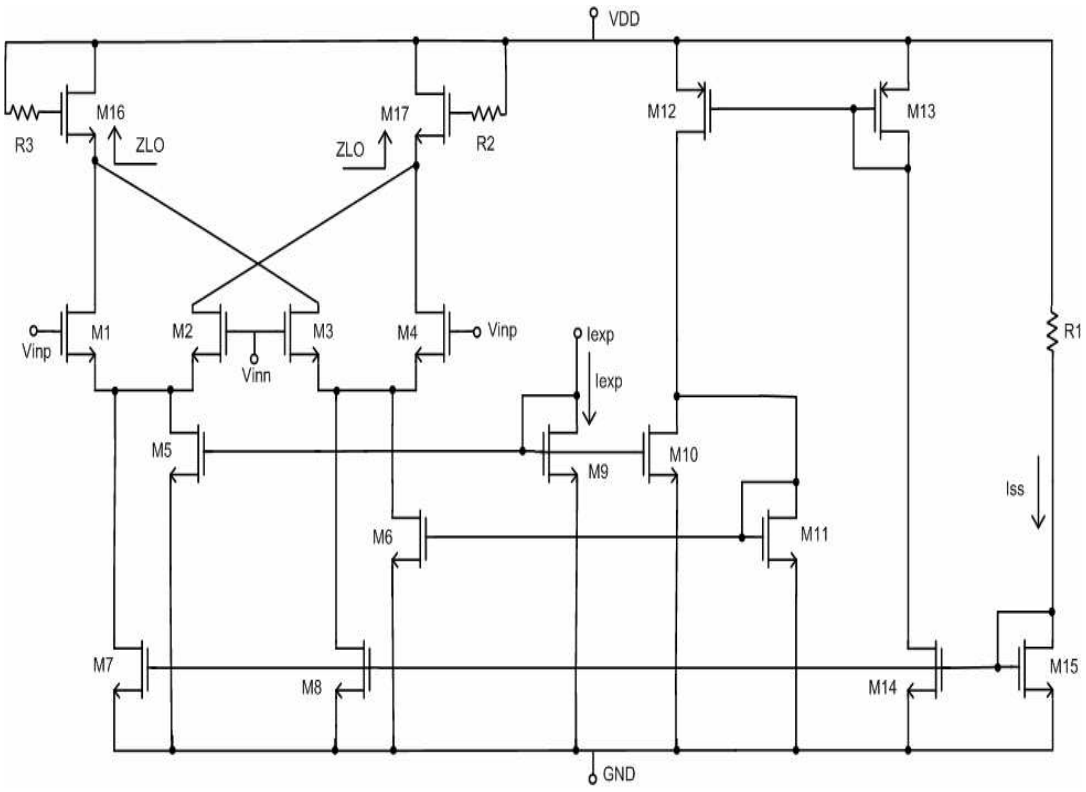

Figure 3.2: Schematic of the proposed VGA core

When sizes of the transistor M_{15} and M_{14} are equal, the drain current of bias transistor M_{15} is mirrored to the drain current of M_{14}. I_{ss}, drain current of M_{14} is mirrored to M_{12} using current mirror M_{13} and M_{12}. The drain current of M_{10} is equal to I_{exp} because of equal size of M_9 and M_{10}. The drain current of M_{11}, I_{D11}, can be given by

$$\begin{aligned} I_{D11} &= I_{D12} - I_{D10} \\ &= I_{ss} - I_{\exp} \end{aligned} \quad \textbf{(3.1)}$$

where, I_{D12} and I_{D10} are the drain current of M_{12} and M_{10}, respectively. This current is mirrored to M_6 with multiplication factor k_1. Thus, current flows through M_6 is given by

$$I_{D6} = k_1\left(I_{ss} - I_{\exp}\right) \quad \textbf{(3.2)}$$

And also, the drain current of M_9, I_{exp}, is mirrored to M_5 with multiplication factor k_1. The drain current of M_5 is given by

$$I_{D5} = k_1 I_{\exp} \quad \textbf{(3.3)}$$

Using current mirror transistor M_7 and M_8, constant I_{ss+} and I_{ss-} current are mirrored to first and second differential branches of the Gilbert cell with multiplication factor k_3 and k_2, respectively. The drain current of M_7 is given by

$$I_{D7} = I_{ss}^{+} = k_3 I_{ss} \quad \textbf{(3.4)}$$

And the drain current of M_8 is given by

$$I_{D8} = I_{ss}^{-} = k_2 I_{ss} \quad \textbf{(3.5)}$$

Using Equations (3.3) and (3.4), the drain current of the first input differential pair's transistors, M_1 and M_2, can be obtained as

$$I_{D1} = I_{D2} = I_{D5} + I_{D7} = \frac{k_1 I_{\exp} + k_3 I_{ss}}{2} \tag{3.6}$$

Using Equations (3.2) and (3.5), the drain current of the second input differential pair's transistors, M_3 and M_4, can be given by

$$I_{D3} = I_{D4} = I_{D6} + I_{D8} = \frac{k_1 \left(I_{ss} - I_{\exp}\right) + k_2 I_{ss}}{2} \tag{3.7}$$

Transconductance of M_1 and M_2 can be given by

$$g_{m1,2} = \sqrt{2\beta_{1,2} I_{D1,2}} = \sqrt{2\beta_{1,2} \frac{k_1 I_{\exp} + k_3 I_{ss}}{2}} \tag{3.8}$$

where $\beta_{1,2} = \mu C_{ox} W_{1,2} / L_{1,2}$. Transconductance of M_3 and M_4 can be given by

$$g_{m3,4} = \sqrt{2\beta_{3,4} I_{D3,4}} = \sqrt{2\beta_{3,4} \frac{k_1 \left(I_{ss} - I_{\exp}\right) + k_2 I_{ss}}{2}} \tag{3.9}$$

where $\beta_{3,4} = \mu C_{ox} W_{3,4} / L_{3,4}$. From Equations (3.8) and (3.9), when all input transistor's sizes are equal and $I_{\exp} = I_{ss}$, transconductance of the input transistors can be obtained as

$$g_{m1,2} = \sqrt{2\beta \frac{k_1 I_{ss} + k_3 I_{ss}}{2}} \tag{3.10}$$

$$g_{m3,4} = \sqrt{2\beta \frac{k_2 I_{ss}}{2}} \tag{3.11}$$

From Equations (3.8) and (3.9), when $I_{\exp} = 0$, transconductance of the input transistors can be obtained as

$$g_{m1,2} = \sqrt{2\beta \frac{k_3 I_{ss}}{2}} \tag{3.12}$$

$$g_{m3,4} = \sqrt{2\beta \frac{k_1 I_{ss} + k_2 I_{ss}}{2}} \quad \textbf{(3.13)}$$

To eliminate the polarity changes, $g_{m1,2} > g_{m3,4}$ in overall control range must be obtained. From Equations (3.10), (3.11), (3.12) and (3.13), following relations can be obtained.

$$k_3 > k_2 - k_1 \quad \textbf{(3.14)}$$

$$k_3 > k_1 + k_2 \quad \textbf{(3.15)}$$

Multiplication factors are positive and using Equations (3.14) and (3.15), Equation (3.16) is obtained.

$$k_3 > k_2 > k_1 \quad \textbf{(3.16)}$$

If multiplication factors are taken like in Equation (3.16), the polarity of the proposed VGA core's gain does not change.

From Equations (3.6) and (3.7), currents of the output load transistors can obtained as

$$I_{L1} = I_{L2} = I_{D1} + I_{D3} = I_{D2} + I_{D4} = \frac{(k_1 + k_2 + k_3) I_{ss}}{2} \quad \textbf{(3.17)}$$

In Equation (3.17), all parameters are constant with respect to the control voltage. Thus, the output node's impedance and capacitance are also not changed by the control voltage. In conclusion, the bandwidth of the proposed VGA core is constant.

Under the estimation of impedance seen from the drain of the input transistor is high enough, gain of the VGA core in Figure 3.2 can be calculated as

$$A_v \cong \frac{1}{2}[(g_{m1} - g_{m3}) - (g_{m4} - g_{m2})] Z_{LO} = (g_{m1,2} - g_{m3,4}) Z_{LO} \quad \textbf{(3.18)}$$

When the input transistors have equal sizes, from Equations (3.8), (3.9) and (3.18), gain can be calculated as

$$A_v \cong \left(\sqrt{2\beta I_{D1,2}} - \sqrt{2\beta I_{D3,4}}\right) Z_{LO}$$
$$= \left(\sqrt{2\beta \frac{k_1 I_{\exp} + k_3 I_{ss}}{2}} - \sqrt{2\beta \frac{k_1 \left(I_{ss} - I_{\exp}\right) + k_2 I_{ss}}{2}}\right) Z_{LO} \quad \textbf{(3.19)}$$

In Equation (3.19), β, I_{ss} and Z_{LO} are constant. From that, gain of the VGA core can be controlled using I_{exp} current. If this current has an exponential characteristic, gain characteristic can also be achieved like an exponential characteristic.

3.2.2 Exponential Current Generator

In CMOS technology, devices do not have an exponential characteristic. To obtain an exponential characteristic, an approximation method can be used. Taylor series approximation of an exponential function can be given by

$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \ldots\ldots + \frac{a^n}{n!}x^n + \ldots\ldots \quad \textbf{(3.20)}$$

where a and x are the coefficient and the independent variable, respectively. If |ax|<<1, exponential function can be approximated by

$$e^{ax} \cong 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \quad \textbf{(3.21)}$$

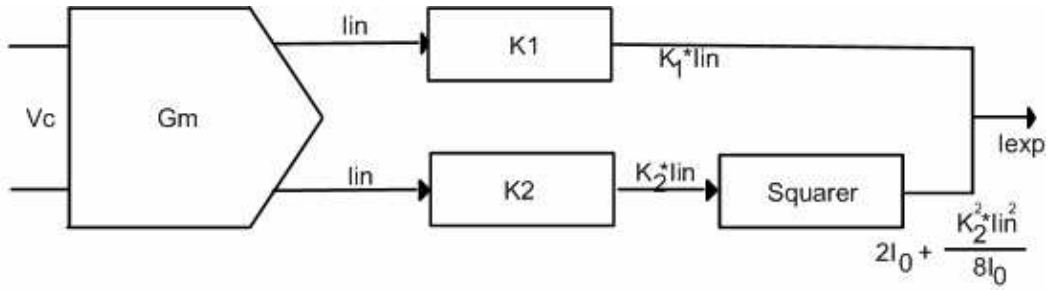

Figure 3.3: Exponential current generator block diagram [12]

The exponential current generator block diagram which realizes the Taylor's approximation is shown in Figure 3.3. A linear V-I converter and a current squarer

are used to synthesize the second-order polynomial [13]. In Figure 3.3, to get the two currents K_1I_{in} and K_2I_{in}, the output current (I_{in}) of linear V-I converter is multiplied by K_1 and K_2, respectively. K_2I_{in} signal is applied to the input of the current squarer, which has the transfer function as shown in Equation (3.42) and K_1I_{in} is added to the output of the current squarer to form output current like in Equation (3.21) [12].

The output current of the exponential current generator is expressed as [12]

$$\begin{aligned} I_{\exp} &= 2I_0 + K_1 I_{in} + \frac{K_2^2 I_{in}^2}{8I_0} \\ &= 2I_0\left(1 + K_1\frac{I_{in}}{2I_0} + \frac{K_2^2 I_{in}^2}{16I_0^2}\right) \end{aligned} \tag{3.22}$$

where I_0 is the bias current of the current squarer. To fulfill Taylor's approximation of the exponential function as in Equation (3.21), coefficient a and independent variable x have to satisfy the following condition [12]

$$\frac{a^2}{2!} = \frac{(K_1/2I_0)^2}{2!} = \frac{K_2^2}{16I_0^2} \tag{3.23}$$

Then

$$\frac{K_2}{K_1} = \sqrt{2} \qquad and \qquad a = \frac{K_1}{2I_0} \tag{3.24}$$

It can be seen from Equation (3.24), if multiplying factors K_1 and K_2 are set properly, the exponential characteristic can easily be obtained. K_1 and K_2 can be implemented easily because these are current mirrors' multiplying factor. Thus, the exponential characteristic depends only on process's parameters [12].

3.2.2.1 Linear V-I Converter

The principle of cross-coupling a matched MOS transistor pair with two identical dc floating-voltage sources as shown in Figure 3.4 can be used as the simplest and the most efficient way to implement a linear transconductor [14]. Drain currents of the MOS transistors in saturation region can be given by

$$I_D = \beta(V_{GS} - V_{TH})^2/2 \quad \textbf{(3.25)}$$

where, V_{GS} is the gate-to-source voltage, V_{TH} is the threshold voltage, and $\beta = \mu C_{ox} W/L$ is the transconductance. The unwanted V_{TH} term in Equation (3.25) can be eliminated by adding the two dc floating-voltage sources of value $V_X + V_{TH}$ as shown in Figure 3.4 [15].

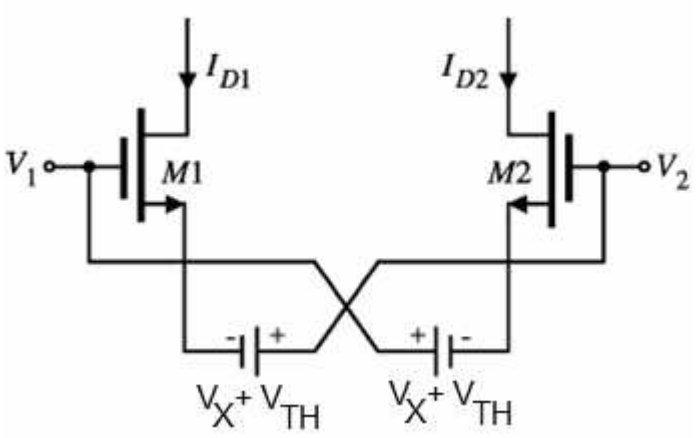

Figure 3.4: Linear transconductor and square-law function circuit principle [15]

The circuit in Figure 3.4 can be used to obtain a linear transconductor by subtracting the drain currents I_{D1} and I_{D2}. The gate source voltages of M_1 and M_2 in Figure 3.4 can be expressed as

$$\begin{aligned} V_{GS1} &= V_{id} + V_{TH} + V_X \\ V_{GS2} &= -V_{id} + V_{TH} + V_X \end{aligned} \quad \textbf{(3.26)}$$

where $V_{id} = V_1 - V_2$. Using Equation (3.25), the differential output current can be calculated as

$$I_{D1} - I_{D2} = \beta\left[(V_{GS1} - V_{TH})^2 - (V_{GS2} - V_{TH})^2\right] \quad \textbf{(3.27)}$$

From Equations (3.26) and (3.27), the V_{TH} terms cancel, resulting in

$$I_{D1} - I_{D2} = \beta\left[(V_{id} + V_X)^2 - (V_X - V_{id})^2\right] \quad \textbf{(3.28)}$$

This can be reduced to

$$I_{D1} - I_{D2} = 4\beta V_X V_{id} \quad \textbf{(3.29)}$$

which gives a linear transconductor [15].

In Figure 3.5, practical realization of the circuit in Figure 3.4 using flipped voltage followers is shown. The two flipped voltage followers are composed of transistors M_3, M_4 and M_5, M_6 and the dc current sources I_B. The flipped voltage follower employs shunt-shunt feedback and this result to very low impedance at the source of M_4. As a result, the gate-source voltages of M_4 and M_6 stay constant as V_1 and V_2 vary [15].

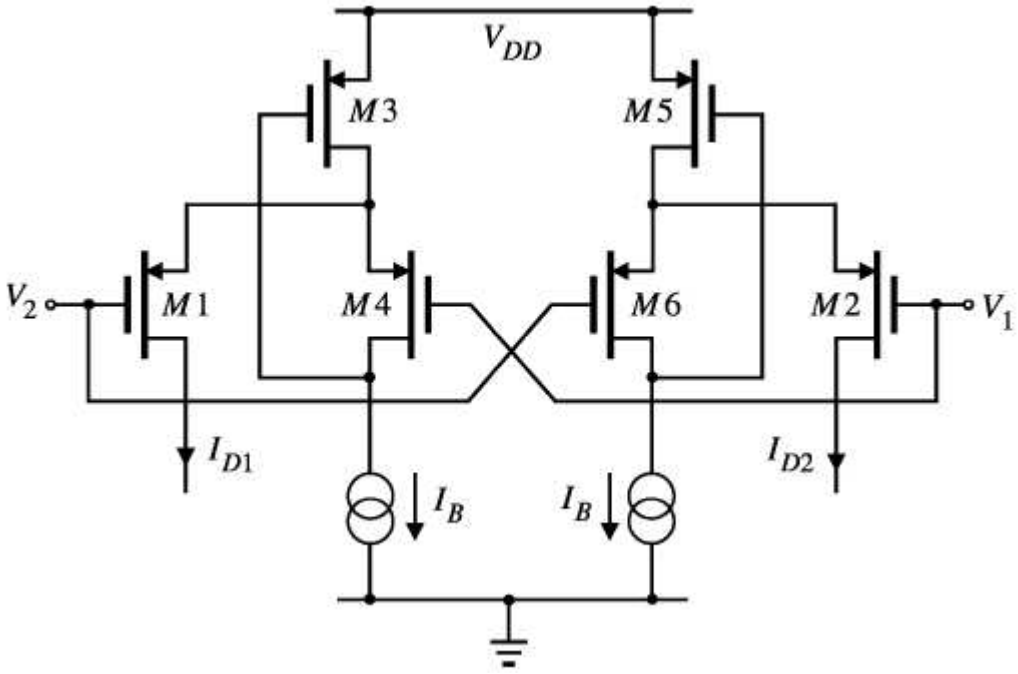

Figure 3.5: Practical realization of the circuit in Figure 3.4 using flipped voltage followers [15]

Under the condition that M_1, M_2, M_4 and M_6 in Figure 3.5 have the same size, the linear transconductance can be given by [15]

$$I_{D1} - I_{D2} = 4\sqrt{\beta I_B} V_{id}\ , \qquad |V_{id}| \le \sqrt{\frac{I_B}{\beta}} \tag{3.30}$$

Using the circuit in Figure 3.5, the linear V-I converter and the current multiplier for the exponential current generator in Figure 3.3 are shown in Figure 3.6. Resistor R_1 and transistors M_{15} and M_{16} are used to obtain bias current. The drain currents of transistors M_1 and M_5 are used to obtain linear transconductor. The difference of I_{o1} and I_{o2} is expressed as I_{in}. $K_2 I_{in}$ can be obtained easily by arranging the proportion of current mirror transistors' size (M_8, M_{10} and M_{11}, M_{12}) as K_2. And also, $K_1 I_{in}$ can be get easily by arranging the proportion of current mirror transistors' size (M_8, M_{14} and M_{11}, M_{13}) as K_1. Furthermore, K_1 and K_2 must be selected as in Equation (3.24).

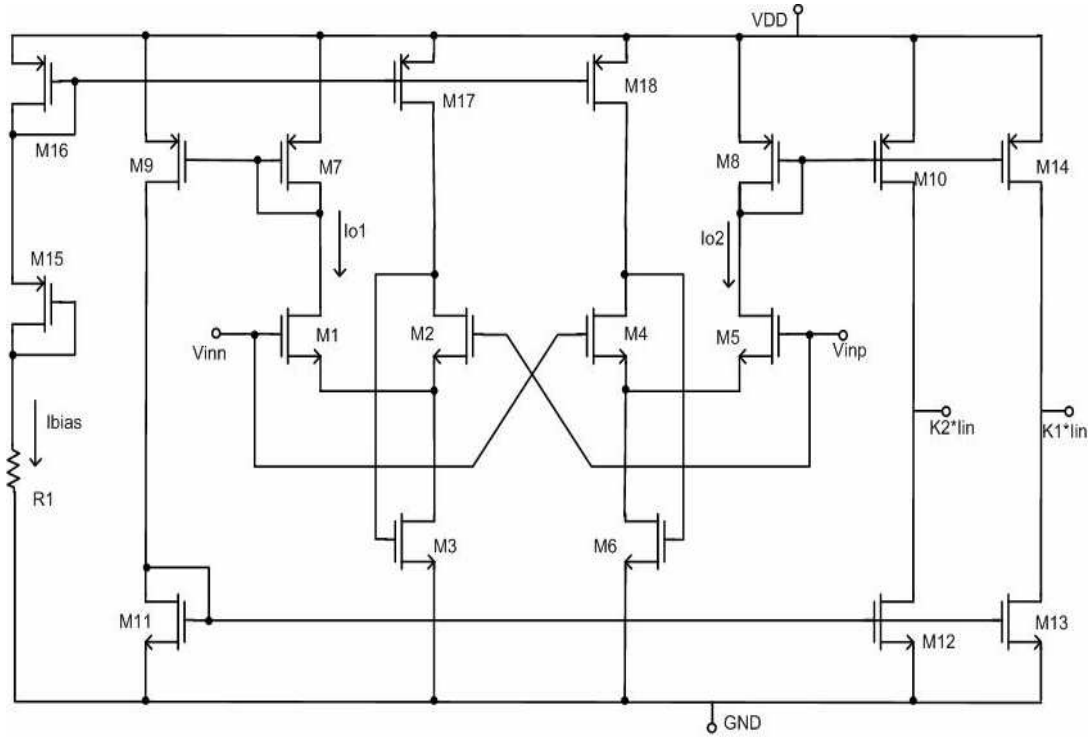

Figure 3.6: Linear V-I converter and current multiplier for exponential current generator in Figure 3.3

3.2.2.2 Current Squarer

The circuit in Figure 3.7 is composed of two identical MOS transistors M_1 and M_2. The gate-source voltages of M_1 and M_2 are equal to V_a and V_b, respectively. V_2, a constant voltage, is equal to sum of the gate-source voltages of M_1 and M_2. The drain currents of these transistors can be expressed as

$$I_1 = \beta(V_a - V_{TH})^2/2 \quad \textbf{(3.31)}$$

$$I_2 = \beta(V_b - V_{TH})^2/2 \quad \textbf{(3.32)}$$

and

$$V_b = V_2 - V_a \quad \textbf{(3.33)}$$

The difference of the drain currents can be calculated as [16]

$$I_1 - I_2 = \beta(V_2 - 2V_{TH})(V_a - V_b)/2 \quad \textbf{(3.34)}$$

The sum of the drain currents can be calculated as [16]

$$I_1 + I_2 = \frac{1}{4}\beta(V_2 - 2V_{TH})^2 + \frac{(I_1 - I_2)^2}{\beta(V_2 - 2V_{TH})^2} \quad \textbf{(3.35)}$$

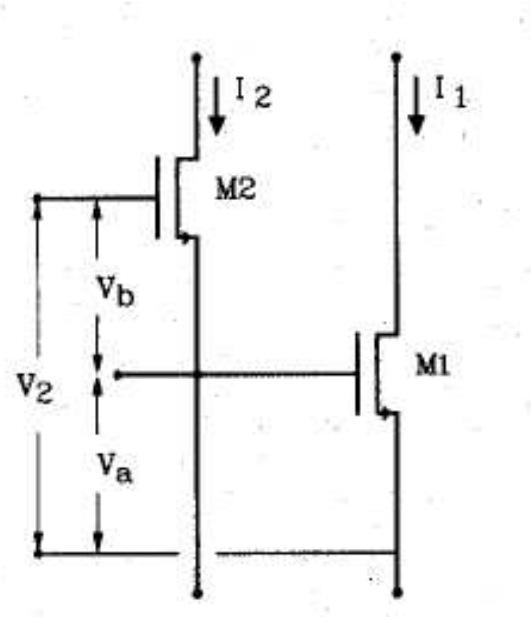

Figure 3.7: The basic two-transistor circuit of current squarer [16]

A current controlled biasing circuit is shown in Figure 3.8, this circuit supplies the sum voltage V_2. The relation between the control current I_0 and the voltage V_2 can be expressed as

$$I_0 = \frac{1}{4}\beta(V_2 - 2V_{TH})^2 \quad \textbf{(3.36)}$$

under the condition $V_2 > 2V_{TH}$ [16].

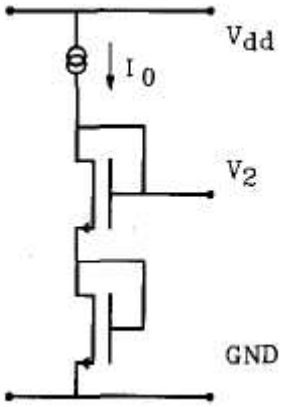

Figure 3.8: The biasing circuit of current squarer [16]

The linear I-V converter, which is obtained by connecting the drain of M_1 in Figure 3.7 to its gate, is shown in Figure 3.9. The output voltage V_{out}, which is equal to V_a, is obtained from the input current I_{in} flowing in to the circuit [16]. Using Equations (3.32)-(3.34), the input current can be calculated as

$$I_{in} = I_1 - I_2 \quad \textbf{(3.37)}$$

and the output voltage as

$$V_{out} = V_a \quad \textbf{(3.38)}$$

The input current can be calculated as

$$I_{in} = 2\beta(V_2 - 2V_{TH})(V_{out} - V_2/2) \quad \textbf{(3.39)}$$

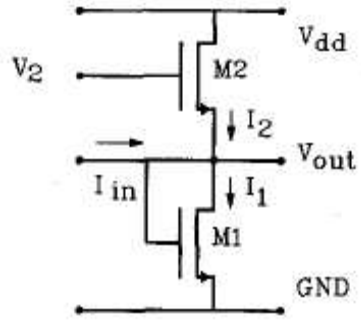

Figure 3.9: The linear I-V converter [16]

The current squaring circuit can be obtained by mirroring of I_1 via transistor M_3 and adding it to current I_2 as shown in Figure 3.10. The output current can be given by

$$I_{out} = I_1 + I_2 \tag{3.40}$$

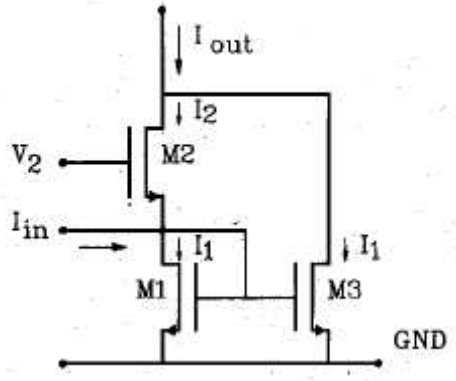

Figure 3.10: The current-squaring circuit [16]

Using Equations (3.37) and (3.40) into Equation (3.35) results [16]

$$I_{out} = \frac{1}{4}\beta(V_2 - 2V_{TH})^2 + \frac{I_{in}^2}{\beta(V_2 - 2V_{TH})^2} \tag{3.41}$$

which gives a current squaring function. Using bias circuit of Figure 3.8 and Equation (3.36) into Equation (3.41), a simple expression is expressed as

$$I_{out} = 2I_0 + \frac{I_{in}^2}{8I_0} \tag{3.42}$$

In order to keep all transistors in the ON state, the input current must be hold in the range

$$|I_{in}| < 4I_0 \quad \textbf{(3.43)}$$

The overall current squarer is shown in Figure 3.11. Resistor R_1, transistor M_1 and M_2 are used to obtain bias current I_0. The output current is mirrored via transistor M_{11} as I_{out} current.

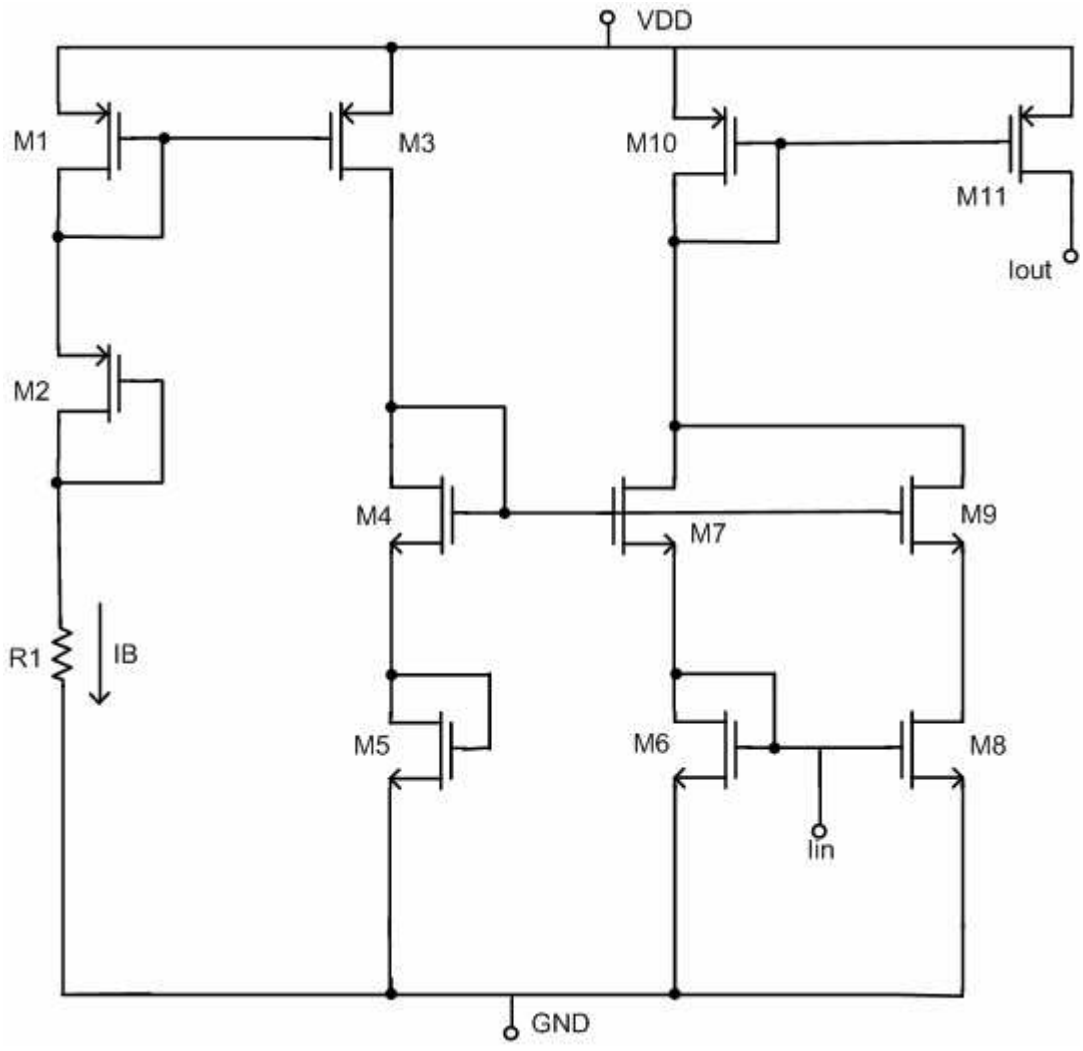

Figure 3.11: The overall current-squaring circuit

The complete schematic of the exponential current generator circuit in Figure 3.1 is shown in Figure 3.12. This circuit generates the I_{exp} current of the VGA core circuit in Figure 3.2.

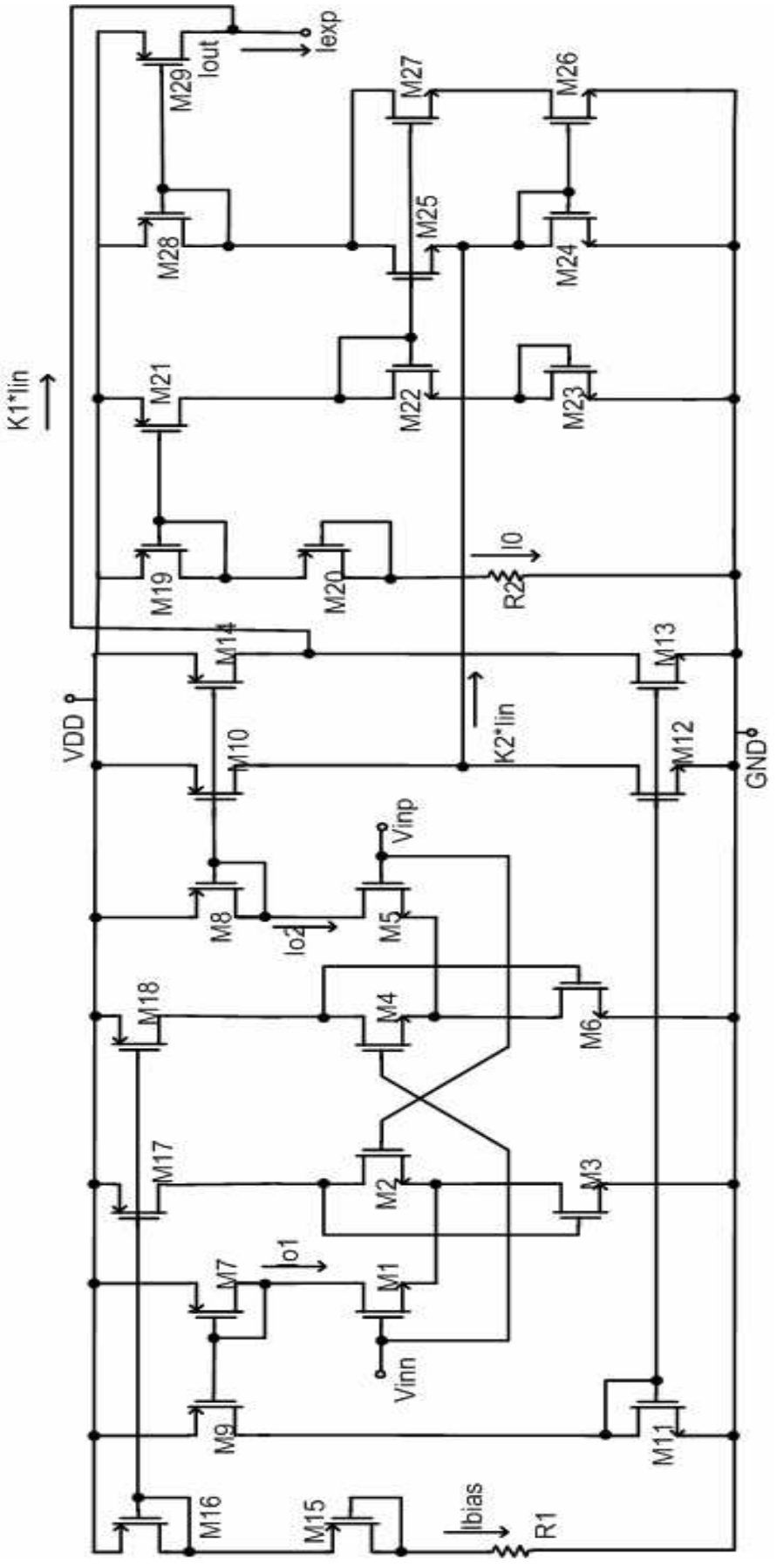

Figure 3.12: The exponential current generator circuit

3.2.3 Post Amplifiers

Post amplifier circuit is shown in Figure 3.13. This circuit as a classical differential amplifier with MOS-L load for the bandwidth extension. Post amplifiers are required to increase the gain of the overall VGA circuit.

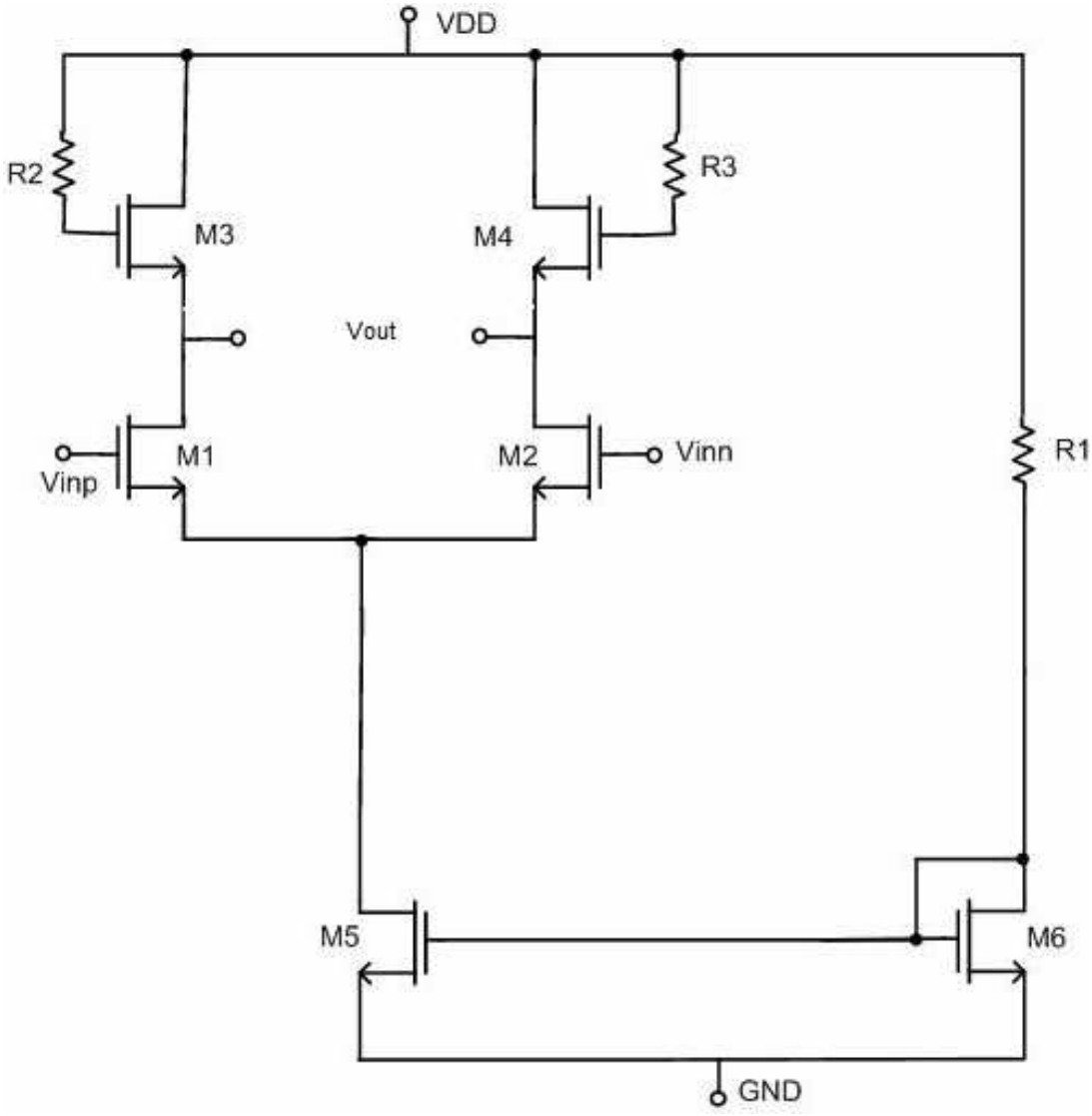

Figure 3.13: Post amplifier circuit

3.2.4 Bandwidth Extension Load

The small signal model of the load impedance in Figure 3.2 is shown in Figure 3.14. To evaluate the impedance Z_{LO}, a test voltage, v_x, is applied to this node. The load impedance can be given by

$$Z_{LO} = \frac{v_x}{i_x} \tag{3.44}$$

The current i_R can be expressed as

$$i_R = \frac{v_{gs} + v_x}{R} \tag{3.45}$$

The current i_R can be given by

$$i_{Cgs} = sC_{gs}v_{gs} = -i_R = -\frac{v_{gs} + v_x}{R} \tag{3.46}$$

Under the condition r_o is high enough to neglect, following expression can be written as

$$i_{Cgs} + g_m v_{gs} + i_x = 0 \tag{3.47}$$

Using Equations (3.45) and (3.46) into Equation (3.47), load impedance can be calculated as

$$Z_{LO} = \frac{sC_{gs}R + 1}{sC_{gs} + g_m} \tag{3.48}$$

This equation has a zero at the frequency $1/2\pi RC_{gs}$.

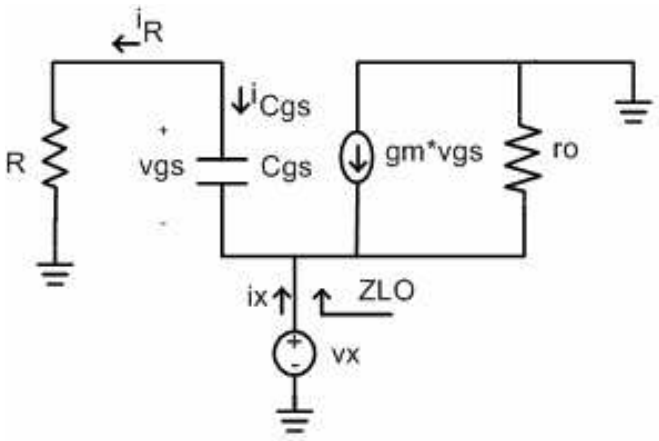

Figure 3.14: The small signal model of the bandwidth extension load

4. SIMULATION RESULTS

This chapter includes schematic simulation results of the proposed VGA. The proposed VGA is designed in UMC 0.13µm CMOS process. Supply voltage of the proposed VGA is 1.2V and the overall power dissipation of the circuit is 16mW. The power dissipations of the proposed VGA's blocks are shown in Table 4.1.

Table 4.1: The power dissipations of the proposed VGA's blocks

	Linear V-I Converter	**Current Squarer**	**VGA Core**	**Post Amplifiers**
Power Dissipation	0.6mW	0.36mW	7.2mW	7.9mW

The output currents of the linear V-I converter in Figure 3.6 with multiplication factors K_1 and K_2 are shown in Figure 4.1. The bias current of this circuit, I_{bias}, is

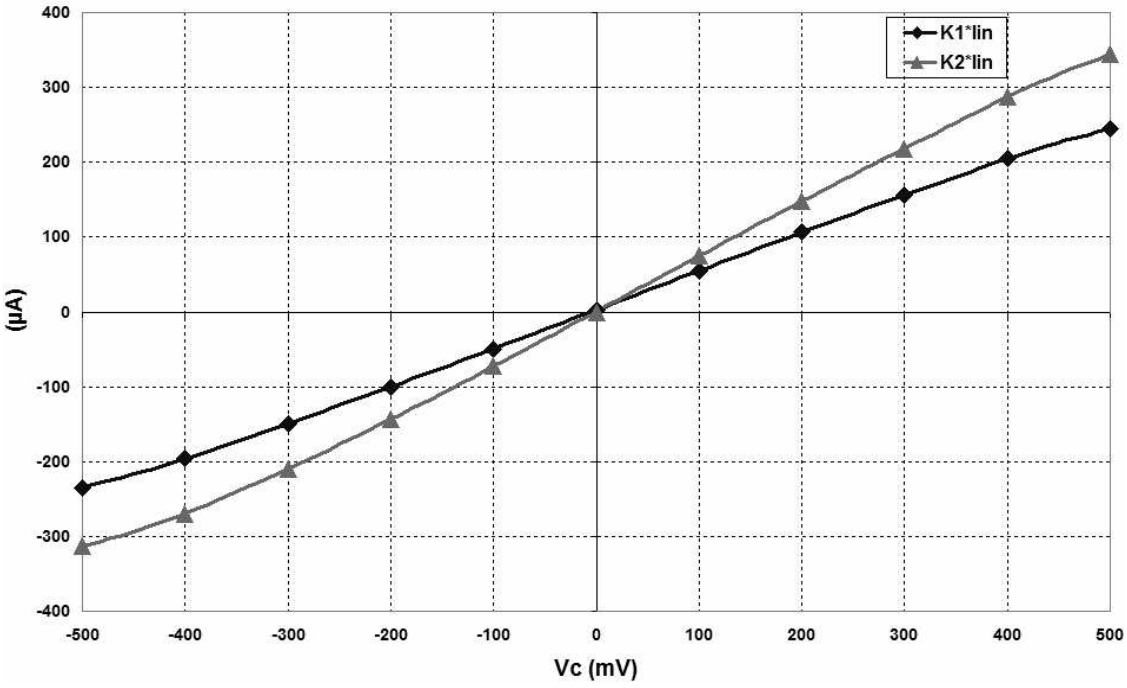

Figure 4.1: The output current of linear V-I converter circuit vs. V_C

100µA. To obtain the exponential characteristic from the Taylor series approximation properly, the proportion of the multiplication factor K_1 and K_2 is designed like in Equation (3.24). As seen in Figure 4.1, the linear V-I converter works properly within a wide range of the control voltage, V_C. A little difference occurs from the ideal characteristic at the end of the control voltage range.

The output current of the current squarer circuit in Figure 3.11 is shown in Figure 4.2. The bias current of this circuit, I_0, is 50µA. The relation between the input current and the bias current should satisfy the condition in Equation (3.43) for proper operation of this circuit. The input current of this circuit is K_2I_{in}. As seen in Figure 4.1, absolute value of K_2I_{in} is lower than 200 µA in -280 mV to 280 mV range of the control voltage. Thus, valuable current squaring operation is obtained in this control voltage range.

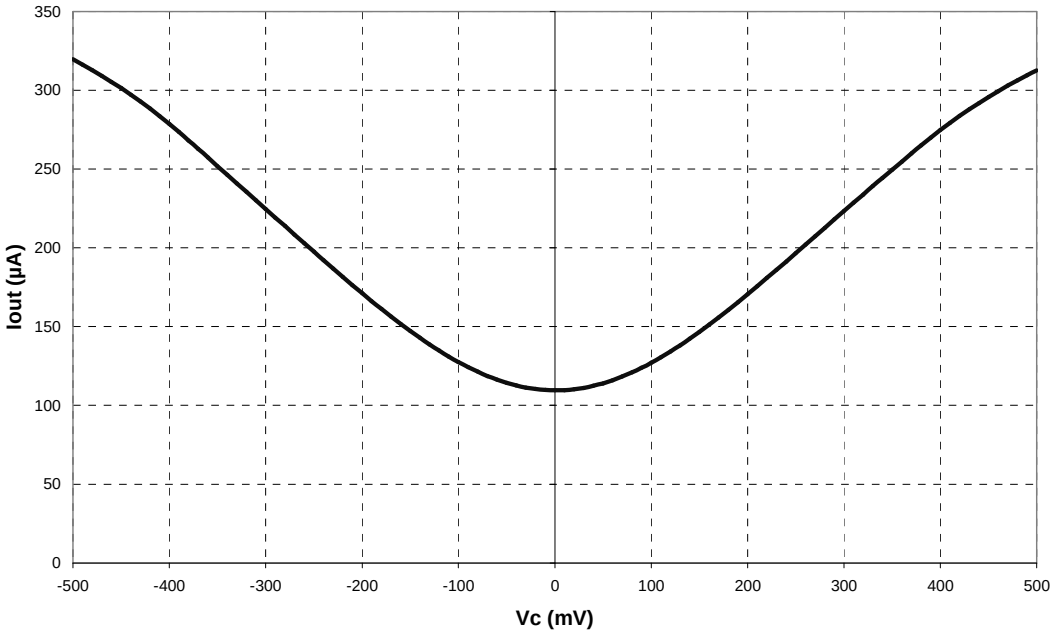

Figure 4.2: The output current of the current squarer circuit vs. V_C

Figure 4.3 shows the output current of the exponential current generator circuit, I_{exp}. As seen in this figure, a current that has the exponential characteristic is obtained with respect to the control voltage.

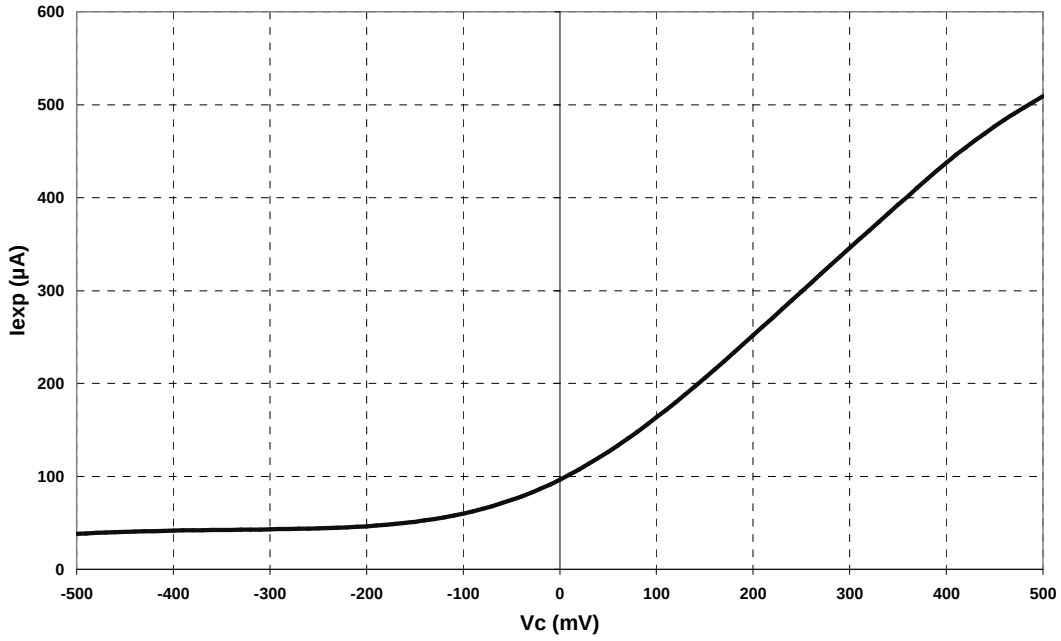

Figure 4.3: The output current of the exponential current generator vs. V_C

The normalized output current of the exponential current generator in logarithmic scale is shown in Figure 4.4. 22 dB normalized output current range was achieved.

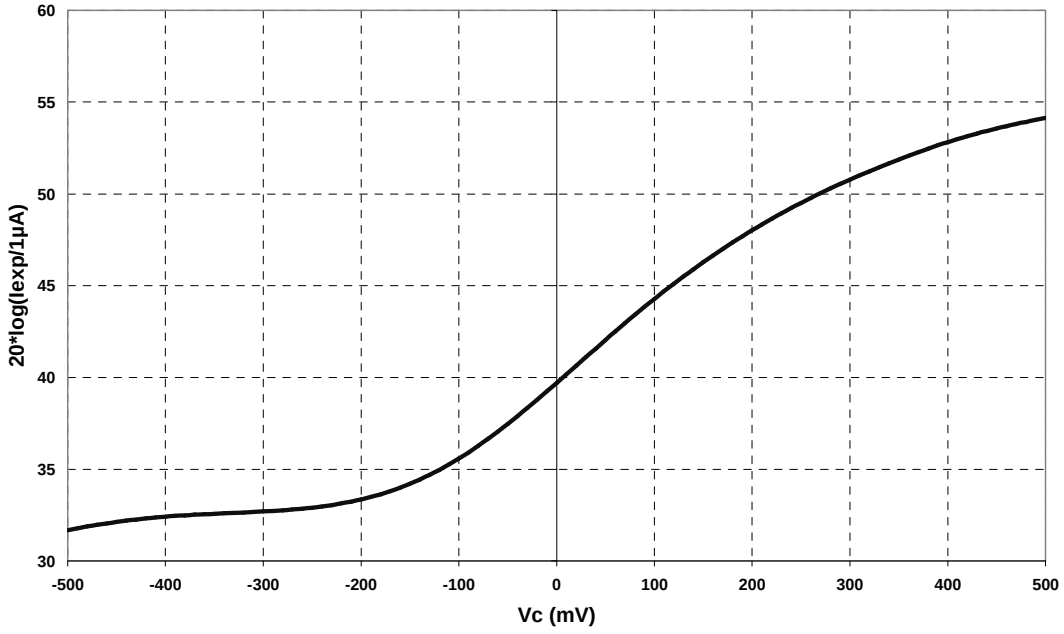

Figure 4.4: The normalized output current of the exponential current generator vs. V_C in logarithmic scale

The small signal gain of the proposed VGA versus the control voltage is shown in Figure 4.5. As shown in this figure, 27 dB gain control range was achieved. 21 dB-linear of this range is achieved with error less than ± 1.5 dB over the range of V_C from -200mV to 200mV.

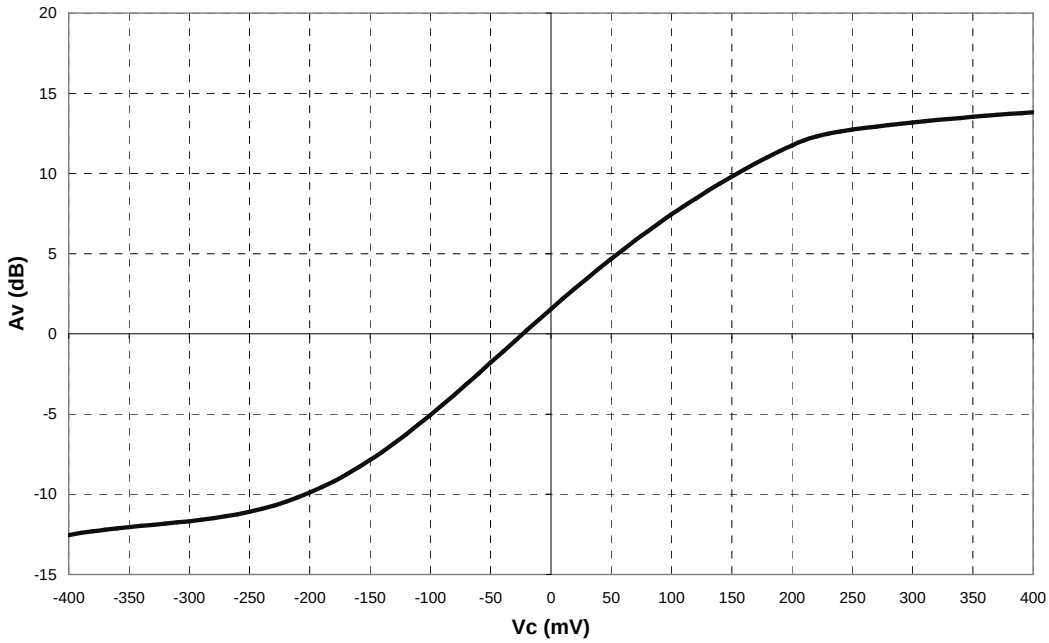

Figure 4.5: Small Signal Gain of the VGA vs. V_C

The small signal gain of the proposed VGA versus frequency versus the control

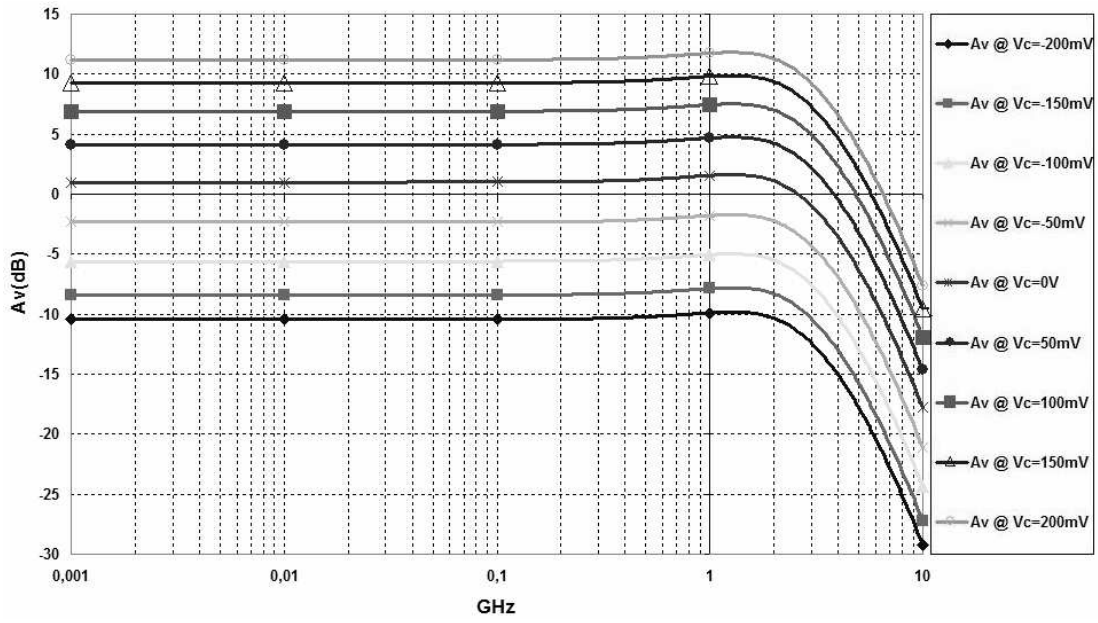

Figure 4.6: Small Signal Gain of the VGA vs. Frquency vs. V_C

voltage is shown in Figure 4.6. 3-dB bandwidth frequency of the proposed VGA is about 3 GHz. 3-dB bandwidth frequency is nearly constant with respect to the control voltage as shown in this figure.

S-parameter analyses of the proposed VGA are done with differential 150 ohm input port resistance and differential 300 ohm output port resistance. The input and output impedance can be determined and redesigned when different values are needed for the requirements of the system's blocks.

Power gain (S_{21}), input return losses (S_{11}) and output return losses (S_{22}) are shown in Figure 4.7 when the control voltage is 200mV. A resistance at the differential input is used to obtain input matching. When frequency increases, input return losses goes to zero because of input transistors parasitic capacitances. When the control voltage is 200mV, S_{21} is 9.3 dB. 3-dB bandwidth frequency is 3 GHz. The input return losses is 6 dB and the output return losses is 11 dB at 3 GHz. A peaking at the gain occurs at 1 GHz because of MOS-L structure and this increases the 3-dB bandwidth frequency to 3 GHz.

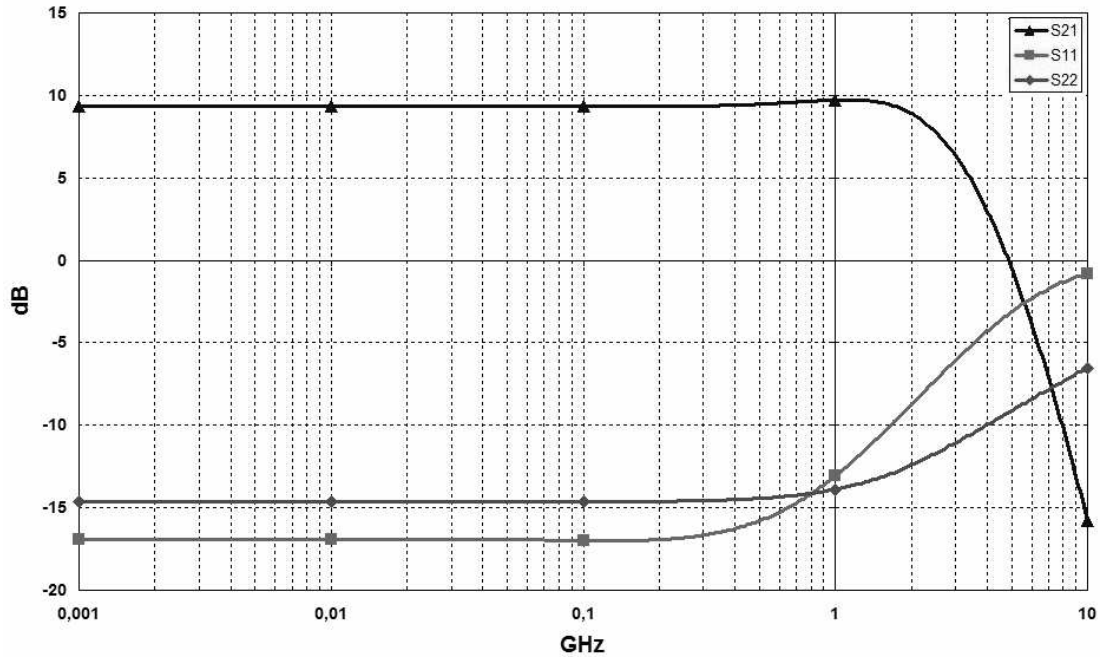

Figure 4.7: S-Parameters of the VGA @ V_C = 200mV

Figure 4.8 shows the S_{21}, S_{11} and S_{22} of the proposed VGA when the control voltage is 0V. Gain is -1 dB at this control voltage. On the other hand, the return losses of the proposed VGA do not change.

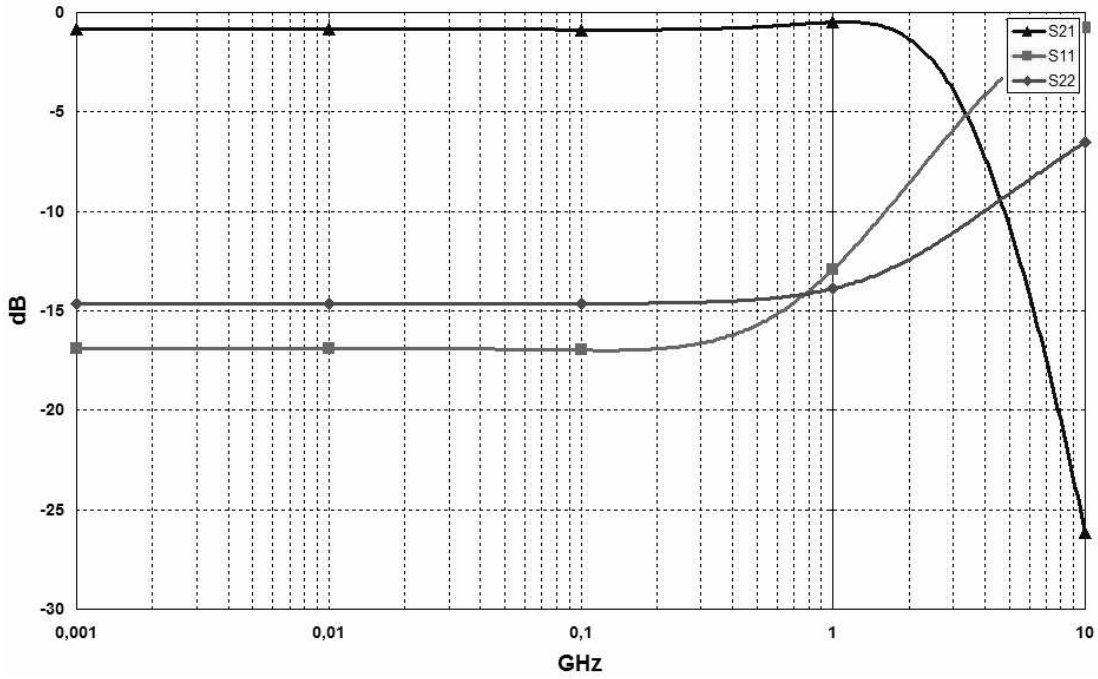

Figure 4.8: S-Parameters of the VGA @ $V_C = 0$ V

Figure 4.9 shows the S_{21}, S_{11} and S_{22} of the proposed VGA when the control voltage is -200 mV. Gain is -12.3 dB at this control voltage.

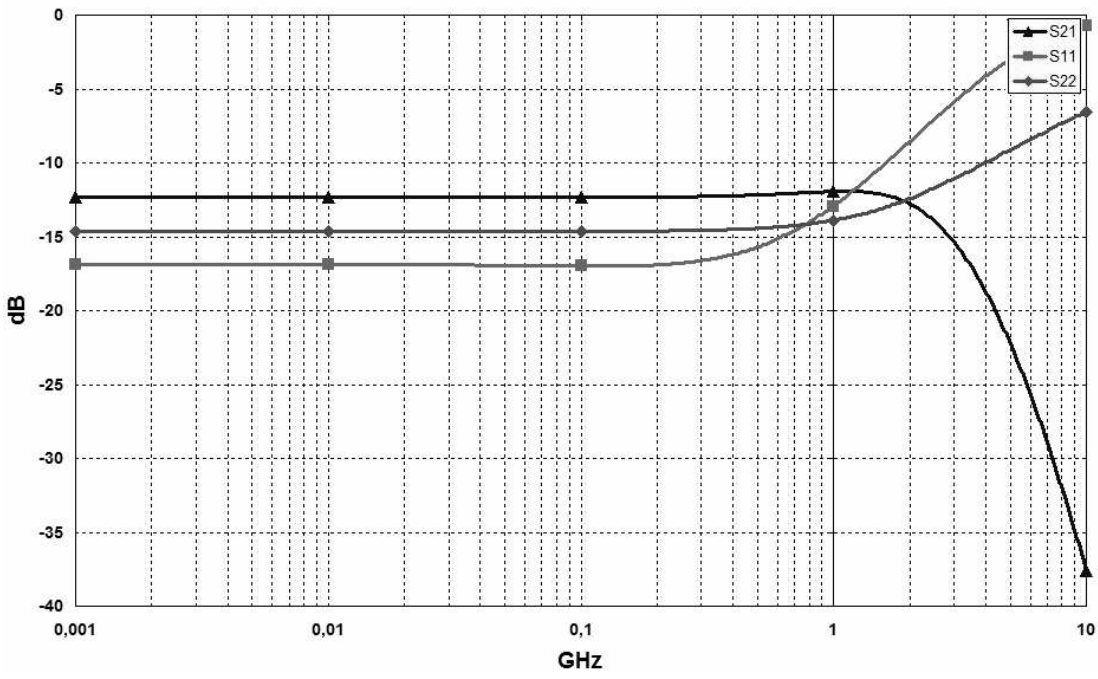

Figure 4.9: S-Parameters of the VGA @ $V_C = -200$mV

Noise figure of the circuit is shown in Figure 4.10 at maximum gain condition. Noise figure is below 15 dB over the frequency range from 1 GHz to 3 GHz.

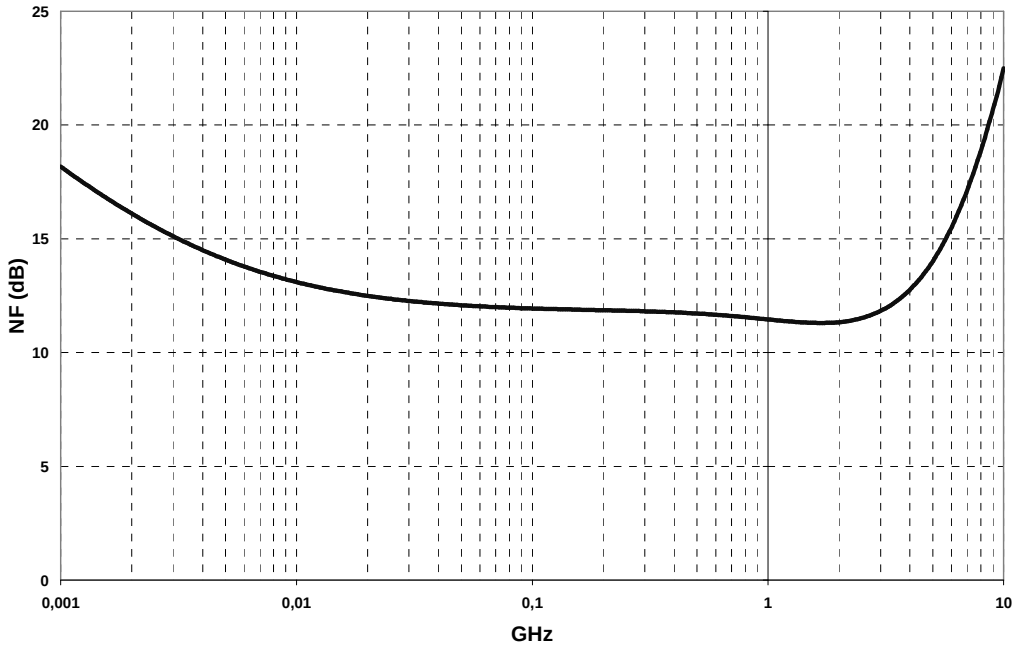

Figure 4.10: NF of the VGA at maximum gain condition

In general, LNA, VGA and mixer comes respectively in a receiver system. A receiver example with noise figure and gain is shown in Figure 4.11. Using Equations (2.29) and (2.30), the noise figure of the example receiver can be calculated as 5.5 dB. From this result, if the gain of LNA is high, increasing on noise figure of the system is not high because of the VGA. This noise figure result is enough for Bluetooth and several tuner IC systems.

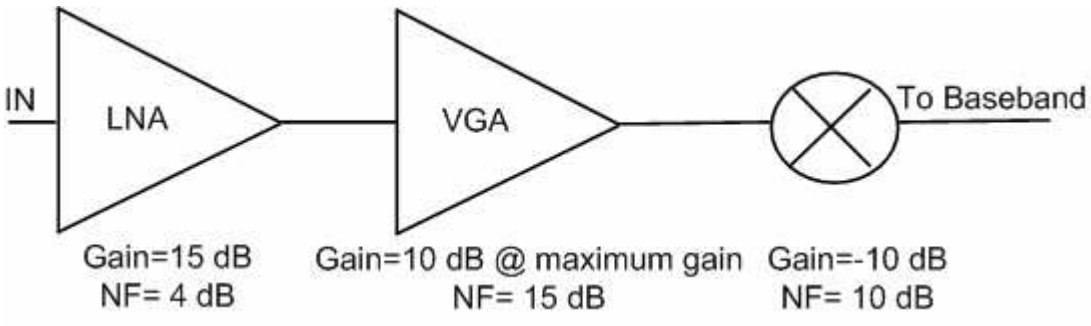

Figure 4.11: An example receiver with gain and NF values of the blocks

Figure 4.12 shows the input and output transient signal of the proposed VGA with 1% THD (Total Harmonic Distortion) when the control voltage is equal to 0V. In general, the input signal range of a receiver has a range from -70 dBm to -20 dBm. -20 dBm means 32 mV sine wave signal in the 50 ohm system.

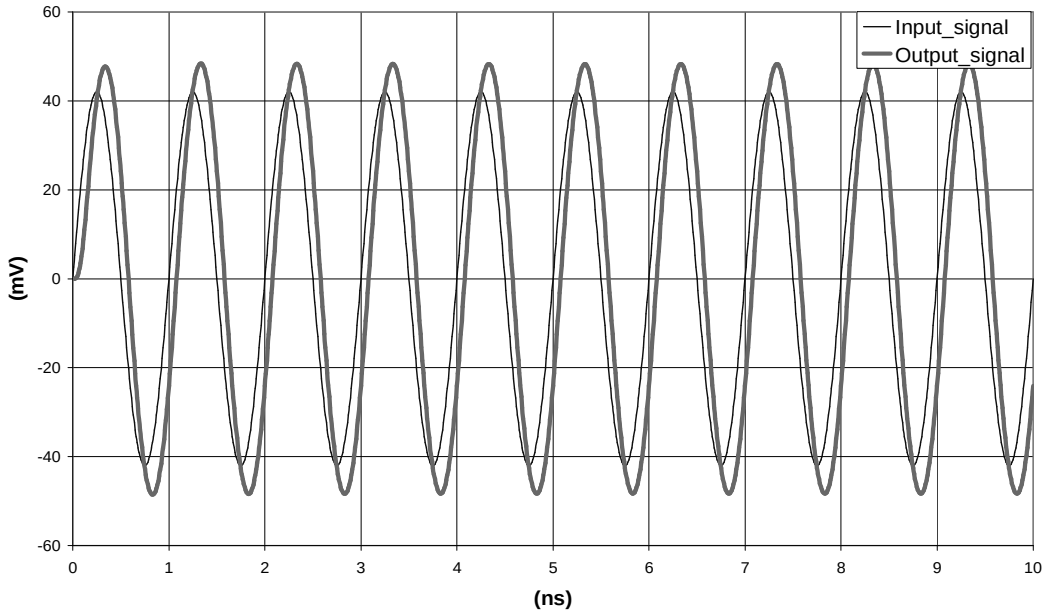

Figure 4.12: Input and output transient signal of the proposed VGA with 1% THD

In Table 4.2, the simulation results of the proposed VGA are presented at three different control voltages. Gain has 21 dB in linear range, and 3-dB bandwidth frequency is constant over the control range. IP_{1dB} is -8 dB at minimum gain setting and -28 dB at maximum gain setting. IIP_3 has a range of -5 dBm to -19 dBm. These mean that the proposed VGA is a functional block as a VGA because IP_{1dB} and IIP_3 increase when gain decreases.

Table 4.2: The simulation results of the proposed VGA

	V_C = -200 mV	**V_C = 0 V**	**V_C = 200 mV**
S_{21} (dB)	-12.3	-1	9.3
f_{3dB} (GHz)	3	3	3
A_v (dB)	-10.5	1	11.2
IP_{1dB} (dBm)	-8	-17	-28
IIP_3 (dBm)	-5	-11	-19

Performance comparison with other CMOS VGAs in the literature is shown in Table 4.3. 3-dB bandwidth frequency of the proposed VGA is better than other VGAs in

Table 4.3: Comparison of CMOS VGA performance

	This Work	**[3]**	**[6]**	**[4]**	**[1]**	**[8]**
Technology	0.13µm CMOS	0.18µm CMOS	0.13µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS
Supply Voltage (V)	1.2	1.8	1.8	1.8	1.8	1.8
Power Consumption (mW)	16	6.48	8.1	23.04	20.52	40
Gain range (dB)	-10.5 ~ 11.2	-48 ~ 36	-34 ~ 20	-24.9 ~ 48.6	-39 ~ 55	-16 ~ 34 (linear in magnitude)
f_{3dB} (GHz)	3 GHz	1 to 0.04	0.743	0.95	0.9 to 0.004	2
NF (dB) at maximum gain	< 15	n. a	n. a	n. a	6.8	n. a
IP_{1dB} (dBm) at minimum gain	-8	-22	n. a	16.4	-11	n. a
IIP_3 (dBm) at minimum gain	-5	n. a.	n. a	n. a	n. a	n. a

the literature. And also 3-dB bandwidth frequency is constant with respect to the control voltage. As seen in Table 4.3, 3-dB frequencies of some VGAs are different at different gain settings. The gain range of the proposed VGA is low, but it can be increased with using two VGA core as cascade but bandwidth decreases. IP_{1dB} of the proposed VGA is good enough when it is compared to IP_{1dB} of the other VGAs.

5. CONCLUSION

The aim of this thesis is to review the theory and topologies of CMOS VGA in literature, and design a CMOS VGA. Linear in dB gain characteristic, wide tuning range, wide and constant bandwidth, IIP_3, IP_{1dB} and NF are the most important specifications of the VGA.

The 3-dB bandwidths of CMOS VGA topologies in literature are not constant with respect to the control voltage. And also, they do not have wide bandwidth. To obtain constant 3-dB bandwidth characteristic, the folded Gilbert cell is used as the VGA core. MOS-L structure is used to increase 3-dB bandwidth. To get linear-in-dB gain characteristic in CMOS technology, pseudo exponential or Taylor series approximation methods are used in literature. In this design, an exponential current generator circuit is designed by using Taylor series approximation method. VGA core of the proposed VGA is folded Gilbert cell, so maximum gain of this core is not high. Therefore, three post amplifiers are used to increase gain.

The proposed VGA is designed using Spectre circuit simulator and UMC 0.13µm CMOS process. 21 dB in linear gain range and 3 GHz constant 3-dB bandwidth are obtained. IP_{1dB} and IIP_3 are obtained as -8 dBm and -5 dBm at minimum gain setting, respectively. As expected, IP_{1dB} and IIP_3 decrease when gain increases.

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