ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

DESIGN OF VARIOUS VCO TOPOLOGIES AND PERFORMANCE COMPARISON AT 2.4 GHz

M.Sc. THESIS

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

FARKLI YAPILARDA VCO TASARIMLARI VE 2.4 GHz'DE PERFORMANS KARŞILAŞTIRMASI

YÜKSEK LİSANS TEZİ

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OCAK 2013

Mehmet BATI, a **M.Sc.** student of ITU **Graduate School of Science Engineering and Technology** student ID 504091249, successfully defended the **thesis** entitled "**DESIGN OF VARIOUS VCO TOPOLOGIES AND PERFORMANCE COMPARISON AT 2.4 GHz**" which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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FOREWORD

I would like to thank my advisor, Assoc. Prof. Dr. Nil TARIM for giving me the opportunity to conduct this research. I would also like to thank my family and friends for their endless support.

January 2013 Mehmet BATI

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ABBREVIATIONS

VCO	**:** Voltage Controlled Oscillator
BPF	**:** Band Pass Filter
PVT	**:** Process Voltage Temperature
Wi-Fi	**:** Wireless Fidelity
LO	**:** Local Oscillator
RF	**:** Radio Frequency
IF	**:** Intermediate Frequency
OPAMP	**:** Operational Amplifier
OTA	**:** Operational Transconductance Amplifier
LOFT	**:** Local Oscillator Feedthrough
SBR	**:** Sideband Rejection

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DESIGN OF VARIOUS VCO TOPOLOGIES AND PERFORMANCE COMPARISON AT 2.4 GHz

SUMMARY

RF transceiver architecture design is critical in the realization of monolithic chip solutions. Low noise and low power designs are necessary for high performance wireless transceivers. Voltage controlled oscillators are among the key building block for the RF communication systems. They are used as local oscillator in up and down converters. Therefore, the performance of voltage controlled oscillator is important to determine overall performance of the transceiver.

Power consumption, phase noise and tuning range are some important design parameters for voltage controlled oscillators. There are many different circuit structures to improve these parameters. However, many of these structures require on-chip inductors. There are several downsides to use IC inductors in design such as high cost and difficult to accurate design.

It is also possible to design an oscillator without using inductors. One of them implements inductor using active circuits. However, noise performance is very poor for these structures. Another approach is ring oscillator topology. Although, it is still worse phase noise performance compared to LC oscillators, they are used in RF systems because of their high tuning range and easy integration. Another oscillator topology without IC inductor is Wien-bridge structure. This topology is based on band-pass filter structure. An operational amplifier is used there to provide stable oscillation. However, this structure isn't suitable for high frequency oscillations because it is limited by operational amplifiers gain-bandwidth product. If an operational transconductance amplifier is used, this structure can also provide high frequency operation. Relaxation oscillators are another alternative to LC oscillators. These kinds of oscillators operate by alternately charging and discharging a capacitor between two threshold voltage levels.

In this thesis, four different voltage controlled oscillator structures are designed in the same 2.4 GHz oscillation frequency. 2.4 GHz is one of the most popular frequency band that is used in Bluetooth, cordless telephones, car alarms and Wi-Fi networks. 0.18μm process and 1.8V supply voltage is used in all designs to compare fairly each other.

The design with LC structure has best phase noise performance (-120 dBc/Hz @ 1MHz) as expected. However, relaxation oscillator topology provides also good phase noise performance especially using quadrature structure (-108 dBc/Hz @ 1MHz). Some applications in RF communication systems such as image rejection mixer topologies require quadrature local oscillators and it is very critical to have signals with 90^0 phase shift to reject image band accurately. Quadrature relaxation oscillators can be alternative to LC oscillators for these applications because LC oscillator phase noise performance decreases in quadrature structure. Ring oscillator and RC BPF based oscillator structures are also analyzed and designed in this work. The phase noise performances are obtained about 95.8 dBc/Hz @ 1 MHz for RC BPF based topology and 97 dBc/Hz @ 1 MHz for ring topology. Their phase noise performances are worse than others but they have also some advantages such as high tuning range, easy design and implementation.

Each design is compared with similar structures in literature at the end of chapters. The best alternative without using on-chip inductor is the quadrature relaxation oscillator structure. Quadrature up conversion mixer is designed as an application for quadrature relaxation oscillator. It is used there as local oscillator. Obtained results are satisfying that quadrature relaxation oscillator can be used effectively in image reject up and down conversion systems.

At the end of thesis, these four structures are compared and discussed in detail. Their advantages and disadvantages are manifested according to each other.

FARKLI YAPILARDA VCO TASARIMLARIVE 2.4 GHz'DE PERFORMANS KARŞILAŞTIRMASI

ÖZET

Gelişen teknoloji ile birlikte, yüksek frekans haberleşme sistemlerinin entegrasyonu daha da önem kazanmıştır. Artık tüm alıcı ya da verici yapısı tek bir entegre ile gerçeklenmeye başlanmıştır. Tasarlanan bu karmaşık entegre devrelerin aynı zamanda düşük gürültülü ve harcadığı enerjinin de az olması beklenmektedir. Gerilim kontrollü osilatör devreleri, bu karmaşık entegre blokların performansını etkileyen önemli bloklardan biridir. Bunlar alıcı ve verici sistemlerde çarpıcı işaret olarak kullanılırlar.

Güç tüketimi, çalışma frekans aralığı, faz gürültüsü gibi özellikler gerilim kontrollü osilatörler için başlıca tasarım parametreleridir. Bu parametreleri iyileştirme açısından bir çok çeşit devre yapıları mevcuttur. Fakat bunların birçoğu entegre endüktans kullanımını gerektirmektedir. Bu durum da maliyeti artırmakta ve endüktansın modellenmesi zor olduğundan güvenilirliği azaltmaktadır.

Entegre endüktans kullanmadan da yüksek frekans osilatör tasarımı mümkündür. Bu konuda değişik devre yapıları önerilmiştir. Bunlardan biri aktif elemanlarla endüktans fonksiyonunu gerçeklemektir. Fakat bu yaklaşımda gürültü performansı kötüleşmektedir.

Ring osilatör yapısı endüktans kullanılmayan bir diğer yaklaşımdır. Temel olarak ard arda eviricilerin bağlanarak osilasyon için gerekli faz çevrimi elde edilir. Faz gürültüleri LC osilatörlere gore kötü olmasına rağmen özellikle frekans çalışma aralığı geniş ve düşük maliyetli uygulamalarda tercih edilirler. Ayrıca bu yapıların entegrasyonu daha basittir.

Endüktans kullanmadan gerçeklenen bir başka osilatör yapısı da Wien-bridge yapıdır. Temel olarak band geçiren filtre karakteristiği gösterir. Fakat bu yapı yüksek frekanslar için uygun değildir çünkü içinde kullanılan operasyonel kuvvetlendirici

devresinin band genişliği osilatörün çıkabileceği maksimum osilasyon frekansını belirlemektedir. Fakat onun yerine işlemsel geçiş iletkenliği kuvvetlendiricisi kullanılırsa daha yüksek frekanslarda çalışabilen bir osilatör devresi tasarlanabilir. Bu devre yapısı da bu tezdeki tasarımlar arasında yer almaktadır.

Son olarak da, bir diğer alternatif osilatör yapısı da relaksasyon osilatörlerdir. Bu osilatörler, bir kapasitenin iki referans gerilimi seviyesi arasında doldurup boşaltılması prensibine gore çalışır.

Bu tez çalışmasında yukarıda bahsedilen 4 farklı osilatör yapısı 2.4 GHz osilasyon frekansı olacak şekilde tasarlanmıştır. Tüm tasarımlar 0.18µm teknolojisinde ve 1.8 V besleme gerilimi ile yapılmıştır. 2.4 GHz frekans bandı günümüzde oldukça yaygın bir kullanım ağına sahiptir. Bluetooth, Wi-Fi standartları ve araba elektronik sistemleri kullanım alanlarından bazılarıdır.

En iyi faz gürültü performansı-120 dBc/Hz (1 MHz ofset) ile LC osilatörden elde edilmiştir. Devrenin değer katsayısı diğer yapılara gore yüksek olduğu için bu beklenen bir sonuçtur. Hem PMOS hem de NMOS transistörler kullanılarak simetrik ve diferansiyel bir yapı oluşturulmuştur. Transistörlere kutuplama akımları ise NMOS akım aynası tarafından sağlanmıştır. Kullanılan diferansiyel endüktans sayesinde daha yüksek Q değerlerine ulaşılmış ve bu değer 8 olarak hesaplanmıştır. Diferansiyel endüktans yapısının frekans arttıkça Q değeri üzerindeki iyileştirme etkisinin daha da etkin olduğu gösterilmiştir.

Faz gürültüsü açısından LC yapıya en yakın sonuç -108.5 dBc/Hz ile relaksasyon osilatör yapısı ile elde edilmiştir. Ayrıca bu yapının önemli bir özelliği, aralarında 90^0 faz farkı ile dört farkı işaret elde etmek için uygulanan tekniğin faz gürültüsünü düşürmesidir. LC yapılarda bu tam tersi şeklinde olur ve faz gürültüsü yükselir. Bu iki farklı diferansiyel çıkış işaretleri arasındaki faz hatasının da 0.5 derece gibi düşük olduğu da gösterilmiştir. Bu tür yapılar günümüz yüksek frekans haberleşme sistemleri için önemlidir. Çünkü kullanılan çarpıcı devre yapılarında istenmeyen banddaki işaretin bastırılması için birbirinin kopyası iki çarpıcı devresi kullanılır ve taşıyıcı işaret girişlerine 90^0 faz farkıyla işaret uygulanır. Bu 90^0 faz farkı üzerinde hata, çarpıcının istenmeyen banddaki işareti bastırma oranını önemli ölçüde etkiler. Bu açıdan bu tür yapılar için faz hatası kritiktir.

Bir başka yaygın olarak kullanılan ring osilatör yapısı da 2.4 GHz osilasyon frekansı için tasarlanmıştır. Bu yapının da olumlu ve olumsuz yönleri ortaya konulmuştur. Geniş frekans ayarlama aralığı, tasarım ve entegrasyon kolaylığı bu yapıyı öne çıkaran özellikler olurken yüksek faz gürültüsü (97 dBc/Hz), üretim ve ortam sıcaklığı gibi değişken parametreler bağımlılığının yüksek olması da zayıf yönleri olarak sıralanabilir.

Ring osilatör yapılarına alternatif olabilecek, işlemsel geçiş iletkenliği kuvvetlendirici ile gerçeklenmiş, band geçiren filtre karakteristiğe sahip osilatör yapısı da yine 2.4 GHz için tasarlanmıştır. Bu yapının ise üretim ve ortam sıcaklığı gibi değişken parametrelere karşı duyarlılığı daha az olduğu görülmüştür. 1 MHz ofset ile 95.8 dBc/Hz faz gürültüsü elde edilmiştir. İşlemsel geçiş iletkenliği kuvvetlendiricisinin parazitik kapasitesi azaltıldığı taktirde bu devre yapısının performansının iyileştirilebileceği gösterilmiştir.

Uygulama devresi olarak ise,çıkışları arasında 90^0 faz farkı olacak şekilde tasarlanmış relaksasyon osilatör yapısı için çarpıcı devresi tasarlanmıştır. Bu uygulama ile relaksasyon devresinin düzgün bir şekilde çıkış işaretlerini üretip bunların çarpıcı devrelerde taşıyıcı işaret olarak kullanılabileceği gösterilmiştir. Özellikle düşük faz hatası ile üretilen çıkış işaretleri istenmeyen banddaki işareti 40 dB den fazla bastırma imkanı sağlamıştır. Buna benzer RF uygulamalar için relaksasyon osilatörünün LC osilatörlere iyi bir alternatif olabileceği gösterilmiştir.

Sonuç bölümünde bu farklı yapılardaki tasarımların karşılaştırması tablo halinde verilmiştir. Birbirlerine gore avantajları ve dezavantajları ortaya konmuştur. Buna gore bir tasarımcının, tasarlayacağı osilatör devresinin hangi uygulamada kullanılacağını bilip buna gore hangi parametrenin önemli olduğunu belirlemesi ve buna uygun tasarım yapısını seçmesi en iyi performansın elde edilmesini sağlayacaktır.

1. INTRODUCTION

1.1 Motivation

Certainly, the reason why the 21st century is called as communication age is developments and advances in electronic technologies and industry. In our daily life, we face computers, navigation, radar technology, microwave communication, cellular infrastructure and automotive technologies that mean we are living with electronic technology together. All these technologies need a common special electronic block called oscillators.

Oscillator circuits generate electronic signals without any input. In other words, they convert its DC power into a continuously repeating ac output signal. This output signal is used for modulation and demodulation or manages the flow of data in communication systems.

The downconversion and upconversion mechanism in communication systems is shown in Figure 1.1.

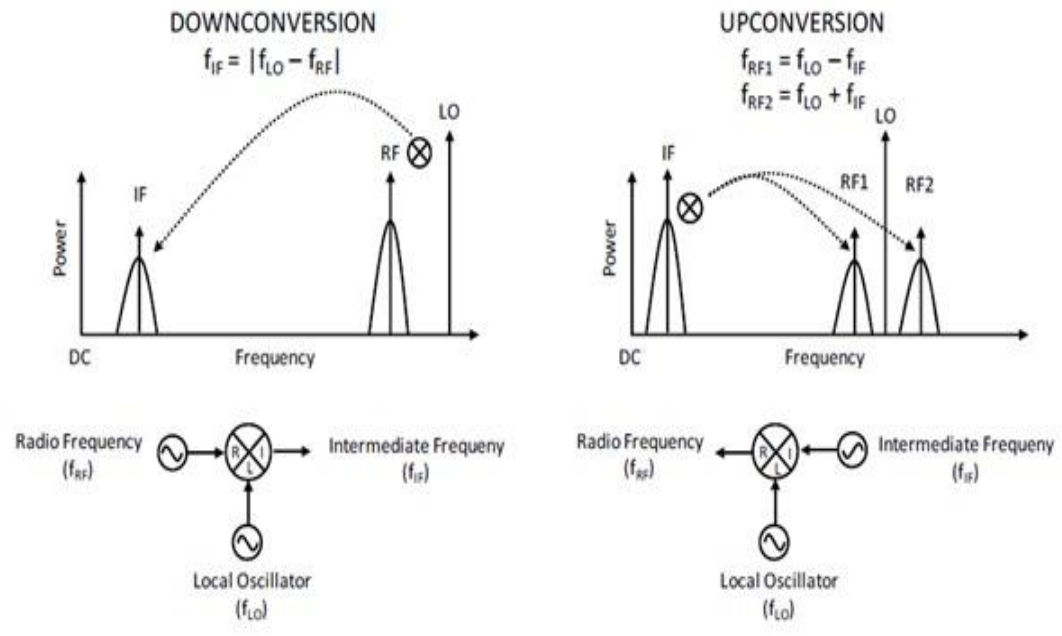

Figure 1.1 : Downconversion and upconversion [1].

The local oscillator signal is also called as carrier in downconversion and upconversion systems. The signal that includes information mixes with this carrier signal and transmitted to air as high frequency signal. In receiver structure, the signal from antenna should also be mixed with same carrier signal to obtain information. Therefore, in wireless communication structure, these local oscillators have critical roles.

Most important parameter in designing an oscillator is the oscillation frequency. The oscillation frequency should be stable and controllable. This control mechanism is also called as tuning range. To obtain the desired oscillation frequency over process and temperature changes, the tuning range should be also wide about 15% - 20%. Power consumption is also critical for oscillator. Very low power designs can be required in power limited systems. Noise is another concern in oscillator structures. It is usually defined as phase noise in these structures. The output power is another design specification because very low amplitude signals aren't sufficient for local oscillators

Over the years, innovations in integrated circuit process technologies allow the design voltage controlled oscillators as monolithic structures. Figure 1.2 shows the evolution of VCO technology over the years.

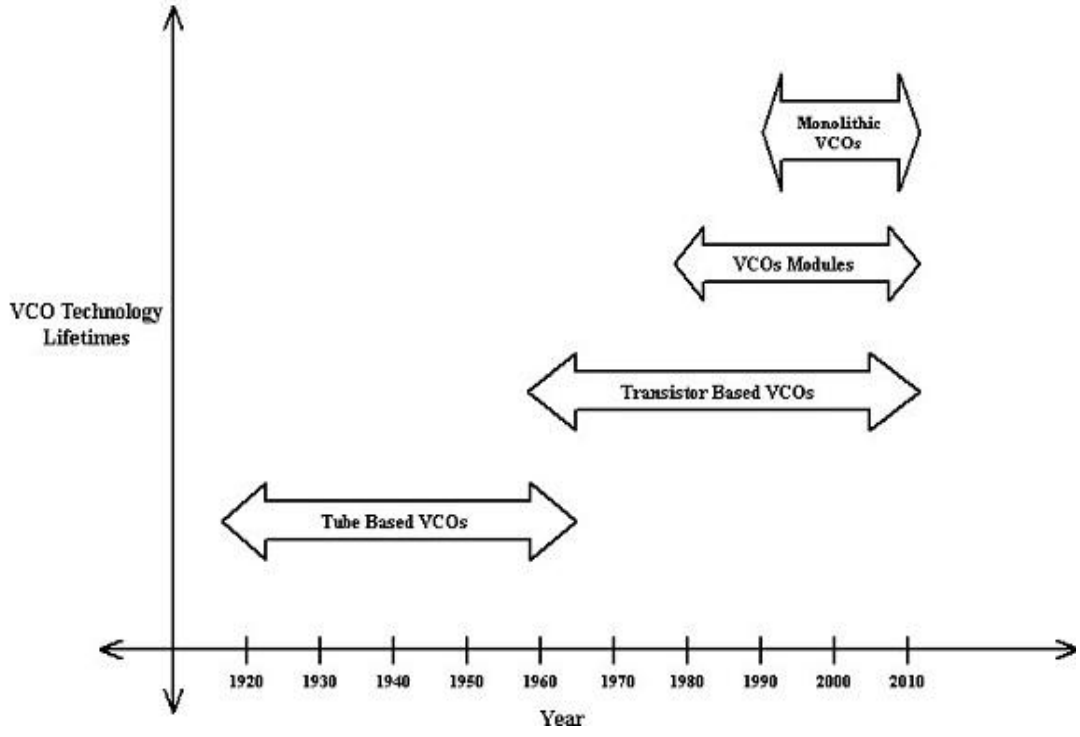

Figure 1.2 : Evolution of VCO technologies [2].

Figure 1.2 shows that, the trend in VCO design is monolithic structures in recent years. Therefore, high integration is more important for new VCO designs.

1.2 Purpose of Thesis

In RF front-end systems, the oscillator is an important block that determines performance of receiver or transmitter. It is used for modulation in transmitter path and for demodulation in receiver path.

There are different circuit structures to design voltage controlled oscillators. It depends on the application; LC oscillators are widely used in RF communication systems because of their best phase noise performance. However, LC oscillators have higher die cost because on-chip inductor cost is higher for high quality factor. Also, it is hard to model and design accurately. Therefore, other oscillator types like ring oscillators can be also useful although its phase noise performance is worse. There are also other RC oscillator topologies because ring oscillators have worse power supply noise dependence and the frequency is limited by stage number. Oscillator with passive RC bandpass filter is one of the alternatives to ring oscillators. Another alternative oscillator structure without using inductor is the relaxation oscillator. It can be very useful especially quadrature signals are required because its phase noise performance can be improved with quadrature structure.

These four types of oscillators are analyzed and designed in this thesis. 0.18μm CMOS technology is used and 2.4 GHz is selected as oscillation frequency because RF performance is important for new communication systems. The best overall performance is obtained with relaxation oscillator without using on-chip inductor. It can be alternative to LC oscillators especially for applications that required quadrature signal. Therefore, quadrature up conversion mixer is designed as an application for relaxation oscillator. It is used there as local oscillator. Satisfying results are obtained with this application circuit.

Finally, an LC VCO is designed at 2.4 GHz oscillation frequency and three other VCO structure is designed as an alternative to LC VCO without using on-chip inductor. These four type VCO designs are compared with each other to show their advantages and disadvantages. Same process and supply voltage is used for fair comparison.

1.3 Organization of Thesis

This thesis is divided into 7 chapters. It is organized in an arrangement that reader can have an intuition for voltage controlled oscillators in RF communication systems.

The motivation and purpose of thesis is presented in Chapter 1 with organization of thesis.

Chapter 2 starts an overview of negative $-g_m$ oscillation theory. Different LC VCO structures are introduced and one of them is designed. Finally, the design is compared with other LC VCO designs.

Chapter 3 provides background information about ring oscillators and theoretical analysis of phase noise in these structures. A ring oscillator for 2.4 GHz is designed and its performance is showed at the end of this chapter.

Chapter 4 shows an alternative RC oscillator design using OTA. Firstly, there is theoretical and design optimization for phase noise and power consumption is introduced. Then, simulation results of design are showed with results.

Last design example with relaxation oscillator structure is introduced in Chapter 5. After the phase noise analysis, the simulation results are shown to compare with other structures.

In Chapter 6, an up conversion mixer is designed as an application. Quadrature relaxation oscillator is used there as local oscillator. At the end of the chapter, simulation results are shown and compared with other designs.

Chapter 7 summarizes the four different VCO designs and compares their performance. Also conclusion of the thesis is presented in this chapter.

2. LC OSCILLATOR DESIGN

An oscillator can be modeled as a feedback system that is shown in Figure 2.1.

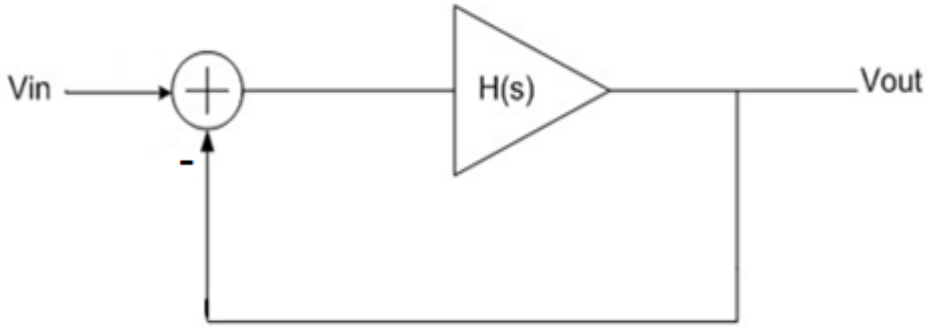

Figure 2.1 : Oscillator feedback system.

The transfer function of this system can be expressed as;

$$\frac{Vout}{Vin}(s) = \frac{H(s)}{1+H(s)} \tag{2.1}$$

For $s = j\omega, H(j\omega) = -1$ where the close loop gain goes to infinity, the system causes its own noise to grow and generates a periodical signal. $H(j\omega)$ should be purely imaginary to reach steady state. This process is shown in Figure 2.2 below.

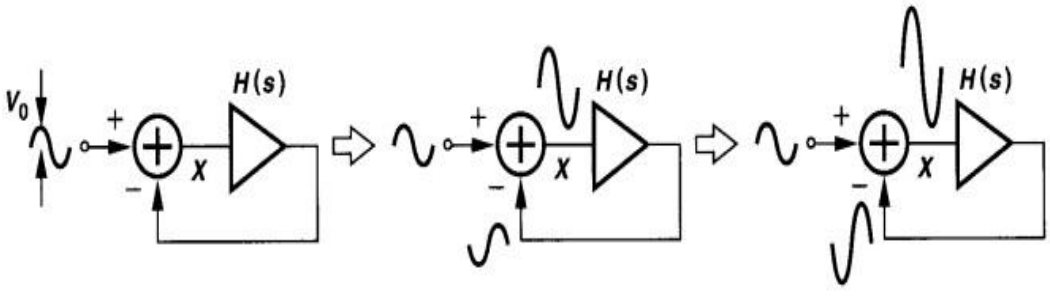

Figure 2.2 : Process of oscillation in time [3].

Consequently, for steady state oscillations to occur at frequency ω, two conditions must be satisfied;

1. $H(j\omega) \geq 1$, loop gain must be equal or greater than 1
2. $\angle H(j\omega) = 360^0$, total phase shift around the loop must be 360^0

The above conditions are commonly known as Barkhausen's criteria. Negative resistance concept is another way to describe this oscillator operation.

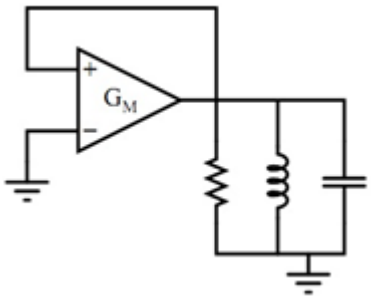

Figure 2.3 : Simple model of negative resistance LC oscillator [4].

A simple model of negative resistance LC oscillator can be seen in Figure 2.3(b). In this figure, the active device is a simple transconductor amplifier that connected in positive feedback to an LC tank circuit. It is conspicuous to show that the tank circuit sees a negative resistance of $-1/G_M$ looking back into the transconductor output.

It can be shown that if the Barkhausen's criteria are satisfied, the negative resistance will exactly cancel the equivalent parallel resistance of the tank circuit. In other words, the total loss energy in the tank circuit should be compensated by the active device. Otherwise, the circuit would simply behave as an underdamped system.

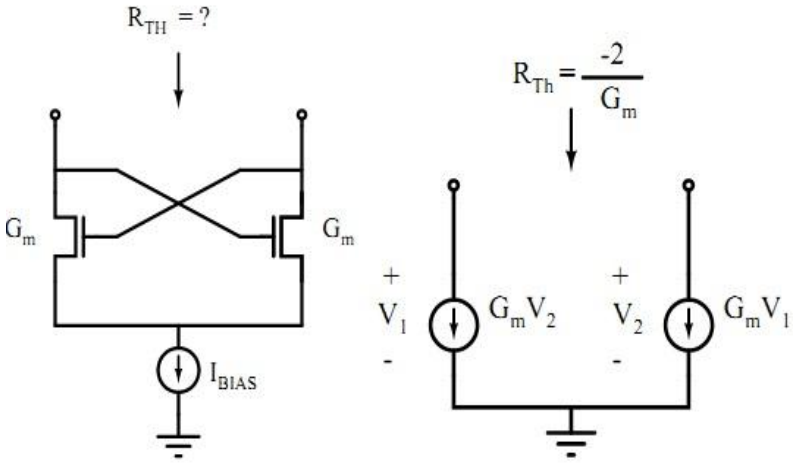

Figure 2.4 : Cross coupled NFET's [4].

Figure 2.4 shows that the input resistance seen looking the cross coupled NMOS transistors is -2/G_M. Parallel resistance of the tank circuit should be greater than this negative resistance to maintain sustained oscillation. Tranconductance and current equations is shown in Equation **(2.2).**

$$\frac{2}{G_M} \le R_P$$

$$I_{DS} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)\left(V_{GS} - V_{th}\right)^2$$

$$G_M = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{Q_{point}} = \mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS} - V_{th}\right) \qquad \textbf{(2.2)}$$

Another part of negative G_M oscillator is LC tank circuit. It is a resonator circuit with a parallel combination of inductor and capacitance that is shown in Figure 2.5. The main contributors of loss in tank are the series resistance of the passive devices. The parasitic resistances can be converted to their parallel equivalent since RF oscillators operate over a narrow band of frequencies.

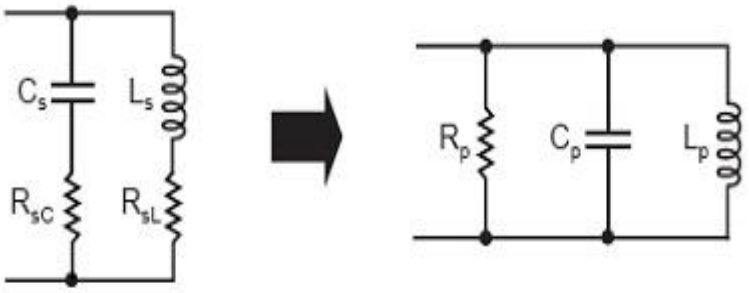

Figure 2.5 : Conversion of series resistance of LC tank into parallel equivalent [5].

The parallel components in Figure 2.5 can be expressed as;

$$C_p \approx C_s$$

$$L_p \approx L_s$$

$$R_p = R_L // R_C = R_{sC} // Q_{sL}{}^2 R_{sL}, \quad (Q_{sL} >> 1, Q_{sC} >> 1) \qquad \textbf{(2.3)}$$

The quality factor of inductor is lower than the quality factor of capacitance even if diode or MOS varactors are used. Therefore, the dominant term of R_p is related to inductor loss.

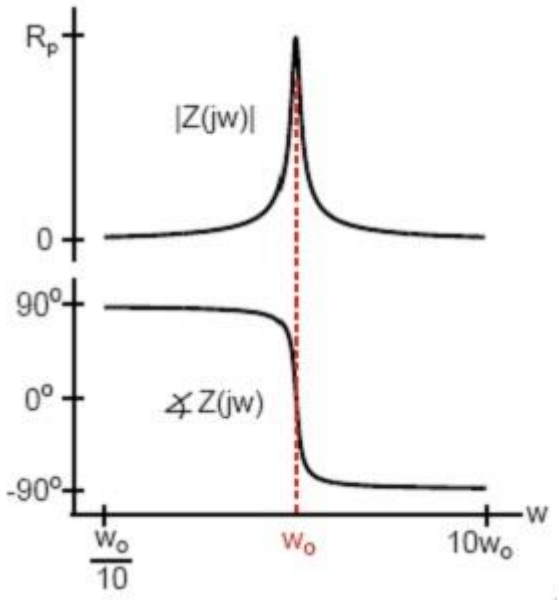

Figure 2.6 : Magnitude and phase spectrum of LC tank [5].

The magnitude and phase characteristics of an LC parallel network are shown in Figure 2.6. The circuit behaves like a pure resistor at resonance frequency. The resonance frequency can be expressed as;

$$\omega_0 = 1/\sqrt{LC} \qquad \textbf{(2.4)}$$

Finally, it is shown in Figure 2.7 that negative g_m and resonator together form an oscillator.

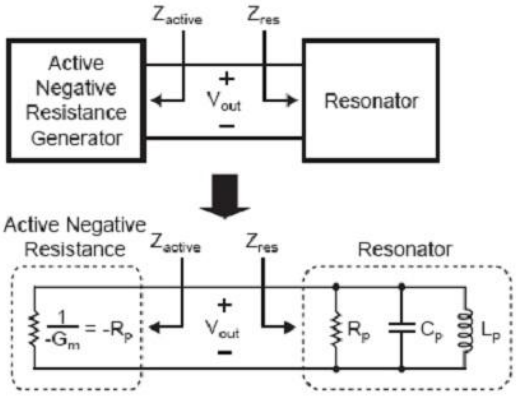

Figure 2.7 : One-port view of LC oscillator [5].

2.1 Cross-Coupled LC Oscillators

In a cross-coupled topology, the transistor pair behaves like an active negative resistance. This negative resistance is chosen at least two times greater than the parallel loss to guarantee oscillation start-up. This topology is very useful because it is simple to design and has differential structure. The NMOS and PMOS implementation of this topology is shown in Figure 2.8.

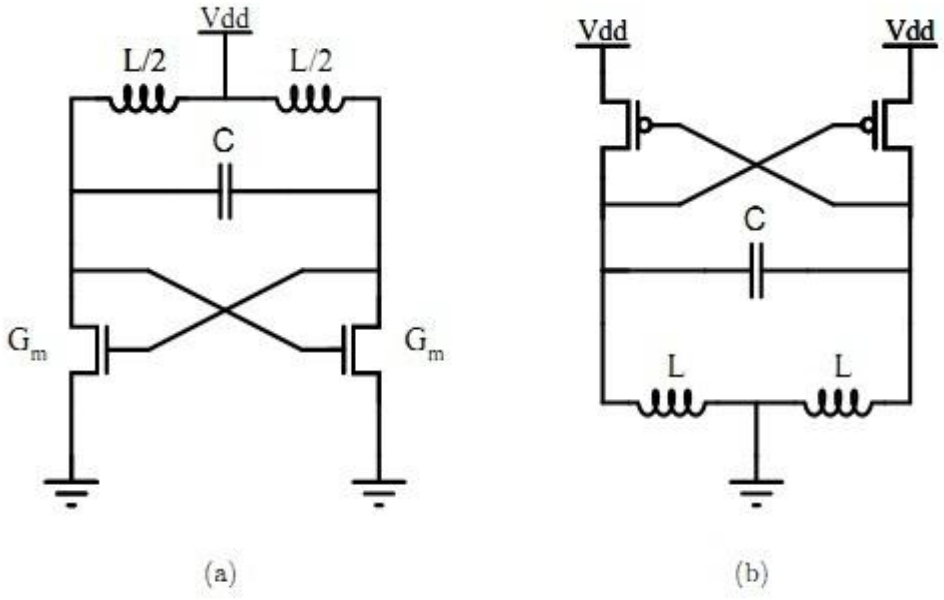

Figure 2.8 : a) Cross-coupled NMOS structure b) Cross-coupled PMOS structure [4].

In Figure 2.8 (a), the negative resistance of transistors is directly related to supply voltage. Therefore, the oscillation amplitude and phase noise also depend on supply voltage. This isn't desirable for oscillators. Therefore, constant tail current source is more useful in this topology.

2.1.1 NMOS only LC VCO

NMOS cross-coupled oscillator structure that consists of two parts, LC tank and negative resistance circuit is shown in Figure 2.9(a). The inductors are common mode coupled to current source. The resonator of oscillator is designed to cover designed frequency band. NMOS structure has higher transconductance with respect to PMOS structure thanks to higher electron mobility. This provides to decrease negative resistance more easily in same power conditions.

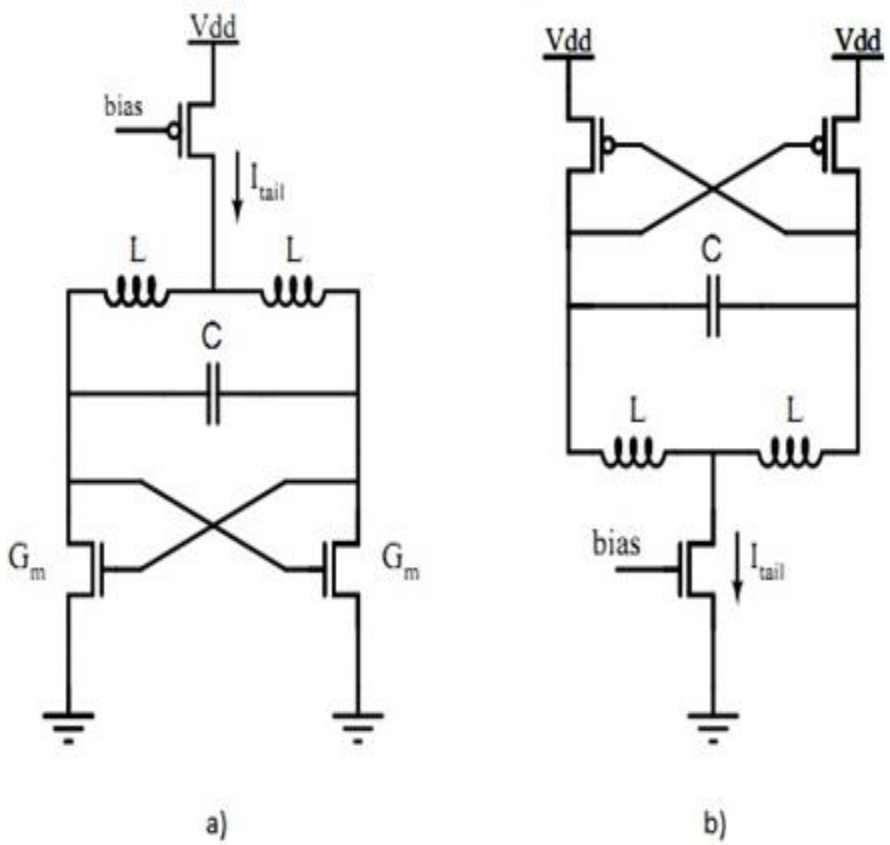

Figure 2.9 : (a) NMOS only $-G_M$ oscillator (b) PMOS only $-G_M$ oscillator [4].

2.1.2 PMOS only LC VCO

PMOS core differential LC oscillator structure is shown in Figure 2.9(b). The PMOS transistor has lower mobility with respect to NMOS. Therefore, the transistor sizes should be larger that means more parasitic capacitance and less tuning range. On the other hand, the advantage of PMOS devices is lower flicker noise. A PMOS transistor has about 10 times lower flicker noise than NMOS counterpart.

2.1.3 Complementary LC VCO

In this structure, the negative resistance is made by both NMOS cross-coupled pair and PMOS cross-coupled pair that shown in Figure 2.10. The total transconductance is increased that results in lower negative resistance for same power conditions. Therefore, this structure provides better phase noise performance with same power consumption. Equation **(2.5)** shows the equivalent resistance.

$$R_{neg} = \frac{-2}{G_{Mn} + G_{Mp}} \qquad \textbf{(2.5)}$$

Another advantage of this topology is that it is fully differential that enables the implementation of differential inductance. Higher quality inductance can be obtained with differential structure.

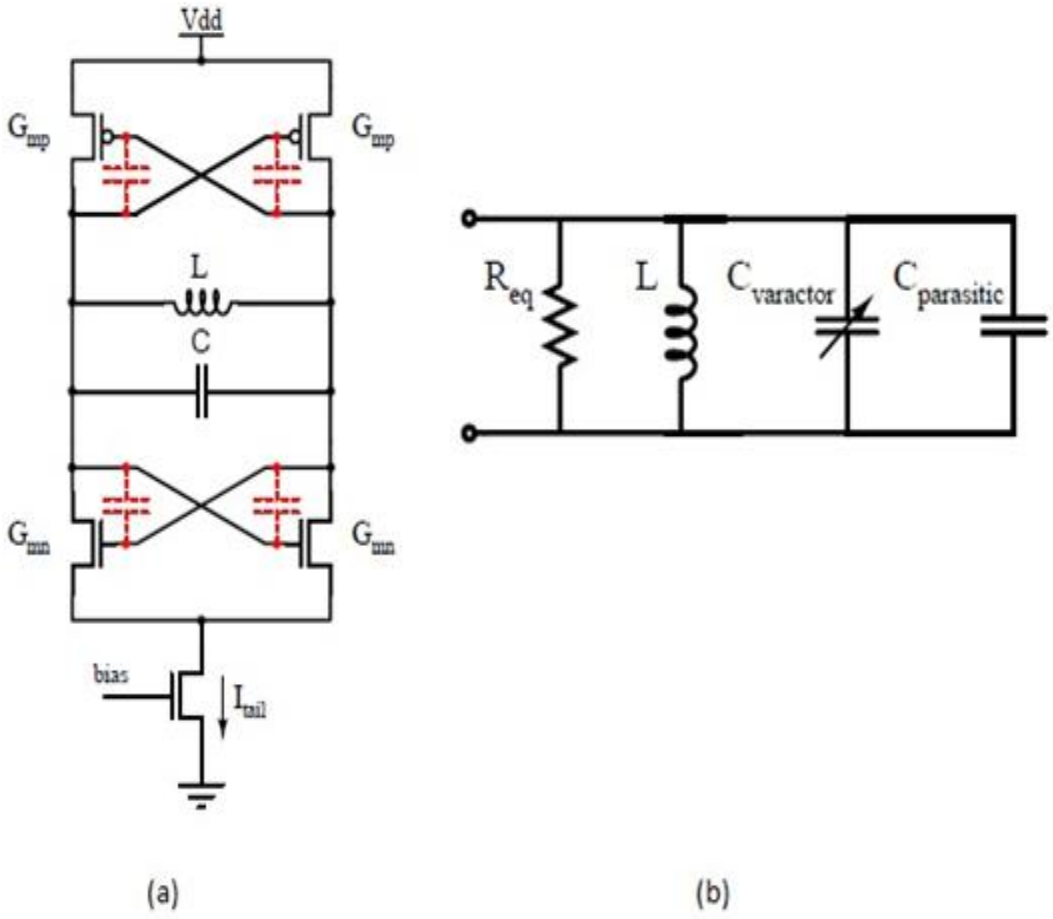

Figure 2.10 : (a) CMOS $-G_M$ oscillator. (b) Equivalent tank circuit model [4].

The disadvantage of this structure is larger parasitic capacitance that comes from both NMOS and PMOS devices and higher parasitic capacitance means lower tuning range.

2.2 LC Oscillator Phase Noise

The most critical parameter of RF oscillators is frequency stability. An ideal oscillator would have an output frequency spectrum that consists of unit impulse centered at oscillation frequency and harmonics shown in Figure 2.11 (a). However, the real case looks like in Figure 2.11(b). In real case, there are also other frequency components near the desired signal. The power of these spurs decreases with related distance to desired signal frequency.

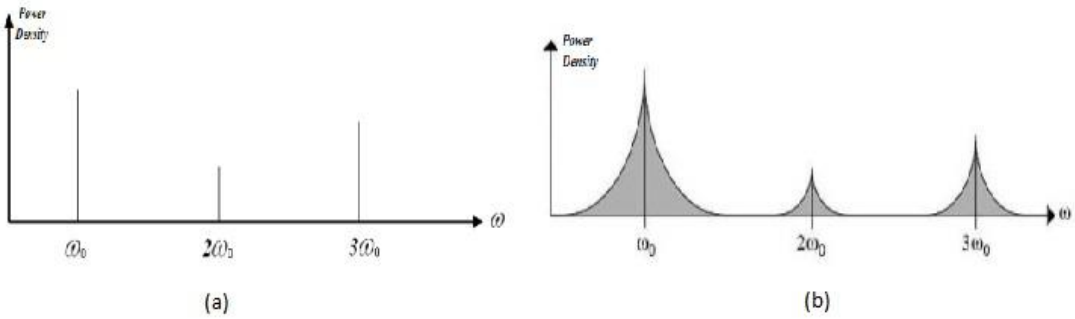

Figure 2.11 : (a) Ideal oscillator spectrum. (b) Practical oscillator spectrum [6].

The phase noise can be defined as undesirable power distribution around desired oscillation frequency. In the time domain, phase noise is also referred to as timing jitter. Mathematical definition of phase noise is also shown below.

$$\mathcal{L}\{\Delta\omega\} = 10\,log\left(\frac{\text{Noise power at } (\omega_0 + \Delta\omega) \text{ in 1 Hz Bandwidth}}{\text{carrier power}}\right) \quad \textbf{(2.6)}$$

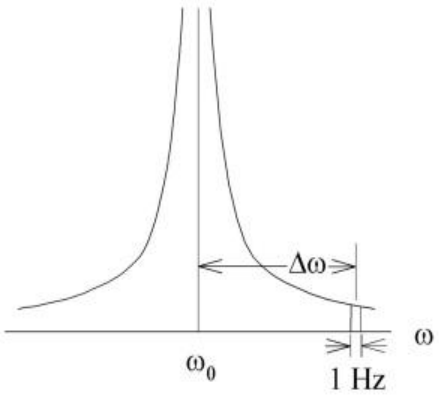

Figure 2.12 : Phase noise in oscillator output spectrum [4].

Figure 2.12 shows the phase noise in oscillators. The unit is decibels below the carrier per Hertz (dBc/Hz).

In the time domain, the output signal of the sinwave oscillator can be expressed as;

$$V_{out}(t) = A\sin(\omega_0 t + \theta) \quad \textbf{(2.7)}$$

However, oscillators implemented with real devices produce their own noise. This noise affects both output signal amplitude and phase. Therefore, the real case is expressed in Equation **(2.8).**

$$V_{out}(t) = A(t)\sin(\omega_0 t + \theta(t)) \quad \textbf{(2.8)}$$

Since A(t) and θ (t) are now functions of time, the frequency spectrum of V_{out} will contain noise sidebands near the oscillation frequency. In many RF systems, the output of the oscillator is limited with limiting amplifier before the LO port of mixer. Therefore, only phase noise is usually considered.

2.2.1 Effect of phase noise on transceiver and transmitter architectures

In a front-end part of transceiver, IF signal is down converted by LO signal without change in shape. However, phase noise skirts of the LO is modulated onto the stronger signal at IF, thereby reducing the signal-to-noise ratio (SNR) of the desired signal at IF frequency. It is shown in Figure 2.13.

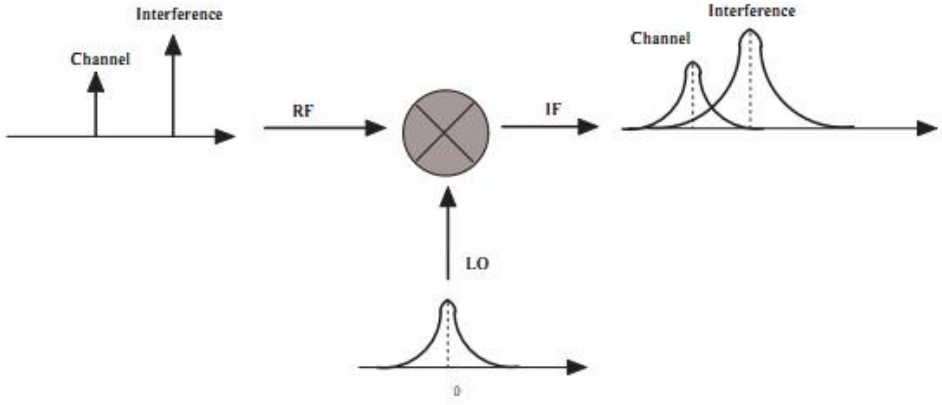

Figure 2.13 : Reciprocal mixing due to phase noise [6].

This phenomenon is usually called as reciprocal mixing and it is also related with how close together channels can be placed. Similarly in transmitter, a strong interferer modulated by LO and its skirts extend over the desired signal in the receiver part. The effect of phase noise in transmitters is shown in Figure 2.14.

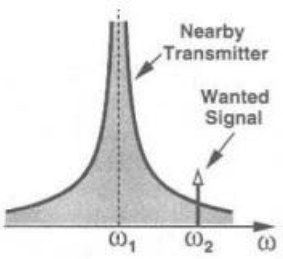

Figure 2.14 : Effect of phase noise in transmitter [5].

Finally, phase noise results in unwanted energy being transmitted outside of the desired band.

2.2.2 Leeson's phase noise model

The intrinsic noise sources in negative G_M oscillators can be put in two categories as the noise of resonator and the noise of active circuit. The noise from loss of the passive elements in first category and thermal, flicker noise of active devices is in the second category.

The one port view of negative G_M oscillators is shown in Figure 2.15.

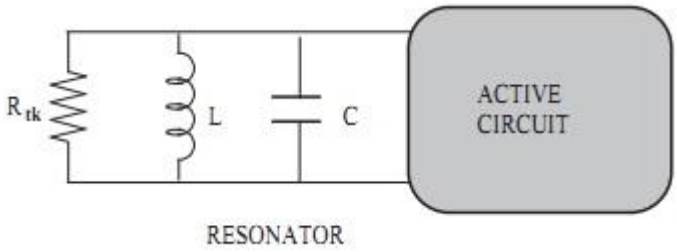

Figure 2.15 : Oscillator with losses in the LC tank [6].

Assuming noise contribution is only by R_{tk} with thermal white noise, the mean square value of the noise voltage is expressed in Equation **(2.9)**.

$$\overline{v_n^2} = \overline{i_n^2}\left|Z_{tk}\right|^2 \tag{2.9}$$

Z_{tk} is the actual tank impedance. The noise current and tank impedance can be expressed as Equation **(2.10)** and finally mean square noise voltage can be obtained.

$$Z(\omega_0 + \Delta\omega) \approx j\frac{\omega_0 L}{2(\Delta\omega/\omega_0)} \approx \frac{R_{tk}}{2}\frac{\omega_0}{Q\Delta\omega}$$

$$\overline{i_n^2} = \frac{4kT\Delta f}{R_{tk}}$$

$$\frac{\overline{v_n^2}}{\Delta f} = kTR_{tk}\left(\frac{\omega_0}{Q\Delta\omega}\right)^2 \tag{2.10}$$

It can be seen from the noise spectral density equation that, both the amplitude and phase noise is inversely proportional to quality factor. Due to the compression and

limiting behavior of circuit, only the phase noise has to be taken into account. Finally, the common phase noise expression is shown in Equation **(2.11)**.

$$L(\Delta\omega) = 10\log\left[\frac{\overline{v_n^2}}{\overline{v_{sig}^2}}\frac{1}{\Delta f}\right] = 10\log\left[\frac{1}{2}\frac{KT}{P_{sig}}\left(\frac{\omega_0}{Q\Delta\omega}\right)^2\right] \qquad \textbf{(2.11)}$$

Ratio of this noise to the carrier power is more important. Therefore, phase noise is usually expressed as dBc/Hz at specified offset frequency.

Equation **(2.11)** shows that, phase noise is related with quality factor, signal power and frequency offset. However, that formula doesn't include the active negative resistance block. In reality, there are some other effects such as flicker noise of transistors, noise of the bias transistors, switching noise of cross coupled transistors.

In real phase noise characteristic, the phase noise degrades -30dB/decade at low offset frequencies. Then, for a wide range the slope is fixed to -20dB/decade. In very high frequency offset, the noise slope is flattening.

The real phase noise characteristic of a negative G_M oscillator is shown in Figure 2.16.

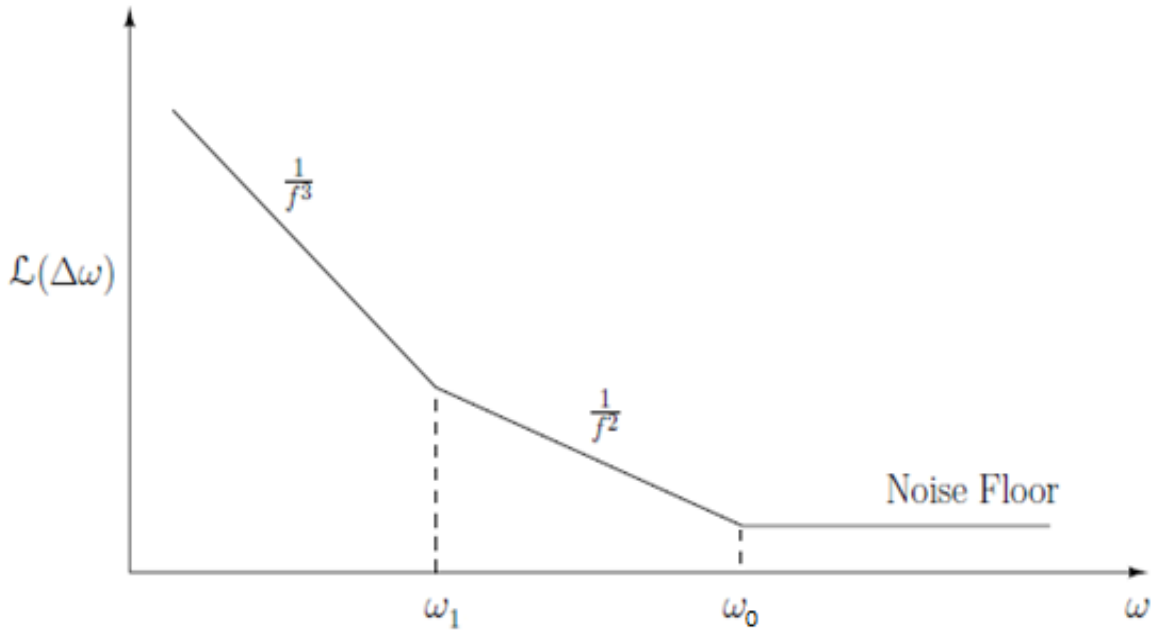

Figure 2.16 : Phase noise spectrum of a practical oscillator [6].

In the late sixties, Leeson proposed a new noise formulation that show in Equation **(2.12)** to get more accurate results [4].

$$L(\Delta\omega) = 10\log\left\{ F\frac{2KT}{P_{sig}}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left[1+\frac{\omega_1}{|\Delta\omega|}\right]\right\} \quad \textbf{(2.12)}$$

In Equation **(2.12),** the last term express the low frequency region and the F factor is empirically determined parameter, k is Boltzman's constant, T is the absolute temperature, P_{sig} is the average power dissipated in the resonator, Q is the loaded quality factor of the resonator.

Finally, the noise analyses of oscillator shows that, phase noise is inversely proportional to second order of quality factor and average power dissipated in tank circuit. Therefore, designing high Q IC inductors and higher oscillation voltage amplitude provide lower phase noise. Usually, the total power is limited by the given specifications. This makes more important to have higher Q value to obtain lower phase noise.

2.3 IC Inductors

This chapter gives information about used inductors in RF IC design.

2.3.1 Bond wire inductors

It is the wire between die and package paddle. The inductance of this wire is about 1 nH/mm. Their loss is very small therefore high Q inductors can be obtained. Double bond wire can be used between die pad and package to reduce inductance and loss. The disadvantage of bond wire inductors is that their value is sensitive. A bond wire example is shown in Figure 2.17.

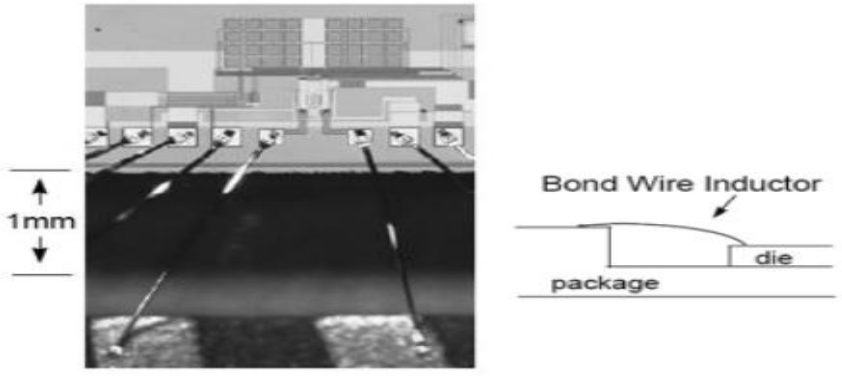

Figure 2.17 : Bond wire inductance [5].

2.3.2 On-chip inductors

Although they have lower quality factor, the most used inductors in RF IC design is on-chip inductors because they can be modeled and designed more accurately. Their main drawback is they take up much space in die and that means higher chip cost.

Most used inductor geometries are shown in Figure 2.18.

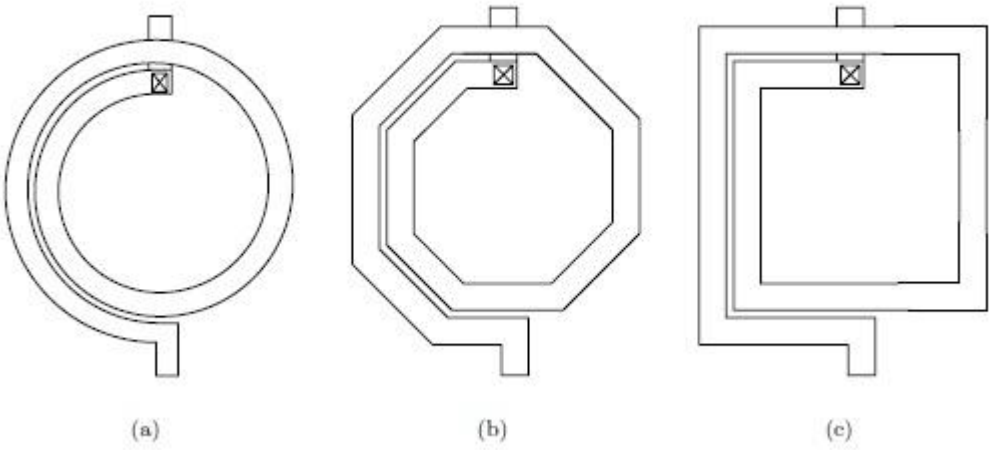

Figure 2.18 : a) Circular spiral. b) Octagonal spiral. c) Square spiral [4].

Optimum structure for minimum area and loss is circular spiral geometry. However, some foundries don't provide it because of harder manufacture process. Sometimes differential structures are also preferred to obtain higher Q.

2.3.2.1 Modeling of on chip inductors

The narrow band model is usually used because of its easy calculation. Figure 2.19 shows the typical lumped model of on-chip inductors.

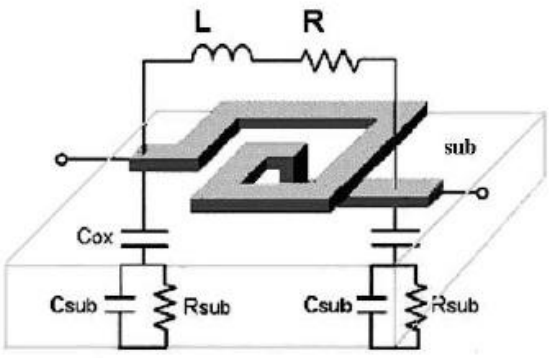

Figure 2.19 : Lumped model of square spiral inductor [4].

In Figure 2.19, L is the series inductor, R is the series resistance, C_{OX} is the oxide capacitance, C_{SUB} is the substrate capacitance and R_{SUB} is the resistance of substrate. The physical model can be translated to narrowband model using Equation **(2.13).**

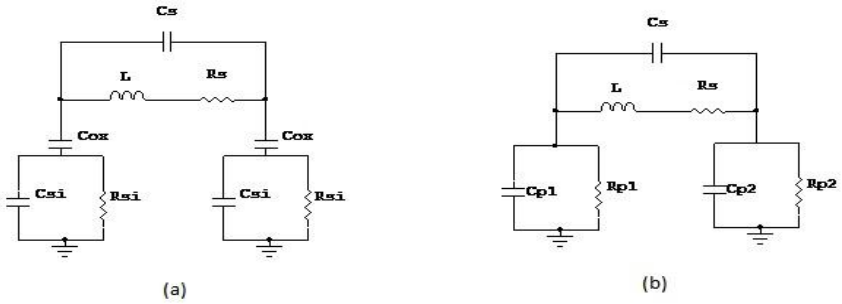

Figure 2.20 : (a) Physical model of IC inductor. (b) Equivalent narrow band model.

Resistance and capacitance values in Figure 2.20 are shown in Equation **(2.13).**

$$R_{p1} = R_{p2} = \frac{1+(\omega \cdot R_{si} \cdot (C_{si}+C_{ox}))^2}{\omega^2 \cdot R_{si} \cdot (C_{si}+C_{ox})} \approx \left(1+\frac{C_{si}}{C_{ox}}\right)^2 \cdot R_{si}$$

$$C_{p1} = C_{p2} = \frac{C_{ox}+\omega^2 \cdot R_{si} \cdot (C_{si}+C_{ox}) \cdot C_{si} \cdot C_{ox}}{1+(\omega \cdot R_{si} \cdot (C_{si}+C_{ox}))^2} \approx \left(\frac{C_{si} \cdot C_{ox}}{C_{si}+C_{ox}}\right) \qquad \textbf{(2.13)}$$

We can express conductance loss of inductor as in Equation **(2.14)** after connecting one port to ground.

$$g_L = \frac{R_s}{(\omega L)^2} + \frac{1}{R_{p1}} \qquad \textbf{(2.14)}$$

If the inductor is driven differentially, conductance loss is decrease. Equation (**2.15)** shows conductance loss when inductor is differentially driven.

$$g_{Ld} = \frac{R_s}{(\omega L)^2} + \frac{1}{R_{p1}+R_{p2}} \qquad \textbf{(2.15)}$$

Therefore, the quality factor is higher when the inductor is driven differentially. Equation **(2.16)** shows the relation between conductance loss and quality factor.

$$Q = \frac{1}{g_L \cdot \omega \cdot L} \qquad \textbf{(2.16)}$$

2.3.2.2 Simulation of on chip inductor

Chip inductor modeling equations are useful only for narrow band and some magnetic effects are ignored such as eddy currents, to simplify equations. Therefore, some high modeling software should be used to get more reliable results when designing IC inductors. Figure 2.21 shows a square inductor that is designed in SONNET. The used metal width is 6µm and edge to edge distance is 150 µm.

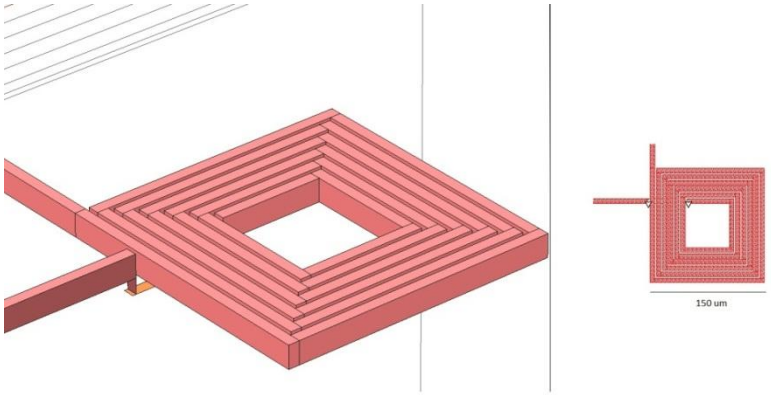

Figure 2.21: IC inductor designed in SONNET.

Figure 2.22 shows the simulation results of this inductor. It is about 5.3 nH inductor with about 9 ohm series loss.

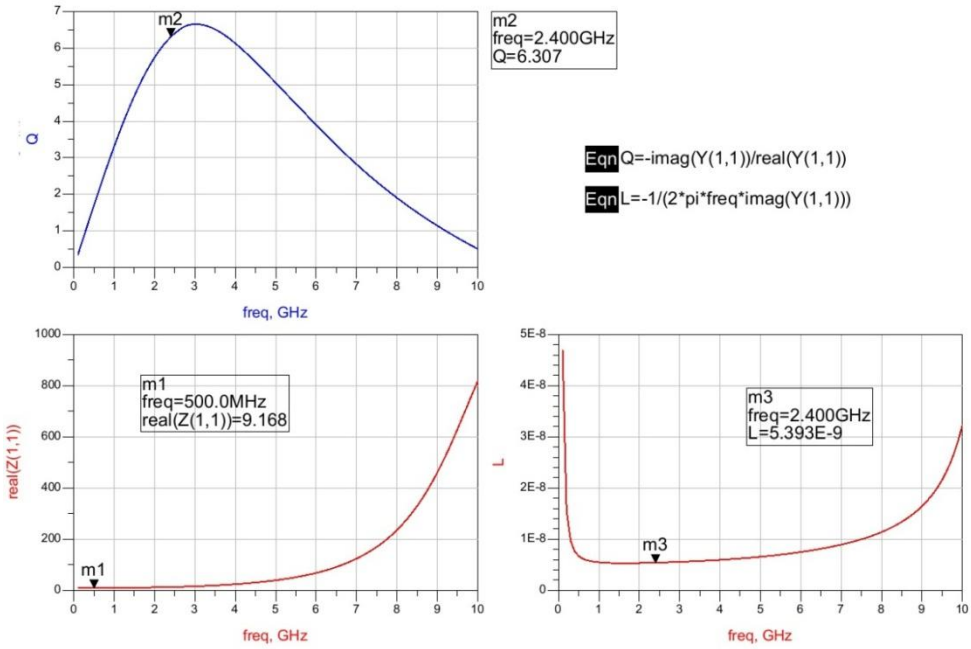

Figure 2.22 : Simulation results of IC inductor.

It can be seen from Figure 2.22 that, the Q value of this IC inductor is above 6 from 2 GHz to 4GHz frequency range.

Equation **(2.15)** shows that, the Q value is higher when driving inductor differentially. It is also simulated with differential structure and the simulation results are shown in Figure 2.23 compared to single ended version.

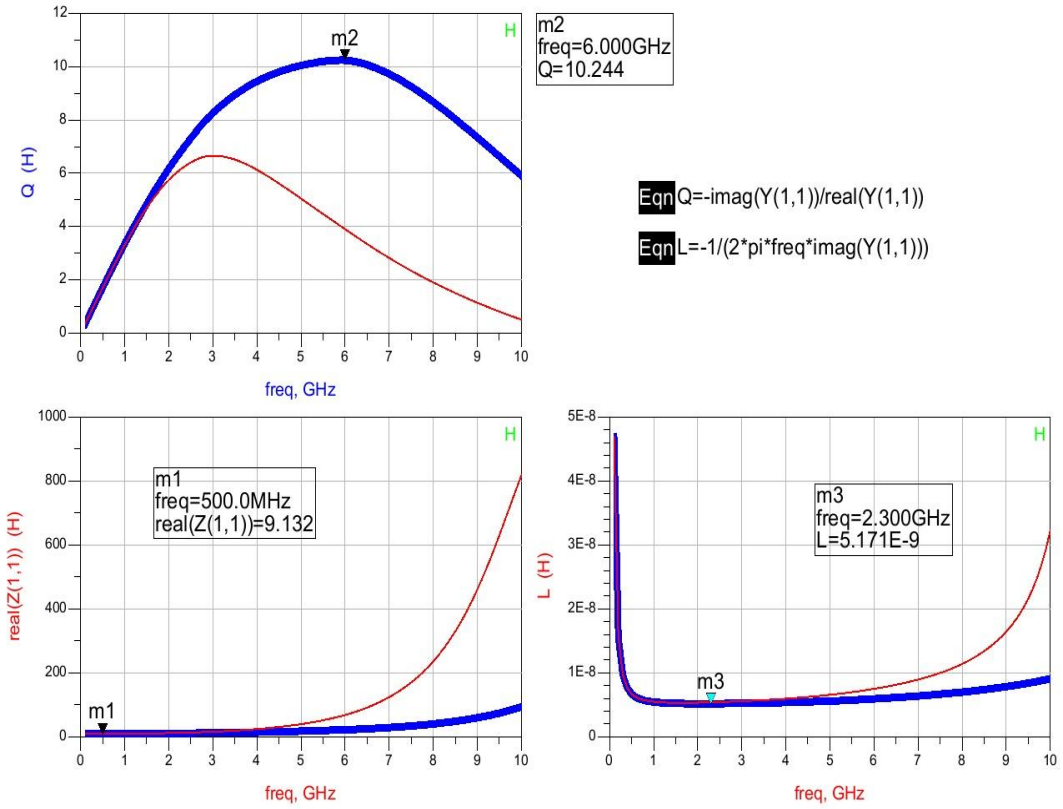

Figure 2.23 : Comparison single ended and differentially driven IC inductor.

It can be seen from Figure 2.23 that, differentially plot reduce the series resistance and provide higher Q value especially at higher frequencies. The maximum Q value is about 10 for 6 GHz.

2.4 MOS Varactor

In CMOS RF voltage controlled oscillators, MOS varactors are widely used to tune oscillation frequency. In this structure, the total capacitance can be changed by voltage across the MOS varactor. Although the quality factor of oscillator is determined by inductor, the design of MOS varactor is also critical. If the varactor isn't carefully designed, it can also increase the phase noise with its series resistance.

The MOS capacitor is also like parallel plate capacitors. One plate is the gate of the transistor and another plate is the channel between drain and source. The capacitance of this structure behaves differently with related to DC voltage of the gate. This

behavior can be distributed as accumulation, depletion and inversion mode. Figure 2.24 shows the cross section and the corresponding C-V graph for each behavior.

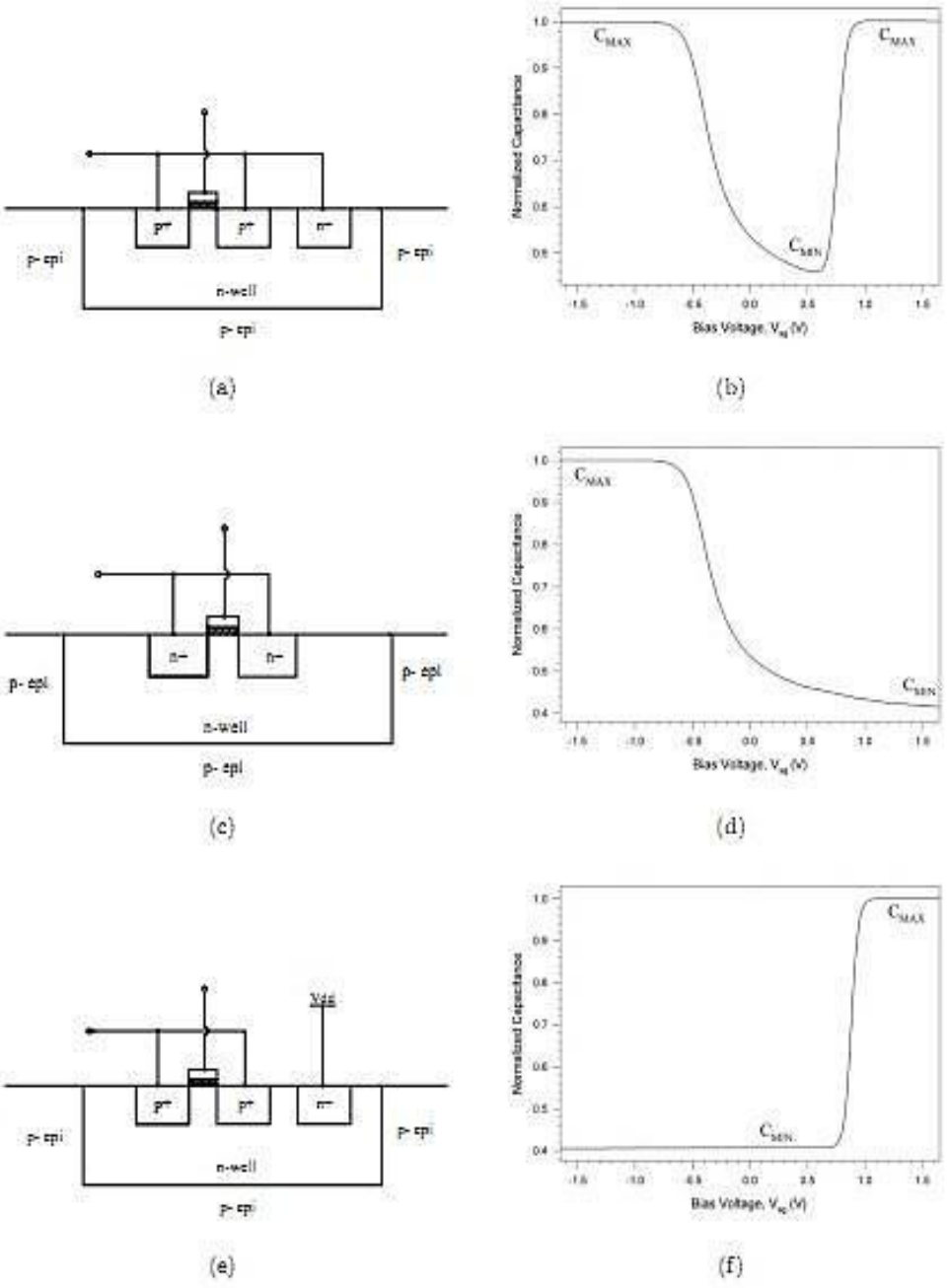

Figure 2.24 : (a) D=S=B structure. (b) D=S=B C-V curve. (c) Accumulation mode. (d) Accumulation mode C-V curve. (e) Inversion mode. (f) Inversion mode C-V curve[4].

The maximum capacitance value is related to C_{OX} in inversion and accumulation mode. Equation **(2.17)** shows this relation.

$$C_{ox} = \frac{3.9\varepsilon_0 WL}{t_{ox}} \quad \textbf{(2.17)}$$

t_{ox} is the gate oxide thickness.

D=S=B mode varactor works in two different regions that are accumulation and inversion. Figure 2.25 shows the simulation result of D=S=B varactor.

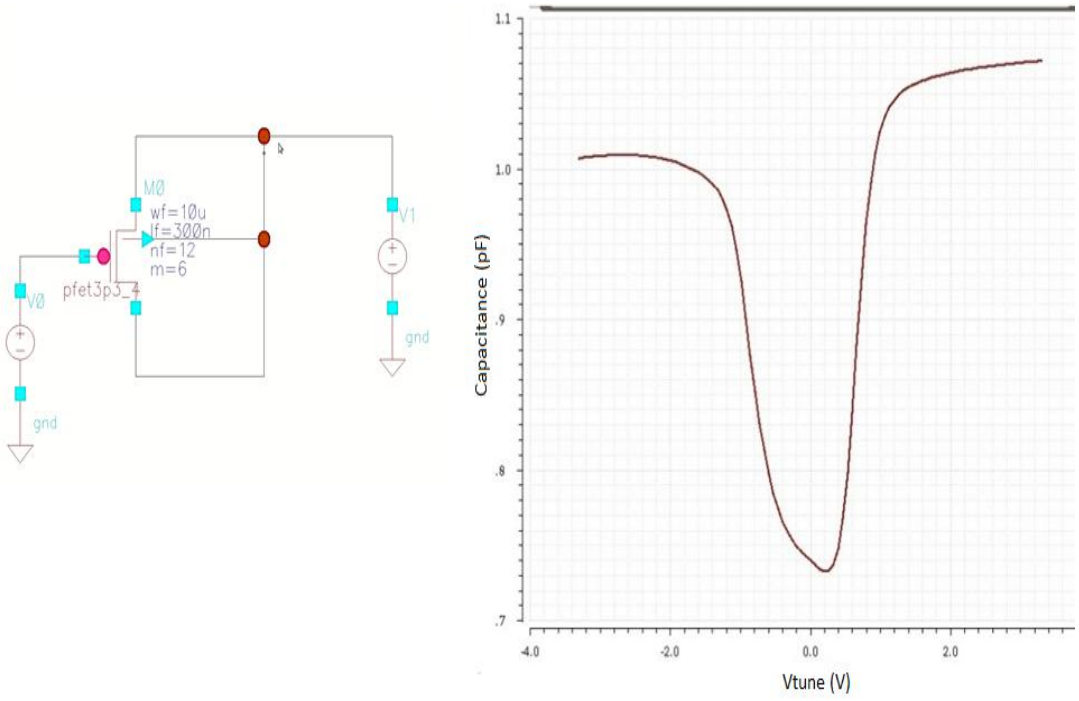

Figure 2.25 : D=S=B varactor schematic and simulation results.

In Figure 2.25 drain, source and bulk of PMOS is connected together and DC voltage is applied. 1V AC signal is applied to gate and total capacitance is calculated as $C=i_g/(2\pi f)$. For $V_G > V_B$, PMOS transistor is in accumulation mode and electron density increases in channel. For $V_G < V_B-V_T$, transistor is in inversion mode. The total maximum capacitance value is equal to $C_v=W*L*C_{ox}$. It is about 1pF for this simulation.

Between accumulation and inversion mode, the channel carrier density is changed and capacitance value also changes. However, this non monolithic behavior isn't useful for voltage controlled oscillators.

If the bulk of transistor is connected to V_{DD}, the transistor works in only inversion mode. The simulation result for this connection is shown in Figure 2.26.

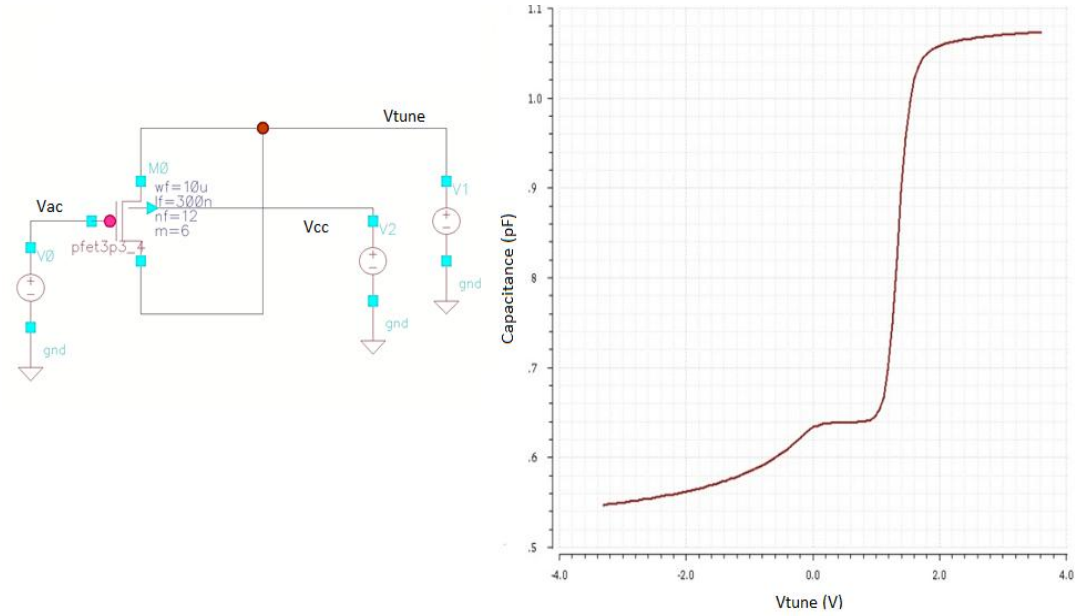

Figure 2.26: Inversion mode MOS varactor.

Difference of the C_{max} and C_{min} of varactor is also determining the tuning range of VCO. C_{max}/C_{min} ratio is proportional to channel length. However, increasing the channel length also decreases the quality factor. Channel length of MOS transistor in varactor can affect the phase noise. Therefore, these effects can be considered in design.

2.5 LC VCO Design

The theory of the $-G_M$ oscillators is discussed before. As a starting point of the design, some basic formulas are used. Usually, VCO's are designed for minimum phase noise under the constraints of power dissipation, tuning range, output voltage swing and production cost.

The most critical parts of LC VCO are inductor and capacitance. Oscillation frequency is 2.4 GHz for this design. Therefore, these passive component values should be chosen to satisfy oscillation frequency. The capacitance value is also determining the tuning range because lower capacitance means low tuning range.

The inductor and capacitance values can be chosen 4nH and 1 pF initially, that looks logical values to implement IC design [4].The complementary structure is chosen because of its lower phase noise performance with same power dissipation. The simple schematic of design is shown in Figure 2.27.

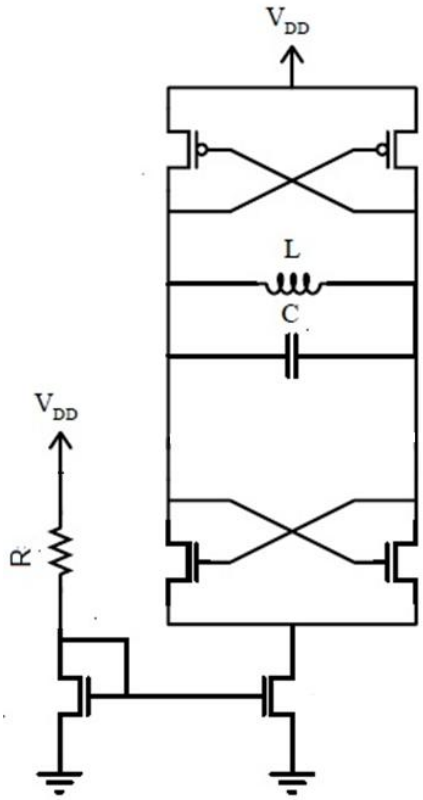

Figure 2.27 : Simple schematic of complementary LC VCO.

R is the equivalent shunt resistance of the tank circuit. Another important parameter is the DC current. The upper current limit can be determined with maximum power dissipation specification.

$$I_{bias} = P_{dc\max} / V_{\text{supply}} \qquad \textbf{(2.18)}$$

It is desired that maximum power consumption should be 10 mW with 1.8V V_{DD}. From the Equation **(2.18)**, the maximum bias current should be around 5 mA.

Next step of the design is determining the quality factor of inductor for desired oscillation frequency. It is mentioned before that quality factor of inductor is important to improve phase noise performance. High quality factor is required for better phase noise performance. Differential structure is used to obtain lower series resistance and phase noise.

Simulation result of quality factor is shown in Figure 2.28 with 150µm x 150µm size inductor. Increasing the inductor size results in increasing quality factor, but it means higher fabrication cost because of wider layout area.

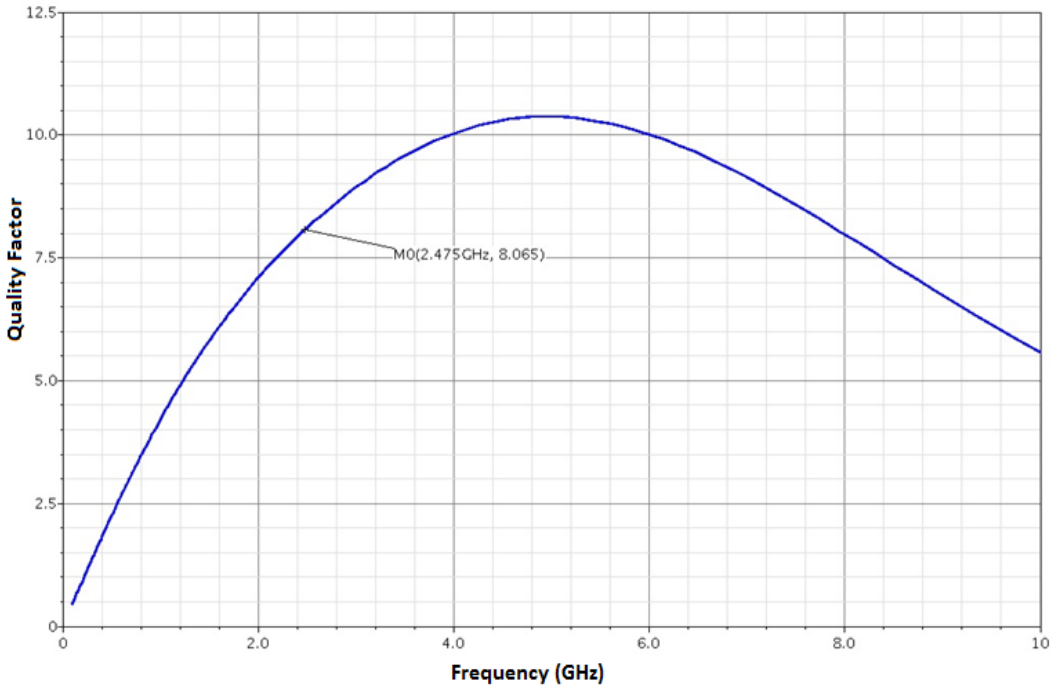

Figure 2.28 : Quality factor simulation of 4.7 nH inductor.

It can be seen that for 2.4 GHz, the quality factor of inductor is about 8. The series loss of inductor is shown in Figure 2.29 and can be expressed as in Equation **(2.19).**

$$R_{series} = \frac{\omega_0 L}{Q_L} \tag{2.19}$$

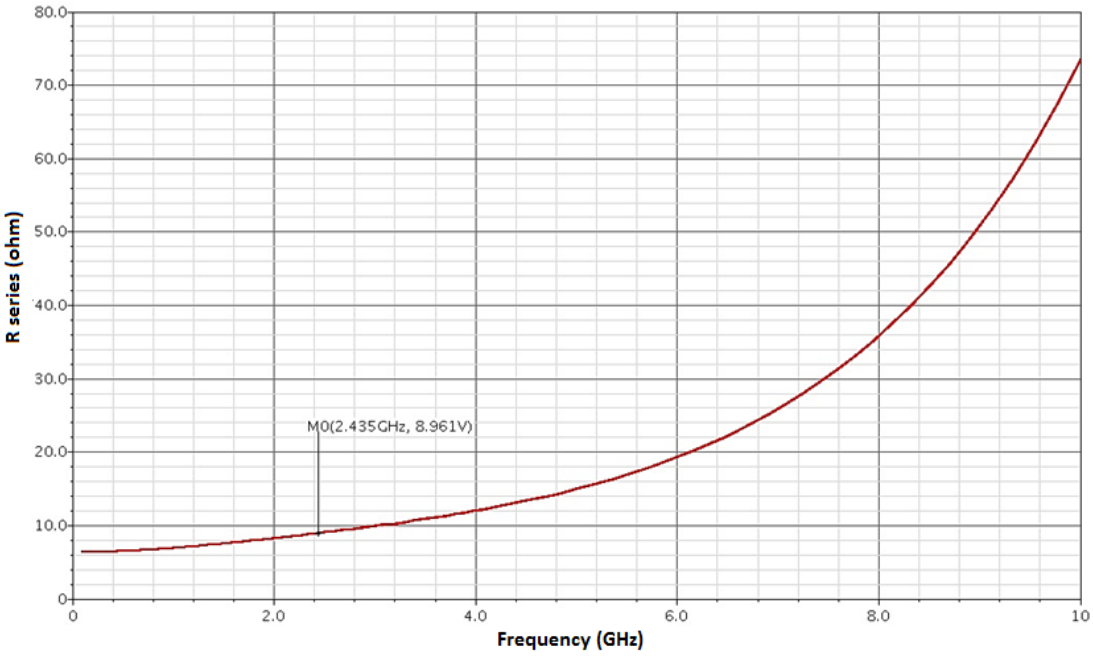

Figure 2.29 : Series resistance of inductor.

Figure 2.29 shows that the series resistance of inductor is about 9 Ω in desired frequency band.

Another important parameter of VCO design is the output voltage swing. High voltage swing is usually desired to reduce phase noise. Equation **(2.20)** shows the output voltage swing relation with inductor.

$$V_{\text{tank}} = I_{bias}\omega_0 L Q_L \qquad \textbf{(2.20)}$$

From Equation **(2.20),** about 1.7 V voltage swing is expected at the output node. The oscillation frequency can be calculated roughly with expression below. It is more complex for high frequency operations.

$$\omega_0 = \frac{1}{\sqrt{LC}}\sqrt{1-\frac{R^2_{series}C}{L}} \qquad \textbf{(2.21)}$$

Using 4.7 nH inductance with about 9 ohm series resistance and 1 pF capacitance, oscillation frequency is calculated as about 2.32 GHz. This is a rough calculation but shows that the design is near to desired oscillation frequency.

Next step of design is determining dimensions of MOS transistors. The desired g_m value indicates the width of the transistors. Equation **(2.22)** shows the minimum g_m value to obtain stable oscillation at desired frequency.

$$g_m \geq \frac{R_{series}C}{L} \qquad \textbf{(2.22)}$$

From Equation **(2.22),** minimum g_m value is determined as 1.9 mS. However; some points such as process corner, temperature can be considered and should add a safety factor to g_m minimum value. Finally, desired g_m value should be minimum 4 mS for safety and stable oscillation. PMOS and NMOS transistors should have same g_m value to provide symmetric sinusoidal signal at the output.

A basic level 1 MOS model gives the transconductance as;

$$g_M = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{Q_{point}} = \mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{GS}-V_{th}\right) \qquad \textbf{(2.23)}$$

$$r_{ds} = \frac{1}{\lambda I_{dsat}}$$

$$C_{gs} = \frac{2}{3} C_{ox} W L_{channel}, C_{gd} = C_{GD} W \quad \textbf{(2.24)}$$

In Equation **(2.23)** and (**2.24),**

$L_{channel}$ = minimum channel length.

V_t= threshold voltage.

λ = channel length modulation factor.

$C_{ox} = t_{ox}/\varepsilon_{ox}$; t_{ox} = gate oxide thickness.

C_{GD} = gate to drain capacitance per unit gate width.

For today technology in CMOS processes, V_{gs} is selected about 0.4 – 0.5 V higher than threshold voltage. If $V_{gs} – V_t$ is too high, g_m is degraded due to effects such as mobility degradation and velocity saturation effects for channel carriers. If it is too small, the transistor width should be too large that means higher parasitic and wasted area. The transistor width should be determined after some iteration because of secondary effects. G_m and transistor width equations are shown in Equation **(2.25).**

$$W = \frac{g_m L_{channel}}{\mu_n C_{ox} (V_{gs} - V_t)}$$

$$g_m = \frac{1}{r_{ds}} + \frac{R_{series}(C + C_{gs} + 4C_{gd})}{L} \quad \textbf{(2.25)}$$

Finally, the design can be simulated and optimization should be done to reduce phase noise at desired frequency. To reduce phase noise;

- Make Q as high as possible
- Make I_{bias} as large as is design for power dissipation.
- Use minimum g_m of MOSFET to satisfy stable oscillation with safety factor.
- Use minimum length that process allows.

Figure 2.30 shows the transient response of the designed circuit

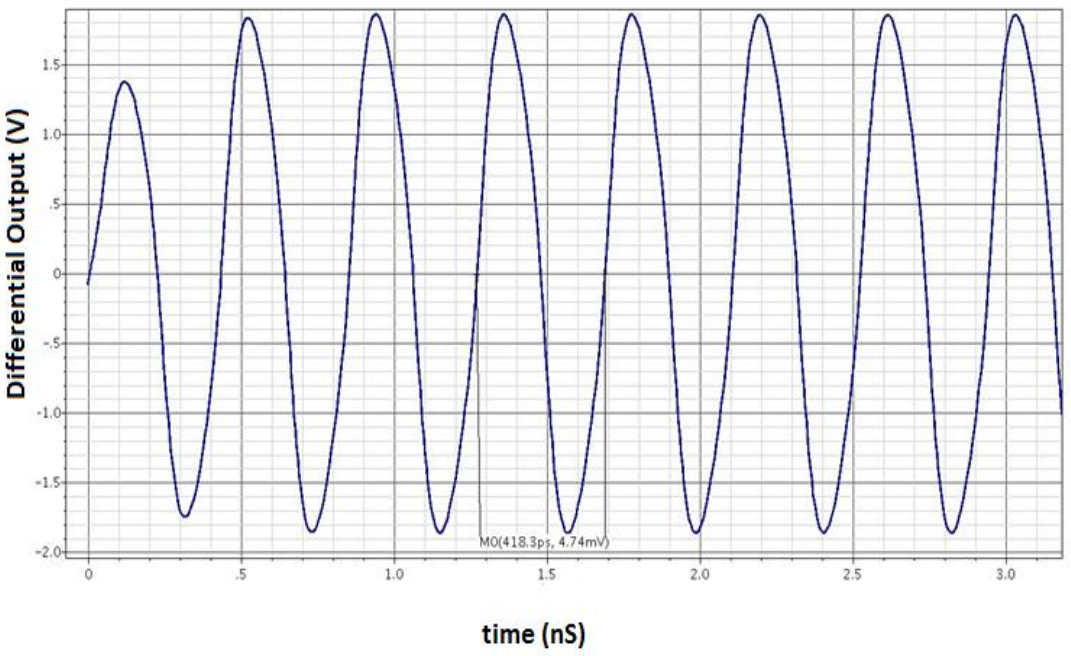

Figure 2.30 : Transient response of LC VCO.

Figure 2.30 shows the output signal and differential voltage swing is 3.5 V at about 2.42 GHz oscillation frequency. The phase noise performance is also shown in Figure 2.31.

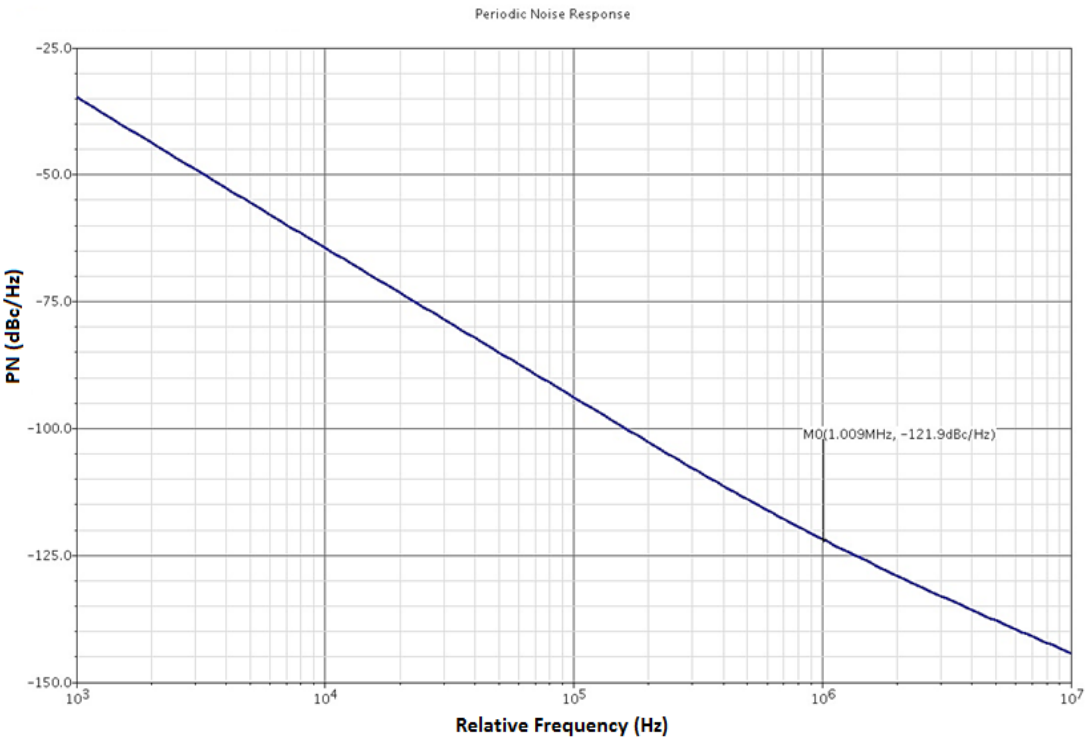

Figure 2.31 : Phase noise performance of LC VCO without varactor.

These results are obtained without varactor. The center frequency is determined and about 0.9 pF capacitance is required for center frequency. For varactor design, PMOS transistors are used in inversion mode.

Designed varactor schematic and its capacitance value with related to V_{tune} voltage is shown in Figure 2.32 below.

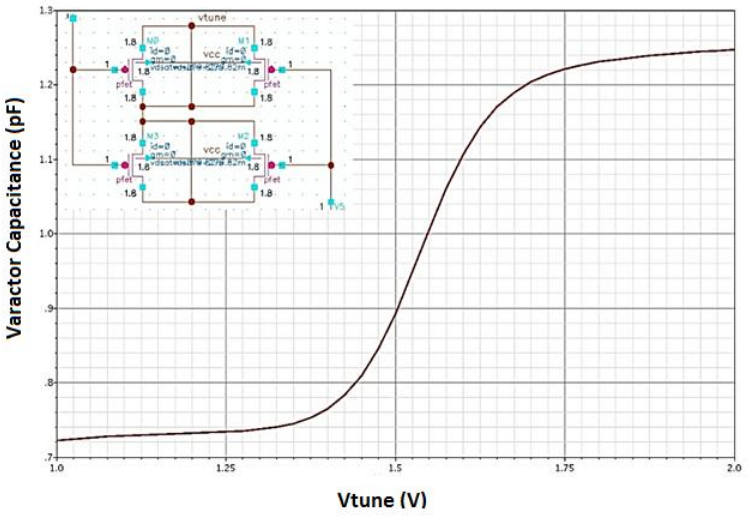

Figure 2.32 : Varacator capacitance versus Vtune.

The length of transistors is chosen as 180nm since it is the minimum length in 0.18µ process. Figure 2.33 shows phase noise comparison of ideal and designed varactor.

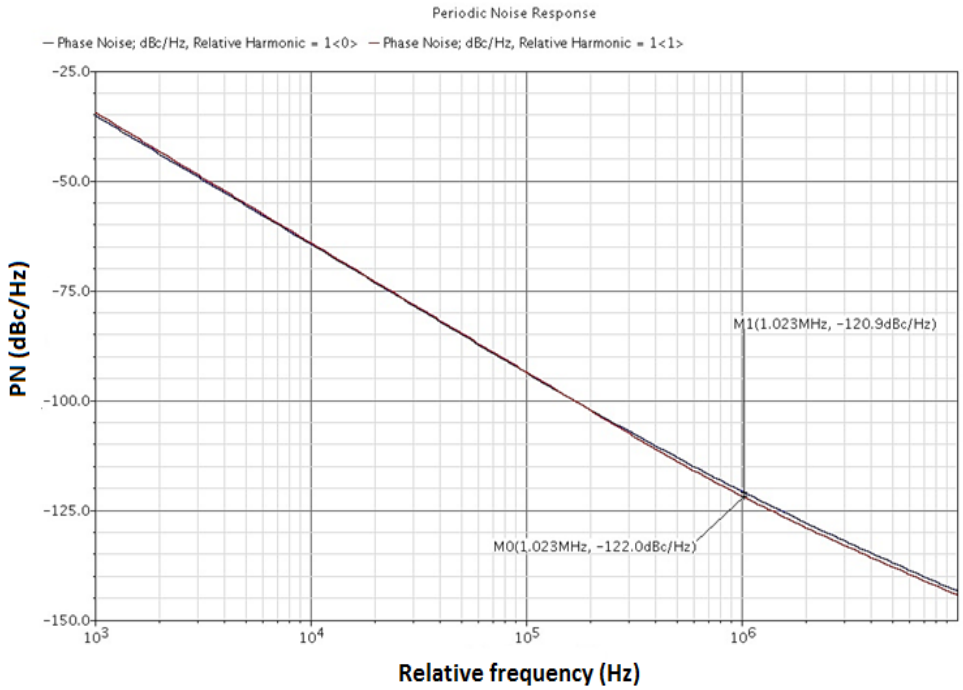

Figure 2.33 : Phase noise comparison with ideal capacitance and varactor.

It looks like loss of the varactor cause about 1 dBc/Hz increase on phase noise @ 1 MHz offset. Figure 2.34 shows the tuning range of VCO.

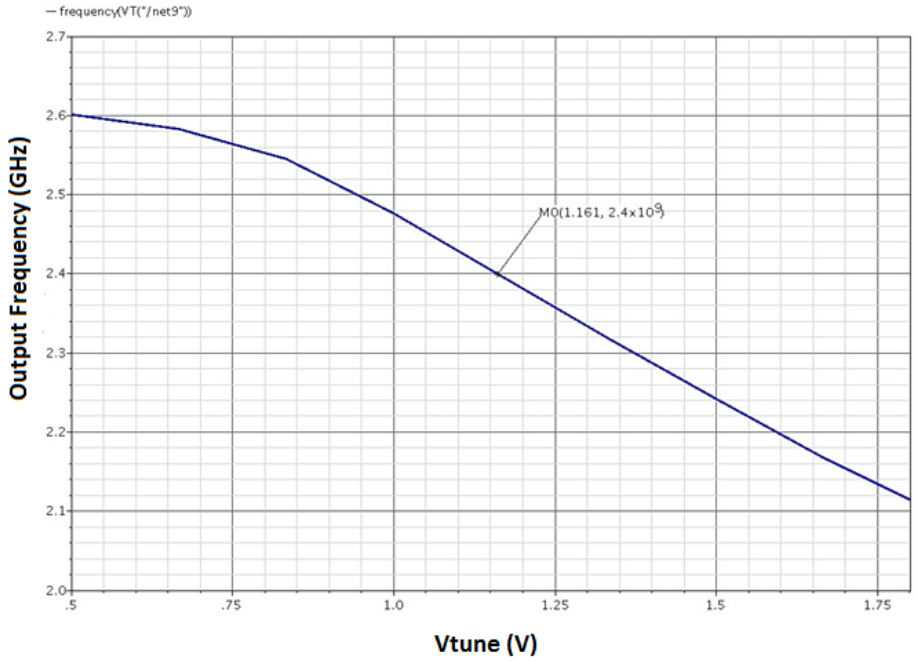

Figure 2.34 : Frequency tuning range of VCO.

From Figure 2.34, tuning range is about 500 MHz that correspond about 20% tuning range. The K_{VCO} is also calculated as 430 MHz/V. The phase noise versus tuning voltage plot is also shown in Figure 2.35.

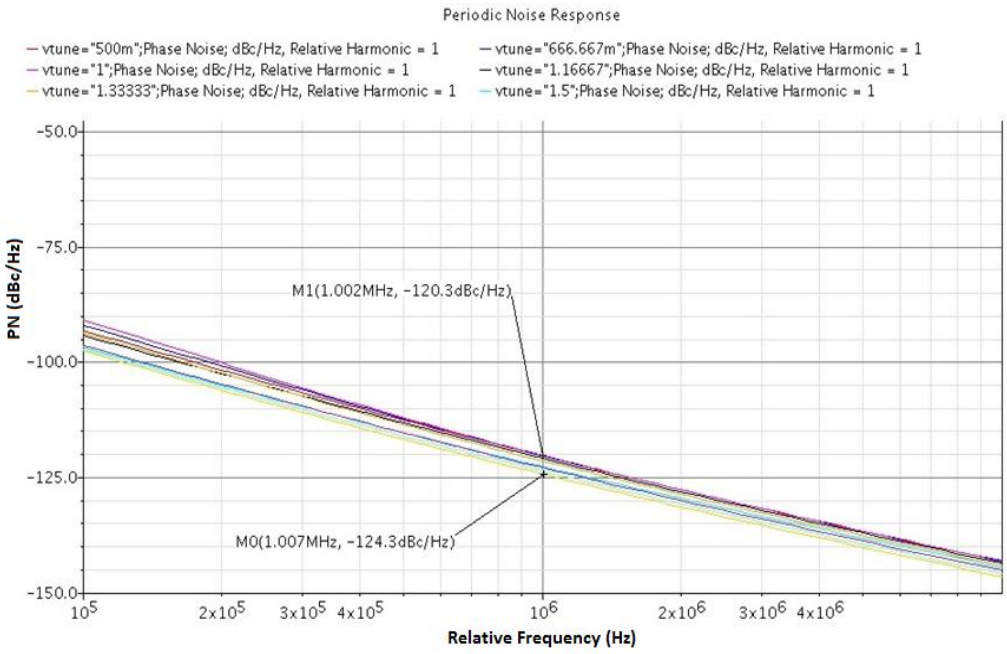

Figure 2.35 : Phase noise versus V_{tune} @ 1 MHz offset.

The phase noise with 1 MHz offset changes 4 dBc/Hz from minimum to maximum oscillation frequency.

The oscillator works in two different regimes, current limited and voltage limited. For low bias currents, it works in current limited regime and increasing the bias current results in increased output voltage swing. However, the tank voltage will be clipped at V_{DD} by the PMOS transistors. Therefore, after that point, increasing bias current cannot change the voltage amplitude. That region is called voltage limited. Phase noise is improved by increasing bias current until the voltage limited region. Figure 2.36 shows the phase noise change related to bias current.

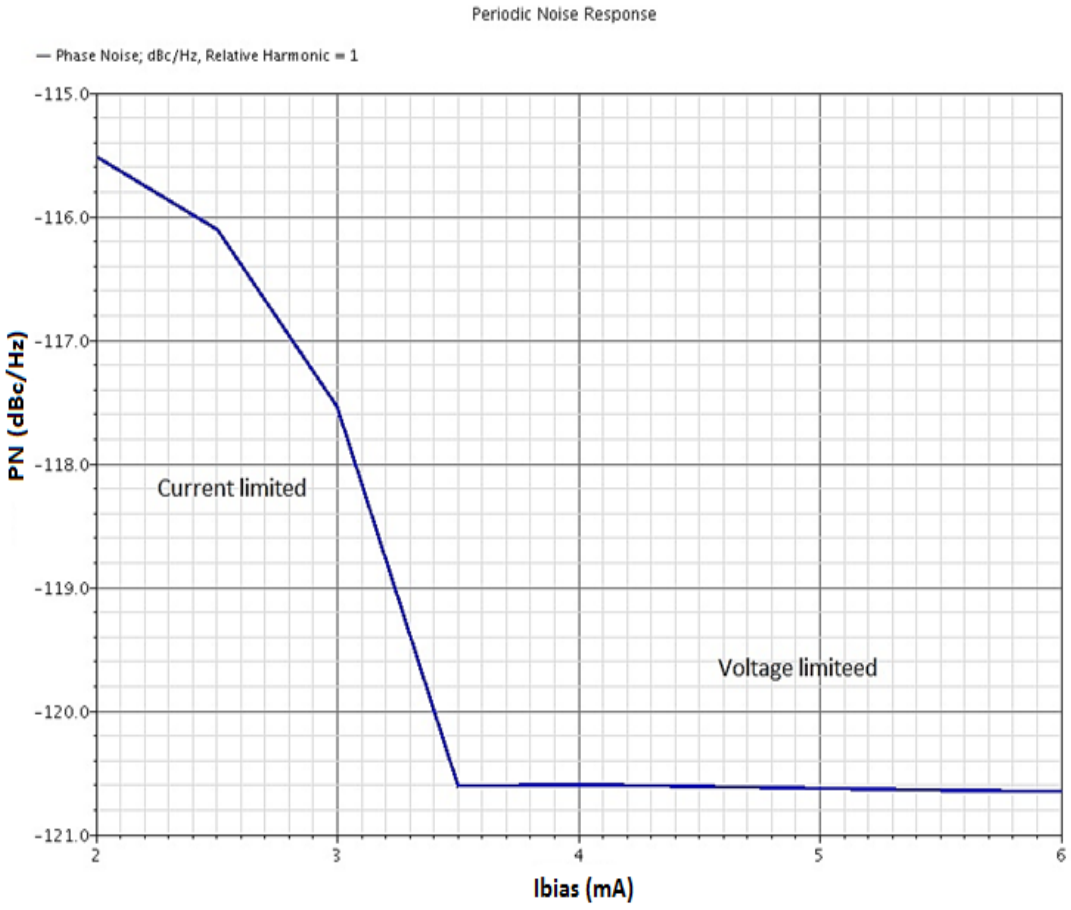

Figure 2.36 : Phase noise with 1MHz offset versus bias current.

Figure 2.36 shows the voltage and current limited regions. It can be seen that, more than about 5 mA bias current is waste of power for this oscillator. The phase noise saturates near 4 mA bias current but it can be chosen a little higher because of temperature and process variations.

The phase noise simulation over temperature is shown in Figure 2.37.

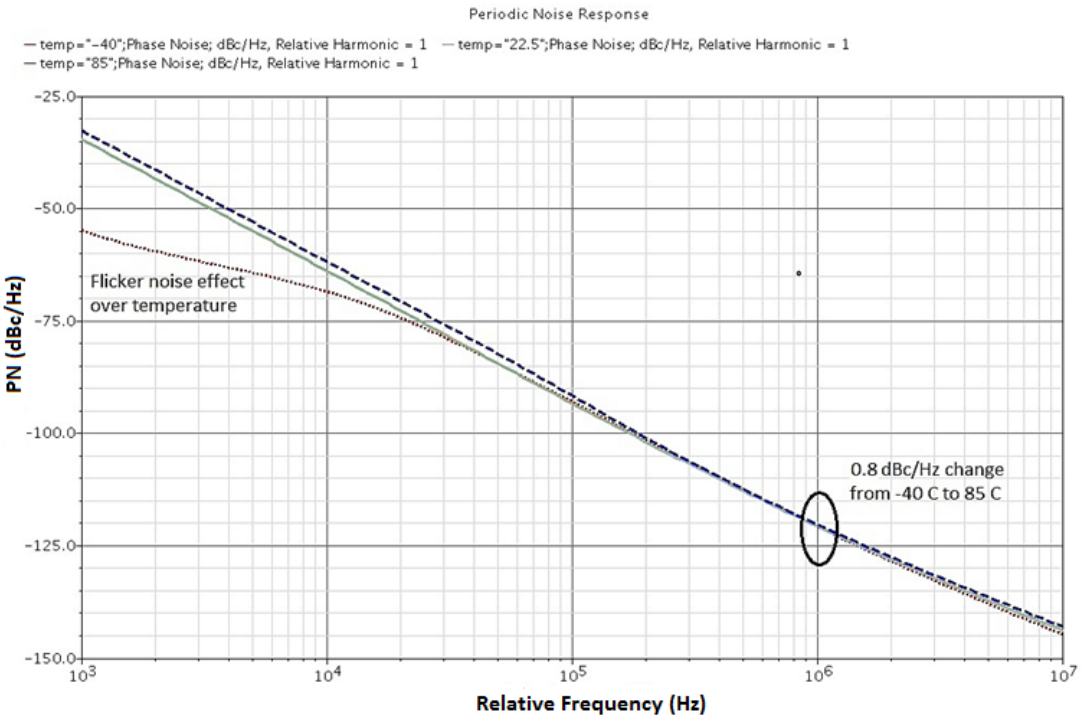

Figure 2.37 : Phase noise over temperature.

It can be seen from Figure 2.37 that, temperature sensitivity is higher in low frequency offsets that corresponds to flicker noise region. Temperature stability of oscillation frequency is shown in Figure 2.38.

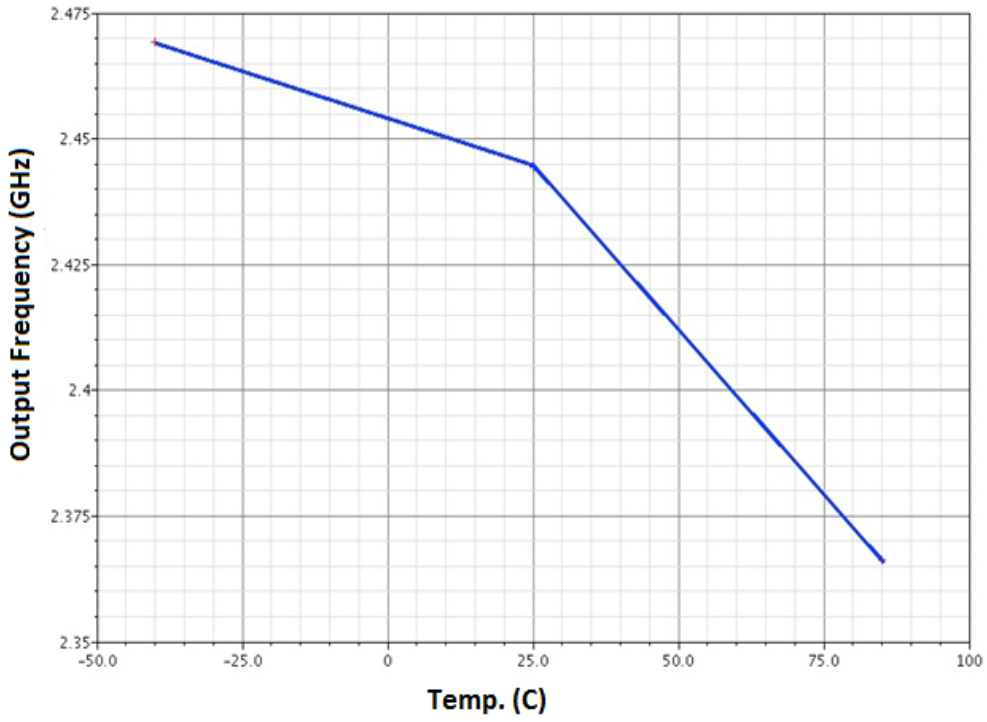

Figure 2.38 : Oscillation frequency over temperature.

The frequency change from -40 ^{0}C to 85 ^{0}C is about 100 MHz for 2.42 GHz oscillation frequency.

Process dependency of circuit is also shown in Figure 2.39 and Figure 2.40.

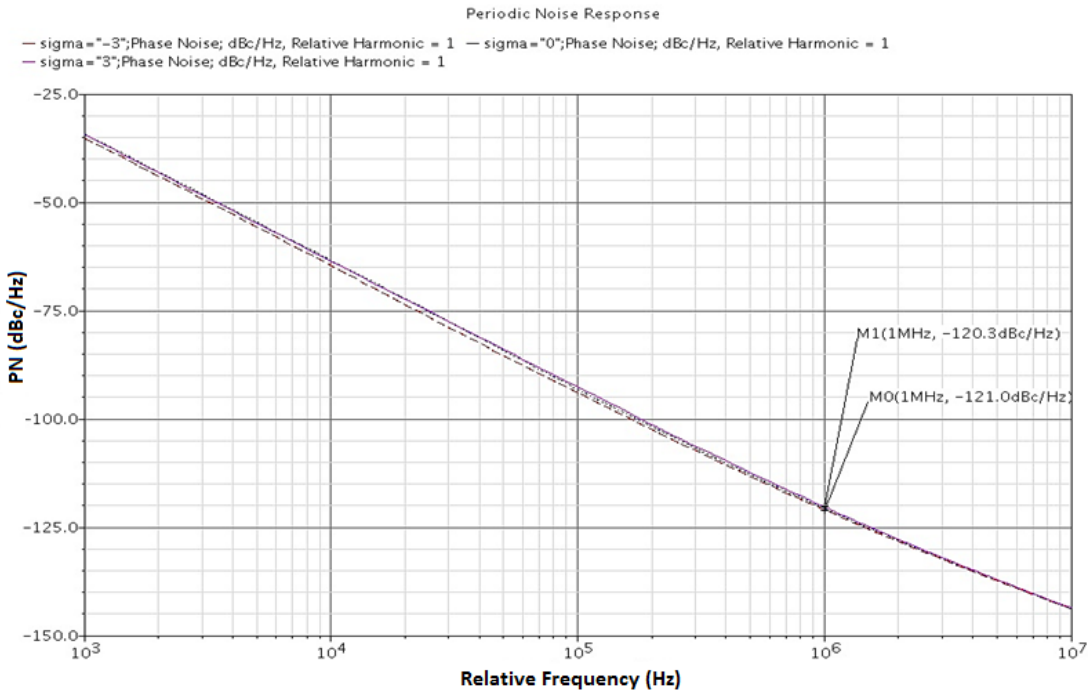

Figure 2.39 : Process corner simulation of phase noise.

Figure 2.39 shows that from -3 sigma to 3 sigma, phase noise changes about 0.7 dBc/Hz. Frequency variation over process is shown in Figure 2.40.

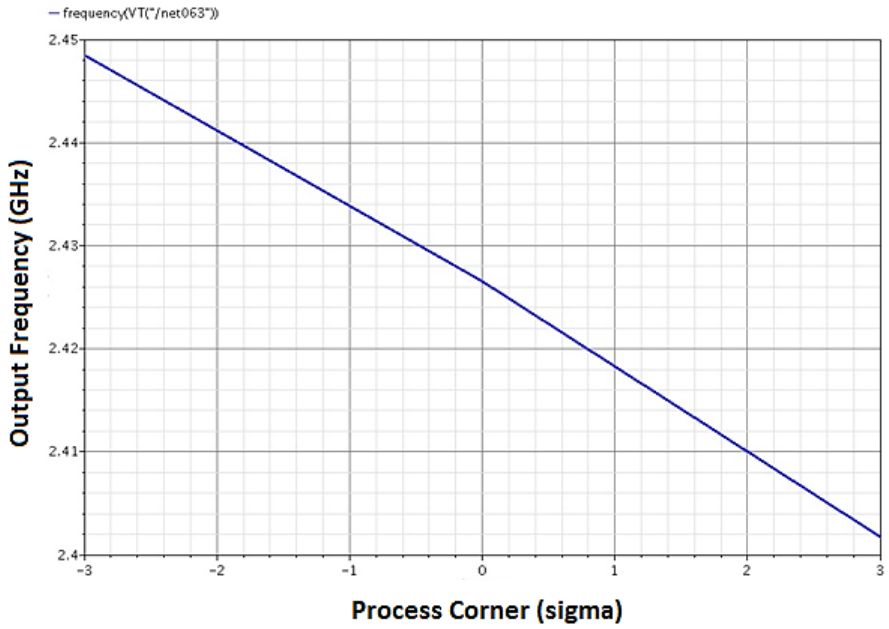

Figure 2.40 : Process corner simulation of oscillation frequency.

Figure 2.40 shows that about 50 MHz frequency variation can occur with respect to process variations.

The dimensions for PMOS transistors are 75µm/ 180nm and for NMOS transistors are 25 µm/180nm. The current mirror NMOS transistors are 500 µm/1µm. Current mirror ratio is about 10 there.

Overall performance of designed LC VCO is summarized in Table 2.1 below.

Table 2-1: Overall performance of designed LC VCO

	This Thesis	**(4)**	**(8)**	**(9)**
VCC	1.8 V	3.3 V	1.8 V	1.5 V
Power Consumption	9 mW	29.7 mW	1.8 mW	10 mW
Oscillation Frequency	2.4 GHz	2.7 GHz	2.2 GHz	1.8 GHz
Tuning Range	2.1 GHz – 2.6 GHz (20%)	433 MHz (18%)	1.94 GHz – 2.55 GHz (55%)	1.14 GHz – 2.46 GHz (73%)
K_{VCO}	430 MHz/V	-	150 MHz/V	270 MHz/V
Phase Noise @ 100 kHz offset	-93 dBc /Hz	-98.9 dBc/Hz	-	-
Phase Noise @ 1 MHz offset	-120 dBc/Hz	TBD	-116 dBc/ Hz	-126.5 dBc/Hz
Technology	0.18 µm	0.35 µm	0.25 µm	0.18 µm

Table 2.1 shows the overall performance of designed LC VCO. It looks that designed circuit has almost similar performance with other designs in literature.

3. RING OSCILLATOR DESIGN

Ring oscillators are composed of a number of inverter-delay cells connected to each other and output of the last stage is connected to input of the first stage. The structure can be single ended or differential. However, in single ended structure, the number of the stages should be odd. Figure 3.1 shows the single ended and differential structures ring oscillator structures.

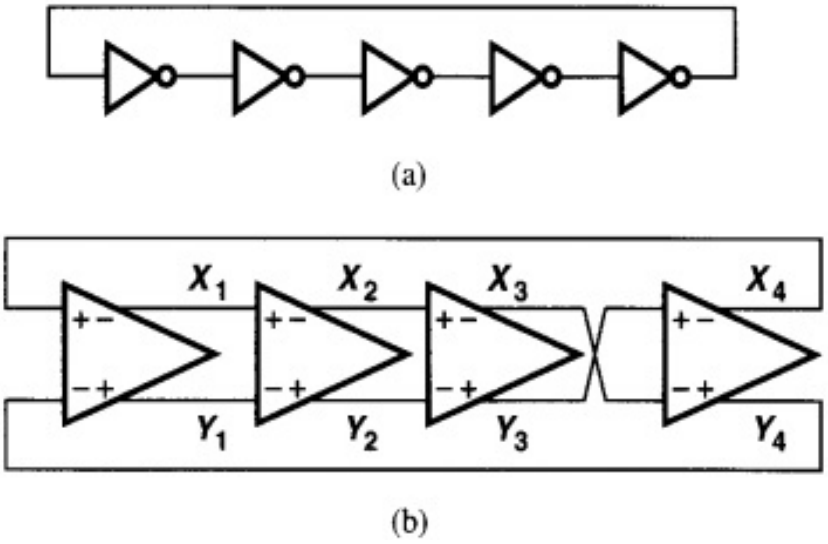

Figure 3.1 : (a) Single ended ring oscillator. (b) Differential ring oscillator [3].

Although, ring oscillator has worse phase noise performance compared to LC VCO, ring oscillators are widely used in RF integrated circuits because of their advantages that are sorted below.

- Easy design with today's integrated technology.
- Allows low voltage design and low power consumption.
- High frequency operation with lower power consumption.
- High electrically tuning range.
- Multiphase output.

Figure 3.2 shows the three stage ring oscillator with basic transistor level implementation.

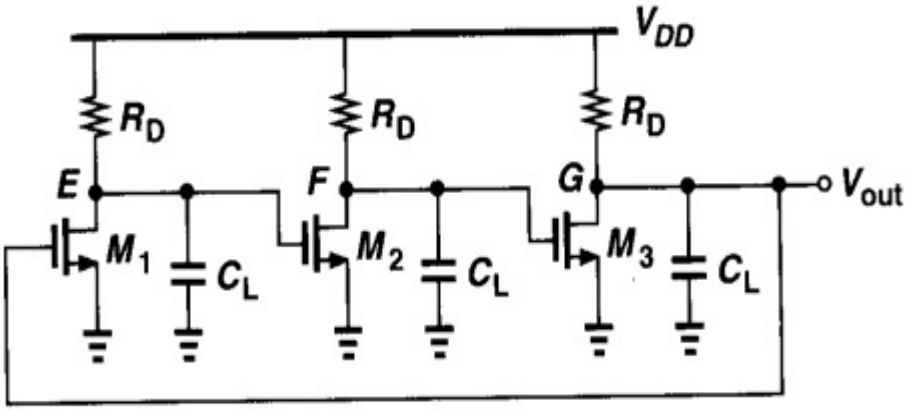

Figure 3.2 : Three stage ring oscillator [3].

The Barkhausen's criteria's are also valid for ring oscillators. Therefore, there is a minimum voltage gain per stage to start oscillation. The total loop gain of three stages can be expressed as Equation **(3.1).**

$$H(s) = -\frac{A_0^3}{\left(1+\frac{s}{\omega_0}\right)^3} \tag{3.1}$$

The total phase shift should be 180^0, therefore in three stages case, 60^0 phase shift should be satisfied to oscillate.

$$\tan^{-1}\frac{\omega_{osc}}{\omega_0} = 60^0 \rightarrow \omega_{osc} = \sqrt{3}\omega_0 \tag{3.2}$$

The loop gain of the oscillator should be one at desired oscillation frequency. Therefore, from Equation **(3.1)** and **(3.2)**, the minimum gain for each stage is obtained as;

$$\frac{A_0^3}{\left[\sqrt{1+\frac{\omega_{osc}}{\omega_0}}\right]^3} = 1 \Rightarrow A_0 = 2 \tag{3.3}$$

As a result, three stage ring oscillator needs two voltage gain per stage to oscillate at $\sqrt{3}\omega_0$ frequency where ω_0 is 3 dB bandwidth of each stage.

The waveforms between the stages are shown in Figure 3.3.

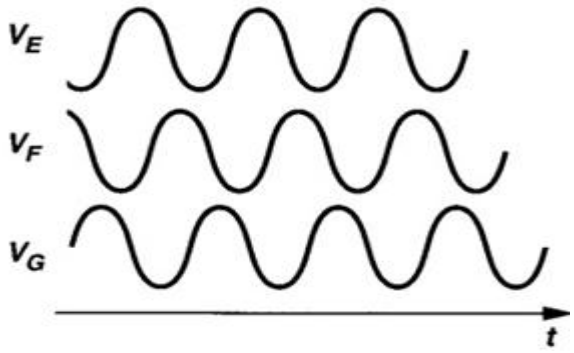

Figure 3.3 : Waveforms in three stage ring oscillator [3].

In Figure 3.3, it can be seen that 60^0 phase shift obtained from each stage. Increasing stage number result in lower minimum gain for each stage but also lower oscillation frequency.

In Figure 3.4, simple CMOS inverter stage is shown with its input and output waveform.

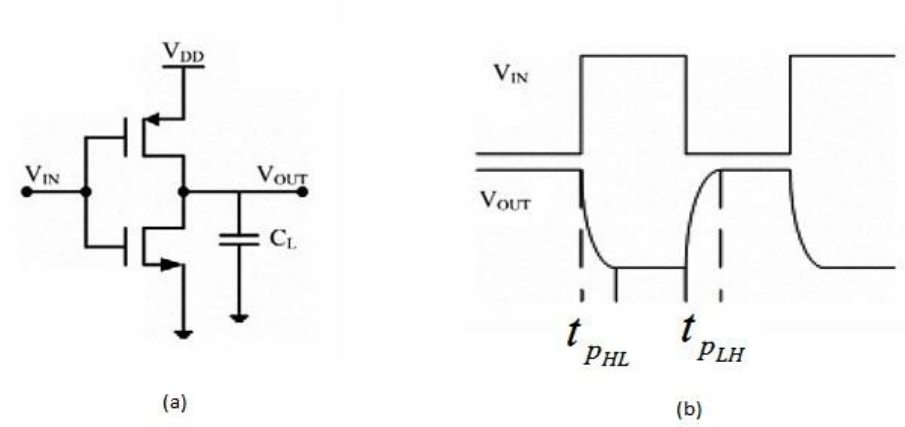

Figure 3.4 : (a) Single ended inverter stage. (b) Input and output waveform [11].

The oscillation frequency of N stages ring oscillator can be expressed as;

$$f_{osc} = \frac{1}{2N\tau} \tag{3.4}$$

The gates to source capacitances are assumed equal for the PMOS and NMOS transistors. Therefore, delay of each cell is calculated in Equation **(3.5).**

$$V_{osc} = \int \frac{I_{ctrl}}{C_L} dt \Rightarrow \tau = \frac{V_{osc} C_L}{I_{ctrl}} \tag{3.5}$$

In Equation **(3.5),** V_{OSC} is the oscillation amplitude. Substituting Equation **(3.5)** into **(3.4)** will give;

$$f_{osc} = \frac{I_{ctrl}}{2NV_{osc}C_L} \tag{3.6}$$

Equation **(3.6)** shows that, oscillation frequency of ring oscillator is related to current, number of stages, load capacitance and oscillation amplitude. For a given process and number of stages, the oscillation frequency can be controlled by I_{ctrl} to provide desired tuning range.

3.1 Analysis of Phase Noise in Ring Oscillators

The phase noise of ring oscillators comes from both intrinsic and extrinsic noise sources. These are up and down converted around of desired oscillation frequency. Intrinsic noise sources include thermal and flicker noises that are operating point depended. Extrinsic noise sources include supply, substrate and control noise.

The quality factor of the ring oscillator is described in reference [10] as;

$$Q_L = \frac{\omega_0}{2}\sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\phi}{d\omega}\right)^2} \tag{3.7}$$

where A and ϕ are amplitude and phase of open loop transfer function and ω_0 is oscillation frequency. In Figure 3.5, a linear model of three stage ring oscillator is shown.

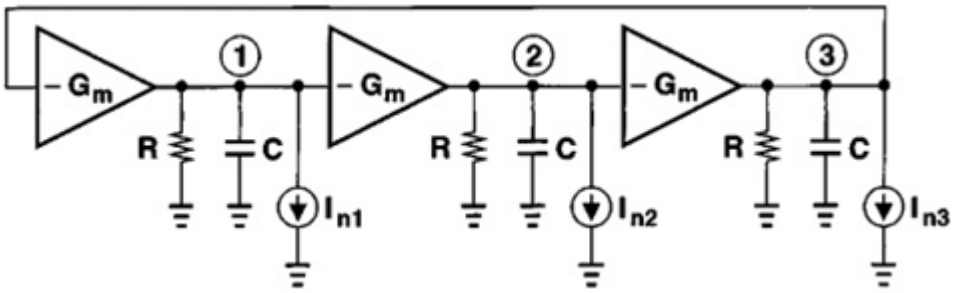

Figure 3.5 : Linearized model of CMOS VCO [3].

The linear approximation allows first order noise analysis. R and C are the output resistance and capacitances of each stage. G_{mR} is required gain for sustained

oscillation. The noise is modeled as current sources named I_n. Each stage should provide 120^0 phase shift with unity gain. Using these conditions, an equation shown in Equation **(3.8),** can be obtained between oscillation frequency and output resistor, capacitor.

$$\omega_0 = \frac{\sqrt{3}}{RC} G_m R = 2 \tag{3.8}$$

Open loop transfer function is shown in Equation **(3.9).**

$$H(j\omega) = \frac{-8}{\left(1 + j\sqrt{3}\frac{\omega}{\omega_0}\right)^3} \tag{3.9}$$

From Equation **(3.9),** $|dA/d\omega| = 9/4\omega_0$ and $|d\phi/d\omega| = 3\sqrt{3}/4\omega_0$. Therefore, Q_L for a three stage ring oscillator is calculated from Equation **(3.7)** as $3\sqrt{3}/4 \approx 1.3$. The more detailed analysis is shown in reference [10].

Total noise power is shown in Equation **(3.10)** [10].

$$|V_{ntot}| = 8kT \frac{R}{9}\left(\frac{\omega_0}{\Delta\omega}\right) \tag{3.10}$$

Equation **(3.10)** shows the trade-off between power and phase noise. Output transconductance (G_m) is inversely proportional to phase noise. To reduce the total noise power by N, the power consumption scales up by factor N also for same oscillation frequency and supply voltage.

Our analysis assumes ring oscillator as linear system. However, in real case most of oscillators are non-linear systems and cause noise aliasing. In single ended ring oscillators, active devices switch between ON and OFF conditions. The large swing and fast transition improve the noise performance of these circuits for the following reasons:

- Large signal level improves the signal to noise ratio.
- The devices don't contribute output noise when they are turned off.
- The sharp transition time means less timing jitter caused by noise.

- Device flicker noise is reduced by switching.

In single ended structures, the noise can be decreased with these reasons but it still suffers from power supply and substrate noise. Especially, when high integration is required, so many digital devices can cause high noises with substrate coupling. Therefore, fully differential structures are widely used for low noise designs.

PMOS loaded basic differential delay cell is shown in Figure 3.6.

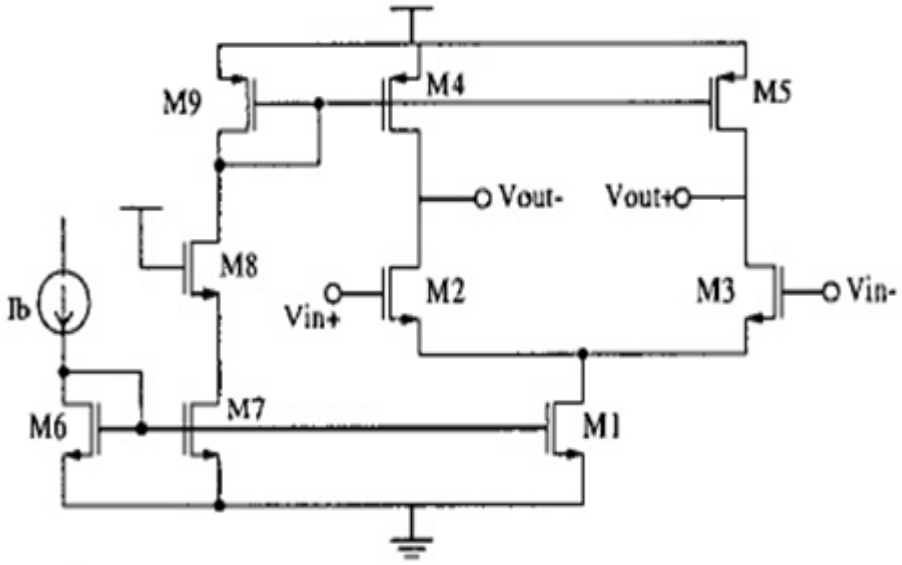

Figure 3.6 : Differential inverter with PMOS load [12].

In differential structure, it is still required to be careful about supply and substrate noises because delay stages have poor common mode rejection when they are in unbalanced state. Also, input transistors suffer from substrate noise because of body effect but this can be solved with using deep n-well devices at the input.

3.2 Design of Differential Ring Oscillator

In this section, 2.4 GHz ring oscillator is designed. First of all, differential structure shown in Figure 3.6 is used and symmetric load is added to decrease phase noise.

In these frequency bands, usually three or four stage ring oscillators are preferred. Four stage designs only have advantage to provide quadrature output signal. Otherwise, three stage structure is more useful to reduce number of noise sources. It is desired to have maximum current as 5 mA. Therefore, about 1.7 mA is used for each stage. The overall schematic is shown in Figure 3.7.

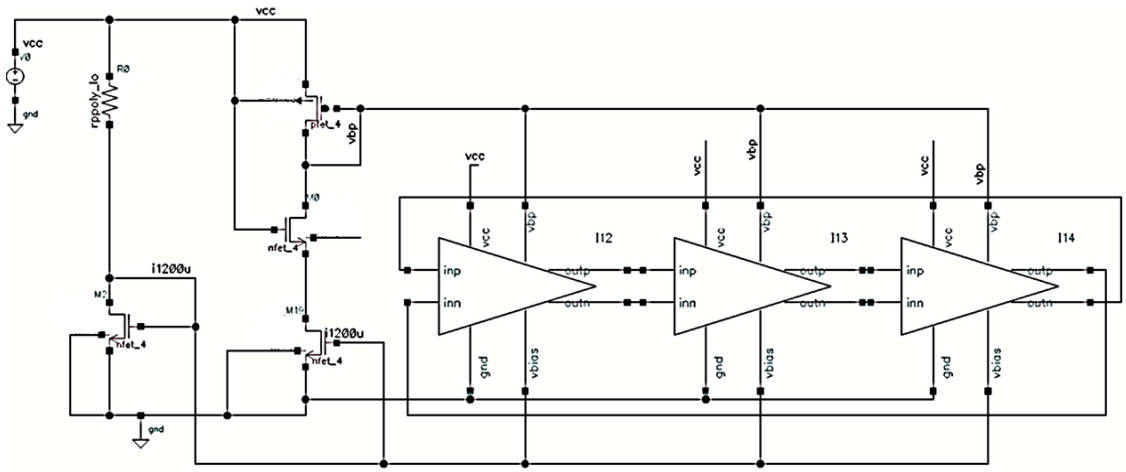

Figure 3.7 : Three stage differential ring oscillator.

Figure 3.7 shows three stage ring oscillator with its basic bias circuit. Output of the each stage is connected to input of the next stage. Supply voltage of the circuit is 1.8 V. Total power consumption is about 9 mW.

Firstly, transient simulation is done for this ring oscillator structure. In simulation world, it is required to add an initial condition on a node in the circuit. Otherwise, the oscillation couldn't start. The transient simulation result is shown in Figure 3.8. The waveform shows differential output of the last stage.

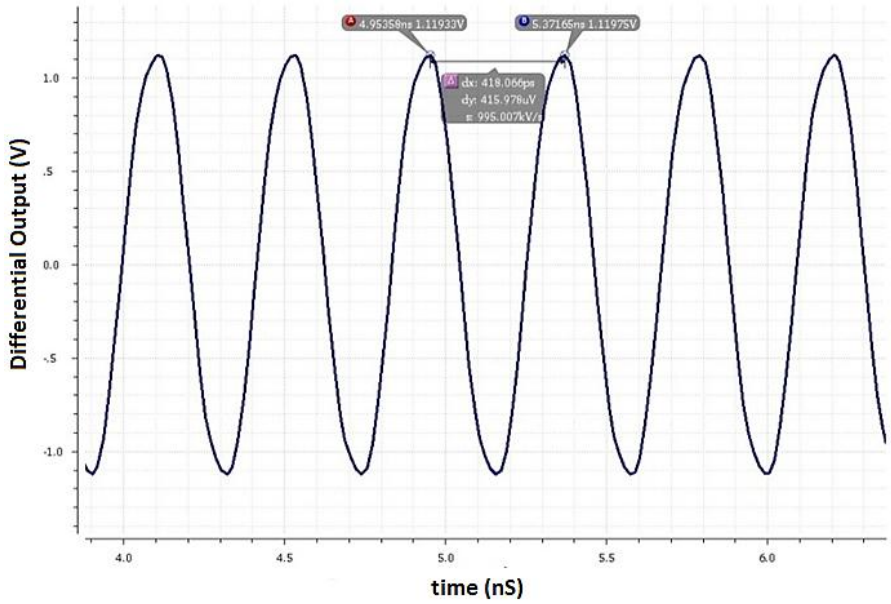

Figure 3.8 : Transient response of ring oscillator.

Figure 3.8 shows that the oscillation frequency is about 2.4 GHz. The common mode node of M2 and M3 is important about phase noise performance. M1 transistor that is

used as a current source in Figure 3.6, should have high output resistance because ringing on this node will cause modulation of current and decrease the performance. Adding about 1.5 pF shunt capacitance to this node improves common mode performance. Transient response of this node is shown in Figure 3.9.

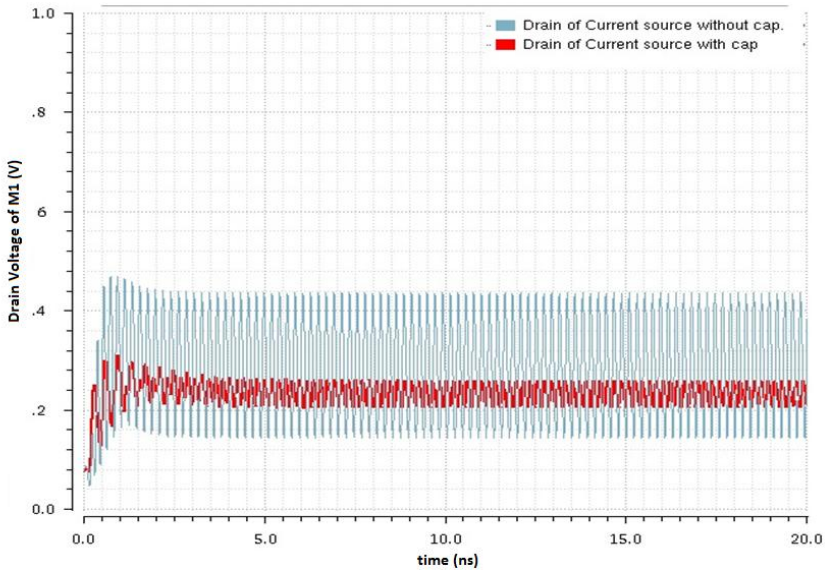

Figure 3.9 : Drain of M1 transistor with and without capacitance.

Phase noise of the circuit is shown in Figure 3.10.

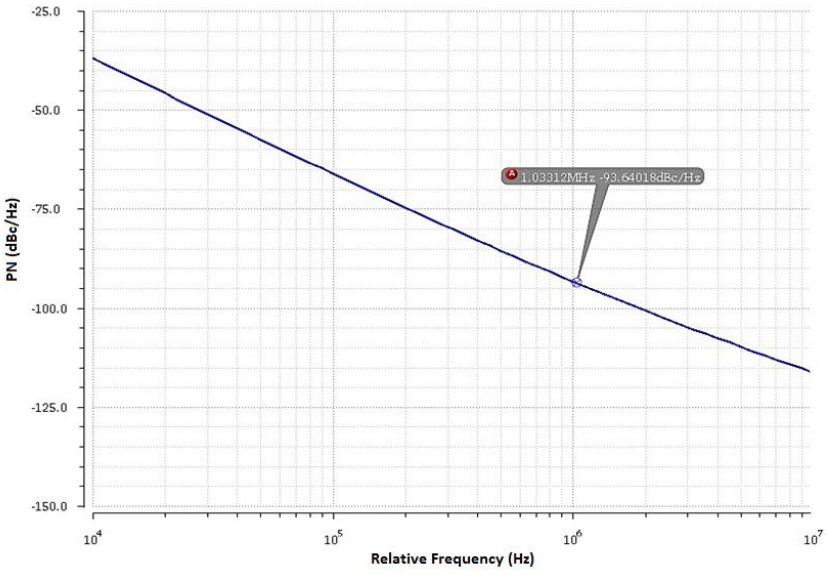

Figure 3.10 : Phase noise performance of ring oscillator.

Simulated phase noise is about -93 dBc/Hz for 1 MHz offset. This noise performance can be improved with changing load structure. Symmetrical PMOS load will provide lower phase noise and better performance to reduce supply sensitivity.

The new schematic of the delay cell with symmetric load is shown in Figure 3.11.

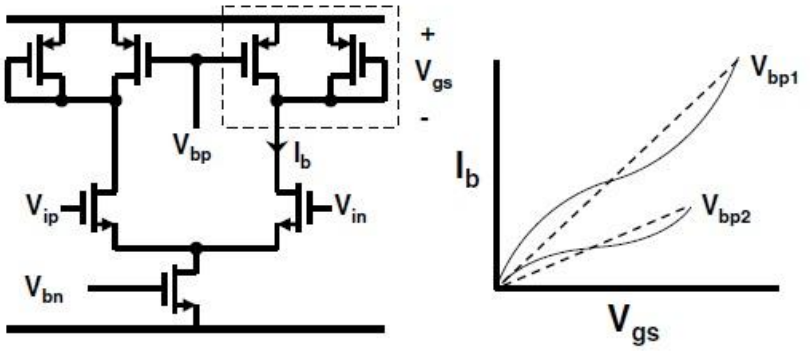

Figure 3.11 : Delay cell with symmetric load [13].

In this structure, the impedance of loads is always equal although the voltages swing change. Therefore, any supply noise becomes common-mode at the output because of this impedance equality and it is rejected by the common-mode rejection of the following delay cell.

V_{gs} voltage and I_b current relationship is simulated for this design and shown in Figure 3.12.

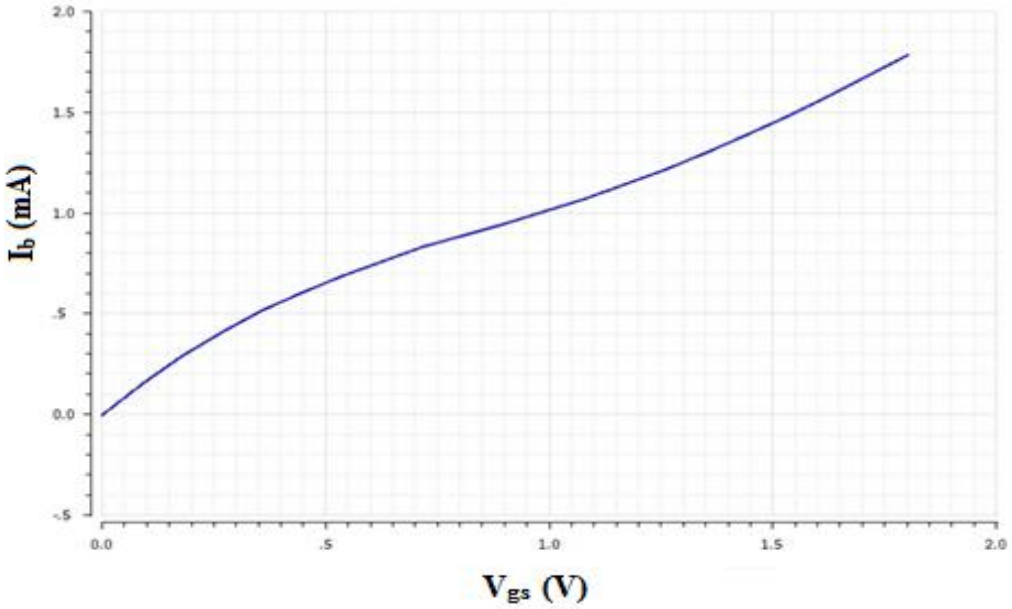

Figure 3.12 : Symmetrical load V_{gs} – I_b curve.

The curve looks like as expected in Figure 3.11. This linear behavior improves the common mode rejection and provides better phase noise. The phase noise analyses are done again for 2.4 GHz oscillation and compared with first case in Figure 3.13

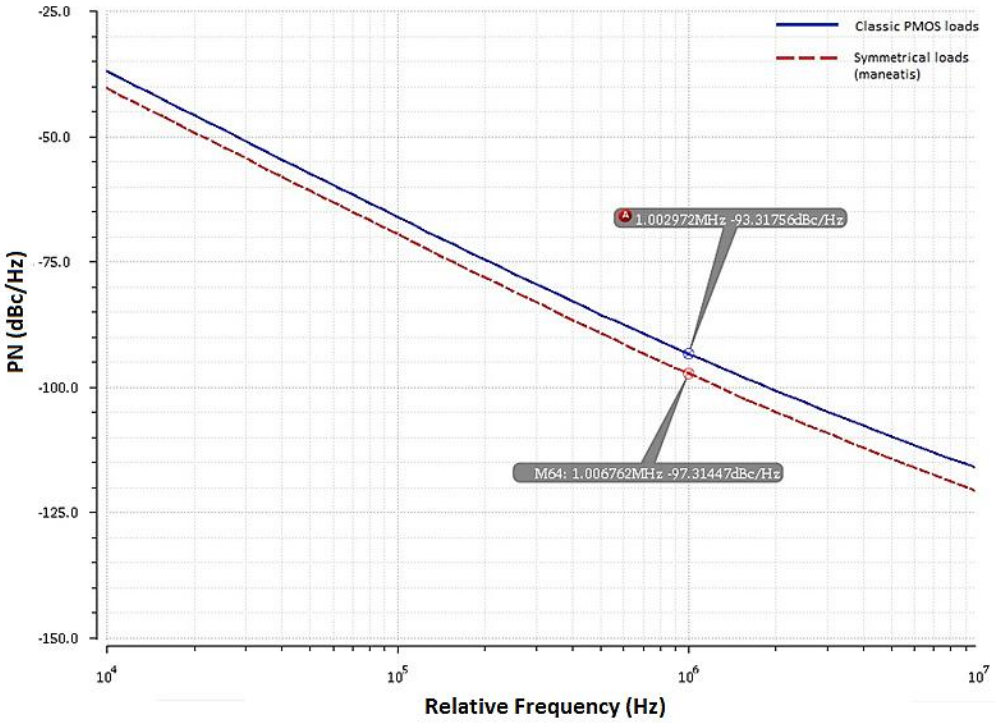

Figure 3.13 : Phase noise comparison, symmetrical load vs. classic PMOS load.

Figure 3.13 shows that about 4 dBc/Hz improvement is obtained for all offset range. The phase noise improved to – 97.3 dBc/Hz for 1 MHz offset at 2.4 GHz oscillation frequency.

Differential output voltage is shown in Figure 3.14.

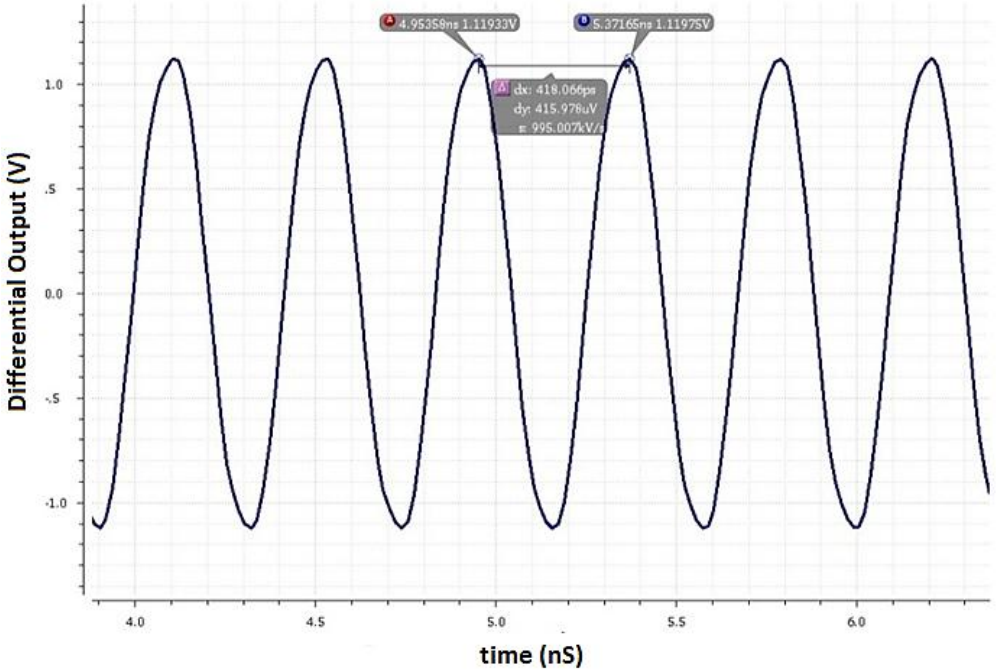

Figure 3.14 : Differential output of ring oscillator.

About 2.3 $V_{peak\text{-}to\text{-}peak}$ differential voltage swing is obtained at the output. One of the advantages of ring oscillator is wide tuning range. The tuning characteristic of oscillator is shown in Figure 3.15.

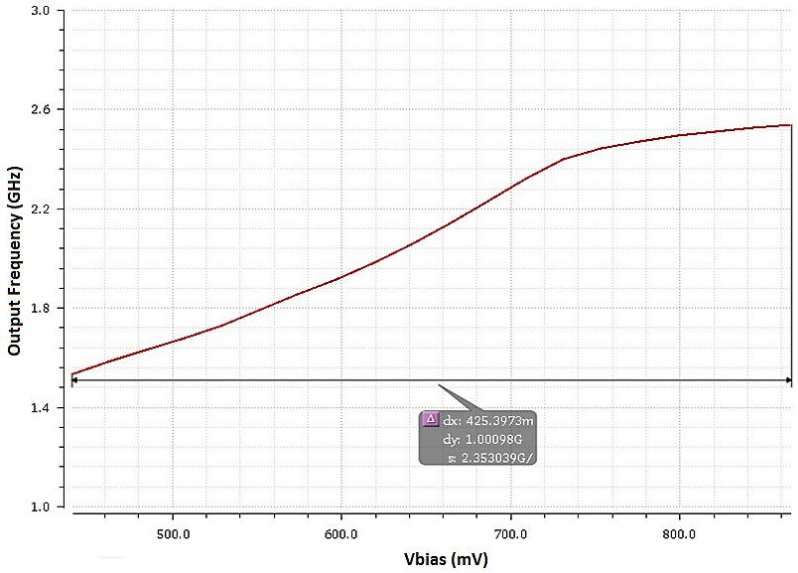

Figure 3.15 : Oscillation frequency versus control voltage.

In Figure 3.15, the ring oscillators can operate from 1400 MHz to 2600 MHz with changing control voltage from 0.3 V to 0.9 V. K_{VCO} of the oscillator is simulated as 2.3 GHz/V. This oscillator can be used for Cellular/3G, WiMAX/4G, Broadband Wireless Access & ISM bands in RF systems.

The phase noise characteristics over different control voltages are shown in Figure 3.16.

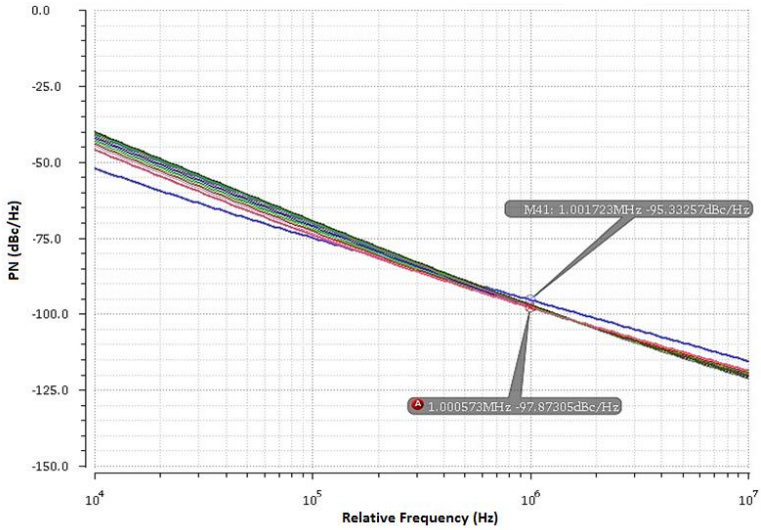

Figure 3.16 : Phase noise over different control voltages.

In Figure 3.16, it can be seen that the phase noise variation at 1 MHz offset is about 2.5 dBc/Hz.

The process, temperature and supply variations are also important for oscillator circuits. In this ring oscillator structure, high sensitivity to temperature and process variations is expected.

Figure 3.17 shows the oscillation frequency over PVT. The X axis shows the ambient temperature and dotted lines show slow and fast corners.

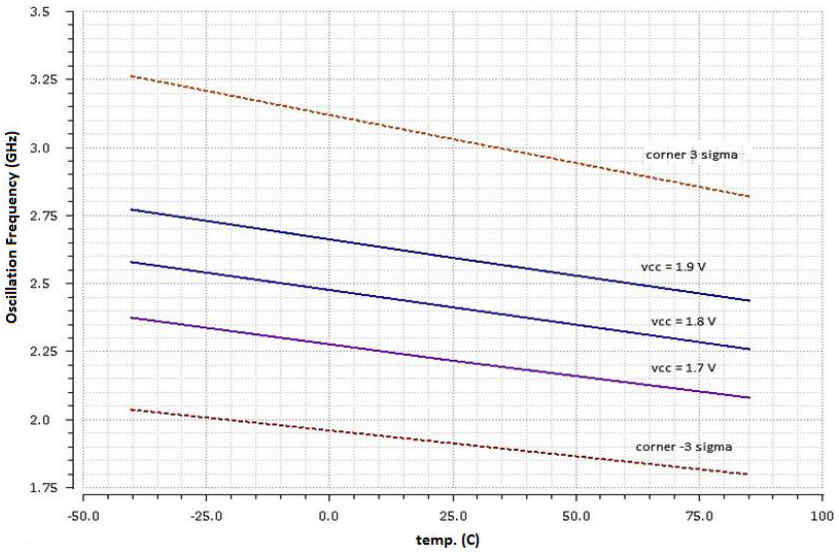

Figure 3.17: Oscillation frequency over PVT.

Ring oscillators frequency stability over PVT is worse than LC oscillators. Therefore, extra biasing circuits with bandgap should be used if the variations are critical. The phase noise characteristic over PVT is shown in Figure 3.18.

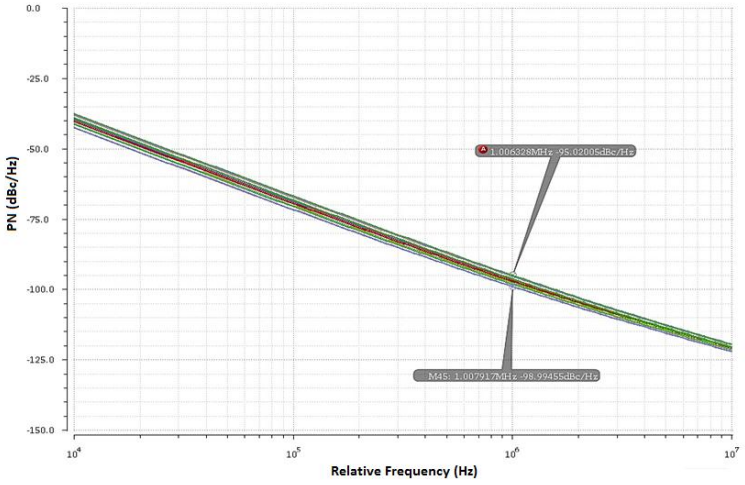

Figure 3.18 : Phase noise simulation over PVT.

Figure 3.18 shows that worst case phase noise at 1MHz offset is 95 dBc/Hz.

In differential delay cell, the dimensions for PMOS transistors are 24μm/ 800nm and for NMOS transistors are 12 μm/180nm. The current mirror NMOS transistors are 80 μm/640μm.

The overall circuit performance is shown in Table 3.1.

Table 3-1: Overall performance of designed Ring VCO

	This Thesis	**(14)**	**(14)**	**(15)**
VCC	1.8 V	-	-	1. 8V
Power Consumption	9 mW	10 mW	20 mW	16 mW
Oscillation Frequency	2.4 GHz	2.4 GHz	1.8 GHz	0.9 GHz
Tuning Range	1.4 GHz – 2.6 GHz	2 GHZ – 2.8 GHz	1.4 GHz – 2.2 GHz	0.4 GHz – 1.4 GHz
K_{VCO}	2300 MHz/V	-	-	
Phase Noise @ 600 kHz offset	-92 dBc /Hz	-	-	- 90 dBc/ Hz
Phase Noise @ 1 MHz offset	-97.3 dBc/Hz	-95.2 dBc/Hz	-100 dBc/Hz	-
Technology	0.18 μm	0.25 μm	0.25 μm	0.18 μm

From Table 3-1, overall performance is satisfying. If the wide tuning range is required, this ring oscillator looks very suitable structure.

4. RC BPF BASED OSCILLATOR DESIGN

In ring oscillator structures, more than one stage is required to obtain sufficient phase shift for oscillation because low pass load is used there. If band pass load is used, required phase shift can be obtained using only one stage. In this structure the oscillation frequency is determined by BPF that is consisted of lumped resistor and capacitor. In this structure, the oscillation frequency is less sensitive to power supply noise.

Wien-bridge oscillator structure is an example that uses BPF load. It is shown in Figure 4.1 (a).

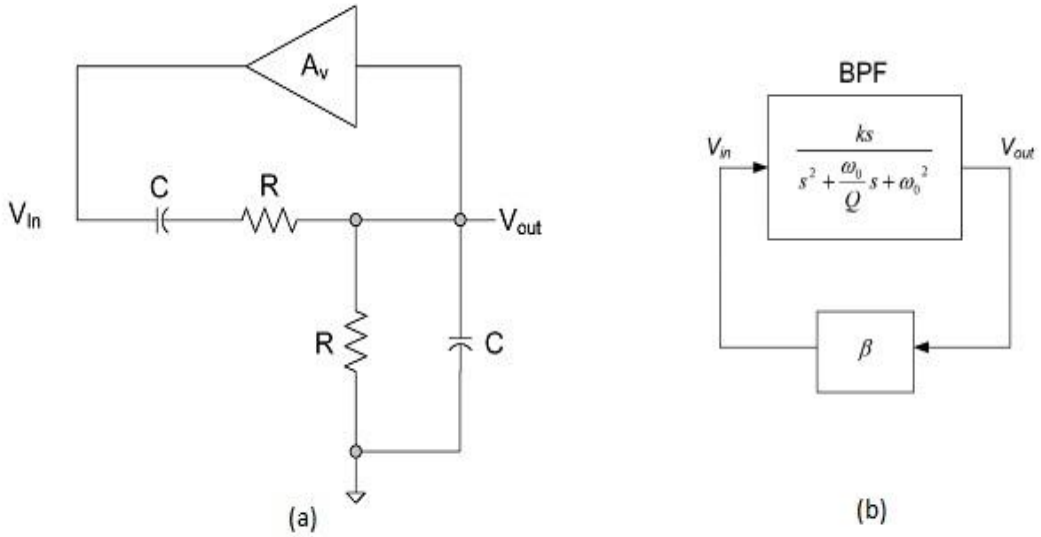

Figure 4.1 : (a) Wien-bridge oscillator. (b) BPF second order model [16].

In Wien-bridge oscillator structures, bandwidth of the used operational amplifier is critical to determine RF performance of oscillator. Therefore, they can't reach high oscillation frequencies.

The BPF can be modeled as second order system that shown in Figure 4.1(b). The center frequency is ω_0 and quality factor is Q. The system has one zero at DC and two poles. These poles cross with zero at center frequency. Nyquist and Bode plots of the system are shown in Figure 4.2.

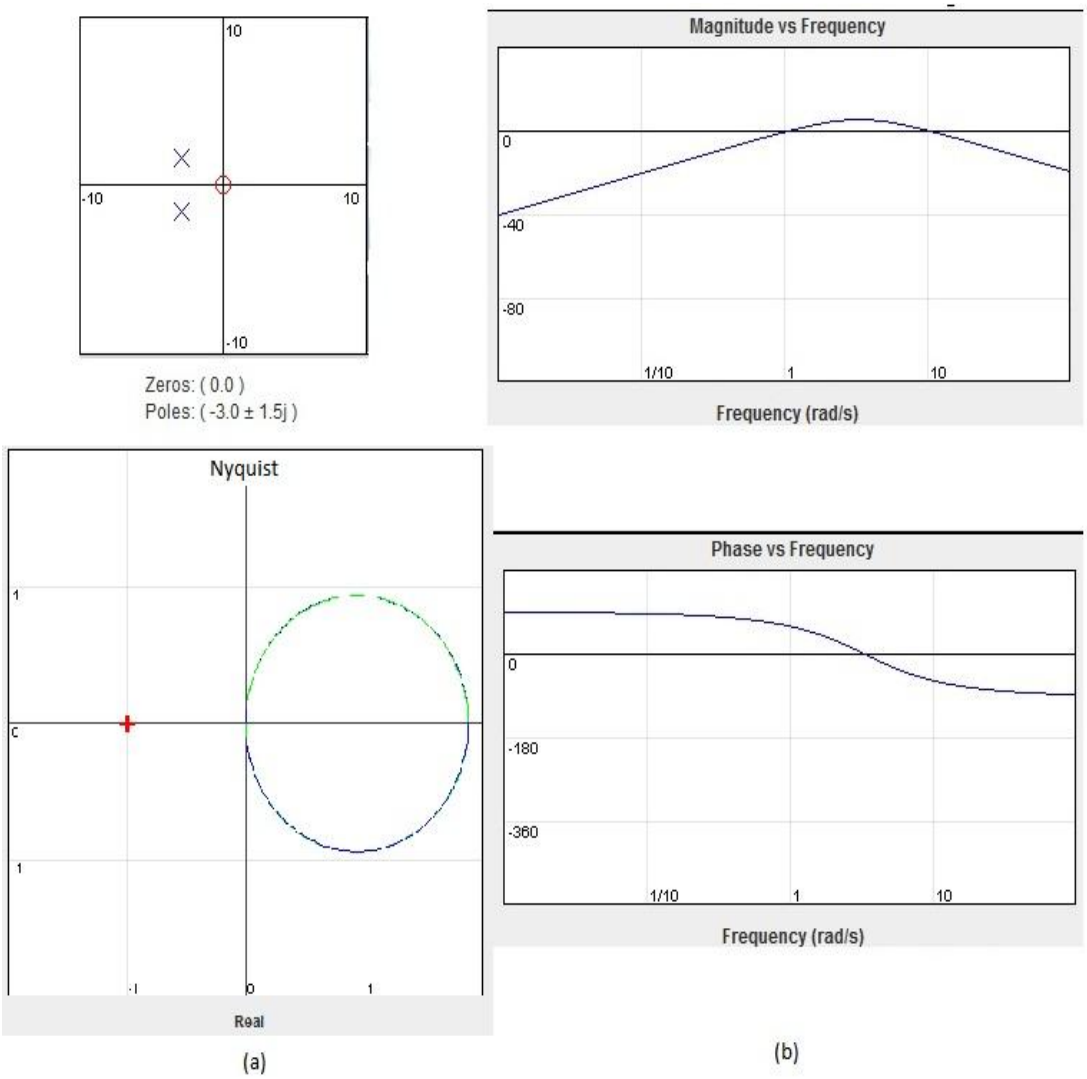

Figure 4.2 : (a) BFP Nyquist plot. (b) BPF Bode plot.

The positive feedback with β loop gain pushes the poles from left-half plane to right-half plane that provides oscillation. The oscillation frequency can be controlled by changing center frequency of BPF.

In Figure 4.1(a), the voltage gain is provided by OPAMP. For low frequency operation, the oscillation frequency can be expressed as 1/RC and oscillation condition is A_v>3. In this structure, the gain-bandwidth product of OPAMP determines the maximum reachable frequency that is about 16.67% of GBP. Therefore, Wien-bridge oscillators aren't useful for high frequency oscillations.

An OTA can be used as gain block to operate higher frequencies because it has low output impedance and can be implemented by simpler structures. Single ended and differential structures are shown in Figure 4.3.

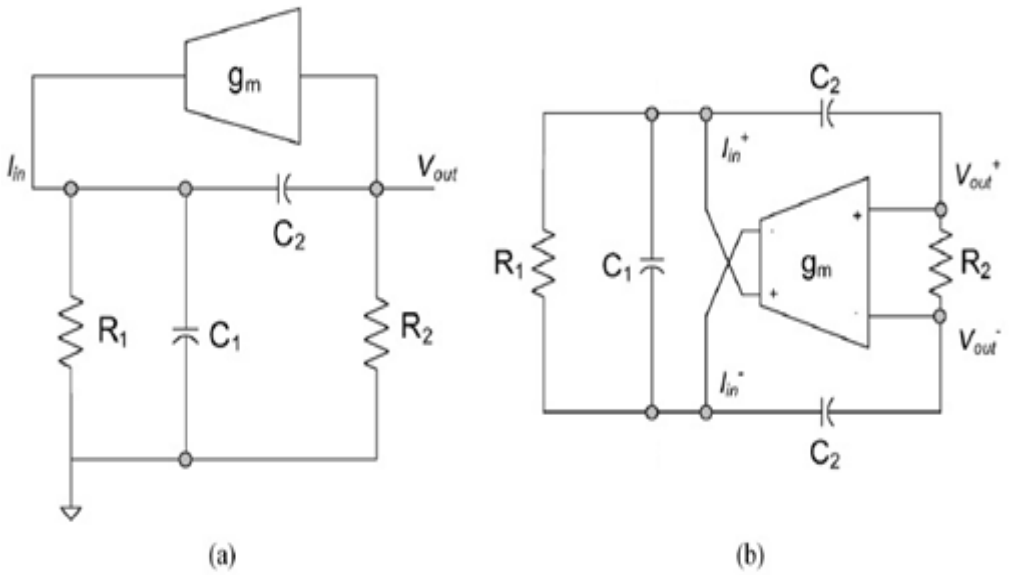

Figure 4.3 : (a) Single ended structure. (b) Differential OTA-RC oscillator [16].

The open loop transfer function of the band-pass filter is shown below.

$$H(s)=\frac{V_{out}}{I_{in}}=\frac{\frac{1}{C_1}s}{s^2+\frac{1+C_1/C_2+R_2/R_1}{R_2C_1}s+\frac{1}{R_1C_1R_2C_2}} \tag{4.1}$$

Transconductance of the OTA should be greater than minimum required gain to start oscillation. The positive feedback of the structure provides at the RHP closed loop poles that cause oscillation. Applying Barkhausen's phase and gain criteria to transfer function, oscillation frequency and oscillation condition is obtained as;

$$\omega_0=\frac{1}{\sqrt{R_1C_1R_2C_2}},\quad g_m\geq\frac{1+C_1/C_2+R_2/R_1}{R_2} \tag{4.2}$$

The quality factor is also another important parameter that determines the phase noise performance of the oscillator. It is expressed in Equation **(4.3).**

$$Q=\frac{\sqrt{(C_1/C_2)(R_2/R_1)}}{1+C_1/C_2+R_2/R_1} \tag{4.3}$$

It can be seen from Equation (4.3) that, the maximum Q number can be 0.5 when C_1/C_2 and R_1/R_2 ratios go to infinity. This shows that, phase noise performance cannot reach LC oscillators but it can be preferred to ring oscillators.

If the C_1 and R_1 values are chosen very high to reduce noise, very high transconductance is also required as oscillation condition. If capacitors and resistors values are chosen equal as C and R, the circuit parameters becomes as;

$$\omega_0 = \frac{1}{RC}, \quad g_m \geq \frac{3}{R}, \quad Q = \frac{1}{3} \tag{4.4}$$

These formulations can be used as a start of desired oscillator design. However, the parasitic capacitances of transistors should be also considered because it affects oscillation frequency and transconductance.

4.1 Further Analysis of OTA-RC Oscillator

4.1.1 Noise analysis

The oscillator structure is further analyzed to determine optimum resistor and capacitor values in this section. The reference [16] includes all these analysis more detailed. Two different parameters are defined to provide constant oscillation frequency. Equation **(4.5)** shows these parameters.

$$k_R = \frac{R}{R_1} = \frac{R_2}{R}, \quad k_C = \frac{C_1}{C} = \frac{C}{C_2} \tag{4.5}$$

The product of the resistors and capacitors are constant to fix oscillation frequency. The circuit parameters can be expressed with k_R and k_C.

$$\omega_0 = \frac{1}{RC}, \quad Q = \frac{k_R k_C}{1 + k_R{}^2 + k_C{}^2}, \quad gm \geq \frac{1 + k_R{}^2 + k_C{}^2}{k_R R} \tag{4.6}$$

The linearized model of the OTA-RC structure is shown in Figure 4.4.

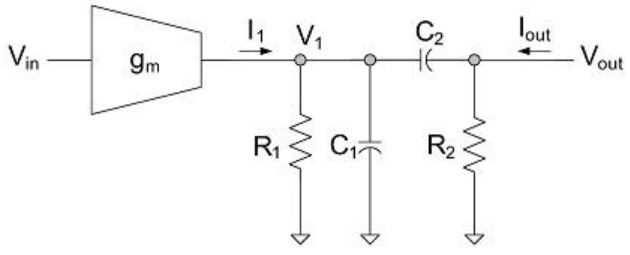

Figure 4.4 : Linearized open-loop model of OTA-RC Oscillator [16].

For the calculation of total noise at V_1 node, current transfer function from I_{out} to I_1 is required because of R_2 noise contribution. This transfer function is expressed in Equation **(4.7).**

$$\left|\frac{I_1}{I_{out}}(j\omega_0)\right| = (1+k_C{}^2)^2 + k_R{}^2 k_C{}^2 \qquad \textbf{(4.7)}$$

There are two different resistors and an active device in linearized model. Therefore, total noise power can be calculated with adding these three different noise sources.

Figure 4.5 shows the individual noise sources in linearized model.

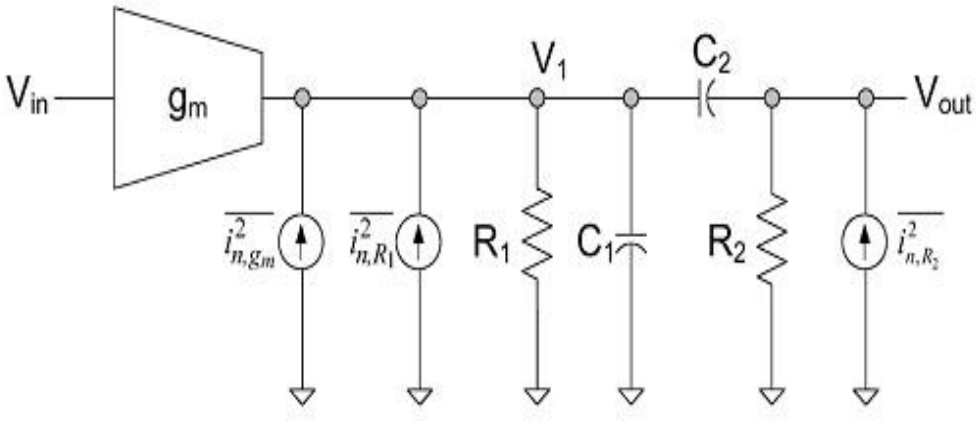

Figure 4.5: Noise current sources in OTA-RC oscillator [16].

Total noise current is expressed in Equation **(4.8).**

$$\overline{I^2_{1,total}} = \frac{4kT}{R_1} + 4kT\gamma g_m + \frac{4kT}{R_2}((1+k_C{}^2)^2 + k_R{}^2 k_C{}^2) \qquad \textbf{(4.8)}$$

Using Equation **(4.6)** and **(4.8),** input referred noise voltage is shown in Equation **(4.9).**

$$\overline{V^2_{in,total}} = \frac{\overline{I^2_{1,total}}}{g^2_{m,\min}} = \frac{4kTk_R{}^2}{(1+k_R{}^2+k_C{}^2)}(1+k_C{}^2+\gamma)(k_R + \frac{1+k_C{}^2}{k_R}) \qquad \textbf{(4.9)}$$

The noise power spectral density in linear oscillator systems is expressed as Equation **(4.10)** [10].

$$\left|\frac{V_{out}}{V_{in}}[\,j(\omega_0+\Delta\omega)]\right|^2=\frac{1}{4Q^2}(\frac{\omega_0}{\Delta\omega})^2 \qquad \textbf{(4.10)}$$

Total output noise voltage can be calculated using Equation **(4.10), (4.9)** and **(4.6).**

$$\left|V_{out}[\,j(\omega_0+\Delta\omega)]\right|^2=\frac{kTR}{k_C{}^2}(1+k_C{}^2+\gamma)(k_R+\frac{1+k_C{}^2}{k_R})(\frac{\omega_0}{\Delta\omega})^2 \qquad \textbf{(4.11)}$$

Equation **(4.11)** is important expression to optimize phase noise and power consumption of designed oscillator. Minimum transconductance and noise is achieved under the condition that is shown in Equation **(4.12).**

$$k_R{}^2=1+k_C{}^2 \qquad \textbf{(4.12)}$$

Using Equation **(4.12),** output noise and minimum required transconductance is simplified as;

$$\left|V_{out}[\,j(\omega_0+\Delta\omega)]\right|^2=\frac{kTR}{k_C{}^2}(1+k_C{}^2+\gamma)(2\sqrt{1+k_C{}^2})(\frac{\omega_0}{\Delta\omega})^2,\quad g_{m,\min}=\frac{2k_C{}^2}{R\sqrt{1+k_C{}^2}} \qquad \textbf{(4.13)}$$

Figure 4.6 shows the variation of these parameters with related to k_C.

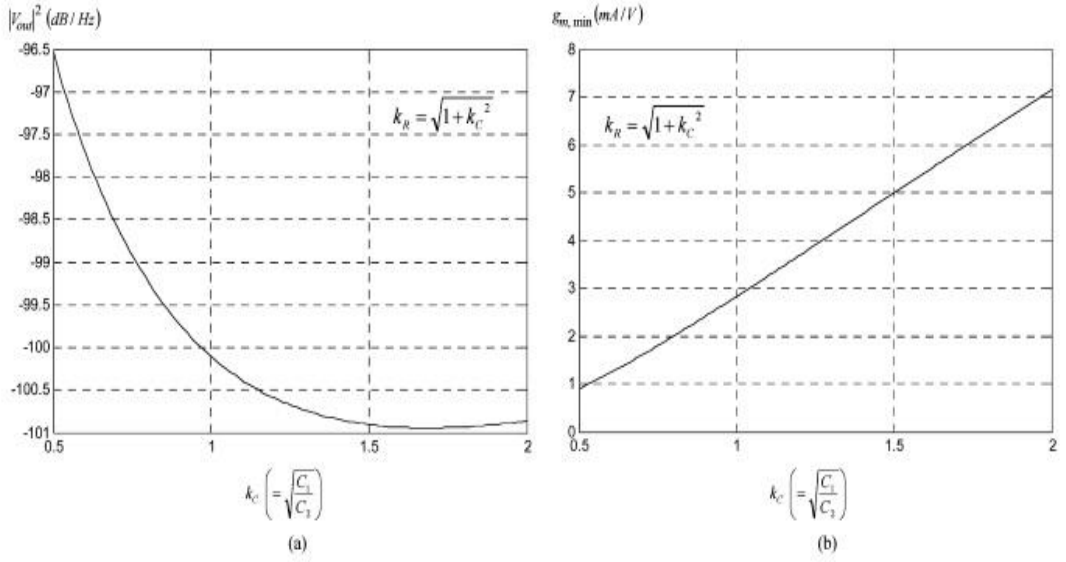

Figure 4.6 : (a) Total noise power. (b) Minimum required transconductance [16].

Figure 4.6 shows that choosing k_C about between 1 and 1.5 is optimum for both noise and power consumption.

4.1.2 Band-pass filter analysis and effect of parasitics

Figure 4.7 shows the band-pass filter structure used in oscillator with parasitic capacitance of used OTA.

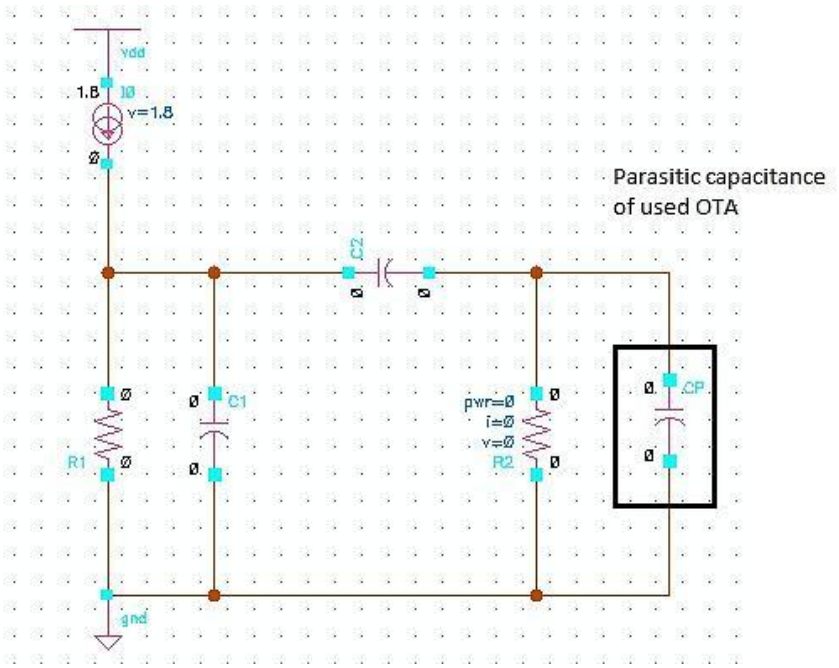

Figure 4.7 : Band-pass filter structure with parasitic capacitance of OTA.

After the noise and power analysis, the capacitances are chosen 200fF and resistors are chosen as 250Ω and 500Ω. Without any parasitic capacitance, the band-pass filter characteristic is shown in Figure 4.8.

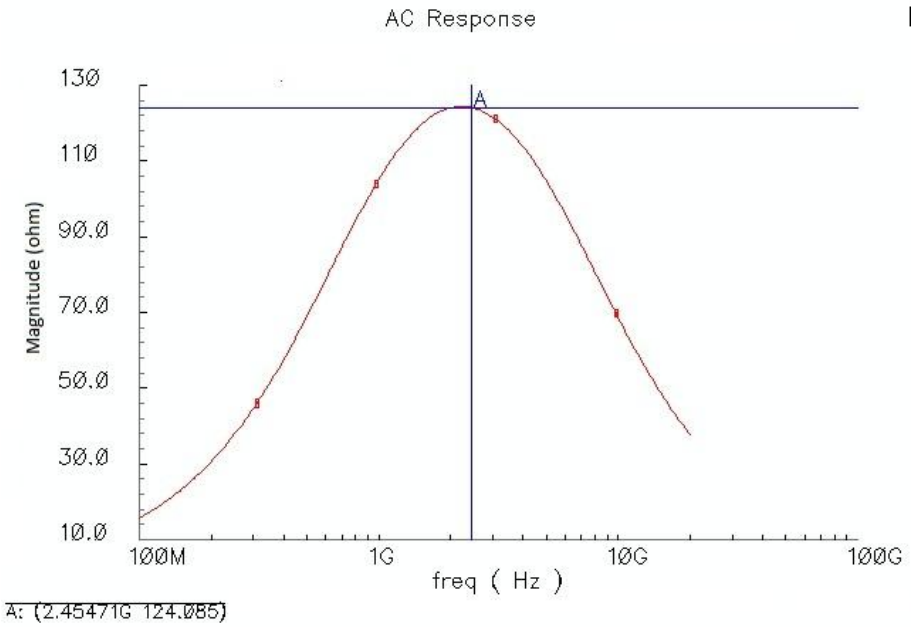

Figure 4.8 : BPF characteristic.

Figure 4.8 shows that center frequency of BPF is settled about 2.4 GHz that determine the oscillation frequency. However, there is also parasitic capacitance of used OTA and Figure 4.9 shows the effect of this capacitance.

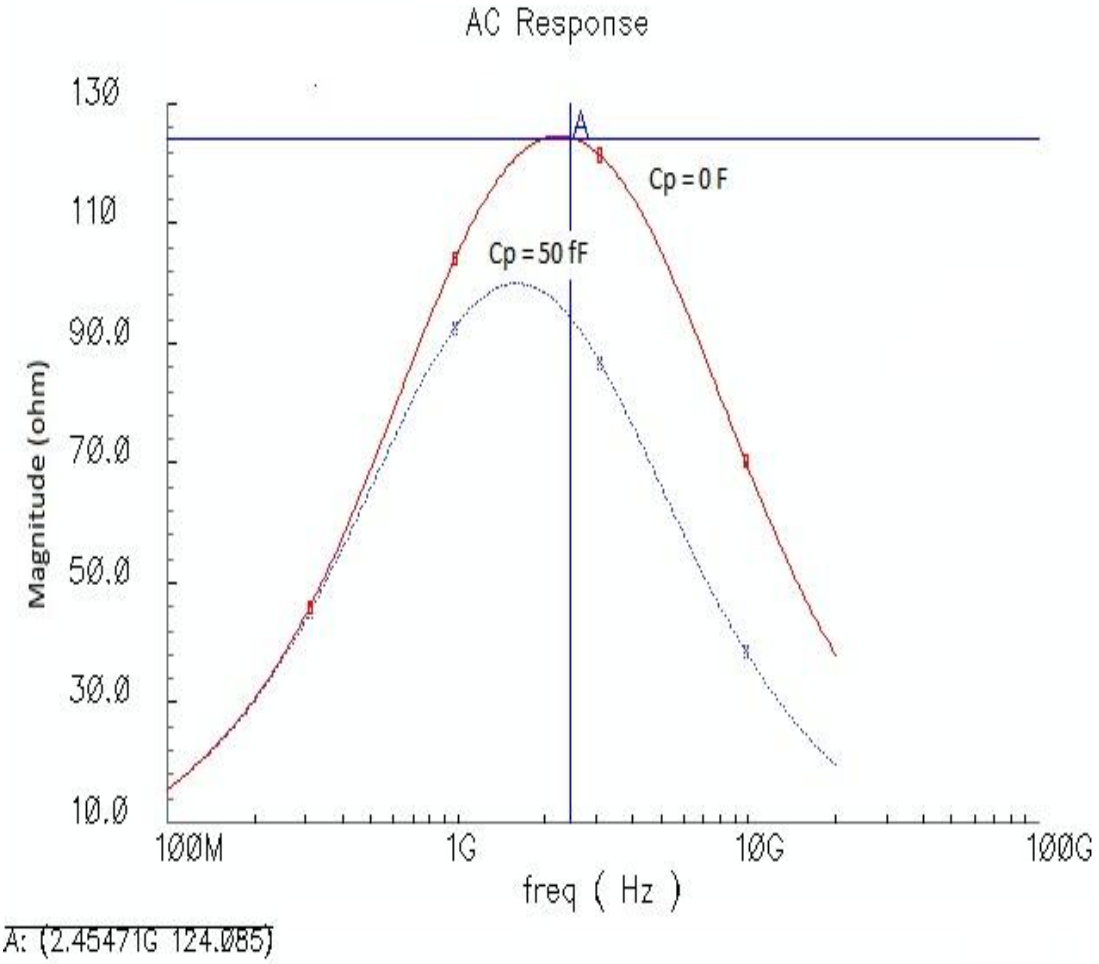

Figure 4.9 : Effect of OTA parasitic capacitance on BPF.

Figure 4.9 shows that, the parasitic capacitance of OTA decreases the oscillation frequency. Therefore, capacitance and resistor values should be decreased and optimized again in the oscillator circuit to obtain same oscillation frequency. It can be seen from this effect that upper limit of oscillation frequency in this structure is quite relevant with the technology because high speed technologies with lower length of transistors can provide lower parasitic capacitance.

4.2 Design of OTA-RC oscillator

The BPF circuit shown in Figure 4.7 is used with fully differential OTA to implement oscillator circuit. Designed structure is shown in Figure 4.10.

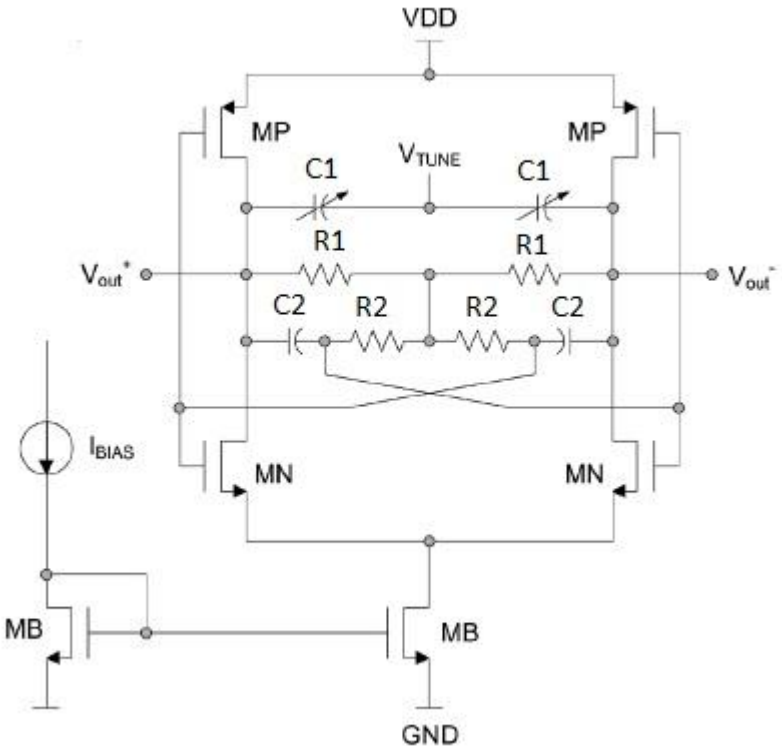

Figure 4.10 : OTA-RC Oscillator fully differentially implementation [16].

MP and MN transistors are used to provide required gain for oscillation. Their bias current is coming from tail current source (MB). The connection between C2 and R2 is also connected to input and this positive feedback causes oscillation.

Output differential transient response of the circuit is shown in Figure 4.11.

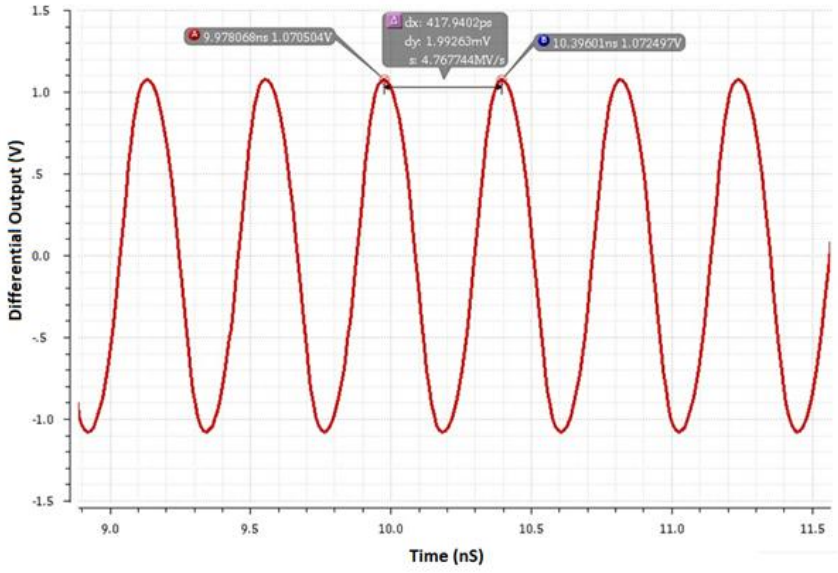

Figure 4.11 : Differential output of OTA-RC oscillator.

From Figure 4.11, it can be seen that oscillation period is about 417 ps that corresponds 2.4 GHz. Output differential amplitude is around 2 V peak-to-peak. The phase noise performance of circuit at 2.4 GHz oscillation frequency is shown in Figure 4.12.

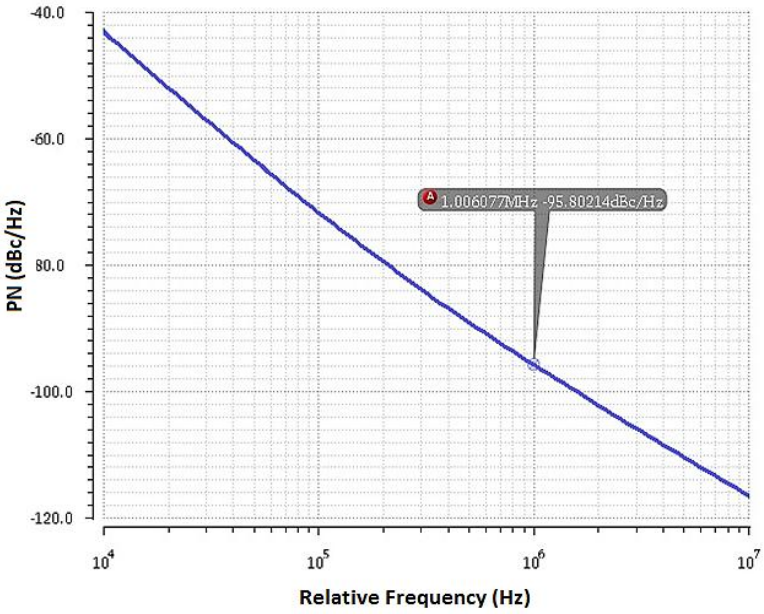

Figure 4.12 : Phase noise performance of OTA-RC Oscillator.

Figure 4.12 shows that the phase noise is simulated as – 95.8 dBc/Hz at1 MHz offset. In this structure, tuning range can be controlled by both capacitor and resistor. Therefore, fine and course tuning can be obtained easily using these components. Figure 4.13 shows the 5 bit controlled variable resistor schematic.

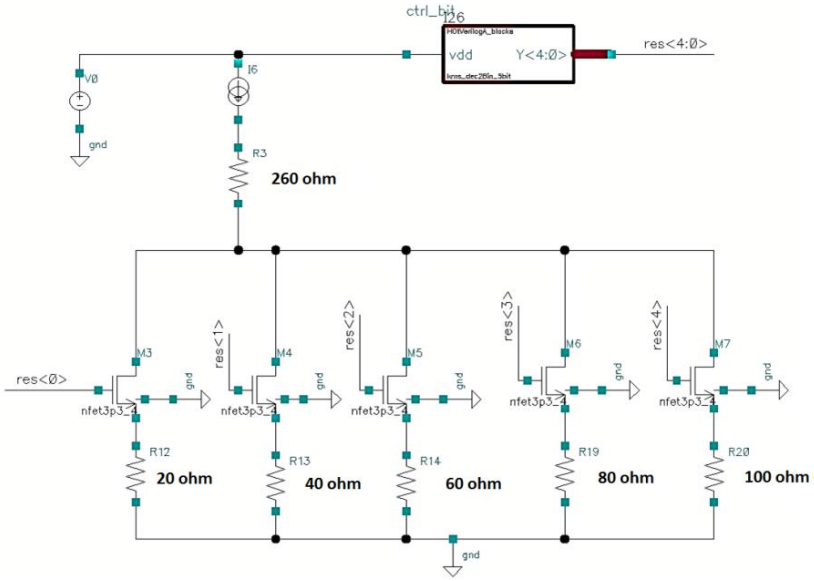

Figure 4.13 : 5 bit controlled variable resistor.

The critical issue on this variable resistor is the r_{ON} resistance of switches. Therefore, switch transistors should be selected large to provide less resistance that doesn't affect total resistance on path. Controlled resistor value with major bits (1, 2, 4, 6, 8, 16) is shown in Figure 4.14.

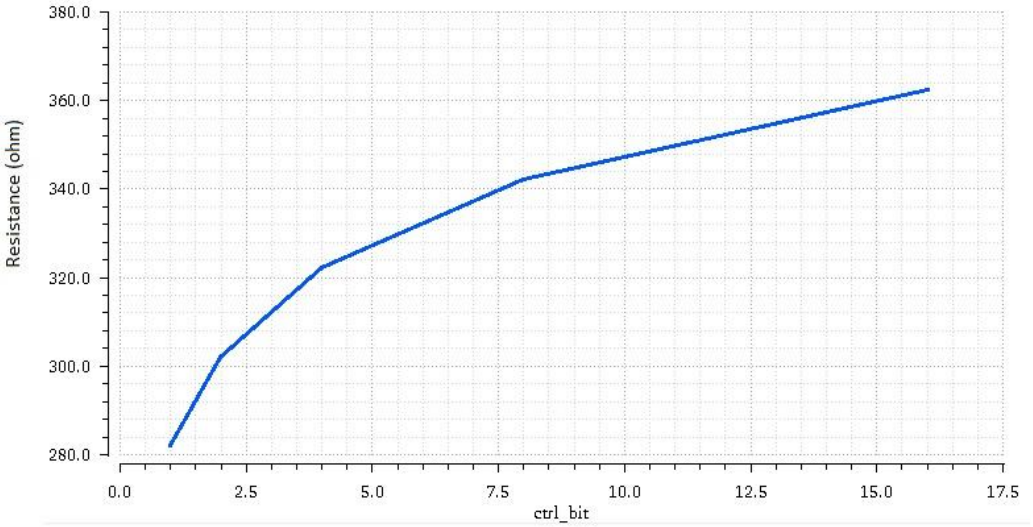

Figure 4.14 : Variable resistance.

Oscillator tuning range with varactor and variable resistor is shown in Figure 4.15

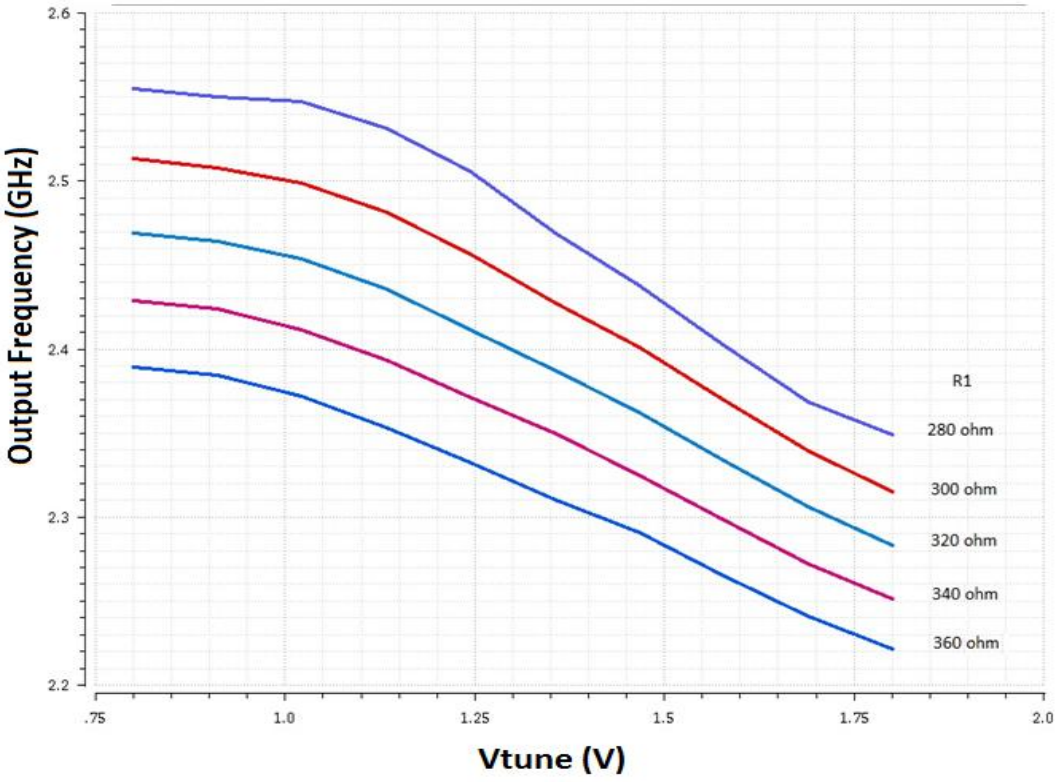

Figure 4.15 : OTA-RC Oscillator tuning frequency.

The simulated K_{VCO} is about 220 MHz/V. The tuning range can be extended using different resistor values. Variation of the phase noise for tuning oscillation frequency is shown in Figure 4.16.

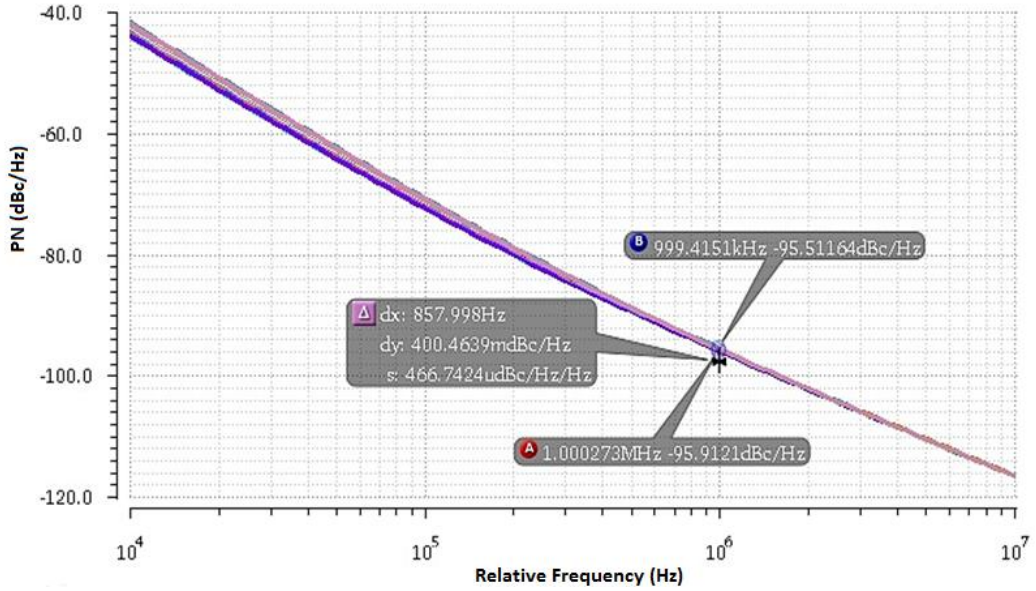

Figure 4.16 : Phase noise variation with related to Vtune.

The oscillation frequency changes from 2.6 GHz to 2.2 GHz and phase noise variation is only 0.4 dBc/Hz in this interval. The frequency stability of the circuit with related to process variation is shown in Figure 4.17.

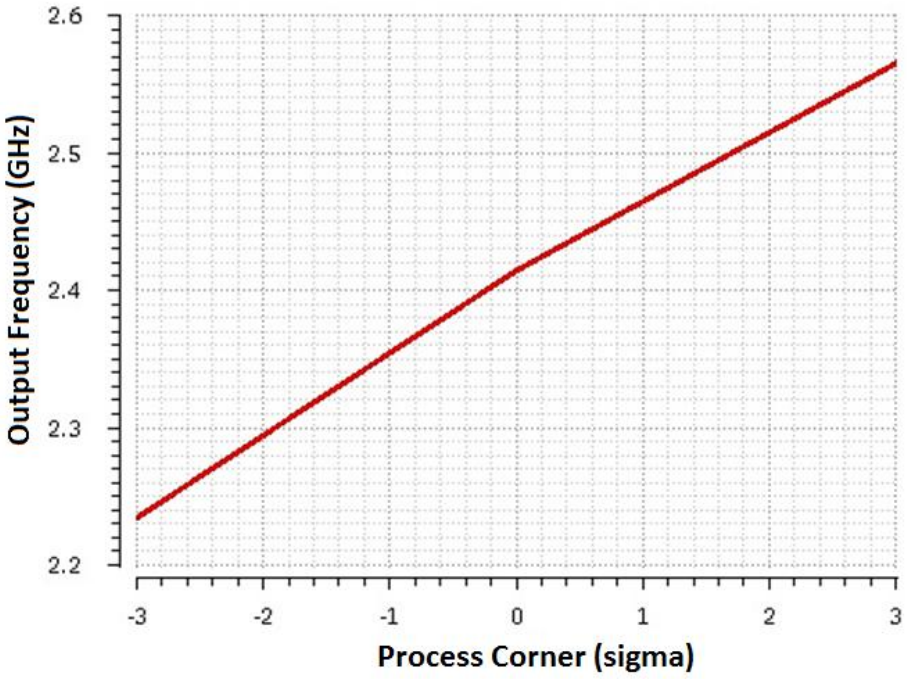

Figure 4.17 : Oscillation frequency over process variation.

The process variation for -3 and 3 sigma is unrealistic but it should be checked the circuit still oscillate in these cases. The output frequency over temperature and supply voltage is shown in Figure 4.18.

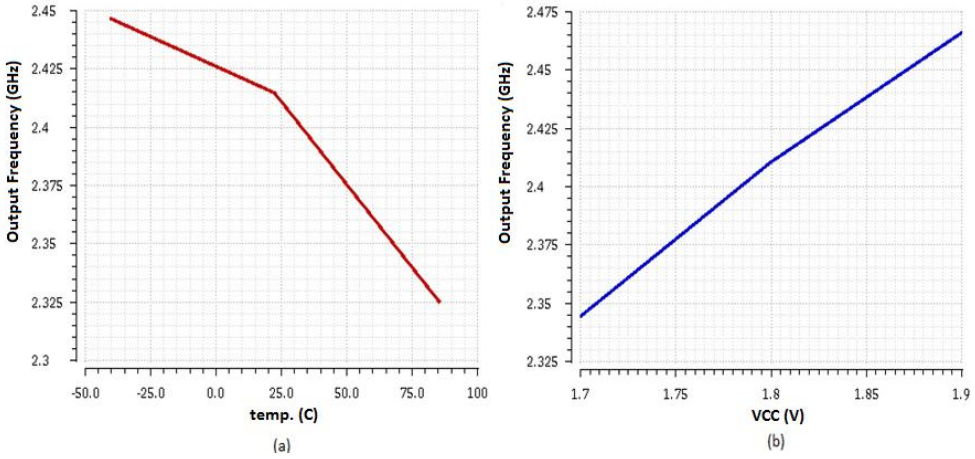

Figure 4.18 : (a) Oscillation frequency vs temp. (b) Oscillation frequency vs supply

The output frequency sensitivity of the circuit over supply, process and temperature variations looks reasonable. Also tuning range covers all these variations.

Final dimensions for PMOS transistors are 30µm/ 180nm and for NMOS transistors are 15 µm/180nm. The current mirror NMOS transistors are 1000 µm/2µm. The overall performance is summarized in Table 4-1.

Table 4-1: Overall performance of designed BPF VCO

	This Thesis	**(16)**
VCC	1.8 V	1.3 V
Power Consumption	5.4 mW	2.8 mW
Oscillation Frequency	2.4 GHz	2.4 GHz
K_{VCO}	220 MHz/V	330 MHz / V
Phase Noise @ 1 MHz offset	-95.8 dBc/Hz	-95.4 dBc/Hz
Technology	0.18 µm	0.13 µm

5. QUADRATURE RELAXATION VCO DESIGN

In today's technology, many up and down converter structures need quadrature LO signals because it is critical to suppress image band. Using two mixers and quadrature LO signals, this image rejection can be obtained more than 40 dB_c.

There are some passive circuits like polyphase filter to produce quadrature signals. These filters are hard to design because it is so sensitive to phase errors. Therefore, post layout simulations are very critical. Divider circuits can be also used to produce quadrature signals. However, it divides the frequency of the signal. That cannot be useful for high frequency operations. Relaxation oscillator can also produce quadrature signals with cross coupling two oscillators.

Relaxation oscillators can produce output signal with charging and discharging a timing capacitor. The high level model of relaxation oscillator is shown in Figure 5.1.

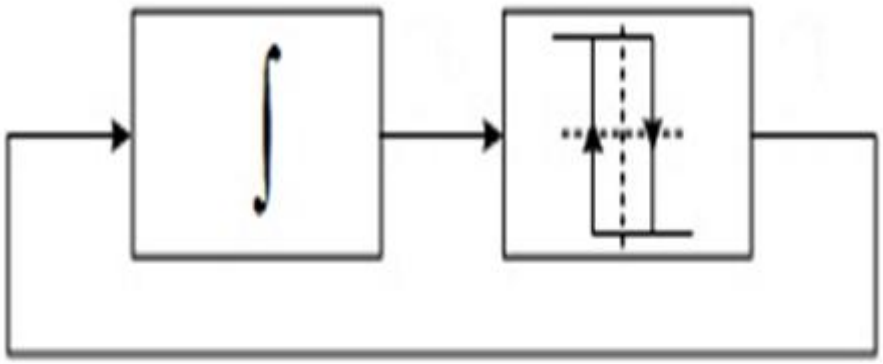

Figure 5.1 : High level model of relaxation oscillator [17].

The Schmitt-trigger is used as memory block and it generates switch levels with comparing integrator output to reference level. To implement the oscillator at very high frequencies we need a circuit as simple as possible. The integrator is implemented simply by a capacitor. Its input is the capacitor current (I_c) and the output is the capacitor voltage (V_c) that IS shown in Figure 5.2.

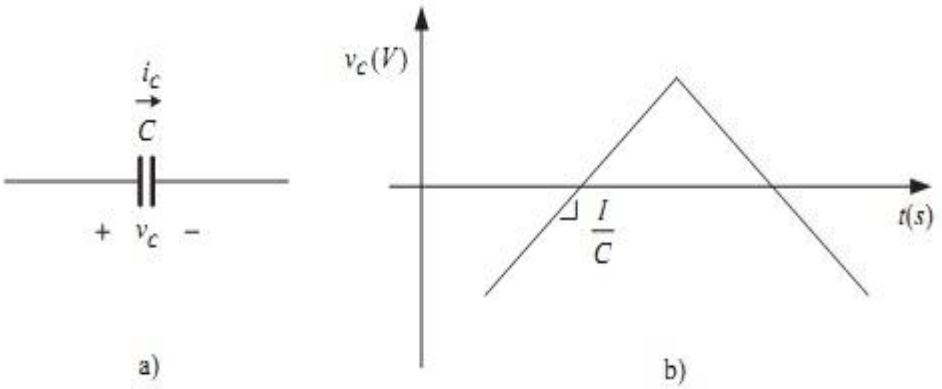

Figure 5.2 : (a) Basic integrator circuit implementation. (b) Integrator waveform [18].

The output voltage of the capacitor (V_c) is the input of the Schmitt-trigger block. The transfer characteristic of the Schmitt-trigger is shown is Figure 5.3. It is assumed that when the sign of $V_{BE1} - V_{BE2}$ changes the switching occurs.

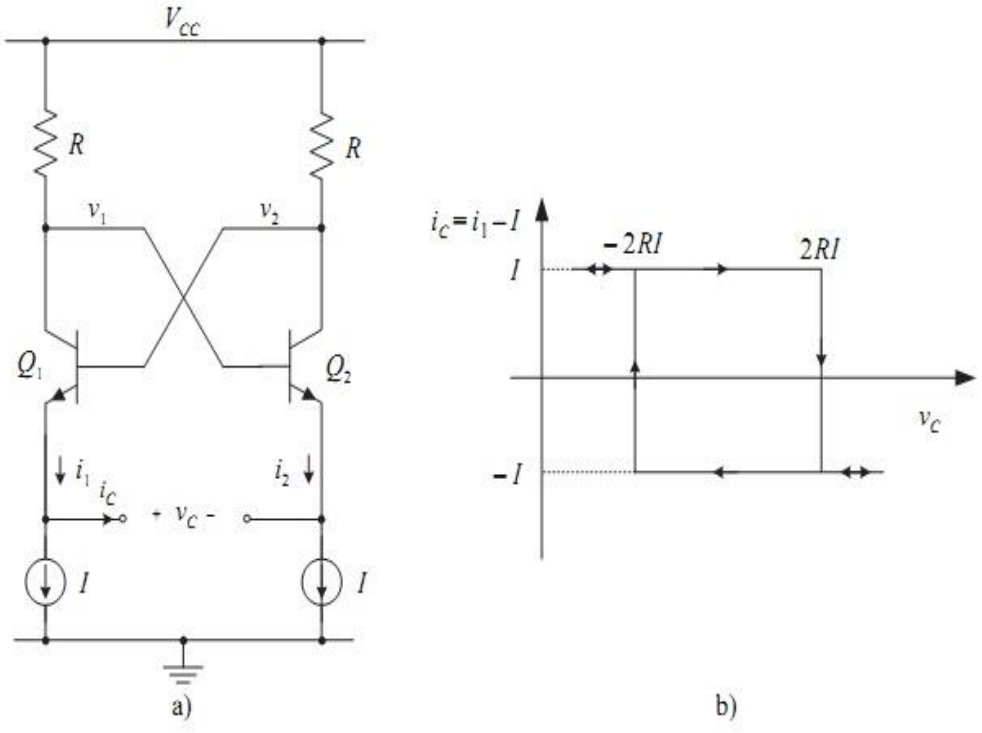

Figure 5.3: (a) Schmitt-trigger circuit implementation. (b) Schmitt-trigger transfer characteristics [18].

The transistors are used as switches in Figure 5.3. The overall implementation of circuit is shown in Figure 5.4.

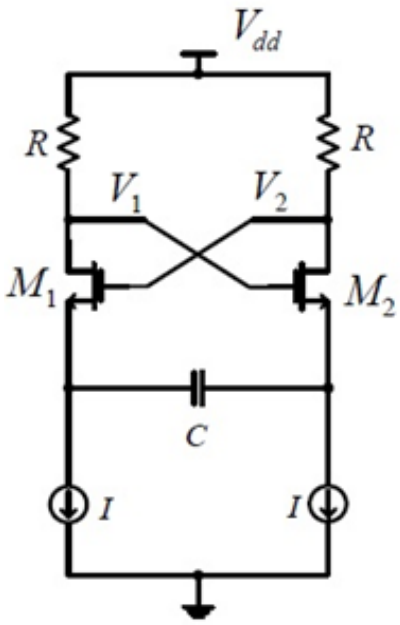

Figure 5.4 : Circuit implementation of relaxation oscillator [17].

In Figure 5.4, the reference signal is generated by bias current on resistors. The integration constant of the circuit is I/C. When the capacitance voltage crosses the reference voltage level, capacitor current direction is changed by switches. This implementation of relaxation oscillator is suitable for RF application because of simple structure with low parasitic effects.

The oscillation amplitude is determined by resistance and current and it can be expressed as 4IR from Figure 5.3. Oscillation frequency is shown in Equation **(5.1).**

$$f_0 = \frac{I}{2C(4RI)} = \frac{1}{8RC} \tag{5.1}$$

This formula isn't accurate for high frequencies. Oscillation frequency depends on more parameters in high frequencies but it is still useful to start design.

5.1 Phase Noise Analysis of Single Relaxation Oscillator

The noise analysis in this section can be studied in more detail in reference [18]. Noise power spectral density function can be used to describe noise of relaxation oscillator. It can be shown as $S(x_n)$, where x_n is a noise variable that can be current or voltage. A noise source x_n with spectral density $S(x_n)$ at the input produces an output noise y_n with spectral density;

$$S(y_n) = \left|H(s)_{s=j\omega}\right|^2 S(x_n) \tag{5.2}$$

where H(s) is the transfer function of the system.

The oscillator output voltage can be expressed as Equation **(5.3)** in time domain.

$$V_{out} = V\cos[\omega_0 t + \theta(t)] \tag{5.3}$$

V_m is the oscillator amplitude and θ(t) contains the oscillator phase-noise. A carrier of amplitude V_m, modulated in phase by a sinusoidal signal of frequency f_m can be represented as

$$V_{out} = V_m\cos[(\omega_0 t) + \frac{\Delta f_{pk}}{f_m}\sin(\omega_m t)] \tag{5.4}$$

Δf_{pk} is the peak frequency deviation. For $f_m << f_0$ the phase modulation results infrequency components on each side of the carrier, with amplitude $V_m\Delta f_0 / 2f_m$:

$$\begin{aligned} V_{out} &\approx V_m[\cos(\omega_0 t) + \frac{\Delta f_0}{2 f_m}[\cos(\omega_0 + \omega_m)t - \cos(\omega_0 - \omega_m)t]] \\ V_{out}\big|_{f=f_0+f_m} &= V_m\frac{\Delta f_0}{2 f_m}\cos(\omega_0 + \omega_m) \end{aligned} \tag{5.5}$$

Therefore, we can obtain spectral noise equation as;

$$S(v_{out})\big|_{f=f_0+f_m} = \left|\frac{V_m}{2 f_m}\right|^2 S(\Delta f_0) \tag{5.6}$$

The spectral density of the phase-noise, $L(f_m)$, is defined as the ratio of the noise power in a one Hz bandwidth at a distance f_m from the carrier relative to the carrier power.

$$L(f_m) = \frac{S(V_{out})\big|_{f=f_0+f_m}}{\frac{1}{2}V_m{}^2} = \frac{1}{2 f_m{}^2}S(\Delta f_0) = \frac{\left|H(jw)^2\right|}{2 f_m{}^2}S(x_n) \tag{5.7}$$

The noise model of relaxation oscillator is shown in Figure 5.5 below. Voltage and current noise sources are shown together.

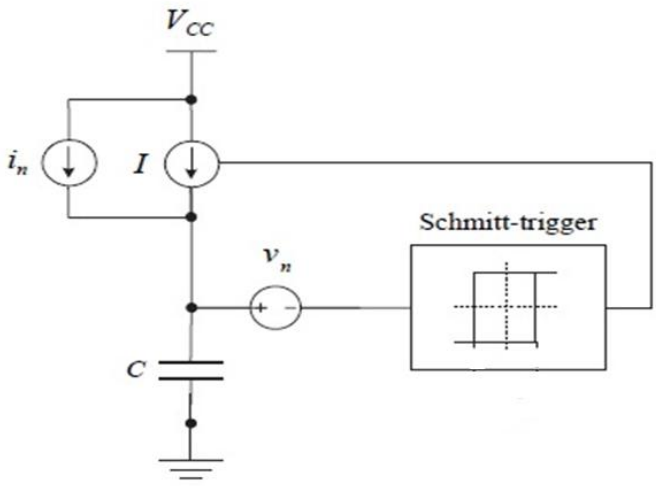

Figure 5.5 : Relaxation oscillator with noise sources [18].

In Figure 5.5, noise sources i_n and v_n causes phase shift at oscillation frequency. Equation **(5.8)** shows the phase noises of these current and voltage noise sources using Equation **(5.7).**

$$L(f_m) = \frac{S(i_n)}{2I^2}\left(\frac{f_0}{f_m}\right)^2, \quad L(f_m) = \frac{S(v_n)}{2I^2}\left(\frac{f_0}{f_m}\right)^2 \qquad \textbf{(5.8)}$$

Equation **(5.8)** shows the inverse proportion between current and phase noise. The current also determines output oscillation voltage swing that shown in Equation **(5.1).** As a result, phase noise and oscillation amplitude is inversely proportional each other.

The relaxation oscillator circuit with parasitic capacitances is redrawn in Figure 5.6.

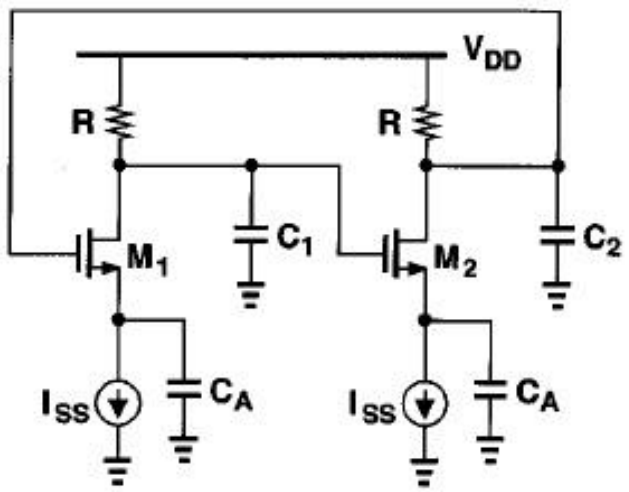

Figure 5.6 : Relaxation oscillator with parasitic capacitances [10].

In Figure 5.6, the circuit looks like two stage ring with capacitive degeneration. The quality factor is expressed as Equation **(5.9)** in reference [10].

$$Q^2 = 4(1-\frac{C_1}{C_A})\frac{C_1}{C_A} \qquad \textbf{(5.9)}$$

The maximum value for quality factor is 1 under the condition that $C_A=2C_1=2C_2$.

5.2 Design of Single Relaxation Oscillator

The circuit is shown in Figure 5.4 is designed for 2.4 GHz oscillation frequency. The transistor and passive element sizes are determined to optimize power consumption and phase noise trade-off. The transistor dimensions are selected as 120µm/180nm. The nominal varactor capacitance for 2.4 GHz oscillation is about 0.6 pF. The load resistors are chosen as 120 Ω. These resistors determine the output amplitude therefore higher resistance means lower phase noise. 140Ω resistors are used as current sources at the sources of transistors. The total power consumption is 18 mW. The output differential signal is shown in Figure 5.7.

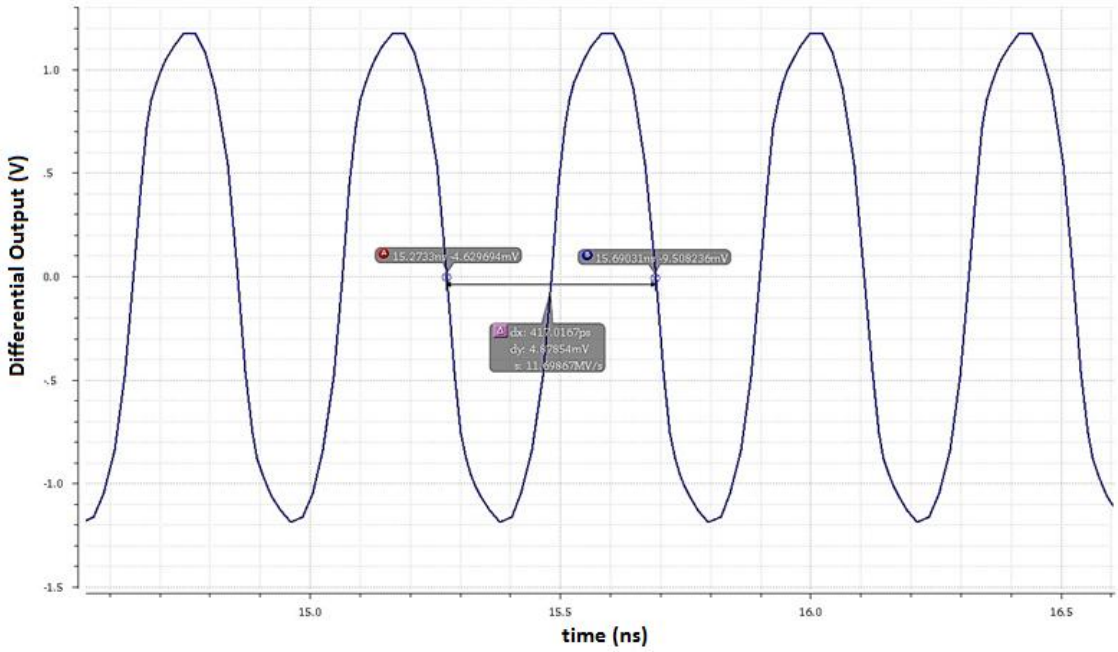

Figure 5.7 : Differential output signal of relaxation oscillator.

The oscillation period is simulated as 417 ps that correspond to about 2.4 GHz oscillation frequency. Differential output signal amplitude is about 2.2 V. The most

critical parameter is that the phase noise of this output signal. It is also simulated with PSS and PNOISE to determine this parameter and the result is shown in Figure 5.8 below.

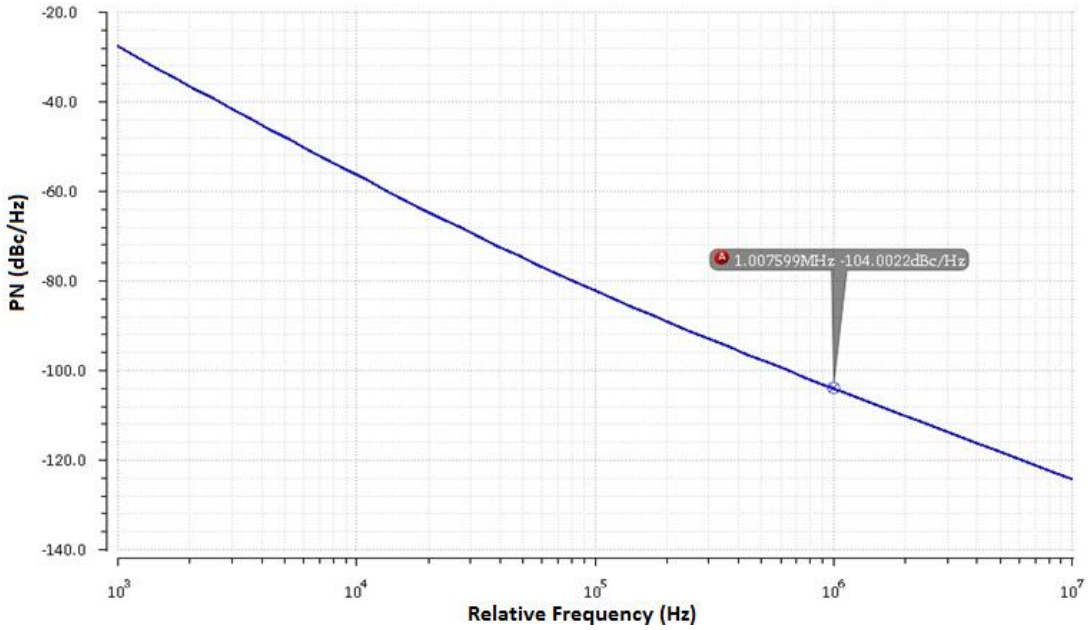

Figure 5.8 : Phase noise performance of relaxation oscillator.

The simulated phase noise is about -104 dBc/Hz @ 1MHz offset. The tuning range of the circuit is simulated with sweeping tuning voltage from 0 to 1.8V. The output frequency variation is shown in Figure 5.9.

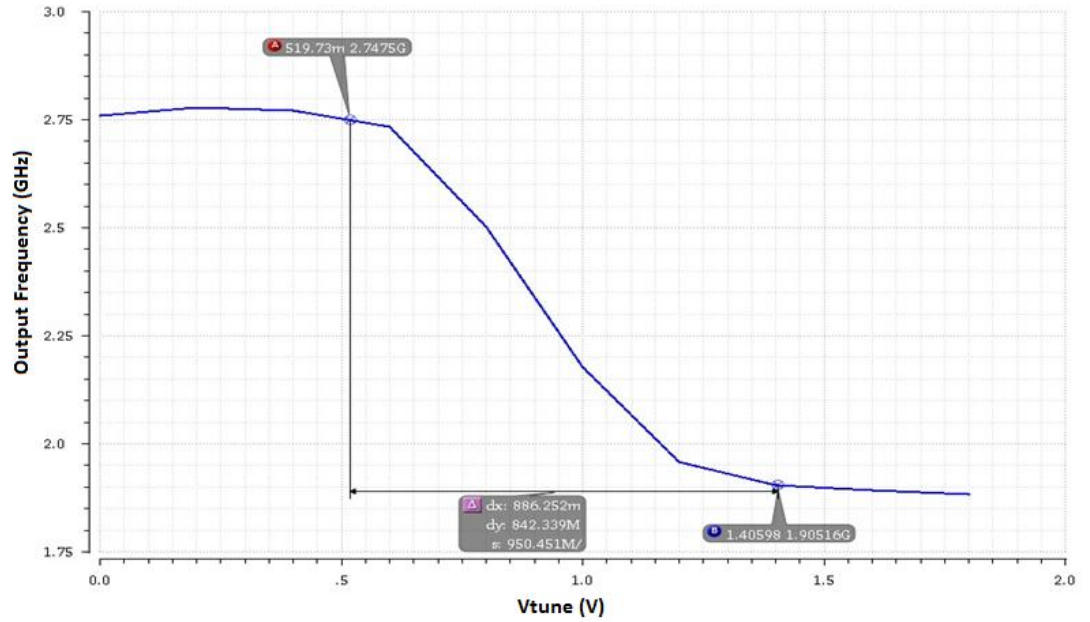

Figure 5.9 : Tuning range of relaxation oscillator.

It can be seen from Figure 5.9 that about 850 MHz tuning range is obtained at 2.4 GHz center frequency (35%). K_{VCO} is calculated as 950 MHz/V. The phase noise variation with related to tuning voltage is shown in Figure 5.10.

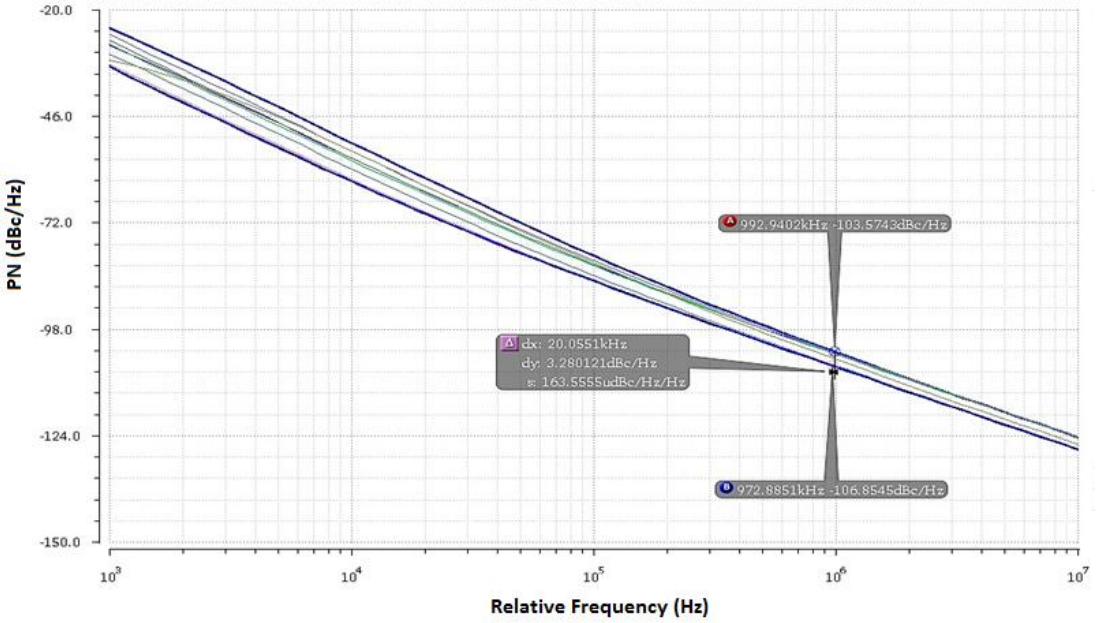

Figure 5.10 : Phase noise of relaxation oscillator versus tuning voltage.

The phase noise variation for all tuning range is just 3 dBc/ Hz. Oscillation frequency stability is also another important criterion for oscillators. Oscillation frequency variation over PVT is shown in Figure 5.11.

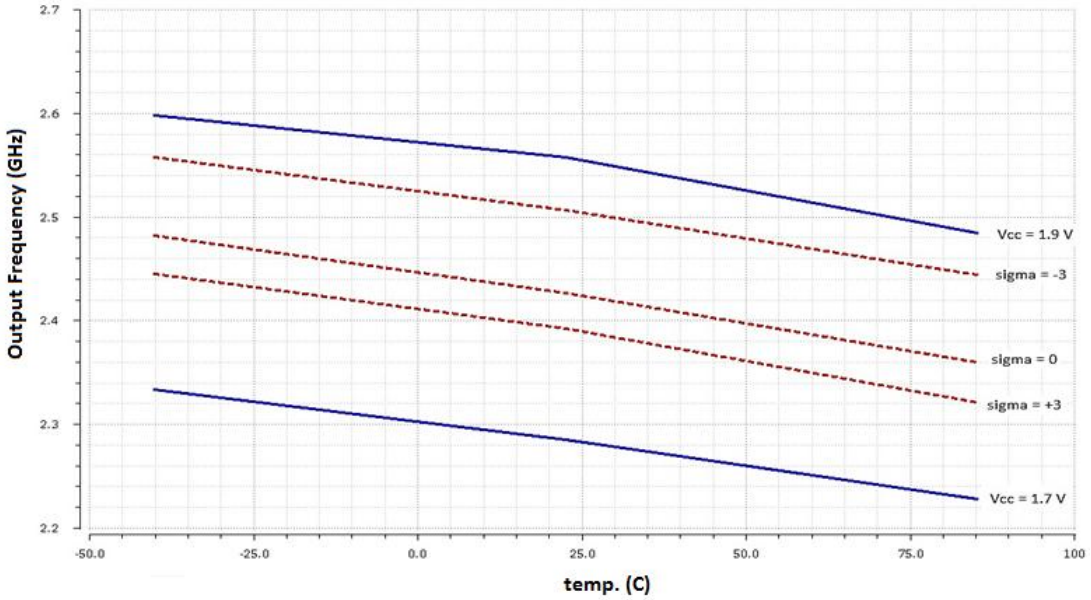

Figure 5.11: Oscillation frequency of relaxation oscillator over PVT.

Figure 5.12 shows the Monte Carlo simulation result of oscillation frequency.

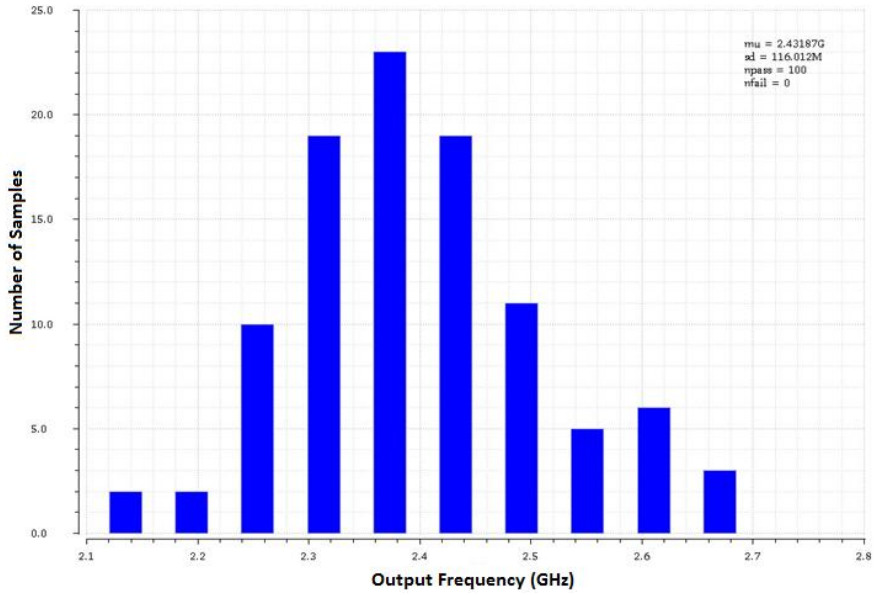

Figure 5.12 : Monte Carlo mismatch simulation of relaxation oscillator.

The Monte Carlo analysis is done for this design to see mismatch effect of transistors and resistors. Its standard deviation is 116 MHz around 2.43 GHz. Both process and mismatch analysis shows that the oscillation condition is ensured for all conditions and frequency changes are little than tuning range.

5.3 Phase Noise Analysis of Quadrature Relaxation Oscillator

The block diagram of this structure is shown in Figure 5.13 below.

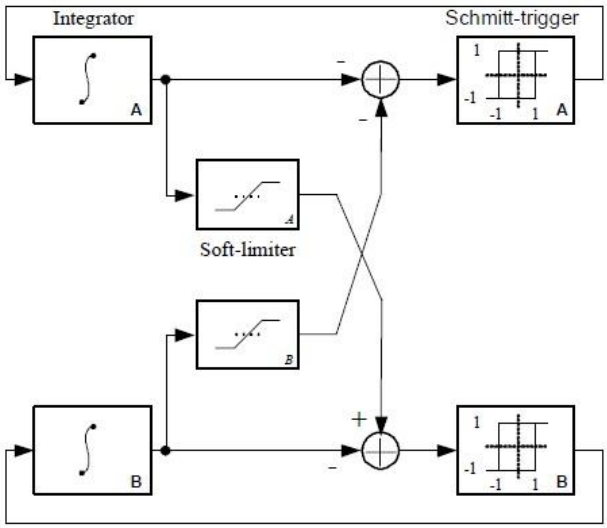

Figure 5.13 : Block diagram of quadrature relaxation oscillator [20].

The quadrature cross-coupled oscillator includes two oscillators that trigger each other in a balanced mode. These two oscillators have same oscillation frequency and Schmitt trigger outputs have 90^0 phase shift that provide quadrature output. In this architecture, phase noise is less sensitive to switching speed with related to soft-limiter gain.

The implementation of this structure should be as simple as possible for the high frequency operation. Therefore, cross coupled transistors are used for Schmitt trigger, capacitor for integrator and differential pairs for soft-limiters that sense the capacitor voltage of one oscillator and conduct to other oscillator differentially. It is shown in Figure 5.14.

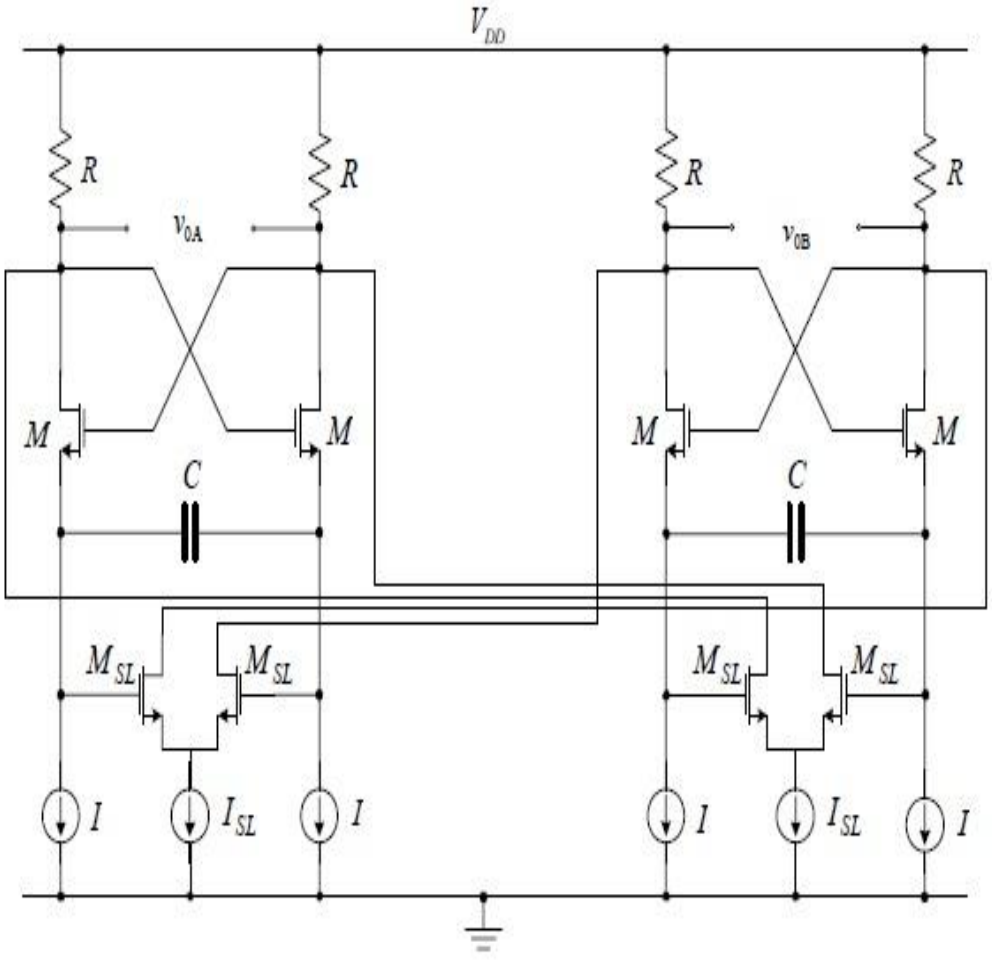

Figure 5.14 : Quadrature relaxation oscillator schematic [20].

The phase noise equation of this structure for high frequencies is very complex but it can be shown that cross-coupled structures reduce the phase noise. Figure 5.15 shows the noise sources in this structure.

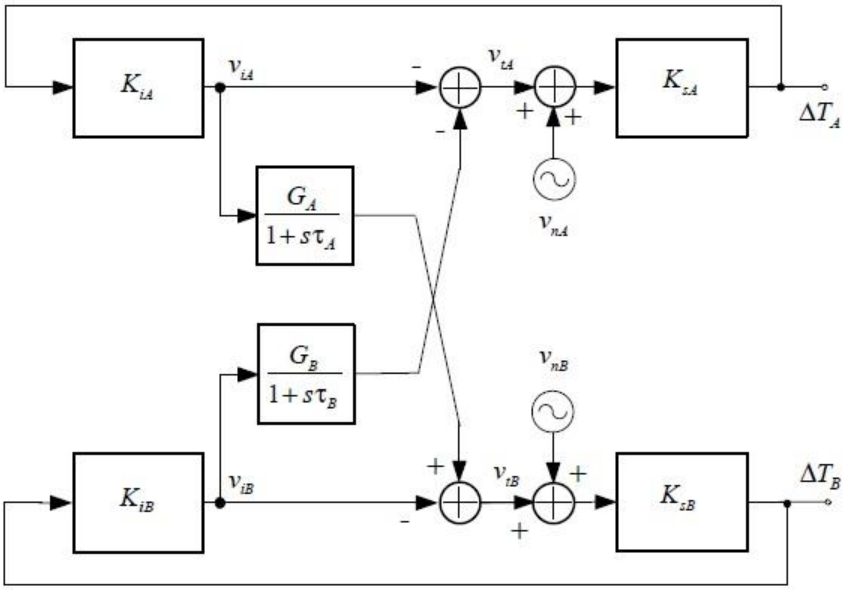

Figure 5.15 : Relaxation oscillator with noise sources [20].

The parameters are explained below.

- $K_{S\{A,B\}}$ Voltage to Time Conversion Factor (Schmitt-trigger A or B)
- $K_{i\{A,B\}}$ Time to Voltage Conversion Factor (Integrator A or B)
- $V_{i\{A,B\}}$ Integrator Output (A or B)
- $\Delta T_{\{A,B\}}$ Oscillator (Schmitt-Trigger) Output (A or B)
- $V_{t\{A,B\}}$ Noiseless Schmitt-Trigger Input (A or B)
- $G_{\{A,B\}}$ Soft-Limiter Gain (A or B)
- $\tau_{\{A,B\}}$ Time constant in Cross-Coupling Path(A or B)
- $v_{n\{A,B\}}$ Input Noise Source (A or B)

Using Figure 5.15, the outputs $\Delta T_{\{A,B\}}$ caused by noise sources are obtained as in Equation **(5.10)** and **(5.11).**

$$\Delta T_A = \frac{1}{K_{iA}K_{iB}(1+G_AG_B)}(K_{iB}v_{nA} + K_{iA}G_Bv_{nB}) \qquad \textbf{(5.10)}$$

$$\Delta T_B = \frac{1}{K_{iA}K_{iB}(1+G_AG_B)}(K_{iA}v_{nB} + K_{iB}G_Av_{nA}) \qquad \textbf{(5.11)}$$

These equations show that increasing the coupling gain attenuates, due the feedback, the effect of the noise sources v_{nA} and v_{nB}.

5.4 Design of Quadrature Relaxation Oscillator

The circuit in Figure 5.14 is designed to obtain quadrature output from relaxation oscillator. Two single oscillators are copied from section 5.12 and M_{SL} transistors are added to couple oscillators with each other. M_{SL} transistor dimensions are selected as 60µm/180nm. 2 mA extra current is added from these paths. The transient differential output signal is shown in Figure 5.16.

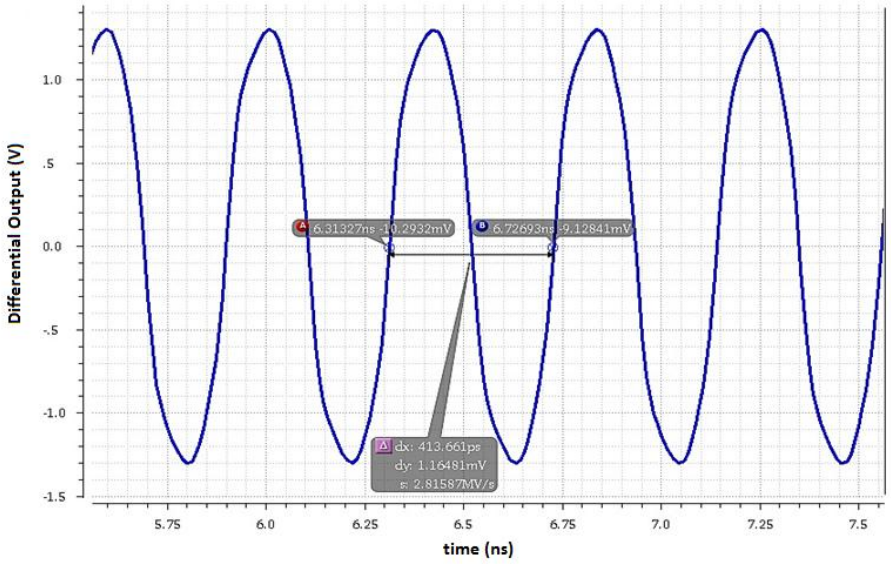

Figure 5.16 : Differential transient output signal of quadrature relaxation oscillator.

2.6V differential output swing is obtained with 2.4 GHz oscillation frequency. The phase noise performance of the circuit is shown in Figure 5.17.

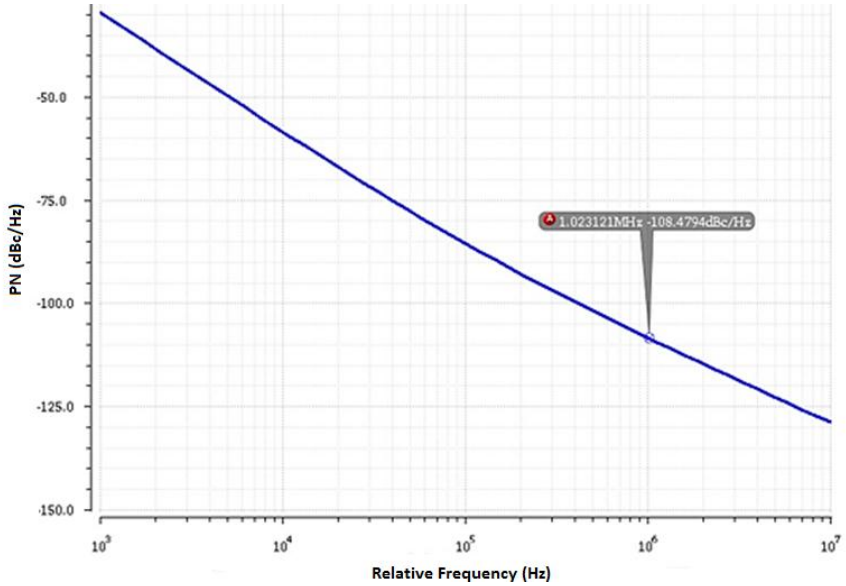

Figure 5.17 : Phase noise performance of the quadrature relaxation oscillator.

It can be seen from Figure 5.17 that, by using coupled structure about 4.5 dBc/Hz phase noise improvement is obtained with -108.5 dBc/Hz phase noise at 1 MHz offset. The frequency tuning range is also simulated with sweeping tuning voltage of the varactor. The tuning range performance of the quadrature relaxation oscillator is shown in Figure 5.18.

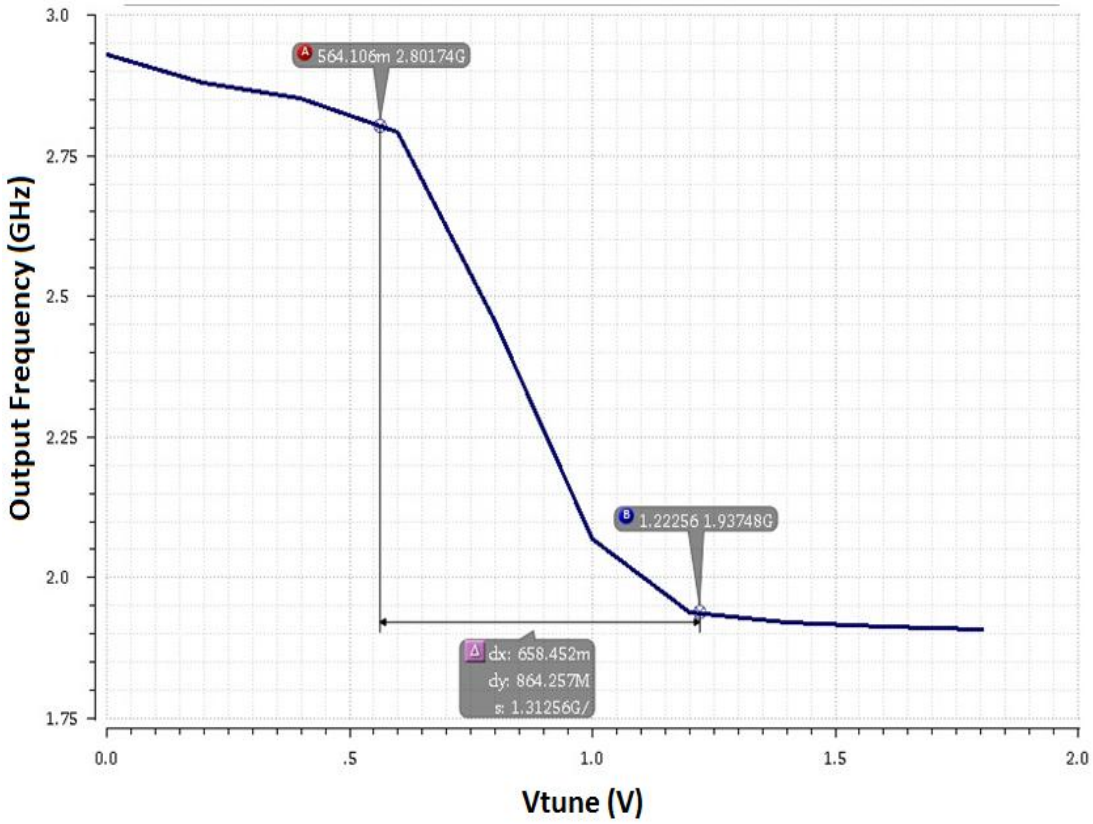

Figure 5.18 : Tuning range of quadrature relaxation oscillator.

The linear tuning range is about 850 MHz with 1.3 GHz/V K_{VCO} value. The quadrature structure doesn't affect the tuning performance of the single relaxation oscillator. It has still about 35% tuning range with 2.4 GHz center frequency.

Another important parameter of the quadrature structure is the phase error of the output quadrature signals. It is very critical to obtain quadrature signals with minimum phase error to reject image band accurately.

Phase error performance of the quadrature relaxation oscillator is shown in Figure 5.19. Differential output signals are shown in Figure 5.19 and it is expected that quarter period time difference should be between differential quadrature outputs without any phase error.

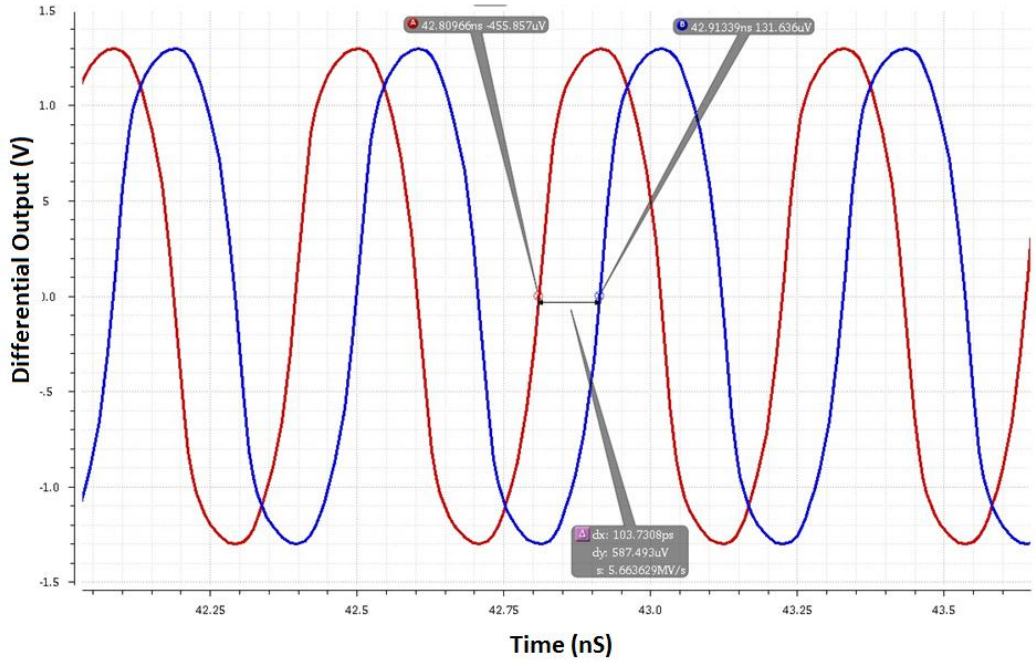

Figure 5.19 : Quadrature phase error of the relaxation oscillator.

The output phase error calculated from Figure 5.19 is about 0.5 degree at 2.4 GHz oscillation frequency. This is satisfying result for double balanced transceiver structures.

The phase noise variation with related to tuning voltage is shown in Figure 5.20

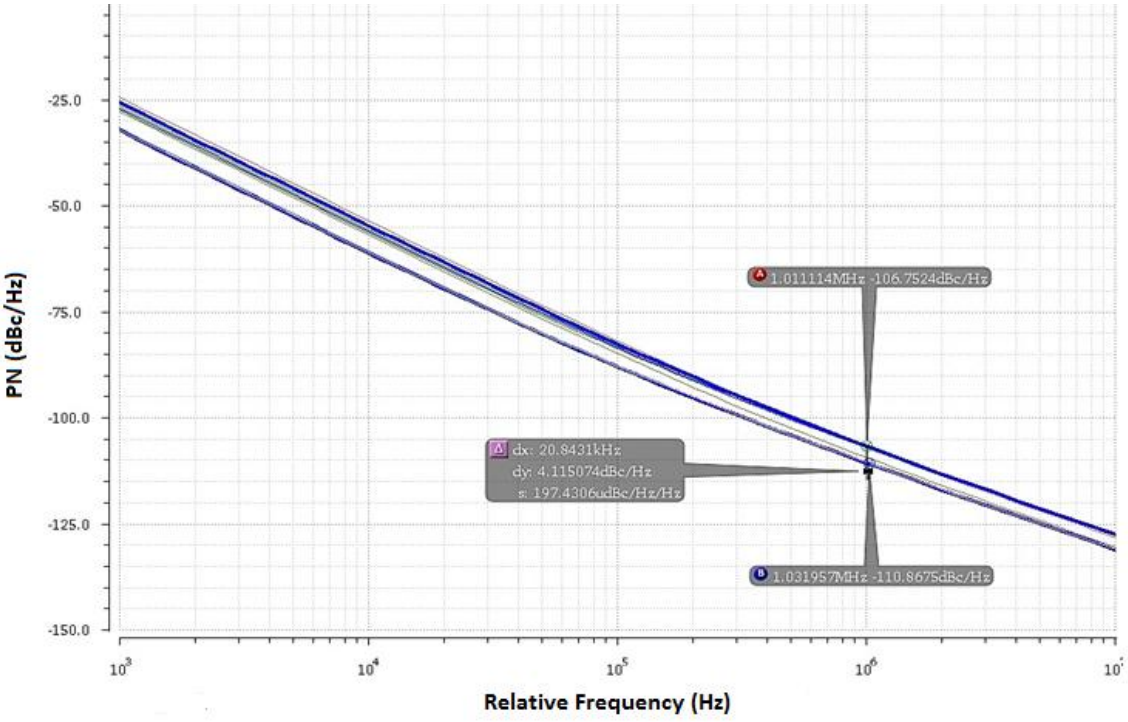

Figure 5.20 : Phase noise variation with tuning oscillation frequency.

The phase noise variation is about 4 dBc/Hz in all linear tuning range (35%).

The output frequency stability is also important over PVT. The performance is shown in Figure 5.21.

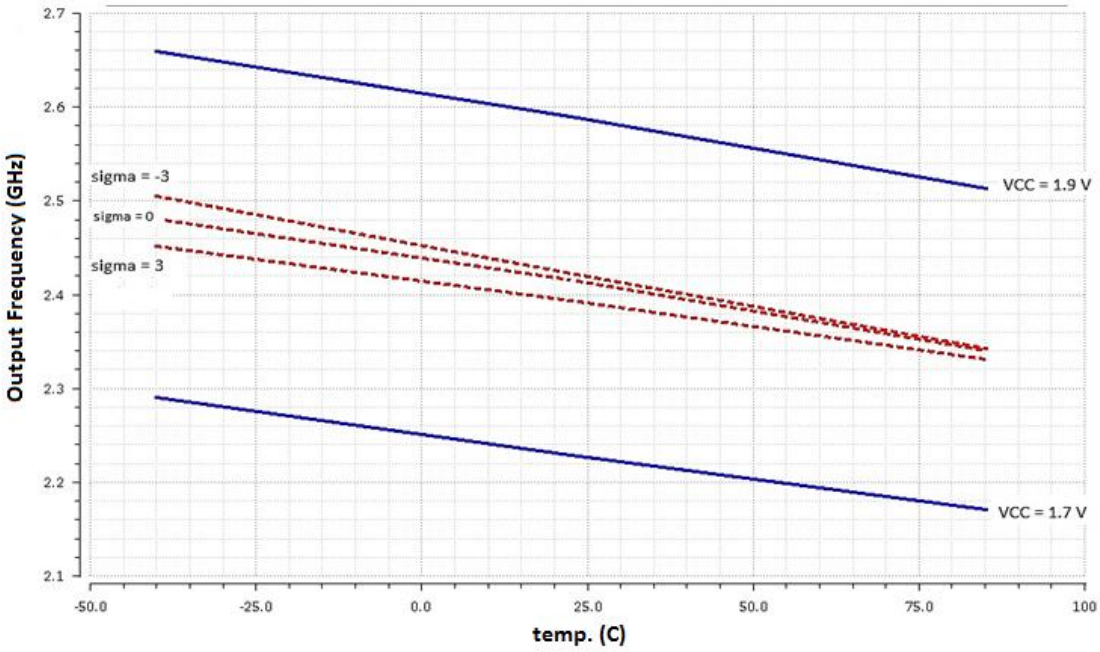

Figure 5.21 : Oscillation frequency of quadrature relaxation oscillator over PVT.

The Monte Carlo Analysis is also shown in Figure 5.22.

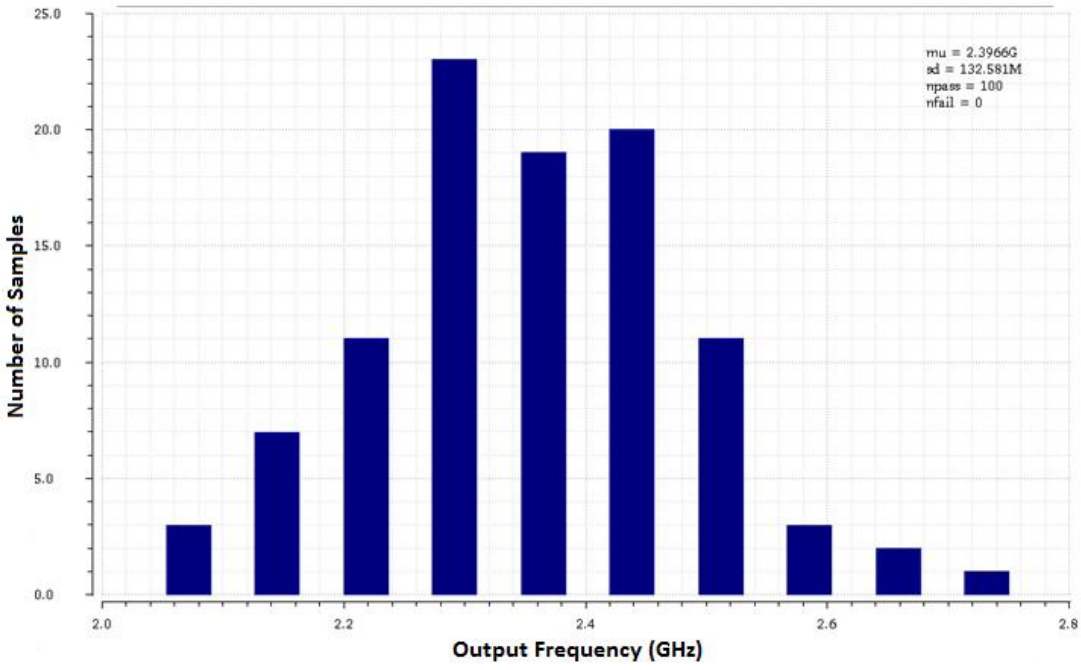

Figure 5.22: Output frequency Monte Carlo simulation of relaxation oscillator.

The overall performance of design is shown in Table 3.1.

Table 3-1: Overall performance of designed relaxation VCO

	This Thesis	**(17)**	**(19)**	**(20)**
VCC	1.8 V	1.3 V		3 V
Power Consumption	48 mW	1 mW	1 mW	23 mW
Oscillation Frequency	2.4 GHz	214 MHz	5 GHz	2.4 GHz
Tuning Range	1.9 GHz – 2.8 GHz (35 %)	-	-	-
K_{VCO}	1300 MHz/V	-	-	-
Phase Noise	-108.5 dBc/Hz @ 1MHz	-132.6 dBc/Hz @ 10 MHz	-97 dBc/Hz @ 1MHz	-104 dBc/Hz @ 1MHz
Technology	0.18 μm	0.13 μm	0.18 μm	0.35 μm

Table 3-1 shows that the performance of the designed circuit is satisfying with related to other designs in literature. Especially low phase error between quadrature outputs is very suitable for quadrature applications.

6. QUADRATURE UP CONVERSION MIXER APPLICATION

In this chapter, a quadrature Gilbert mixer is designed and relaxation oscillator is used as local oscillator source. Figure 6.1 shows the quadrature mixer block diagram.

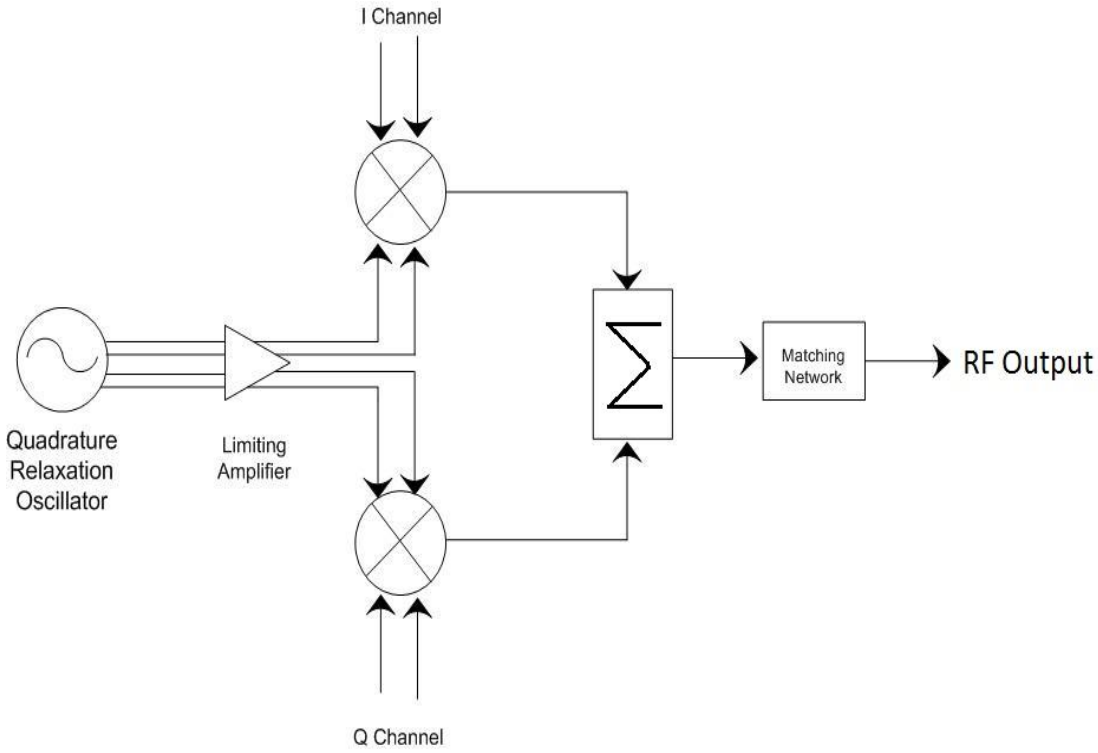

Figure 6.1 : Quadrature mixer block diagram.

In Figure 6.1, output of the relaxation oscillator is connected to limiting amplifier. This amplifier provides saturated signals for the mixer. This square wave signal results in high speed switching for the mixer. Output of the mixers are summed up using balun and matched to 50 Ω after matching network.

The most common mixer structure is Gilbert mixer that is shown in Figure 6.2. This double-balanced structure provides high isolation between ports. QM1 – QM4 transistors are used as the LO stage. The exponential current – voltage relationship of BJT's provides good switching performance. Q1 and Q2 transistors convert IF voltage to current.

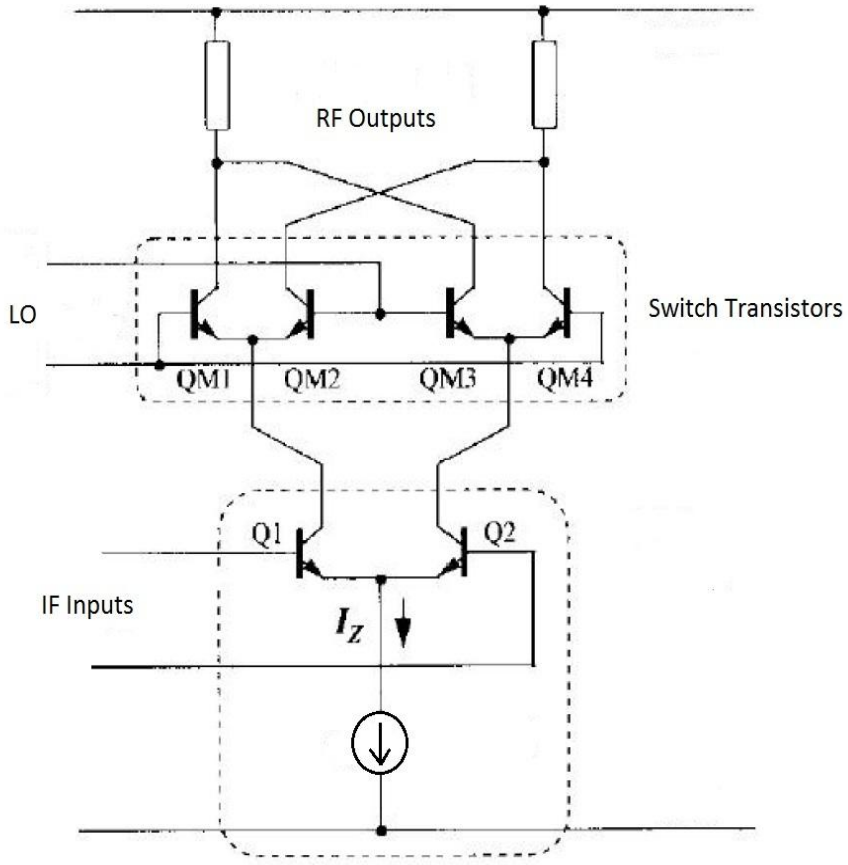

Figure 6.2 : Mixer core.

Important design parameters of the mixer are shown below:

- Conversion Gain
- LO Feedthrough
- Sideband Rejection
- Noise Figure and Output Noise Power
- IIP3
- Return Loss

6.1 Simulation Results of Quadrature Relaxation Oscillator + Mixer

In this section, simulation results of quadrature mixer are shown. Relaxation oscillator is used as local oscillator. Its quadrature output provides LO signals without using polyphase filter.

The overall blocks of mixer are shown in Figure 6.3.

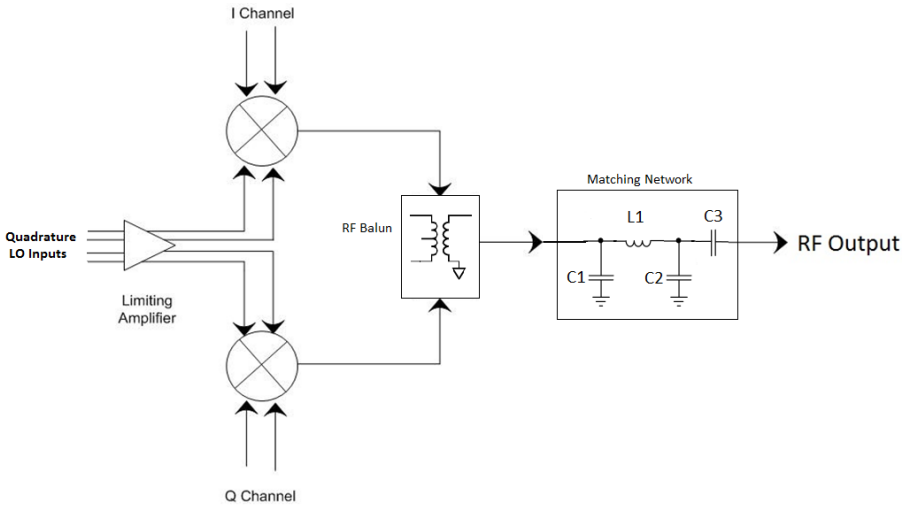

Figure 6.3 : Quadrature mixer blocks.

In Figure 6.3, s parameter model of RF balun is used for the simulation. It is modeled in SONNET.

After the oscillator, limiting amplifier is used because Gilbert mixers require strong LO signal. It is important for the fast switching. The disadvantage of this strong LO signal is worse LO – RF isolation. Using double balanced structure that is shown in Figure 6.2, differential LO signal cancels each other. Therefore only the coupling can be problem for the LO – RF isolation. Also, matching of transistors are another parameter to reject LO feedthrough.

Firstly, transient simulation result of the circuit is shown in Figure 6.4.

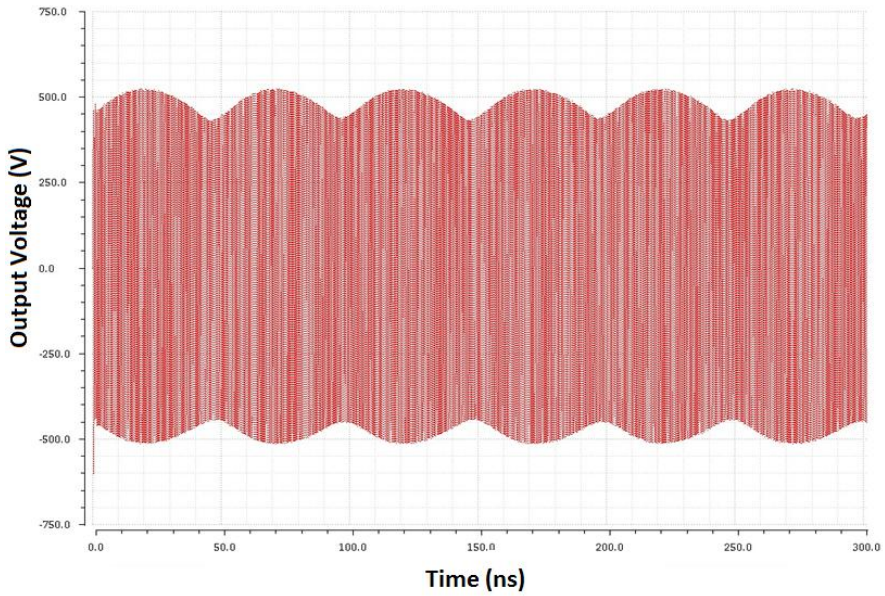

Figure 6.4 : RF Output of the mixer.

Output frequency of the oscillator is controlled by V_{tune} voltage. It is adjusted to 2.4 GHz oscillation frequency. 1 MHz signal is used to IF inputs. Therefore, RF signal consists of 1 MHz information signal and about 2.4 GHz carrier signal. Harmonic balance simulation is done to show conversion gain that is shown in Figure 6.5.

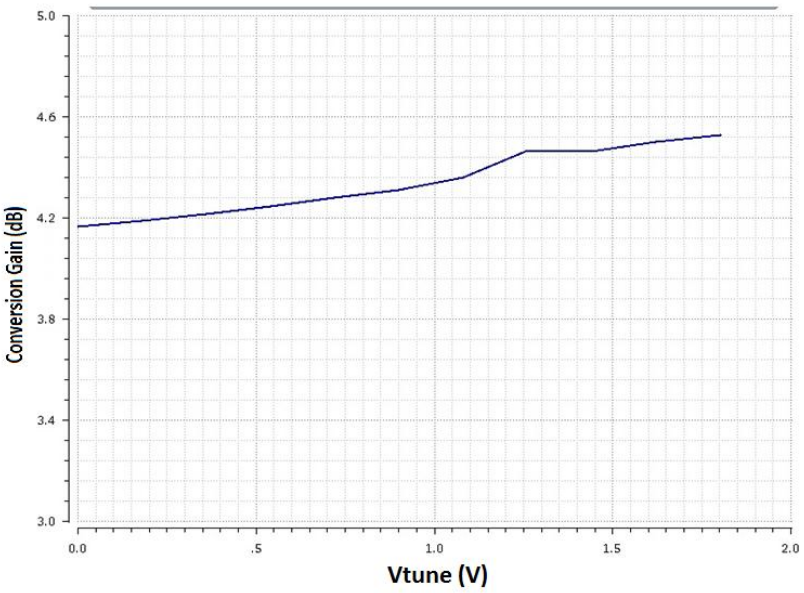

Figure 6.5 : Conversion gain of mixer.

Figure 6.5 shows that the mixer has about 4.5 dB conversion gain. Monte Carlo simulation is required to simulate LO feedthrough and sideband rejection because in this double balanced structure, these signals are canceled at the output. Mismatch and coupling cause LOFT and SBR at the output. Monte Carlo simulation results are shown in Figure 6.6 and Figure 6.7.

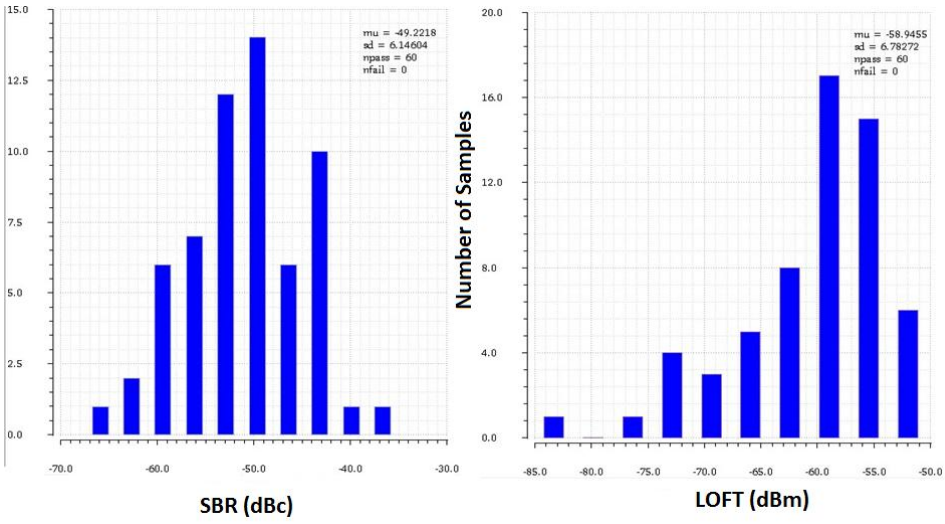

Figure 6.6 : LOFT and SBR Monte Carlo simulation results.

It can be seen from Figure 6.6 that, SBR is about - 50 dBc and LOFT is about - 60 dBm. In Monte Carlo simulation, 60 points are simulated.

It can be concluded from this simulation that oscillator provides sufficient quadrature signals that result in – 50 dBc sideband rejection. Using this double balanced mixer structure and quadrature oscillator, very clean RF signal can be obtained at the output. Usually – 40 dBc rejection is sufficient for most applications in RF systems.

Another important parameter for mixer is noise figure. HBNOISE simulation is done and NF simulation result is shown in Figure 6.7

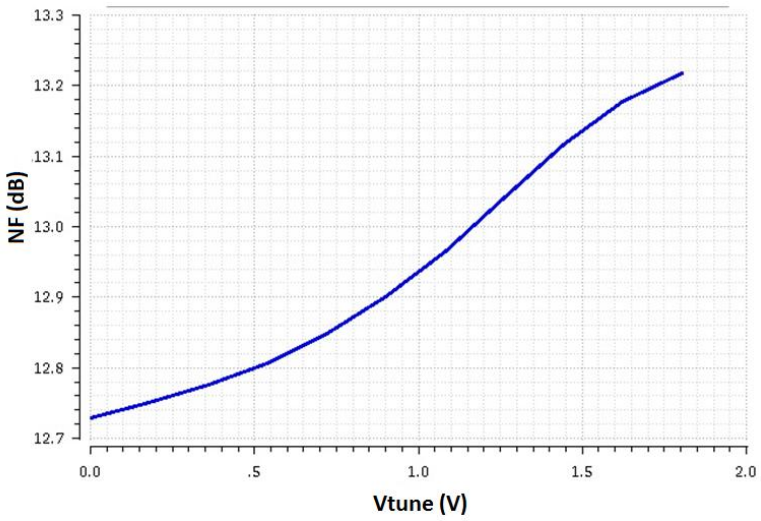

Figure 6.7 : Noise figure versus V_{tune}.

For 2.4 GHz operation, about 13 dB noise figure is obtained.

Linearity performance is another important parameter of the mixers. Multi-tanh structure shown in Figure 6.8 is used to improve linearity of the circuit.

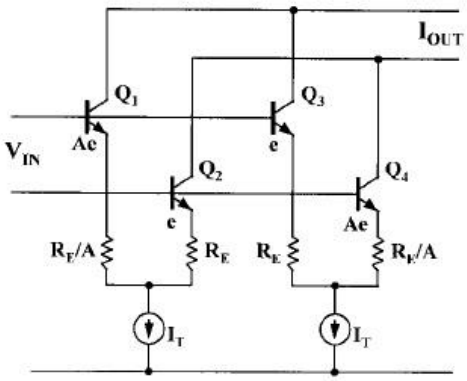

Figure 6.8 : Multi – tanh doublet with emitter resistance [21].

Two tone test is applied for the IP3 simulation. The simulation result is shown in Figure 6.9.

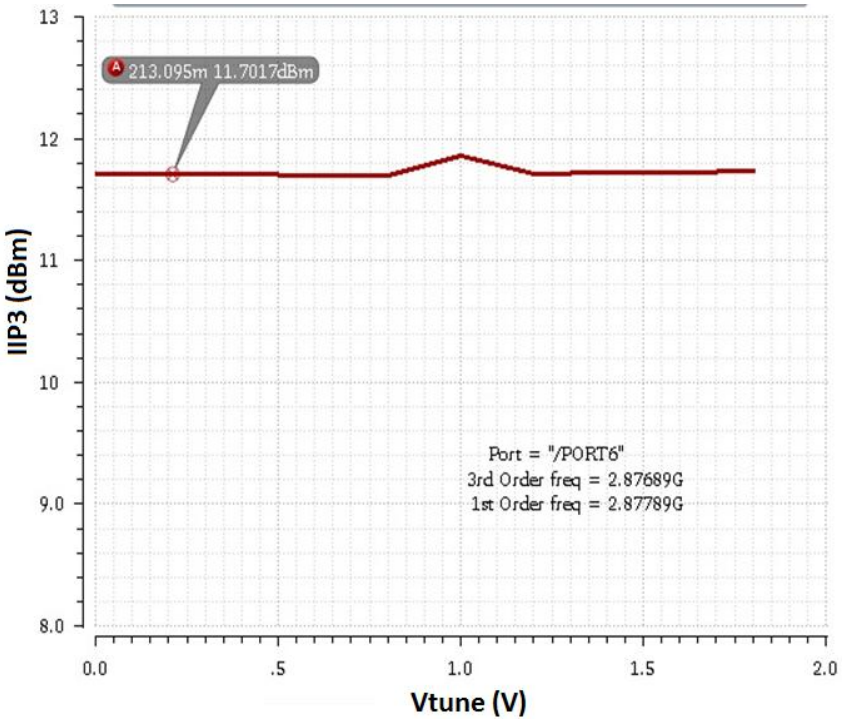

Figure 6.9 : IP3 simulation result.

Another important parameter of mixer is the RF port return loss. The impedance seen from the RF port should be matched to 50 Ω to transform power perfectly. The return loss is shown in Figure 6.10.

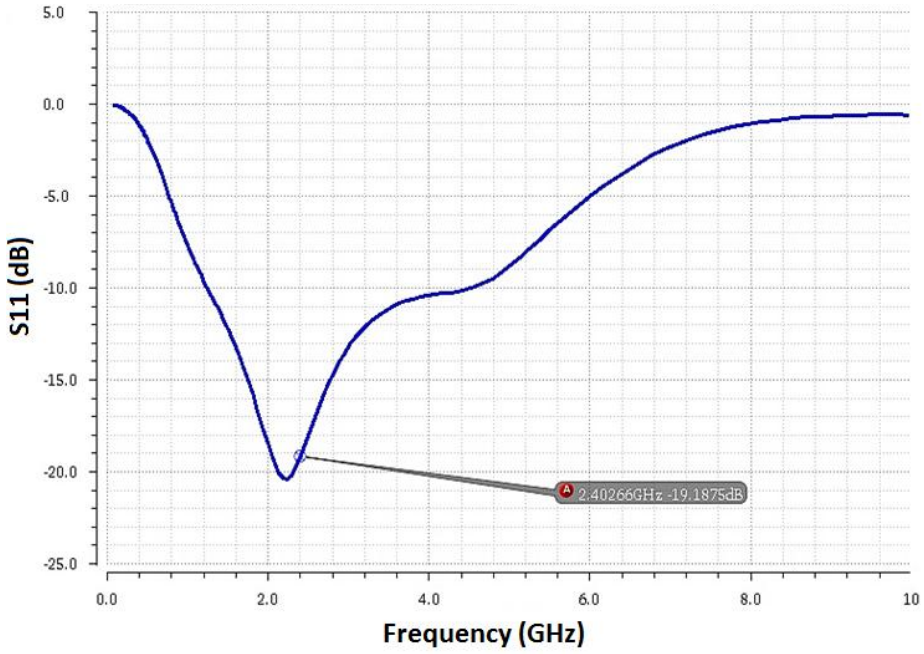

Figure 6.10 : RF output return loss.

In Figure 6.10, the RF return loss around 2.4 GHz is about -20 dB. Usually less than -10 dB is sufficient for 50 Ω systems.

Overall performance of the oscillator + mixer circuit is shown in Table 6-1 below.

Table 6-1: Overall performance of relaxation oscillator + mixer

	This Work	**[22]**	**[23]**	**[24]**	**[25]**
VCC (V)	3.3	2	1.8	1	1
Power Consumption (mW)	33	18	15.8	40	11
Operation Frequency (GHz)	1.9 – 2.8	2.4	5.25	1.3 – 4.1	3 - 5
Conversion Gain	4.5	-18	6.3	5.5	6.5
LOFT	-60	< -50	-	-	< -40
SBR	-50	-	-	-	-
NF	13	-	-	14.5	12.5
IIP3	11.7	6.5	- 8.9	0	11.6
Return Loss	-20	-	-	-	-

Table 6-1 shows that, relaxation oscillator and up conversion mixer structure can be used in 2.4 GHz RF application contentedly.

7. CONCLUSION

This chapter concludes the research work presented in this thesis. LC, ring, BPF and relaxation type VCO circuits are designed at 2.4 GHz oscillation frequency. The overall performance of the designs is compared at Table 6-1.

Table 7-1: Overall performance comparison of designed VCO structures

	LC VCO	**Ring VCO**	**BPF VCO**	**Relax. VCO**
VCC (V)	1.8	1.8	1.8	1.8
Power Consumption (mW)	9	9	5.4	48
Oscillation Frequency (GHZ)	2.4	2.4	2.4	2.4
Tuning Range (GHz)	2.1 – 2.6	1.4 – 2.6	2.2– 2.6	1.9 – 2.8
K_{VCO}(MHZ/V)	430	2300	220	1300
Phase Noise (dBc/Hz) at 1MHz	-120	-97.3	-95.8	-108.5
Temperature Variation (-40C to 85 C)	110 MHz	330 MHz	130 MHz	120 MHz
Process Variation (-3σ to 3σ)	50 MHz	1000 MHz	300 MHz	40 MHz
Technology	0.18 µm	0.18 µm	0.18 µm	0.18 µm

The highest quality factor can be obtained with LC VCO structure. Therefore, best phase noise performance is obtained in LC design as expected. However, its fabrication cost is highest due to the integrated inductor. Also, it is required more

detailed design and modeling issue. Usually in LC VCO designs, the used inductor is slightly changed to generate different design versions that increase the cost.

Ring VCO structure is easier to design than LC VCO. It can be designed in standard CMOS processes that mean cheap fabrication cost. Also, die area is very small with related to LC VCO. Tuning range performance is best for ring structure. However, phase noise performance is poor and supply sensitivity is very high with related to other structures.

BPF structure also has similar performance with ring structure. Also, temperature, process and supply sensitivity is better than ring structure. It also has advantages of ring structure like low cost, easy design. However, their phase noise performances are still far away with related to LC VCO.

Relaxation oscillator structure has best phase noise performance (-108.5 dBc/Hz at 1MHz) without using inductor. Therefore, it has low cost and easy design advantages. Another important advantage of this structure, obtain accurate quadrature signals that is very important for double balanced mixer structure. In LC VCO structures, the phase noise performance is decreased to have quadrature outputs. Therefore, this relaxation oscillator structure might be considered as good alternative to LC structures. The disadvantage of this structure is that it requires more power than other structures.

7.1 Future Work

As a future work, the inductor can be optimized for higher quality factor using different shapes or using transformer structures in LC structure. Temperature, process and power supply sensitivity of the ring oscillator can be reduced by adding compensation circuits. For BPF oscillator structure, if the used OTA is designed with lower parasitic like in 90 nm process or 45 nm, the performance of the circuit will be improved. In relaxation oscillator structure, transistors with higher f_T can decrease the power consumption.

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APPENDICES

APPENDIX A: PSS and PNOISE Analysis Setup on Cadence Analog Environment

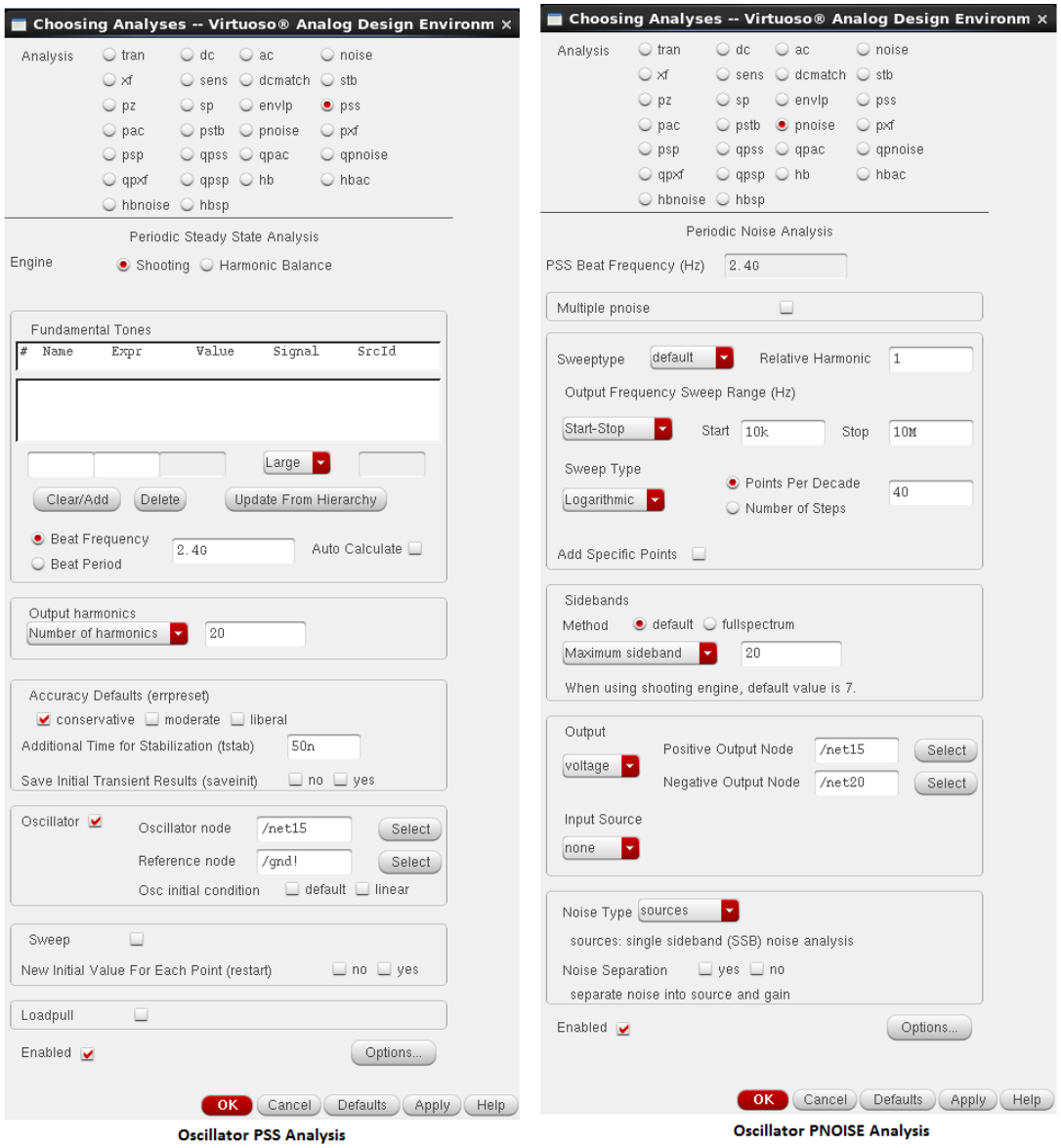

Figure A.1: PSS and PNOISE Simulation Setup

APPENDIX B: Netlists

LC VCO

```
// Generated for: spectre
// Generated on: Jan 28 18:37:57 2013
// Design library name: VCO
// Design cell name: LC
// Design view name: schematic
simulator lang=spectre
global 0
parameters vcc=1.8 ibias=2m vtune=0.5
include "one_sigma.scs" section=ONE_SIGMA
include "statistics.scs" section=params
include "global.scs" section=NOM
include "ind.scs" section=NOM
include "npn.scs" section=NOM
include "lvres.scs" section=NOM
include "hvres.scs" section=NOM
include "salres.scs" section=NOM
include "rnw.scs" section=NOM
include "n1p8.scs" section=NOM
include "p1p8.scs" section=NOM
include "n3p3_5p0.scs" section=NOM
include "p3p3_5p0.scs" section=NOM
include "cap.scs" section=NOM
include "hpvar.scs" section=NOM
include "hppnp.scs" section=NOM
include "npn_rth.scs" section=NO_RTH
include "circuit.scs" section=CIRCUIT
include "fet.scs" section=BSIM

// Library name: VCO
// Cell name: LC
// View name: schematic
R0 (vcc net0115 sub) rpp3t w=4u l=4.4u m=1 strips=1
C3 (net9 net9 sub) c3t_mim w=30u l=28.0u caprows=1 capcols=1
m=1
L3 (net063 net038 sub) ind_3u xsize=150.00000u
ysize=150.00000u w=6u s=2u \
        n=5 ls=3.64593e-09 rvia=0.0305556 rl1=6.94544
ll1=1.03849e-09 \
        rl2=15.5305 ll2=4.64426e-10 rl3=34.7272 ll3=2.07698e-
10 \
        rl4=77.6523 ll4=9.28852e-11 cp=2.2206e-15 cx=1.1103e-
15 \
        cox1=4.06551e-14 cox2=3.59336e-14 csub1=6.25703e-14 \
        csub2=6.25703e-14 rsub1=176.552 rsub2=176.552 lval=-1
rp=-1 \
rsub=-1 rs=-1 csub=-1 wf=3u
M5 (net0115 net0115 0 0) nfets wf=50u lf=1u nf=20 slices=1
cur=0 m=5
M4 (net058 net0115 0 net043) nfets wf=50u lf=1u nf=20 slices=1
cur=0 m=5
```

```
M2 (net038 net063 net058 gnd) nfets wf=5u lf=180.0n nf=5
slices=1 cur=0 \
        m=1
M3 (net063 net038 net058 gnd) nfets wf=5u lf=180.0n nf=5
slices=1 cur=0 \
        m=1
M7 (vtune net063 vtune vcc) pfets wf=14.0u lf=180.0n nf=60
slices=1 cur=0 \
        m=1
M0 (vtune net063 vtune vcc) pfets wf=14.0u lf=180.0n nf=60
slices=1 cur=0 \
        m=1
M9 (vtune net038 vtune vcc) pfets wf=14.0u lf=180.0n nf=60
slices=1 cur=0 \
        m=1
M8 (vtune net038 vtune vcc) pfets wf=14.0u lf=180.0n nf=60
slices=1 cur=0 \
        m=1
M1 (net063 net038 vcc vcc) pfets wf=5u lf=180.0n nf=15
slices=1 cur=0 m=1
M6 (net038 net063 vcc vcc) pfets wf=5u lf=180.0n nf=15
slices=1 cur=0 m=1
V2 (vtune 0) vsource dc=vtune type=dc
V0 (vcc 0) vsource dc=vcc type=dc
ic net063=0
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-
12 temp=27 \
tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5
maxwarns=5 \
digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
checklimitdest=psf
tran tran stop=20n errpreset=conservative write="spectre.ic" \
writefinal="spectre.fc" annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000
annotate=status
dcOpInfo info what=oppoint where=rawfile
pss ( net063 0 ) pss fund=2.4G harms=11
+    errpreset=conservative tstab=40n annotate=status
pnoise ( net063 net038 ) pnoise relharmnum=1 start=1k
+       stop=10M dec=40 maxsideband=20 annotate=status
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts  where=rawfile
saveOptions options save=all pwr=all subcktprobelvl=2
```

Ring VCO

```
// Generated for: VCO
// Generated on: Jan 24 14:31:10 2013
// Design library name: deneme
// Design cell name: basic_ring
// Design view name: schematic
simulator lang=spectre
global 0 sub!
parameters vctrl=860m vcc=1.8 sigma=0 hppnp_global_sigma=sigma
\
    hpvar_global_sigma=sigma cap_global_sigma=sigma \
    p3p3_5p0_global_sigma=sigma n3p3_5p0_global_sigma=sigma \
    p1p8_global_sigma=sigma n1p8_global_sigma=sigma
rnw_global_sigma=sigma \
    salres_global_sigma=sigma hvres_global_sigma=sigma \
    lvres_global_sigma=sigma npn_global_sigma=sigma
ind_global_sigma=sigma \
    global_global_sigma=sigma
include "one_sigma.scs" section=ONE_SIGMA
include "statistics.scs" section=params
include "global.scs" section=X_SIGMA
include "ind.scs" section=X_SIGMA
include "npn.scs" section=X_SIGMA
include "lvres.scs" section=X_SIGMA
include "hvres.scs" section=X_SIGMA
include "salres.scs" section=X_SIGMA
include "rnw.scs" section=X_SIGMA
include "n1p8.scs" section=X_SIGMA
include "p1p8.scs" section=X_SIGMA
include "n3p3_5p0.scs" section=X_SIGMA
include "p3p3_5p0.scs" section=X_SIGMA
include "cap.scs" section=X_SIGMA
include "hpvar.scs" section=X_SIGMA
include "hppnp.scs" section=X_SIGMA
include "npn_rth.scs" section=NO_RTH
include "circuit.scs" section=CIRCUIT
include "fet.scs" section=BSIM

// Library name: VCO
// Cell name: delaycell_man
// View name: schematic
subckt delaycell_man gnd inn inp outn outp vbias vbp vcc
    M5 (net11 vbias gnd gnd) nfet w=10u l=640n nf=8 slices=1
cur=0 m=1 \
as=3.475p ad=2.9p ps=13.195u pd=10.58u
    M11 (outp inn net11 gnd) nfet w=4u l=180n nf=3 slices=1
cur=0 m=1 \
as=1.46667p ad=1.46667p ps=6.06667u pd=6.06667u
    M12 (outn inp net11 gnd) nfet w=4u l=180n nf=3 slices=1
cur=0 m=1 \
as=1.46667p ad=1.46667p ps=6.06667u pd=6.06667u
    C0 (net11 gnd) capacitor c=2p
    M1 (outp vbp vcc vcc) pfet w=4u l=860n nf=6 slices=1 cur=0
m=1 \
as=1.46667p ad=1.16p ps=6.06667u pd=4.58u
```

```
    M2 (outn vbp vcc vcc) pfet w=4u l=860n nf=6 slices=1 cur=0
m=1 \
as=1.46667p ad=1.16p ps=6.06667u pd=4.58u
    M6 (outn outn vcc vcc) pfet w=4u l=860n nf=5 slices=1
cur=0 m=1 \
as=1.344p ad=1.344p ps=5.472u pd=5.472u
    M4 (outp outp vcc vcc) pfet w=4u l=860n nf=5 slices=1
cur=0 m=1 \
as=1.344p ad=1.344p ps=5.472u pd=5.472u
ends delaycell_man
// End of subcircuit definition.

// Library name: deneme
// Cell name: basic_ring
// View name: schematic
R0 (vcc i1200u sub!) rpp3t w=7u l=(7u) m=1 strips=2
V0 (vcc 0) vsource dc=vcc type=dc
I14 (0 net22 net23 net15 net20 i1200u vbp vcc) delaycell_man
I13 (0 net17 net18 net22 net23 i1200u vbp vcc) delaycell_man
I12 (0 net20 net15 net17 net18 i1200u vbp vcc) delaycell_man
M1 (vbp vbp vcc vcc) pfet w=4u l=860n nf=12 slices=1 cur=0 m=1
as=1.31333p \
ad=1.16p ps=5.32333u pd=4.58u
M19 (vbp i1200u 0 0) nfet w=10u l=640n nf=8 slices=1 cur=0 m=1
as=3.475p \
ad=2.9p ps=13.195u pd=10.58u
M2 (i1200u i1200u 0 0) nfet w=10u l=640n nf=8 slices=1 cur=0
m=1 as=3.475p \
ad=2.9p ps=13.195u pd=10.58u
ic net18=0
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-
12 temp=27.0 \
tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5
maxwarns=5 \
digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
checklimitdest=psf
dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000
annotate=status
dcOpInfo info what=oppoint where=rawfile
tran tran stop=20n write="spectre.ic" writefinal="spectre.fc"
\
annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts  where=rawfile
saveOptions options save=allpub subcktprobelvl=2
```

RC BPF based VCO

```
// Generated for: spectre
// Generated on: Jan 28 17:07:55 2013
// Design library name: VCO
// Design cell name: OTA_osc
// Design view name: schematic
simulator lang=spectre
global 0 sub!
parameters vcc=1.8 vtune=1.25 c1=47f c2=188f r2=400 r1=320
sigma=0 \
    hppnp_global_sigma=sigma hpvar_global_sigma=sigma \
    cap_global_sigma=sigma p3p3_5p0_global_sigma=sigma \
    n3p3_5p0_global_sigma=sigma p1p8_global_sigma=sigma \
    n1p8_global_sigma=sigma rnw_global_sigma=sigma \
    salres_global_sigma=sigma hvres_global_sigma=sigma \
    lvres_global_sigma=sigma npn_global_sigma=sigma
ind_global_sigma=sigma \
    global_global_sigma=sigma
include "one_sigma.scs" section=ONE_SIGMA
include "statistics.scs" section=params
include "global.scs" section=X_SIGMA
include "ind.scs" section=X_SIGMA
include "npn.scs" section=X_SIGMA
include "lvres.scs" section=X_SIGMA
include "hvres.scs" section=X_SIGMA
include "salres.scs" section=X_SIGMA
include "rnw.scs" section=X_SIGMA
include "n1p8.scs" section=X_SIGMA
include "p1p8.scs" section=X_SIGMA
include "n3p3_5p0.scs" section=X_SIGMA
include "p3p3_5p0.scs" section=X_SIGMA
include "cap.scs" section=X_SIGMA
include "hpvar.scs" section=X_SIGMA
include "hppnp.scs" section=X_SIGMA
include "npn_rth.scs" section=NO_RTH
include "circuit.scs" section=CIRCUIT
include "fet.scs" section=BSIM
// Library name: VCO
// Cell name: OTA_osc
// View name: schematic
M7 (vtune net019 vtune vcc) pfet w=4u l=180n nf=1 slices=1
cur=0 m=10 \
as=2.08p ad=2.08p ps=9.04u pd=9.04u
M1 (vtune net030 vtune vcc) pfet w=4u l=180n nf=1 slices=1
cur=0 m=10 \
as=2.08p ad=2.08p ps=9.04u pd=9.04u
M3 (net019 net2 vcc vcc) pfet_rf w=5u l=180n nf=6 slices=1
cur=0 \
sa=480.00n sb=480.00n ring_sub=1 ngcon=1 postlayout=0 nqs=1
m=1
M2 (net030 net4 vcc vcc) pfet_rf w=5u l=180n nf=6 slices=1
cur=0 \
sa=480.00n sb=480.00n ring_sub=1 ngcon=1 postlayout=0 nqs=1
m=1
```

```
C2 (net019 net4 sub!) c3t_mim w=18u l=10u caprows=1 capcols=1
m=1 \
        cmima_nom=1m cmima_max=1.15m cmimp_nom=100p
cmimp_max=130p \
        coxa_nom=7.3u coxa_max=8.1u coxp_nom=31.8p
coxp_max=33.5p \
        rshtp_nom=18m rshtp_max=22m rshbp_nom=66m
rshbp_max=86m tc=36u \
tbp=620n ttp=1.59u rvia=2.2 wvia=500n
C1 (net030 net2 sub!) c3t_mim w=18u l=10u caprows=1 capcols=1
m=1 \
        cmima_nom=1m cmima_max=1.15m cmimp_nom=100p
cmimp_max=130p \
        coxa_nom=7.3u coxa_max=8.1u coxp_nom=31.8p
coxp_max=33.5p \
        rshtp_nom=18m rshtp_max=22m rshbp_nom=66m
rshbp_max=86m tc=36u \
tbp=620n ttp=1.59u rvia=2.2 wvia=500n
V2 (vtune 0) vsource dc=vtune type=dc
V0 (vcc 0) vsource dc=vcc type=dc
M6 (net02 net02 0 0) n3p3fet w=50u l=3u nf=60 slices=1 cur=0
m=5 \as=14.8833p ad=14.5p ps=52.262u pd=50.58u
M4 (net027 net02 0 0) n3p3fet w=50u l=3u nf=60 slices=1 cur=0
m=5 \as=14.8833p ad=14.5p ps=52.262u pd=50.58u
R8 (net07 net4 sub!) rpp3t w=4u l=(6.6u) m=1 strips=1
R7 (net2 net07 sub!) rpp3t w=4u l=(6.6u) m=1 strips=1
R6 (net07 net019 sub!) rpp3t w=4u l=(5.2u) m=1 strips=1
R5 (net030 net07 sub!) rpp3t w=4u l=(5.2u) m=1 strips=1
R4 (vcc net02 sub!) rpp3t w=4u l=(3.6u) m=2 strips=1
M0 (net019 net2 net027 net027) nfet w=5u l=180n nf=3 slices=1
cur=0 m=1 \
as=1.7p ad=1.7p ps=7.34667u pd=7.34667u
M5 (net030 net4 net027 net027) nfet w=5u l=180n nf=3 slices=1
cur=0 m=1 \
as=1.7p ad=1.7p ps=7.34667u pd=7.34667u
ic net2=0
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-
12 temp=27.0 \
tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5
maxwarns=5 \
digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
checklimitdest=psf
dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000
annotate=status
dcOpInfo info what=oppoint where=rawfile
tran tran stop=20n errpreset=conservative write="spectre.ic" \
writefinal="spectre.fc" annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts  where=rawfile
saveOptions options save=allpub subcktprobelvl=2
```

Relaxation VCO

```
// Generated for: spectre
// Generated on: Jan 28 18:10:31 2013
// Design library name: VCO
// Design cell name: RC
// Design view name: schematic_108dbc_2.4ghz_osc
simulator lang=spectre
global 0 sub!
parameters vcc=1.8 vtune=850m n2=6 n1=12 i2=2m i=4m r=120
sigma=0 \
    hppnp_global_sigma=sigma hpvar_global_sigma=sigma \
    cap_global_sigma=sigma p3p3_5p0_global_sigma=sigma \
    n3p3_5p0_global_sigma=sigma p1p8_global_sigma=sigma \
    n1p8_global_sigma=sigma rnw_global_sigma=sigma \
    salres_global_sigma=sigma hvres_global_sigma=sigma \
    lvres_global_sigma=sigma npn_global_sigma=sigma
ind_global_sigma=sigma \
    global_global_sigma=sigma
include "one_sigma.scs" section=ONE_SIGMA
include "statistics.scs" section=params
include "global.scs" section=STAT
include "ind.scs" section=STAT
include "npn.scs" section=STAT
include "lvres.scs" section=STAT
include "hvres.scs" section=STAT
include "salres.scs" section=STAT
include "rnw.scs" section=STAT
include "n1p8.scs" section=STAT
include "p1p8.scs" section=STAT
include "n3p3_5p0.scs" section=STAT
include "p3p3_5p0.scs" section=STAT
include "cap.scs" section=STAT
include "hpvar.scs" section=STAT
include "hppnp.scs" section=STAT
include "npn_rth.scs" section=NO_RTH
include "circuit.scs" section=CIRCUIT
include "fet.scs" section=BSIM

// Library name: VCO
// Cell name: RC
// View name: schematic_108dbc_2.4ghz_osc
R6 (net022 0 sub!) rpp3t w=4u l=(7u) m=3 strips=1
R4 (net019 0 sub!) rpp3t w=4u l=(7u) m=3 strips=1
R0 (net03 a2 sub!) rpp3t w=4u l=(6u) m=3 strips=1
R2 (net03 a1 sub!) rpp3t w=4u l=(6u) m=3 strips=1
M1 (a1 a2 net019 0) nfet w=10u l=180n nf=12 slices=1 cur=0 m=1
as=3.28333p \
ad=2.9p ps=12.3233u pd=10.58u
M0 (a2 a1 net022 0) nfet w=10u l=180n nf=12 slices=1 cur=0 m=1
as=3.28333p \
ad=2.9p ps=12.3233u pd=10.58u
C3 (a1 0) capacitor c=50.0f
C4 (a2 0) capacitor c=50.0f
V3 (vcc 0) vsource dc=3.3 type=dc
V1 (vtune 0) vsource dc=vtune type=dc
```

```
V0 (net03 0) vsource dc=vcc type=dc
M3 (vtune net022 vtune vcc) pfet w=4u l=180n nf=33 slices=1
cur=0 m=10 \
as=1.18788p ad=1.18788p ps=4.71515u pd=4.71515u
M2 (vtune net019 vtune vcc) pfet w=4u l=180n nf=33 slices=1
cur=0 m=10 \
as=1.18788p ad=1.18788p ps=4.71515u pd=4.71515u
ic a1=0
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-
12 temp=27.0 \
tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5
maxwarns=5 \
digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
checklimitdest=psf
dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000
annotate=status
dcOpInfo info what=oppoint where=rawfile
tran tran stop=100n write="spectre.ic" writefinal="spectre.fc"
\
annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
pss ( a1 0 ) pss fund=2.2G harms=3
errpreset=conservative
+    tstab=40n  annotate=status
pnoise ( a1 a2 ) pnoise sweeptype=relative relharmnum=1
+       start=1k  stop=10M  maxsideband=20  annotate=status
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts  where=rawfile
saveOptions options save=allpub subcktprobelvl=2
```

CURRICULUM VITAE

Name Surname: Mehmet Batı

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- 4 weeks as an intern **(** 2007)

ITU VLSI Lab.

- 5 weeks as an intern (2008)

Microelectronic R&D Design Center

- 4 weeks as an intern (2008)

Hittite Microwave Corporation

- IC Design Engineer (2009 - …)