ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

DESIGN OF EFFICIENT WIDEBAND POWER AMPLIFIERS

Ph.D. THESIS

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Department of Electronics and Communication Engineering

Electronics Engineering Programme

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

GENİŞ BANTLI VERİMLİ GÜÇ KUVVETLENDİRİCİLERİN TASARIMI

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To my family

FOREWORD

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ABBREVIATIONS

PA	**:** Power Amplifier
IC	**:** Integrated Circuit
PAE	**:** Power Added Efficiency
DE	**:** Drain Efficiency
IMD	**:** Inter Modulation Distortion
UWB	**:** Ultra Wideband
ITU-R	**:** International Telecommunication Union Radiocommunication
MMIC	**:** Monolithic Microwave Integrated Circuit
BJT	**:** Bipolar Junction Transistor
HBT	**:** Heterojunction Bipolar Transistors
HEMT	**:** High Electron Mobility Transistor
MESFET	**:** Metal Semiconductor Field Effect Transistor
LDMOS	**:** Laterally Diffused Metal Oxide Semiconductor
2-DEG	**:** Two-Dimensional Electron Gas
ATL	**:** Artificial Transmission Line
DPA	**:** Distributed Power Amplifier
TWPA	**:** Travelling Wave Power Amplifier
VSWR	**:** Voltage Standing Wave Ratio
RFC	**:** Radio Frequency Choke
CAD	**:** Computer Aided Design
LTCC	**:** Low Temperature Co-fired Ceramic
DUT	**:** Device Under Test
SSTWPA	**:** Single-Stage Travelling Wave Power Amplifier
CSSTWPA	**:** Cascaded Single-Stage Travelling Wave Power Amplifier
DSTWPA	**:** Double Stage Travelling Wave Power Amplifier

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DESIGN OF EFFICIENT WIDEBAND POWER AMPLIFIERS

SUMMARY

Beyond the communication systems, there are many radar, electronic warfare, microwave system front/back ends, digital/optical communication equipment, which need to generate, amplify and process wideband signals. Among all sub-system blocks, wideband PAs are the most important parts. Both the output power delivered to the given load (e.g. antenna) and the overall wideband system efficiency are directly related to the PA performance. The heat generated especially in high power and high volume amplifiers needs to be removed from the environment and this process would be expensive when the amplifier occupies high volume by construction. Thus, high efficient power amplifiers are needed to overcome these problems.

Nowadays, with the help of sophisticated technologies, the design of wideband PAs are getting more attention. Some of the technologies including relatively cheap silicon based SiGe, LDMOS, SiC and III–V compounds like GaAs and GaN devices are developed with the help of HBT, (P)HEMT and MESFET process technologies. Integrated technologies seem to have some drawbacks when designing such wideband circuitries. The most effective drawback of such IC technologies is the substrate loss, which most manifests itself when the frequency increases. Silicon based technologies suffer from these loss effects and unfortunately, they are not suitable to implement MMIC techniques successively. Moreover, there are many topological investigations to improve overall performance of wideband PAs in integrated circuits. One of the most well-known and used design techniques to implement wideband PAs is the distributed amplification technique, where the use of inherent parasitic capacitances at the input and output terminals of the transistor together with the external inductive elements forms artificial transmission lines.

In this thesis, distributed amplification became the starting topology for the proposed techniques. Initially, the number of devices was reduced to only a single device and the input artificial transmission line is conserved and modified as lossy. This core design circuitry was called “single-stage travelling wave power amplifier” (SSTWPA). By this way, gain flatness is provided in the entire band. Additionally, a series-series feedback was applied to given single transistor, which widened the bandwidth. Moreover, at the output side, load-line match was applied to construct the output line in which the terminating impedance was removed. Thus, the output power and the efficiency were improved. In addition to this design, a second PA circuit was designed as the cascaded version of the proposed core, where the input driver core feeds two another identical cores in parallel configuration and their outputs are combined to increase the output power by twofold over the desired frequency bandwidth. We have called this implementation as CSSTWPA. These two

designs were realized using 0.35µm SiGe HBT technology. Measurement results of the amplifiers closely agree with simulation results.

From the output matching network point of view, the maximum linear output power could be obtained from class-A operated transistor by simply applying load-line matching. Additionally, it is possible to use load-pull techniques as the extended version of the load-line approach. Load-pulling is more complicated approach than the load-line and it finds out optimum $Z_L(j\omega)$ impedances for the given device in the wideband. Process continues with the synthesis of the matching network, which ensures the maximum power is delivered to predefined load impedance (e.g. 50Ω). Although there are many well-defined analytical solutions to wideband matching problem, this is not an easy task at all. Most solutions come up with high-order networks, which are hard to realize over lossy IC processes and discrete elements. From these facts, simplified design approaches seem to be essential and useful to overcome design difficulties and complexity of the circuits.

According to given explanations, in the second phase of the work, a new load-pull based graphical technique was proposed to design simple networks to fulfil matching purpose over wideband. 0.25µm GaAs PHEMT MMIC technology was selected to design and implement latter designs. Series-series feedback had been formerly used in SiGe PA design and this technique was replaced with the capacitively coupled transistor in GaAs PHEMT, which lowers the input capacitance seen by the artificial transmission line. The new wideband SSTWPA successfully operated in the 1 to 8 GHz. Continuously, a cascaded version of GaAs SSTWPA was proposed as the new design strategy, which offers a complete systematic to design both driver and power stages. This technique was shown to use large signal power definitions in the design equations. In addition to these GaAs MMIC designs, an ac grounded transmission line is offered and implemented as the wideband RFC, which helps to minimize the total output capacitance of the power devices where the bandwidth of the stages are directly proportional to output capacitance of the transistors.

In the last phase of the work, a systematic technique based on a susceptance minimizing concept at the output matching is presented. The proposed approach uses two main sub-blocks which are: a short-circuited transmission-line for susceptance minimizing and multisection transformer for the remaining matching purpose. The design procedure is investigated conceptually and simple theoretical analyses are given to show that how the proposed method could help to simplify wideband design by means of computer aided optimizations. Moreover, the given approach not only improves the output power and efficiency performance of the transistor but also takes care of the biasing network simultaneously over the wide range of the frequencies.

To sum up, this thesis study proposes some design techniques and modifications, which simplifies both the design procedures and circuit complexities. In this respect, output power and the efficiency is improved with the help of simple and reduced number of matching elements, in which both substrate and parasitic loss effects are compensated.

GENİŞ BANTLI VERİMLİ GÜÇ KUVVETLENDİRİCİLERİN TASARIMI

ÖZET

Temel telsiz haberleşme uygulamalarının ötesinde, başta radar ve askeri elektronik harp sistemleri olmak üzere, sayısal optik haberleşme sistemleri ve mikrodalga ekipmanları, geniş bant karakteristikli darbe işaretlerini oluşturacak, kuvvetlendirecek ve işleyebilecek alt sistem bloklarına ihtiyaç duymaktadır. Geniş bantlı güç kuvvetlendiricileri ise bu uygulamaları oluşturan sistem alt bloklarının en önemlisidir. Anten gibi uç birimler üzerinden aktarılmak istenen gücün miktarı doğrudan güç kuvvetlendiricinin performansıyla ilişkilidir. Benzer biçimde, geniş bantlı sistemin verimi, güç kuvvetlendiricisinin verimiyle doğrudan ilişkilidir. Dolayısıyla özellikle yapısal olarak yer kaplayan ve yüksek güçlerde çalışan kuvvetlendiricilerde ortaya çıkan ısının ortamdan uzaklaştırılması ve bu sistemlerin ihtiyaç duyduğu yüksek besleme gücü problemlerinin en aza indirilmesi, geniş bantlarda ve yüksek verimlerde çalışan kuvvetlendiricilerin tasarımıyla mümkündür.

Günümüzde, mikrodalga frekanslarında, ucuz maliyetli silisyum tabanlı SiGe, LDMOS ve SiC gibi malzemelerin yanında, yüksek frekans ve yüksek güç özellikleriyle öne çıkan GaAs ve GaN gibi III–V grubu ürünleri, HBT, (P)HEMT ve MESFET gibi transistör teknolojilerinde yoğun olarak kullanılmaktadır. Tümleştirmeye uygun kuvvetlendiriciler için çıkışta elde edilebilir gücün özellikle frekans yükseldikçe azalması, kullanılan teknoloji ve taban malzeme özellikleriyle doğrudan orantılıdır. Söz gelimi silisyum tabanlı birçok teknoloji, sahip olduğu olumlu ayrıcalıkların yanında yüksek frekans ve yüksek güç uygulamalarında taban kayıpları dolayısıyla, ilgili devre bloklarının tasarımında birçok zorluğu da beraberinde getirmektedir.

Devre topolojisi açısından bakıldığında, literatürde güç kuvvetlendiricilerini tümleşik olarak gerçekleştirmek üzere çeşitli yapılar önerilmiştir. Giriş ve çıkışta yapay hatlar kullanan dağılmış parametreli güç kuvvetlendiricileri de yüksek geniş bant başarımı sebebiyle sıklıkla tercih edilen temel yapılardan birisidir. Transistör giriş ve çıkış kapasitelerinin ayrı ayrı yapay iletim hatlarına dahil edilmesiyle, kazancı düzgün ve giriş-çıkış için yansıma oranı düşük olan yapılar geniş bir bantta elde edilebilmektedir. Bununla birlikte, özellikle çıkış hattındaki sonlandırma empedansı nedeniyle, transistörlerde üretilen gücün yarısı heba olmaktadır. Hat davranışlarının geniş bantlarda düzgün olması, çoğunlukla transistör giriş ve çıkış kapasitelerinin doğrusal olmasıyla mümkün olacağından, bu yapılarda transistörler A-sınıfı çalışacak şekilde kutuplanmaktadır. Ayrıca yüksek frekanslara gidildiğinde ardışık transistörler arası gecikmeler önem kazandığından, güçlerin aynı fazda toplanamaması ve dolayısıyla da devre verimin önemli oranda azalması söz konusu olmaktadır. Sonuç olarak da, literatürde önerilen klasik dağılmış parametreli güç kuvvetlendiricilerin büyük bir kısmında verim %15'nin altında kalmaktadır.

Bu tez kapsamında gerçekleştirilen çalışmalarda ilk olarak, yukarıda bahsedilen klasik dağılmış parametreli güç kuvvvetlendiricisi temel alınmıştır. Bu doğrultuda, klasik topolojinin geniş bant çalışma özelliklerini koruyan ve verimini iyileştiren basit yaklaşımlar sunulmuştur. Klasik yapıda, yüksek hızlarda ortaya çıkan ardışık kazanç katları arasındaki gecikmeler, transistörlerin kollektör/savak uçlarında, çıkış yüküyle aynı fazda olmayan yükleme etkilerini doğurur. Bunun sonucunda, yapıdaki kimi transistörler, devrede güç sağlayan diğerlerinden ayrı olarak direnç yükü gibi davranarak güç tüketirler. Bu durum klasik yapının yüksek frekanslardaki düşük veriminin en önemli sebebidir. Buradan yola çıkarak, klasik yapıdaki kazanç katlarını teke düşüren ve tek transistor kullanan bir yapı bahsedilen verim problemi için uygun bir çözüm olarak görülmüştür. Klasik yapıdaki giriş hattının tek transistörlü halde de korunmasıyla geniş bant davranışı devam ettirilebilir. Teke inen transistor sayısıyla birlikte daha az sayıda yapay hat elemanı kullanılmaktadır. Bu durumun olası bir sakıncası, giriş hattı davranışının frekansla düzgün değişmemesidir. Bundan dolayı da kazanç eğrisi dalgalılık gösterir. Bir diğer sakınca da, geniş bantlı uygulamalar açısından önem taşıyan grup gecikmesinin, frekansın bir fonksiyonu olarak değişiklik göstermesidir. Bu olumsuzluklara çözüm olarak yapay hattın eleman sayısını arttırmanın kırmık üzeri alan maliyeti bulunmaktadır. Buna karşılık, ilgili hattın kayıplı olarak gerçekleştirilmesinin, kazanç eğrisinin frekansla düzgün değişimine katkı sağladığı gösterilmiştir. Sonuçta , tek transistörlü olarak ve yapay giriş hattının kayıplı olarak gerçekleştirildiği bu yapı, tezde kullanılan çekirdek hücreyi oluşturmuştur.

Bu çekirdek hücrede çıkış hattı tasarlanırken, klasik yapıda kullanılan sonlandırma empedansı kaldırılmıştır. Böylece geriye doğru ilerleyen gücün kaybı önlenmiştir. Çıkış yansıma katsayısını kabul edilebilir bir seviyede tutmak ve gücün 50Ω'luk yüke geniş bantlarda uygun aktarımını sağlamak için transistör yük doğrusunu temel alan bir yaklaşım kullanılmıştır. Yine çıkışta kullanılan hat eleman değerleri de bu şekilde belirlenmiştir. Çıkış hattı tasarımının da eklenmesiyle elde edilen yapıya, tek transistörlü yürüyen dalga güç kuvvetlendiricisi (SSTWPA) adı verilmektedir. Tasarımın başarımını göstermek amacıyla, transistörün çalışma bandını arttıracak şekilde emetörde direnç kullanan geri beslemeli bir yapı 0.35µm SiGe HBT teknolojisinde gerçekleştirilmiştir. Devrenin güç kazancı bir dekat üzerinde (0.2-2.2 GHz) düzgün dağılım göstermiştir. Önerilen tek transistörlü devrenin temel hücre olarak kullanıldığı iki katlı bir hali de çıkıştaki kat ayrıca paralellenerek yeniden oluşturulmuştur. Bu yeni durumdaki devreye, kaskatlanmış tek transistörlü yürüyen dalga güç kuvvetlendiricisi (CSSTWPA) adı verilmiştir. Önerilen CSSTWPA devresi ile hem çıkış gücünün ve verimin, hem de kazancın arttırılabileceği gösterilmiştir.

Tez çalışmasında ikinci aşamada, çıkış hattında kullanılan yük doğrusu yaklaşımının daha karmaşık ve genişletilmiş bir uyarlaması olan yük taraması yöntemini kullanan yöntemler araştırılmıştır. Yük taraması yöntemi, transistör çıkışına bağlanan bir $Z_L(j\omega)$ yükünün, uygun seçilmiş değerler kümesi içinde taranarak çıkış gücünün ve verimin birlikte gözlenmesi ilkesine dayanır. Bu yöntem ile elde edilen yük empedansı değer kümesini, uygun bir yüke (örn. 50Ω) uyduracak empedans uydurucunun geniş bantlarda tasarımı ise zor bir problemdir. Literatürde sunulan geniş bantlı empedans uydurucu tekniklerin büyük bölümü analitik çözümlere dayalıdır. Uydurulmak istenen $Z_{opt}(j\omega)$ empedansının karmaşıklığı arttıkça analitik çözümlerin derecesi artmaktadır. Dolayısıyla da önerilen devrelerin karmaşıklığı ile beraber kullanılan eleman sayısı da artmaktadır. Bu bakımdan, yüksek başarımlı

analitik yaklaşımların yerine kullanılabilecek türden, daha basit ve devre başarımı açısından kabul edilebilir yöntemler bu kısımda araştırılmıştır.

Bu doğrultuda, çıkış hattında kullanılabilecek türden geniş bantlı ve basit bir empedans uydurucu yapı, grafik tabanlı bir yöntem doğrultusunda önerilmiştir. Bir transistörün tek bir frekansta verebileceği en büyük gücü aktardığı yük empedansının değeri tektir. Bununla birlikte, aktarılan güç azaldıkça, karşılık gelen yük empedansı değer kümesi de büyür. Bu gerçekten hareketle, önceden karar verilmiş bir güç seviyesi için uygun düşen empedansların geniş bantlardaki değer kümesi yeni önerilen yaklaşımın temelini oluşturur. Smith abağı üzerinde bu empedans çözüm kümesi içinde kalacak olan her uydurma devresi, amaca uygun çözümü verecektir. Bu tekniği kullanan gene tek transistörlü bir devre, 0.25µm GaAs PHEMT MMIC teknolojisinde, geniş bir bant aralığında (1-8 GHz) çalıştırılmıştır. Sözü geçen devrede kullanılan geniş bantlı empedan uydurucu devre uygun çözümler içinden basitlik açısından tek elemanlı olarak seçilmiştir. Bu devrenin bir adım sonrasında, aynı teknolojinin yüksek kazançlı kaskat bir uygulaması da önerilmiştir. Bu devrede, sürücü ve çıkış katının ayrı ayrı ve sistematik tasarımı yeni bir yaklaşıklıkla birlikte sunulmuştur. Buna göre, kaskat yapıdaki sürücü ve çıkış katı, ara empedans tasarımlarıyla birlikte, çıkış gücünü ve dolayısıyla verimi yüksek tutacak şekilde transistor büyük işaret davranışlarıyla beraber düşünülerek gerçekleştirilmiştir. Böylece kaskat tasarımda, klasik gerilim modlu anlayıştan ayrı olarak katlar arası geçiş için güç ve dolayısıyla verimliliği ifade eden terimler tasarım denklemlerinde kullanılmıştır. Bu yöntemi doğrulayan bir tasarım da gerçekleştirilerek üretilen tümdevre başarımı ölçülmüştür. Tüm bu çalışmalara ek olarak, MMIC teknolojilerinde kullanılmaya uygun ve transistörlerin savak kutuplamalarında geniş bantlı RFC görevini üstlenebilecek bir iletim hattı ayrıca sunularak bahsedilen tümdevre yapılarında kullanılmıştır.

Son bölümde ise, özellikle gelecekteki araştırmalara yol gösterebilecek şekilde ayrık güç elemanlarında uygulanabilir basit bir geniş bantlı empedans uydurucu yapı tanıtılmıştır. Buna göre, seçilen yüksek güçlü bir GaN HEMT çıkışındaki kılıf kökenli parazitik kapasiteyi karşılayan basit bir yapı, çıkıştaki empedans uydurma problemini görece düşük-Q değerli bir uydurma problemine indirgemiştir. Verilen yapının bir diğer faydası da, çıkış hattında transistörün kutuplamasında kullanılacak RFC ihtiyacını ortadan kaldırmasıdır. Çıkış katı tasarımına ilişkin yapılan benzetim sonuçları ile yöntemin potansiyel faydaları literatürdeki örnekleriyle birlikte başarım karşılaştırmalı olarak sunulmuştur.

Sonuç olarak bu çalışmada, geniş bantlı güç kuvvetlendirici tasarımında kullanılacak şekilde; basitleştirilmiş topolojik yaklaşımları ve eleman sayısı azaltılmış çıkış katlarını, sistemli ve kolay tasarlayan iyileştirmeler ve yöntemler önerilmiştir. Bu yöntemlerdeki başarı, karmaşık ve zorlu tasarım süreci gerektiren diğer yaklaşımların ulaştığı sonuçlarla kıyaslanır mertebededir.

1. INTRODUCTION

The wireless communications market is changing very rapidly. The recent and fast growth in technology and the successful commercial production line of wireless communications are significantly affecting our daily lives. Pushed by the customer requirements, new systems for wireless communications are emerging very fast. In order to increase flexibility on the market and functionality of radio frequency (RF) and microwave transceivers, designers are pursuing solutions for cost effective multi-standard transceivers. The tendency from analog to digital communications, the increase of third and fourth generation radio systems, and the replacement of wired type connections with the wireless (e.g. Wi-Fi and Bluetooth) are enabling consumers to access a wide range of information from anywhere and at any time. As the consumer demand for higher capacity, faster service, and more secure wireless connections increases, new enhanced technologies have to be offered in the overcrowded RF spectrum in which every radio technology allocates a specific part of the spectrum. For instance, the signals for TVs, radios, cell phones, etc. are carried on different frequencies to avoid interference with each other. As a result, the constraints on the availability of the RF spectrum become more and more strict with the introduction of new radio services. From these perspectives, wideband technology proposes a promising solution to the RF spectrum by allowing new services to coincide with current radio systems with minimal or no interference.

Wideband[1] operations were traditionally accepted as pulse radio, but the Federal Communications Commission (FCC) and the International Telecommunication Union Radio communication Sector (ITU-R) have drafted a new ultra-wideband (UWB) definition. According to this definition, UWB has the properties of having a

[1] The term Ultra-wideband is also used frequently instead of wideband terminology. A term "Broadband" is also used instead of wideband. We prefer to use broadband term when the lower limit of the bandwidth drops to DC (i.e. zero frequency).

fractional bandwidth is greater than 25% or occupies 1.5 GHz or more of spectrum[2]. In this definition, the center frequency of the transmission was defined as the average of the upper and lower –10dB points (FCC 02-48, 2002). FCC's –10 dB choice of bandwidth, rather than the –20 dB bandwidth used by Office of the Secretary of Defense (OSD) and Defense Advanced Research Projects Agency (DARPA) was because of the UWB devices operate so close to the noise floor that in many cases it may not be possible to measure the –20 dB bandwidth.

Many applications in the area of solid-state RF microwave electronics need well organized and defined system blocks performing wideband operation for the given specific purpose. Operational functionality of such wideband operated blocks mostly depends on the design of wideband active and passive networks. Active RF front-end sub-blocks including: low noise amplifiers (LNAs), mixers, voltage-controlled oscillators (VCOs), power amplifiers (PAs) and etc. have already been studied and inspected for many decades. Circuit realizations of these RF blocks realized in both integrated and discrete technologies including silicon (e.g. SiGe, LDMOS, SiC) and III–V compounds semiconductors (e.g. GaAs, GaN) by means of their wide band gap and high-speed properties. Nowadays, researchers and designers are still trying to improve performance metrics of such front-ends to obtain better responses in the desired wideband frequency of operation.

Power amplifiers are often the most critical stage of any wideband RF/microwave communications systems and consequently the focus of intense research is to achieve increased linearity and power efficiency. Beyond that, many forms of wideband power amplification are being developed to meet the needs of the commercial wireless communication equipment, military industry and the world's demand for greater information transmission.

1.1 Scientific Background of Wideband Power Amplifiers: A Historical Perspective

Power amplifiers are vital enabling sub-blocks for wireless communication systems. The present and next generation of developments in this technology is expected to

[2] 1.5 GHz maximum bandwidth limit would only apply when the center frequency is greater than 6 GHz.

place heavy demand on the PA efficiency and linearity due to the use of more complex waveforms. In the history of RF, Guglielmo Marconi transmitted the radio waves over a very long distance for the first time. He had sent Morse code sequences across the Atlantic Ocean in 1901 using radio transmitters. In fact, it was also the first version of wideband communication since the Morse codes have pulse like signal properties. However, the benefit of the wide bandwidth and the capability of implementing multiuser systems provided by electromagnetic pulses were never considered at that time.

Wideband communication fundamentally differs from other communication techniques because it employs very short RF pulses. As shown in Figure 1.1, utilizing such short duration pulses directly generates a wide bandwidth in the frequency spectrum and offers several advantages, such as large throughput, covertness, robustness to jamming and coexistence with current radio services (Nekoogar, 2006).

In the early days of wireless communication (i.e. from 1895 to the mid 1920s), RF power was generated by spark, arc, and alternator techniques. In this way, by charging a capacitor to a high voltage, usually from the batteries and a discharge (i.e. spark) through the gap could cause resonance between the capacitor and tuning inductor tied to the antenna. As a result, a radiation of a damped sinusoid occurs over antenna. Spark-gap transmitters were relatively inexpensive and capable of generating 500W to 5kW up to many MHz range (Raab et al, 2003). A representative circuit schematic for Marconi's transmitter is shown in Figure 1.2.

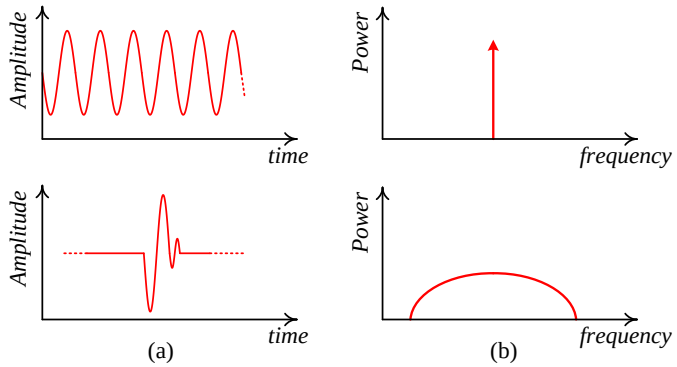


Figure 1.1 : Narrowband (top) and wideband (bottom) signal in (a) time domain (b) corresponding frequency domain.

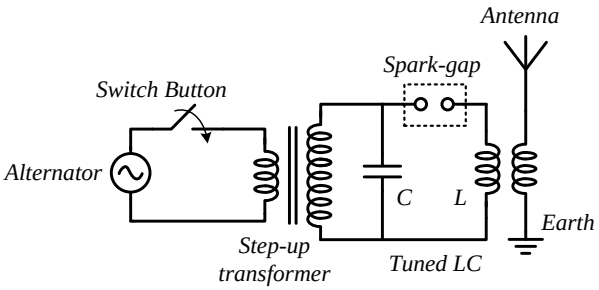


Figure 1.2 : A representative circuit of Marconi's Transmitter (Torzyn, 1984).

In the first period of radio communication, designers recognized that operating at higher frequency could enhance system performance dramatically: the amount of transmitted information scales with the operational bandwidth while the antenna gain is proportional to the square of the operating frequency (Granatstein et al, 1999). With the advent of vacuum tubes, which are electronically generating and controlling RF signals, they allowed the transmission of continuous wave signals and the operation bandwidths switched to higher frequencies.

In the 1930's, the amplifier performance degraded sharply with the decreasing wavelengths which became comparable in size to the tube elements. This occurred when the electron transit time between the electrodes become longer than the period of the sinusoidal input signal. Additionally, the inductive reactance of the connecting wires and the capacitive admittance between electrodes increase with frequency and tend to "short circuit" the amplifier. It was attempted to overcome these problems by minimizing both the area of the electrodes and the length of the connecting wires. Also, special tube structures and concepts were developed to increase power-frequency product of such devices.

Approximately fifty years after Marconi, modern pulse-based transmission gained momentum in military applications especially in the design of impulse radars (Richards et al, 2010).

Discrete solid state RF power devices began to appear at the end of the 1960s with the introduction of silicon bipolar transistors. GaAs MESFETs were introduced in the late 1970s. In the early 1980s, there has been a strong push to replace vacuum tube based devices with their solid-state counterparts. This brought out many advantages, including: reliability and maintainability, modularity and potential for future performance (Raab et al, 2003). Tube based PAs require high voltage power supply, typically require warm-up time and have significant aging related issue.

However, there are many applications, where solid-state devices cannot yet compete with vacuum tube devices in terms of output power, efficiency, and cost. It is predicted that solid-state devices will not be able to replace tubes in many radar and electronic warfare applications that require hundreds of kilowatts of average power.

The increasing number of solid-state technologies attracted the attention of researchers on the design of wideband PAs since there are a huge number of applications that need to employ wideband system blocks.

Nowadays, wideband radar applications are gaining more attention in which fine spatial resolution, extraction of target feature characteristics and low probability of interception and noninterfering signal waveform are some of the advanced features of using wideband signal processing. Thus, wideband radar offers possible solutions to defense requirements such as passive target identification, target imaging and discrimination and signal covering from electronic warfare equipment and anti-radiation missiles. Frequency spectrum sharing with other radar and communications systems is another potential use of wideband systems. Future wideband radar applications will depend on the ability of a particular wideband system to perform a given detection or remote sensing function competitively with alternative systems or to provide some operational advantage, such as a low probability of intercept signal (Taylor, 2001).

There is a huge number of solid-state power amplifier applications that need to cover a wide frequency band of operation from dc to several tens of GHz region where most of the fractional bandwidths are in the range of 25% to 200%. Figure 1.3 shows a simple chart as an overview of applications for PAs with different device technologies over IEEE frequency bands.

Since this chart depicts up to date applications of PAs, some of the well-known wideband PA applications could be summarized as,

- Microwave electronic warfare (EW) applications (Bahl, 2007; Lin et al, 2009; Colantonio et al, 2009; Xie and Pavio, 2007)
- High resolution short range radar and systems (Sewiolo et al, 2009)
- Phase array radars (Krishnamurthy et al, 2000b; Zhongzi et al, 2009)
- Software defined radios (SDRs) (Narendra et al, 2009)

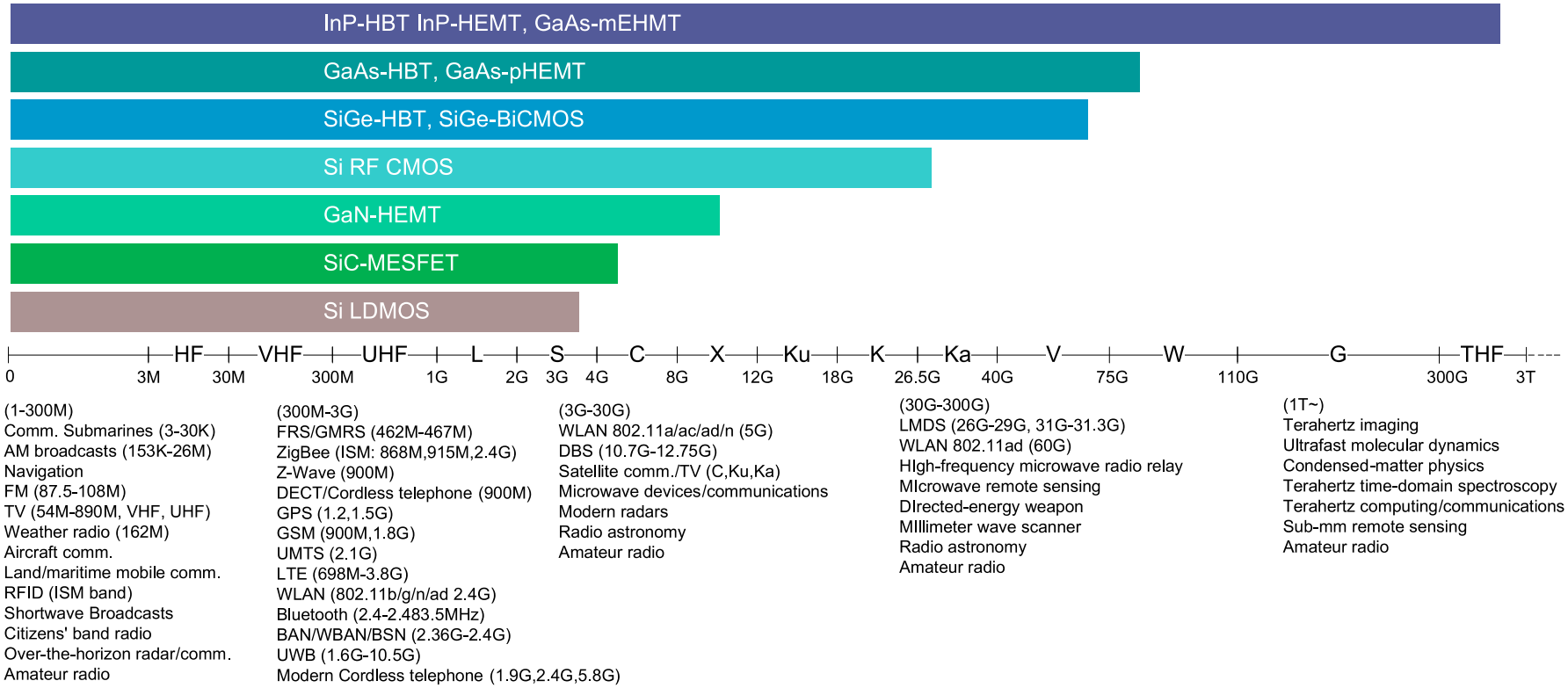


Figure 1.3 : Applications of PAs with the different device technologies over IEEE frequency bands (Joung, 2013).

- Digital optical communication systems (Banyamin and Berwick, 2000b; Xu et al, 2011)
- Instrumentation and measurement equipment (Liang and Aitchison, 1995b)

As an example, a summary of FCC restrictions on UWB operation in the 3.1 to 10.6GHz band are given in Table 1.1 (FCC 02-48, 2002).

Table 1.1 : Summary of FCC restrictions on UWB operation.

Application	**Frequency Band for Operation at Part 15 Limits**	**User Restrictions**
Communications and Measurement Systems (sensors)	3.1-10.6GHz (different emission limits for indoor and outdoor systems)	None
Vehicular Radar for collision avoidance, airbag activation, and suspension system control	3.1-10.6GHz (different emission limits for indoor and outdoor systems)	None
Ground Penetrating Radar to see or detect buried objects	3.1-10.6GHz and below 960 MHz	Law enforcement, fire and rescue, research institutions, mining, construction
Wall Imaging Systems to detect objects contained in walls	3.1-10.6GHz and below 960 MHz	Law enforcement, fire and rescue, mining, construction
Through-wall Imaging Systems to detect location or movement of objects located on the other side of a wall	1.99-10.6GHz and below 960 MHz	Law enforcement, fire and rescue
Medical Systems for imaging inside people and animals	3.1-10.6GHz	Medical personnel
Surveillance Systems for intrusion detection	1.99-10.6GHz	Law enforcement, fire and rescue, public utilities, and industry

From the design point of view, the most popular wideband PA topologies implemented in both integrated and discrete technologies are classified into four groups, which are: reactively matched, lossy matched, feedback, and travelling wave (also known as distributed) PAs. Although Section 3 will give a detailed explanation of the basic topologies, a brief summary of the basic topologies will be provided below. Among all solid-state topologies, travelling wave concept is the most mature one to implement wideband PA. The principal of distributed amplification was originally applied to vacuum tube structures (Ginzton et al, 1948). The basic

principle underpinning the travelling wave power amplifier is the use of inherent parasitic capacitances at the input and output terminals of the transistor together with the external inductive elements to form artificial transmission-lines.

The cut-off frequency of this class of amplifiers is determined by the cut-off frequency of the artificial-lines. The resulting structure readily provides broadband performance, usually above one decade.

Reactively matched wideband PAs are implemented using lossless reactive elements in the matching network for both at the input and output of the active device. Resonance characteristics of the reactive elements are the most challenging part of the wideband-matching network design.

Lossy matched PAs use resistor at the input as the loss elements to improve the amplifier's gain flatness and matching performance. Bandwidth of this type of amplifiers is wider than the reactively matched case; however, it is at the expense of low gain, low power and low power-added efficiency.

Feedback PAs employ negative feedback from output to input. This would help to implement flat gain response and improved matching characteristics. Although this class of amplifier's circuitry is less complex and its stability is assured in most cases, power performance and hence the efficiency are degraded due to the resistive element used in the feedback path.

1.2 Present and Future Requirements

The most difficult part of the wideband PA design is to provide input and output matching at different frequencies adaptively in order to satisfy different sets of specifications, high gain and good linearity, which are mutually dependent. Until now, many approaches to synthesize wideband-matching networks have been offered. In 1950, Fano showed the theoretical limitations on the broadband matching of arbitrary impedances. For this aim, his set of integral equations is used to determine these constraints, while Youla formulated the constraints in terms of Laurent series expansions (Youla, 1964). Additionally, Carlin proposed an iterative procedure for this purpose (Carlin, 1977). Networks for matching a complex load to a complex source are often required. A theoretical approach to solve this class of problems was presented by Chen and Satyanarayana (1982), and more recently,

Carlin and Yarman (1983) introduced an alternative and simplified theory. They had also developed iterative techniques for matching a complex load to a complex source (Yarman and Carlin, 1982).

Despite all the proposed analytical approaches, wideband impedance matching is still a challenging problem since the active device parasitic elements are nonlinear by nature and they complicate the impedance data over a wide band. As a result, matching of such nonlinear behavior increases the degree of the analytical solutions, which realize high-order networks. However, implementing and realizing such circuitry are very challenging tasks. The proposed analytical solutions to wideband-matching problem are not always applicable to every device sizing and biasing condition. That is to say, optimum impedance complexity changes from one biasing to another and from one transistor size to another. This is again due to the nonlinear nature of the device, which is strongly depended on the biasing condition and device geometry.

When defining the needs of a multi-standard single chip solution, one of the major problems encountered is the cost of implementation. This is not surprising as the RF chip integrates the mixed-signal and radio frequency front-end blocks on a single substrate. Silicon based solution has established a strong foothold in the communications marketplace by offering a cost competitive solution for large-scale integration capability and the relatively low cost processes. SiGe HBT technologies currently address various applications ranging up to hundreds of GHz. At the heart of this success is the ease of integration of a high performance SiGe HBT with state-of-the-art CMOS and passive elements. However, one of the drawbacks of this technology is the silicon substrate loss, which makes the design of wideband PAs more complicated and inefficient compared to other relatively low-loss substrates such as III–V based GaAs, InP and GaN processes (Raghavan et al, 2008). The tradeoff between cost and performance of BiCMOS processes like SiGe HBTs incites researchers to focus on the design circuitry that improves the efficiency of high power and wide bandwidth PAs (Analui and Hajimiri, 2004).

Employing high-order and complex matching networks increases the total lost power dissipated in the substrate and discrete element parasitics, in most cases. Additionally, the matching network area on the chip/substrate gets to be larger, which in translates to a higher cost.

Apart from the matching problem, PA efficiency is a big concern when operating in the wideband. For any pulse shaped signal, the corresponding active device (e.g. transistor) must be ready to deliver the stored energy in a short time and then be ready for the other interval. From the device basics, it is not possible to implement such an operation by switching on and off the device for a short time periods. Thus, wideband operated devices must be ready for all the time to conduct (or supply) sufficient current to charge (or discharge) the output load. Due to this fact, the corresponding classes of operation suitable for wideband operation are class-A/AB in most cases. However, this makes the efficiency issues a challenging and hard task especially when the mobility is concerned. Moreover, device nonlinearities are the least when the operation class is A/AB. This is also significant when designing wideband-matching circuitry where the input and output of the device parasitics are involved in the matching networks and significantly depend on the class of operation.

There is a trend for wideband power amplifiers for pulse shaped signaling applications in electronic warfare (EW) such as phase array radars and future radar systems with multi-band functionality, e.g. combining the C and X-band (Kinghorn, 2008). Other applications for high power wideband amplifiers, which include: secure communication systems with spread spectrum techniques, software defined radios and next generation mobile systems are inside the scope of the efficient wideband PA design, where the mobility and thus the higher efficiency is a must for most future applications.

1.3 Motivation and Goals of This Work

The proposed thesis study is motivated by the previously explained requirements. Relaxation of both the output-matching network and PA design complexity are desired to be examined. In addition to this, improving the PA efficiency in the wideband is another motivation for the study.

Consequently, simple and efficient techniques to implement wideband-matching networks are vital for designers. By this way, the circuit complexity could be reduced which is important especially when designing with ICs, where the cost is directly related to the chip area occupied.

From the designer point of view, simple and straightforward design methodologies are preferable since the design time is also another important factor. Compact and repeatable design procedures are needed to obtain wideband PAs in different device technologies.

Since high-order networks are complicated to realize and if the required bandwidth is very wide (i.e. above one decade), these matching networks require much more elements to implement and thus, controlling the parasitic of the elements are too complicated when designing with discrete components.

Finally, we could list the goals of the study as:

- Simple and relaxed output network designs without disturbing the overall PA performance significantly in the wideband.
- Simplified and less complicated wideband PA topologies.
- Improved efficiency in the wideband.

Behind these basic goals, of course, there are additional and detailed objectives, which are provided in the corresponding chapter sections.

1.4 Thesis Organization

After the introduction, some of the basics and metrics of the PA will be introduced in Section 2. This section will also include the fundamental limitations on wideband PA design.

In the first phase of Section 3, a brief comparison on various solid-state device technologies including both silicon and III–V compound devices will be presented, which are frequently used in the design of wideband PA. In the second phase of Section 3, a review of the conventional design topologies for the discrete, hybrid and monolithic design of wideband PAs will be given with the examples of previously proposed PAs.

Section 4 will cover the basic designs of the thesis. In the load-line based design section, an SSTWPA circuit will be introduced in 0.35μm SiGe HBT technology. Afterwards, an extended version of the SSTWPA, namely CSSTWPA will be presented to show that output power could be doubled without sacrificing the bandwidth. Additionally, load-pull based designs for single transistor and cascaded

TWPAs will be proposed in 0.25μm GaAs PHEMT MMIC technology. Finally, a systematic design procedure to design cascaded TWPA will be proposed in details. All simulation and measurement results will be given together to verify the performance of the proposed structures.

Further improvements on the design of efficient wideband PAs will be presented in Section 5. This chapter will introduce the design of a discrete wideband GaN PA based on a systematic susceptance minimizing technique. Simulation results will show the effectiveness of the design over analytical solutions.

Section 6 will conclude the thesis study with related possible future works.

2. SPECIFICATIONS OF POWER AMPLIFIERS

2.1 Basic Characteristics

In this chapter, some of the basics and metrics of the PA will be introduced briefly. Although there are many characterizing parameters for many different types of PA operations (e.g. linear, nonlinear), we will focus on some of the definitions frequently used in the designing and characterizing wideband PAs. Figure 2.1 is a block representation of any PA and given to indicate common notations used in the definitions.

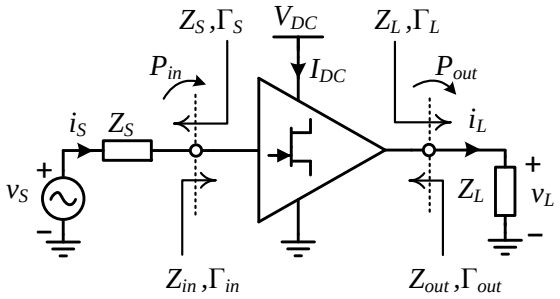


Figure 2.1 : Basic PA representation.

2.1.1 Output power

Simply, the output power, P_{out}, is the power delivered to the given load impedance, Z_L. For the PA representation in Figure 2.1, the maximum available power could be obtained from the source, if the input impedance of the device Z_{in}, equals the complex conjugate of the source impedance (Cripps, 2006).

$$Z_{in} = Z_S^* \tag{2.1}$$

Similarly, after the amplification process, maximum power could be delivered to load impedance Z_L, if the output impedance of the PA is equal to the complex conjugate of the load impedance Z_L.

$$Z_{out} = Z_L^* \tag{2.2}$$

In the most practical cases, active PA input/output impedances are not matched to source/load impedance level and it is a common need to use impedance matching networks between the unmatched impedance levels. In the phasor domain, the exact value of the power delivered to the load Z_L, can be written as

$$P_{out} = \frac{1}{2}\mathrm{Re}\{V_L I_L^*\} \tag{2.3}$$

In the ideal case, according to equation (2.3), any PA can deliver any power to the load since it can supply any current to the given load impedance with the related voltage across its output terminals. However, in the real case, due to the both the nonlinear *i-v* characteristics of the device and the voltage/current limitations of the device operation, the output power is limited to a value where the linear approximations and direct sinusoid approaches do not make sense anymore. At this point, some of the metrics to evaluate power delivered to the load need to be determined.

The output power of an amplifier typically exhibits a linear correspondence to the P_{in} as it increases from a low level. As illustrated in Figure 2.2, if P_{in} successively rises, at a certain point of P_{in}, the output power no longer corresponds linearly to the input power.

The input referred 1dB compression point specifies the output power of PA at which the output signal lags behind the nominal output signal by 1dB. The common notation for this power level is $P_{o,1dB}$.

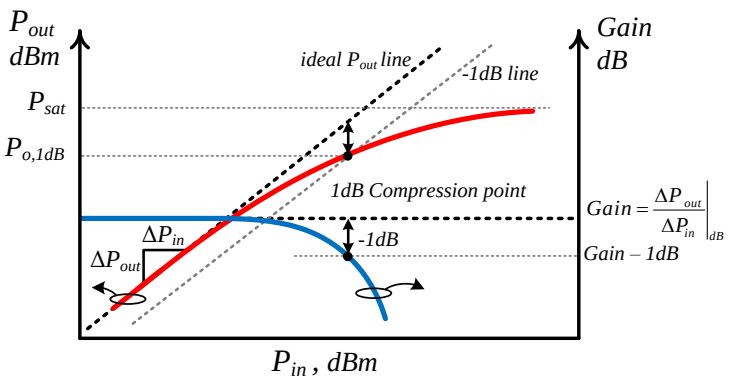


Figure 2.2 : Definition of $P_{o,1dB}$ and P_{sat}.

For further increases in P_{in}, there is an increasing P_{out} deviation, and after some P_{in} value, P_{out} starts to compress and this maximum power is called saturated output power, P_{sat}. A more detailed investigation about the gain compression will be introduced later in the nonlinearity section.

2.1.2 Power gain

Power gain or namely "operating power gain", G_P, is the ratio of the output power, P_{out} to the input power, P_{in}. In this definition, Z_{in} and Z_{out} of the PA are assumed not to match the Z_S and Z_L impedances, respectively. Available gain, G_{av}, is another definition where both Z_{in} and Z_{out} conjugately match the Z_S and Z_L impedances, respectively. In this case, we can call P_{in} and P_{out} as the maximum available input and output powers, $P_{in,av}$ and $P_{out,av}$ respectively. Moreover, if the conjugate matching condition exists only between Z_S and Z_{in} of PA and additionally, if no matching is assumed between Z_{out} and Z_L, then the gain is called as "transducer power gain", G_T. In terms of the terminal impedances, Γ reflections and small-signal s-parameters, gain definitions could be summarized as below:

$$G_P = \frac{P_{out}}{P_{in}} = \frac{1}{1-|\Gamma_{in}|^2}|S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \quad \textbf{(2.4)}$$

$$G_{av} = \frac{P_{out,av}}{P_{in,av}} = \frac{1-|\Gamma_S|^2}{1-|\Gamma_{in}|^2}|S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \quad \textbf{(2.5)}$$

$$G_T = \frac{P_{out}}{P_{in,av}} = \frac{1-|\Gamma_S|^2}{|1-\Gamma_S\Gamma_{in}|^2}|S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \quad \textbf{(2.6)}$$

2.1.3 Efficiency

In most cases, there are two efficiency definitions, which are used often in power amplifier characterization. Drain (or collector) Efficiency, DE, is determined as,

$$DE = \eta = \frac{P_{out}}{P_{DC}} = \frac{P_{out}}{V_{DC}I_{DC}} \quad \textbf{(2.7)}$$

where P_{out} is the total-overall output power and P_{DC} is the total-average dc power supplied from the dc biasing sources. Drain efficiency is independent of the power gain of the amplifier.

Another efficiency definition, power added efficiency (PAE), takes also P_{in} into account to show the influence of power gain on the overall efficiency. If the gain, G is low, PAE would be low even if the drain efficiency is high. PAE can be defined as,

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \eta\left(1 - \frac{1}{G}\right) \qquad \textbf{(2.8)}$$

The PAE definition is useful for constant amplitude signals. However, depending on the application, there are many other definitions to represent the efficiency of a given PA. For applications with complex modulation schemes (i.e. the information is carried both with amplitude and with phase of the signal), the efficiency is highest at the peak output power (at peak amplitude) and decreases as output/input power (amplitude) decreases as illustrated in Figure 2.3. In these applications, when amplifying a digitally modulated signal, most of the PAs operate far below the peak output power with high peak to average ratio. For this reason, the average efficiency definition makes sense in these kinds of applications (Shrestha, 2010).

Efficient conversion from dc to high frequency signal leads to low power dissipation in the devices and low heating of the amplifier. In this case, the cooling systems of the PA can be simplified which means smaller size and cost-efficient design.

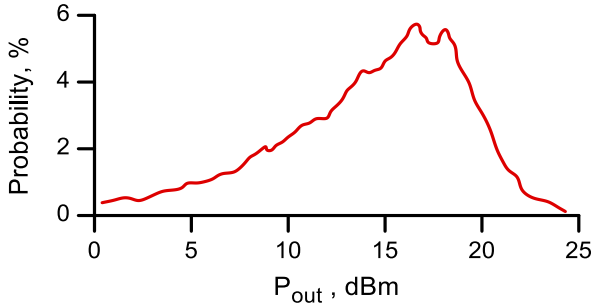


Figure 2.3 : Typical output power probability distribution for IEEE 802.11g signals (Wang et al., 2004).

2.1.4 Bandwidth

The bandwidth represents the amount or width of the frequencies that the corresponding system is able to amplify or reject the signal power. For band-pass systems, bandwidth is defined as the difference of the highest, f_{high} and lowest, f_{low} frequencies at which the magnitude of the power/voltage transfer function (i.e. Gain) drops by $1/\sqrt{2}$ or 3 dB.

$$BW = f_{high} - f_{low} \tag{2.9}$$

This bandwidth is often called the –3dB bandwidth. Although the most frequently used and known definition of the bandwidth is based on –3dB reference, any chosen dB drop with respect to reference value is possible to determine system bandwidth for the given application, which is shown in Figure 2.4.

A fractional definition of bandwidth, namely fractional bandwidth, FBW is also used to determine bandwidth of a given system.

$$FBW = \frac{f_{high} - f_{low}}{f_0} \tag{2.10}$$

where f_0 is the center frequency of the given bandwidth and equal to

$$f_0 = \frac{f_{high} + f_{low}}{2} \tag{2.11}$$

According to (2.10), FBW can have value between 0 and 2. It is very common to represent FBW in percentage where the boundary values become 0% to 200%.

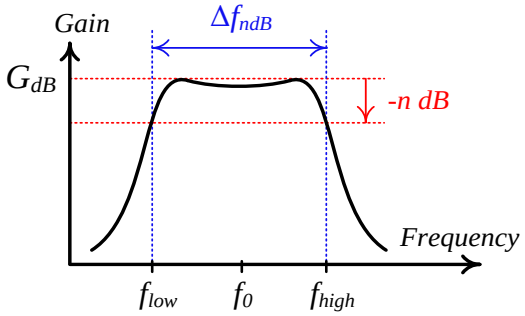


Figure 2.4 : Definition of –n dB bandwidth for typical amplifier.

From the bandwidth point of view, PAs could be classified into two categories namely, wideband and narrowband depending on the bandwidth over which they can provide constant output power. As it was mentioned before in the introduction, >25% of bandwidth is accepted to be wideband according to FCC regularities.

2.1.5 Nonlinearity

Nonlinearity is a circuit behavior, particularly in power amplifiers, in which the output signal does not vary in direct proportion to the input signal. A typical power amplifier is a nonlinear block, as it has to handle large input and output signals with reasonable power efficiency. For a memoryless, time-invariant and weakly nonlinear system, output voltage, $v_{out}(t)$ can be approximated using a power series expansion as,

$$v_{out}(t) = a_1 v_{in}(t) + a_2 v_{in}^2(t) + a_3 v_{in}^3(t) + \cdots \tag{2.12}$$

where $v_{in}(t)$ is the input signal. By taking a sinusoidal input $v_{in}(t)=A\cos\omega t$, we can rearrange $v_{out}(t)$ as,

$$\begin{aligned} v_{out}(t) &= a_1 A\cos\omega t + a_2 A^2\cos^2\omega t + a_3 A^3\cos^3\omega t + \cdots \\ &= a_1 A\cos\omega t + \frac{a_2 A^2}{2}\left(1+\cos 2\omega t\right) + \frac{a_3 A^3}{4}\left(3\cos\omega t + \cos 3\omega t\right) + \cdots \\ &= \frac{a_2 A^2}{2} + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos\omega t + \frac{a_2 A^2}{2}\cos 2\omega t + \frac{a_3 A^3}{4}\cos 3\omega t + \cdots \end{aligned} \tag{2.13}$$

In the final equation (2.13), the first term is the frequency independent dc term and $\cos\omega t$ is the fundamental term where a_1 is the linear gain term. Remaining $\cos(n\omega t)$ terms are the harmonics of the system. In this final equation, some of the important nonlinear effects could be observed:

1. Even order harmonics result from a_{2n} (n=1,2,3,...) and vanish, if the system has odd symmetry. (i.e. fully differential circuits.)

2. Under small-signal assumption: Since the small-signal assumption is a linear approximation, only the first term of equation (2.12) exists and the harmonics do not exist. Small-signal gain is then equal to a_1.

3. Gain Compression under large-signal excitation: When the applied $v_{in}(t)$ is large in amplitude, nonlinearity becomes evident. Large-signal gain, G_{LS} is then equal to,

$$G_{LS} = a_1 A + \frac{3a_3 A^3}{4} \tag{2.14}$$

and large-signal gain is dependent on the signal amplitude, *A*. When $a_3<0$ and *A* increases, $v_{out}(t)$ is a compressive or saturating function of the input. With the given explanation, now we can determine the 1dB compression gain, G_{1dB}, and the signal amplitude, A_{1dB} at that compression point equal to;

$$G_{1dB} = 20\log|a_1| - 1dB = 20\log\left|a_1 + \frac{3a_3 A_{1dB}^2}{4}\right| \tag{2.15}$$

$$A_{1dB} = \sqrt{0.145\frac{a_1}{a_3}} \tag{2.16}$$

Nonlinearity in the RF power amplifier creates two main spectral products: inter-modulation distortion (IMD) and harmonics. Harmonic distortion, however, in many cases can be removed easily by filtering. The consequence of a filter is that the resulting system becomes narrowband. IMD results from mixing of two or more signals of different frequencies due to the higher order odd terms, which appear in the expansion of (2.12). In most cases, the cubic term is the dominant one and causes the IMD products. The spurious output occurs at the sum and/or difference of integer multiples of the input frequencies. By assuming an input signal of $v_{in}(t)=A_1\cos\omega_1 t+A_2\cos\omega_2 t$, we can rearrange $v_{out}(t)$ in (2.12) as,

$$\begin{aligned} v_{out}(t) &= a_1\left(A_1\cos\omega_1 t + A_2\cos\omega_2 t\right) + a_2\left(A_1\cos\omega_1 t + A_2\cos\omega_2 t\right)^2 \\ &\quad + a_3\left(A_1\cos\omega_1 t + A_2\cos\omega_2 t\right)^3 + \cdots \end{aligned} \tag{2.17}$$

and using the trigonometric identity,

$$\cos\alpha\cos\beta = \frac{1}{2}\left(\cos(\alpha+\beta)+\cos(\alpha-\beta)\right) \tag{2.18}$$

It is concluded that the second-order expansion can be written as,

$$\begin{aligned} a_2\left(A_1\cos\omega_1 t + A_2\cos\omega_2 t\right)^2 = {} & \frac{a_2(A_1^2+A_2^2)}{2} + \\ & \frac{a_2A_2^2}{2}\cos 2\omega_1 t + \\ & \frac{a_2A_2^2}{2}\cos 2\omega_2 t + \\ & \frac{a_2A_1A_2}{2}\left[\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t\right] \end{aligned} \qquad \textbf{(2.19)}$$

and the third-order one is,

$$\begin{aligned} a_3\left(A_1\cos\omega_1 t + A_2\cos\omega_2 t\right)^3 = {} & \left(\frac{3a_3A_1^3}{4} + \frac{3A_1A_2^2}{2}\right)\cos\omega_1 t + \\ & \left(\frac{3a_3A_2^3}{4} + \frac{3A_1^2A_2}{2}\right)\cos\omega_2 t + \\ & \frac{a_3A_1^3}{4}\cos 3\omega_1 t + \\ & \frac{a_3A_2^3}{2}\cos 3\omega_2 t + \\ & \frac{3a_3A_1^2A_2}{4}\left[\cos(2\omega_2+\omega_1)t + \cos(2\omega_2-\omega_1)t\right] \end{aligned} \qquad \textbf{(2.20)}$$

Similar to the second-order term, the third-order term also produces spurious terms in the output, which do not exist in the input. The difference mixing terms appearing in the output signal are spectrally close to the original signals, making them difficult to remove by using filters. They possibly fall within the pass band of the system and cause interference.

The intersection of the second and third-order lines with the line produced by the linear (i.e. first-order) term are known as the intercept points (IP). The second-order intercept point is called IP2 and the third-order intercept point is called IP3. The intercept points are further defined with respect to the input amplitude or the output amplitude where the intersections occur. For example, the input IP3 is represented as IIP3, whereas the output IP3 is represented as OIP3.

2.2 Transistor Figures of Merit

BJT and FET representations and simplified small-signal equivalent circuits are given together in Figure 2.5. The short-current gain, which is equal to the ratio of output and input current, can be examined using the small-signal implementation of FET as in Figure 2.6, where the effect of C_{gd} capacitance is small and neglected in the most simplified cases. As the output is short-circuited whereas the input is driven by ac current source, the short-current gain equal to the hybrid parameter of h_{21} can be found as,

$$h_{21} = \frac{i_{out}}{i_{in}} \cong \frac{g_m}{j2\pi f C_{gs}} = \frac{f_{T,FET}}{jf} \tag{2.21}$$

where the transient frequency, $f_{T,FET,}$ appears to be the unity current gain cut-off frequency and equal to,

$$f_{T,FET} \cong \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2.22}$$

A similar analysis also yields that with using BJT equivalent, the transient frequency for BJT could be equal to,

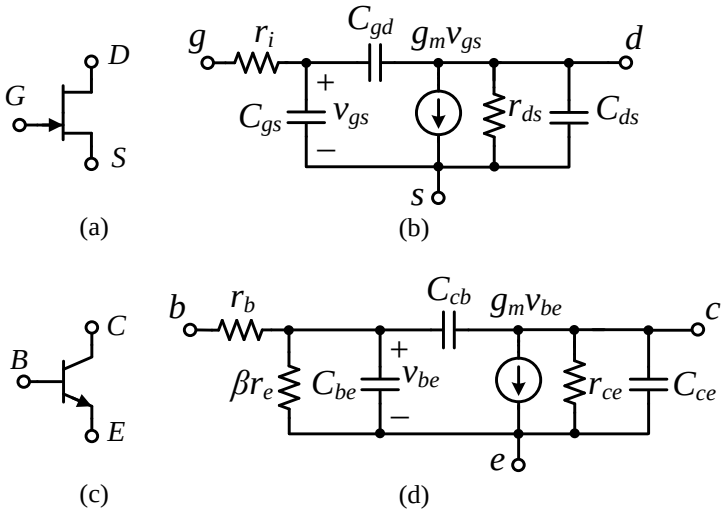


Figure 2.5 : (a) FET symbol and (b) simplified small-signal ac equivalent model. (c) BJT symbol and (d) Simplified small-signal ac equivalent model.

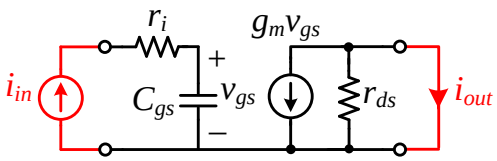


Figure 2.6 : Small-signal configuration to examine FET short-current gain.

$$f_{T,BJT} \cong \frac{g_m}{2\pi(C_{be}+C_{cb})} \tag{2.23}$$

From the transient frequency definitions, a transistor is said to operate up to f_T frequency, if current amplification is needed. However, when talking about the PA, a power gain is more suitable to figure out the transistor performance over the current gain definition. That is, a definition for the frequency, which indicates the unity power gain cut-off frequency, f_{max}, is essential to be determined[3]. For this purpose, power transfer networks (i.e. lossless matching networks) are needed to guarantee that maximum power is delivered both to the input of the active transistor and to the load, at the output of the given transistor.

In the case where both input and output are exactly matched, the maximum available power gain, MAG, and resulting f_{max} of the FET could be defined as below by using the circuit representation in Figure 2.7.

$$MAG = \frac{P_{L,av}}{P_{S,av}} = \frac{\mathrm{Re}\{V_L I_L^*\}}{\mathrm{Re}\{V_S I_S^*\}} \cong \frac{g_m^2 r_{ds}}{16\pi^2 f^2 C_{gs}^2 r_i} = \left(\frac{f_{max,FET}}{f}\right)^2 \tag{2.24}$$

$$f_{max,FET} \cong \frac{f_{T,FET}}{2\sqrt{r_i / r_{ds}}} \tag{2.25}$$

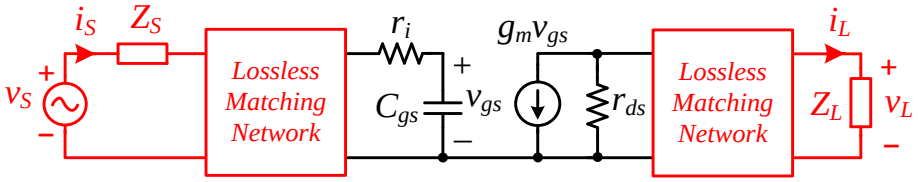


Figure 2.7 : Small-signal circuit equivalent to calculate power gain and f_{max} of the given FET transistor.

[3] f_{max} is also known as the maximum oscillation frequency.

A similar analysis is also possible for BJT devices which gives $f_{max,\mathrm{BJT}}$ as,

$$f_{max,BJT} \cong \sqrt{\frac{f_{T,BJT}}{8\pi r_b C_{cb}}} \tag{2.26}$$

2.2.1 Maximum power transfer

A very well-known theory, maximum power transfer, states that one can obtain maximum external power from a source with a finite internal resistance, if and only if the load resistance is equal to the resistance of that source. It is very simple to extend the theory to ac circuits, which include reactance terms and then maximum power transfer occurs when the load impedance is equal to the complex conjugate of the source impedance.

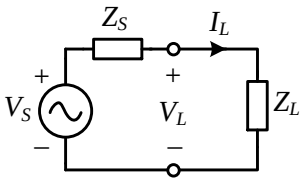


Figure 2.8 : Circuit to derive maximum power theorem.

To derive the theorem by using the simplified circuit representation of Figure 2.8, both source and load impedances could be chosen as complex ones as

$$Z_S = R_S + jX_S \tag{2.27a}$$

$$Z_L = R_L + jX_L \tag{2.27b}$$

By taking phasor magnitude voltage $|V_S|$, resulting phasor magnitude current $|I_L|$ can be written as,

$$|I_L| = \frac{|V_S|}{|Z_S + Z_L|} \tag{2.28}$$

The average power P_L dissipated in the load is the square of the current multiplied by the resistive part R_L of the load impedance as,

$$
\begin{aligned}
P_L &= I_{rms}^2 R_L \\
&= \frac{1}{2}\left|I_L\right|^2 R_L \\
&= \frac{1}{2}\frac{\left|V_S\right|^2 R_L}{(R_S + R_L)^2 + (X_S + X_L)^2}
\end{aligned}
\tag{2.29}
$$

where R_S and X_S are the real and imaginary parts of Z_S, similarly R_L and X_L is the real and imaginary part of Z_L.

Since V_S, R_S and X_S are fixed, we should determine the R_L and X_L, which makes the denominator minimum in order to determine the maximum value of P_L. It is easy to show that the denominator is minimized so that the P_L is maximized by taking,

$$X_L = -X_S \tag{2.30}$$

Then the power delivered to the load will be reduced to a value of,

$$P_L = \frac{1}{2}\frac{\left|V_S\right|^2 R_L}{(R_S + R_L)^2} \tag{2.31}$$

There we need one more relation between the R_S and R_L to maximize P_L. That is,

$$R_L = R_S \tag{2.32}$$

The conditions given in (2.30) and (2.32) constitute the load condition for a given source impedance to achieve maximum power transform. Equation (2.30) and (2.32) can be written in a complex conjugate form to determine generalized maximum power transform condition as,

$$Z_L = Z_S^* \tag{2.33}$$

Conjugate matching is sometimes referred to as the gain match in the design of RF and microwave amplifiers when the output power is not the dominant outcome. Many gain relations are derived and based on the conjugate match condition between the inner stage blocks.

2.2.2 Load-line of the transistor

Power transferring by using conjugately matched source and load impedances are not practical especially when the source is implemented by using active devices such as transistors. This situation can be illustrated with a simplified circuit in Figure 2.9 where the current generator can be thought as the output of the transistor with the output resistance as R_S loaded with load impedance R_L.

In the active devices, there exist physical limitations on both the current and voltages. These are shown in the graph of the illustrated circuit of Figure 2.10 where V_{max} is the maximum voltage (i.e. breakdown voltage) of an active device at its output port. I_{max} is the maximum output current which can be generated at the output.

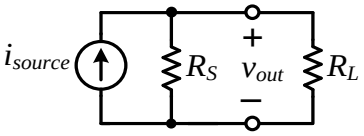


Figure 2.9 : Circuit model to represent conjugate and load-line matching.

For a given transistor, conjugate match could need a value of $R_L=R_{out}$ and this load may possibly saturate either output voltage or current of the transistor. As a result, the transistor will be limited by its available output power capability, which is simply equal to P_{max}.

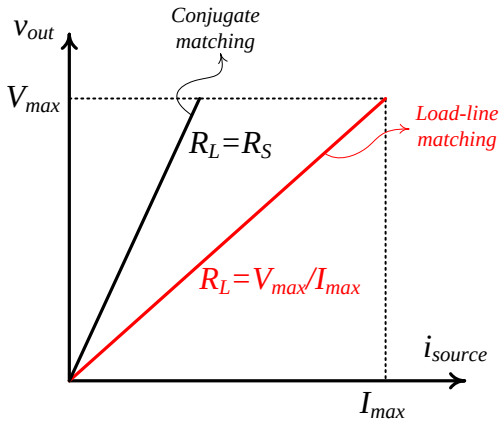


Figure 2.10 : Graphical representation for conjugate and load-line matching.

A simple numeric example can make the problem clearer. Let us say a transistor whose small signal model is shown in Figure 2.11a has I_{max}=1A and V_{max}=16V and small-signal output resistance, R_{out} of 200Ω. According to the conjugate match theorem, one should use a 200Ω load resistance to transfer maximum power according to conjugate matching. The voltage appearing across the output terminal

should be measured as 100V if 200Ω load resistance is used. However, according to given specifications, maximum output voltage across the output terminal cannot be higher than 16V. That is, the transistor will be limited by its output voltage to 16V and the corresponding output current in this condition will be less than its I_{max} value. As a result, the power output will be less than P_{max} that the transistor can supply.

It is now easy to observe that there exists a load condition where the transistor (or in general – active device) can deliver maximum power. The load condition to obtain P_{max} can be determined from the simplified output *i-v* curves for a given transistor as illustrated in Figure 2.11b and the corresponding load is then,

$$R_{opt} = \frac{V_{max}}{I_{max}} \qquad \textbf{(2.34)}$$

which is named "optimum-load" for a given transistor and the corresponding matching method is called "load-line match" or "power match".

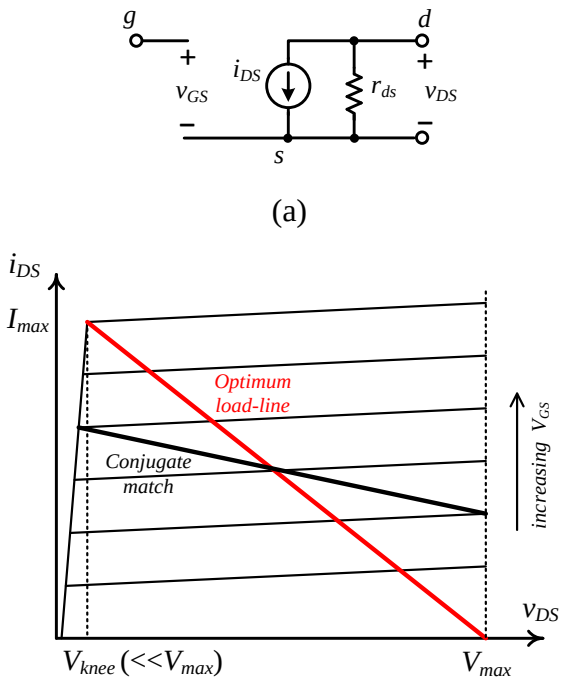


Figure 2.11 : (a) Simplified transistor model and (b) related *i-v* characteristic.

R_{out} is assumed to be such that R_{out}>>R_{opt}. If this is not valid for the transistor then R_{out} should be taken into account as,

$$R_{opt} // r_{ds} = \frac{R_{opt} r_{ds}}{R_{opt} + r_{ds}} = \frac{V_{max}}{I_{max}} \quad \textbf{(2.35)}$$

In Figure 2.12, an example of class-A amplifier compression characteristic is given to investigate both conjugately-matched and load-line match conditions at the output. As can be seen in the graph, the maximum linear power, which is referred to as 1 dB compression, has a higher value when there exists load-line match. In a typical application, the conjugate match would yield a 1 dB compression power significantly lower than that of a power match condition where the power loss is around 0.5-4 dB according to RF power transistor manufacturers (Cripps, 2006).

Because that the power transistors are often the most expensive individual part of an RF system block, this kind of wasted power will be translated directly into a unnecessary cost.

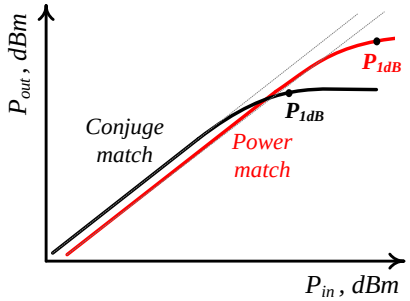


Figure 2.12 : Typical compression characteristics of a conjugately and load-line matched transistor.

2.2.3 Load-Pull analysis of the transistor

Cripps (1983) has shown that the basic and elementary load-line principles could be extended to predict load-line contours at microwave frequencies for a device, which is operating in linear region. The concept of the load-pull is to provide information for the load reflection coefficient as a function of output power.

Basic analysis shows that a device (i.e. transistor) can deliver a maximum available power to a single impedance load when in the linear operation and for a given frequency, this impedance value could be shown as a single point on the Smith chart. By decreasing the output power level, one can have some kind of load impedance points forming contours, which indicate the exact output power level.

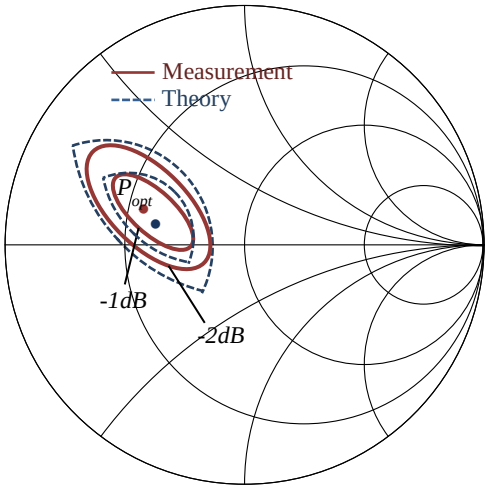
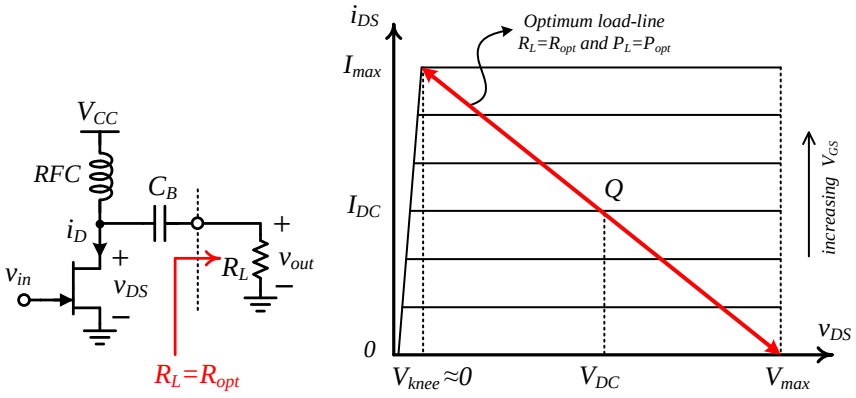


Figure 2.13 : An illustrative comparison of the experimental and theoretical load behavior for the optimum load inspection.

In Figure 2.13, an example load-pull analysis in comparison to experimental measurement, is illustrated together. As shown in the figure, simplified load-pull model is simply suitable to predict real measurements for a given device under test (DUT). Today, there are many nonlinear transistor models suitable to predict device characteristics when the device is operating under nonlinear regimes. There are also computer aided design (CAD) tools, which can quickly investigate the optimum load conditions for a given nonlinear model. It is also important to make load-pull measurements for being sure about the overall real behavior of the DUT. Starting point for the load-pull analysis includes a simple class-A common source circuit representation given in Figure 2.14a. The FET transistor here represents a highly nonlinear device with zero output conductance. *i-v* characteristics of the device given in Figure 2.14b determine the load-line of the device.



(a) (b)

Figure 2.14 : (a) Class-A operating common source PA and (b) idealized transistor behavior to inspect optimum load.

The transconductance of the transistor is assumed to be linear in I_{max}, V_{max} boundaries. This will make our linear operating assumptions valid only in the given operating range. Except for these limitations; we will assume that the device operation is fully nonlinear.

According to the characteristics in Figure 2.14b, the current swing will be equal to its maximum linear range, which is zero to I_{max}. In this case, a sinusoidal waveform will have an amplitude of $I_{max}/2$ and the voltage swing will be equal to $2V_{DC}$. Using these voltage and current descriptions, the optimum load definition given in (2.34) could be written as,

$$R_{opt} = \frac{V_{DC}}{I_{max}/2} = \frac{V_{DC}}{I_{DC}} \tag{2.36}$$

In this optimum load condition, the device can deliver an RF power, which is equal to,

$$P_{opt} = \frac{1}{2} V_{DC} I_{DC} = \frac{V_{DC}^2}{2R_{opt}} = \frac{1}{2} I_{DC}^2 R_{opt} \tag{2.37}$$

Since the dc power consumption is equal to,

$$P_{DC} = V_{DC} I_{DC} \tag{2.38}$$

it is easy to show that theoretical class-A drain efficiency is simply equal to 50%.

According to Cripps (2006), load-line theory can be extended to get load-pull contours by using a simple approach. For this aim, a power level of P_{opt}/p is to be investigated where p is a scaling constant. By using the P_{opt} equation in (2.37), one can show that there are two possible solutions of R_{opt}, that make the output power level P_{opt}/p, which are low and high values of the optimum load, $R_{opt,L}$ and $R_{opt,H}$, respectively.

$$R_{opt,L} = R_{opt} / p \tag{2.39}$$

$$R_{opt,H} = pR_{opt} \tag{2.40}$$

When the optimum load is equal to $R_{opt,L}$, the transistor can swing over the full current range of I_{max} but the corresponding voltage swing is only V_{DC}/p which corresponds to an RF output power of P_{opt}/p.

Moreover, in the case of $R_{opt,H}$, the drive level at the input has to be reduced to diminish the current swing and keep the voltage swing at the maximum linear peak value of $2V_{DC}$. It is clear that the current amplitude has to be reduced by the ratio of p to deliver a power level of P_{opt}/p. The two load situations are shown in Figure 2.15 and Figure 2.16 by means of the load-lines superimposed on the transistor output i_{DS}-v_{DS} characteristic. In addition to this, Figure 2.17 shows the Smith chart representation of the loads.

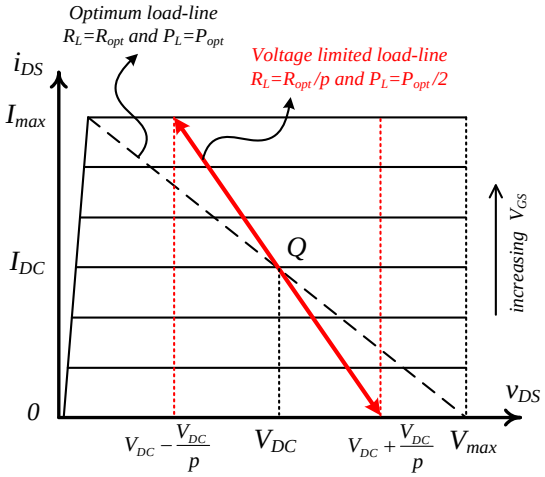


Figure 2.15 : Voltage limiting mechanism over the transistor output characteristic.

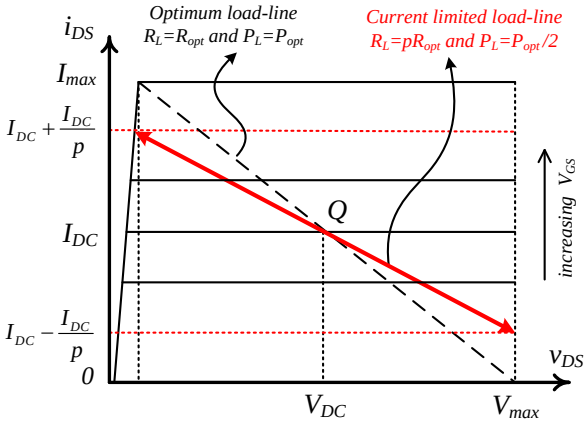


Figure 2.16 : Current limiting mechanism over the transistor output characteristic.

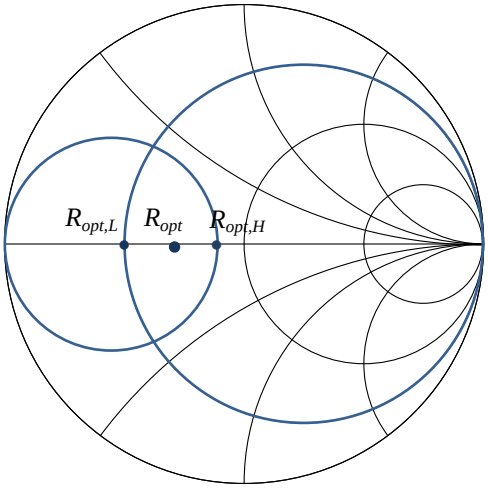


Figure 2.17 : The resistive loads to investigate P_{opt} and P_{opt}/p.

Now we can think about a load impedance Z_L consisting of R_L in series with a reactance X_s and can calculate the power delivered to the load as shown in Figure 2.18a.

By taking $R_L=R_{opt}/p$ and the calculating the corresponding $p_{L,}$ we can conclude that Z_L is equal to,

$$Z_L = \frac{R_{opt}}{p} + jX_s = |Z| \angle \theta \tag{2.41}$$

By taking the phasor quantities,

$$I_L = |I_L| \angle 0° \quad \text{and} \quad V_L = I_L |Z| \angle \theta \tag{2.42}$$

Then by taking the time domain instantaneous power $p_L(t)$,

$$p_L(t) = i_L(t) v_L(t) = \frac{|Z| I_{DC}^2}{2} \cos\theta + \frac{|Z| I_{DC}^2}{2} \cos(2t + \theta) \tag{2.43}$$

where cosθ is equal to,

$$\cos\theta = \frac{R_{opt}}{p|Z|} \tag{2.44}$$

and the average power delivered to the load will be equal to the constant term in the equation (2.43),

$$P_L = \frac{1}{2}|Z|I_{DC}^2 \cos\theta = \frac{1}{2}|Z|I_{DC}^2 \frac{\left(R_{opt}/p\right)}{|Z|} = \frac{1}{2}\left(I_{DC}^2 \frac{R_{opt}}{p}\right) = \frac{1}{2}P_{opt} \quad \textbf{(2.45)}$$

The result given in (2.45) is very interesting that although the load impedance is now Z_L by adding a series reactance X_s, the power delivered to the load is still equal to P_{opt}/p which is the same power with the pure resistive load $R_L=R_{opt}/p$. Now the question of what the limit values for the reactance X_s that do not alter the delivered power P_{opt}/p are arises.

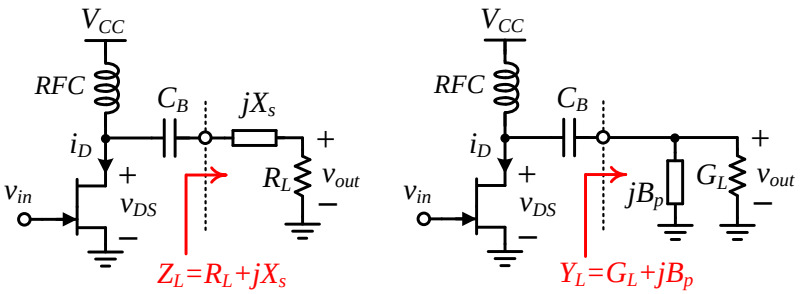
Intuitively, we cannot increase X_s value as much as we desire. Because of the active device *i-v* limitations, above some values of $|X_s|$, voltage across the drain-source terminals will be limited by V_{max}. At the limiting point, it can be written that the $v_L(t)$ voltage will reach the maximum available swing range and it is,

$$V_{DC} = |Z|I_{DC} \quad \textbf{(2.46)}$$

$$R_{opt} = \sqrt{\left(\frac{R_{opt}}{p}\right)^2 + X_s^2} \quad \textbf{(2.47)}$$

and the limits for the reactance X_s can be written as,

$$X_m = R_{opt}\sqrt{1-1/p^2} \qquad \text{where} \qquad -X_m \le X_s \le +X_m \quad \textbf{(2.48)}$$



(a) (b)

Figure 2.18 : PAs loaded with (a) $Z_L=R_L+jX_s$ and (b) $Y_L=G_L+jB_p$ loads.

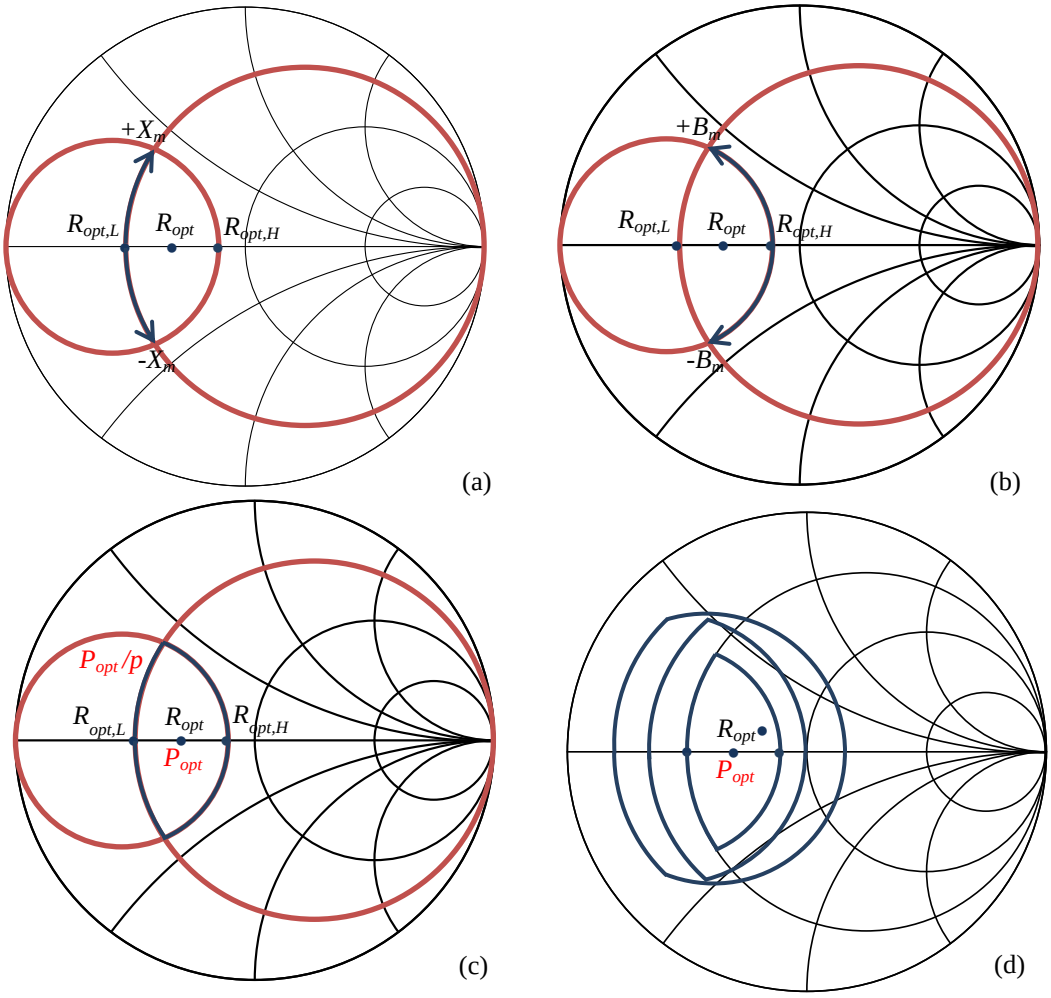


Figure 2.19 : Construction of the load-pull contours for the given load conditions. (a) Arc segment of given Z_L, (b) Arc segment of given Y_L, (c) Non-circular power contour for the output power of P_{opt}/p. (d) Power contours stepped to outer in a decreasing power manner.

According to result given in (2.48), an arc segment of a constant power on the Smith chart can be drawn for the added series reactance X_s given in Figure 2.19a.

A similar approach can be applied to a situation where the load admittance Y_L now consists of the load conductance with a shunt susceptance is added. This situation is shown in Figure 2.18b. Similar expressions can be derived for the new situation and finally limit values for the additive susceptance can be written as,

$$B_m = G_{opt}\sqrt{1-1/p^2} \qquad \text{where} \qquad -B_m \le B_p \le +B_m \tag{2.49}$$

Again, in Figure 2.19b, arc segment of a constant power on the Smith chart can be drawn and the final superimposed load-pulled power non-circular contour would be

constructed as shown in Figure 2.19c. Similar analyses are possible to show how the load-pull contours look like when the output power is stepped down as indicated in Figure 2.19d.

2.2.4 Common source amplifier

In the transistor circuit topology, when the input and output terminals share the "source" or "emitter" of the amplifying transistor, we call the configuration as the common source (CS) amplifier. Figure 2.20a shows a typical simplified circuit implementation for common source amplifier.

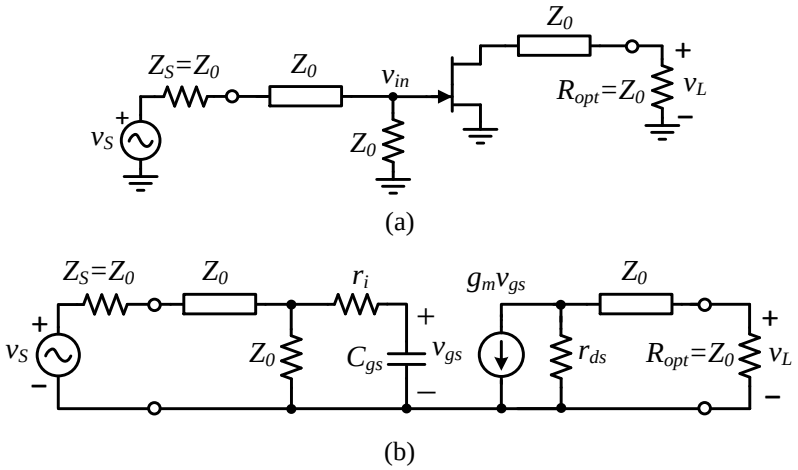


Figure 2.20 : (a)Typical CS amplifier for microwave frequencies. (b) Small-signal equivalent.

For the CS amplifier, the forward transmission coefficient ($s_{21,CS}$) of the CS amplifier can be written as,

$$s_{21,CS} = -G_m Z_0 \tag{2.50}$$

and resulting mid-frequencies transducer power gain, $G_{T,CS}$ is could be given in terms of the transistor parameters as,

$$G_{T,CS} = \left|s_{21,CS}\right|^2 = \left(\frac{V_{br} - V_{knee}}{V_p}\right)^2 \cong \left(\frac{V_{max}}{V_p}\right)^2 \tag{2.51}$$

where V_{br}, V_{knee} and V_p is the drain-source breakdown, drain-source saturation and pinch-off (threshold) voltage of the given FET device, respectively. Typical

frequency response of the CS amplifier is shown in Figure 2.21. 3dB cutoff frequency can easily be determined as

$$f_{3dB,CS} = \frac{1}{2\pi(Z_0/2 + r_i)C_{gs}} \tag{2.52}$$

Since only the input is terminated with the line characteristic impedance, Z_0, and the output of the transistor has only load-line match without Z_0 termination, gain-bandwidth product of the CS amplifier is shown to be limited to $2f_T$.

$$\left|s_{21,CS}\, f_{3dB,CS}\right| = \frac{G_m Z_0}{\pi(Z_0 + 2r_i)C_{gs}} \cong \frac{G_m}{\pi C_{gs}} = 2\, f_T \tag{2.53}$$

The problem of missing Z_0 termination at the output results in degraded output reflection (s_{22}) performance at the output port. By adding that missing Z_0 impedance, as a tradeoff, both the gain and gain-bandwidth product will be halved.

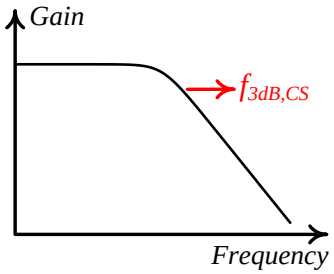


Figure 2.21 : Typical Gain vs. Frequency characteristic of a CS amplifier.

Besides these small-signal based definitions, it is also useful to determine large-signal power gain, G_{LSG} on which we have to focus more. Figure 2.22 shows a representation of a simplified large-signal model for load-line matched CS amplifier. Model notations are capitalized to represent large-signal behavior.

We assume that $r_{DS} >> G_{LSG}$ of the CS amplifier and resulting large-signal power gain cutoff frequency can be determined as below, respectively.

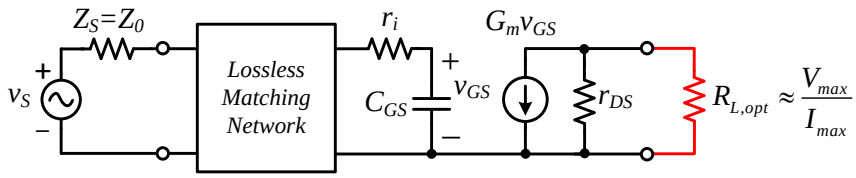


Figure 2.22 : Definition of large-signal power gain.

$$G_{LSG} = \frac{P_L}{P_{S,av}} \cong \left(\frac{V_{max}}{V_p}\right) \frac{G_m}{4\pi^2 f^2 C_{GS}^2 r_i} = \left(\frac{f_{LSG}}{f}\right)^2 \quad \textbf{(2.54)}$$

$$f_{LSG} = \sqrt{\frac{R_{L,opt}}{r_i}} \cdot f_T \quad \textbf{(2.55)}$$

2.2.5 Cascaded amplifiers

Single-stage transistor amplifiers are inadequate for meeting most design requirements for PAs (e.g. gain, PAE, linearity). Therefore, it is a common method to use more than one amplifying stage in the PA design.

Figure 2.23 represents a cascaded (or multi-stage) amplifier block to examine stage-by-stage gain and cutoff frequency performance. As given in Table 2.1, at the first stage, both input and output are matched. In second stage, only the input is matched, and at the third stage, both input and output are unmatched.

Additionally, first stage gain is equal to half of the second and third stages. This is because of the Z_0 termination, which halves the output impedance. Direct termination of the Z_0 load impedance at the second and third stages improves the gain performance.

Moreover, at the input, since the termination impedance Z_0 is used to improve s_{11}, the gain-bandwidth product is to be halved, which is equal to f_T. It is interesting that, the gain-bandwidth product improvement in the multi-stage cells can only be obtained once since both input and output are required to be terminated by Z_0 impedances to minimize reflections.

As it was mentioned before in the efficiency section that, the amplifier gain directly affects the PAE performance of the amplifier as in equation (2.8). When the gain is very high, the second term in the parentheses becomes negligible and the PAE is the same as the drain/collector efficiency. The main source of PA efficiency, the output stage, is by far the largest consumer of current and has the highest output power in the cascaded chain of amplifiers. It also generates most of the linearity problems, since it must operate as close as possible to compression point to achieve the required efficiency.

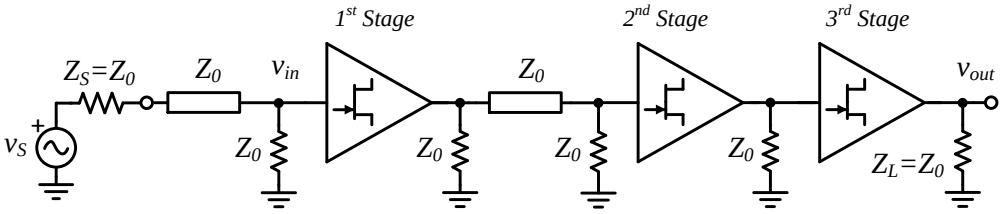


Figure 2.23 : A block representation for the cascaded-gain cells.

Therefore, in the cascaded amplifier stages, previous stages are backed off as much as possible from saturation to minimize their role in the nonlinear behavior of the amplifier. This results in the previous stages being less efficient than the output stage; however, their contribution to the overall efficiency is smaller because of their smaller output power (Patterson, 2002).

Table 2.1 : Gain, f_{3dB} and f_T comparison of cascaded cells given in Figure 2.23.

1st Stage	2nd Stage	3rd Stage
$\lvert G_{v1}\rvert = G_m \dfrac{Z_0}{2}$	$\lvert G_{v2}\rvert = G_m Z_0$	$\lvert G_{v3}\rvert = G_m Z_0$
$f_{3dB} = \dfrac{1}{2\pi(Z_0/2 + r_i)C_{gs}}$	$f_{3dB} = \dfrac{1}{2\pi(Z_0/2 + r_i)C_{gs}}$	$f_{3dB} = \dfrac{1}{2\pi(Z_0 + r_i)C_{gs}}$
$\lvert G_v\rvert\, f_{3dB,CS} = f_T$	$\lvert G_v\rvert\, f_{3dB,CS} = 2 f_T$	$\lvert G_v\rvert\, f_{3dB,CS} = f_T$

2.3 Limitations on Wideband Power Amplifier Design

Design of wideband power amplifiers needs to consider some of the limitations, which limit the performance of the circuit. None of the basic design specifications including power, linearity, efficiency, and bandwidth is free of the other from the design perspective and all the specifications have tradeoffs between each other. In this section, we will determine some of well-known limitations to design wideband and efficient amplification.

2.3.1 Limitation on power-bandwidth

The power frequency limit (known as pf^2) originates from the inherent limitation of the breakdown voltage that can be achieved by any given high frequency device technology. This limits the output power that can be obtained by the device over a wide bandwidth. It can be shown that there exists a relation (Rohde et al, 2010),

$$f_T V_{br} \leq \frac{E_{max} v_{sat}}{2\pi} \quad \textbf{(2.56)}$$

where E_{max} is the breakdown electric field, v_{sat} is the velocity of carrier (i.e. electron in most of the high-speed, high power devices). This equation indicates the tradeoff between the high power (i.e. high breakdown voltage) and wideband operation of the device.

For a given device, simply by taking $R_{L,opt}$ to be equal to Z_0, P_{out} over this load related to the equation (2.56) can be written as,

$$P_{out,max} \cong \frac{V_{br}^2}{8Z_0} \leq \frac{(E_{\max} v_{sat})^2}{8\pi^2 Z_0 f_T^2} \quad \textbf{(2.57)}$$

By rearranging the equation, we can conclude the power frequency limit as,

$$f_T^2 P_{out,max} \leq \frac{(E_{\max} v_{sat})^2}{8\pi^2 R_{L,opt}} \quad \textbf{(2.58)}$$

It is important to notice that this trade off does not mean that high f_T devices have lower power capabilities. High output power can be obtained over narrow bandwidths at high frequency by matching to $R_{L,opt}$.

2.3.2 Limitation on wideband matching

In wideband PAs, the crucial task is to transfer power from source to load by transforming complex load impedance $Z_L=R_L+jX_L$ to match a resistive or complex source impedance $Z_S=R_S+jX_S$ over a wide frequency band. These impedances are usually measured at a finite number of radio frequencies. We have shown that at any particular frequency, the maximum available source power to the load occurs when input impedance is a complex conjugate of source impedance. In the design of wideband impedance transformers, the aim is to find an equalizer network that minimizes the mismatch, thus maximizing the transducer gain. Carlin and Civalleri (1998) indicated that conjugate matching is not physically possible over a finite frequency band.

The most critical step of any wideband power amplifier design is the synthesis of the matching networks, which ensure that maximum power is transferred to a load within the operation band. In practice, this cannot be realized easily for all the frequencies of interested. Fano (1950) has shown the theoretical limitations for the broadband matching of any arbitrary impedance. According to his study, there is a general limitation on the bandwidth which an arbitrarily impedance match can be obtained in the case of a complex load impedance. A general and well-known name of the criterion called Bode-Fano limit can be derived for parallel RC load impedance as given in Figure 2.24.

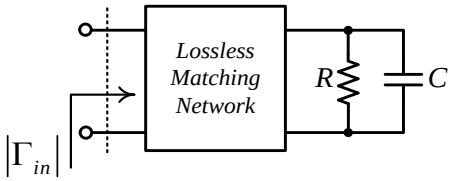


Figure 2.24 : Matching network representation for parallel-RC load impedance.

The corresponding Bode-Fano expression is,

$$\int_0^{\infty} \ln \frac{1}{|\Gamma_{in}(\omega)|} d\omega \leq \frac{\pi}{RC} \tag{2.59}$$

where **(2.59)** can be rearranged to be inspected by terms of both Δf and $|\Gamma_{in}(\omega)|$ as given below.

$$\Delta f \leq \frac{-1}{2RC \ln |\Gamma_{in}(\omega)|} \tag{2.60}$$

$$|\Gamma_{in}(\omega)|_{min} \geq e^{\frac{-1}{2\Delta f RC}} \tag{2.61}$$

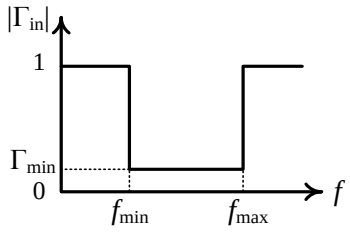


Figure 2.25 : Ideal representation for reflection coefficient of RC-loaded lossless matching network.

Figure 2.25 shows an ideal illustration for the reflection coefficient $|\Gamma_{in}(\omega)|$ seen from the input of an ideal RC-loaded lossless matching network. According to the expressions above, it is possible to have theoretically infinite bandwidth with zero value capacitance or zero value susceptance. Networks having no susceptance part only need to match their real admittances (i.e. conductances). Real impedance transformation is the matching problem of the real-only impedances. The theoretical bandwidth for any real-only impedance matching network is infinite as derived above given equations.

In practice, there are always reactance/susceptance parts for the complex impedances at both input and output ports of any given active device. Behind that, active device input/output terminals behave nonlinear under large signal conditions. From the power device perspective, the main problem arises as the optimum impedance-tracking problem of the matching network, which must ideally keep the track of load-pull impedances data with the increasing frequency. Generally, this is not an easy task. In other words, one cannot easily obtain convenient matching networks to transform optimum impedance loads into a known real load (e.g. 50Ω) in the entire band. In general, frequency response of the optimum output impedance rotates counter-clockwise direction on the smith chart while the corresponding matching networks simply rotate on clockwise direction. Because of this fact, there are only a few (simply two) frequencies where the solution matches perfectly and the impedance matching network provides the desired power matching condition (Sechi and Bujatti, 2009).

There are many approaches to synthesize wideband-matching networks to alter wideband power transferring problem. Yarman (2010) summarized various analytical techniques suitable for the wideband-matching of the networks in which the Real Frequency method is emphasized mostly. Vatankhah and Boumaiza (2009) also reviewed the well-known synthesis methodologies suitable for such wideband-matching networks. Because the detailed underlying theory for wideband-matching problem is out of the thesis scope, it will not be considered here in detail.

2.3.3 Limitation on class of operation

In this section, we will look at the classes of operation that are suitable for the use of wideband PA design. Although there are many different class of operation, we will

focus mostly on class-A and AB/B operations which will be shown to best suit wideband operation.

2.3.3.1 Class-A

Class-A operation for an amplifier means that the transistor operates in the active region at all times. Figure 2.26 shows the simple class-A circuit. In this class of operation, drain/collector current flows for 360° of the signal cycle (Gupta et al, 2001). The designer usually tries to bias Q-point somewhere near the middle of the load line as shown in Figure 2.27.

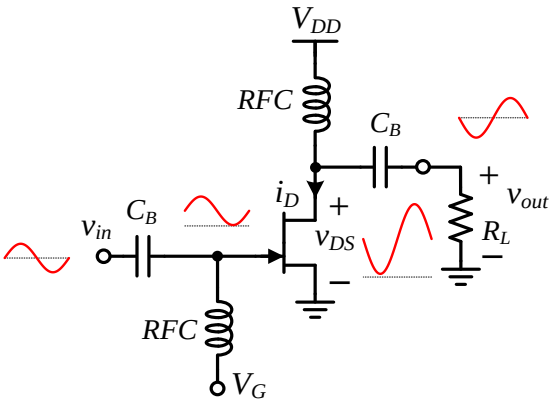


Figure 2.26 : Class-A PA circuit schematic.

Optimum load for this operation is,

$$R_{L,opt} = \frac{V_{br} - V_{knee}}{I_{DSS}} \tag{2.62}$$

The maximum power obtainable from the output is then equal to

$$P_{out,max} = \frac{\left(V_{br} - V_{knee}\right)^2}{8R_{L,opt}} \tag{2.63}$$

In class-A operation, the transistor small-signal parasitic elements are relatively invariant through the signal swing operation yielding low distortion operation. This simplifies the design. However, the linearity degrades at higher input powers when the load-line reaches the knee or cutoff. High bandwidth could be obtained, as the harmonic frequencies need not be tuned. Since the transistor is always on, the large-signal gain is the highest in this configuration. For power amplifiers whose frequency

of operation is a significant fraction of f_{max}, class A can be the only possible mode of operation with reasonable power gain (Paidi, 2004).

Class-A power amplifiers have the highest linearity and power gain compared to other amplifier classes. However, due to the bias point in the middle of the transconductance region of *i-v* curves, a large quiescent current flows into the device resulting in huge power dissipation. The theoretical maximum power efficiency is 50%.

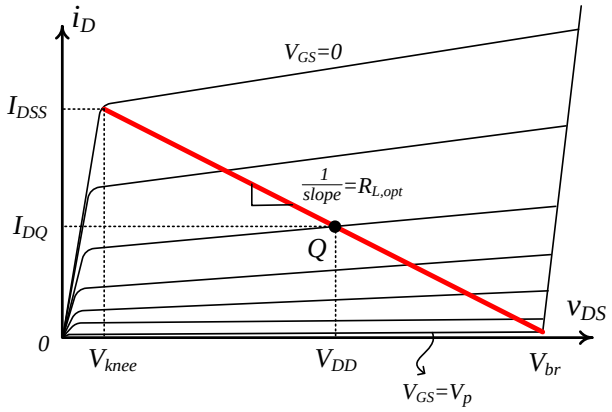


Figure 2.27 : Load-line of class-A operation.

2.3.3.2 Class-AB/B

A class-AB power amplifier is a good compromise between a class-A and a class-B amplifier and is biased such that the conduction angle is between 180° and 360°. The biasing condition of PA in a class-B is set at the threshold of conduction so the transistor is active half of the time and the drain current is a half-sinusoid. Since the amplitude of the drain current is proportional to drive amplitude, class-B provides linear amplification only when conducting. The instantaneous efficiency varies linearly with the RF-output voltage and reaches to a maximum value of nearly 78.5% for an ideal PA. For low-level signals, class-B is significantly more efficient than class-A, and its average efficiency can be several times that of class-A at high peak-to-average ratios (Raab, 2002).

The linearity of class-AB amplifiers is close to that of class-A amplifiers while the efficiency is close to that of class-B amplifiers (Shrestha, 2010). The bias point for class-AB/B amplifiers is selected depending on the linearity and efficiency requirements. Figure 2.28 shows a class-AB/B tuned amplifier where the sinusoidal output signal is obtained using an LC resonator tuned to the fundamental frequency.

The drain voltage and current waveforms are sinusoidal and half-sinusoidal respectively and the drain is biased at roughly half the peak-peak RF output voltage swing. Since the transistor is off when the voltage across it is high, lower dc consumption and hence higher efficiency is succeeded. However, this configuration is inherently narrowband because the LC resonator that is designed to be a short circuit (when series) or open circuit (when parallel) at the fundamental frequency and vice versa at the second harmonic and so even bandwidths of 2:1 (i.e. 66%) are hard to realize (Krishnamurthy, 2000a).

As mentioned above, a single class-B operation produces a large amount of distortion in the signal. This distortion takes the form of adding harmonics of the fundamental frequencies. By the use of a push-pull circuit, we are able to cancel the even harmonics in the class-B amplifier and both high efficiency and good output signal is possible to obtain.

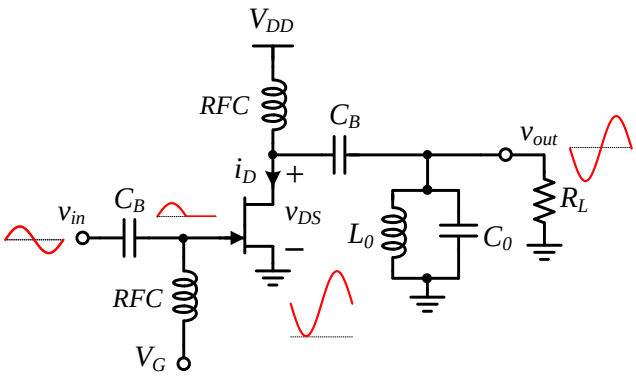


Figure 2.28 : Class-AB/B tuned amplifier.

Load-line of a class-B operation for a given FET device is given in Figure 2.29. As the current conduction happens only half of the period, load-line slope is increases ($R_{L,opt}$ is decreases) in class-B (also in class-AB) operation. Linear power amplification can also be achieved with using class-B push-pull implementations. Push-pull operation also provides a larger impedance transformation ratio than parallel in-phase combining, which is particularly important for large periphery devices.

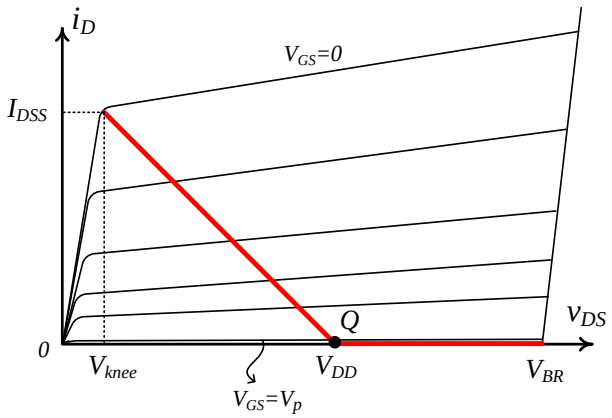


Figure 2.29 : Load-line of class-B operation.

In the push-pull operation, transistors conduct on alternate half of the signal to provide fully sinusoidal output waveform. For this aim, a transformer is needed at the input and output (Lee, 2003). Since complementary devices and magnetic materials are not available at microwave frequencies, 180º hybrid couplers known also as the balanced to unbalanced transformer (balun) have to be used instead of transformers. A class-B push-pull configuration is shown in Figure 2.30.

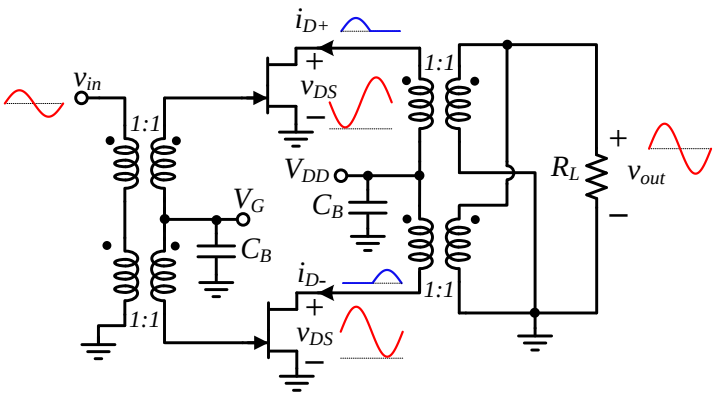


Figure 2.30 : Class-B push-pull amplifier.

According to operation, the two primary and secondary windings are connected in series at the input (i.e. series-series transformer). By this way, we can create equal amplitude and 180° out of phase voltages for the two devices. Such a balun (or transformer) used in the circuit provides a high impedance (open) termination for even mode signals and is not suitable for the output.

Moreover, at the output, we have 180° out of phase sinusoidal voltage waveforms from the two transistors, but the current waveforms have to be out of phase and half sinusoids for a true class-AB/B operation. This requires a zero impedance (short) termination for the even mode (symmetric) drain current. This is achieved using

transformers by connecting the primary windings in series and the secondary windings in shunt (series-shunt transformer).

On the other hand, a series-shunt transformer in Figure 2.31a could be realized using a series-series transformer as shown in Figure 2.31b. By this way, we can short the symmetric drain currents with a separate even mode termination. For broadband operation we require that both the balun and the even mode termination be broadband (Krishnamurthy, 2000a).

In the wideband design, the difficulty of balun designs often came from being physically too large to fit into IC chips, which are impossible to fabricate in a monolithic form (Nguyen, 2012).

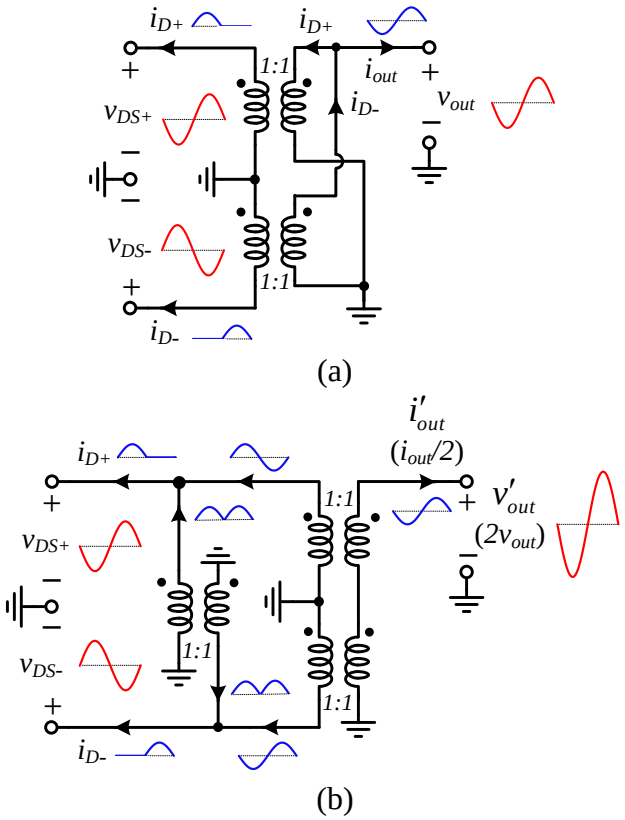


Figure 2.31 : Transformer configurations for class-B operation (a) series-shunt (b) series-series operation (Krishnamurthy, 2000a).

2.3.3.3 Nonlinear classes of operations

These classes of amplifiers are different from the linear classes because the output power is not a linear function of the input power. Nonlinear classes of PA operations such as D, E and F are based on the idea that the active device operates in saturation and behaves as a switch with low impedance while the linear classes of operations such as A, AB, and B employ transistors as current sources with high impedance. If

the transistor is an ideal switch, a 100% of efficiency can be achieved by the proper design of the output-matching network.

Linear power amplifiers preserve amplitude and phase information, whereas nonlinear power amplifiers only preserve phase information. Linear power amplifiers can drive both broadband and narrowband loads where the nonlinear power amplifiers usually drive a tuned circuit and narrowband load. Nonlinear classes are out of the thesis scope and will not be studied any more.

2.4 Chapter Evaluation

In this chapter, we have started by introducing the basic characteristics of PAs. Although there are many terms and terminologies to characterize high frequency and microwave PA behavior, we have focused on the titles, which are useful in the design of wideband PAs. Continuously, the transistor figures of merit are defined to introduce active device behavior by means of power and maximum operating frequency. In this manner, we have introduced the load-line theory and load-pull concepts to show their importance over small-signal conjugate matching technique. After that, the most common and basic structures: common source and cascaded amplifiers are inspected with their capabilities over wideband operations. After all basic and fundamental subjects, the limitations on wideband PA design are given to show the basic and fundamental problems in the design of wideband PAs. Here we have concluded that, although the low-efficiency problem is inevitable, the linear class of operation is required to operate in the wideband.

From now on, we will start inspecting for possible solutions previously proposed in the literature and will try to make some of the design suggestions and systematics to help any designer on the design of wideband PAs.

3. COMPARISON ON DEVICE TECHNOLOGIES AND DESIGN TOPOLOGIES

In this chapter, in the first phase, we will review various solid-state device technologies, which are used frequently in the design of wideband PAs. Since the applications extend from low-frequency range of a few hundred MHz to microwave range, the choice of a device is affected by many different criteria, which are related to fundamental operation mechanisms and they determine the overall performance. From this perspective, we will examine the most frequently used solid-state device technologies.

In the second phase of this chapter, we will introduce the basic and well-known design topologies to implement wideband power amplifiers. For this aim, we will classify circuit topologies into sub categories and will examine the basic and fundamental operations of these topologies with the given comparative example designs.

3.1 Solid-State Device Technologies for Wideband Power Amplifiers

In this section, we will introduce some of the silicon and III–V compound based device technologies, which are suitable for high-power and wide bandwidth applications. These technologies are silicon based ones: silicon-germanium (SiGe) heterojunction bipolar transistors (HBT), laterally diffused metal oxide semiconductor (LDMOS) devices, silicon carbide (SiC) devices and metal semiconductor field effect transistor (MESFET).

Beyond those devices, we also summarize some of the high electron mobility transistor (HEMT) technologies, which are used in today's modern III–V compound semiconductor technology such as gallium arsenide (GaAs) and gallium-nitride (GaN) HEMT. Selecting a suitable device technology depends on the needs of the given application. Among all the specifications, output power and bandwidth are the

most sufficant factors, which also determine the cost of the overall implementation process.

3.1.1 SiGe HBT device technology

At the beginning of the 1980s, III–V HBTs have been intensively studied due to their high potential for high-speed analogue and digital electronics systems. In the 1990s, Si and SiGe HBTs from a bipolar complementary metal-oxide semiconductor (BiCMOS) technology have been developed for the wireless market applications (Andrews, 2009). It seems obvious that the high integration level and the low cost of the SiGe technology are the significant advantages over the III–V technology (e.g. GaAs, InP HBTs).

The main physical difference between the HBTs and traditional homojunction bipolar transistor (BJT) is that at least one of HBTs two junctions is composed of different semiconductor materials. Table 3.1 summarize the frequently used HBT material combinations according to substrate material. Figure 3.1 shows a cross-section of SiGe HBT where the base Si region is compounded with the Ge atoms to form a thin SiGe layer. In the npn-type HBTs, the emitter-base junction is a heterojunction where the emitter is wide gap and the base is narrow gap material. By this way, a high potential barrier over emitter-base heterojunction stops holes from being injected back into the emitter region and for that reason; it enables the emitter efficiency to be almost one even if the base is highly doped. In this way, base sheet resistance is lower than in ordinary BJTs and the resulting operating frequency is accordingly higher and noise performance is better (Burghartz, 2013).

Nowadays, SiGe HBT technologies are commercially available in a number of foundries and f_T/f_{max} frequencies are possible to over 300/500GHz as seen in Figure 3.2. The main advantage of HBT with respect to FET devices, where PAs are concerned, is said to be the higher linearity, which seems to be related to the base-emitter junction capacitance and its beneficial effect in reducing the intermodulation products (Oki et al, 1997). The main drawback of SiGe HBTs appears when designing PAs. This is due to SiGe's low breakdown voltages compared to other III–V technologies.

Table 3.1 : Frequently used HBT material combinations according to substrate material (Pascal et al, 2003).

Type of HBT	Emitter	Base	Collector	Substrate
Single HBT	*AlGaAs*	GaAs	GaAs	
Single HBT	GaInP	GaAs	GaAs	GaAs
Two HBT	*AlGaAs*	GaAs	*AlGaAs*	
Single HBT	*InP*	GaInAs	GaInAs	
Single HBT	*AlInAs*	GaInAs	GaInAs	InP
Two HBT	*AlInAs*	GaInAs	*InP*	
Single HBT	*α-Si*	Si	Si	
Single HBT	*SiC*	Si	Si	Si
Two HBT	Si	*SiGe*	Si	

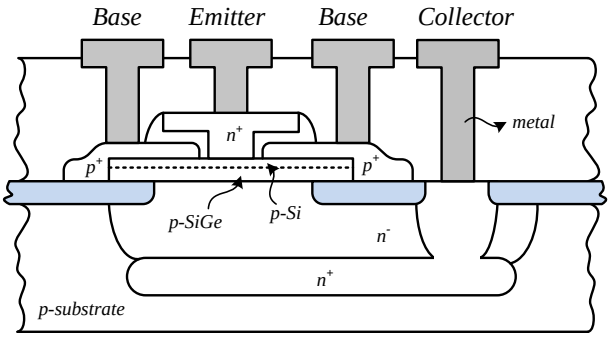


Figure 3.1 : An illustrative cross-section for SiGe HBT.

Breakdown voltage in SiGe is inherently related to peak f_T of operation through the $V_{br} \times f_T$. While SiGe has f_T values over 500GHz, the need for high breakdown voltages in power amplifier design has seen only relatively high power PAs designed at low frequencies in this technology and making the realization of a power amplifier in SiGe HBTs suitable for millimeter-wave operation particularly challenging (Larson, 2004).

Because the SiGe HBT it is a vertical transport device, by scaling-down the device size, its speed does not increase as much as CMOS technology. In other words, f_T/f_{max} of SiGe HBT does not depend on lithography as strongly as it does in CMOS. Giving an example that; a CMOS process of 65nm or possibly even 45nm has the equal performance (as characterized by the peak f_T/f_{max}) with 130nm SiGe. This difference is important, since lithography is the major cost problem in integrated circuit production (Cressler, 2013).

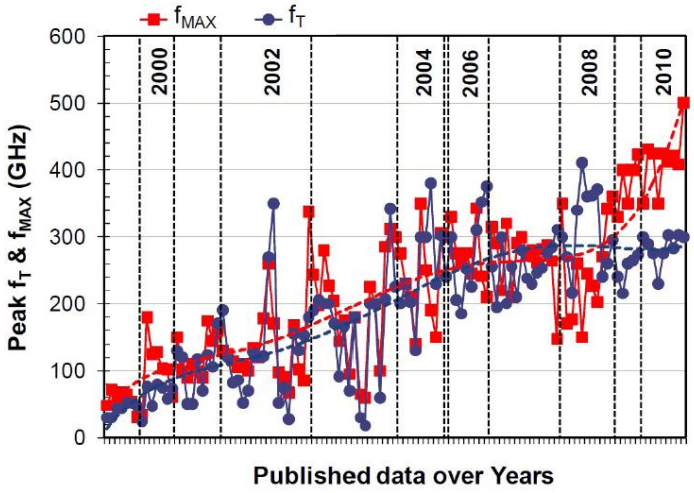


Figure 3.2 : Evolution of the peak f_T and peak f_{max} of SiGe HBTs at 300°K (Cressler, 2013)

3.1.2 LDMOS device technology

Unlike the BJT, LDMOS is a relatively recent technology, developed between the late 1980s and early 1990s, which has become the technology of choice for PA designs for base station applications. Due to its higher gain and efficiency, and most importantly superior linearity, LDMOS has completely replaced the BJT as the technology of choice for linearity critical applications such as the wireless infrastructure base station market (Burger, 2004). Today, LDMOS is the leading technology for a wide variety of RF power applications, such as base station, broadcast, FM, VHF, UHF, industrial, scientific, medical (ISM), and radar applications (Vye et al, 2009).

A cross-section representation for LDMOS transistor is given in Figure 3.3. LDMOS transistor has a drain extension region (drift region) to improve the breakdown voltage up to 80V. Low drain to source on resistance (R_{DSon}) is also achieved through this drift region, which also results in excellent efficiency for pulsed class B power amplifiers (Brech et al, 2003). The LDMOS n-source region is connected to the backside via a metal bridge, a p-type sinker, and a highly conducting p-type substrate. Electrons flow from the source to drain if the gate is positively biased and it inverts the laterally diffused p-well channel. The drain is shielded from the gate by a field plate realizing an extremely low C_{gd} feedback capacitance and good hot carrier reliability properties (Theeuwen and Qureshi, 2012).

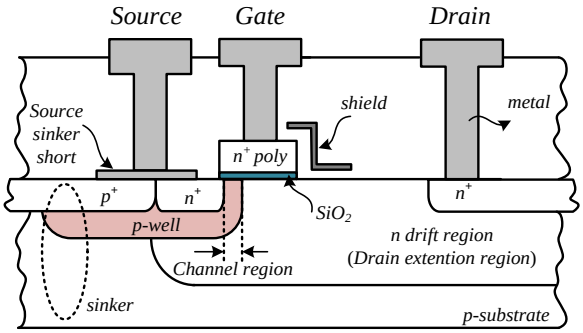


Figure 3.3 : An illustrative cross-section for LDMOS device.

3.1.3 SiC MESFET device technology

MESFETs have a physical structure similar to MOSFETs. The difference is the gate electrode, which uses a metal-semiconductor (Schottky junction) contact instead of a poly-silicon arrangement as in MOSFET. A typical structure of a MESFET is depicted in Figure 3.4. There are two n+ regions, one for source and the other for the drain, while an n-type channel is present between drain and source terminals and connected to the gate by a Schottky junction (Colantonio et al, 2009). Although MESFET is a well-known technology, most mature technology, it is not the best choice for power, especially when the operation frequency is high. This is due to the requirement of small gate length imposed by the high frequency, which translates to smaller channel thickness. This imposes higher doping in order to conserve the current performance and thus smaller breakdown and power (Pavlidis, 1999).

In recent years, silicon carbide has received remarkable attention during the last two decades and there are increasing requests for higher speed, power, efficiency, and broader bandwidth power transistors. SiC MESFET has been attracting much attention as a wide band gap semiconductor device due to its superior properties such as high breakdown field, wide band gap, high electron saturation velocity and large thermal conductivity.

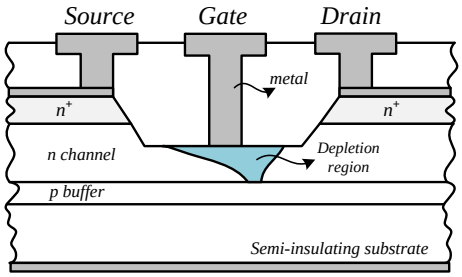


Figure 3.4 : An illustrative cross-section for MESFET device.

The wide band gap of SiC results in both high mobility and high breakdown voltage. Therefore, a SiC MESFET can have a frequency response comparable to that of a GaAs MESFET and breakdown voltages double that of Si LDMOS. On the other hand, the cost of SiC devices is at presently about ten times that of Si LDMOS. (Raab et al, 2002). The high thermal conductivity of the SiC substrate is particularly useful in high-power applications. It is often cited that the thermal conductivity of SiC is higher than that of copper at room temperature (Saddow and Agarwal, 2004). In common, Si, as temperature increases, intrinsic carriers increase exponentially so that undesired leakage currents grow unacceptably large, and eventually at still higher temperatures, the semiconductor device operation is overcome by uncontrolled conductivity as intrinsic carriers exceed intentional device doping. Depending upon specific device design, the intrinsic carrier concentration of silicon generally confines silicon device operation to junction temperatures less than 300°C. With the much smaller intrinsic carrier concentration of SiC, a device operation at junction temperatures exceeding 800°C is theoretically permitted (Neudeck, 2000).

The higher operating voltage and associated higher load impedance greatly simplify output matching networks and power combining. SiC MESFETs typically operate from a 48V supply. Devices with output densities of up to 20W/mm and 20/70GHz of f_T/f_{max} are currently available (Elahipanah and Orouji, 2012).

3.1.4 GaAs HEMT device technology

HEMTs are the improved version of the MESFET geometry by separating the schottky and channel functions. There are some additional layers added to basic MESFET geometry, which are: a heterojunction consisting of an n-doped AlGaAs Schottky layer, an undoped AlGaAs spacer, and an undoped GaAs channel. The discontinuity in the band gaps of AlGaAs and GaAs causes a thin layer of electrons, which is the hearth of the HEMT devices and known as “two-dimensional electron gas” (2-DEG). 2-DEG form below the gate at the interface of the AlGaAs and GaAs layers as shown in Figure 3.5. Separation of the donors from the mobile electrons reduces collisions in the channel, improving the mobility, and hence high frequency response, by a factor of about two (Raab, 2002).

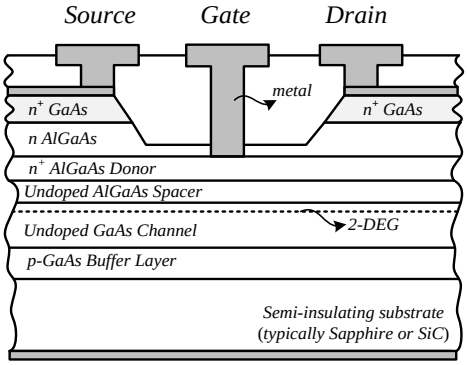


Figure 3.5 : An illustrative cross-section for HEMT device.

The pseudomorphic HEMT (PHEMT) is an enhanced and improved version over the basic HEMT by employing an InGaAs channel. The main purpose on designing the PHEMT material structure is to increase the 2-DEG concentration and improve mobility (Li and Yang, 2013). The increased mobility of In with respect to GaAs increases the band gap discontinuity and therefore the number of carriers in the two-dimensional electron gas.

HEMTs are known in the literature by a wide variety of different names, including MODFET (Modulation-Doped FET), TEGFET (Two-dimensional Electron-Gas FET) and SDFET (Selectively Doped FET). Up to 120/250GHz of f_T/f_{max} are possible to implement using 100nm GaAs PHEMT technology (Url-1, 2013).

Structures with different indium content in the channel. PAs based upon HEMTs exhibit output power levels in excess of tens of watts at X-band and above (Colantonio et al, 2009).

3.1.5 GaN HEMT device technology

GaN HEMTs are the next generation of radio frequency (RF) power transistor technology that offers the unique combination of higher power, higher efficiency and wider bandwidth than competing GaAs and Si based technologies. The design activity and adoption rate is increasing each year; as more GaN based RF component suppliers enter the market with production ready, reliable products (Aichele, 2009).

Many manufacturers of radar, space, and military communication equipment are search for solid-state components to replace travelling wave tube amplifiers where GaN stands as the top choice. Electrical properties of GaN and related components (e.g. AlGaN, InAlN) such as: higher breakdown field, higher electron channel

density and mobility are the main reasons for such high interest (Babic et al, 2010; Jardel, 2012; Lanzerie et al, 2012).

Moreover, an increasing number of GaN PAs designs based on the well-known wideband techniques are proposed to show both high-power and wideband performance simultaneously. The combination of good electron transport capabilities and high breakdown field in GaN compared to common semiconductors enables the realization of high voltage, high power and high frequency transistors. Power densities as high as 40 W/mm have been reported (Wu et al, 2006). Significant research is also being invested in GaN for power generation at millimeter frequencies. Recently reported f_{max} of 400 GHz shows how GaN may play a part in bridging the THz range applications (Shinohara et al, 2010).

3.1.6 Comparison for different device technologies

It is clear from the previous subsections that, there are huge advantages of the wide band gap devices when designing wideband and high output devices. Table 3.2 shows the advantages of wide band gap devices according to the needs of applications. From the material properties of view, comparison of Si and wide band gap semiconductors is listed in Table 3.3 with the depicted figure of merits (FoMs).

Table 3.2 : Some of the advantages of wide band gap devices.

Goal	How to success?	Advantage
High-power per unit width	Wide band gap, High field	Compactness, Simple matching
High V_{sup}	High V_{br}	Eliminating step-down biasing circuitry
High-linearity	HEMT	Optimum Band Allocation
High-frequency	High-electron velocity	Bandwidth, mili/micro wave operation
High efficiency	High V_{sup}	Power saving, reduced cooling
High junction temperature	Wide band gap devices	Reliabity, reduced cooling

SiGe HBTs has the capabilities of easy integration and so they are very cost effective devices. However, the SiGe HBT device structure remains a relatively low power capabilities, thus it is not a candidate for high power and high frequency applications.

If very-high frequency linear operation is required, (P)HEMTs offer the best choice due to their high gain up to millimeter-wavelengths and their good noise and power

performance over HBTs are attractive at cellular radio frequencies for power amplification. The advantages of the HEMT include its high carrier concentration and its higher electron mobility due to reduced ionized impurity scattering. The combination of high carrier concentration and high electron mobility results in a high current density and a low channel resistance, which are especially important for high frequency operation and power switching applications (Mishra et al, 2008).

The high performance of SiC thermal conductivity over Si, GaAs and GaN is worth considering. The wide bandgap energy and low intrinsic carrier concentration of SiC allow it to maintain semiconductor behavior at much higher temperatures than Si and GaAs technologies. SiC MESFETs benefit from the excellent thermal conductivity of its substrate. However, its electron mobility is significantly lower than that of GaN, which is related to the lack of availability of heterojunction technology in this material system. On the other hand, the ability of GaN to form heterojunctions makes it superior compared to SiC, in spite of having similar breakdown fields and saturation electron velocities (Colantonio, 2009). GaN can be used to fabricate HEMTs whereas SiC can only be used to fabricate metal semiconductor field effect transistors MESFETs. GaN is also cost-effective to SiC. High quality GaN transistors can be grown onto large diameter Si substrates, being a major cost advantage (Visalli et al, 2009).

As was seen from Table 3.3, although Diamond (C) seems to have excellent properties to other materials, there are still many issue need to be solved before having cost-effective and stable diamond based devices.

Table 3.3 : Some properties of wide band gap materials over Si.

Property	Si	GaAs	SiC[4]	GaN[5]	InP	Diamond
Bandgap, E_g (eV)	1.12	1.43	3.26	3.45	1.35	5.45
Dielectric Const. ε_r	11.9	13.1	10.1	9.0	10	5.5
Breakdown Field, E_c (MV/cm)	0.3	0.45	2.2	2	50	10
Electron mobility, μ_n (cm^2/Vs)	1500	8500	1000	1~2×10^3	5400	2200
Hole mobility, μ_p (cm^2/Vs)	450	330	115	850	200	850
Thermal Conductivity (W/cm°K)	1.5	0.46	4.9	1.3	0.68	22
Saturated velocity, v_{sat} (×10^7cm/s)	1	1	2	2.2	2	2.7
Baliga FoM (Baliga, 1989)	1	16	34	100	6.5	12500
Johnson FoM (Johnson, 1965)	1	11	410	790	31	5800

[4] SiC metarial here is a hexagonal polytypes of 4H-SiC.
[5] Mobility quantity of GaN is belong to AlGaN/GaN heterostructure .

Some of the wide band gap technology based nominal device performances are summarized in Table 3.4. As seen in the table, GaN HEMT has the highest W/mm power density among the others. A high power density is advantageous as the physical size is smaller and suffers less from parasitic. Since the R_{opt} impedance level is higher in the GaN HEMT than the GaAs version, it helps to implement both hybrid and MMIC high power PAs due to the possible power combining techniques. A higher R_{opt} is also suitable with LDMOS technology, however, at the price of much higher output capacitance and so the less bandwidth. As it was shown before in Bode-Fano criteria in equation (2.59), the fractional bandwidth and the matching criteria could be re-arranged as Andersson (2013) depicted:

$$\frac{\Delta\omega}{\omega_0}\ln\frac{1}{|\Gamma|} \leq \pi\frac{X_{Cds}}{R_{opt}} \tag{3.1}$$

According to equation, there exists a fundamental limitation on matching, depend on the both device parameters, R_{opt} and X_{Cds}. The X_{Cds}/R_{opt} ratio is also independent of the device periphery and gives information about the possible bandwidth of the device operation. Higher the X_{Cds}/R_{opt} ratio is better when designing wideband networks.

Table 3.4 : Technology based nominal electrical properties of some wide band gap materials (Cripps, 2006).

	V_{sup} (V)	I_{max} (mA/mm)	C_{ds} (pF/mm)	R_{opt} (Ω.mm)	X_{Cds}/R_{opt} (f_o=1GHz)
GaAs PHEMT@2GHz	10	350	0.25	57	5.6
GaAs PHEMT@10GHz	10	350	0.25	57	1.1
Si LDMOS@850MHz	28	200	1.0	280	0.7
Si LDMOS@2GHz	28	200	1.0	280	0.3
GaN HEMT@2GHz	40	600	0.3	133	3
GaN HEMT@10GHz	40	600	0.3	133	0.6

3.2 Basic Design Topologies for Wideband Power Amplifiers

In this section, we will review the conventional design topologies for the discrete, hybrid and monolithic design of wideband PAs previously presented and implemented. Conventional approaches to design and implementation of wideband amplifiers could be classified into some of sub-categories such as: Resistive/reactive feedback PAs, Reactively matched PAs, lossy-matched PAs and distributed PAs. It is

evident to clarify pros and cons of these topological structures and distinguish the differences between the implementations. By this way, we could choose a suitable approach and go on to success on the motivations and aims of this work.

3.2.1 Resistive/reactive negative feedback power amplifiers

First topological approach to wideband PAs is the resistive/reactive feedback technique, which is used widely in general wideband RF amplifier design. Feedback technique has the advantages of increasing bandwidth, stable operation, simple design, controlling over the input/output impedances, reducing parametric sensitivities and increasing linearity (Sayed, 2005; Virde et al, 2006).

From the basic feedback knowledge, four basic feedback configurations could be listed as: shunt-shunt, shunt-series, series-shunt and series-series.

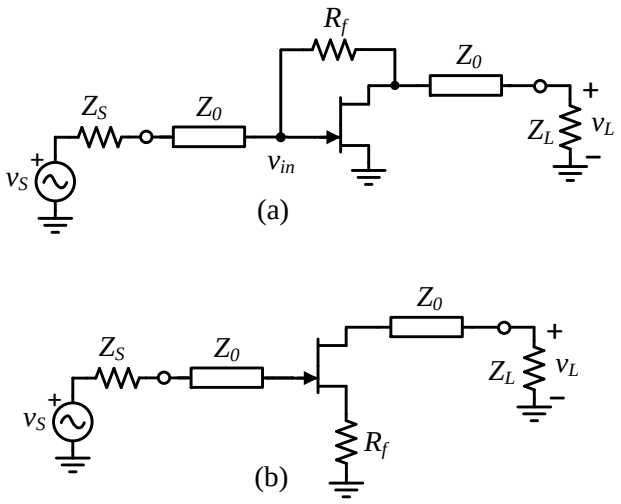


Figure 3.6 : Simple representation for (a) resistive shunt-shunt feedback (b) series-series feedback CS PA.

The feedback amplifiers shown in Figure 3.6a-b employs shunt-shunt and series-series feedback, respectively where R_f's are the feedback resistors.

With the help of small-signal equivalent given in Figure 2.5b and ignoring the internal parasitic for simplicity, we can written the device y-parameters when shunt-shunt feedback is applied

$$[y]=\begin{bmatrix} \frac{1}{R_f} & -\frac{1}{R_f} \\ g_m-\frac{1}{R_f} & \frac{1}{R_f} \end{bmatrix} \tag{3.2}$$

then converting y-parameters into s-parameters, we can conclude that,

$$\begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix}=\frac{1}{\Delta}\begin{bmatrix} 1-\frac{g_m Z_0^2}{R_f} & -2g_m Z_0^2+\frac{2Z_0}{R_f} \\ \frac{2Z_0}{R_f} & 1-\frac{g_m Z_0^2}{R_f} \end{bmatrix} \tag{3.3}$$

where Δ is equal to,

$$\Delta=1+\frac{2Z_0+g_m Z_0^2}{R_f} \tag{3.4}$$

As for the matching purpose of the device, s_{11} and s_{22} is desired to have zero value, by applying the conditions we can get the value of feedback resistor as,

$$R_f\Big|_{s_{11}=s_{22}=0}=g_m Z_0^2 \tag{3.5}$$

When inspecting the equation (3.3), we see that the gain related to s_{21} could be flatten by proper design of R_f as in (3.5).

The resistive feedback configuration results in poor output power density due to the additional loss in the feedback resistor. On the other hand, the reactive feedback PA topologies are suitable for bandwidth less than one octave and suitable for high power and relatively higher PAE. Since they use frequency dependent reactive elements, they require more matching elements to implement wider bandwidth. However, because of higher-Q of the reactive elements, poor gain flatness and narrow band input/output matching is also another drawback in reactive feedback configurations (Bahl, 2007).

Using an inductor is preferable when designing with reactive feedback. This is related more to noise specifications. Using inductor in source/emitter may help to improve overall noise performance of the amplifier. By this way, the input could be both more resistive and low ohmic that results in relaxed impedance matching at the input side.

From the literature point of view, although they have design simplicity and cost effective and multi-octave performance, the feedback amplifier designs are not preferred much when concerning with the power amplifiers. This is mostly due to the loss of the resistive part, which is dropping the efficiency more at the lower end of the operation bandwidth.Table 3.5 lists the some of the previously proposed Resistive/Reactive feedback wideband high-power PAs. In most of the cases, including the table circuits, resistive/reactive circuits are the parts of the overall PA design. They are generally placed to drive a higher power output stage circuitry. By this way, an improved input matching and overall PA stability could be ensured.

3.2.2 Reactively matched power amplifiers

Reactively matched amplifiers are another PA design topology to obtain wideband power amplification. The idea behind the reactively matched amplifier is based on the resonance of inductive and capacitive elements. The input and output terminals of any given transistor can be represented by either series or parallel combination of capacitor and resistor (see Figure 2.5). To match a real impedance (e.g. Z_s=50Ω) to complex input impedance of the given transistor, one have to resonate the reactance part of the input impedance. It is clear that the resonance is a frequency dependent operation or in another way to say, these reactive elements together form a filter, which limits and narrow the bandwidth.

In Figure 3.7a-b, a simple circuit implementation of reactively matched amplifier and its characterizing frequency response is shown. To resonate the internal C_{gs} capacitance of the input impedance, an inductance, L is shunted at the input of the transistor.

Table 3.5 : Some of the previously proposed resistive/reactive negative feedback wideband PAs.

Reference	Technology (Vendor)	Implementation	Die Size (mm^2)	BW (GHz)	BW (%)	P_{out} (dBm)	P_{sat} (dBm)	Gain (dB)	PAE (%)	DE (%)
Sun et al, (2012)	0.13µm CMOS	IC Cascaded	1.1×0.8	0.7 – 6	158	6 – 11	-	20±3	>6%	-
Lin et al, (2011)	GaN on SiC (TriQuint)	Hybrid, Multi Stage	-	0.03 – 4	197	35	-	42±1.75	-	-
Huang et al, (2010)	GaAs+CMOS	MMIC, Stacked	0.9×0.76	1 – 5	133	18 – 20	20–22	17.5±2.5	18 – 36	-
Seo et al, (2010)	LDMOS (Freescale)	Discrete, Stacked	-	0.002-0.51	198	46– 48	-	43±2	28 – 49	-
Kobayashi *et al*, (2007)	0.2µm GaN on SiC	MMIC	1.7×1.7	0.2–8	190	33	34	14±6	28–37	-
Ezzeddine and Huang (2006)	0.5µm GaN	MMIC	4	0.03–2.5	195	33– 36	33–37	21±1	-	20–40
Sayed, (2005)	GaAs+SiC	Discrete	-	0.01 – 2.4	198	37 – 39	-	23±1	28	-
Krishnamurthy et al, (2000b)	TriQuint GaAs IC	Flip Chip Bonding	1.1×1.45	0.2 – 6	187	23 – 25	-	13±1	22 – 40	-
Sayginer et al, (2011b)	**0.35µm SiGe HBT**	**IC**	**1.0×1.3**	**0.2 – 2.2**	**167**	**13 – 16**	**-**	**7.5±1**	**11 – 35**	**-**
Sayginer et al, (2011b)	**0.35µm SiGe HBT**	**IC**	**1.8×2.3**	**0.2 – 2.2**	**167**	**17 – 20**	**-**	**22±3**	**10 – 30**	**-**
Sayginer et al, (2013)	**0.25µm GaAs PHEMT**	**MMIC**	**1.3×2.9**	**1 – 8**	**156**	**25 – 28**	**28 – 30**	**~9**	**27 – 45**	**-**
Sayginer et al, (submittion)	**0.25µm GaAs PHEMT**	**MMIC**	**3.4×1.4**	**1.5 – 9**	**143**	**28 – 29**	**29 – 30**	**15±1**	**36 –39**	**-**

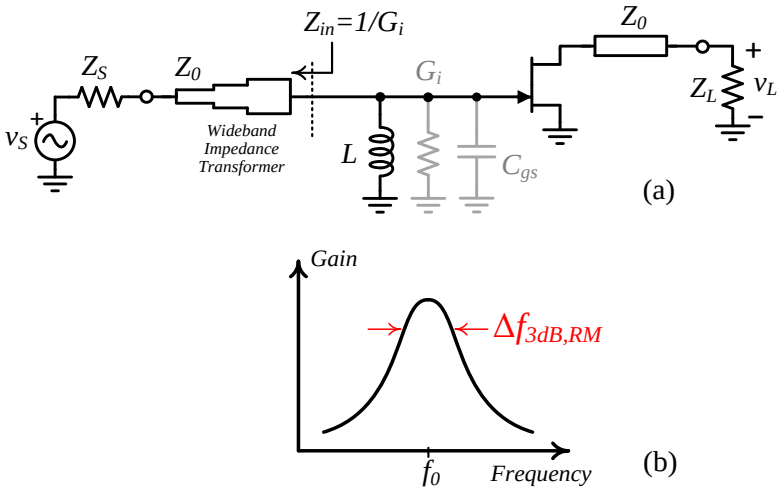


Figure 3.7 : Simple representation for (a) reactively matched amplifier and (b) corresponding frequency response.

After all, the only need for complete matching is to transform equivalent real input conductance into the real source impedance. For this aim, we could possibly use a wideband impedance transformer (Krishnamurthy, 2000a). Basic circuit analysis yields that the required inductance value to resonate with input C_{gs} is equal to,

$$L = \frac{1}{4\pi^2 f_0^2 C_{gs}} \tag{3.6}$$

where f_0 is the center design frequency and by taking the load-line match at the output, corresponding $s_{21,RM}$ and transducer power gain, $G_{T,RM}$ of the amplifier could be calculated as,

$$s_{21,RM} = \frac{g_m Z_0}{2\pi f_0 C_{gs}\sqrt{R_i Z_0}} \tag{3.7}$$

$$G_{T,RM} = \frac{(V_{br} - V_{knee})\,I_{DSS}}{V_p^2}\,\frac{1}{4\pi^2 f_0^2 C_{gs}^2 R_i} \tag{3.8}$$

where V_{br} is the transistor break-down voltage (V_{max}), I_{DSS} is the maximum current obtainable from the device (I_{max}) and V_p is the pinch-off (or threshold) voltage of the transistor (see Figure 2.14b for details). The bandwidth of the PA can be examined by taking $f_0 << 1/(2\pi R_i C_{gs})$ and can be showed that (Krishnamurthy, 2000a),

$$Q \equiv \frac{f_0}{\Delta f_{3dB,RM}} = \frac{1}{2\pi f_0 C_{gs} R_i} \tag{3.9}$$

$$\Delta f_{3dB,RM} = 4\pi f_0^2 C_{gs} R_i \tag{3.10}$$

3.2.3 Lossy-matched power amplifiers

The input matching performance and the bandwidth of the PA could be increased by introducing loss element (i.e. resistor). In this case, it is possible to damp the resonance and absorbe the reflected power (Ellinger, 2007). The amount of gain reduction in low-frequencies can be controlled by the added loss element, G, as shown in Figure 3.8a-b with the corresponding amplifier frequency response. The positive side effect of the lossy-matched topology is enhanced stability. Major drawback is the increased noise and decreased output power at the point where the loss element is used. A similar analysis can show that the corresponding $s_{21,LM}$, transducer power gain, $G_{T,LM}$, and the bandwidth of the amplifier could be calculated as,

$$s_{21,LM} = \frac{g_m Z_0}{2\pi f_0 C_{gs} \sqrt{Z_{in} Z_0}} \tag{3.11}$$

$$G_{T,LM} = \frac{(V_{br} - V_{knee}) \mathrm{I}_{DSS}}{V_p^2} \frac{1}{4\pi^2 f_0^2 C_{gs}^2 Z_{in}} \tag{3.12}$$

$$\Delta f_{3dB,LM} = \frac{1}{\pi C_{gs} Z_{in}} \tag{3.13}$$

where the bandwidth is shown to be improved with respect to the reactively-matched condition at the cost of gain reduction as illustrated with the frequency response in Figure 3.8b. The designer is responsible to select proper G loss element to trade between the gain and bandwidth. Figure 3.9 shows an example PA representation where both input and output is reactively/lossy matched and suitable for the bandwidth of much less than an octave.

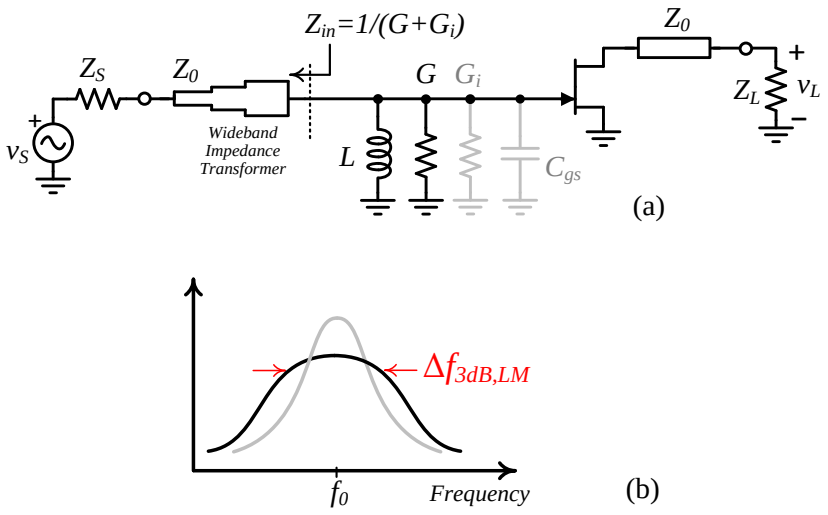


Figure 3.8 : Simple representation for (a) lossy matched amplifier and (b) corresponding frequency response comparing with the reactively matched one.

Reactively/lossy matched topologies require more matching elements to implement wider bandwidth. However, this may result in poor gain flatness and worse matching performance. Unfortunately, wideband-matching of the active devices is not an easy task. Nonlinear behavior of the device input/output impedances make possible solutions harder to apply. There are many studies on the design of wideband-matching networks where many of them are based on the analytical approaches like making closed form solutions as Dawson (2009) was proposed and a well-known real frequency techniques for wideband-matching as was mentioned before in the limitations section (Yarman, 2010). In addition to relax the matching problem, some of the solutions are also based on the impedance tracking methods which are strongly depend on both the optimization techniques and CAD tools (Colantonio et al, 2008; Chen et al, 2007; Patterson et al, 2007). Unfortunately, there are not many systematics to design a wideband-matching in PA easily. Every design has its own specification and its own self-design procedure. Although these disadvantages, reactively/lossy matched topologies are more suitable for high power and high PAE (Bahl, 2007). They are very suitable for the power dividing/combining techniques to improve output power capability of the PA. In Table 3.6, some of the previously proposed reactively/lossy-matched wideband PAs could be observed by their performance metrics.

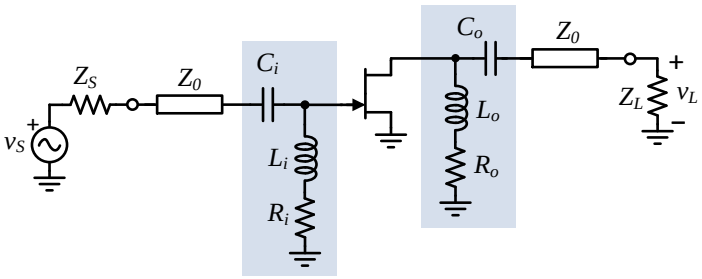


Figure 3.9 : A representation of input and output reactively/lossy matched PA.

3.2.4 Distributed power amplifiers

From the circuit topology point of view, the distributed power amplifiers (DPAs) or known as the travelling wave power amplifiers (TWPAs) are one of the most suitable and preferred circuit implementation to obtain wideband power amplifier for a given specific application. A conceptual operation of the DPA is illustrated in Figure 3.10. If the transmission structures are identical, a wave can be launched on the gate-line and be coherently amplified onto the drain-line. In practice, the constructing of such transmission lines are simple with the identical properties on the gate and drain lines assuming a unilateral transistor over a very wide range of frequencies. Thus, these amplifier topology is naturally broadband.

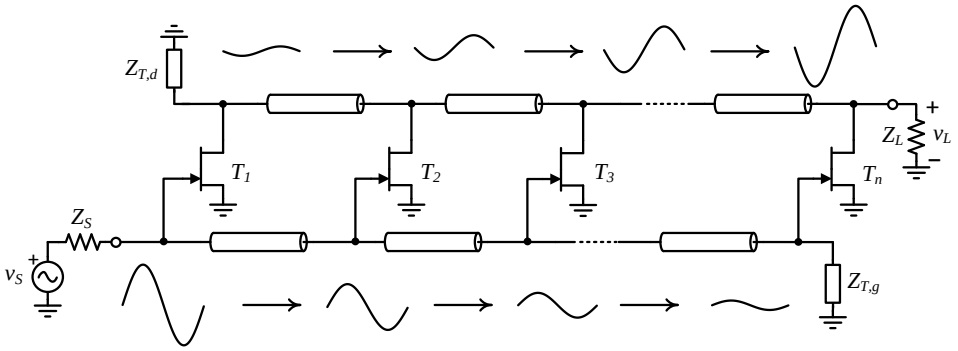


Figure 3.10 : Conceptual representation for DA.

To absorb potential reflections, both lines are terminated with the proper line termination impedances of $Z_{T,d}$ and $Z_{T,g}$. DPAs provide the best gain×bandwidth product with flat gain and low voltage standing wave ratio (VSWR). They are capable of multi-octave bandwidth. However, they have limited output power and poor PAE (Bahl, 2007). DPAs also have low circuit sensitivities (Xie and Pavio, 2007).With using the device parasitic as the part of the transmission lines, device bandwidth related limitations can be avoided.

Table 3.6 : Some of the previously proposed reactively/lossy-matched wideband PAs.

Reference	**Technology (Vendor)**	**Implemen-tation**	**Die Size (mm^2)**	**BW (GHz)**	**BW (%)**	**P_{out} (dBm)**	**P_{sat} (dBm)**	**Gain (dB)**	**PAE (%)**	**DE (%)**
Camarchia et al, (2012)	0.25µm GaN HEMT	MMIC	1.6×4.6	7 – 14	67	>37	-	6.8±1.2	-	43 – 59
Yamada et al, (2011)	GaN HEMT	MMIC	2.0×3.1	6 – 15	86	-	32 – 34	14±2	< 40	-
Jeong et al, (2011)	GaAs HEMT	MMIC	2.36	17 – 28	49	21.5	-	20±2	-	-
Moon et al, (2011)	GaN (Cree)	Discrete	-	1.3 – 2.7	70	40 – 42	-	11±1	-	56 – 70
Krishnamurthy et al, (2008)	0.5µm GaN on SiC HEMT	Multi-chip	5.0×6.0	0.05 – 2.2	198	-	39	12.5±1	32 – 56	37 - 40
Bahl, (2008)	GaAs MESFET	MMIC	5.0×6.3	2 – 8	120	38 – 40	-	15±2	32 – 37	-
Xu et al (2000)	GaN HEMT	Flip-chip	-	3 – 10	108	37 – 39	-	8±2	5 – 19	-
Arell and Hongsmatip, (1993)	0.5µm GaAs MESFET	MMIC	4.4	2 – 6	100	29 – 31	-	20	30 - 37	-
Sayginer et al, (2011b)	**0.35µm SiGe HBT**	**IC**	**1.0×1.3**	**0.2 – 2.2**	**167**	**13 – 16**	**-**	**7.5±1**	**11 – 35**	**-**
Sayginer et al, (2011b)	**0.35µm SiGe HBT**	**IC**	**1.8×2.3**	**0.2 – 2.2**	**167**	**17 – 20**	**-**	**22±3**	**10 – 30**	**-**
Sayginer et al, (2013)	**0.25µm GaAs PHEMT**	**MMIC**	**1.3×2.9**	**1 – 8**	**156**	**25 – 28**	**28 – 30**	**~9**	**27 – 45**	**-**
Sayginer et al, (submittion)	**0.25µm GaAs PHEMT**	**MMIC**	**3.4×1.4**	**1.5 – 9**	**143**	**28 – 29**	**29 – 30**	**15±1**	**36 –39**	**-**

That is to say that, the basic principle underpinning the DAs is the use of inherent parasitic capacitances at the input and output terminals of the transistor together with the external inductive elements to form artificial transmission-lines (ATLs) (Wong, 1993; Virdee, 2000). The cut-off frequency of this class of amplifier is determined by the cut-off frequency of the ATLs. The resulting structure readily provides broadband performance, usually above one decade.

The distributed amplifier is an unconventional technique that allows an amplifier designer to escape the tradeoff between gain and bandwidth. A schematic ATL implementation of a DPA is given in Figure 3.11. Transistor total input and output capacitances C_g and C_d form the shunt elements of low-pass ladder networks. The series inductances and the shunt capacitances of these networks form lumped ATL sections having a cutoff frequency of

$$f_c = \frac{1}{\pi\sqrt{L_g C_g}} = \frac{1}{\pi\sqrt{L_d C_d}} \qquad \textbf{(3.14)}$$

where it is very important to notice that the phase velocities on the gate and drain lines should be identical. Under this circumstance; the signal on the drain line add in the forward direction and arrive at the output as the amplified signal. The waves travelling in the reverse direction are not in phase and uncancelled signal is absorbed by the drain-line termination. As a result of this fact, half of the output power is wasted and so that the efficiency is halved (Beyer et al, 1984; Virdee et al, 2004).

DPA topology has been studied in details for many years to extract its all benefits to improve PA designs. Beyer et al (1984) showed that the frequency response of the DPA is limited by the gate-line attenuation. Prasad et al (1988) inspected the power-bandwidth considerations of the DPAs and they showed that the gate-line attenuation of DPA could possibly be reduced by inserting series capacitors with the active device's gate terminal. As a result, the bandwidth and input power capability increase. In addition to this, the reduction in the gain of the amplifier due to the gate series capacitors can be compensated by increasing the effective gate width of the amplifier or by cascading amplifiers while maintaining a specified bandwidth. This results in an increase in both the output power and the power-bandwidth product of the amplifier.

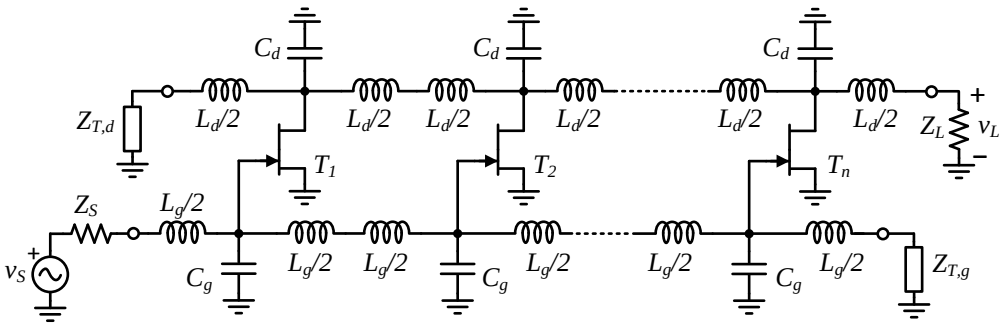


Figure 3.11 : A schematic ATL implementation of a DPA.

The power-limiting mechanisms in DPAs are related to the basic *i-v* limitations of each device, which include gate related voltage limitations: forward conduction and pinch-off voltages and drain related voltage limitations: breakdown voltage. Each device yields its maximum output power when all these limits are reached simultaneously. However, these conditions cannot be simultaneously met in a conventional DPA.

For the PA concept, these constraints, which are limiting to get power from the device and the circuit can be identify in four separate power-limiting mechanisms (Ayasli et al, 1984a). The issues involved in distributed power amplification and power-limiting mechanisms could be classified into four titles, which will be inspected below.

1) *Finite RF voltage swing on the input gate line:* This swing is limited on the positive RF cycle by the forward conduction of the gate and on the negative cycle by the pinch off voltage of the device. Hence, for a 50Ω input impedance amplifier with -3V pinch off voltage transistor and assuming the devices are biased at a drain current of $I_{DSS}/2$ (i.e. class-A), the maximum input RF power to the amplifier is limited by

$$P_{in,\max} = \frac{V_{p-p}^2}{8R_{in}} = \frac{(|-3|+0.5)^2}{8\times 50} = 0.03W \equiv +14.9dBm \qquad \textbf{(3.15)}$$

Where we assumed the forvard conducting voltage as around 0.5V. Thus, maximum output power from the amplifier can not be larger than Gain×$P_{in,max}$.

2) *Maximum total gate periphery:* Due to the frequency-dependent nature of input-line loss, as the input drive increases, usually the first transistor reaches saturation much earlier than the others do. By the time all the transistors are saturated, the first

one is already over-driven, leading to poor efficiency and reliability (Wu et al, 1999). Reported monolithic distributed power amplifiers typically have 10% to 15% PAE. Typically at microwave frequencies, the device nearest the output terminal contributes the most power whilst the device farthest away contributes minimal. Over some frequency ranges, some of the FETs sink rather than source power (Eccleston, 2000).

Ayasli et al (1984) also show that the small-signal gain expression for the distributed amplifier is approximately equal to

$$G \cong \frac{g_m^2 n^2 Z_0^2}{4}\left(1-\frac{\alpha_g l_g n}{2}\right)^2 \qquad \textbf{(3.16)}$$

where, n is the number of the stages, l_g is the length of the gate transmission line per unit cell and α_g is the effective gate-line attenuation per unit length. With using the equation **(3.16)**, it is possible to show that $\partial G/\partial n=0$ occurs at $\alpha_g l_g n=1$. Therefore, the following inequality has to be satisfied for a given design if one intends to employ the devices in a single-stage design most efficiently.

$$\alpha_g l_g n \le 1 \qquad \textbf{(3.17)}$$

By relating the l_g and α_g to the device input parameters r_i and C_{gs}, as in Figure 2.5b, we can write down

$$r_i \omega^2 C_{gs}^2 Z_0 \le 2 \qquad \textbf{(3.18)}$$

Here, r_i varies inversely and C_{gs} varies directly with the periphery of the given device. Hence, in terms of the periphery w per device, equation (3.18) becomes,

$$nw\omega^2 \le \text{constant} \qquad \textbf{(3.19)}$$

As a result, for a specified maximum frequency of operation and for a given device, there is an upper limit to the maximum total periphery, $n \times w$, that can be employed in a DPA design. This maximum periphery determines the gain and consequently the output power of DPA.

3) *Gate - drain breakdown voltage:* When the signal is amplified, the drain terminal voltage swing must be kept under the breakdown voltage limitation. Lowering of the output impedance is not a solution for this limitation since the gain is proportional to the impedance level as given in equation (3.16).

4) *Optimum ac load-line requirements:* For a DPA, the load-line that each individual device sees is predetermined by the drain-line characteristic impedance. In this manner, the only flexibility to control the load-line in the design is the periphery of the unit device. On the other hand, the total periphery is also predetermined from gate-loading considerations. This limitation is always faced as an unmatched condition for the load impedance level (i.e. 50Ω).

For a given device, there exists an optimum value of n to maximize the DPA gain×bandwidth product. Increasing the stage number, *n* will increase the upper frequency gain until the gate-line attenuation cancels the gain contribution of the last device section since it is unable to feed by the input-line. At this point, any additional device will not improve the DPA bandwidth. For the maximum output power, *n* must be as large as possible without degrading the minimum acceptable amplifier gain×bandwidth product (Hartnagel, 1989).

Above all the limitations encouraged the researchers to look for suitable solutions to improve performance of the classical DPA. Consequently, there are many different sub-topologies of DPAs proposed in the literature.

To get rid of the wasted half power problem at the drain-line side, people use the drain impedance tapering technique (Shastry and Ibrahim, 2006; Narendra et al, 2008; Campbell et al, 2009; Sewiolo et al, 2009). In theory, DPAs using tapered impedance drain-lines can provide efficiencies up to the class-A limit of 50%, by eliminating the reverse termination as illustrated in the schematic in

Figure 3.12. In this technique, in order to achieve maximum power contribution from each cell of a DPA, the cell outputs are sequentially connected to a transmission line network that comprises of line segments having predefined characteristic impedance which are not the same that in general changes from segment to segment, and is therefore non-uniformly occurs among cells. By this way, we can rid of the termination impedance at the drain-line and both output power and efficiency theoretically doubled.

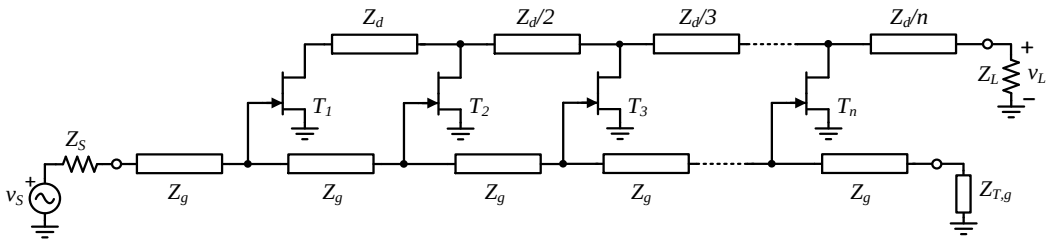


Figure 3.12 : Schematic of tapered-line DPA.

However, because the decreasing nature of the impedance level, tapered drain-line TWAs require high impedance transmission lines with limited current carrying capability, and thus are hard to realize for high output powers in monolithic form.

Dual-fed DPAs are the variation of the conventional single-fed DPAs whereby the input signal is fed to both ends of the input line using a hybrid, and signals appearing at both ends of the output line are combined using another hybrid (Eccleston, 2000). The dual-fed distributed amplification principle is an operation in which the bi-directional nature of the distributed amplifier is used to enhance circuit performance (Aitchison, 1989). There is no idle gate and drain line terminations in the dual-fed DPAs, for this reason, dual-fed DPAs have demonstrated its gain and efficiency advantages over the conventional DPA (Eccleston, 2005). However, wideband hybrids are the main hard issue to overcome when designing dual-fed DPAs.

In the conventional case, a single transistor in the common-source/emitter configuration is the common gain-cell for the DPA as given in Figure 3.13a. Other gain cell structures are also possible to implement. A cascade of two common-source/emitter stages and a cascode (common source-common gate) circuit have been implemented by designers aiming higher gain and/or bandwidth for their DPAs (Green et al, 2001; Liu et al, 2004; Arbabian and Niknejad, 2009; Sewiolo et al, 2009). A cascode gain-cell consists of a common source/emitter transistor followed by a common-gate/base transistor shown in Figure 3.13b. It has higher output impedance, where its output impedance increases by a factor of approximately $(1+g_mR_{ds})$. The higher output impedance reduces the drain/collector line losses and therefore the decreased drain/collector-line attenuation may allow for a better overall match to the drain line or it may allow the designer to use more stages and increases the number of sections which can be utilized (Shohat, 2005). In addition to these, a higher breakdown voltage, a lower input impedance, and reduced Miller effect is also the advantages of the cascode gain cells.

The main drawback of the cascode cell is that; it may worsen the stability of the DPA caused by resonances in the output-line of the amplifier, since the drain/collector-line becomes much less lossy. The cascode structurre might be useful in technologies where R_{ds} is lower, such as in bipolar technology.

Another option for the gain-cell was using the cascaded gain cells instead of the single transistor cell. It can boost the gain. However, the output impedance in the cascade one is identical to that of the common-source/emitter one. The key design step of the cascade gain-cells is the matching network between the two stages. Without some sort of impedance matcher, the bandwidth of the cell is very low. For a narrowband application, it would be possible to simply resonate out the $C_{gs(be)}$ of the second transistor using a parallel inductor as indicated in the reactively matched PA section. This solution is not sufficient for the bandwidth of DPAs, however.

Narendra et al. (2010) proposed a wideband PA topology based on a cascaded gain-cell distributed approach that is featured by vectorially combined current sources. Each section of the work was composed of two non-identical high-f_T, cascaded to the power transistor by means of an inter-stage tapered impedance. Three sections were cascaded in their design. Using three cascaded-stages help to improve gain level up to 37dB. Authors of the paper use load-pull technique to determine optimum load impedance of the output power transistors.

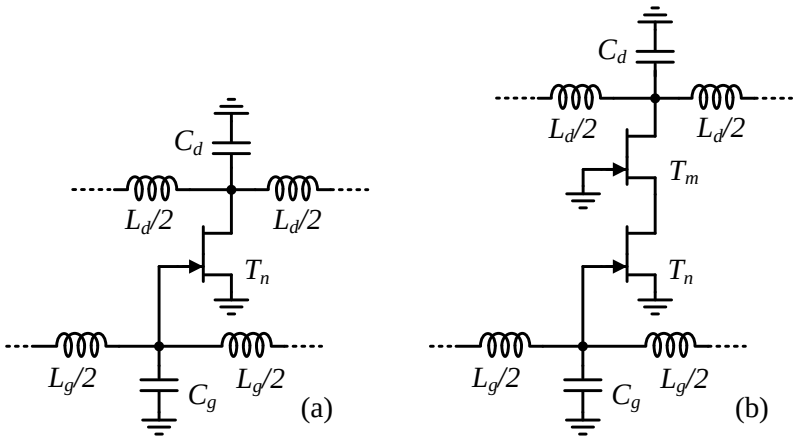


Figure 3.13 : Basic gain-cells for DPA (a) conventional common-source (b)Cascoded version

Moreover, their design makes use of tapered-line design approach to ensure there is not any backward propagation from the each device and so that this makes the design more difficult with the identical output power devices. As a result, it is not surprising

to obtain PAE degradation as the frequency is increased. One another drawback of a such non-terminated distributed approach is the lower impedance level at the output which is needed to be transformed into the reference impedance level (i.e. 50Ω) with the use of wideband impedance transformer which is another design difficulty for most cases (e.g. it is 12Ω to 50Ω transformer problem in the paper).

In conclusion, for the DPAs, there are many proposed and implemented DPAs to improve conventional case. A summarizing table is given in Table 3.7 to compare different DPA implementations.

3.3 Chapter Conclusions

In this section, in the first place, we introduced some of the silicon (SiGe HBT, LDMOS) and III–V compound based device technologies (GaAs, GaN (P)HEMT, SiC MESFET), which have potentials for mid-to-high power and wide bandwidth applications. Despite the fact that SiGe HBT is the most cost-effective solution, it suffers from the low-to-mid output power and high-loss of Si-substrate (i.e. low-efficiency) in the microwave frequencies, which complicates the MMIC based design strategies in the wideband and high-power range. LDMOS is an alternating silicon technology to improve the power density. Nevertheless, the problem now arises with the low bandwidth of operation.

With the help of very high electron mobility and thanks to 2-DEG of (P)HEMT technology; GaAs based devices work very well to design very wide bandwidth amplifiers and low-loss substrate is a plus to design with MMIC design. However, the power densities are limited since GaAs is unfortunately a narrow-gap device related to other III–V based device technologies and for that reason, the breakdown voltage is insufficient to boost the power much more. In addition to these, its thermal conductivity is almost the worst among the all other technologies. Of course, the cost of the device fabrication and other production-based problems are still challenging. Bandgap engineering helps to boost power densities with the help of wide band gap GaN HEMT and SiC MESFET devices, which are feasible to fabricate on the high thermal conductive substrates like SiC and Diamond.

Table 3.7 : Some of the previously proposed distributed wideband PAs.

Reference	Technology (Vendor)	Implementation	Die Size (mm^2)	BW (GHz)	BW (%)	P_{out} (dBm)	Gain (dB)	PAE (%)
Thein et al, (2012)	GaAs HBT	MMIC	1.8	2.5 – 6	82	28.5	~7	33 – 43
Narendra et al, (2012)	GaN (Cree)	Discrete	-	0.04 – 2	198	43	~37	32 – 56
Xu et al, (2011)	GaAs HBT	MMIC	1.0	1 – 12	169	14	8.1±0.5	<22
Sewiolo et al, (2009)	0.25µm SiGe HBT	IC Cascoded	1.16	DC – 12	200	14	9±0.5	6.5 – 9.5
Ciccognani et al, (2009)	0.25µm GaAs PHEMT	MMIC	5×4.5	2 – 8	120	<35	18±2	<27
Teiksiew et al, (2006)	MOSFET	Discrete	-	0.1 – 0.6	143	30	~13	<26
Eccleston (2005)	FET	Discrete (Dual-fed)	-	1.4 – 1.9	30	16 – 23	11±4	15 – 35
Zhao et al, (2003)	GaAs PHEMT	MMIC	-	0.8 – 2.1	90	~30	~11	>37
Duperrier et al, (2001)	0.25µm GaAs PHEMT	Hybrid LTTC	-	4 – 19	130	~30	**~7**	<20
Green et al, (2001)	GaN HEMT	MMIC	2.5×1.4	DC – 8	200	~35.7	~14	<23
Sayginer et al, (2011b)	**0.35µm SiGe HBT**	**IC**	**1.0×1.3**	**0.2 – 2.2**	**167**	**13 – 16**	**7.5±1**	**11 – 35**
Sayginer et al, (2011b)	**0.35µm SiGe HBT**	**IC**	**1.8×2.3**	**0.2 – 2.2**	**167**	**17 – 20**	**22±3**	**10 – 30**
Sayginer et al, (2013)	**0.25µm GaAs PHEMT**	**MMIC**	**1.3×2.9**	**1 – 8**	**156**	**25 – 28**	**~9**	**27 – 45**
Sayginer et al, (Submittion)	**0.25µm GaAs PHEMT**	**MMIC**	**3.4×1.4**	**1.5 – 9**	**143**	**28 – 29**	**15±1**	**36 –39**

High electron transportation and high breakdown field in GaN devices compared to other technologies, enables the realization of high voltage, high power and high frequency transistors, which help to design efficient high-power and wideband designs in the wide application range. The most challenging task for the wide band gap devices is still the cost of fabrication and yield of the feasible devices.

To summarize and compare visually the device technologies, Figure 3.14 is given to show the application based power-frequency usage map of the given technologies.

In the second place of the section, we have introduced the basic design topologies for wideband PAs that are classified mainly into the four sub-categories, which are

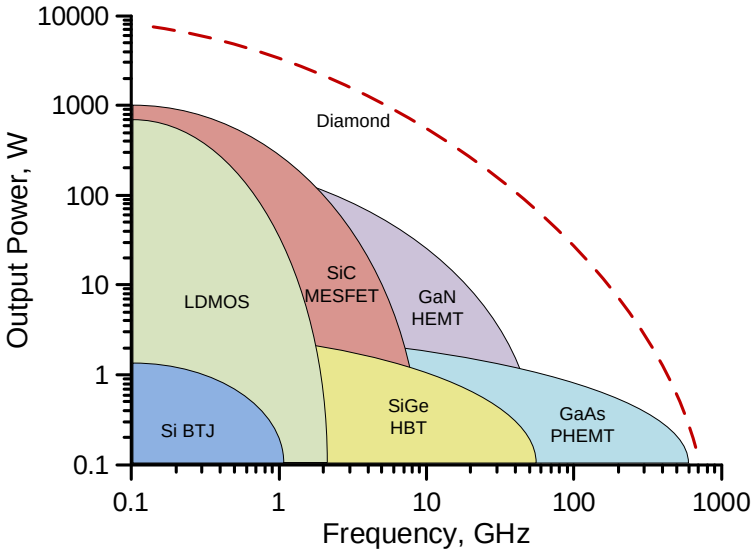


Figure 3.14 : A simplified and application based power-frequency map of different device technologies.

Resistive/reactive feedback PAs, Reactively-matched PAs, Lossy-matched PAs and Distributed PAs. From the design point of view, basic pros and cons of all classes are summarized in which the DPAs have been focused more. Feedback PAs were shown to realize a flat gain response and improved matching characteristics in a less complex and stable circuitry. However, power performance and hence the PAE is to degrade due to the resistive element used in the feedback path, which make the feedback designs less preferable especially when designing high-power PA.

Reactively matched amplifiers are shown as the another option to design wideband PAs. Due to the resonance behavior of this topology, wideband designs are getting more complicated and analytical solutions for the nonlinear input and output impedances are hard to realize. Moreover, the gain-bandwidth product of reactively

matched amplifiers is limited by the shunt capacitance of the active device. This limitation can be overcome with distributed amplifier topology.

As it was depicted that, the DPA is one of the most suitable and preferred circuit implementation to obtain wideband power amplifier. There are many different types of DPA topologies, proposed in the literature. The most fundamental drawback of DPAs is the low-efficiency problem. A typical frequency response of the distributed amplifier with respect to the lumped (e.g. the amplifier topologies which are not used the distributed concept) and tuned amplifier is given in Figure 3.15. As it can be observed in the figure, the advantage of using distributed concept is the available in the frequency band which is more than the lumped concept and it is possible to operate up to maximum oscillation frequency where the lumped configurations can only gain up to transient frequency of the given device.

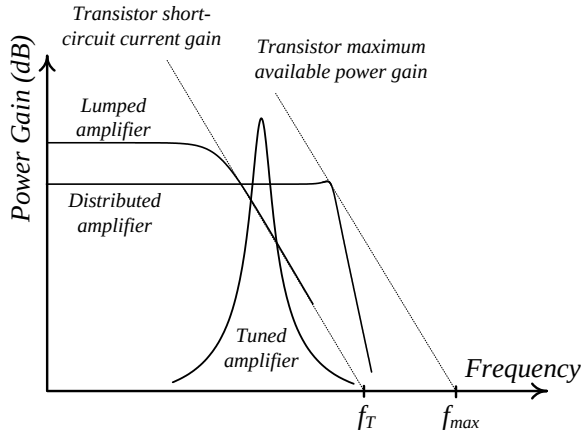


Figure 3.15 : Typical frequency response of distributed amplifier with respect to the Lumped and tuned amplifiers.

4. DESIGN OF SINGLE TRANSISTOR AND CASCADED TWPAs

The aim of this chapter is to propose some of the design techniques and systematics to implement wideband PAs with using simple design topologies based on the DPA. In the first phase of the chapter, SiGe HBT technology is used to design and realize wideband PAs in the single transistor and cascaded-paralleled case. In the second phase, GaAs PHEMT technology will be the base of the two proposed designs, which are employing a graphical load-pull technique and a systematic design approach.

4.1 Aim of the Designs and Planned Contributions

From now on, we will try to enhance the topological simplicity of the wideband PAs where the core circuitry is the single transistor DPA topology, which has the efficiency advantage over the multi-transistors case. A relatively low output power due to the reduced number of transistor could be doubled by removing the output-line terminating impedance/resistance. PA bandwidth could be widened with the help of series-series feedback and gain flatness could be improved with the help of lossy input ATL. Besides that, power combining with using parallel design cores will be also shown to be useful for preserving the bandwidth. Moreover, a new technique to relax matching problem will be presented, which uses a graphical design approach to guarantee a selected level of power would be delivered. In addition to these contributions, a systematic design for the cascaded version of single transistor core will be presented, which proposes a simple and straightforward design flow.

4.2 Load-line Design of SSTWPA and CSSTWPA using 0.35µm SiGe HBT

As it was noticed before that, wideband power amplifiers are typically implemented with using the travelling wave concept where the inherent input and output parasitic capacitances of the transistor forms ATL together with the external inductive structures. The cut-off frequency of a TWPA circuit is determined by the cut-off

frequency of the ATLs. From the ATL design point of view, three types of ATL sub-sections can be defined which are namely: L-type, T-type and π-type shown in Figure 4.1. As frequency approaches the cut-off frequency (f_c) of an artificial-line, the characteristic impedance of T-type section decreases, where π-type-section characteristic impedance increases. Since the line termination is required to avoid any reflection, typical ATLs obtained in TWPAs are employed using T-type topology where the termination impedance could be attached easily without disturbing the matching condition at the termination node.

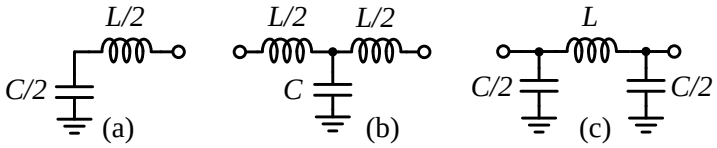


Figure 4.1 : Artificial transmission-line sub-sections: (a) L-type (b) T-type (c) π-type

However, for the circuit analysis purpose, the π-type approach is more convenient and necessary due to the capacitive behavior of the input and output terminals of the active device. ATL sub-sections given in Figure 4.1 behave like low-pass filter and corresponding Z_0 characteristic impedance and the f_c cut-off frequency for a limited number of cascaded sections could be given in (4.1) and (4.2) respectively.

$$Z_0 \cong \sqrt{\frac{L}{C}} \tag{4.1}$$

$$f_c \cong \frac{1}{\pi\sqrt{LC}} \tag{4.2}$$

A simplified ac equivalent circuit model representing the SiGe HBT transistor, shown in Figure 4.2, is preferred for the basic small-signal analysis of TWPA.

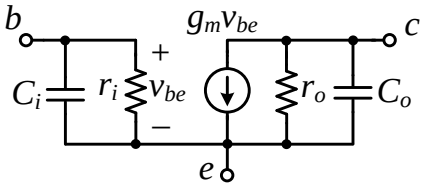


Figure 4.2 : Simplified small-signal SiGe HBT active device model.

This model includes input (C_i) and output (C_o) parasitic capacitances, input shunt resistance (r_i) and output resistance (r_o). In the classical design approach, both the capacitances form ATLs with the externally attached inductive components. The magnitude of the active device's intrinsic resistive element has a significant effect on the performance of the ATLs. Although this simplified model cannot predict the device behavior completely, it provides an understanding of the amplifiers behavior and operation.

A single transistor case of the TWPA, which is referred to as single-stage travelling wave power amplifier (SSTWPA) is shown conceptually in Figure 4.3 where it uses SiGe HBT as the active device. SSTWPA consists of an input and output ATL constituted from transistor's input/output capacitance. Although the TWPA concept uses multiple devices together, a single transistor case with using terminated input and output ATLs still differ the SSTWPA from a regular wideband PA by definition.

An input signal propagates through the input ATL and stimulates active device. Output signal of the stimulated active device is divided into two and one goes to output and the other goes to the termination impedance $Z_{T,c}$.

The magnitude of the low-frequency gain for the SSTWPA can be calculated from the small-signal representation as,

$$|A_0| = g_m \left(\frac{Z_0}{2} // r_o \right) \qquad \textbf{(4.3)}$$

Coming from this basic information and using the base-topology of the SSTWPA, we can improve the performance of the structure with making some modification on the circuit.

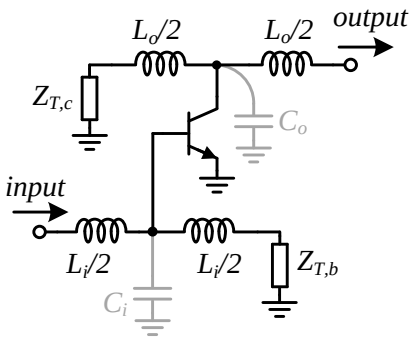


Figure 4.3 : Basic SSTWPA topology.

With using a lossy-ATL at the input would improve the amplifier's operational bandwidth, gain-flatness and matching performance (Virdee et al, 2007). Wider bandwidth can be realized by lowering the transistor's input capacitance C_i as it was in (4.2). The magnitude of C_i can be reduced by using an emitter degeneration resistor (i.e. series-series feedback) at the emitter terminal of the transistor (Yazgi et al, 2010). This effectively reduces the transistor's input capacitance due to the Miller Effect. Although this modification sacrifices the amplifier's gain performance, however it enhances the bandwidth. Additionally, extra line sections in the input of an SSTWPA can improve gain-frequency behavior.

The main obstacles in the design of silicon-based DAs are the low quality factors of on-chip spiral inductors and transmission lines which reduces gain and efficiency (Lee et al, 2003). Hereby, SSTWPA output network was designed for optimum power matching which entailed removing the output ATL termination impedance (Sayginer et al, 2011). Although this modification reduces the output reflection performance, it improves the amplifier's output power and power-added efficiency performance significantly. Thus, power gain, output power and power-added efficiency performances is doubled. Hence, it can be deduced that the modified SSTWPA circuit is a convenient structure for power applications. The circuit schematic of the modified SSTWPA, excluding the dc biasing and emitter degeneration resistor, is shown in Figure 4.4.

Although the output matching performance (usually characterized by S_{22}) is expected to deteriorate after this modification, this negative effect may be minimized by keeping the value of the load impedance close to 50Ω.

At the input ATL, design equation for the line-capacitance, C is,

$$C \cong C_{in} \qquad \textbf{(4.4)}$$

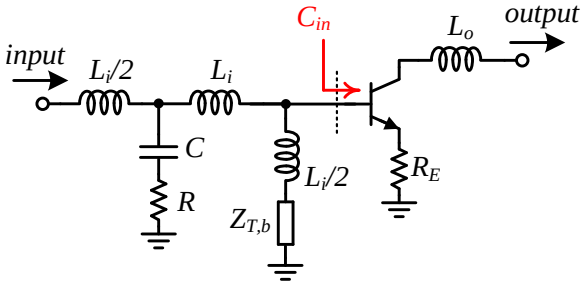


Figure 4.4 : Modified SSTWPA schematic.

while the line-inductance is calculated to provide characteristic impedance value of Z_0,

$$L_i = Z_0^2 C_{in} \quad \textbf{(4.5)}$$

Inductance value at the output is determined by optimum load line of the active device (Z_{opt}) and can be given by

$$L_o = Z_{opt}^2 C_o \quad \textbf{(4.6)}$$

In this equation, Z_{opt} is obtained from maximum voltage and current swings. If Z_{opt} is not equal 50Ω, a wideband impedance matching structure or a transformer at the output of the circuit may increase the power performance. The expressions given so far can be used in the first design step. After the basic design is completed, CAD tools and optimization steps can provide some improvements on the circuit performance.

4.2.1 Realization of SiGe SSTWPA

An SSTWPA circuit is designed according to the previous discussion. The aim of the design is to maximize power performance over the amplifiers widest possible operating frequency bandwidth. AMS 0.35μm SiGe HBT technology is used to design and realize the PA circuit. An NPN type transistor, NPN245h5, was used because of its full compatibility with CMOS technology and complex high-speed system-level integration as well for its high operational frequency.

The first step of the design process involves determining suitable transistor dimensions and the bias point. Thus, a transistor employing process maximum 96μm emitter-length was determined as the best choice for power output. For this device, I_C=34mA and V_{CE}=3.3V were obtained as the optimum bias point.

In the second step, the chosen transistor was investigated for its suitability for SSTWPA application. Its input and output parasitic capacitances, input resistance, output resistance and gain variations were studied. It was observed that the bandwidth performance of the chosen dimension was limited to around 1GHz due to its high input capacitance which was around 5pF. To tackle this problem, an emitter degeneration resistor (R_E=7Ω) was employed. In this way, owing to the Miller effect,

the value of the equivalent input capacitance decreased to around 1.2pF. Although this modification resulted in the sacrificing the amplifier's gain performance, it realized a wider bandwidth.

At the output, for a maximum voltage swing of 1.8V which is extracted from the output dc characterizing, the optimum load line is obtained to be approximately 50Ω. With the output C_o capacitance of around 0.5pF, using the equation (4.6), we can find the output inductance as 1.25nH.

The SSTWPA was designed based on the expressions given above. Unfortunately, the design resulted in S_{22} exceeding above 0dB in a small region of the frequency response. This meant that the circuit designed to have an input line with characteristic impedance of 50Ω was unstable. This problem was resolved by decreasing the characteristic impedance of the input line. However, this was at the expense of the input mismatch, which was around 30Ω. For the input line inductance, L_i can be calculated using equation (4.1) as 1.1nH. Predetermined values of the circuit elements are given in Table 4.1. After determining the values of the elements, the performance of the circuit was optimized using Cadence Design Environment and the SSTWPA chip layout is shown in Figure 4.5.

Table 4.1 : Element values of SSTWPA shown in Figure 4.4.

Element	Value
L_i	1.1nH
C	1.2pF
R	5Ω
$Z_{T,b}$	30Ω
R_E	7Ω
L_o	1.25nH

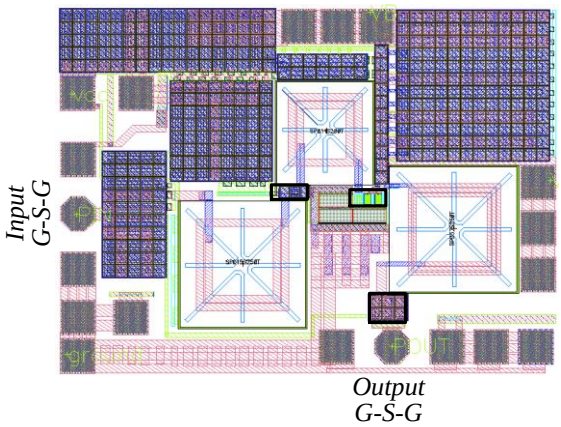


Figure 4.5 : Layout of the SSDA circuit.

4.2.2 Measurement Results for SiGe SSTWPA

The SSTWPA topology was realized with AMS 0.35µm SiGe HBT process. Fabricated chip die photo is given in Figure 4.6. Bare die size is 1.3×1mm^2. The dc biasing circuits are off the chip components and their parasitic effects are included in the simulations. Bare die chip was attached into an open-pack QFN16 package which is mounted on a FR4 PCB test board given in Figure 4.7. Ground-Signal-Ground (GSG) type probes and probe station were used to measure the input and output signals directly from the die chip. The SSTWPA was operated in class-A with a bias voltage of 3.3V and the collector dc current of 34mA.

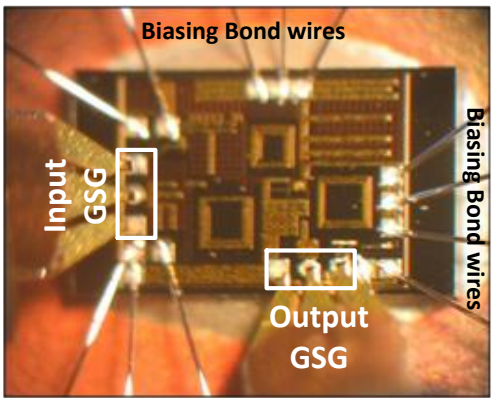


Figure 4.6 : Die chip photograph of the SSTWPA (1.3×1mm^2).

The simulated and measured small-signal s-parameters and group delay performance of the SSTWPA circuit are given in Figure 4.8 and Figure 4.9, respectively. The results confirm that the input ATL improves S_{11} performance within the desired frequency bandwidth. The average gain of the circuit was around 7dB and drops under 5dB beyond the 2.5GHz band. As expected from the conceptual point of view that S_{22} performance is sacrificed to improve output power performance of the

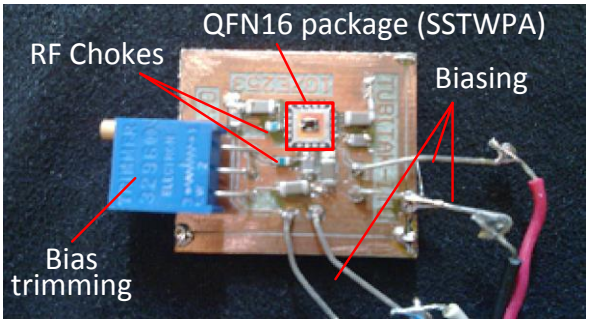


Figure 4.7 : Test fixture for the SSTWPA.

amplifier. It is not in the figures but s_{12} performance is also good and the the magnitude is under -45dB inside the band. Measured group delay performance is also agree with the simulations.

Over the same frequency span, the output 1dB compression point power level (P_{o1dB}) and power-added efficiency (PAE) are shown in Figure 4.10 and Figure 4.11, respectively for both the simulation and measurements.

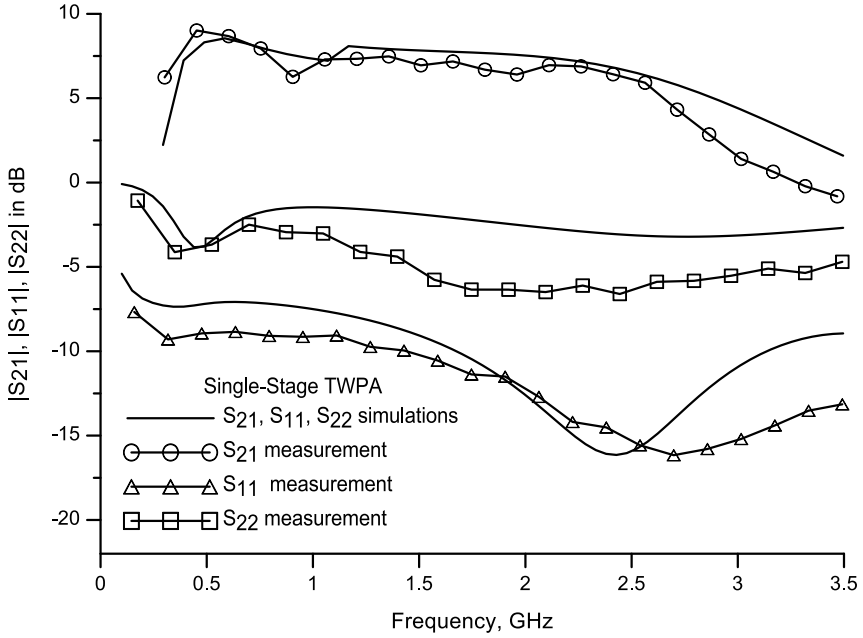


Figure 4.8 : Simulated and measured small-signal s-parameters of the SSTWPA.

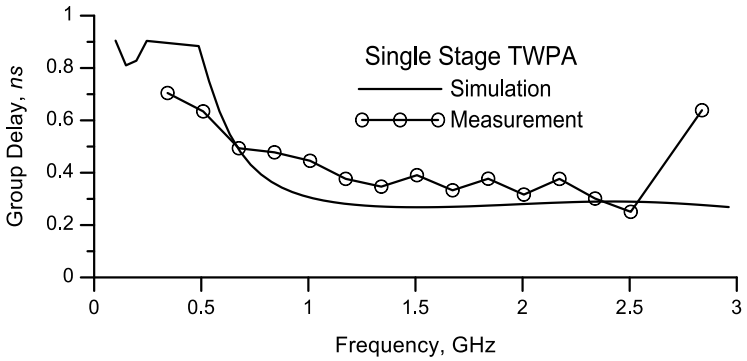


Figure 4.9 : Group delay performance of the SSTWPA.

Output power of >13.5dBm was obtained in the desired frequency band of 0.2-2.2 GHz, and PAE decreases with increasing frequency, where it is around 30% at the lower end of the frequency band and drops to a level of ~10% around 2.5GHz. This is caused mostly by the relatively high loss of the silicon substrate, which reduces the power and efficiency performance of the PA circuit used for wideband operation. The transistor was operated in class-A with a bias voltage of 3.3V and amplifier

absorbed a current of 34mA. The results confirm the input ATL improved S_{11} performance within the desired frequency bandwidth. The average gain of the circuit was around 7dB and drops under 5dB beyond the 2.5GHz band. As expected from the conceptual point of view, S_{22} performance is sacrificed to improve output power performance of the amplifier.

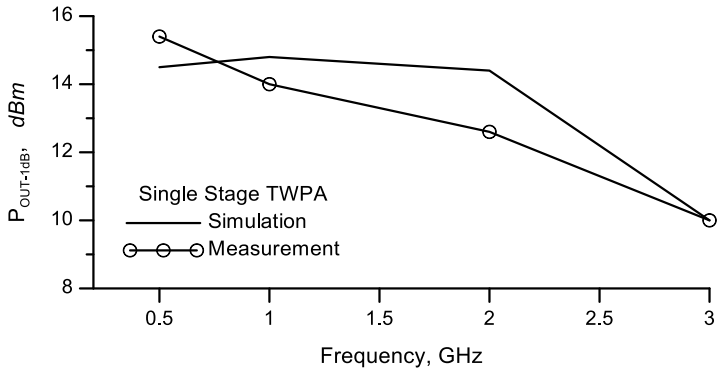


Figure 4.10 : Power performance of the SSTWPA.

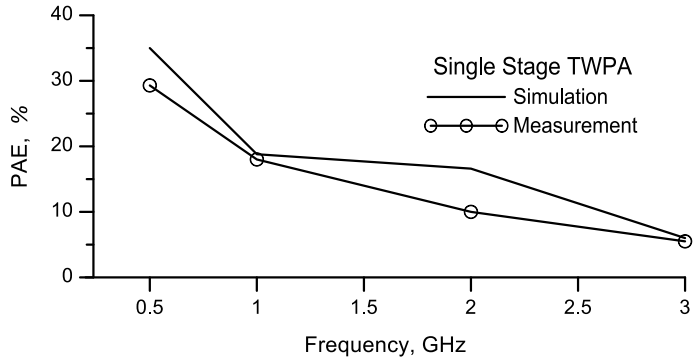


Figure 4.11 : Efficiency performance of the SSTWPA.

4.2.3 Cascading and paralleling SSTWPA cells for power doubling: CSSTWPA

To further increase the small-signal gain and the output power of the single-stage TWPA design, a unique topology is proposed as shown in Figure 4.12, which will be referred to as cascaded single-stage TWPA (CSSTWPA) (Sayginer et al, 2011b). This amplifier comprises of an input single-stage TWPA feeding two identical single-stage TWPAs in a parallel configuration whose outputs are combined together. This topology not only improves the gain but also doubles the output power. In the design, T_1 serves as the driver for the next stage by providing sufficient

power to the input of the output transistor T_2 and T_3 so that they operate up to their saturation power levels.

In a single-stage design, it is possible to double output power by using larger transistor size or directly paralleling the transistors. However, this increases the transistor's input and output capacitances, which diminishes the ATL cut-off frequency and hence the operational bandwidth.

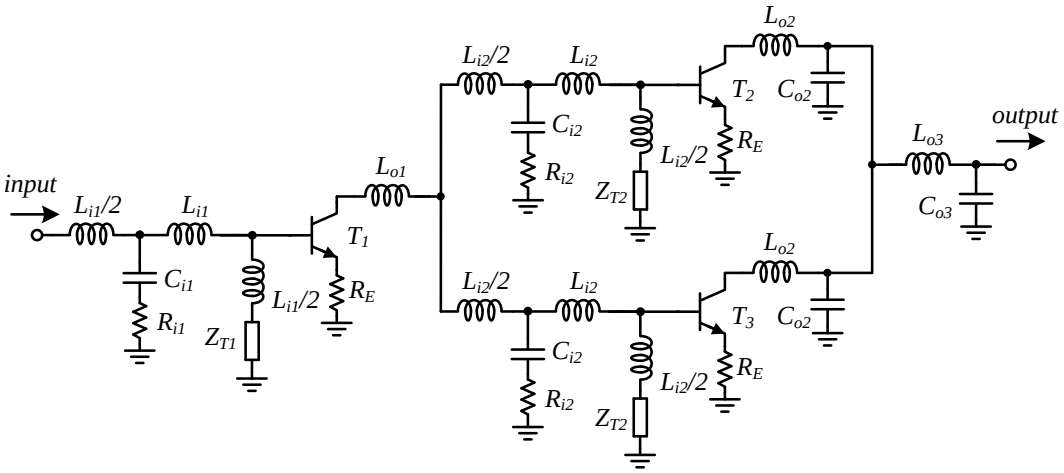


Figure 4.12 : Structure of the cascaded single-stage travelling wave power amplifier (CSSTWPA).

In the cascaded design depicted here, the overall bandwidth of the circuit is maintained as the SSTWPA shown in Figure 4.4 with the advantage of output power doubling which is equal to a 3dB improvement. It was found that the inner stage ATLs have no significant effect on the bandwidth performance of the TWPA.

From the topology given in Figure 4.12, at the input ATL, design equation for the line-capacitance, C_{i1};

$$C_{i1} \cong C_{in1} \tag{4.7}$$

could be selected. Line-inductance could be selected by providing a proper characteristic impedance of the input ATL which is also equal to termination impedance, Z_{T1}.

$$L_{i1} = Z_{T1}^2 C_{in1} \tag{4.8}$$

Inductance value at the output of the driver stage is determined by optimum load line of the active device (Z_{opt1}) and can be given by

$$L_{o1} = Z_{opt1}^2 C_{o1} \quad \textbf{(4.9)}$$

Since the first stage is driving the parallel two output stages, the input ATL of the both output stage should have the characteristic impedance of $2Z_{opt1}$ so that the parallel equivalent will have the same impedance level with the driver stage output impedance. Then the L_{i2} of the output stage is equal to,

$$L_{i2} = 4Z_{opt1}^2 C_{in2} \quad \textbf{(4.10)}$$

At the output, L_{o2} is calculated in a similar way with the (4.9). L_{o3} and C_{o3} simply used to matching purpose for the combined power at the output. Design values of the elements used in the implementation is given in Table 4.2. Figure 4.13 shows the implemented circuit layout of the CSSTWPA circuit drawn in Cadence Design Environment.

Table 4.2 : Element values of CSSTWPA circuit in Figure 4.12.

Element	Value
L_{i1}	1.1nH
C_{i1}	1.2pF
R_{i1}	5Ω
Z_{T1}	30Ω
R_E	7Ω
L_{o1}	1.25nH
L_{i2}	12nH
C_{i2}	1.2pF
R_{i2}	5Ω
Z_{T2}	98Ω
L_{o2}	1.25nH
C_{o2}	0.5pF
L_{o3}	0.9nH
C_{o3}	0.35pF

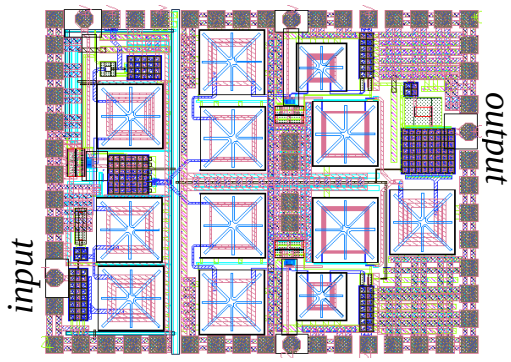


Figure 4.13 : Layout of the CSSTWPA circuit.

4.2.4 Measurement results for SiGe CSSTWPA

For the CSSTWPA circuit the s-parameter results are given in Figure 4.14. The driver and the output parallel structure comprising of single-stage amplifiers using identical transistors. In comparison to SSTWPA, small-signal gain $|S_{21}|$ is boosted to an average level of 22dB in the frequency band between 0.2 – 2.2GHz. S_{11} is almost <-10dB.

By using a matching network at the output, an effective load-line of 25Ω is matched to 50Ω. As a result, S_{22} performance is enhanced to be around -10dB. Group delay measurements also agree very well with the simulation results given in Figure 4.15. The average group delay is 0.6ns in the desired bandwidth.

As expected the P_{o1dB} is approximately 3dB higher than that of SSTWPA and the power level drops from 20dBm to 17dBm across the operation bandwidth from 0.2–2.2GHz, as seen in Figure 4.16. The CSSTWPA's PAE over this frequency range drops from 30% to 10%, as shown in Figure 4.17.

The high frequency discrepancy between simulations and the measurements of the PAE and P_{o1dB} of the CSSTWPA is thought to be the substrate loss of output power combining stage.

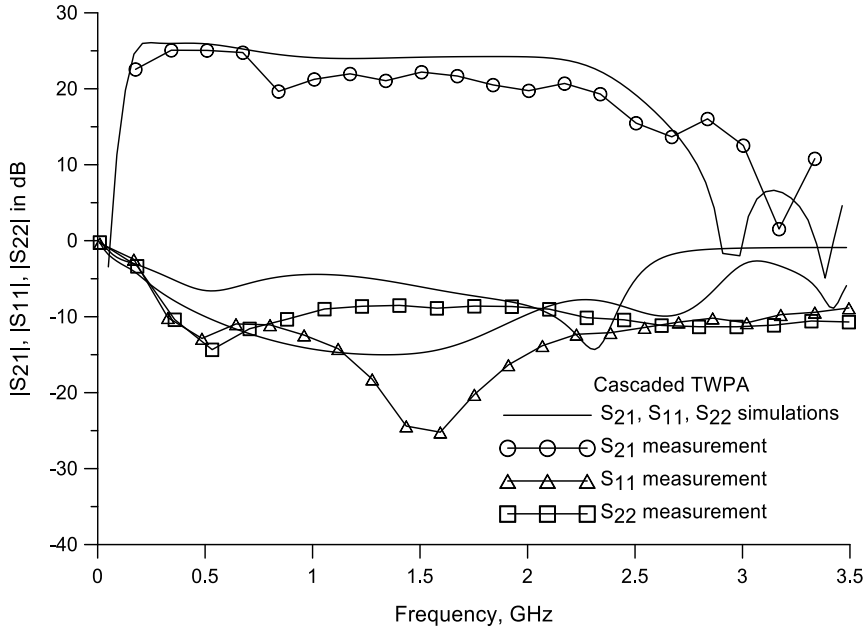


Figure 4.14 : Simulated and measured small-signal S-parameters of the CSSTWPA.

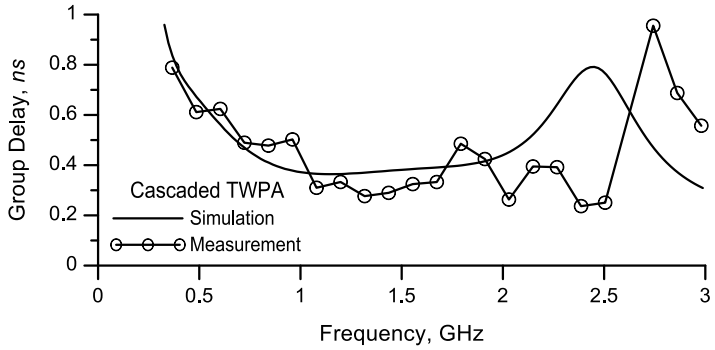


Figure 4.15 : Group delay performance of the CSSTWPA.

Overall dc power consumption for the CSSTWPA is around 330mW. As the above results indicate, no unstable operation is observed across the frequency band over which the measurements were performed. Sensitivity analyses were also performed during the design process to ensure reasonable flat gain response in the desired frequency band.

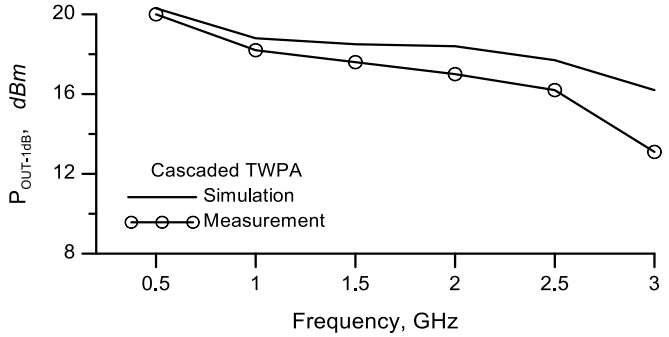


Figure 4.16 : Power performance of the CSSTWPA.

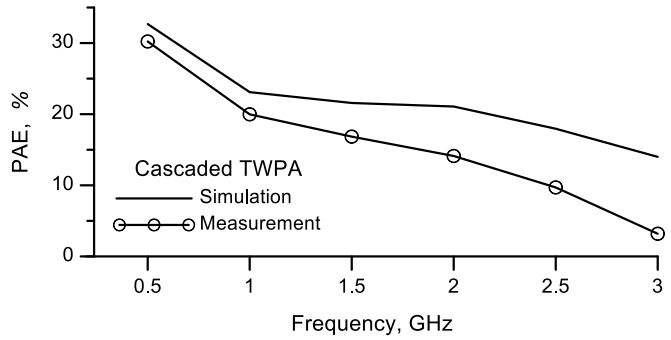


Figure 4.17 : Efficiency performance of the CSSTWPA.

CSSTWPA die chip photograph are shown in Figure 4.18. Only dc pads are bonded to outside open-pak QFN28 package, and modeled GSG RF probe pads are depicted at the input and output ports of the PA.

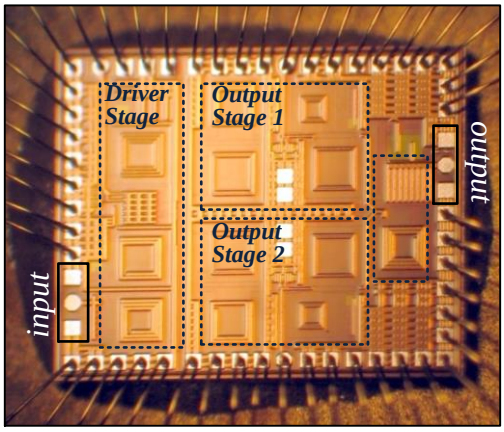


Figure 4.18 : Die chip photograph of the CSSTWPA (1.8×2.3mm^2).

CSSTWPA have the chip dimensions of 1.8×2.3mm^2. To reduce the feedback effect of ground bonding wire inductive effect, multi-pad ground bonding wires are used. The chip is attached in an open-pack QFN package and all the RF signals left inside the chip while dc supplies are fed with the help of a test board designed for all the testing and measurement purposed. Test board could be inspected in Figure 4.19.

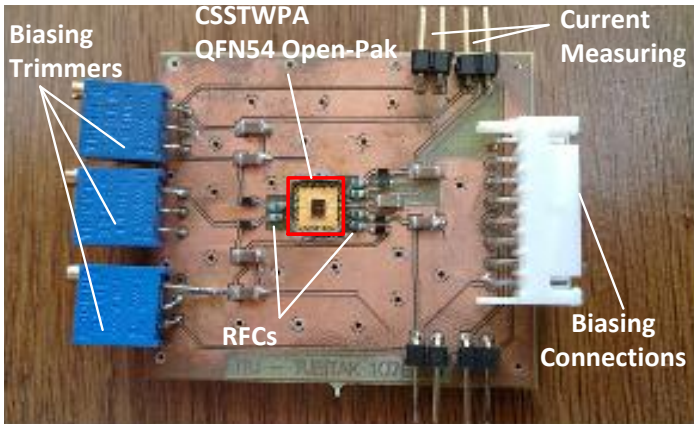


Figure 4.19 : CSSTWPA test board design.

4.3 Load-Pull Based Designs for Single Transistor and Cascaded TWPAs

In this sub-section, two different wideband PA operating in Class-A/AB are presented with using 0.25µm GaAs PHEMT MMIC technology from United Monolithic Semiconductor (UMS). One of the PA is a single transistor in which, capacitive coupling and frequency dependent lossy artificial-line are employed at the input of the active device. The proposed technique significantly enhances the amplifier's gain-bandwidth product, input match and gain flatness performance. To ensure the amplifier delivers a predefined power to the load over its entire operating band 2-to-8 GHz a broadband load-pull technique was applied at the output of the amplifier. To avoid reduction in the amplifier's bandwidth resulting from parasitic capacitive effects associated with the off-chip choke inductor, a wideband RF choke was also designed.

The second wideband PA is based on a systematic design approach. The overall amplifier structure comprises of two transistors in the cascaded topology. In the design, the first transistor is employed as a driver while the second is as a power transistor. The concept of the artificial transmission-line and capacitive coupling technique and wideband load-pull are employed in the cascade design in order to improve broadband amplification performance up to a decade bandwidth.

4.3.1 Wideband-matching with the help of load-pull design technique

Before starting the PA designs, it will be useful to review on the load-pull characterizing and matching of the wideband PAs. Extracting the source/load-pull characteristics of a device in the wideband and then applying matching networks both at the source and load side is the simple idea for the wideband design of PAs using source/load-pull techniques. As it was dedicted in the section: limitation on wideband matching, the main problem when designing such wideband-matching networks arises as the impedance-tracking problem of the matching network, which is ideally, must keep the track of source/load-pull impedance when the frequency is increased. Because of the power performance of the device depends on the nonlinear characteristics of the device, it is always hard to obtain convenient optimum load impedances for the given wide frequency range of operation. However simple

inspections can make simple predictions on the behavior of the device under test that the frequency response of the optimum output impedance generally rotates counter-clockwise direction on the smith-chart while the corresponding matching networks simply rotate clockwise direction in generally (Sechi and Bujatti, 2009).

Figure 4.20 shows a representation for a typical wideband load-pull characteristic of optimum load impedance, Z_{opt} and corresponding wideband-matching network impedance, Z_{IM}. As seen from the figure, there exist only two exact matching impedance points in the entire band of f_L to f_H.

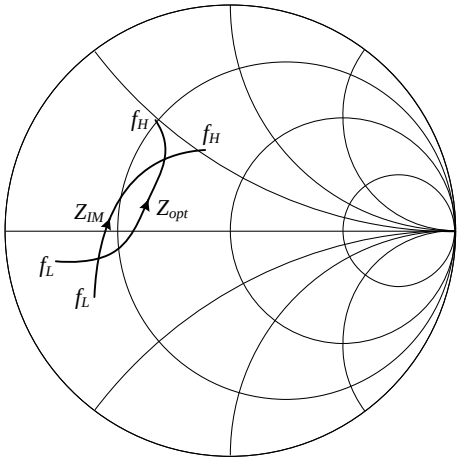


Figure 4.20 : Typical wideband load-pull characteristic of Z_{opt} and Z_{IM}.

4.3.2 Design of single-transistor TWPA using 0.25µm GaAs PHEMT

An improved version of SSTWPA design, that employs capacitive coupling and frequency dependent lossy artificial transmission-line at the input of the GaAs PHEMT was presented (Sayginer et al, 2013). A broadband load-pull technique is applied at the device's output to ensure the amplifier delivers predefined power to the load over the desired wideband operating range. The design procedure presented here is relatively simple to implement to realize amplifiers for wideband applications using just a single active device. The technique described improves the efficiency of the amplifier compared to conventional multistage and cascaded amplifier structures. Furthermore, the design time and overall fabrication cost are significantly reduced. A general and simplified topology of the SSTWPA circuit was depicted in Figure 4.3 which is also used as a base topology for the corresponding design given in Figure 4.21. Input signal propagates along the input ATL and stimulates the active device gate terminal. Z_T is the termination impedance of the input-line. The amplified signal

at the drain terminal propagated over the output ATL formed by the output capacitance of the FET device and the series output inductance, L_o.

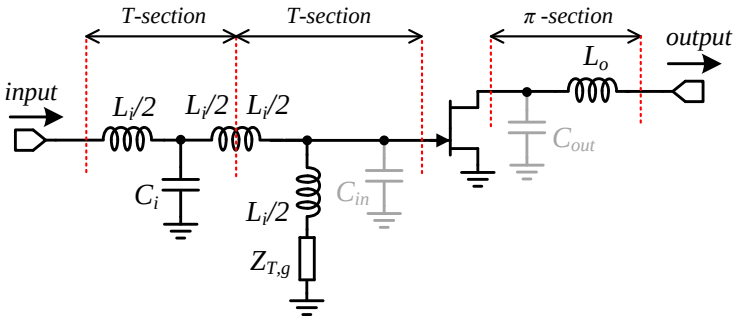


Figure 4.21 : GaAs PHEMT SSTWPA topology.

The simplified small-signal equivalent device model given in Figure 2.5b was used for the small-signal analysis of the PA. The input ATL in a TWPA is designed using T-type sections, which is terminated with impedance $Z_{T,g}$. Capacitance C_{in}, in Figure 4.21, is absorbed into the line and forms T-type sections with the external inductance $L_i/2$. Since ATL consists of replicated T- or π-type sections, the capacitance C_i is given by

$$C_i \cong C_{in} \tag{4.11}$$

Frequency response of the terminated ATL shows a low-pass filter behavior. For a lossless scenario the characteristic impedance and cut-off frequency of the input line are given as in in (4.1) and (4.2) respectively.

The gain-frequency performance of the amplifier can be improved with using frequency dependent lossy ATL sections at the input of the amplifier, which was used in the previous sections. As it was indicated, employing such lossy sections improves the input match and gain flatness, as well as ensuring stability of the amplifier by lowering the Q-factor of the line. Thus, this technique prevents resonance condition to initiate, which would otherwise force the amplifier to become unstable and oscillate.

In addition to this, a coupling capacitance C_c could also be added in series with the input gate terminal. This modification helps to increase the bandwidth of the amplifier by decreasing the effective capacitance of the input line (Ayasli et al, 1984b). However, the capacitive coupling technique reduces the amplifier's gain as

the voltage at the gate terminal is divided between the C_c and the C_{in} as represented in Figure 4.22.

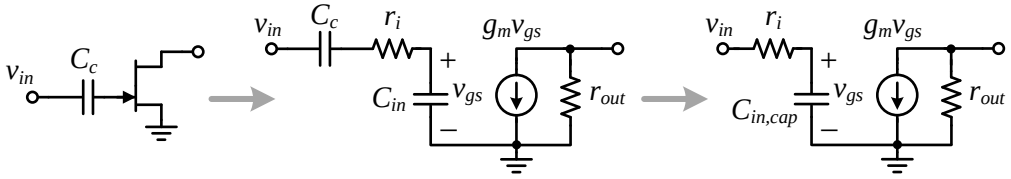


Figure 4.22 : A small-signal representation for capacitive division at the input.

By taking $\omega C_{gs} r_i << 1$, we can write the equivalent input capacitance, $C_{in,cap}$ and the voltage over the gate-source terminal, v_{gs} as below,

$$C_{in,cap} = \frac{C_{gs} C_c}{C_{gs} + C_c} \tag{4.12}$$

$$v_{gs} = \frac{C_c}{C_{gs} + C_c} v_{in} \tag{4.13}$$

By using the aforementioned technique and assuming the input-line to be lossless for simplicity, the expression for the line elements C_i, L_i and the loss element R_i are given by

$$C_i = \frac{C_{in} C_c}{C_{in} + C_c} \tag{4.14}$$

$$L_i = Z_{0,in}^2 C_i \tag{4.15}$$

$$R_i = r_{in} \tag{4.16}$$

The value of the inductance at the input line is calculated to provide characteristic impedance of $Z_{0,in}$. Resistance R_i is taken equal to the input r_{in} of the given device. The small-signal gain for the modified SSTWPA is given by

$$|A_o| \cong \left(\frac{C_c}{C_{in} + C_c} \right) g_m Z_{L,opt} \tag{4.17}$$

where $Z_{L,opt}$ is the optimum load impedance at the output. The above equations were used to design the input line of the SSTWPA. It should be noted that the circuit obtained may not provide the optimum performance because of the unaccounted

inherent parasitic effects. It is necessary to instigate optimization steps in order to improve the gain flatness performance of the SSTWPA in the desired frequency band of operation.

4.3.2.1 A Wideband-matching technique for optimum load contours

The most critical design issue of the SSTWPA is the determination of the output-line elements to obtain wideband matching. In the conventional SSTWPA design, an active device load-line characteristic determines the output inductance L_o (Yazgi et al, 2010). It's important to obtain the device's i_D-v_{DS} characteristics and determine the load-line to find the optimum output impedance (Cripps, 2006). Load-pull characterization across the amplifiers operation band is necessary to design the output stage. Load-pull characterization is followed by properly designing the matching circuitry at the output to track optimum impedances across the desired frequencies. However, the matching circuit design will be approximate as the optimum load impedance will not be unique as it changes with frequency. Load-pull characterization was done using the device's nonlinear model provided by the vendor. A load-pull set up is used to simulate and collect load-pull data shown in Figure 4.23 where the dc bias is fixed. The RFCs provide necessary isolation of the signal while biasing the active device. In addition, once the available input power and input reflection are known, the output power, transducer gain and power gain can be simulated or measured with any combination of load impedance.

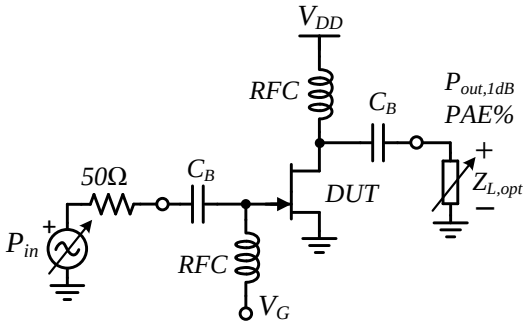


Figure 4.23 : Simulation set-up for load-pull characterization.

In the SSTWPA structure, output inductance value was determined by using wideband load-pull analysis instead of using load-line at the output. The SSTWPA output design equation could be approximated as

$$Z_{L,opt} \approx \sqrt{L_o / C_{out}} \qquad \textbf{(4.18)}$$

where the $Z_{L,opt}$ is the frequency dependent optimum output impedance seen from the device output. Since the optimum load values vary with frequency, it is impossible to track frequency depended optimum load impedances perfectly. That is to say a simple and accurate way of determining output L_o inductance is needed. Hence we have used an impedance tracking concept based on a graphical representation of the given load impedances. According to the technique, the process starts with collecting the optimum impedances for a predefined power level, which is less than the maximum one in the desired frequency band. As a result, optimum impedance points for the given power level constitute a closed-contour on the Smith-chart instead of a single impedance point corresponding to a maximum obtainable power at the output for a given specific frequency. The impedance is selected from inside the load contour to ensure predefined power is delivered to the load (Sayginer et al, 2011).

Figure 4.24 shows the representation of the power contours for the device under test. Given impedance data is gathered for different frequencies in the entire band where the reference power level is taken equal to 0.5W. It is noticeable that the optimum load contours rotates counter-clockwise direction on the Smith-chart with the increasing frequency and this fact is challenging when designing proper wideband-matching network since the tracking nature of the impedance matching networks are known to be rotating to clockwise direction when the frequency is increased.

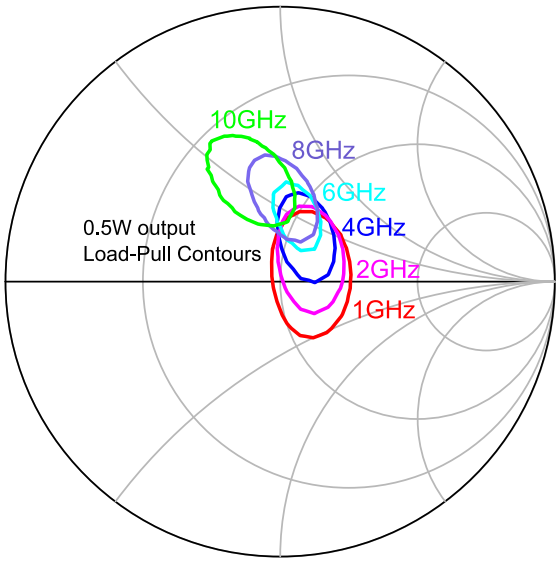


Figure 4.24 : Load-pull power contours of 0.5 W for DUT simulated across 1 to 10GHz.

4.3.2.2 Realization of GaAs PHEMT SSTWPA

The proposed SSTWPA circuit was designed according to the previous discussion. The main objective was to maximize the amplifier's power and efficiency performance over the widest possible frequency band. Overall circuit implemented is shown in Figure 4.25.

Design process starts with determining the transistor dimensions and choosing the convenient bias point. A single transistor having maximum channel width of 125μm and 12 fingers geometry was selected. Device was biased at I_D=140mA and V_{DS}=8V, which is the optimum bias condition for class-A/AB operation.

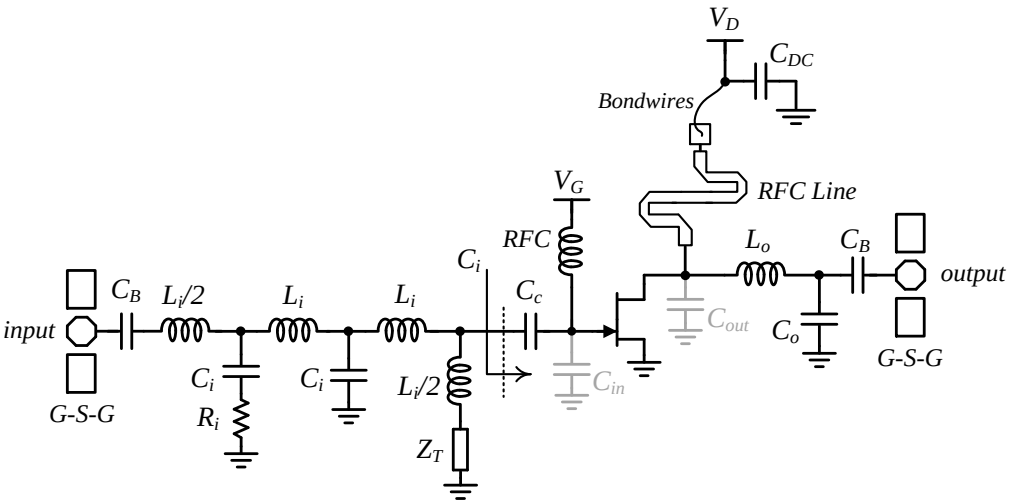


Figure 4.25 : Proposed SSTWPA circuit.

In the second step, the chosen transistor was investigated for its suitability for SSTWPA application. This involved studying the effects of its input/output parasitic capacitances, input resistance, output resistance and gain variations as a function of frequency. Simulated small-signal s-parameters for the device is given in Figure 4.26.

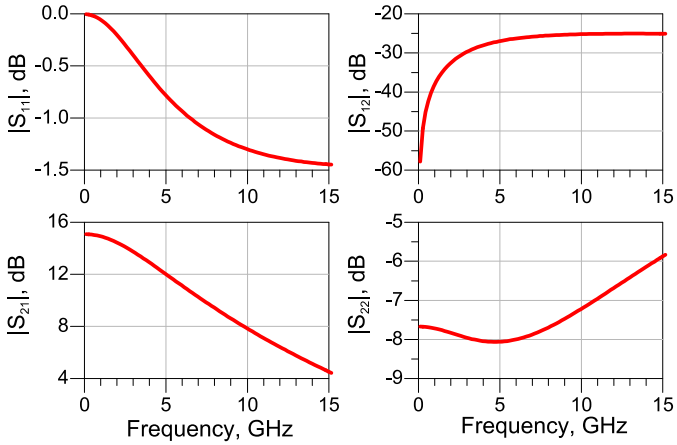


Figure 4.26 : Small-signal s-parameters of a 12×125µm GaAs PHEMT device biased at I_D=140mA and V_{DS}=8V.

The amplifier has an input characteristic impedance of 50Ω. A simple inspection according to the equation (4.1) and (4.2) can state that the bandwidth performance of the chosen transistor is limited to 2GHz due to its high input capacitance (C_{in}) of 3pF. To improve the bandwidth performance, capacitive coupling is employed at the input gate terminal of the device. In this way the equivalent input capacitance of the transistor is reduced to around 1 pF when an optimized value of C_c=2.1pF is used.It was found from simulation investigation that the input line has the best performance when $Zo_{,in}$≈40 Ω. Input line employs a lossy section to make use of lossy-line properties.

The magnitude of R_i is taken to be around 3Ω according to (4.16). Although these modifications sacrifice the amplifier's gain performance, it enables the realization of a much wider bandwidth from 1-to-8 GHz. The output-matching network comprising of the single inductive element (L_o) was determined using the load-pull technique. A non-dominant shunt capacitance C_o was used to optimize the amplifier's power performance. Impedance tracking performance shown in Figure 4.27 was used to determine the inductance L_o for the best matching condition. To achieve this, L_o was found to be 0.57nH.

According to the tracking profile, there still exist some impedance values outside the predefined 0.5W contours. These small mismatching conditions will possibly causes small degradations on the power performance of the SSTWPA. Predetermined values of the circuit elements are given in Table 4.3.

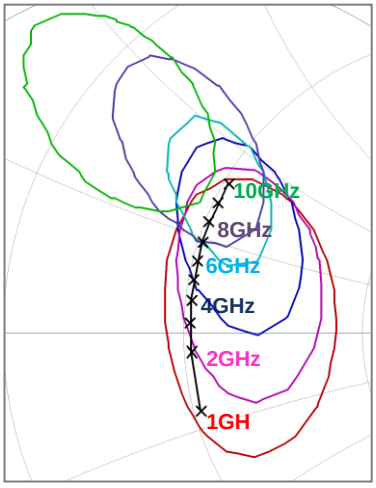


Figure 4.27 : Single inductance solution to the given matching problem.

Table 4.3 : Element values of SSTWPA circuit in Figure 4.12.

Element	Value
L_i	1.6nH
C_i	1pF
C_c	2.1pF
R_i	3Ω
Z_T	40Ω
L_o	0.57nH
C_o	0.2pF
C_B	8pF

An on chip inductive microstrip transmission-line was constructed to provide wideband RF choke for biasing purpose at the drain terminal of the active device, as shown in Figure 4.28. The RF choke line is based on a transmission-line shorted at one side, which is shown to behave like an inductance. By definition, any transmission line terminated with any arbitrary Z_L impedance at one end has the input impedance defined by

$$Z_{in,TL} = Z_0 \frac{Z_L + jZ_0 \tan(\beta d)}{Z_0 + jZ_L \tan(\beta d)} \qquad \textbf{(4.19)}$$

where Z_0 is the characteristic impedance of the line, β and d are the phase constant and the length of the line, respectively. By short circuiting one end of the line (Z_0= 0) one obtains an inductive impedance given by

$$Z_{in,TL} = jZ_0 \tan(\beta d) \qquad \textbf{(4.20)}$$

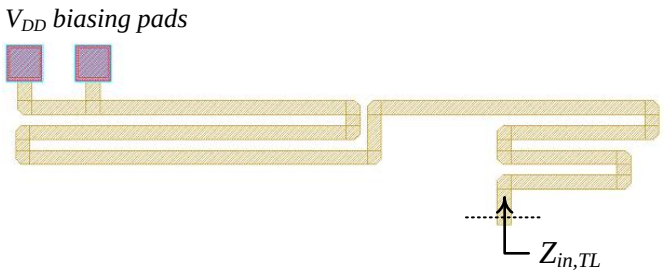
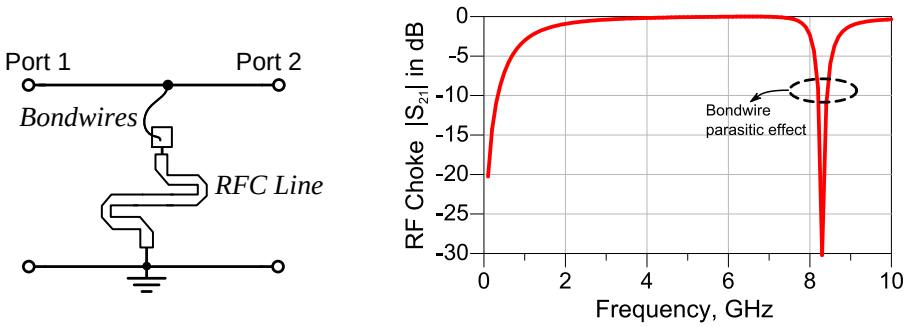


Figure 4.28 : Microstrip-line based RF choke structure.

This line was used as an RF choke by ensuring the magnitude of the frequency dependent $Z_0\tan(\beta d)$ term is sufficiently high across the operating band of the amplifier. Simulation setup for the proposed RF choke is shown in Figure 4.29a. Agilent's Advanced Design System (ADS) Momentum simulation tool was used to optimize the performance of the RF choke. The performance of the proposed RF choke structure is given in Figure 4.29b. The given microstrip line structure performs adequately well to stop RF signal leaking across the desired wideband while feeding the active device with dc bias. Parasitic effect of the bond wire at the biasing end of the RF choke is important as it can adversely affect the overall performance of the RF choke. It was found the length of the bond wire should be as short as possible to minimize resonance effects, which were observed around 8GHz as shown in Figure 4.29b. The finalized layout of the SSTWPA is shown in Figure 4.30.



(a) (b)

Figure 4.29 : (a) RF choke line simulation setup. (b) RF choke performance including the parasitic inductance effect of the bond wire.

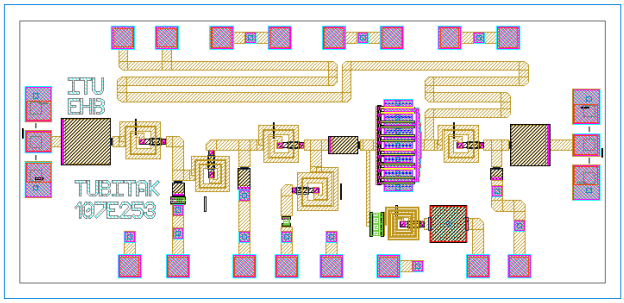


Figure 4.30 : Layout of the proposed GaAs SSTWPA.

4.3.2.3 Measurement Results for GaAs PHEMT SSTWPA

The proposed SSTWPA design was fabricated using UMS 0.25µm GaAs PHEMT MMIC process. The chip area is 1.31×2.93 mm^2 and die photograph is shown in Figure 4.31. The bare die chip is attached to an external printed circuit board via epoxy and using gold bond-wires. PCB is used for the dc bias supply. GSG type RF probes with 150µm pitch size are used with a manually controlled probe station. In the case of class A/AB operation, I_D and V_{DS} are set to 140mA and 8V, respectively. Both stability factor (K>1) and stability measure (B>0), in Figure 4.32, show the amplifier design to be stable across 1-to-10GHz.

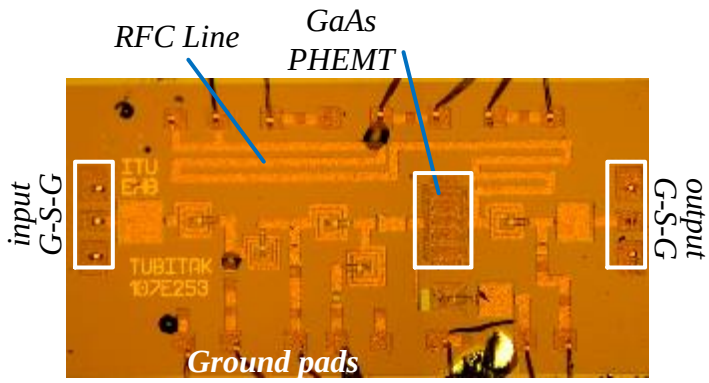


Figure 4.31 : Photograph of the fabricated SSTWPA chip (1.31×2.93 mm^2).

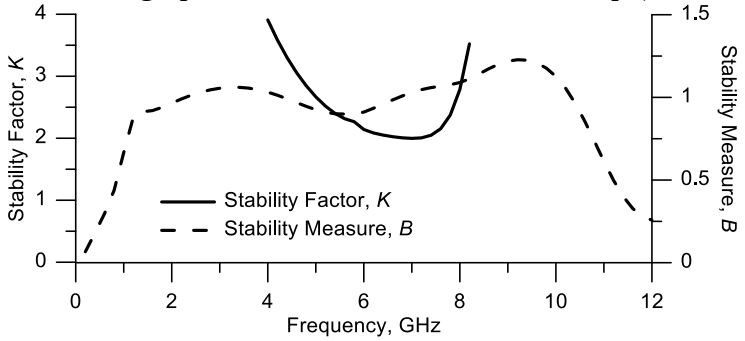
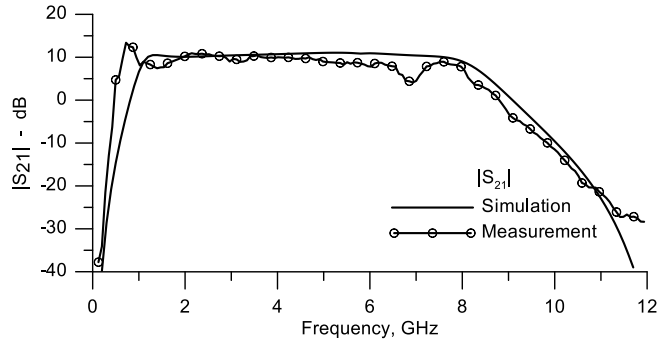


Figure 4.32 : Stability performance of the SSTWPA (K>1 and B>0).

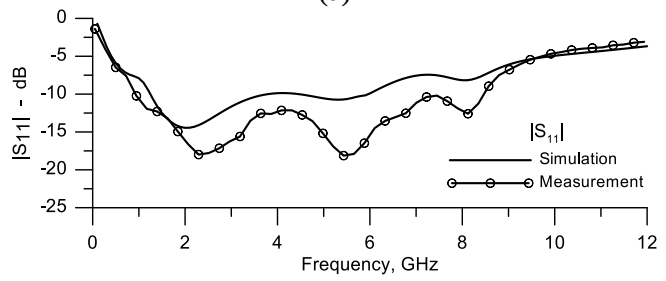
As seen from Figure 4.33(a), the SSTWPA exhibits an average gain of 9 dB over 1-to-8 GHz. Gain degradation around 7GHz is due to the bond-wire parasitic inductance which appears at lower frequencies according to the simulation results.

On the other hand, output matching performance of the circuit is not as good as the input match. Figure 4.33(c) shows s_{22} is around -5dB. In fact this is not surprising since the output wideband-matching network is optimized to improve the power performance, i.e. power matching via load-pull instead of a small-signal conjugate matching.

As seen from Figure 4.33(d), measurement and simulation performances of the reverse isolation of the amplifier give similar results (below -30dB). The group delay performance of the SSTWPA, given in Figure 4.34, was measured using a vector network analyser, and is in good agreement with the simulation results.



(a)



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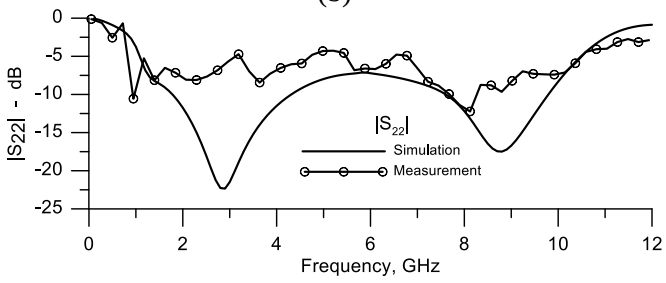
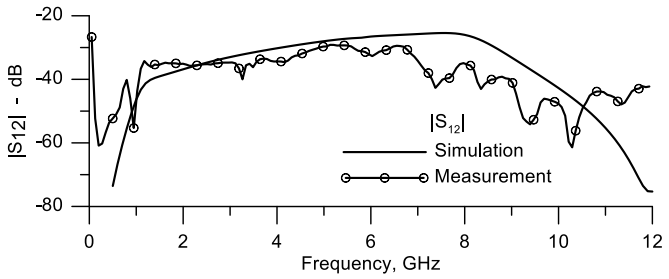


(c)



(d)

Figure 4.33 : Simulated and measured small-signal S-parameters of the SSTWPA, (a) Gain $|s_{21}|$, (b) input reflection coefficient $|s_{11}|$ (c) output reflection coefficient $|s_{22}|$, and (d) reverse isolation $|s_{12}|$.

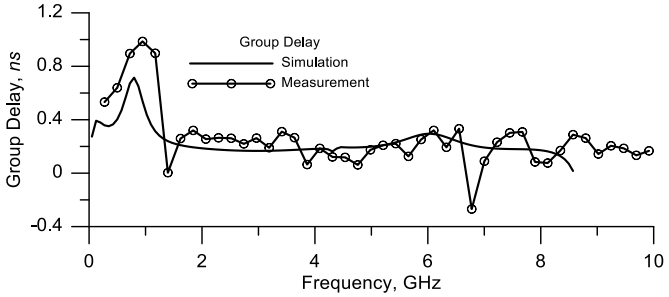


Figure 4.34 : Group delay performance of the SSTWPA.

Saturated output power (P_{sat}) and 1dB compression point power ($P_{out,1dB}$) were measured in the operating band. The amplifier's power-added efficiency (PAE) performance was also measured. These results are shown in Figure 4.35. The average values of $P_{out,1dB}$ measured is around 26dBm, and the P_{sat} level is approximately 29 dBm across the operating band of the amplifier. PAE values are between 27-43% and 48-76% for $P_{out,1dB}$ and P_{sat}, respectively. Mismatch between the simulation and measurement results are attributed to the unpredictable effects of the parasitic elements in the amplifier design.

In conclusion, the proposed structure demonstrated a technique to significantly enhance the performance of a wideband travelling wave power amplifier, which uses a single transistor operating in Class-A/AB. The single-stage travelling wave power amplifier (SSTWPA) comprised of capacitive coupling and frequency dependent

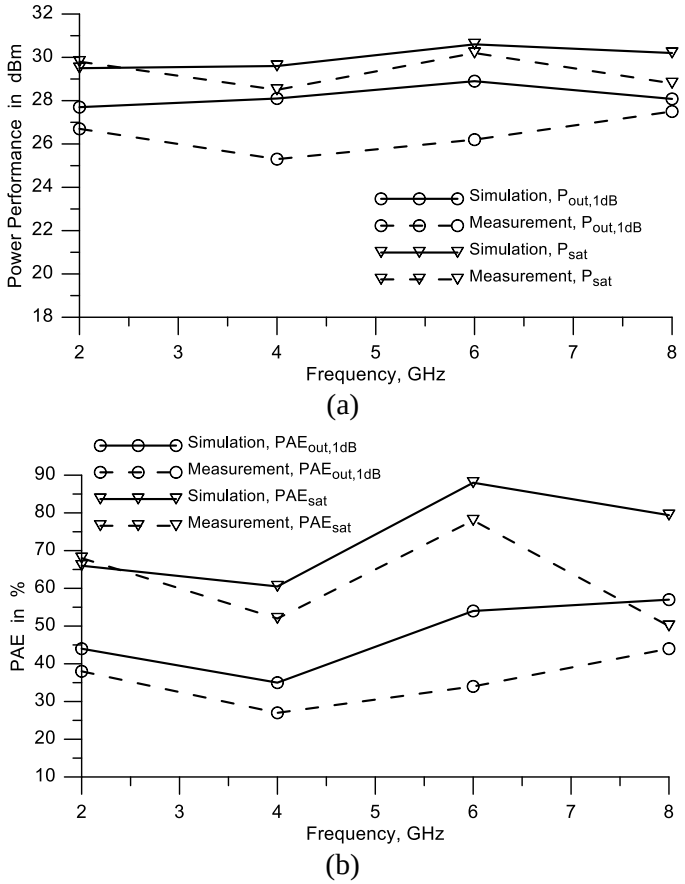


Figure 4.35 : (a) Saturated and 1 dB compression point power performance of the SSTWPA, and (b) PAE performances for the SSTWPA.

lossy artificial transmission-line to enhance the amplifier's frequency-bandwidth product, input matching and gain flatness response.

A broadband load-pull technique using a graphical design approach was used to ensure a predefined power level is delivered to the load over the amplifier's operating bandwidth. The parasitic capacitance associated with the off-chip RF choke degrades the bandwidth performance of the amplifier. To eradicate this problem an integrated microstrip line is implemented at the drain node, which is used as RF choke to operate over a wideband. The proposed SSTWPA was designed using 0.25μm GaAs PHEMT process. The fabricated amplifier provides a gain of approximately 8-10dB across 1-to-8GHz. The P_{sat} and $P_{out,1dB}$ of the amplifier have peak values of 1W (30dBm) and 0.6W (27.8dBm), and the corresponding PAE are above 48% and 27%, respectively. The proposed SSTWPA design provides wideband operation with gain flatness, optimized flat power performance and high efficiency in the desired band. Moreover, the single transistor design is relatively simple to implement, occupies less chip area and thus cost effective compared with the multi-stage version of TWPAs.

4.3.3 A systematic design of cascaded single-stage TWPA using 0.25µm GaAs PHEMTs

By cascading single-stage blocks, the gain could be boosted (Virdee et al, 2000; Banyamin and Berwick, 2000a) and as a result, efficiency could be improved for the same power level. Liang and Aitchison was compared the gain performance of a cascaded single stage TWA with the CTWA (1995a). Banyamin and Berwick was also analyzed the performance of a four-cascaded single-stage TWA (2000b). According to their works, since there is no need to match internal stage of the cascaded structure, overall gain can be boosted while conserving the bandwidth by taking the proper internal impedance and using optimization techniques. Moreover, Virdee presented a cascaded reactively terminated single-stage DA where the output power and efficiency of the design were improved with using large-signal impedance matching network (Virdee, 2001). In addition to these individual cascaded designs, Deng et al made a study to compare performance metrics of the different cascaded structures (2003).

Above the mentioned studies were generally concentrated on the design of cascaded DAs without making clear referring and comparison to the single stage version. Additionally, their design perspectives are focused mostly on gain-boosting of the overall amplifier in a wideband. However, there are not enough and certain design suggestions and straightforward systematic to improve the output power and the efficiency performances besides the small-signal gain-boosting.

From this perspective, a simple and systematic approach to design and realize a wideband power amplifier will be put forward in the cascaded topology. In this study, a two-stage design is shown to be sufficient to obtain a decade bandwidth, flat gain, high power and efficient with the reasonable chip size. In that case, the structure would be called as double stage travelling wave power amplifier (DSTWPA).

In the design of the proposed DSTWPA, we have gathered some of the previously used techniques where; frequency dependent lossy artificial transmission-line is used to improve input matching performance and capacitive coupling technique is applied to widen bandwidth. In addition to this small-signal techniques, the broadband large-signal load-pull approach used in the former section applied to determine ATL

elements at the output side and consequently, high output power with an improved efficiency is achieved.

Proposed DSTWPA is fabricated using 0.25um GaAs PHEMT MMIC process. The measurement results of the fabricated DSTWPA circuit are shown to agree with the theoretical and simulation results. The DSTWPA circuit performs high output power and efficiency performance with the flat and reasonable small-signal-gain level. All simulation and measurement results verify the effectiveness of the presented systematic design approach.

In comparison to a previously proposed single-stage case, proposed DSTWPA shows that the power performance could be increased and the efficiency could be boosted. That is to say that, it is possible to obtain a simple and systematic way of designing high performance cascaded wideband power amplifier with the presented methodology.

4.3.3.1 Systematic design of DSTWPA

An equivalent and simplified high-frequency small-signal circuit model representing the GaAs PHEMT transistor is shown again in Figure 4.36a. When the condition $\omega^2 C_i^2 r_i << 1$ is satisfied, it is possible to show that series of r_i and C_i could be transformed into the parallel equivalent circuit as in Figure 4.36b where g_i is now frequency dependent and its value equals to $\omega^2 C_i^2 r_i$. In the design of DSTWPA, we use the parallel equivalent model at the input of the transistor as long as the condition for the series-to-parallel transformation exists for the device.

This simple model, however, cannot predict the device behavior completely (e.g. large-signal behavior) but by investigating the variations of the parameters in the model versus frequency, it is possible to predict the gain-frequency performance of the DSTWPA.

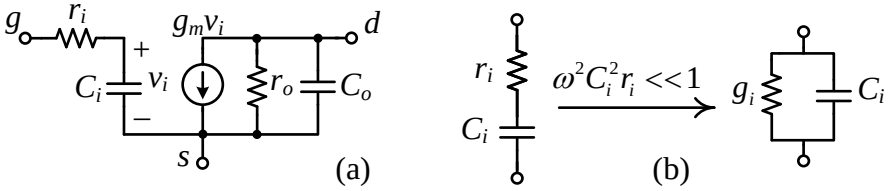


Figure 4.36 : (a) Simplified high-frequency ac model of the GaAs PHEMT. (b) Series-to-parallel transform to represent input of the transistor.

A step-by-step design flow will be presented here to obtain a complete cascaded amplifier. The design starts from the output stage with the help of load-pull analysis to determine optimum load impedances as well as the biasing conditions for the output power transistor. Afterwards, with using simple equations, both the inner stage characteristics and the driver stage (i.e. first stage transistor) biasing point will be determined. Finally, ATL inductor values will be determined according to the input ($C_{i1,2}$) and output ($C_{o1,2}$) parasitic capacitances of the active devices since the external inductive components form ATLs with the inherent parasitic capacitances.

4.3.3.2 Analysis and design of the output stage

In the first step, a large gate periphery output (power) transistor is examined using load-pull simulations. The aim of the load-pull analysis is not only to find out frequency dependent optimum load impedances ($Z_{L,opt}$), but also to find an optimum lower bound for the bias current ($I_{D2,opt}$) of the given transistor. When the load is taken as the optimum value for a given specific size of the device, this lower bound current of I_{D2} simply states that;

1) With the increasing biasing ($I_{D2}<I_{D2,opt}$), the level of 1dB compression power ($P_{o,1dB}$) at the output will also increase and then it becomes to saturate smoothly for $I_{D2}\geq I_{D2,opt}$. For $I_{D2}>>I_{D2,opt}$ device starts to output nearly the same $P_{o,1dB}$.[6] Note that the higher order nonlinearities and related metrics are not concerned in this wideband design.

2) Additionally, when the current is choosen as $I_{D2,opt}$, corresponding PAE would be expected higher than any $I_{D2}>>I_{D2,opt}$ condition since the bias current at that point is optimized to a lower boundary and still having the same $P_{o,1dB}$.

After I_{D2} is determined (i.e. $I_{D2,opt}$), the transconductance of the device (G_{m2}) can be simplified as,

$$G_{m2} = \sqrt{K_2 I_{D2}} \qquad \textbf{(4.21)}$$

[6] Reader should not confuse the "saturated $P_{o,1dB}$" and general "power saturation" terminologies. When saying saturated $P_{o,1dB}$ here, we mean that the level of $P_{o,1dB}$ starts to increase lower and lower with the increasing bias current. On the other hand, a well-known phenomenon, namely: "power saturation" is related to the compression of the output power beyond the 1dB compression with the increasing input power. In most cases, the reference compression level for saturation is taken as 3dB (i.e. one-half the power).

where the device is assumed to have quadratic *i-v* relation for simplicity and the parameter K_2 could be thought as the gain factor for the device. Now, we can write the magnitude of voltage gain for the output stage as,

$$|A_{v2}| = G_{m2}|Z_{L,opt}| \quad \textbf{(4.22)}$$

Since $Z_{L,opt}$ is frequency dependent, a wideband-matching network is essential at the output to match optimum load impedance into the standard 50Ω load. To prevent device from nonlinear operation (i.e. saturation), input gate voltage should be in the range, which guarantees to operate in the linear region. By referring the sinusoidal excitations, power delivered to the optimum-load can be written as,

$$P_{o2,1dB} \approx \frac{V_{o2,max}^2}{2|Z_{L,opt}|} \quad \textbf{(4.23)}$$

where $V_{o2,max}$ is the maximum voltage amplitude at the device output when 1dB power compression occurs. By using the gain relation in (4.22), maximum voltage amplitude ($V_{i2,max}$) at the device input can also be derived easily as in (4.24) and this voltage definition will be used in the next design step.

$$V_{i2,max} = \sqrt{\frac{2P_{o2,1dB}}{K_2 I_{D2}|Z_{L,opt}|}} \quad \textbf{(4.24)}$$

4.3.3.3 Analysis and design of the inner and input stage

Equation **(4.24)** states that for a proper non-saturated operation, there should be a limit for the level of the voltage at the input of the power device and this limitation can be determined by the power device parameter such as optimum load and biasing current characteristics. After the upper bound value of V_{i2} is determined, the next step of the design is to find another relation for V_{i2} using the inner and the driver stage parameters. Figure 4.37 gives a representation of two-stage cascade amplifier to clarify given design step description.

Since the overall design is a two-stage cascaded amplifier and the output is driven by the driver stage, we can conclude that V_{i2} is a function of both the driver stage current (I_{D1}) and the inner stage impedance level ($Z_{O,int}$).

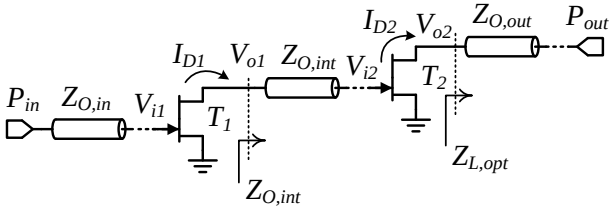


Figure 4.37 : Simplified two-stage design to determine design equations.

By using these definitions, we can get another design relation at first glance which gives a boundary condition determined for a non-saturated operation at the output:

$$V_{i2,max} \geq \left|Z_{O,int}\right| I_{D1} \tag{4.25}$$

By combining equation (4.24) and (4.25), we can complete the equation set for the stages, which gives the required conditions for the linear operation. Hence, the boundary condition for I_{D1} is found as,

$$I_{D1} \leq \frac{1}{\left|Z_{O,int}\right|}\sqrt{\frac{2P_{o,1dB}}{K_2 I_{D2}\left|Z_{L,opt}\right|}} \tag{4.26}$$

I_{D1} boundary condition in (4.26) explains that if the driver device is biased at the upper bound current level, the output device could obtain maximum non-saturated $P_{o,1dB}$ at the output. As the value of $|Z_{O,int}|$ is needed to be defined, small-signal input capacitance value (C_{i2}) is required. More details on this procedure are given in the following step 3. To determine the non-saturated operation condition for the input, similar analyses can also be used at the driver side. With using the equation (4.21) and (4.22), it is obvious that the input voltage of the driver device has to have the following condition to operate in the non-saturated region.

$$V_{i1,max} \geq \frac{V_{i2}}{G_{m1}\left|Z_{O,int}\right|} \tag{4.27}$$

4.3.3.4 Design of input, inner and output ATLs

As the third step, after determining the simplified design equations for the simplified large-signal behavior and selecting the proper biasing conditions for input and output stages, we can continue to analyze and design ATLs used at the input, inner and

output stages. From the ATL design point of view, three types of ATL sub-sections was given in Figure 4.1.

Since the active device's biasing condition is determined before in the first and second design step, frequency dependent input and output shunt capacitances (C_{i1}, C_{o1} and C_{i2}) can be extracted from small-signal s-parameter simulations. By attaching external series inductances, it is possible to implement input, inner and output ATLs to complete overall design.

Loss components (r_i and r_o) of the simplified high frequency device model are effective on the gain-bandwidth performance of the amplifier. The importance of these elements arises when their values effects Z_O and f_c of the ATLs. That is to say, higher r_i and/or lower r_o values mean more loss of the signal propagating through the ATLs. In general case, the effective contribution of the loss components increases with the increasing frequency. Gain and output power performance of the amplifier is therefore expected to degrade with the increasing frequency. In other words to say, Z_0 characteristic impedances of the ATLs will be a strong function of those loss elements in the upper frequency band of the operation.

Input Stage ATL Design: At first glance, choosing a characteristic impedance of 50Ω is reasonable through the design of input ATL. Although this can help to improve the input return loss performance (S_{11}), bandwidth limitation is possibly to be faced since the input ATL cut-off frequency $f_{c,in}$ is inversely proportional to the $Z_{0,in}$ impedance as given in equations (4.1) and (4.2).

In this study, both the input and the inner stage ATL of the DSTWPA are given to employ lossy T-sections. These lossy sections do not only improve the input/inner stage matching and gain flatness but also help to ensure stability of the amplifier in the wideband operation. Furthermore, the DSTWPA circuit also employs a capacitor (C_c) in serial to the gate terminal of the input driver device to increase the bandwidth of operation by decreasing the effective input capacitance (C_{in1}). This technique of capacitive coupling however reduces the amplifier gain as a drawback. Since the transistor high-frequency small-signal parameters r_{i1}, C_{i1} is extracted and the input ATL characteristic impedance $Z_{O,in}$ is determined, the value of coupling capacitor, loss resistor and the ATL inductor now can be determined with the similar design equations was given in (4.14) to (4.16). On account of this fact, input $Z_{O,in}$

impedance can be designed in a lower value (i.e. 30~50Ω) in order to obtain relatively more bandwidth together with sufficient input matching performance (i.e. $|S_{11}|< -10dB$).

For the proposed DSTWPA topology, a general and simplified circuit representation is presented in Figure 4.38 where some of the biasing network elements are not shown to simplify drawing. The input signal propagates along with the input ATL and stimulates T_1 gate terminal. Z_{T1} is the termination impedance of the input ATL which improve the return loss performance of the amplifier in the entire band.

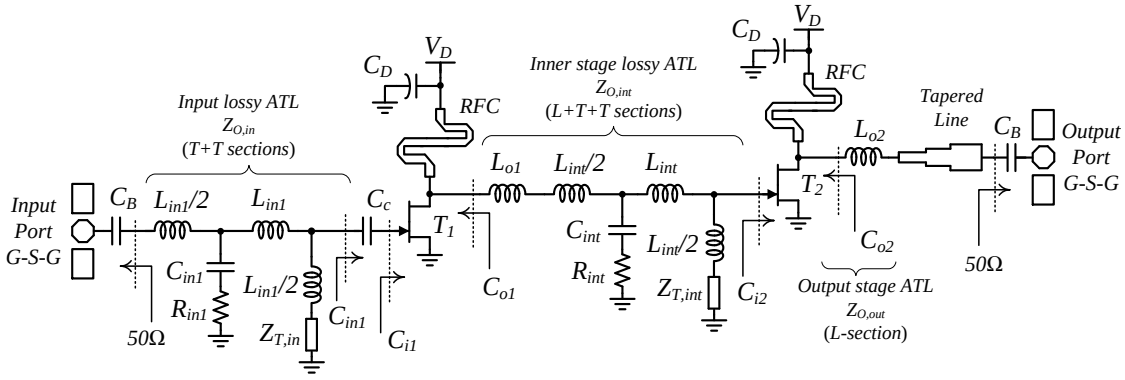


Figure 4.38 : Simplified structure of the proposed DSTWPA circuit. (Gate biasing networks are now shown.)

Inner Stage ATL Design: The amplified signal at the output of T_1 goes through the inner stage L-section ATL formed by the C_{o1} output capacitance of T_1 device and the series inductance L_{o1} and stimulates the gate terminal of T_2 power stage transistor over two T-type sections. Both input and inner stages are employing lossy ATLs comprising of loss resistors R_{in1} and R_{int}. Note that the number of the ATL sub-sections could be optimized during the design procedure and it affects mostly the gain-flatness and high frequency loss.

From the design point of view, since the only task is to drive input of T_2 and there is no need to transform any impedance into or from 50Ω, the inner stage design is less complicated than the input and output stage designs. However, inner stage characteristic impedance cannot be lower than an exact value, which can cause driving problems. In that case, driver transistor T_1 cannot provide sufficient current level; therefore, the maximum voltage swing cannot be obtained at the input of T_2. Because of this situation, T_2 cannot output its predefined maximum power and as consequence, corresponding PAE level would easily degrades. On the other hand, the

inner stage characteristic impedance cannot be also too high where a bandwidth limitation can occurs easily. Thus, when designing the inner stage network, the tradeoff between the driving capability of the driver stage and the bandwidth optimization must be taken into consideration. Input and inner stage ATL terminations should be chosen to fit the line characteristic impedances as $Z_{T,in}=Z_{0,in}$ and $Z_{T,int}=Z_{0,int}$. This will ensure the circuit stability over the bandwidth of operation. Since the power levels are not high in the input and inner stage, any power absorbed on the Z_T terminations and loss elements (R_{in1} and R_{int}) will not degrade the overall PAE performance.

The Output Stage Design: The design of the wideband output power-matching network is based on a previously proposed simple and accurate wideband load-pull characterization in order to determine an appropriate and optimum single L_{o2} output-line inductance. Since the occupied inductor area on the die becomes higher with the increasing inductance value for a given current density, limiting the value of the inductance at the output stage is very important. High frequency loss (e.g. substrate loss and stray capacitances effects) increases when the inductor size is large and as a result, amplifier's overall output power and efficiency performance degrades. Moreover, using small number of elements at the output helps to overcome such power-loss problems and the amplifier's construction.

In the design of DSTWPA, output signal propagates directly into the L-section of C_{o2} and L_{o2}, which is maintaining simple wideband load-pull, based matching purpose as mentioned before. The output stage ATL is designed to obtain optimum load seen by the transistor output. Additionally, an optimized tapered impedance transformer is used to improve and optimize overall matching as much as possible into the standard 50Ω load.

4.3.3.5 Realization of GaAs PHEMT SSTWPA

Above given systematic methodology is used to design and realize DSTWPA with using 0.25μm GaAs PHEMT MMIC process. Proposed design steps are given in details with the corresponding circuit design parameters and determined element values.

As the first step of the design procedure, an output power transistor having channel width of 125μm and 12 fingers geometry is selected to examine. Selected geometry

is investigated for its suitability and capability of the predefined specifications where $P_{o,1dB}$ >0.5W is expected. The upper limit of the bandwidth is targeted up to 10GHz. Here to note that before starting the design procedure, a quick dc analysis and small-signal inspections at various reasonable biasing currents can give some opinions about the device characteristics such as gain and bandwidth characteristics. In addition, a load-pull simulation environment using Agilent Advanced Design System (ADS) and high accuracy nonlinear device model supplied from the vendor (United Monolithic Semiconductor) are used to determine the device large-signal behavior.

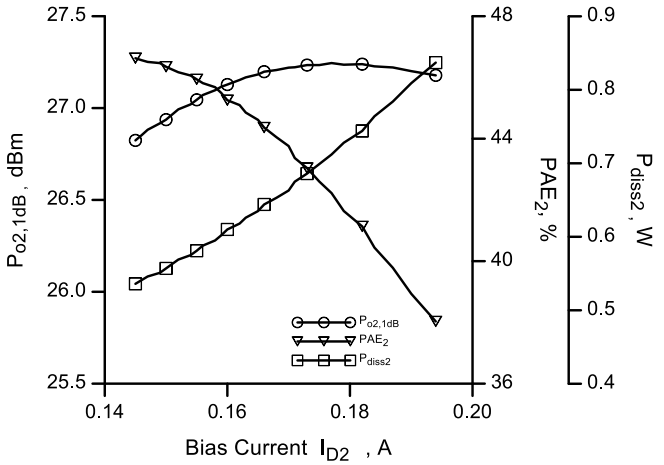


Figure 4.39 : 1dB compression ($P_{o2,1dB}$), efficiency (PAE_2) and the dissipated power (P_{diss2}) performance of 125x12µm (T_2) device at 4GHz.

To make use of the wideband and linear characteristic of the device, it is convenient to bias the device in class-A operation. For the proposed design procedure, it is necessary to determine $I_{D2,opt}$ biasing current for the given device before switching to inspect load-pull data. For this purpose, device is excited over a standard 50Ω impedance. From the simulations, output power at 1dB compression and the corresponding PAE values are collected where the device biasing current is taken as the swept parameter.

Figure 4.39 summarizes the performance of the output device at 4GHz operation. (i.e. the expected mid-band frequency.) It is clear from the characteristics that the device 1dB compression power level ($P_{o2,1dB}$) is increasing proportionally with the bias current. After some current level, $P_{o2,1dB}$ starts to saturate. At this point, we can choose a bias current value which is not only maximize both $P_{o2,1dB}$ and PAE but also guarantee a stable and safety operation for the device itself due to increasing junction temperature which is directly proportional to the dissipated power (P_{diss2}) inside the junction.

Table 4.4 : The simulated load-pull data for 125x12µm (T_2) devices at $I_{D2,opt}$=150mA.

Frequency [GHz]	$Z_{L,opt}@P_{o,1dB}$ $[R_{L,opt}+jX_{L,opt}]$[Ω]	$P_{o2,1dB}$ [dBm]	PAE $@Z_{L,opt}$ [%]
1	42.0+5.6j	28.0	43.6
2	28.3+3.2j	28.6	47.0
4	19.9+11.4j	29.9	48.3
6	13.1+9.3j	29.6	47.6
8	20.5+5.0j	30.6	51.4

From these facts, I_{D2} is selected as 150mA which is equal to $I_{D2,opt}$ parameter of the first design step. After determining $I_{D2,opt}$, we can search the optimum load values in the desired frequency range. Table 4.4 shows the optimum load impedances taken at $P_{o,1dB}$.

Since the biasing current I_{D2} was determined before in the first step, we can find maximum input voltage across the T_2 input using the equations (4.21) to (4.24). For this aim, we have to extract K_2 value of the device for the given I_{D2}. Figure 4.40 shows G_{m1} and G_{m2} characteristics of the two devices where I_{D1} and I_{D2} are the swept parameters. As seen in the plot that, G_{m2} value of the power device at 150mA biasing is around 0.42S and so that K_2 could be calculated around $1.18AV^{-2}$. With the addition of the other parameters (0.5W of $P_{o2,1dB}$ and 23Ω of $|Z_{L,opt}|$), it is possible to use Figure 4.24 and find $V_{i2,max}$ around 0.5V. Note that the maximum ratings (i.e. breakdown voltages) for the gate terminal also should be checked from the device/process vendor for a proper and safe operation.

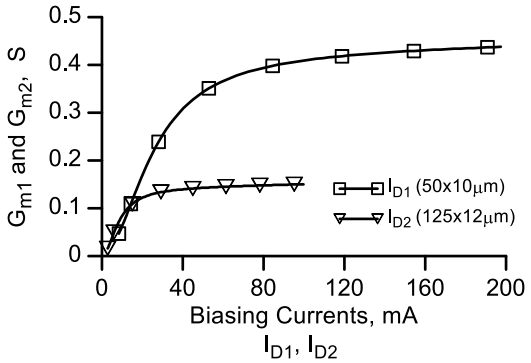


Figure 4.40 : G_{m1} and G_{m2} characteristics vs biasing currents of the transistors.

After finding the input voltage limit of the power device, we can jump to second step and choose a proper biasing for the driver stage according to Figure 4.41. To

determine the value of I_{D1}, we need to know $|Z_{O,int}|$. In this point, we have to jump to third step for a while and rearrange equation (4.1) and (4.2) as below

$$Z_{0,int} \cong \sqrt{\frac{L_{int}}{C_{i2}}} \quad \textbf{(4.28)}$$

$$f_{c,int} \cong \frac{1}{\pi\sqrt{L_{int}C_{i2}}} \quad \textbf{(4.29)}$$

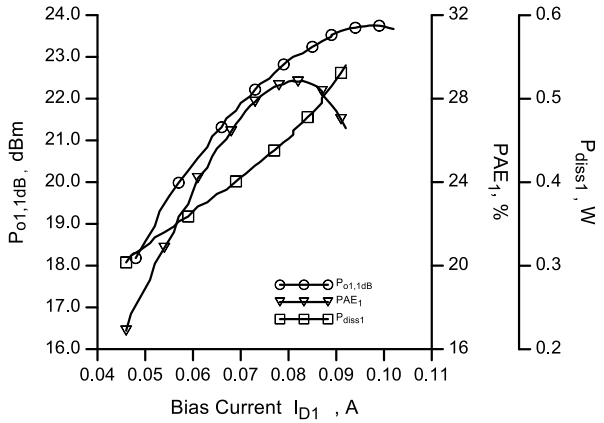


Figure 4.41 : 1dB compression ($P_{o1,1dB}$), efficiency (PAE_1) and the dissipated power (P_{diss1}) performance of 50×10µm (T_1) devices at 4GHz.

Since the design was desired to operate up to 10GHz and as I_{D2} was determined as 150mA, C_{i2} could be extracted around 4.5pF (See Figure 4.42) and equation (4.29) obtains 0.23nH of L_{int} value. Continuously, we could determine $|Z_{0,int}|$ equal to 7.1Ω with help of (4.28). Now we can complete second step and determine driver device biasing current. According to (4.26), I_{D1} could be calculated as <69mA.

As we have determined boundary value for I_{D1}, we have to select a proper geometry for the driver device which have to be large enough to supply <69mA and at that biasing boundary, it should satisfy the both non-saturated linear operation and proper efficiency. According to this information, a driver transistor of 50×10µm geometry is selected and I_{D1} of 60mA is observed suitable for the given specifications. Figure 4.41 shows the device characteristics for the driver T_1 of 50x10µm. As clear from the $P_{o1,1dB}$ behavior, output power starts decreasing over 70mA which is expected to happen.

If the calculated I_{D1} was higher than the given characteristics, we would have possibly increased the transistor geometry. This would not only help to increase linearity but also to overcome thermal management problems. However, if the

calculated I_{D1} was too low, of course the device geometry have should be selected as low as possible to make design both efficient and high bandwidth.

After determining the biasing currents of the two devices, small-signal characteristics including the input and output capacitance/conductance values could be examined. Figure 4.42 shows input and output capacitances for the devices respectively. This information is the base of corresponding ATL design equations given before in the third step.

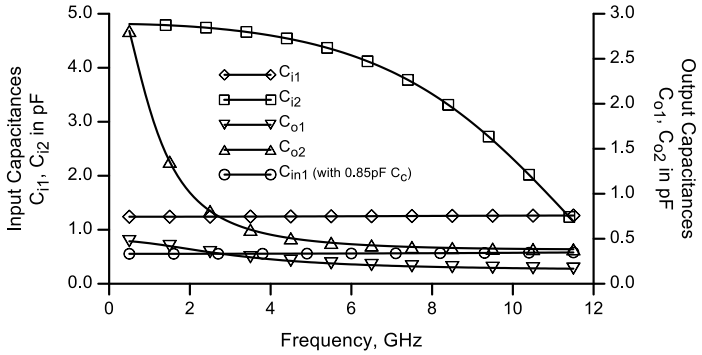


Figure 4.42 : Small-signal input and output capacitance characteristics of the T_1 and T_2 devices.

At the input, to match into the standard 50Ω source impedance, it is desirable to design 50Ω input ATL characteristic impedance ($Z_{0,in}$) in the entire bandwidth. When Capacitor C_c is not used, equation (4.1) and (4.2) could be rearranged for the input ATL as

$$Z_{O,in} \cong \sqrt{\frac{L_{in1}}{C_{i1}}} \qquad \textbf{(4.30)}$$

$$f_{c,in} \cong \frac{1}{\pi\sqrt{L_{in1}C_{i1}}} \qquad \textbf{(4.31)}$$

and by taking $Z_{0,in}$ as 50Ω and 1.2pF of C_{i1}, input ATL inductance L_{in1} could be calculated as 3nH. Then switching to line cut-off frequency equation, $f_{c,in}$ can be calculated as 5.3GHz which is far from the desired 10GHz of operation. To solve the problem of input ATL $f_{c,in}$, a capacitive coupling technique is employed to reduce equivalent input capacitance (C_{in1}) of the device. The drawback of using such technique is reducing the overall gain level since the signal voltage is divided between the coupling capacitance (C_c) and the gate-source capacitance of the device. In this way, C_{in1} is reduced to around 0.5pF where 0.85pF of C_c is taken as an

optimized value. By replacing C_{i1} with C_{in1} in (4.30) and (4.31), we can conclude to around 12GHz of $f_{c,in}$ when using 50Ω ATLs at the input which is quite enough for the desired bandwidth. Overall input line is constructed with using two T-sections one of which is lossy. In this way, we have more possibilities of managing the gain flatness and stability concerns in the wideband of operation. For the output side, according to the given impedance values and using the proposed technique, a simple output stage ATL L-type network could be designed by choosing a best fitting impedance value of 0.6nH for L_{o2} where C_{o2} of the device is around 0.5pF. For the biasing purposes at the drain nodes, on chip inductive lines are constructed to form wideband RF chokes (RFCs) which was previously proposed. By doing this kind of on-chip RFCs, the parasitic addition to the drain-source capacitance is minimized according to off-chip high parasitic RFCs. The magnitude of the impedance tied to corresponding RFC pads is strongly needed to be as low as possible (theoretically perfect ac ground) for the proper operation of the on chip RF choke. Finally, the magnitude of the simplified small-signal gain for the DSTWPA circuit could be given by

$$|A_o| \cong \left(\frac{C_C}{C_{i1} + C_C} \right) G_{m1} G_{m2} Z_{O,int} Z_{O,opt} \qquad \textbf{(4.32)}$$

It is obvious that the expressions given above are used in the first order design of the DSTWPA circuit. It is necessary to instigate optimization steps in order to improve the small-signal and power performances of the DSTWPA circuit in the desired frequency band of operation. For this aim, since the simulation results is converged to goal characteristics by design procedure, gradient type optimization was also selected to finalize design by choosing 10% of deviations for the passive devices.

4.3.3.6 Measurement results for GaAs PHEMT SSTWPA

The proposed DSTWPA design is fabricated using UMS 0.25μm GaAs PHEMT MMIC process. All the circuit level and electromagnetic simulations are performed using ADS simulation environment. The fabricated die chip of DSTWPA is shown in Figure 4.43 where the bare-die chip size is $3.4 \times 1.4 mm^2$. Test chip is attached on an FR4 substrate using conductive epoxy and all RF signals are left inside the chip and only dc biasing is supplied with the aid of wire bonding. RF measurements are fulfilled using probe station and GSG type probes at both input and output ports.

Table 4.5 : Element values of CSSTWPA circuit in Figure 4.38.

Element	Value
L_{in1}	3nH
C_{in1}	0.5pF
R_{in1}	3Ω
$Z_{T,in}$	50Ω
C_c	0.85pF
L_{o1}	0.25nH
L_{int}	0.23nH
C_{int}	4.5pF
R_{int}	3Ω
$Z_{T,int}$	7.1Ω
L_{o2}	0.6nH
C_B	8pF
C_D	100nF

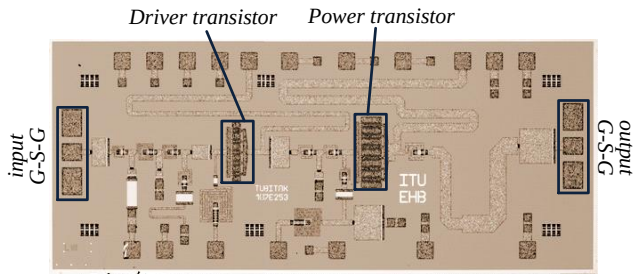


Figure 4.43 : Chip photograph of the fabricated DSTWPA circuit. Bare-die chip size is 3.4×1.4mm^2.

The simulated and measured small signal *s*-parameter performances of the DSTWPA will be presented below: the gain performance (S_{21}) is shown in Figure 4.44 and as seen from the figure that there is an agreement between the simulation and measurement results within the most of the band. The DSTWPA circuit exhibits almost flat gain response of 15dB across the bandwidth of 1.5-to-9GHz. Figure 4.45 shows the input matching (S_{11}) performance of the DSTWPA. As seen from the figure, there is an agreement between the simulation and measurement results in the most of the band. S_{11} is obtained below -10dB entire the 1.5-to-9GHz of operation. Figure 4.46 shows the output matching (S_{22}) performance of the DSTWPA. S_{22} of the amplifier is not below -10dB for most of the band. However, this is an expected result since the output stage of the circuit was designed to obtain optimum power performance (load-pull match) where a small-signal conjugate matching condition is not used in the design. Figure 4.47 gives the reverse gain (S_{12}) performances of the DSTWPA. It is seen that the reverse gain (or isolation) is below -50dB which is low enough for most of the applications.

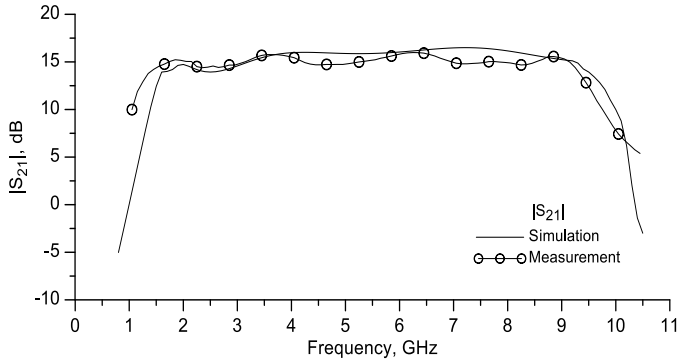


Figure 4.44 : The simulated and measured gain ($|S_{21}|$) performance of the proposed DSTWPA.

Figure 4.45 : The simulated and measured input matching ($|S_{11}|$) performance of the DSTWPA.

Figure 4.46 : The simulated and measured output matching ($|S_{22}|$) performance of the DSTWPA.

Figure 4.47 : The simulated and measured reverse gain ($|S_{12}|$) performances of the DSTWPA.

Figure 4.48 shows the output power performances of the DSTWPA in terms of the output referred 1dB compression point ($P_{o,1dB}$) and saturated power level ($P_{o,sat}$).

From the measurement results, the saturated output power level is measured nearly 1W (30dBm) in most of the band while the $P_{o,1dB}$ is around 0.65W (~28dBm). Figure 4.49 gives PAE performance of the DSTWPA at $P_{o,1dB}$ and $P_{o,sat}$ level. The saturated PAE (PAE_{sat}) is above 50% and corresponding PAE (PAE_{1dB}) is above 36% in most of the band.

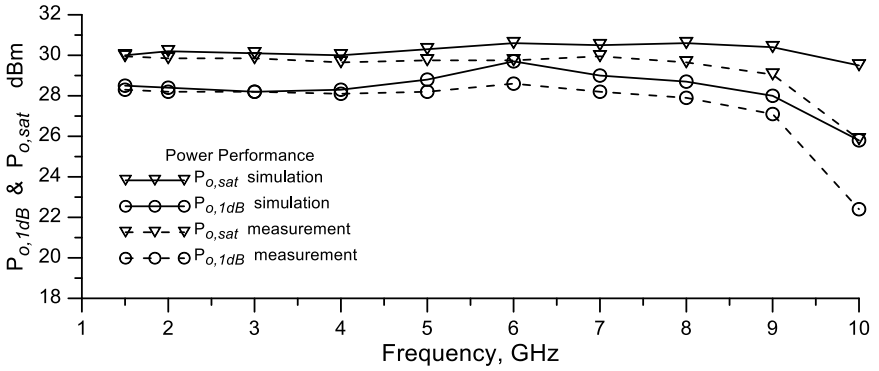


Figure 4.48 : Output power performances of the DSTWPA at the output referred 1dB compression and saturated power points.

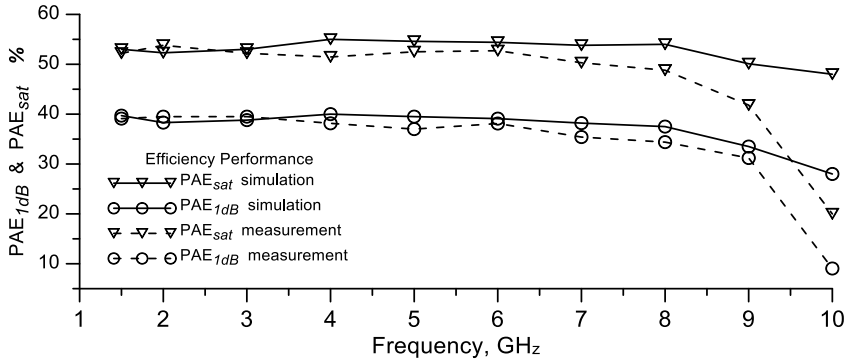


Figure 4.49 : Power added efficiency (PAE) performance of the DSTWPA at 1dB compression and saturated power points.

There is a good agreement with the simulation and measured results in the most of the band. To show the advantages of the proposed methodology, overall DSTWPA performance is compared to the SSTWPA which includes only one active power device. Since it is a single stage amplifier, gain is lower to cascaded version and for a similar transistor size, output power and corresponding efficiency level is expected to be same. To make the comparison clear and meaningful, previously proposed SSTWPA circuit is used, which employs the same T_2 power transistor of the proposed DSTWPA circuit. Measurement results of the fabricated SSTWPA chip are used here to compare the results with the DSTWPA. The SSTWPA circuit has a bandwidth of 1-to-8GHz with an average reduced gain of 9dB as expected. The

comparisons of the power performances of the DSTWPA and SSTWPA are given below in Table 4.6. According to the results, DSTWPA has provided better power performance at $P_{o,1dB}$. This is due to the higher gain performance of the DSTWPA circuit.

Table 4.6 : The measured power and PAE performances of the proposed DSTWPA and the SSTWPA.

Frequency (GHz)	**SSTWPA** (Sayginer et al, 2013)				**DSTWPA** (This work)			
	$P_{o,1dB}$ (dBm)	PAE_{1dB} (%)	$P_{o,sat}$ (dBm)	PAE_{sat} (%)	$P_{o,1dB}$ (dBm)	PAE_{1dB} (%)	$P_{o,sat}$ (dBm)	PAE_{sat} (%)
2	27	40	30	68	28	39	30	54
4	25	27	28	54	28	38	30	53
6	26	34	30	78	29	39	30	54
8	28	45	29	50	28	36	30	50
10	-	-	-	-	23	10	29	22

Since the lower gain values causes an increase over the input nonlinearity, the output power level at 1dB compression decreases accordingly. Consequently, PAE performance of the SSTWPA decreases because of the lower output power level than the DSTWPA circuit. On the other hand, both topologies have given similar saturated output power performance where the devices are in a heavy nonlinear operation. Moreover, PAE performance of the SSTWPA is better for the saturated power case. This is due to using only one transistor while the DSTWPA circuit includes an additional driver stage which consumes extra-power.

4.4 Chapter Conclusions

In this chapter, four wideband PA designs were given. Two of the designs were based on 0.35μm SiGe HBT and the remaining two designs were in 0.25μm GaAs PHEMT MMIC process. The first two designs were decade bandwidth medium power PAs. The starting PA was a single-stage TWPA employing only a single transistor and was load-line matched at the output. By removing the output ATL termination impedance, both the output power and PAE was improved. The second amplifier design is a cascaded version of the first PA where the input amplifier stage feeds the two identical amplifiers in a parallel configuration whose outputs are combined together to increase the output power by twofold over the desired operational frequency bandwidth. At the beginning of the bandwidth, the amplifiers'

measured results closely agreed with the simulation results and when the frequency is increased, both the substrate loss of Si and external collector feed bias circuity dominates by their parasitic and thus more output power is lost. This is the reason of mismatced power and PAE characteristics of simulation and measurement at the upper portion of the bandwidth.

In the second phase of the chapter, an SSTWPA was comprised of capacitive coupling and frequency dependent lossy artificial transmission-line to enhance the amplifier's frequency-bandwidth product, input matching and gain flatness response. A broadband load-pull technique using a graphical design approach was used to ensure a predefined power level is delivered to the load over the amplifier's operating bandwidth. The parasitic capacitance associated with the off-chip RF choke degrades the bandwidth performance of the amplifier. To eradicate this problem, an integrated microstrip line is implemented at the drain node, which is used as RF choke to operate in the wideband. The proposed SSTWPA design provides wideband operation with gain flatness, optimized flat power performance and high efficiency in the desired bandwidth. Moreover, the single transistor design is relatively simple to implement, occupies less chip area and thus cost effective compared with the multi-stage version of TWPAs.

Additionally, a straightforward systematic design of a cascaded-double stage PA circuit operating in Class-A is proposed. The DSTWPA employs two transistors one of which is the driver and the other serves as the output power device. The proposed circuit comprised of the capacitive coupling and frequency dependent lossy ATL techniques to enhance the amplifier frequency-bandwidth product, input match and gain flatness response. In addition to this, previously proposed broadband load-pull technique is used to predict output ATL line elements, which improve the broadband-power performance of the circuit. Output ATL line is comprised of a simple L-type ATL section to achieve an optimum power-bandwidth and PAE performance. Gain-frequency and power performances of the DSTWPA were compared to the performance of a single stage travelling wave power amplifier which was employed the same power transistor. As it was proved that, the DSTWPA circuit has given better performances over the single stage version. Proposed methodology shown to simplify the design of cascaded topologies in an efficient and

systematic way, meanwhile obtaining the high performance metrics over the bandwidth and the output power/efficiency.

It would be also useful to compare the load-line design technique with respect to load-pull approach. Since load-pull data stores the frequency dependent impedance information, there is no doubt that the power matching performance of the load-pull based methods are better. To clarify the issue, for a single transistor GaAs design, a comparison at different operating frequencies for both load-line and proposed load-pull match are given in Figure 4.50a and Figure 4.50b, respectively. Similarly, the comparison of the output 1dB power and PAE simulations could be observed in Figure 4.51 and Figure 4.52, respectively.

As seen from the results that, laod-pull approach has better performance characteristics over the load-line method. However, collecting load-pull impedance data is a complex task according to load-line process which can simply be extracted from the device *i-v* characteristics.

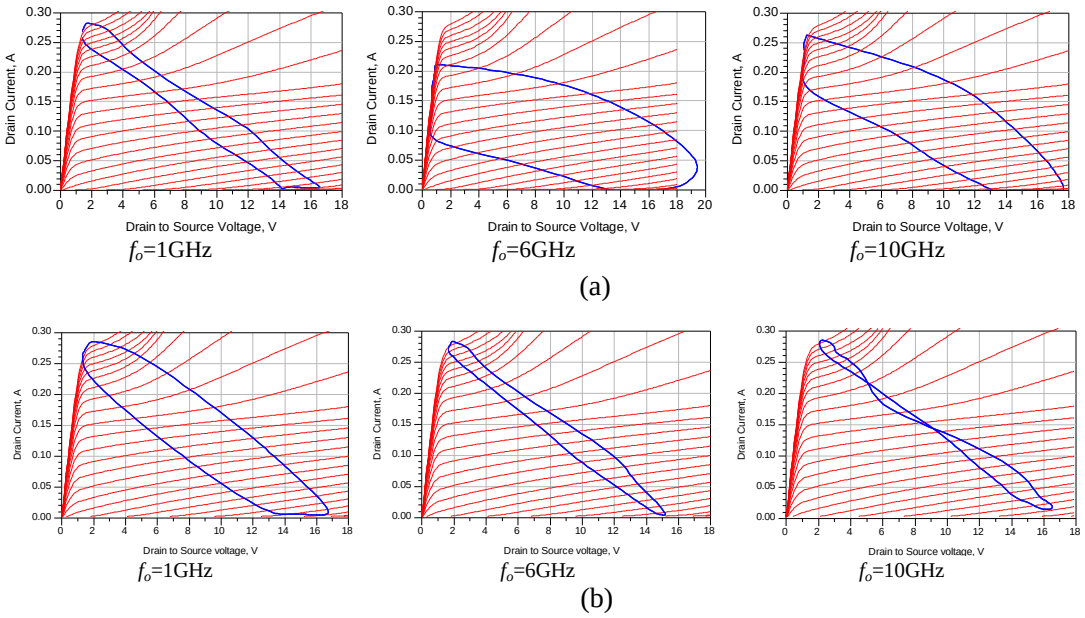


Figure 4.50 : Comparison of the output load-line simulations at different operating frequencies (a) for load-line match (b) for proposed load-pull match.

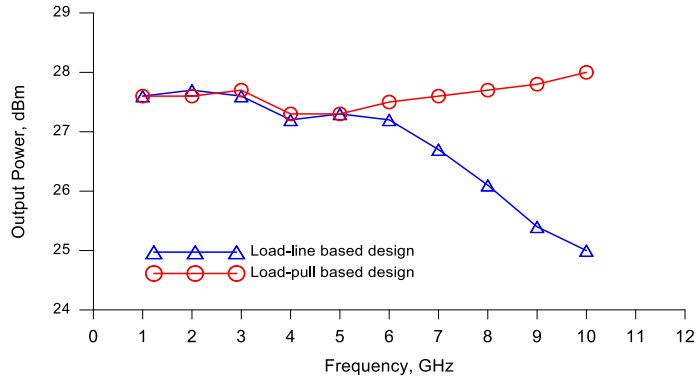


Figure 4.51 : Comparison of the output 1dB power simulations (a) for load-line match (b) for proposed load-pull match.

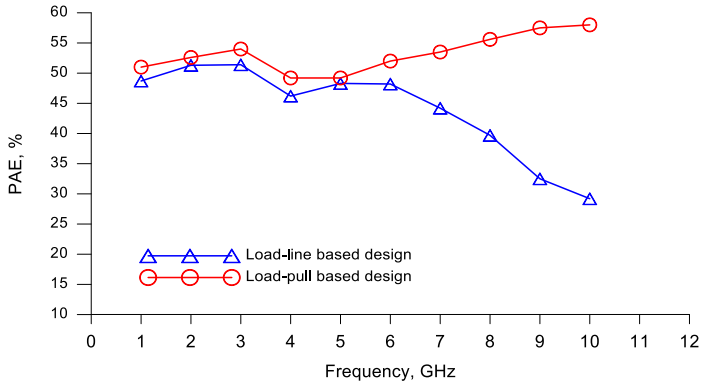


Figure 4.52 : Comparison of the PAE (a) for load-line match (b) for proposed load-pull match.

5. FURTHER IMPROVEMENTS ON THE DESIGN OF EFFICIENT WIDEBAND GaN PAs

In this section, some of the design methodologies for the wideband power amplifiers are studied where at first; a systematic technique based on a susceptance minimizing concept at the output matching network is presented. Proposed approach uses two main sub-blocks, which are a short-circuited transmission-line for susceptance minimizing and multi-section transformer for the remaining matching purpose. The design procedure is investigated conceptually and simple theoretical analyses are given to show that how the proposed method could help to simplify wideband design. Moreover, the given approach not only improves the output power and efficiency performance of the given transistor but also takes care of the biasing network simultaneously over the wide range of the frequencies.

5.1 Design of Wideband GaN PA Based on a Systematic Susceptance Minimizing Technique

A systematic technique to design output stage of a wideband PA will be presented conceptually. A design example to show the performance of the presented approach will be studied using GaN HEMT transistor where a high performance solution to the new technique is constituted. Continuously, a real design example is fully implemented in the ADS environment with using microstrip design techniques and the PA performance will be inspected within the desired band. Finally, a comparison of the design performance to the known design solutions is given to show advantages of the method.

5.1.1 Characterizing the power device: load-pull analyses

Proposed design methodology starts with selecting a suitable transistor and gathering $Z_{L,opt}(j\omega)$ optimum load impedances. A GaN HEMT transistor designated CGH40010F from Cree is selected to examine in this study. Cree's CGH40010F is an unmatched, packaged GaN HEMT, operating from a 28V rail and serving up to 6

GHz of operation. CGH40010F offers a general purpose, broadband solution to a variety of RF and microwave applications (Url-2).

A fully nonlinear ADS device model provided from the vendor is used for all linear/nonlinear simulations. To gather $Z_{L,opt}(j\omega)$ data from the device, a sufficient number of load-pull analyses are examined in the range of 0.5-to-6.5GHz and output power is inspected at 1dB compression ($P_{o,1dB}$) to look for $Z_{L,opt}(j\omega)$ impedances together with the corresponding PAE levels.

Table 5.1 shows the tabulated $Z_{L,opt}(j\omega)$ impedances and the corresponding $P_{o,1dB}$ and PAE levels for the simulated frequencies. Optimum reflection coefficient ($\Gamma_{L,opt}$) values on the Smith Chart is also illustrated in Figure 5.1.

From the simulation results, CGH40010F seems to be able to supply over 10W output power in the wideband operation while the corresponding PAE levels are >50% for class-A/AB operation of the transistor where the device is biased at I_D=640mA and V_{DS}=28V.

Table 5.1 : Optimum load impedances of CGH40010F at $P_{o,1dB}$.

Frequency [GHz]	$Z_{L,opt}@P_{o,1dB-max}$ $[R_{L,opt}+jX_{L,opt}][\Omega]$	$Z_{L,opt}@PAE_{max}$ $[R_{Lopt}+jX_{L,opt}][\Omega]$	$P_{o,1dB-max}$ [dBm]	PAE_{max} [%]
0.5	33.7+8.2j	41.25+9.55j	40.29	55.17
1.0	29.3+7.45j	33.25+10.25j	40.64	56.49
1.5	25.35+6.65j	26.7+14.7j	40.78	57.13
2.0	22.0+4.35j	24.55+10.05j	40.96	56.50
2.5	18.75+3.95j	19.5+8.7j	40.95	56.39
3.0	17.8+0.85j	18.55+5.4j	41.04	56.14
3.5	17.75-0.6j	17.25+3.65j	41.00	54.92
4.0	16.55-2.0j	14.85-0.75j	40.98	55.56
4.5	15.4-6.1j	14.1-1.9j	41.03	55.42
5.0	14.85-8.95j	13.95-6.05j	41.05	54.73
5.5	15.5-12.1j	12.1-9.55j	41.04	54.41
6.0	15.4-16.6j	11.7-13.45j	41.02	54.06
6.5	16.7-21.4j	13.55-19.3j	41.04	52.91

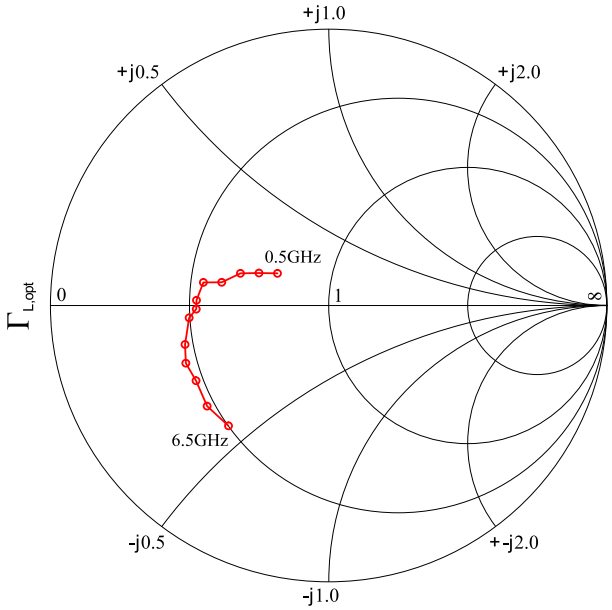


Figure 5.1 : Wideband $\Gamma_{L,opt}$ trace for CGH40010F related to $P_{o,1dB}$ where the device is biased at I_D=640mA and V_{DS}=28V. Circles on the trace are spaced in 0.5GHz.

5.1.2 Modeling for susceptance minimizing technique

As it was given before, one can obtain maximum power from a source having finite internal resistance, if and only if the load resistance is equal to the resistance of the corresponding source. It is also possible to extend the theory to AC circuits, which include reactance part, and the maximum power transfer occurs when the load impedance is equal to the complex conjugate of the source impedance. However, power transferring by using conjugately matched source and load impedances are not practical especially when the source is implemented by active devices (i.e. transistors), which have limited voltage and current characteristics.

Coming from this fact, since the collected $Z_{L,opt}(j\omega)$ values are related to the large-signal power matching condition, a conjugate matching approximation and could be used to represent power transferring networks as shown in Figure 5.2. Thus, following impedance relation could be written to define maximum power condition;

$$Z_{T,out}(j\omega) = Z^{*}_{L,opt}(j\omega) \qquad \textbf{(5.1)}$$

Above explained approximation could help to build up a simple and useful wideband large-signal tabulated device model as in Figure 5.3. According to the model, G_m simply represents the large-signal transconductance of the device. $Y_{T,in}(j\omega)$ and

$Y_{T,out}(j\omega)$ represent the input and output large-signal complex admittances respectively where $Y_{T,out}(j\omega)$ is equal to $1/Z_{T,out}(j\omega)$ by definition.

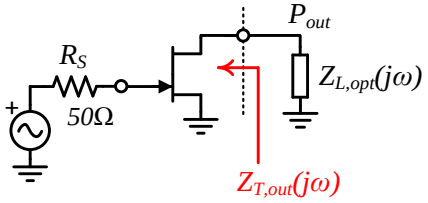


Figure 5.2 : Simplified device representation showing both $Z_{L,opt}(j\omega)$ and $Z_{T,out}(j\omega)$ impedances.

Input admittance $Y_{T,in}(j\omega)$ is not going to be interested in this study since the maximizing of the output power strongly depends on the output matching condition. Once the output-matching network is determined then the overall design procedure will be followed to implement a proper wideband input matching network to flatten gain response without sacrificing the output power and efficiency level substantially.

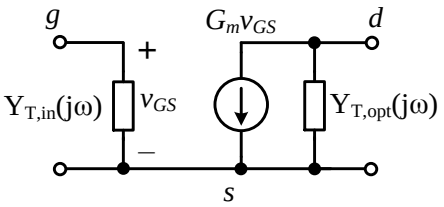


Figure 5.3 : Simplified admittance representation of the GaN HEMT device.

Device $Y_{T,out}(j\omega)$ output complex admittance could be split into the real and imaginary parts as

$$Y_{T,out}(j\omega) = G_{T,out}(\omega) + jB_{T,out}(\omega)$$
$$= \frac{R_{L,opt}(\omega)}{R_{L,opt}^2(\omega) + X_{L,opt}^2(\omega)} + j\frac{X_{L,opt}(\omega)}{R_{L,opt}^2(\omega) + X_{L,opt}^2(\omega)} \qquad \textbf{(5.2)}$$

where both $G_{T,out}(\omega)$ and $B_{T,out}(\omega)$ are frequency dependent large-signal output conductance and susceptance respectively. Moreover, frequency dependency of the $G_{T,out}(\omega)$ is not only correlated to $X_{L,opt}(\omega)$ term but it also depends on the frequency dependent real $R_{L,opt}$ part of the device optimum $Z_{L,opt}(j\omega)$ impedance as it was indicated in Table 5.1.

Above given complex $Y_{T,out}(j\omega)$ expression is the origin of the susceptance minimizing technique. From this moment on, the question arises if there exists any way to cancel or minimize the imaginary part of $Y_{T,out}(j\omega)$ admittance in the entire

frequency band. In other words, we could simplify the wideband-matching problem by removing $B_{T,out}(\omega)$ susceptance at the output since there will remain only $G_{T,out}(\omega)$ conductance to be matched in the entire band. Therefore, we need a susceptance minimizing network having $B_{B,in}(\omega)$ susceptance equal to $-B_{T,out}(\omega)$ profile in the whole operation band. Additionally, $B_{B,in}(\omega)$ circuitry is also needed to be implemented as simple as possible to make sure of not consuming any undesirable amount of power since the both power level and bandwidth are very high at the output. In other words, there should be no additional resistive/conductive parasitic term attached to the $B_{B,in}(\omega)$ implementation.

From the narrow band design of interest, cancelation (or absorption) of $B_{T,out}(\omega)$ is applicable with using various types of impedance matching networks. On the other hand, wideband designs are not suitable to obtain such narrowband design techniques.

Almost the most critical step of any wideband PA design is the synthesis of the matching networks, which ensure maximum power is transferred to a load within the operation band. In practice, this cannot be realized easily for all the frequencies that we have interested which was indicated before.

In practice, there are always reactance/susceptance parts for the complex impedances at both input and output ports of any given active device. From the power device perspective, the main problem arises as the optimum impedance tracking problem of the matching network, which must ideally keep the track of load-pull $Z_{L,opt}(j\omega)$ impedances data with the increasing frequency. Generally, this is not an easy task. In other words, one cannot easily obtain convenient matching networks to transform optimum impedance loads into a known real load (e.g. 50Ω) in the entire band. In this section, a simple and realizable way for the output-matching network is examined. Proposed technique helps to relax optimization steps for the wideband methods by applying a sequential design procedure for the matching network. Proposed design procedure includes the design of two sub-blocks: First sub-block is the susceptance minimizing process as illustrated conceptually in Figure 5.4. By doing this, one can get a susceptance free real $Y_{T,out}(j\omega)$ admittance at the output. Second part is the transforming of the susceptance free real-admittance into the real load impedance.

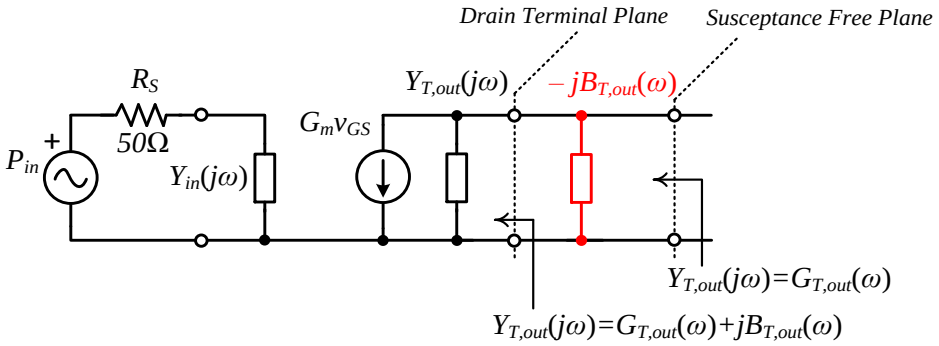


Figure 5.4 : Susceptance cancelation with using $-jB_{T,out}(\omega)$ at the device output.

As was mentioned before, for the given design problem here, $R_{L,opt}(\omega)$ is frequency dependent. In this step, by using the conjugate matching condition, $G_{T,out}(\omega)$ will be transformed into real 50 load impedance with using a multisection transforming network. Figure 5.5a and b show the classical wideband-matching network synthesis problem and the systematic approach given in this study respectively. The approach given here uses a systematic design procedure including the relaxed optimization steps. In the next sub-section, a suitable circuit implementation of $B_{B,in}(\omega)$ will be examined.

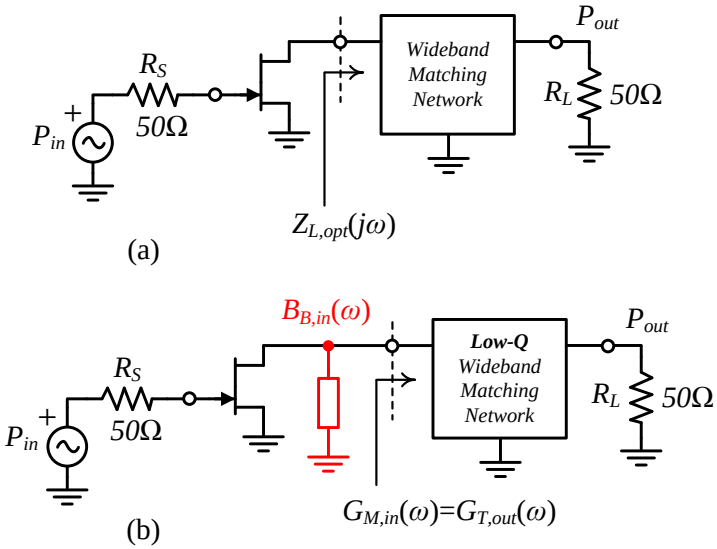


Figure 5.5 : (a) Wideband-matching problem at the output of PA. (b)Proposed matching approach for the output of a wideband PA.

5.1.3 Circuit implementation for negative susceptance

A possible circuit implementation of $B_{B,in}(\omega)$ equal to $-B_{T,out}(\omega)$ is the bottle neck of the proposed approach. It is also possible to make a simple conversion and use the term capacitance at the output of the device,

$$C_{T,out} = \frac{B_{T,out}(\omega)}{\omega} \qquad \textbf{(5.3)}$$

$C_{T,out}$ could be said as the output frequency dependent large-signal capacitance including the non-linarites. Using capacitance notation is sometimes convenient since the shunt capacitance representation is suitable when dealing with the real physical circuit elements. For the given transistor, Figure 5.6 shows the both $Z_{T,out}(j\omega)$ and $Y_{T,out}(j\omega)$ in terms of real and imaginary parts.

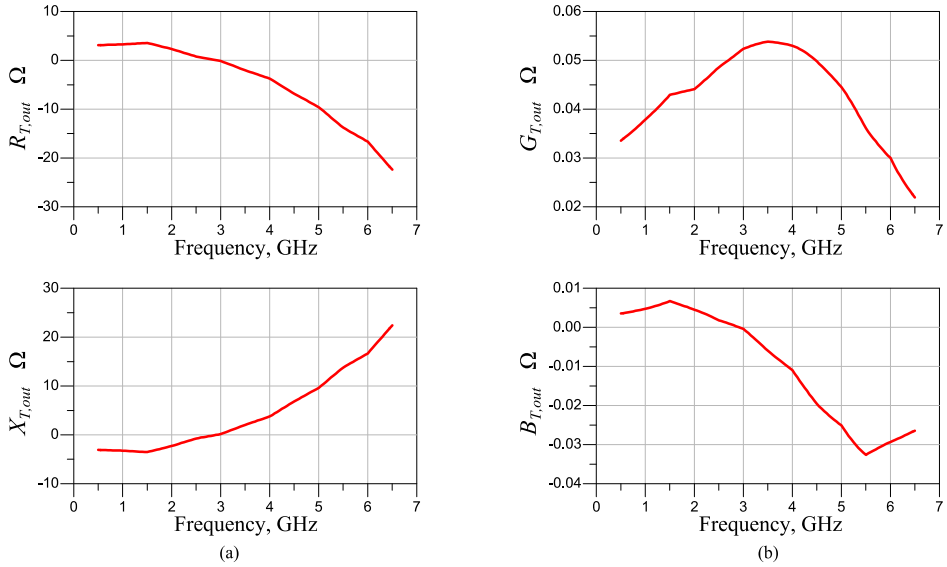


Figure 5.6 : CGH40010F output (a) $Z_{T,out}(j\omega)$ impedance and (b) $Y_{T,out}(j\omega)$ admittance in the real and imaginary parts.

It is seen that the device output susceptance (i.e. $C_{T,out}$) profile has shown to be positive for <3GHz and becoming negative for >3GHz. That is to say, according to the susceptance minimizing process we have to make sure of having ideally zero value total susceptance profile for the entire band after applying $B_{B,in}(\omega)$ at the output. In other words, we should design a network having capacitance profile shunted at the drain terminal of the transistor. We could call this capacitance as the equalizer capacitance and it should have a profile opposite to $C_{T,out}$ as given in Figure 5.7b. Since the device optimum impedances are gathered at the device's $P_{o,1dB}$ point for all the frequencies and the almost class-A operation is obtained, counter-clockwise rotation of $Z_{L,opt}(j\omega)$ on the smith chart given in Figure 5.1 was mainly due to the terminal parasitic elements where the packaging parasitic dominates the most. According to the given device model, a series inductance of 0.5nH is modeled at the output terminal of CGH40010F to include drain side packaging effect (Url-3).

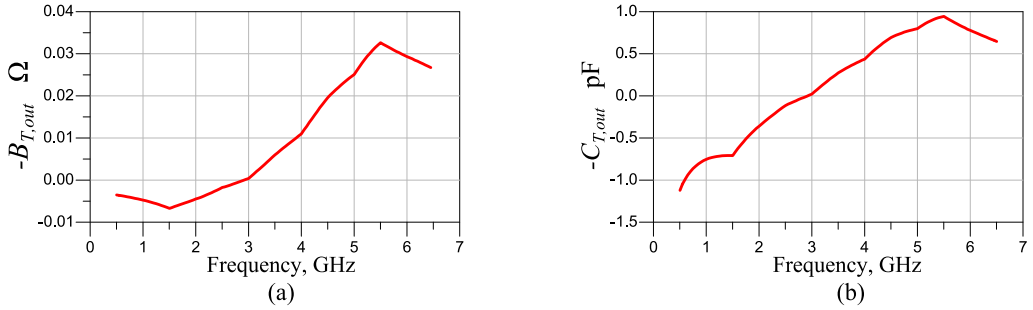


Figure 5.7 : (a) $-B_{T,out}(j\omega)$ susceptance and (b) corresponding capacitance profile.

Coming from this fact, since the conjugate matching condition was defined as $Z_{T,out}(j\omega)$ is equal to $Z_{L,opt}(j\omega)$, a negative-to-positive capacitance profile of Figure 5.7 is not surprising since the parasitic inductance dominates at higher frequencies and resulting a shunt negative capacitance effect at the output.

Various active device circuitries could be used to implement such an equalizer capacitance profile to attach at the device output. There are many proposed active negative capacitance circuitries to be used in the fields of microwave circuit design such as active-tunable filters, voltage controlled oscillators, antenna matching network and so on (Kolev et al, 2001; Kaya and Yuksel, 2007; Ghadiri and Moez, 2010). Most of the examples use gyrator-based feedback topologies to implement negative capacitance circuits. However, there is an important restriction on the use of such active circuits at the output of any high power PA. As the voltage may reach up to many ten volts in most cases, it will definitely exceed the negative capacitance circuit active device gate-source breakdown voltage (e.g. for CGH40010F, nominal drain-to-source voltage is 28V which means that the maximum level could reach up to 56V where the maximum gate-to-source breakdown voltage range is given to be -10V to +2V) (Url-2). In addition to this limitation, one another issue to be mentioned here is the PAE degradation and the increased circuit complexity and relatively high-cost of the overall PA design when implementing such additional active circuitries.

Above the given limitations for the use of active networks, passive solutions to implement possible $-B_{T,out}(\omega)$ profile would become both preferable and valuable. Since the characteristic of the $-B_{T,out}(\omega)$ profile given in Figure 5.8 simply resembles to any single shunt inductance characteristics, it is possible to make use of such simple approach to implement desired capacitance profile. Any ideal single-shunt inductance has the input admittance of pure imaginary as

$$Y_{ind}(j\omega) = \frac{1}{j\omega L_{ind}} = -jB_{ind} \qquad \textbf{(5.4)}$$

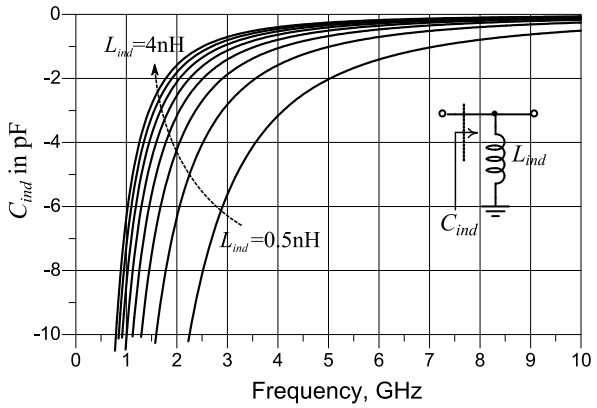


Figure 5.8 : Input capacitance (C_{ind}) of shunted inductance.

where $Y_{ind}(j\omega)$ is equivalent to negative susceptance where B_{ind} and C_{ind} are equal to

$$B_{ind} = \frac{1}{\omega L_{ind}} \qquad \textbf{(5.5)}$$

$$C_{ind} = \frac{B_{ind}}{2\pi f} \qquad \textbf{(5.6)}$$

from the given characteristic, a capacitance profile is seen where the value of the inductance effects the slope of the profile. By adding a positive capacitance, we can have a profile having both negative and positive capacitance values as desired. Figure 5.9 gives the characteristic of such implementation. C_{offset} is the adding capacitance to determine zero passing frequency for the profile.

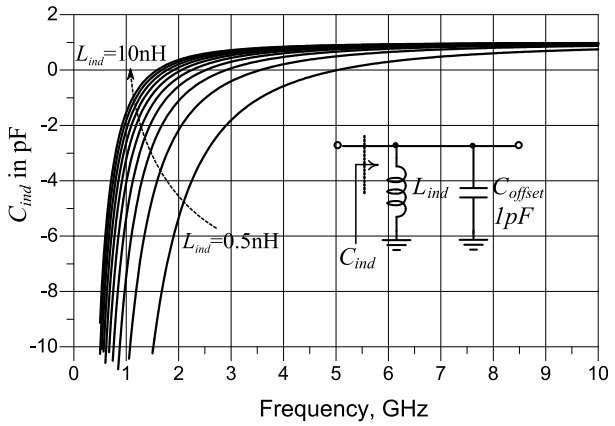


Figure 5.9 : Shifting C_{ind} profile to the positive capacitance side.

From the design perspective of view, any passive inductance could be replaced by a transmission-line based structure such as microstrip line. It is to say that any lossless short-circuited transmission-line could be possibly replaced with the inductance. Input admittance of any short-circuited line could be written as

$$Y_{in,TL}(j\omega) = -j\frac{1}{Z_0}\cot\beta l = -jB_{in,TL} \qquad \textbf{(5.7)}$$

where Z_0 is the line characteristic impedance and βl is the electrical length of the line. Equation (5.7) shows that the line admittance is periodic in l and repeats for $l=n\lambda/2$ where n=1, 2, 3, … As an example, a short circuited microstrip line can be characterized by changing the line length (L) and width (W) (i.e. Z_0 and βl) and results are given in Figure 5.10 and Figure 5.11 respectively.

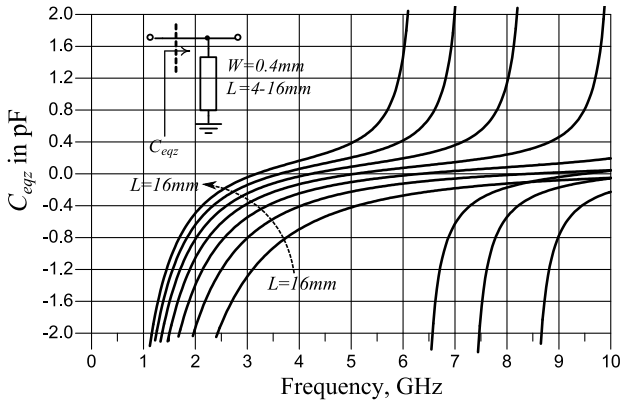


Figure 5.10 : Short circuited transmission line capacitance characteristic where the line-length (L) is selected as the parameter.

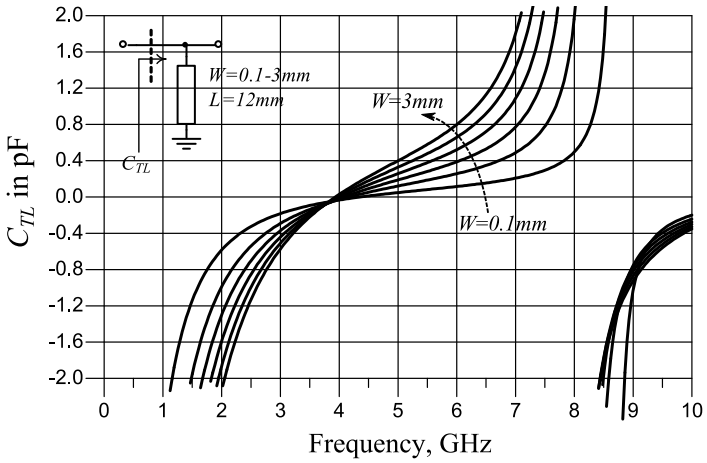


Figure 5.11 : Short circuited transmission line capacitance characteristic where the line-width (W) is selected as the parameter.

Both zero-passing frequency and the slope of the capacitance profile could be controlled by changing the line dimension. Given microstrip structures are simulated using Taconics TSM-DS3 substrate (ε_r=3 and tanδ=0.0011). Overall results show that any short-circuited transmission-line could be useful to present $-jB_{T,out}(\omega)$ profile at the device output to minimize susceptance part. Since the line is short-circuited at one side, using such implementation can also simplify the realization of the biasing network where there is need for additional circuitry to supply drain terminal voltage and current in most cases. That is to say, drain supply voltage can be tied to ac short-circuited side of the line and as a result, there is no need to design additional biasing network. Figure 5.12 shows the $B_{B,in}(\omega)$ circuitry with the included biasing network solution.

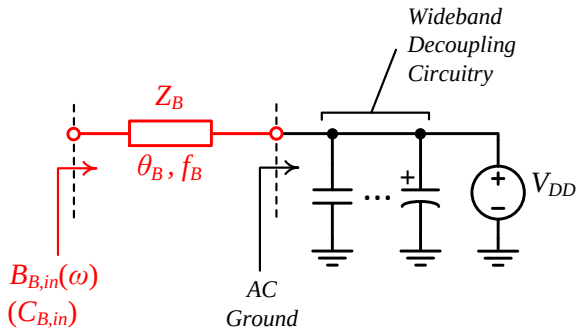


Figure 5.12 : Implementation of $B_{B,in}(j\omega)$ negative susceptance circuitry.

5.1.4 Design of low-Q wideband-matching network

This section will describe the design of remaining low-Q matching network. As mentioned in the previous section, a desired profile of susceptance (or capacitance) could be implemented by using short-circuit terminated transmission-line approach. By doing this, one can obtain a lowered susceptance value at the output node and the need for the wideband match is reduced to design of frequency dependent real conductance only matching problem. In theory, real conductance matching problem is a low-Q matching problem by definition. Thus, wideband real-to-real impedance or admittance transformation is possible with using multisection transformers (e.g. Binomial and Chebyshev multisection transformers) (Pozar, 2001). Output $G_{T,out}(\omega)$ was given in Figure 5.6b is needed to be transformed into 50Ω which is not directly suitable with using well-known multisection transformer methods which are all for constant value of real-impedance or real-admittance transforming purposes. Thus, we need to modify transforming structures to make use of such frequency dependent

conductance to match into a real 50Ω load. A multisection impedance transformer can be represented as shown in Figure 5.13. Given Z_n's are the characteristic impedances, θ_n's are the electrical lengths and Γ_n's are the partial reflection coefficients where n=1, 2, …, N. Overall reflection coefficient $\Gamma_{in}(\theta)$ seen from the input port of the multisection transformer could be approximated by,

$$\Gamma_{in}(\theta) = \Gamma_0 + \Gamma_1 e^{-j2\theta_1} + \Gamma_2 e^{-j2(\theta_1+\theta_2)} + \cdots + \Gamma_N e^{-j2(\theta_1+\cdots+\theta_N)} \qquad \textbf{(5.8)}$$

where the partial reflection coefficients can be defined as follows;

$$\Gamma_0 = \frac{Z_1 - Z_0}{Z_1 + Z_0} \qquad \Gamma_1 = \frac{Z_1 - Z_0}{Z_1 + Z_0} \qquad \cdots \qquad \Gamma_N = \frac{Z_L - Z_N}{Z_L + Z_N} \qquad \textbf{(5.9)}$$

A special case of multisection transformer where assuming all θ_n's are equal to $\lambda/4$ and all Γ_n are arranged in a symmetrical sequence where $\Gamma_0 = \Gamma_N$, $\Gamma_1 = \Gamma_{N-1}$, $\Gamma_2 = \Gamma_{N-2}$ etc. In addition, all Z_n increase or decrease monotonically across the transformer while Z_L is real, then the transformer could be designed as Binomial or Chebyshev type multisection transformer by properly choosing the Z_n impedances (Pozar, 2001). Since the all Γ_n are real for both special cases, these type of matching networks are suitable to match only real and frequency independent impedances which is seems to be useless for transforming $G_{T,out}(\omega)$ into 50Ω. Equation (5.8) could be rewritten in the form of sinusoids as follows;

$$\begin{aligned}\Gamma_{in}(\theta) = \Gamma_0 &+ \Gamma_1\{\cos 2\theta_1 - j\sin 2\theta_1\} \\ &+ \Gamma_2\left\{\cos\left[2(\theta_1+\theta_2)\right] - j\sin\left[2(\theta_1+\theta_2)\right]\right\} \\ &+ \cdots \\ &+ \Gamma_N\left\{\cos\left[2(\theta_1+\theta_2+\cdots+\theta_N)\right] - j\sin\left[2(\theta_1+\theta_2+\cdots+\theta_N)\right]\right\}\end{aligned} \qquad \textbf{(5.10)}$$

which shows that $\Gamma_{in}(\theta)$ could be designed as a complex function by properly choosing θ_n's.

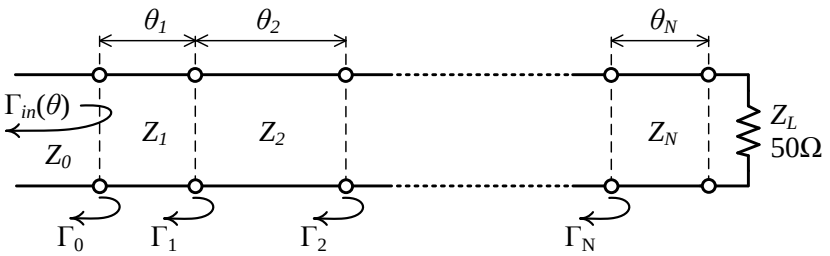


Figure 5.13 : A general representation for multisection matching transformer.

It is possible to realize a complex admittance function $Y_{M,in}(j\omega)$ looking into the multisection transformer as;

$$Y_{M,in}(j\omega) = \frac{1}{Z_0}\frac{1-\Gamma_{in}(\omega)}{1+\Gamma_{in}(\omega)} = G_{M,in}(\omega) + jB_{M,p}(\omega) \quad \textbf{(5.11)}$$

where $B_{M,p}(\omega)$ is the additional parasitic susceptance part of $Y_{M,in}(j\omega)$ contributes to $B_{T,out}(\omega)$ and should also be eradicated from the output. Proper θ_n and Γ_n values could be selected by fitting real $G_{T,out}(\omega)$ function to equation (5.10). Therefore, all Z_n impedance values could be extracted. Figure 5.14 shows the line design parameters for the multisection transformer used in the design.

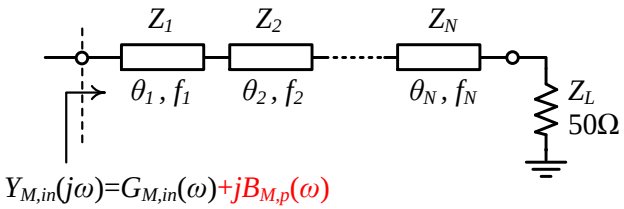


Figure 5.14 : Multisection transformer line parameters and $Y_{M,in}(j\omega)$ input admittance.

5.1.5 Overall design of the output matching network

After inspecting the two main design blocks at the output-matching network, now we could build up a systematic way to complete overall design for wideband impedance matching. Proposed overall design procedure has three main steps to be completed.

Step 1: Design a multisection impedance transformer to obtain

$$G_{M,in}(\omega) = G_{T,out}(\omega) \quad \textbf{(5.12)}$$

After the design is completed, the input admittance of the transformer will be equal to

$$Y_{M,in}(j\omega) = G_{T,out}(\omega) + jB_{M,p}(\omega) \quad \textbf{(5.13)}$$

where a parasitic susceptance $B_{M,p}(\omega)$ arises at the input port of the multisection transformer.

Step 2: After extracting the parasitic contribution of $B_{M,p}(\omega)$ from Step 1 and since $B_{T,out}(\omega)$ is known, it is possible to design a short-circuited line having $B_{B,in}(\omega)$

susceptance at the input to remove the remaining susceptance contribution as follows,

$$\begin{aligned} B_{B,in}(\omega) &= -B_{T,out}(\omega) - B_{M,p}(\omega) \\ &= B_{L,opt}(\omega) - B_{M,p}(\omega) \end{aligned} \quad \textbf{(5.14)}$$

In this point, a parasitic conductance term seen from the input port of the $B_{B,in}(\omega)$ line could be neglected since the value of the conductance is very small.

Step 3: Multisection transformer designed in Step 1 and short-circuited line design in Step 2 is now joined together to complete overall design. Since we have started with $Z_{L,opt}(j\omega)$, A final optimization step is somewhat needed to correct mismatching of $R_{L,opt}(\omega)$ and $X_{L,opt}(\omega)$ since $Z_{L,opt}(j\omega)$ is equal to

$$R_{L,opt}(\omega) = \frac{G_{T,opt}(\omega)}{G_{T,out}^2(\omega) + B_{T,out}^2(\omega)} + j\frac{B_{T,opt}(\omega)}{G_{T,out}^2(\omega) + B_{T,out}^2(\omega)} \quad \textbf{(5.15)}$$

Table 5.2 shows the design parameter values of the proposed structures. Multisection transformer is selected as a four-section transformer monotonically increasing the impedance values. An ac short circuited microstrip line obtaining $B_{B,in}(\omega)$ susceptance is a single segment microstrip line as was indicated in Figure 5.12. Output matching network model for the proposed design methodology is shown in Figure 5.15.

Table 5.2 : Line parameters and microstrip line dimensions for the overall matching network.

Line No.	Z_n Ω	f_n GHz	θ_n Degree	W_n *mm*	L_n *mm*
TL_1	19.3	3.7	90	6.8	12.4
TL_2	27.1	3.5	90	4.5	13.4
TL_3	37.5	3.5	90	2.9	13.5
TL_4	45.6	3.6	90	2.2	13.2
TL_B	27.4	3.9	100	4.4	13.3

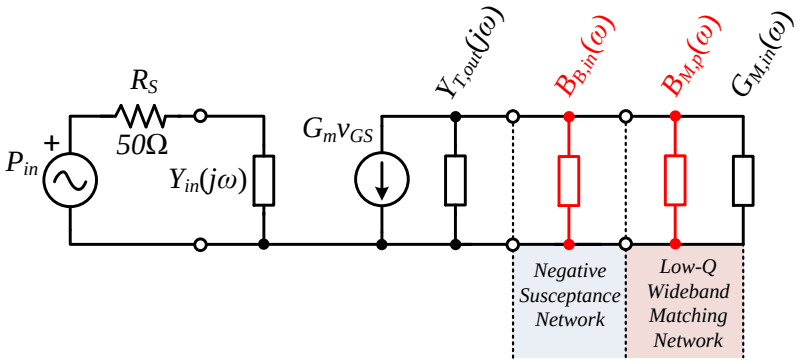


Figure 5.15 : Output matching network model for the proposed design methodology.

5.1.6 Simulation results and comparison

Proposed method is implemented on the design of a wideband output-matching network for the Cree's CGH40010F packaged GaN transistor. Impedance tracking performance of the proposed output stage is drawn in Figure 5.16. Since the aim of this work was to design the output stage, the overall gain of the amplifier is expected to be 10-12dB with using a proper input wideband-matching network. Input $Z_{MB,in}(j\omega)$ impedance of the proposed overall structure could be inspected as the sum of real ($R_{MB,in}(j\omega)$) and imaginary ($X_{MB,in}(j\omega)$) parts given as in Figure 5.17. It is seen that $R_{MB,in}(j\omega)$ is in a good agreement with the $R_{L,opt}(j\omega)$ inside the band and $X_{MB,in}(j\omega)$ has the similar characteristic to $X_{L,opt}(j\omega)$ one which is resulted from the susceptance minimising process.

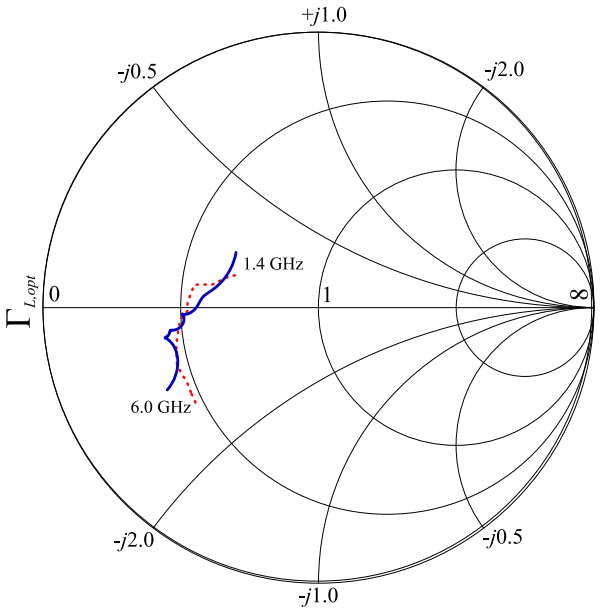


Figure 5.16 : $Z_{L,opt}(j\omega)$ tracking performance (solid-line) of the proposed design method shown on the Γ plane.

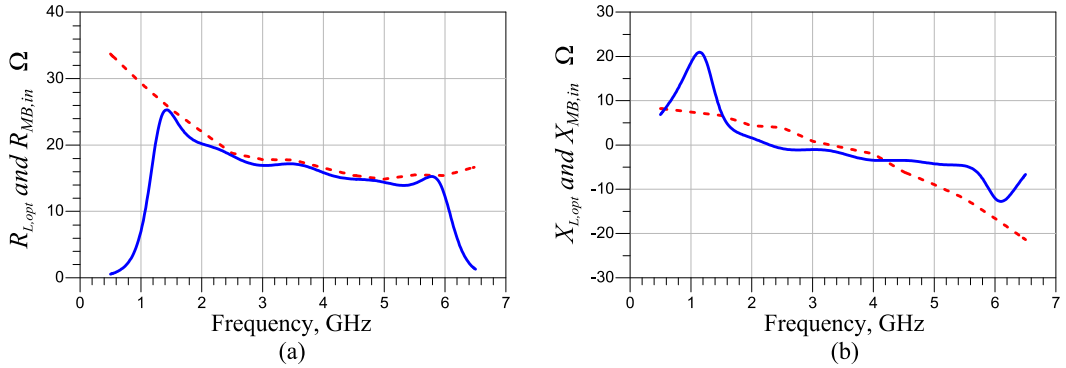


Figure 5.17 : Proposed matching network design input $Z_{MB,in}(j\omega)$ impedance real ($R_{MB,in}(\omega)$) and imaginary ($X_{MB,in}(\omega)$) parts given with the real and imaginary part of $Z_{L,opt}(j\omega)$ impedance (dashed lines).

Mismatch of the lines in figures shows the degradation of the power matching performance of the output network. Output 1dB compression power levels and the corresponding PAE performance is given in Figure 5.18. Output design is shown to deliver over >10W of power in the frequency band of 1.4-to-6GHz and the PAE level appears to be in the range of 44% to 55%.

To compare the tracking performance of the proposed methodology, Chebyshev based direct analytical design of impedance transforming network to transform $Z_{L,opt}(j\omega)$ into 50Ω is implemented using the matching impedance tool of ADS. Orders was selected as n=5, 9 and 13 within the desired band of operation. Additionally, the real-frequency technique is applied to implement transforming network with the order of n=9 and 11 again with using the ADS environment. Tracking performance of the both analytic and real-frequency technique is shown in Figure 5.19a and b respectively in comparison with the proposed method.

To compare the results with the formerly proposed wideband PA structures, a detailed comparison table is given in Table 5.3. Among the given reference designs, proposed method seems to have succeeded the highest PAE performance. This is due to the better $Z_{L,opt}(j\omega)$ tracking performance of the proposed design method where the device is capable of maximum power transfer to given 50Ω. As could be inspected from the results that, the given method is applicable for the design of output stage of PAs since the number of elements to be optimized is only a few with comparing to high order direct analytical design methods where the order of the design means more the elements to be used and more the time is needed for optimizations procedures.

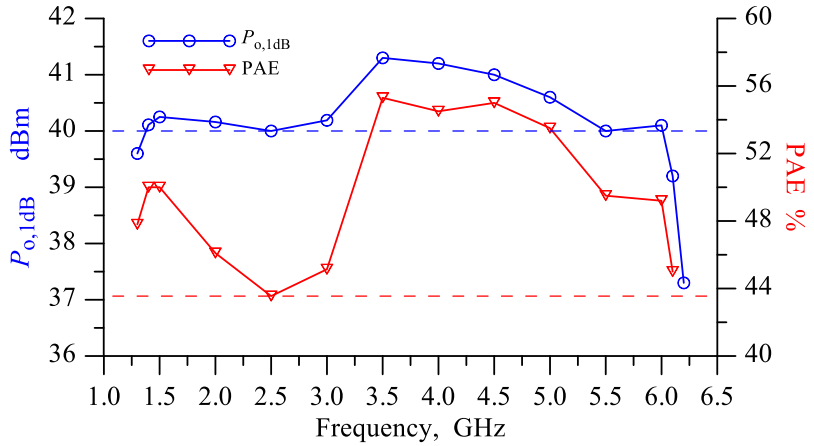
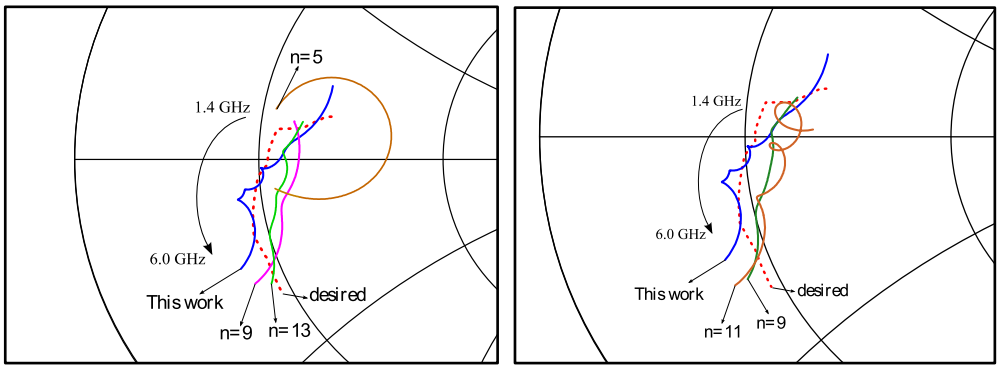


Figure 5.18 : Power and PAE performance of the amplifier output stage.



(a) (b)

Figure 5.19 : Comparative $Z_{L,opt}(j\omega)$ tracking performance of the (a) classical analytic (Chebyshev type) method for n=5, 9 and 13 (b) Real-frequency method for n=9 and 11.

5.1.7 Chapter conclusions

In this study, a design methodology for the output stage is studied where a systematic and step-by-step procedure based on a susceptance minimizing technique is presented. Proposed approach uses short-circuited transmission-line concept to minimize or cancel susceptance contributions at the drain terminal of a discrete GaN HEMT and a multisection transformer line to employ wideband matching purpose.

The method is useful for the packaged type transistors where the output parasitic contribution needed to be canceled out by using an inverse characteristic one. Another usefulness of the proposed technique is the elimination of the additional biasing network at the drain side. This is accomplished by terminating the $B_{B,in}(\omega)$ line with V_{DD} supply, which serves ac short-circuit condition for the line.

As could be inspected from the results that the given method is applicable for the design of output stage of PAs since the number of elements to be optimized is only a

few with comparing to high order direct analytical design methods where the order of the design means more the elements to be used.

Table 5.3 : Comparison of the previously proposed GaN based PA performances.

Reference	Technology	BW (GHz)	BW (%)	$P_{o,1dB}$ (W)	P_{sat} (W)	PAE (%)	DE (%)	Gain (dB)
Ding et al, (2013)	Discrete GaN	2 – 4	67	13.1 – 14.1	–	36.5 – 53.4	–	11.1 – 12.6
Tuffy et al, (2012)	Discrete GaN	1.45 – 2.45	51	11 – 16.8	–	–	70 – 81	10 – 14
Mimis et al, (2012)	Discrete GaN	1.6 – 2.2	32	10	–	–	55 – 68	11 – 12
Chen and Peroulis, (2012)	Discrete GaN	1.3 – 3.3	87	10 – 11	–	–	60 – 83	10 – 14
Demenitroux et al, (2011)	Discrete GaN	1.8 – 2.5	33	10 – 15	–	–	65 – 75	12.5 – 15.5
AlMuhaisen et al, (2011)	Discrete GaN	0.6 – 2.4	120	10	–	–	57 – 75	–
Komiak et al, (2011)	GaN MMIC	1 – 6	143	–	8.2 – 14.5	18 – 46	–	8.4 – 10.6
Carubba et al, (2011)	Discrete GaN	0.55 – 1.1	66	10.5	–	–	>65	9.5 – 12
Narendra et al, (2010)	Discrete GaN	DC – 2	200	15	–	20 – 45	–	37
Saad et al, (2010)	Discrete GaN	1.9 – 4.3	78	10 – 15	–	–	57 – 72	9 – 11
Lin et al, (2009)	Discrete GaN	0.02 – 3	197	–	>5	>27	–	>13.4
Sayed et al, (2009)	Die GaN	0.35 – 8	183	5	–	20 – 30	–	8 – 10
Wright et al, (2009)	Discrete GaN	1.4 – 2.6	60	9 – 11	–	–	60 – 70	11 – 12
Colantonio et al, (2008)	Discrete GaN	0.8 – 4	133	>1.6	–	–	40 – 55	>7
Azam et al, (2008)	Discrete GaN	0.7 – 1.5	73	9 – 10	–	30 – 35	–	11 – 14
This work (Simulation)	**Discrete GaN**	**1.4 – 6**	**124**	**10 – 13.5**	**–**	**44 – 55**	**–**	**10 – 12**

6. CONCLUSIONS AND RECOMMENDATIONS

Design of efficient wideband PA is a very challenging task and this thesis study intended to propose some of the implementation techniques and methods to make possible relaxation on the design procedures. For this purpose, both techniques: load-line and load-pull design of the output network are taken into account. From the circuit topology point of view, the single transistor travelling wave concept is chosen as the best efficient core for the overall PA design where the output termination is removed to improve output power and so the efficiency. In addition to these large-signaling improvements, PA bandwidth is shown to be extended with the help of using series-series feedback and gain flatness improved with the help of lossy input ATL. Besides that, power combining with using parallel design cores is also shown to be useful for power doubling while preserving the operating bandwidth.

In the first phase of study, to verify the simulation results of the proposed load-line techniques, two different and decade bandwidth medium power PAs were designed and fabricated using 0.35μm SiGe HBT technology. The first design (SSTWPA) was a single-stage TWPA employing only a single transistor where the second PA (CSSTWPA) was a cascaded/paralleled version of the SSTWPA. Measurement results of the two PAs were given and shown as closely agree with the simulation results.

In the second phase, the technology is switched to 0.25μm GaAs PHEMT process. A broadband load-pull technique using a graphical design approach and capacitively coupled class-A/AB PA was presented to ensure a predefined power level is delivered to the load in the entire bandwidth. The parasitic capacitance associated with the off-chip RF choke could easily degrade the bandwidth performance and for this reason; an integrated microstrip line is presented and implemented as the RF choke.

In the cascaded version of GaAs PA, a straightforward systematic design is proposed to show how it would simplify the design of cascaded topologies in an efficient and

systematic way meanwhile obtaining high performance on both bandwidth and power/efficiency metrics.

6.1 Contributions and Achievements

In this study, three different technologies are used to implement and realize proposed improvements on the design of wideband PAs. Since the simulation and measurement results verified the most of the improvements, we could summarize the contributions as below;

- In the low to mid power amplifiers, emitter feedback is shown to be useful to increase power×frequency performance.
- By sacrificing the output termination and employing lossy-ATL together, single transistor PA is shown to have flat gain response in the entire bandwidth as it was in the multi transistor case. This core topology is shown to double the output power in a cascaded/paralleled configuration where the bandwidth is still conserved.
- A graphical approach for load-pull design is proposed. By this way, output power is selected above a predefined minimum level and the corresponding power contours could help graphically to select a suitable matching network without using complicated analytic synthesis methods.
- For the biasing aim, an ac shorted transmission-line is proposed to use for wideband RFC purpose.
- A new systematic approach to design cascaded wideband PA is given, which helps to select optimum device size for the design specifications.
- A technique based on a susceptance minimizing concept at the output of discrete GaN HEMT is presented. Proposed approach could help to simplify wideband design by means of computer aided optimizations.

To sum up, this thesis study proposes some design techniques and modifications, which simplifies both the design procedures and circuit complexities. In this respect, output power and the efficiency is improved with the help of simple and reduced number of matching elements, in which both substrate and parasitic losses effects are compansated.

6.2 Future Works

Given in Section 5, a GaN device based susceptance minimizing technique is presented to relax complex wideband-matching problem at the output. The potential advantage of the design is an open issue since the given performance results are based on the simulation results.

Additionally, both power splitter and combiner techniques could be studied and adopted with the base core structures since CSSTWPA is shown to double output power with cascading and paralleling of the cores in together.

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