

**CURRENT DIFFERENCING BUFFERED AMPLIFIER
(CDBA) AND ITS APPLICATIONS**

İTÜ MERKEZ KÜTÜPHANESİ

Demirbaş No: 67827

Sınıflama No:



M.Sc. Thesis by

Muhammed Abdalbaki IBRAHİM, B.Sc.

(F0496Y077)

EL
U2945
13R

Date of Submission: 5 January 1999

Date of Defence Examination: 1 February 1999

Supervisor (Chairman): Prof. Dr. Cevdet ACAR

Members of the Examining Committee: Prof. Dr. Cuneyt GUZELIS

Assistant Prof. Dr. Herman SEDEF

FEBRUARY 1999

**GERİLİM İZLEMELİ AKIM FARK
KUVVETLENDİRİCİSİ (CDBA) VE UYGULAMALI**

YÜKSEK LİSANS TEZİ

Müh. Muhammed Abdulbaki İBRAHİM

(F0496Y077)

Tezin Enstitüye Verildiği Tarih : 5 Ocak 1999

Tezin Savunulduğu Tarih : 1 Şubat 1999

Tez Danışmanı: Prof. Dr. Cevdet ACAR

Diğer Jüri Üyeleri Prof. Dr. Cüneyt GÜZELİŞ

Yar. Doç. Dr. Herman SEDEF

ACKNOWLEDGEMENT

I wish to thank hereby my adviser Prof. Dr. Cevdet Acar for his kind interest and invaluable support to my work.

I also wish to thank my respectful Assistant Prof. Dr. Ali Toker, Assistant Prof. Dr. Herman Sedef, Research Assistant Serdar Ozoguz and my friends, without their help the typing of this thesis would not be possible. I thank especially my family for their encouragement and their trust in me.

January, 1999

M. Abdulbaki Ibrahim

CONTENTS

ABBREVIATIONS LIST OF FIGURES LIST OF SYMBOLS SUMMARY ÖZET

1. INTRODUCTION

2. INTRODUCTION TO CDBA

- 2.1 Circuit Description of CDBA
- 2.2 The Structure of CDBA

3. BASIC BUILDING BLOCKS USING CDBA

- 3.1 Voltage Gain Amplifier
- 3.2 Current Gain Amplifier
 - 3.2.1 First Configuration
 - 3.2.2 Second Configuration
- 3.3 Summing Point Amplifiers
- 3.4 Integrators
 - 3.4.1 Voltage Mode Integrator
 - 3.4.2 Current Mode Integrator
 - 3.4.2.1 First Configuration
 - 3.4.2.2 Second Configuration
- 3.5 Differentiators
 - 3.5.1 Voltage Mode Differentiator
 - 3.5.2 Current Mode Differentiator
 - 3.5.2.1 First Configuration
 - 3.5.2.2 Second Configuration
- 3.6 Inductor Simulator
- 3.7 Implementation of Gyrator
- 3.8 Negative Resistance Generator

4. THE EFFECTS OF THE NON-IDEALITY OF CDBA

- 4.1 Non-Ideality Effects on the Terminal Currents and Voltages
- 4.2 The Behaviour of CDBA at Low Frequencies
- 4.3 The Behaviour of CDBA at High Frequencies
- 4.4 The Cut Off Frequency of CDBA
- 4.5 Non-Ideality Effects on the Current Integrator

5. CDBA-BASED SECOND-ORDER ACTIVE FILTERS

- 5.1 Introduction to Biquad Filters
- 5.2 Realisation of Biquad Filters Using CDBA
 - 5.2.1 Realisation of Biquad Filters in Voltage Mode
 - 5.2.2 Realisation of Biquad Filters in Current Mode
- 5.3 CDBA-Based Biquad Filter Realisation Using MOS Resistors
 - 5.3.1 Suitable MOS Resistor Configurations for CDBA-Based Biquad Filters

6. RESULT AND CONCLUSION	41
6.1 Experimental Results Using PSPICE	41
6.2 Conclusion	42
REFERENCES	43
APPENDIX	45
BIOGRAGHY	48

active-RC	: Active resistor-capacitor circuit
CCII	: Second generation current conveyor
CDBA	: Current differencing buffered amplifier
CFA	: Current feedback amplifier
CM	: Current mode
FDNR	: Frequency dependent negative resistor
IC	: Integrated circuit
MOS	: Metal oxide semiconductor
MRC	: MOS resistive circuit
op-amp	: Operational Amplifier
SMRC	: Simplified MOS resistive circuit
VLSI	: Very large scale integration

LIST OF FIGURES

Fig. 2.1 : Symbol of CDBA	3
Fig. 2.2 : Equivalent circuit of CDBA	3
Fig. 2.3 : Implementation of CDBA using CFAs	4
Fig. 2.4 : Model of CDBA using AD844	5
Fig. 3.1 : Voltage gain amplifier	6
Fig. 3.2 : Current gain amplifier	7
Fig. 3.3 : Second configuration of current gain amplifier	8
Fig. 3.4 : Voltage summing point amplifier	10
Fig. 3.5 : Current summing point amplifier	10
Fig. 3.6 : Voltage mode integrator	11
Fig. 3.7 : Current mode integrator	12
Fig. 3.8 : Second configuration of current mode integrator	13
Fig. 3.9 : Voltage mode differentiator	14
Fig. 3.10 : Current mode differentiator	15
Fig. 3.11 : Second configuration of current mode differentiator	16
Fig. 3.12 : Grounded inductor simulator	18
Fig. 3.13 : Gyrator symbol	19
Fig. 3.14 : Gyrator equivalent circuit	19
Fig. 3.15 : Implementation of gyrator using CDBA	20
Fig. 3.16 : Gyrator simulation	21
Fig. 3.17 : Implementation of FDNR using gyrator	21
Fig. 3.18 : Negative resistance generator circuit	22
Fig. 4.1 : Model of CDBA at low frequencies	25
Fig. 4.2 : Model of CDBA at high frequencies	27
Fig. 4.3 : Current integrator with appearance of CDBA structure	28
Fig. 5.1 : State variable block diagram of complete biquadratic filter	31
Fig. 5.2 : Complete voltage mode biquadratic filter employing CDBA and realising $H(s)$ of eqn. (5.1)	32
Fig. 5.3 : The lowpass filter realising $H(s)$ of eqn. (5.8)	33
Fig. 5.4 : The bandpass filter realising $H(s)$ of eqn. (5.10)	34
Fig. 5.5 : The highpass filter realising $H(s)$ of eqn. (5.12)	34
Fig. 5.6 : Complete current mode biquadratic filter employing CDBAs and realising eqn. (5.1)	35
Fig. 5.7 : The simple circuit that cancels out the non-linearity of MOSFET devices	37
Fig. 5.8 : The simplified MOS resistive circuit (SMRC)	37
Fig. 5.9 : CDBA-based integrator circuit using SMRC	38
Fig. 5.10 : CDBA-based complete voltage mode biquadratic filter realising eqn. (5.1) using SMRC circuits	39
Fig. 5.11 : CDBA-based complete current mode biquadratic filter realising eqn. (5.1) using SMRC circuits	39

LIST OF SYMBOLS

- A constant (typically 0.5 A)
- A constant (typically 0.001)
- Angular frequency
- A constant (typically 0.7 V in our case)
- Pole frequency
- A constant (typically 10^{-6})
- Carrier electric field (V/m) in SiO_2 channel
- Capacitor
- Frequency dependent frequency response
- Cross-section of the channel
- Conductance
- D.C. gain of the transfer function (voltage or current gain)
- Transfer function in s -domain
- Current in s -domain
- Gate voltage
- Aspect ratio of the device
- Quality factor
- Pole quality factor
- Transfer resistance
- Resistor
- Voltage in s -domain
- Admittance in s -domain
- Impedance in s -domain

LIST OF SYMBOLS

γ : A constant (typically $0.5 \frac{1}{V^2}$)

ε : A constant (typically 0.9998)

ω : Angular frequency

Φ_B : A constant (typically 0.7 Volt at room temperature)

ω_p : Pole frequency

ξ : A constant (typically 10^{-6})

μ : Carrier effective mobility in MOSFET channel

C : Capacitor

D : Frequency dependent negative resistance

g : Gyration tranconductance

G : Conductance

H : D.C. gain of $H(s)$ transfer function (voltage or current gain)

$H(s)$: Transfer function in s-domain

I : Current in s-domain

L : Inductor

W/L : Aspect ratio of MOSFET transistor's channel (channel width to length ratio)

Q : Quality factor

Q_p : Pole quality factor

r : Gyration resistance

R : Resistor

V : Voltage in s-domain

Y : Admittance in s-domain

Z : Impedance in s-domain

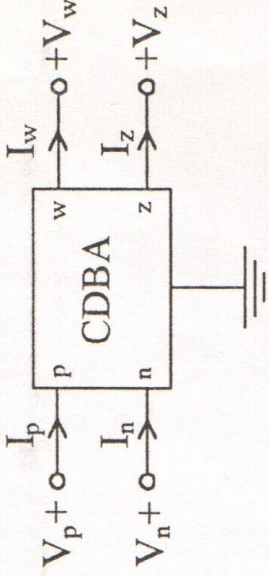
CURRENT DIFFERENCING BUFFERED AMPLIFIER (CDBA) AND ITS APPLICATIONS

SUMMARY

This thesis introduces recently proposed an active element, Current Differencing Buffered Amplifier (CDBA) in order to use in realisation of biquad filters as well as basic building blocks.

In chapter one, the evaluation from the classical filter circuits, through discrete active configurations, to completely integrable single chip continuous time filters is explained shortly.

In chapter two, the Current Differencing Buffered Amplifier (CDBA) is introduced as a grounded four-port network represented by the black box shown below with the four ports denoted by p, n, w, and z.



Symbol of CDBA

The terminal characteristics can be represented best by a hybrid matrix giving the outputs of the four ports in terms of their corresponding inputs as

$$\begin{bmatrix} I_z \\ V_w \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_w \\ I_p \\ I_n \end{bmatrix}$$

It should be noted that all currents and voltages in the equation above are in s-domain.

In addition, the active element CDBA and its equivalent circuit involving dependent sources are given. An implementation of CDBA also is included using commercially available current feedback amplifier (CFA), AD844.

In chapter three, CDBA-based amplifiers in both voltage and current mode are explained. Using CDBAs the realisations of other basic building blocks as integrator, differentiator, inductor simulator, gyrator and negative resistance generator are also described.

in chapter four, the effects of the non-unity gain of the op-amp are given so as to take their effects into account.

In chapter five, the realisation of biquad filters using CDBA is presented based on state variable block diagram. Moreover, the realisation of CDBA-based biquad filters using MOS resistors is presented. It is shown that the active element CDBA is suitable to realise active MOSFET-C filters, i.e., it is suitable to develop controllable fully integrated continuous-time filters.

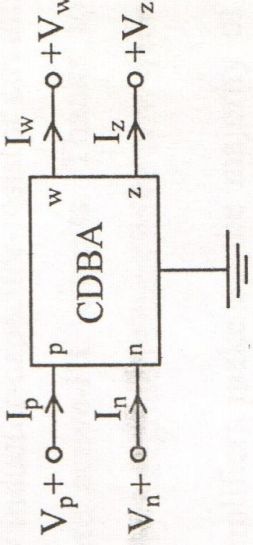
GERİLİM İZLEMELİ AKIM FARK KUVVETLENDİRİCİSİ (CDBA) VE UYGULAMALARI

ÖZET

Temel yapı taşlarını oluşturmak ve ikinci dereceden filtreleri gerçekleştirmek amacıyla bu çalışmada CDBA ile gösterilen son zamanlarda önerilen bir aktif eleman tanıtılmıştır.

Birinci bölümde, klasik filtre devrelerinden ayrık aktif konfigürasyonlardan tam entegre tek çip sürekli-zaman filtrelerine gelişimi kısaca açıklanmıştır.

İkinci bölümde aşağıda simbolü görülen p, n, w, ve z ile ifade edilen, topraklanmış dört-kapılı devre olarak CDBA tanıtılmıştır.



CDBA Simbolü

Dört kapı çıkışının, uygun gelen girişler cinsinden verildiği bir hibrid matrisiyle terminal karakteristikleri

$$\begin{bmatrix} I_z \\ V_w \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_w \\ I_p \\ I_n \end{bmatrix}$$

biçiminde gösterilebilir. Yukarıdaki eşitlikte akım ve gerilimler s-domenindedir. Ayrıca, CDBA aktif elemanı ve CDBA'nın bağımlı kaynaklı eşdeğer devresi verilmiştir. Aynı zamanda, piyasada bulunan akım geribeslemeli kuvvetlendiriciyi, yani CFA yada AD844'ü kullanarak CDBA gerçekleştirilmesi yapılmıştır.

Üçüncü bölümde, gerilim ve akım modundaki CDBA-temelli kuvvetlendiriciler verilmiştir. CDBA kullanarak İntegral alıcı, türev alıcı, endüktans devresi, FDNR devresi, ve negatif direnç devresi gerçekleştirilmiştir.

Dördüncü bölümde, CDBA'nın idealsızlık etkileri tartışılmıştır. İlgili denklemler hesaplamalara katılmak üzere belirtilmiştir.

Beşinci bölümde, CDBA kullanarak durum değişkeni blok diagramıyla ikinci dereceden filtre tasarımı sunulmuştur. Buna ek olarak, MOS dirençleri içeren CDBA-temelli ikinci dereceden filtre tasarımı da verilmiştir. Son olarak CDBA elemanının aktif MOSFET-C filtre tasarımında elverişli olduğu gösterilmiştir.

1. INTRODUCTION

In parallel to the rapid increase of importance of electrical communications in our everyday life, the need for high quality signal processing circuits at reduced cost is continuously growing. Frequency selective filters are essential elements for any signal processing task, and especially continuous time filters are the most prevalent circuits, because most of the communication systems and consumer products are analog designs; even the digital filters need continuous time filtering at their points of connection with the real world, i.e., at the input and the output interfaces.

From the bulky and heavy inductor-capacitor-resistor circuits, continuous time filters have evolved into discrete active-RC circuits. Thanks to the advances in VLSI technology single chip fully integrated filters have now become feasible.

At present operational amplifiers make up the majority of the active filter circuits found in electronic applications in both discrete and monolithic form. Unfortunately, however, for stability reasons the frequencies at which these circuits operate are limited by the op-amps compensation network. This therefore limits voltage op-amps to operate at frequencies 100-500 times less than the unity gain bandwidth of the individual transistors.

Filters using such amplifiers are of course further restricted operating at approximately 10-50 times lower than those of the voltage amplifiers themselves. Moreover, with economic pressures forcing VLSI semiconductor manufactures to pack larger numbers of digital circuits into a given area, they are forced into a situation where IC power supply-voltage levels must be reduced. With analog circuitry on the same chip, reduced voltage supply levels result in reduced daynamic range, thus making analog circuit solutions less attractive than their digital counterparts.

To make greatest use of the available transistor bandwidth, and operate at low voltage supply levels, it has become apparent that analogue signal processing can greatly benefit from processing current signals rather than voltage signals. Besides

of adding, subtracting or multiplying signals represented by currents are simpler to perform than when they are represented by voltages. This also means that the resulting circuits are simpler and require less silicon area.

In the last decade, owing to the well-known advantages of the current mode operation [1], the use of the second-generation current conveyors (CCII's) in many applications has been found beneficial [2]. The advantages of this current mode active element (CCII) have been demonstrated to provide wider bandwidth and better accuracy compared with the conventional op-amps (see [3-4] and the references cited therein). Therefore, it is desirable to develop various analog signal processing circuits, such as analog filtering circuits, amplifiers, and oscillators using CCII with respect to the counterparts of various active filter transfer functions using CCII's have received considerable attention [5-7].

The purpose of this study is to introduce the use of the current differencing buffered amplifier (CDBA) [8] in implementation of basic building blocks and the realisation of biquad filters widely used in analog signal processing systems.

In chapter 2, the active element CDBA and its equivalent circuit involving dependent sources are given. An implementation of CDBA also is included using commercially available current feedback amplifier (CFA), AD844 [9,10].

In chapter 3, the CDBA-based amplifier in both the voltage mode and the current mode is introduced. Using CDBAs the realisations of other basic building blocks as integrator, differentiator, inductor simulator, gyrator, and negative resistance generator are also introduced.

In chapter 4, The effects of the non-ideality of CDBA are presented including its behaviour at low and high frequencies and its cut-off frequency. A real CDBA-based integrator is introduced.

In chapter 5, the realisation of biquadratic filters using CDBA is presented. Moreover, the realisation of CDBA-based biquad filters using MOS resistors is presented. Design outlines are given.

2. INTRODUCTION TO CDBA

In this chapter the active element CDBA and its equivalent circuit involving dependent sources are given. An implementation of CDBA also is included using commercially available current feedback amplifier (CFA), AD844 [9,10].

2.1 Circuit Description of CDBA

The circuit symbol of the active element, CDBA [8], is shown in Fig. 2.1, where (p) and (n) are input terminals and (w) and (z) are output terminals.

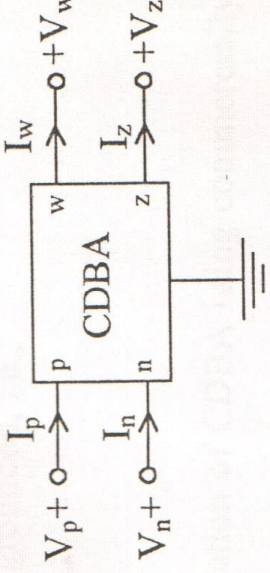


Fig. 2.1 Symbol of CDBA

This element is equivalent to the circuit of Fig. 2.2, which involves dependent current and voltage sources.

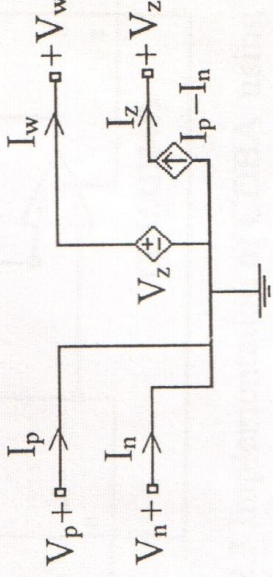


Fig. 2.2 Equivalent circuit of CDBA

The characteristic of CDBA can be modelled as below:

$$\begin{bmatrix} I_z \\ V_w \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ I_w \\ I_p \\ I_n \end{bmatrix} \quad (2.1)$$

According to the above describing equations and equivalent circuit of Fig. 2.2, current through z-terminal (I_z) follows the difference of the currents through p-terminal (I_p) and n-terminal (I_n), and hence z-terminal can be named as current differencing output, i.e.,

$$I_z = I_p - I_n \quad (2.1a)$$

p-terminal also is named as positive (non-inverting) input and n-terminal as negative (inverting) input. Moreover, voltage of w-terminal (V_w) follows the voltage of z-terminal (V_z), i.e.,

$$V_w = V_z \quad (2.1b)$$

Hence w-terminal can be named as voltage output. Finally, note that the input terminals p and n, are grounded, i.e.,

$$V_p = V_n = 0 \quad (2.1c)$$

A possible implementation of CDBA using commercially available CFA, AD844 is given in Fig. 2.3.

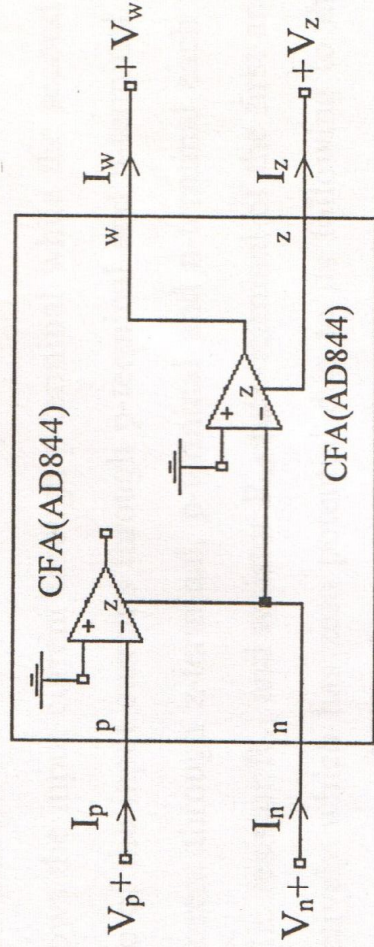


Fig. 2.3 Implementation of CDBA using CFAs.

2.2 The Structure of CDBA

Since the CDBA can be implemented using two CFAs, AD844, using the model of AD844 [9,10] the model of the CDBA can be obtained as shown in Fig. 2.4 below using CCII+s and voltage buffers.

3. BASIC BUILDING BLOCKS USING CDBA

After the introduction of CDBA it's ready now to discuss the basic CDBA blocks that are used to construct active filters. Although it is difficult to identify the function of the CDBA basic blocks in terms of the elementary operations to be treated in this chapter, in many cases it is readily apparent that this active element will be used to amplify signals, to sum signals, or to simulate the behaviour of inductors and/or capacitors. The latter is accomplished either by integrating a signal, i.e., by an operational simulation of the function of inductors and capacitors or by building a circuit whose impedance "looks" like that of an inductor [11].

3.1 Voltage Gain Amplifier

Fig. 3.1 shows a voltage gain amplifier implemented using CDBA. This circuit involves one CDBA and three resistors.

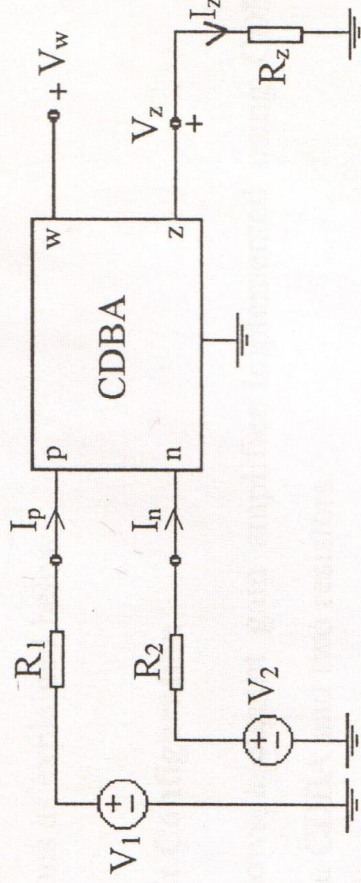


Fig. 3.1 Voltage gain amplifier

The following equations can be written for this circuit:

$$V_z = I_z R_z \quad (3.1)$$

$$V_w = V_z = (I_p - I_n) R_z \quad (3.1a)$$

$$I_p = \frac{V_1}{R_1} \quad (3.2)$$

$$I_n = \frac{V_2}{R_2} \quad (3.3)$$

These equations give the following input- output relation:

$$V_w = \frac{R_z}{R_1} V_1 - \frac{R_z}{R_2} V_2 \quad (3.4)$$

As seen from equation (3.4) non-inverting voltage gain can be obtained by setting $V_2=0$:

$$V_w = \frac{R_z}{R_1} V_1 \quad (3.4a)$$

Similarly inverting voltage gain can be obtained by setting $V_1=0$:

$$V_w = - \frac{R_z}{R_2} V_2 \quad (3.4b)$$

3.2 Current Gain Amplifier

Current gain amplifier also can be implemented using CDBA. It has got two configurations as explained below.

3.2.1 First Configuration

Fig. 3.2 shows a current gain amplifier implemented using CDBA. This circuit involves one CDBA and two resistors.

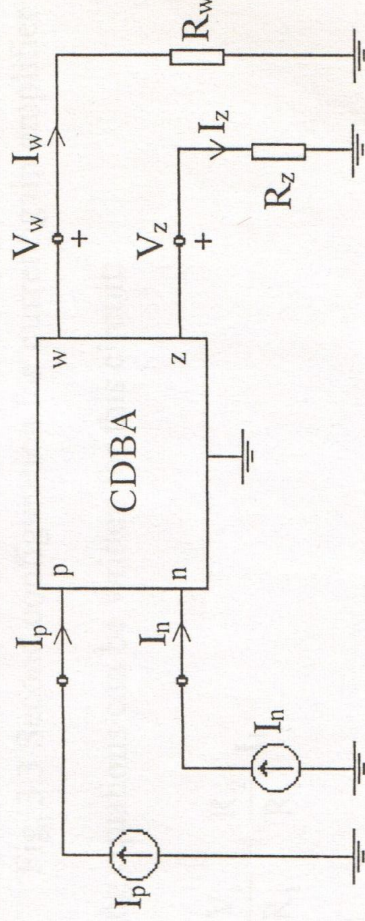


Fig. 3.2 Current gain amplifier

The following equations can be written for this circuit:

$$I_w = (I_p - I_n) \frac{R_z}{R_w} = \frac{R_z}{R_w} I_p - \frac{R_z}{R_w} I_n \quad (3.6)$$

Equation (3.6) yields non inverting current gain by setting $I_n=0$ and yields inverting current gain by setting $I_p=0$ as shown below:

$$I_w = \frac{R_z}{R_w} I_p \quad (\text{non-inverting current gain}) \quad (3.6a)$$

$$I_w = - \frac{R_z}{R_w} I_n \quad (\text{inverting current gain}) \quad (3.6b)$$

3.2.2 Second Configuration

Another configuration of current gain amplifier is shown in Fig 3.3 in which the effect of the parasitic admittance at z-terminal is eliminated by grounding this terminal. This circuit uses one CDBA, four resistors and two buffers.

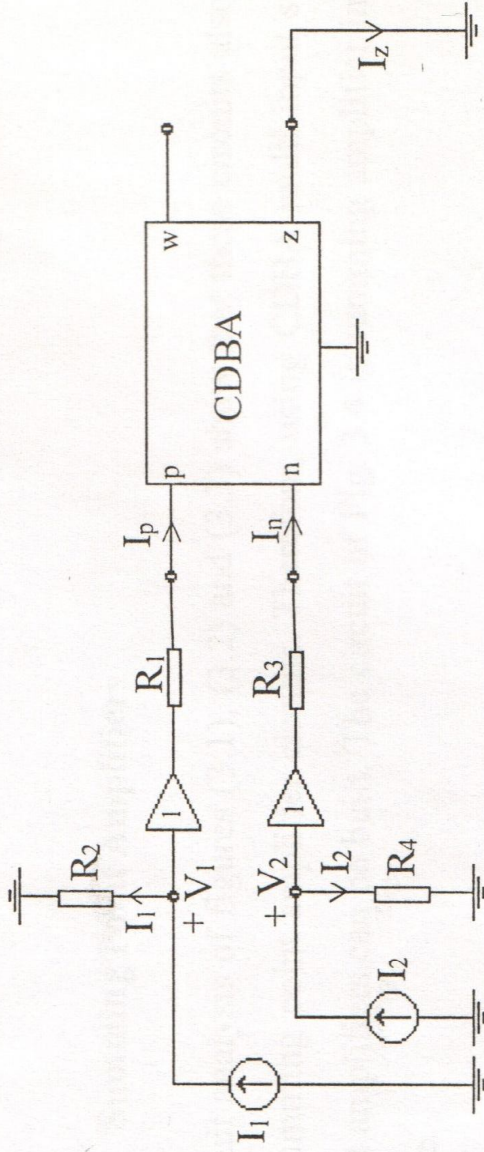


Fig. 3.3 Second configuration for current gain amplifier

The following equations can be written for this circuit:

$$I_p = \frac{V_1}{R_1} = \frac{R_2}{R_1} I_1 \quad (3.7)$$

$$I_n = \frac{V_2}{R_3} = \frac{R_4}{R_3} I_2 \quad (3.8)$$

which yield

$$I_z = \frac{R_2}{R_1} I_1 - \frac{R_4}{R_3} I_2 \quad (3.9)$$

This means that non-inverting current gain can be obtained for $I_2=0$, and inverting current gain for $I_1=0$:

$$I_z = \frac{R_2}{R_1} I_1 \text{ (non-inverting current gain)} \quad (3.9a)$$

$$I_z = - \frac{R_4}{R_3} I_2 \text{ (inverting current gain)} \quad (3.9b)$$

By removing the two buffers shown in the figure above, it can be obtained that:

$$I_z = \frac{R_2}{R_2 + R_1} I_1 - \frac{R_4}{R_4 + R_3} I_2 \quad (3.9c)$$

Both the coefficients $\frac{R_2}{R_2 + R_1}$ and $\frac{R_4}{R_4 + R_3}$ are less than one, therefore, there is no gain and attenuation appears at the output.

3.3 Summing Point Amplifiers

Circuit analysis of figures (3.1), (3.2) and (3.3) show that these circuits also behave as summing point amplifier circuits. Therefore, using CDBA multi input summing point amplifiers can be built. The circuit of Fig. 3.4 is summing amplifier in voltage mode.

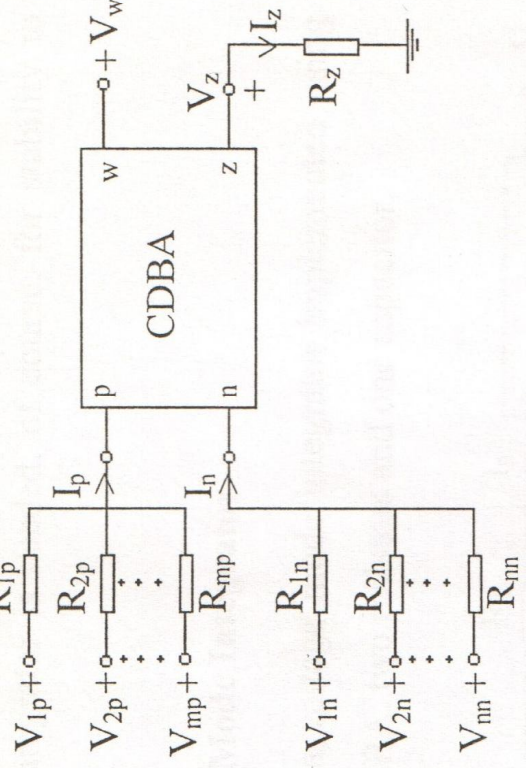


Fig. 3.4 Voltage summing point amplifier

The following equation can be written for this circuit:

$$V_w = \left(V_{1p} \frac{R_z}{R_{1p}} + V_{2p} \frac{R_z}{R_{2p}} + \dots + V_{mp} \frac{R_z}{R_{mp}} \right) - \left(V_{1n} \frac{R_z}{R_{1n}} + V_{2n} \frac{R_z}{R_{2n}} + \dots + V_{nn} \frac{R_z}{R_{nn}} \right) \quad (3.10)$$

The circuit of Fig. 3.5 below shows current summing point amplifier.

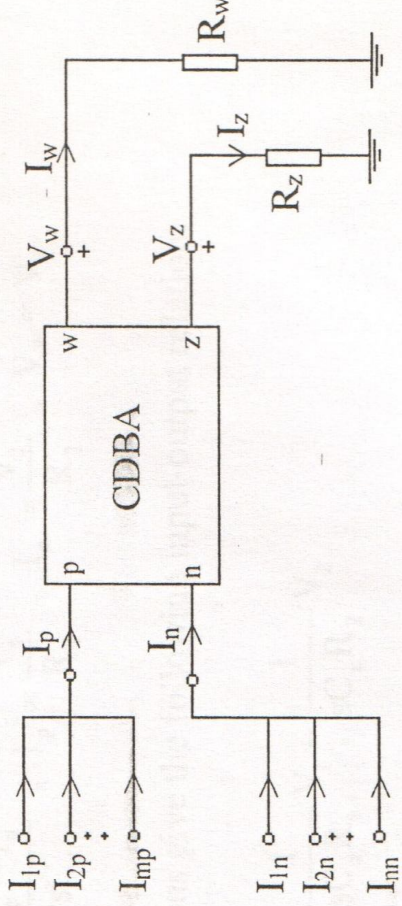


Fig. 3.5 Current summing point amplifier

The following equation can be written for this circuit

$$I_w = (I_{1p} + I_{2p} + \dots + I_{mp}) \frac{R_z}{R_w} - (I_{1n} + I_{2n} + \dots + I_{nn}) \frac{R_z}{R_w} \quad (3.11)$$

3.4 Integrators

Integrators perform an important function in active filter work; not only can they simulate the performance of inductors and capacitors, but they are also used to build second-order filter sections by connecting two integrators in a loop. Combining an

The inverting integrator is needed, of course, for stability to make the loop gain negative.

3.4.1 Voltage Mode Integrator

Fig. 3.6 shows a voltage mode integrator implemented using CDBA. This circuit contains one CDBA, two resistors and one capacitor.

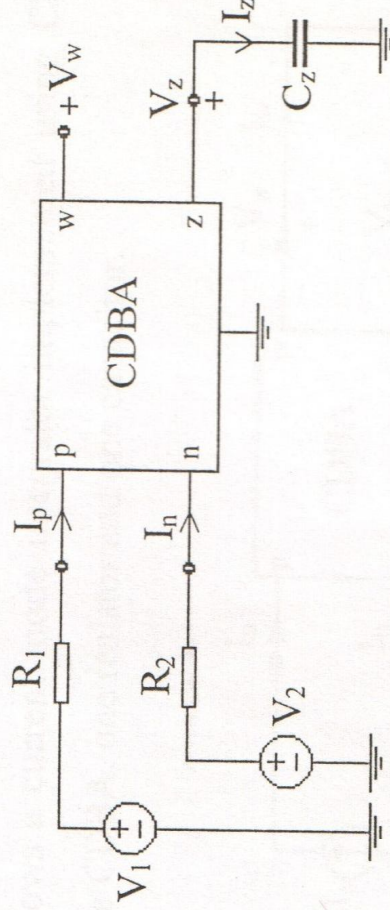


Fig. 3.6 Voltage mode integrator

Circuit analysis yields the following set of equations:

$$V_z = \frac{I_p - I_n}{sC_z}, \quad I_p = \frac{V_1}{R_1}, \quad I_n = \frac{V_2}{R_2}, \quad V_w = V_z \quad (3.12)$$

These equations give the following input-output relation:

$$V_w = \frac{1}{sC_z R_1} V_1 - \frac{1}{sC_z R_2} V_2 \quad (3.13)$$

$$\text{If } V_2 = 0 \text{ then } V_w = \frac{1}{sC_z R_1} V_1 \quad (3.13a)$$

and the circuit behaves as non-inverting voltage mode integrator.

$$\text{If } V_1 = 0 \text{ then } V_w = -\frac{1}{sC_z R_2} V_2 \quad (3.13b)$$

and the circuit behaves as inverting voltage mode integrator.

From the equations it can be seen that the output voltage is the difference of the

negative integrator of the input voltage connected to the p-terminal or the n-terminal respectively.

3.4.2 Current Mode Integrator

Current mode integrator also can be implemented using CDBA. It has got two configurations as explained below.

3.4.2.1 First Configuration

Fig. 3.7 shows a current mode integrator implemented using CDBA. This circuit contains one CDBA, one resistor and one capacitor.

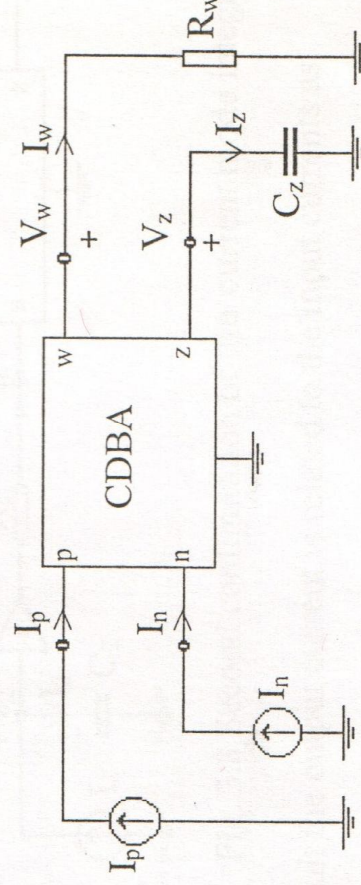


Fig. 3.7 Current mode integrator

Circuit analysis yields the following equation:

$$I_w = \frac{I_p - I_n}{sC_z R_w} \quad (3.14)$$

$$\text{If } I_n = 0 \text{ then } I_w = \frac{I_p}{sC_z R_w} \quad (3.14a)$$

and the circuit behaves as non-inverting current mode integrator.

$$\text{If } I_p = 0 \text{ then } I_w = -\frac{I_n}{sC_z R_w} \quad (3.14b)$$

and the circuit behaves as inverting current mode integrator.

From the equations it can be seen that the output current is the difference of the integrated input currents. It can also be seen that the circuit behaves as a positive or a negative integrator of the input current connected to the p-terminal or the n-terminal

respectively. Note that the number of passive elements used is less in the proposed current mode integrator than in proposed voltage integrator.

3.4.2.2 Second Configuration

Another configuration of current mode integrator is shown in Fig. 3.8 in which the effect of the parasitic admittance at z-terminal is eliminated by grounding this terminal. This circuit uses one CDBA, two resistors, two capacitors and two buffers.

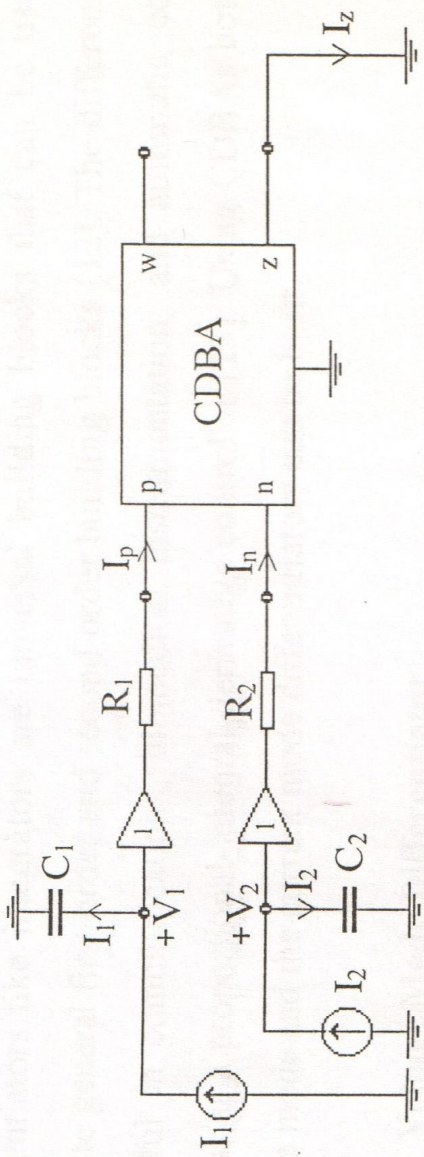


Fig. 3.8 Second configuration of the current mode integrator

In this circuit the output current is related to the input currents as:

$$I_z = \frac{1}{sC_1R_1}I_1 - \frac{1}{sC_2R_2}I_2 \quad (3.15)$$

$$\text{If } I_2 = 0 \text{ then } I_z = \frac{1}{sC_1R_1}I_1 \quad (3.15a)$$

and the circuit behaves as non-inverting current mode integrator.

$$\text{If } I_1 = 0 \text{ then } I_z = -\frac{1}{sC_2R_2}I_2 \quad (3.15b)$$

and the circuit behaves as inverting current mode integrator.

By removing the two buffers shown in figure above the following result can be obtained:

$$I_z = \frac{1}{\frac{1}{sC_1} + R_1}I_1 - \frac{1}{\frac{1}{sC_2} + R_2}I_2 \quad (3.16)$$

Note that both of the terms $\frac{sC_1}{1 + R_1 sC_1}$ and $\frac{sC_2}{1 + R_2 sC_2}$ are less than one, therefore, a

lossy integrator can be obtained.

3.5 Differentiators

Differentiators like integrators are universal building blocks that can be used to generate general first order and second order building blocks [12]. The differentiator is useful in communications, biomedical instrumentation, and automatic control systems as a proportional-integral-derivative controller [13]. Using CDBAs both the voltage mode and the current mode differentiators can be built.

3.5.1 Voltage Mode Differentiator

Fig. 3.9 shows a voltage mode differentiator implemented using CDBA. This circuit uses one CDBA, one resistor and two capacitors.

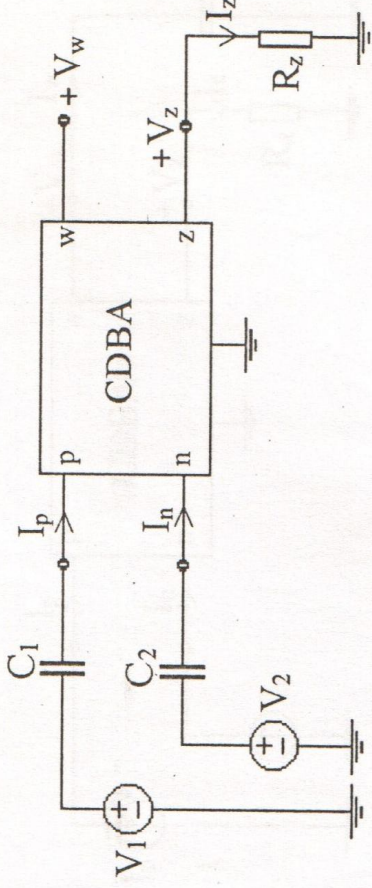


Fig. 3.9 Voltage mode differentiator

Circuit analysis yields the following set of equations:

$$V_z = \frac{I_p - I_n}{R_z}, \quad I_p = sC_1 V_1, \quad I_n = sC_2 V_2 \quad (3.17)$$

These equations give the following input-output relation:

$$V_w = sC_1 R_z V_1 - sC_2 R_z V_2 \quad (3.18)$$

$$\text{If } V_2 = 0 \text{ then } V_w = sC_1 R_z V_1 \quad (3.18a)$$

And the circuit behaves as non-inverting voltage mode differentiator.

$$\text{If } V_1 = 0 \text{ then } V_w = -sC_2 R_z V_2 \quad (3.18b)$$

And the circuit behaves as inverting voltage mode differentiator.

From the above equations it can be seen that the output voltage is the difference of the differentiated input voltages. It can also be seen that the circuit behaves as a positive or a negative differentiator of the input voltage connected to the p-terminal or the n-terminal respectively

3.5.2 Current Mode Differentiator

Current mode differentiator also can be implemented using CDBA. It has got two configurations as explained below.

3.5.2.1 First Configuration

Fig. 3.10 shows a current mode differentiator implemented using CDBA. This circuit involves one CDBA, one resistor and one capacitor.

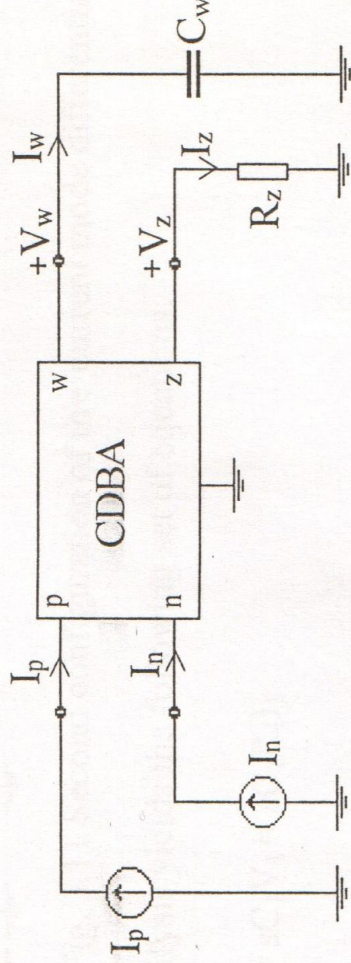


Fig. 3.10 Current mode differentiator

The input-output relation of this circuit is:

$$I_w = sC_w R_z I_p - sC_w R_z I_n \quad (3.19)$$

$$\text{If } I_n = 0 \text{ then } I_w = sC_w R_z I_p \quad (3.19a)$$

and the circuit behaves as non-inverting current mode differentiator.

$$\text{If } I_p = 0 \text{ then } I_w = -sC_w R_z I_n \quad (3.19b)$$

and the circuit behaves as inverting current mode differentiator.

the differentiated input currents. It can also be seen that the circuit works as a positive or negative differentiator of the input current connected to the p-terminal or the n-terminal respectively.

3.5.2.2 Second Configuration

Another configuration of the current mode differentiator is shown in Fig. 3.11 in which the effect of the parasitic admittance at z-terminal is eliminated by grounding this terminal. In this circuit one CDBA, two resistors, two capacitors and two buffers are used.

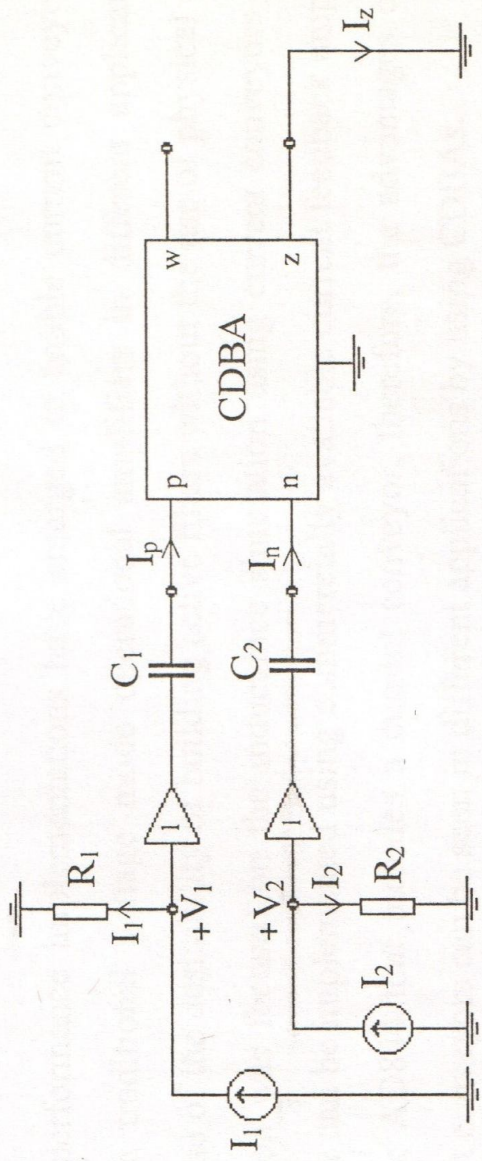


Fig. 3.11 Second configuration of the current mode differentiator

Circuit analysis yields the following set of equations:

$$I_p = sC_1 V_1 = sC_1 R_1 I_1 \quad (3.20)$$

$$I_n = sC_2 V_2 = sC_2 R_2 I_2 \quad (3.21)$$

which give

$$I_z = sC_1 R_1 I_1 - sC_2 R_2 I_2 \quad (3.22)$$

$$\text{If } I_2 = 0 \text{ then } I_z = sC_1 R_1 I_1 \quad (3.22a)$$

and the circuit behaves as non-inverting voltage mode differentiator.

$$\text{If } I_1 = 0 \text{ then } I_z = -sC_2 R_2 I_2 \quad (3.22b)$$

and the circuit behaves as inverting voltage mode differentiator.

By removing the two buffers shown in the figure above the following result can be obtained:

$$I_z = \frac{sC_1R_1}{sC_1R_1 + 1}I_1 - \frac{sC_2R_2}{sC_2R_2 + 1}I_2 \quad (3.23)$$

Note that both of the coefficients $\frac{sC_1R_1}{sC_1R_1 + 1}$ and $\frac{sC_2R_2}{sC_2R_2 + 1}$ are less than one, therefore, there is no gain and attenuation appears at the output.

3.6 Inductor Simulator

High performance implementations have emerged to enable current conveyors to replace traditional voltage mode operational amplifiers in different applications. Because of the desirability of building active filters without the use of physical coils, attention was focused on the inductance simulation using current conveyors [14]. CDBA can be implemented using commercially available current feedback amplifier (CFA); AD844 that includes a current conveyor, therefore, the advantages of the current conveyors can be seen in different applications by using CDBAs.

A configuration of the grounded inductor simulator circuit is shown in Fig. 3.12. The disadvantage of this circuit is that the simulated inductance is not a pure inductor.

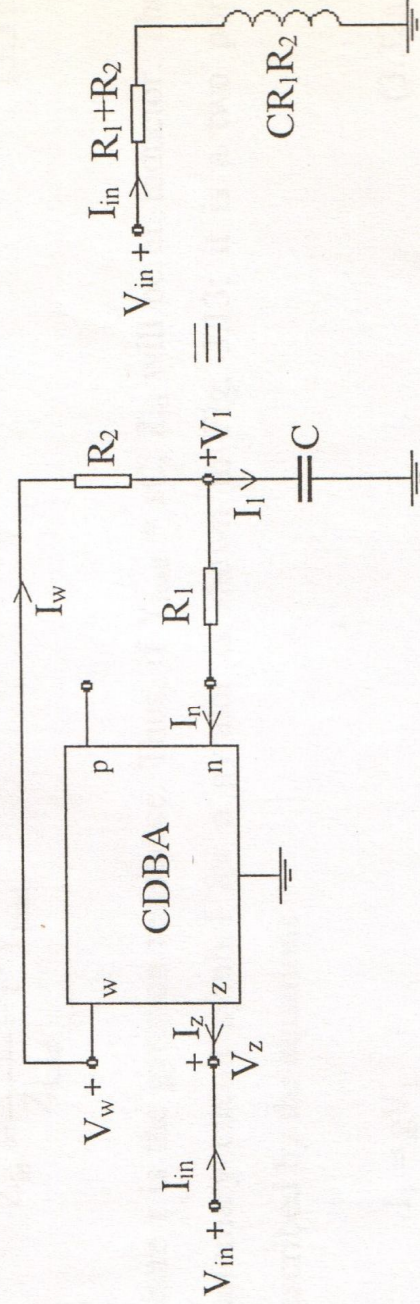


Fig. 3.12 Grounded inductor simulator

Describing equations of this circuit are:

$$V_{in} = V_z = V_w \quad (3.24)$$

$$sCR_2 + \frac{R_2}{R_1} + 1$$

$$I_n = \frac{1}{sCR_1R_2 + R_1 + R_2} V_{in} \quad (3.26)$$

$$I_{in} = -I_z = I_n \quad (3.27)$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = sCR_1R_2 + (R_1 + R_2) \quad (3.28)$$

which behaves as a lossy inductor.

$$\text{If } \omega CR_1R_2 \gg (R_1 + R_2) \text{ is chosen then } Z_{in} \cong sCR_1R_2 \cong sL \quad (3.29)$$

where

$$L = CR_1R_2 \quad (3.30)$$

3.7 Implementation of Gyrator

The best known method for inductor simulation is probably that of using a gyrator. A gyrator is a two port whose input impedance equals

$$Z_{in} = \frac{r^2}{Z_{load}} = r^2 Y_{load} \quad (3.31)$$

where r is the gyration resistance. Thus, if $Y_{load} = sC$, Z_{in} will be an inductor. The customary circuit symbol for a gyrator is shown in Fig. 3.13; it is a two port described by the equations

$$I_1 = gV_2 \quad (3.32a)$$

$$I_2 = -gV_1 \quad (3.32b)$$

$$Z_{in} = \frac{V_1}{I_1} = \left(-\frac{I_2}{V_2} \right) \frac{1}{g^2} = \frac{Y_{load}}{g^2} \quad (3.33)$$

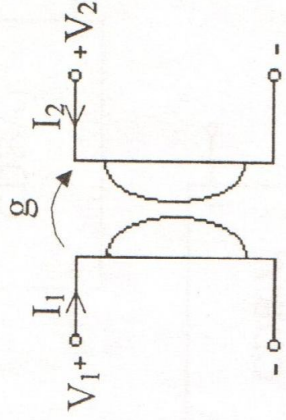


Fig. 3.13 Gyrator symbol

Normally, one attempts to construct the two ports such that the gyrator does not introduce any (parasitic) frequency dependence of its own as shown in gyrator equivalent circuit shown in Fig. 3.14. Further, to obtain the relationship of equation (3.31), frequently the gyrator is designed such that $g = 1/r$.

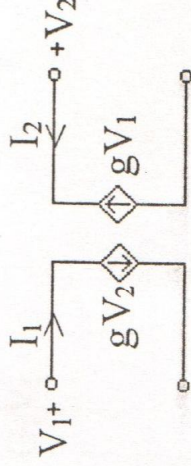


Fig. 3.14 Gyrator equivalent circuit

It is evident from equations (3.32a) and (3.32b) and Fig. 3.14 that gyrator operation is inherently based on transconductances, i.e., the design of such devices is accomplished easily by use of voltage-controlled current source [11]. The required design can be achieved using the advantage of CDBA which can be used as voltage-controlled current source by connecting its input terminal (p-terminal or n-terminal) to the voltage source and taking the output from z-terminal as a current source depending on the input current which is controlled by the voltage source.

Fig. 3.15 shows a gyrator implemented using CDBA. This circuit uses two CDBAs and two resistors by setting $G_1 = G_2 = g$.

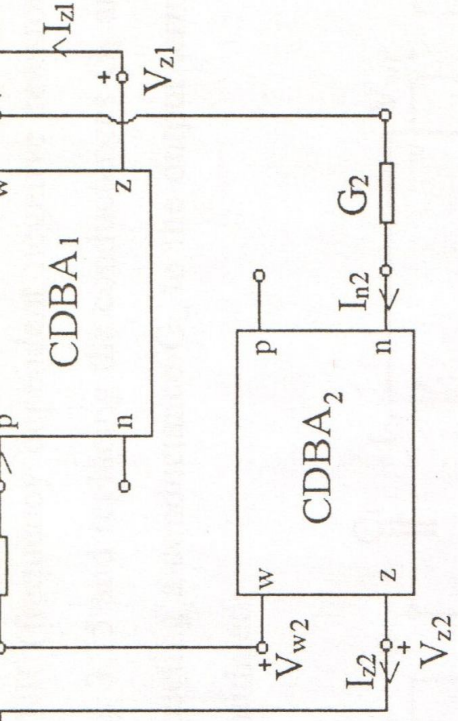


Fig. 3.15 Implementation of gyrator using CDBAs

Circuit analysis yields the following equations:

$$V_{w1} = V_{z1} = V_2, \quad V_{w2} = V_{z2} = V_1 \quad (3.34)$$

$$I_{p1} = G_1 V_{w2} = G_1 V_2 = G_1 V_1 \quad (3.35)$$

$$I_{z1} = I_{p1} = G_1 V_1 = -I_2 \quad (3.36)$$

$$I_{n2} = G_2 V_{w1} = G_2 V_{z1} = G_2 V_2 \quad (3.37)$$

$$I_{z2} = -I_{n2} = -G_2 V_2 = -I_1 \quad (3.38)$$

Because most electronic gyrator designs have a common ground connection between input and output ports as shown in Fig. 3.16a, the simulated inductor will be grounded. A floating gyrator (with no common ground connection) is difficult to build; therefore, to simulate a floating inductor one usually resorts to cascading two grounded gyrators and a capacitor as illustrated in Fig. 3.16b [11].

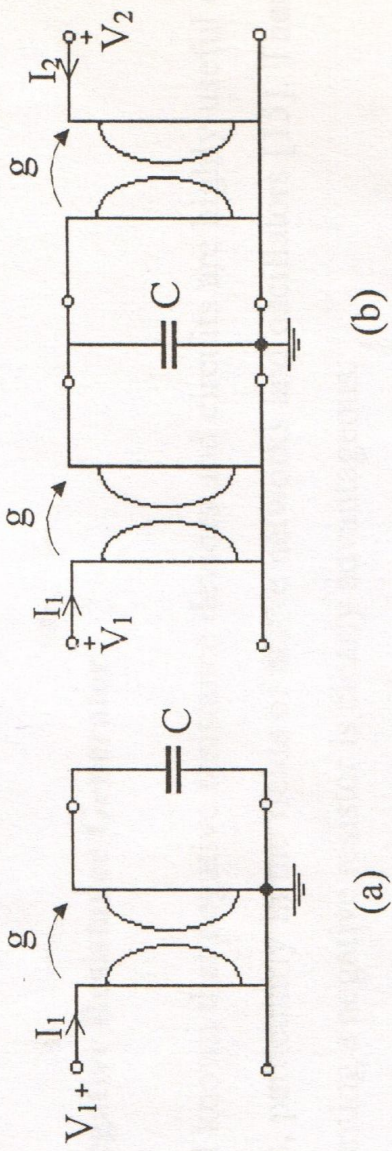


Fig. 3.16 Gyrator simulation of (a) grounded inductor; (b) floating inductor

methods is the FDNR (frequency dependent negative resistor). Using the gyrator circuit shown in Fig. 3.15 and replacing the conductances G_1 and G_2 with capacitors C_1 and C_2 and connecting a conductance G_L to the output terminal as shown below an FDNR can be simulated:

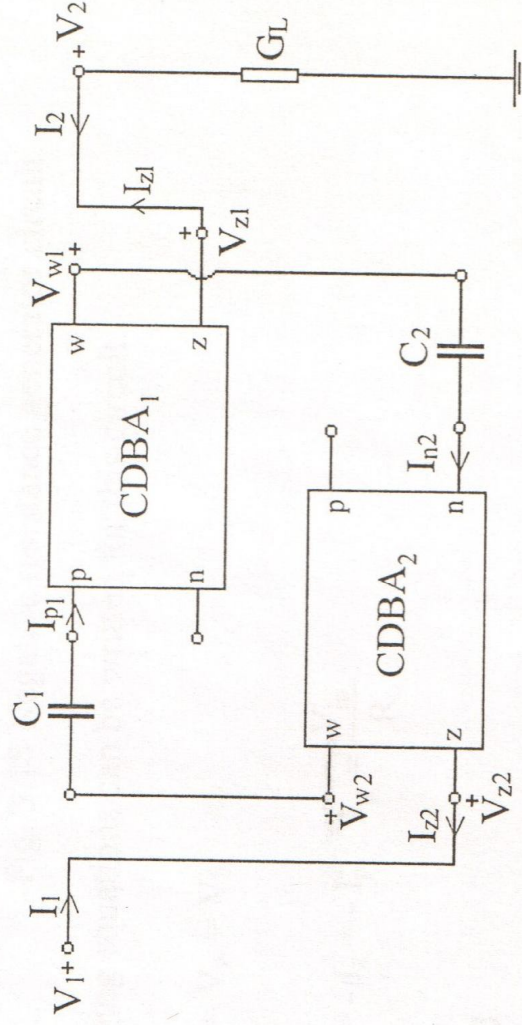


Fig. 3.17 Implementation of FDNR using gyrator

Using the gyrator impedance equation in (3.33) the following equations can be written for this circuit:

$$Y_{in} = \frac{Y_1 Y_2}{Y_L} = \frac{s^2 C_1 C_2}{G_L} = s^2 D \quad (3.39)$$

where

$$D = \frac{C_1 C_2}{G_L} \quad (3.40)$$

3.8 Negative Resistance Generator

It is well known that negative resistance devices and circuits are highly useful circuit elements, particularly in the fields of active networks and oscillators [15]. Therefore, implementing a negative resistor is clearly advantageous.

The realisation scheme for a negative resistance generator is shown in Fig. 3.18. This circuit involves one CDBA and one resistor.

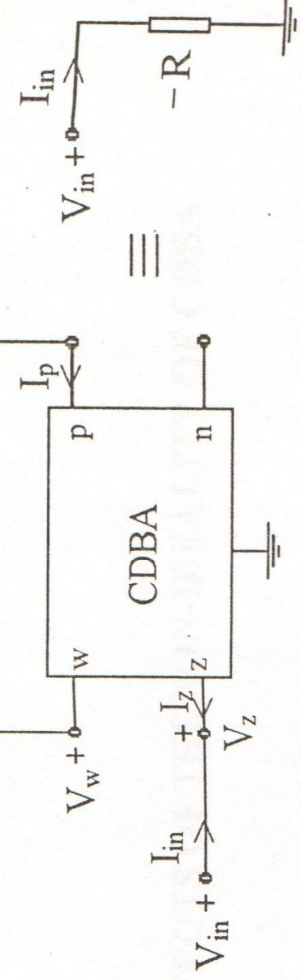


Fig. 3.18 Negative resistance generator circuit.

The following equations can be written for this circuit:

$$V_z = V_w = V_{in} \quad (3.41)$$

$$I_{in} = -I_z = -I_p, \quad I_p = \frac{V_{in}}{R} \quad (3.42)$$

which yield

$$Z_{in} = \frac{V_{in}}{I_{in}} = -R \quad (3.43)$$

4. THE EFFECTS OF THE NON-IDEALITY OF CDBA

In the realisation of the basic building blocks it is assumed that the CDBA shown in Fig. 2.1 is a linear component, and in the ideal case it is defined using the equations (2.1a), (2.1b) and (2.1c). In practice, CDBA as the other types of op-amps and active elements is an electronic circuit, composed of many transistors, resistors and capacitors. Consequently, their input and output impedances can not in general be expected to be zero or infinite, respectively, and their gain and bandwidth must be finite and not infinite as assumed for the ideal model. Because an exact representation of the electronic CDBA circuit would be too complicated to handle, it is still necessary to develop an approximate model, but one that contains all relevant CDBA imperfections with sufficient accuracy to permit realistic predictions of CDBA and active filter behaviour. A suitable circuit is shown in Fig. 2.4, and typical parameters are named there.

4.1 Non-Ideality Effects on the Terminal Currents and Voltages

As seen from the model of CDBA shown in Fig. 2.4, the input voltages are not actually zero, therefore, the following equation can be written for the voltage of p-terminal:

$$V_p = I_p R_{x1} \quad (4.1)$$

By substituting the value of R_{x1} the above equation becomes

$$V_p = 50 I_p \quad (4.1a)$$

Let $V_p \ll \xi$ be chosen then the current equation of p-terminal becomes:

$$I_p \leq \frac{\xi}{R_{x1}} \quad (4.1b)$$

where ξ is a very small value. For $\xi = 10^{-6}$ the last equation becomes:

And the following equations can be written for the voltage of n-terminal

$$V_n = I_{x2} R_{x2} \quad (4.2)$$

The current I_{x2} can be expressed by doing circuit analysis on the circuit of Fig. 2.4 as:

$$I_{x2} = (I_n - I_p) \frac{\frac{1}{sC_{z1} + \frac{1}{R_{z1}}}}{\frac{1}{sC_{z1} + \frac{1}{R_{z1}}} + R_{x2}} \quad (4.3)$$

By substituting the value of I_{x2} in equation (4.2) it becomes

$$V_n = (I_n - I_p) \frac{\frac{1}{sC_{z1} + \frac{1}{R_{z1}}}}{\frac{1}{sC_{z1} + \frac{1}{R_{z1}}} + R_{x2}} R_{x2} \quad (4.4)$$

In order to obtain the output current of z-terminal (I_z) a load of Z_z can be connected to this terminal, and the current can be expressed as.

$$I_z = -I_{x2} \frac{1}{1 + sC_{z2}Z_z + \frac{Z_z}{R_{z2}}} \quad (4.5)$$

By substituting the value of I_{x2} in the last equation and by doing some algebra it becomes

$$I_z = (I_p - I_n) \frac{1}{1 + \frac{R_{x2}}{R_{z1}} + sC_{z1}R_{x2}} \times \frac{1}{1 + \frac{Z_z}{R_{z2}} + sC_{z2}Z_z} \quad (4.5a)$$

It is known that the ratio $\frac{R_{x2}}{R_{z1}} \ll 1$ (as given in the data of [10]). If $\frac{|z1|}{R_{z2}} \ll 1$,

$\omega C_{z1} R_{x2} \ll 1$ and $\omega C_{z2} Z_z \ll 1$ are chosen then equation (2.1a) will be true and the ideal conditions will be achieved. For example if the load of a capacitor C_z in parallel with a resistor R_z is connected then the frequency must be chosen as

$$\omega \leq \left\{ \frac{0.1}{C_{z1} R_{x2}}, \frac{0.1(R_{z2} + R_z)}{(C_{z2} + C_z) R_{z2} R_z} \right\}, \text{ in order to neglect the parasitics.}$$

4.2 The Behaviour of CDBA at Low Frequencies

As seen from the equations of the last section that the input voltage of n-terminal and the output current of z-terminal both are indexed to frequency. Therefore, the behaviour of CDBA changes with frequency. At low frequencies when $\frac{1}{R_{z1}} \gg \omega C_{z1}$

and $\frac{1}{R_{z2}} \gg \omega C_{z2}$ the effects of capacitors C_{z1} and C_{z2} can be negligible and Fig. 2.4

can be redrawn as below in Fig. 4.1.

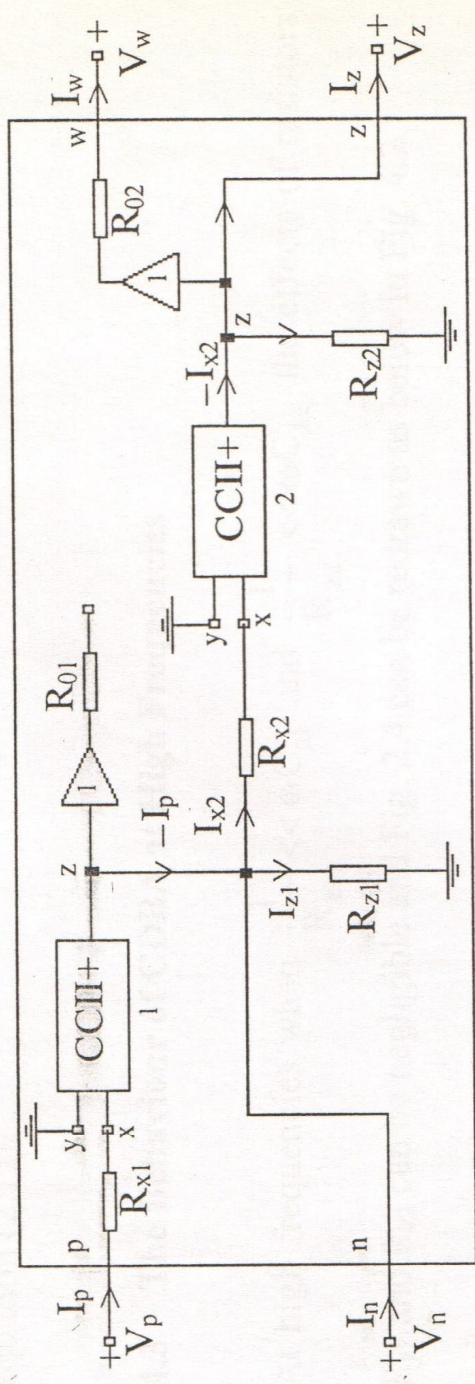


Fig. 4.1 Model of CDBA at low frequencies

Equation (4.4) becomes

$$V_n = (I_n - I_p) \frac{R_{z1}}{\frac{R_{z1}}{R_{x2}} + 1} \quad (4.6)$$

By substituting the values of R_{z1} and R_{x2} , the above equation becomes

and equation (4.5a) becomes

$$I_z = (I_p - I_n) \times \frac{1}{1 + \frac{R_{x2}}{R_{z1}}} \times \frac{1}{1 + \frac{Z_z}{R_{z2}}} \quad (4.7)$$

By substituting the values of R_{z1} and R_{x2} the above equation becomes

$$I_z = \varepsilon(I_p - I_n) \times \frac{1}{1 + \frac{Z_z}{R_{z2}}} \quad (4.7a)$$

where

$$\varepsilon = 0.99998$$

If Z_z is chosen as $|Z_z| \ll R_{z2}$ then it can be obtained that

$$I_z = \varepsilon(I_p - I_n) \quad (4.7b)$$

and it can be seen that I_z is very close to its theoretical value which is given in equation (2.1a).

4.3 The Behaviour of CDBA at High Frequencies

At high frequencies when $\frac{1}{R_{z1}} \ll \omega C_{z1}$ and $\frac{1}{R_{z2}} \ll \omega C_{z2}$ the effects of resistors

R_{z1} and R_{z2} can be negligible and Fig. 2.4 can be redrawn as below in Fig. 4.2.

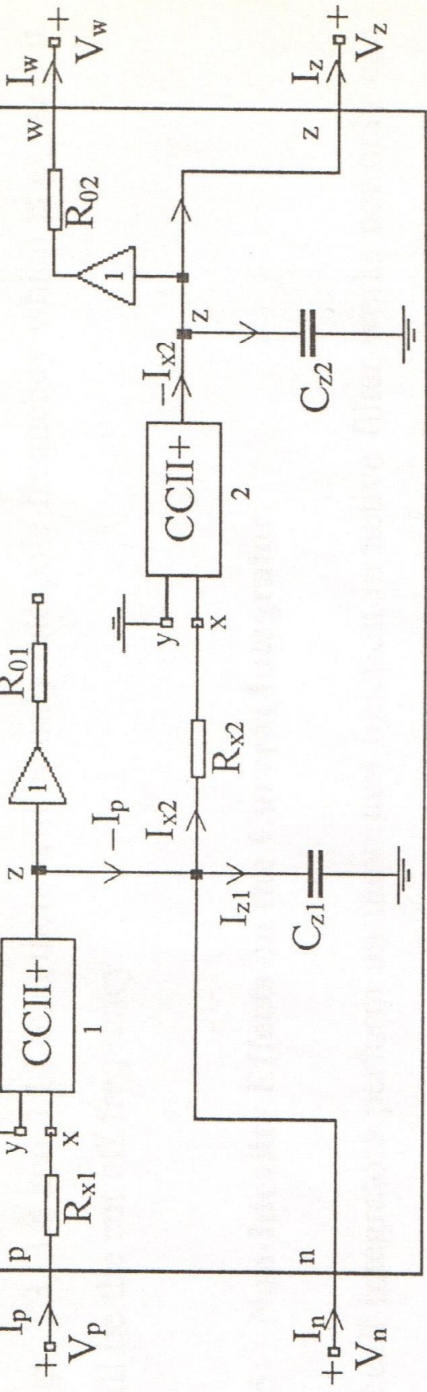


Fig. 4.2 Model of CDBA at high frequencies

Equation (4.4) becomes

$$V_n = (I_n - I_p) \frac{1}{\frac{1}{R_{x2}} + sC_{z1}} \quad (4.8)$$

and equation (4.5a) becomes

$$I_z = (I_p - I_n) \frac{1}{1 + sC_{z1}R_{x2}} \times \frac{1}{1 + sC_{z2}Z_z} \quad (4.9)$$

When $Z_z = 0$ is chosen as in the circuits of Figs. 3.3, 3.8 and 3.11 the above equation becomes

$$I_z = (I_p - I_n) \frac{1}{1 + sC_{z1}R_{x2}} \quad (4.9a)$$

4.4 The Cut Off Frequency of CDBA

The bandwidth of the CDBA as other types of op-amps is the most important limiting factor for filter operation. The frequency response of the electronic CDBA circuit shown in Fig. 2.4 is determined from equation (4.5a). The cut off frequency can be obtained from the poles of the equation that are:

$$\omega_{p1} = 2.22 \cdot 10^8 \text{ rad} \text{ (for load resistance } R_z = 1 \text{ K}\Omega \text{ connected to z-terminal)} \quad (4.10a)$$

$$\omega_{p2} = 4.45 \cdot 10^9 \text{ rad} \quad (4.10b)$$

Therefore, the cut off frequency will be ω_{p1} . If $Z_z = 0$ is chosen as in the circuits of Figs. 3.3, 3.8 and 3.11 then there will be only one pole frequency which is ω_{p2} and it will be the cut off frequency.

4.5 Non-Ideality Effects on the Current Integrator

Recall integrators perform an important function in active filter work; not only can they simulate the performance of inductors and capacitors, but they are also used to build second-order filter sections. Therefore, it is better to show the effect of non-ideality upon the current mode type CDBA integrator shown in Fig. 3.7. Using the electronic CDBA circuit shown in Fig. 2.4 a real current mode integrator can be drawn as shown below:

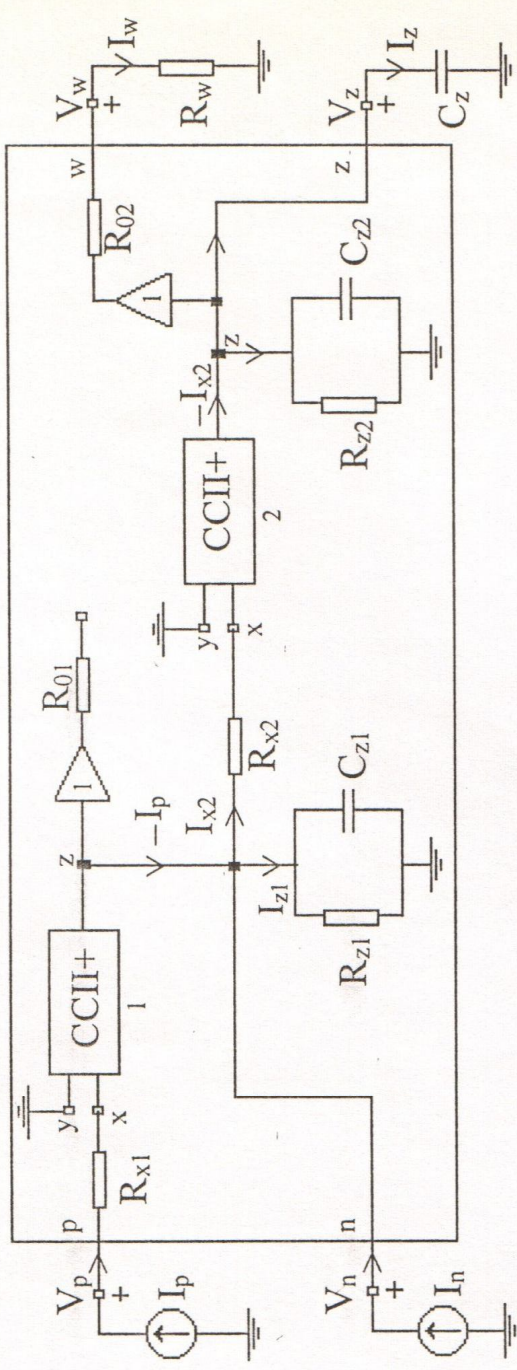


Fig. 4.3 Current integrator with the appearance of CDBA's structure.

Equation (3.12) shows that

$$I_w = \frac{I_p - I_n}{sC_z R_w} \quad (4.11)$$

By substituting the real value of $(I_p - I_n)$ which is I_z from equation (4.5a) the above equation becomes

$$I_w = \frac{1}{sC_z R_w} \cdot x(I_p - I_n) \cdot \frac{1}{1 + \frac{R_{x2}}{R_{z1}} + sC_{z1}R_{x2}} \cdot x \cdot \frac{1}{1 + \frac{1}{sC_z R_{z2}} + \frac{C_{z2}}{C_z}} \quad (4.11a)$$

$$I_z = (I_1 \frac{1}{sC_1R_1} - I_2 \frac{1}{sC_2R_2}) \frac{1}{1 + \frac{R_{x2}}{R_{z1}} + sC_{z1}R_{x2}} = (I_p - I_n) \frac{1}{1 + \frac{R_{x2}}{R_{z1}} + sC_{z1}R_{x2}} \quad (4.12)$$

4.2 Introduction to Bandwidth

The universal integrator filter is capable of providing simultaneous low-pass, bandpass, and high-pass transfer functions. Usually the universal integrator filter is obtained using the well-known state variable implementation. Active filters can be realized in a variety of ways.

$$I(s) = \frac{D s^2 + B s + A}{s^2 + A s + B} \quad (4.13)$$

continuous to play an important role. These signals are often used to drive in continuous and transient operation. For example, a simple low-pass filter may be used to reduce high-frequency noise in a system or to limit the signal bandwidth in a measurement system. Similarly, for a second-order bandpass filter, a relatively narrow signal bandwidth, a second-order bandpass filter may be sufficient to remove or reject high-frequency noise component or a notch filter may be employed to block a troublesome signal at one frequency, such as 60-Hz power supply noise.

More important, however, is the fact that a fundamental building block for the construction of filters of higher order is the cascade of cascade of integrator-loop feedback topologies. Because of the fact that the integrator is essential to exponential variation and oscillation, it is known that cascading integrator-second-order building blocks retains the characteristics of the first filter (4.12).

5. CDBA-BASED SECOND-ORDER ACTIVE FILTERS

In this chapter the realisation of biquadratic filters using CDBA is presented. Moreover, the realisation of CDBA-based biquad filters using MOS resistors is presented.

5.1 Introduction to Biquad Filters

The universal biquad filter is capable of providing simultaneously the lowpass, bandpass, and highpass transfers. Usually this universal second-order filter is obtained using the well-known state variable implementation. Active filters that realise the biquadratic transfer function

$$H(s) = \frac{B_2 s^2 + B_1 s + B_0}{s^2 + A_1 s + A_0} = \frac{B_2 s^2 + B_1 s + B_0}{s^2 + s \frac{\omega_p}{Q_p} + \omega_p^2} \quad (5.1)$$

continuous to play an important role. These biquads are often used own right in communications and measurement equipment, for example, a simple lowpass filter may be used to reduce high-frequency noise in a system or to limit the signal bandwidth in preparation for sampled-data signal processing. Similarly, for measurements over a relatively narrow signal bandwidth, a second-order bandpass filter may be sufficient to eliminate dc and high frequency noise component; or a notch filter may be employed to block a troublesome signal at one frequency, such as 60-Hz power supply interference.

More important, however, biquad form a fundamental building block for the construction of filters of higher order in the form of cascade or multiple-loop feedback topologies because of the resulting reduced sensitivities to component variations and tolerances. It is known that choosing low-sensitive second-order building blocks reduces the sensitivities of the total filter [11].

biquad. In our selection of suitable filters, we shall always insist on low sensitivities to component variation, but other criteria are also important for a design to be economical and useful in practice. To be manufacturable, the component values be practical and the component spread should not be excessive. Since analog filters usually require some adjusting, the biquad must be easy to tune, preferably such that tuning the important filter parameters, ω_p and Q_p , is non-interactive.

In the last decade, owing to the well-known advantages of the current mode operation [1], several current mode current conveyor-based filter realisations have been presented [2,10]. In this chapter the realisation of biquad filters using the proposed active element CDBA by [8] in both voltage mode and current mode is presented. Moreover, the realisation of CDBA-based biquad filters using MOS resistors is presented.

5.2 Realisation of Biquad Filters Using CDBA

A complete biquadratic filter has a transfer function given by equation (5.1). This transfer function can be implemented by voltage-mode or current-mode state variable scheme shown in Fig. 5.1.

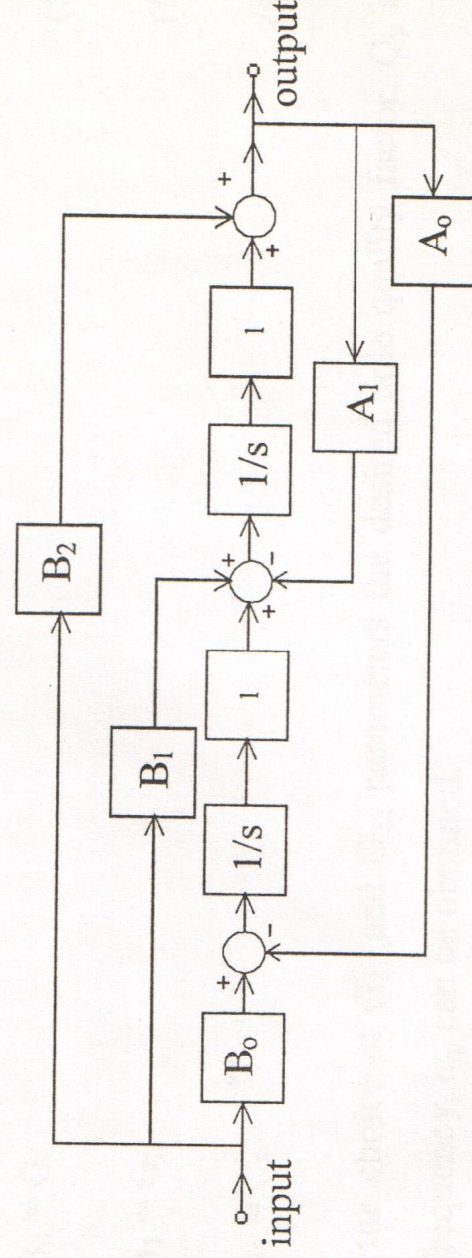


Fig. 5.1 State variable block diagram of complete biquadratic filter

To implement a circuit from a block diagram configuration using CDBAs, integrators and summing point amplifiers are required and in addition a current distributor (take-off point) is needed in current mode.

5.2.1 Realisation of Biquad Filters in Voltage Mode

The realisation scheme for the voltage mode biquad filter is shown in Fig. 5.2. This circuit includes two CDBAs, five resistors and three capacitors.

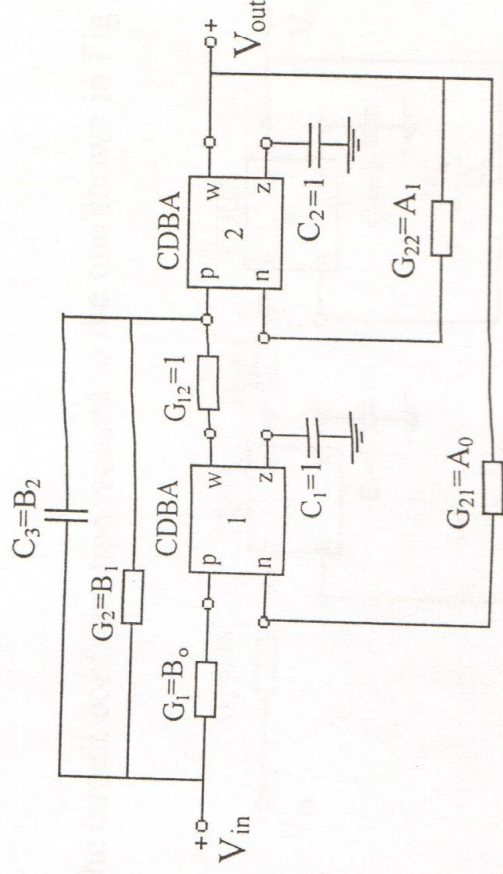


Fig. 5.2 Complete voltage mode biquadratic filter employing CDBAs and realising $H(s)$ of eqn.(5.1)

The design equations can be written for this circuit as given below:

$$\omega_p^2 = G_{21} \quad (5.2)$$

$$\frac{\omega_p}{Q_p} = G_{22} \quad (5.3)$$

$$B_0 = G_1 \quad (5.4)$$

$$B_1 = G_2 \quad (5.5)$$

$$B_2 = C_3 \quad (5.6)$$

With the choice of G_{21} and G_{22} parameters the desired pole quality factor, Q_p and pole frequency, ω_p can be obtained.

We shall now consider special cases of Fig. 5.2.

a-Lowpass case:

In addition to the design equations (5.2) and (5.3), if the following parameters are chosen as:

$$G_1 = H\omega_p^2, \quad G_2 = 0, \quad C_3 = 0 \quad (5.7)$$

$$H(s) = \frac{H\omega_p^2}{s^2 + s\frac{\omega_p}{Q_p} + \omega_p^2} \quad (5.8)$$

In this case the circuit configuration reduced to the one shown in Fig. 5.3 below:

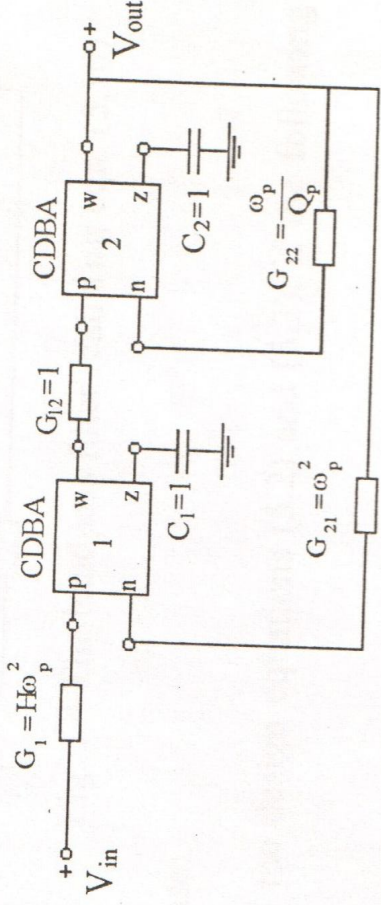


Fig. 5.3 The lowpass filter realising $H(s)$ of eqn. (5.8)

b-Bandpass case:

In addition to the design equations (5.2) and (5.3), if the following parameters are chosen as:

$$G_1 = 0, \quad G_2 = H\frac{\omega_p}{Q_p}, \quad C_3 = 0 \quad (5.9)$$

the following bandpass transfer function will be realised:

$$H(s) = \frac{H\frac{\omega_p}{Q_p}s}{s^2 + s\frac{\omega_p}{Q_p} + \omega_p^2} \quad (5.10)$$

In this case the circuit configuration reduced to the one shown in Fig. 5.4 below:

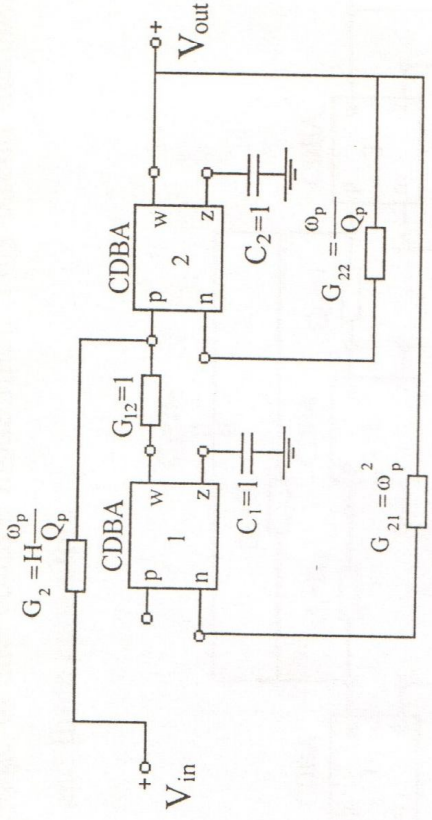


Fig. 5.4 The bandpass filter realising eqn. (5.10)

c-Highpass case:

In addition to the design equations (5.2) and (5.3), if the following parameters are chosen as:

$$G_1 = 0, G_2 = 0, C_3 = H \quad (5.11)$$

the following highpass transfer function will be realised:

$$H(s) = \frac{Hs^2}{s^2 + s \frac{\omega_p}{Q_p} + \omega_p^2} \quad (5.12)$$

In this case the circuit configuration reduced to the one shown in Fig. 5.5 below:

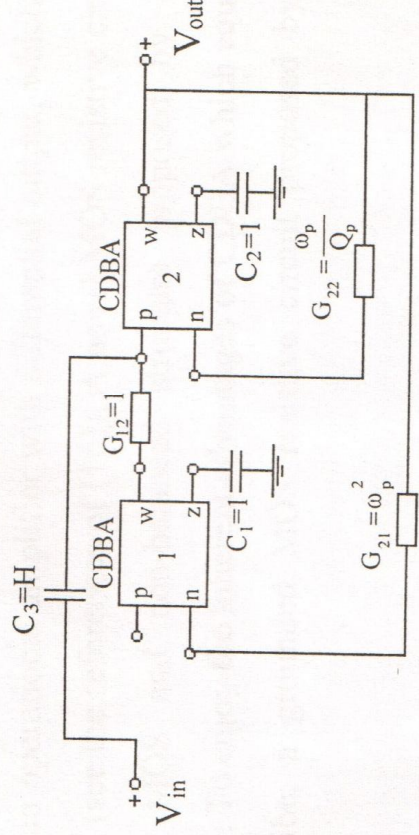


Fig. 5.5 The highpass filter realising eqn. (5.12)

5.2.2 Realisation of Biquad Filters in Current Mode

The realisation scheme for the current mode biquad filter is shown in Fig. 5.6. The difference between this circuit and the one of Fig. 5.2 is that a current distributor is

added to first stage of the voltage mode filter. This circuit includes three CDBAs, seven resistors and three capacitors.

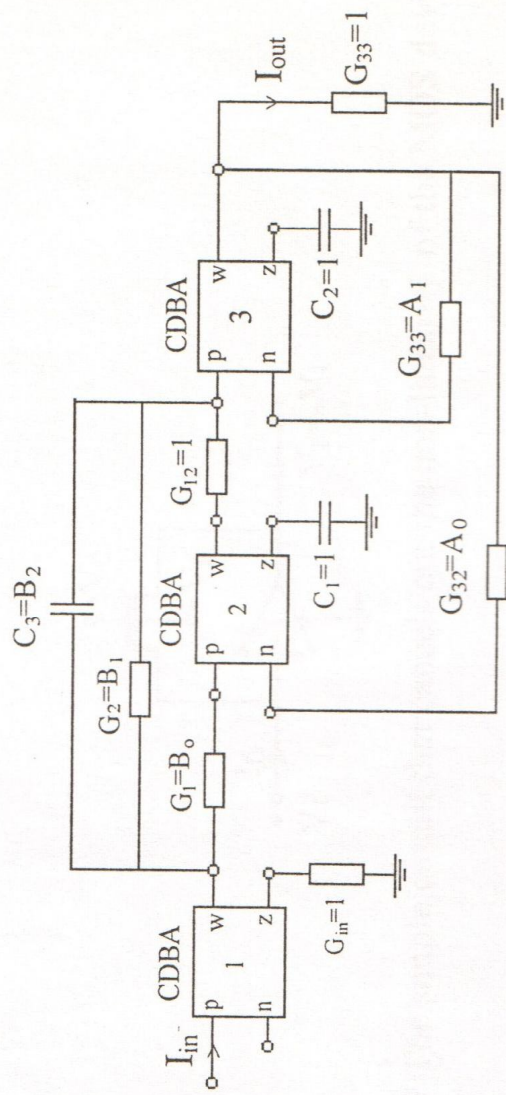


Fig. 5.6 Complete current mode bi quadratic filter employing CDBAs and realising eqn. (5.1)

The transfer function of this circuit and the special case parameters are the same of the voltage mode.

5.3 CDBA-Based Biquad Filter Realisation Using MOS Resistors

Fully integrated continuous-time linear circuits can be realised in MOS technology by using MOS transistors in lieu of conventional resistors. Many attempts have been made to utilise such circuits as non-linearity cancellation can be achieved in them. The MOS balanced linear circuit structures minimise or cancel the non-linearity, but they require an operational amplifier with differential output, which increases power consumption (see the references of [16]). A novel MOS resistive circuit proposed by [16] and a MOS and non-balanced structure proposed by [17] avoid this disadvantage. To enjoy the inherent advantages of CDBA which equations (2.1a) and (2.1c) describe, a grounded MOS resistive circuit proposed by [18] is highly desirable.

5.3.1 Suitable MOS Resistor Configurations for CDBA-Based Biquad Filters

In order to implement biquad filters using MOS resistors, it is better to recognise the behaviour of the convenient MOS resistors proposed by [17] and [18].

non-linearity of the MOS device. This circuit involves one MOSFET transistor and an inverting unity gain amplifier.

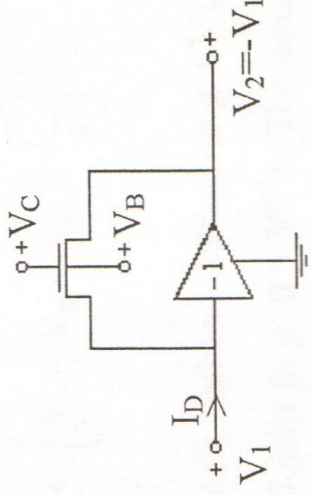


Fig. 5.7 The simple circuit that cancels out the non-linearity of the MOS device

In the figure above V_C , V_B , V_1 and V_2 are the control (gate), substrate, drain and source voltages, respectively. After the non-linearity cancellation the drain current (I_D) for an n-channel device can be written as:

$$I_D = K_1 a_1 (2V_1) = 2V_1/R \quad (5.13)$$

where

$$R = \frac{1}{K_1 a_1} = R_s \left(\frac{L}{W} \right) = \frac{L/W}{\mu C_{ox} (V_C - V_T)} \quad (5.14)$$

W and L are the channel width and length, W/L is the aspect ratio of the transistor, which is a design parameter, and R_s is a sheet resistance. V_T is the threshold voltage of the transistor corresponding to a substrate bias V_B (e.g. $2V$), μ is the carrier effective mobility in the channel and C_{ox} is the gate oxide capacitance per unit area, where $(\mu C_{ox})^{-1}$ is typically 20 to 100 $k\Omega V$. Thus the MOS transistor in this configuration behaves as a linear resistor over an extended voltage range.

Furthermore, in order to be able to use the MOS transistor as a linear resistor, not only the terminal voltages of the MOS transistor (i.e. V_1 and $V_2 = -V_1$) must be kept equal in magnitude and opposite in sign but they must also remain in the non-saturation region. In the other words, the terminal voltages must also satisfy the following conditions:

$$V_B + V_Q \leq V_1, V_2 \leq V_C - V_k \quad (5.15)$$

where V_1 and $V_2 = -V_1$ are the terminal voltages. V_C is a d.c. control voltage (e.g. 3 to 5V). V_B is a fixed d.c. bias voltage (e.g. -5V). V_k and V_Q are safety margin voltages. V_Q is a non-critical quantity and V_k is given by:

$$V_k = V_{FB} + \phi_B - \frac{\gamma^2}{2} + \gamma \left(V_C - V_B - V_{FB} + \frac{\gamma^2}{4} \right)^{1/2} \quad (5.16)$$

where V_{FB} is the transistor's flatband voltage (e.g. 0V), ϕ_B is typically 0.7 V at room temperature. γ is a coefficient (e.g. 0.5 $V^{1/2}$). The control voltage, V_C , can vary the resistor values.

Fig. 5.8 shows the proposed MOS resistive circuit by [18] that cancels out the non-linearity of the MOS device. Let's name this circuit as Simplified MOS Resistive Circuit (SMRC). This circuit involves two MOSFET transistors only.

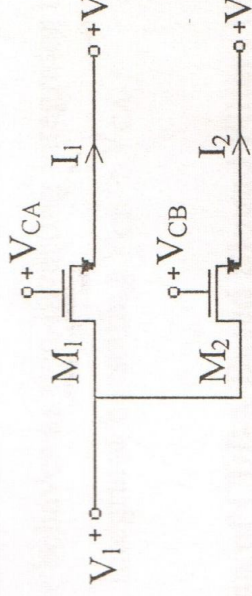


Fig. 5.8 The simplified MOS resistive circuit (SMRC)

where V_{CA} , V_{CB} , V_B , V_1 and V are the first transistor's control (gate), the second transistor's control (gate), substrate, drain and source voltages, respectively. The following equations can be written for this circuit:

$$I_1 = F(V_1, V_{CA}) - F(V, V_{CA}) \quad (5.17a)$$

$$I_2 = F(V_1, V_{CB}) - F(V, V_{CB}) \quad (5.17a)$$

$$\Rightarrow I_1 - I_2 = F(V_1, V_{CA}) - F(V_1, V_{CB}) - (F(V, V_{CA}) - F(V, V_{CB}))$$

$$I_1 - I_2 = 2.K_2.(V_1 - V).(V_{CA} - V_{CB}) \quad (5.18)$$

where

$$K_2 = \frac{1}{2} \mu C_{ox} \frac{W}{L} \quad (5.19)$$

setting $V_{CB} > V_{CA}$.

A CDBA-based integrator circuit using SMRC circuit can be designed as shown in

Fig. 5.9 below:

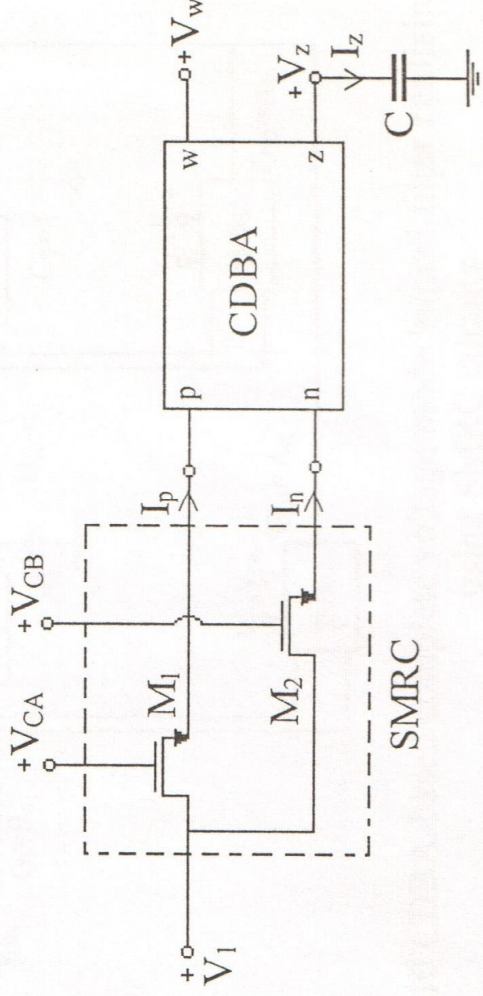


Fig. 5.9 CDBA-based integrator circuit using SMRC

Note that the integrator behaves as non-inverting integrator by setting $V_{CB} < V_{CA}$ and it behaves as inverting integrator by setting $V_{CB} > V_{CA}$.

5.3.2 Implementation of CDBA-Based Biquad Filters Using SMRC

After the introduction of the behaviour of the MOS resistors, it's ready now to design CDBA-based biquad filters using the certain configurations discussed in the previous section.

The complete voltage mode biquad filter shown in Fig. 5.2 can be realised using SMRC as in Fig. 5.10 below:

conductances connected to z-terminal of related CDBAs. The simulated grounded conductances G_{in} and G_{out} each is equivalent to the conductances G_{in} and G_{33} of the circuit of Fig. 5.6 respectively. These indicated circuits could be replaced by the indicated circuits shown in Fig. 5.7 to simplify the circuit of Fig. 5.11 as a second configuration as below:

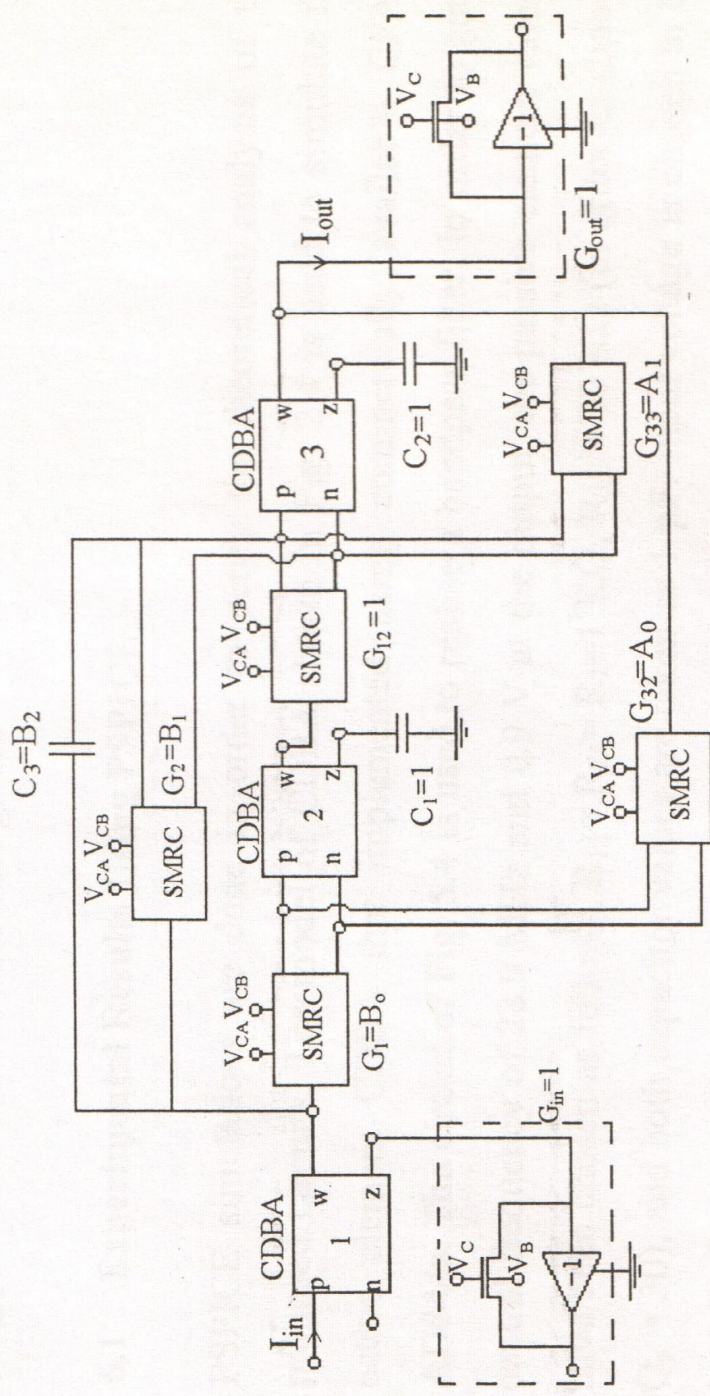


Fig. 5.12 CDBA-based complete current mode biquad filter realising eqn. (5.1) using SMRC and the simple non-linearity cancellation circuit

Note that the voltage transfer functions given in the above equations are ideal, and recall from Chapter 4 that parasitic input and output impedances cause errors in filter performance that should be investigated from case to case. At high frequencies for which CDBA designs are intended, the deviations on output characteristic may not be negligible. For filters in the audio-frequency range, however, errors caused by parasitic components and also by finite bandwidth of CDBAs are usually negligible. Take into account that the non-linearity cancellation of MOS resistors used in SMRCs is dependent on the exactly the same voltage termination which is grounded input voltage of CDBA in this thesis, i.e., a distortion caused by this non-linearity may be appeared in the output signal of filters.

6. RESULT AND CONCLUSION

In this chapter the experimental results that are obtained using PSPICE computer programme and a conclusion are given.

6.1 Experimental Results Using PSPICE

PSPICE simulations are done in order to verify the theoretical analysis of the proposed circuits. The model of CDBA shown in Fig. 2.4 is used to simulate the active element CDBA that implemented using commercially available CFAs, AD844s. The circuit of Fig. 5.4 is used to realise a bandpass filter. In order to get a central frequency of 28.9 MHz and 0.9 V at the output, the passive element values have been chosen as follows, $R_{12} = R_{21} = R_2 = 1 \text{ K}\Omega$, $R_{22} = 30 \text{ K}\Omega$ (in order to choose $Q_p = 30$), and both capacitor values are taken as 1 pF. Input voltage is chosen to be 0.03 V. The measured frequency is 28.89 MHz, and the phase angle is approximately equal to -0.6° , the output voltage is 0.94 V (because H is chosen to be 30 by setting $R_2 = 1 \text{ K}\Omega$), i.e., experimental results which are shown in Fig. 6.1 below is verifying theoretical analysis. The computer programme is given in Appendix A.

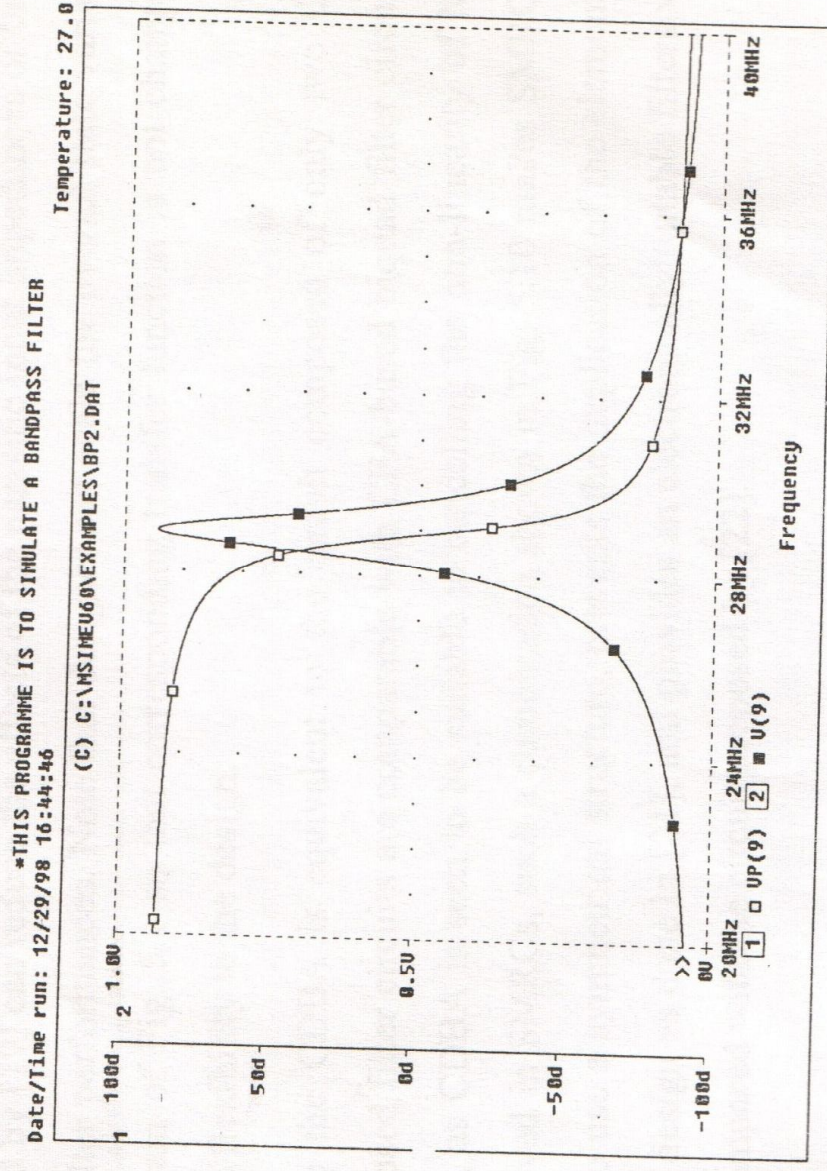


Fig. 6.1 The phase and the magnitude responses of the circuit of Fig. 5.4

transistors' drain currents. It is seen that almost full cancellation of non-linearity is achieved at the output of the integrator circuit of Fig. 5.9 by taking the Fourier transformation of output capacitor current. For this simulation the W/L ratio is chosen as $10\text{ }\mu\text{m}/4\text{ }\mu\text{m}$ for N-type transistors used in SMRC circuit, the capacitor is 45 pF and the power supply is 0.1 V at 100 KHz. The total harmonic distortion of first nine harmonics is %0.68. The computer programme is given in Appendix B.

6.2 Conclusion

The choice of the active element CDBA as the building block for continuous time filters is justified. A simple synthesis procedure has been presented for generating a CDBA-based biquade filter. The method presented here is straightforward and simple in that it gives not only the configuration but also the element values directly from the coefficients of the biquad transfer function. As seen from the proposed voltage mode biquad circuit, only two commercially implementable active components (i.e. CDBA) are required. The proposed filter circuit uses at most five resistors and three capacitors. But the number of the passive elements depends on non-zero coefficients, and hence it is considerably reduced in realisation of lowpass, bandpass, and highpass filter responses. The use of CDBA as active component simplifies the implementation. Selecting the impedance-scaling factor properly as stated by [19] can reduce the effects of the parasitic input impedances of the CDBAs on filter performances. Note that designer can scale the overall state variable block diagram of Fig. 5.1 so that corresponding transfer function is not changed, which gives flexibility to the design.

Since the CDBA is equivalent to the circuit composed of only two CFAs, the proposed filter circuits are comparable with CFA-based biquad filter circuit in [20]. Also, as CDBA is seen to be suitable to cancelling the non-linearity of MOSFETs involved in SMRCs, such a combination shown in Fig. 5.10 makes SMRC possible not to use a symmetrical structure, prevents the duplication of the elements used in filter design as done in [21], and provides an electronically tunable filters which can be compared with the circuit proposed by [22].

REFERENCES

- [1] ROBERS, G. W. and SEDRA, A. S., 1989. All current-mode frequency selective circuits, *Electronics Letters*, **25**, 759-761.
- [2] SEDRA, A. S., and SMITH, K., 1970. A second-generation current conveyor and its applications, *IEEE Trans. Circuit Theory*, **17**, 132-134.
- [3] LIU, S. I., TSAO, H. W., and WU, J., 1990. Cascadable current-mode single CCI-biquad, *Electronics Letters*, **26**, 2005-2006.
- [4] SENANI, R., 1996. A simple approach of deriving single-input-multiple-output current-mode biquad filters, *Frequenz*, **50**, 124-127.
- [5] TOUMAZOU, C. and LIDGEY, F. J., 1986. Universal active filter using current conveyors, *Electronics Letters*, **22**, 662-664.
- [6] TEK, H. and ANDAY, F., 1989. Voltage transfer function synthesis using current conveyors, *Electronics Letters*, **25**, 1552-1553.
- [7] ACAR, C., 1996. Nth-order transfer function synthesis using a commercially available active component: Signal-flow graph approach, *Electronics Letters*, **32**, 1933-1934.
- [8] ACAR, C. and OZOGUZ, S., 1998. A new versatile building block: current differencing buffered amplifier suitable for analog signal-processing filters, to be published in *Microelectronics Journal*.
- [9] ANALOG DEVICES, 1990. *Linear products data book*, Norwood, MA.
- [10] SOVOBODA, J. A., MCGORY, L., and WEBB, S., 1991. Applications of a commercially available current conveyor, *Int. J. Electron.*, **70**, 159-164.
- [11] SCHAUMANN, R., GHAUSI, M. S. and LAKER, K. R., 1990. Design of analog filters, Prentice-Hall, Inc.
- [12] EL-MASRY, Ezz I., and GATES, John W., 1996. A novel continuous-time current-mode differentiator and its applications, *IEEE Trans. Circuit and Systems-II*, **43**, 56-59.
- [13] AL-ALAOUI, M. A., 1988. A stable differentiator with a controllable signal-to-noise ratio, *IEEE Trans. Instrumentation and Measurement*, **37**, 383-388.

- [15] SURAKAMPONTORN, W., 1992. CMOS floating voltage-controlled negative resistor, *Electronics Letters*, **28**, 1457-1459.
- [16] CZARNUL, Z., 1986. Novel MOS resistive circuit for synthesis of fully integrated continuous-time filters, *IEEE Trans. Circuit and Systems, CAS-33*, 718-721.
- [17] ACAR, C. and GHAUSI, M. S., 1987. Fully integrated active-RC filters using MOS and non-balanced structure, *Int. J. Circuit Theory & Applications*, **15**, 105-121.
- [18] AKBULUT, C. A., 1995. MRC ve akım taşıyıcı elemanları ile devre sentezi, *M.Sc. Thesis*, I.T.U. Institute Of Science And Technology, Istanbul.
- [19] SVOBODA, J. A., 1994. Transfer function synthesis using current conveyors, *Int. J. of electronics*, **76**, 611-614.
- [20] SUN, Y. and FIDLER, J. K., 1994. Versatile active biquad based on second-generation current conveyors, *Int. J. of electronics*, **76**, 91-98.
- [21] BANU, M. and TSIVIDIS, Y., 1983. Fully-integrated active-RC filters in MOS technology, *IEEE J. Solid State Circuits*, **SC-18**, 644-651.
- [22] PAPAZOGLU, C. A. and KARYBAKAS, C. A., 1997. Noninteracting electronically tunable CCII-based current-mode biquadratic filters. *IEE Proc. -Circuits Devices Syst.*, **144**, 178-184.

APPENDIXES

Appendix A

*THIS PROGRAMME IS TO SIMULATE A BANDPASS FILTER
*USING PSPICE PROGRAMME

*SUBCIRCUIT OF REAL CDBA

.SUB CDBA P N Z W

VF_FP 1C 0

R_RX1 1C 0

VF_FNN 2C 0

R_RZ1 2C 0 3E6

C_CZ1 2C 0 4.5E-12

F_FP 0 2C VF_FP -1

R_RX2 2C 3C

VF_FNN 3C 0 0

F_FNN 0 Z VF_FNN -1

R_RZ2 Z 0 3E6

C_CZ2 Z 0 4.5E-12

E_EW W 0 Z 0 1

.ENDS CDBA

*RESISTORS

R_RRP 2 0 1E12

R_R1 1 6 1K

R_RO1 5 6 1K

R_R21 9 7 30k;WP/QP

R_R20 9 3 1K;WP^2

*CAPACITORS

C_CO 4 0 1E-12

C_C1 8 0 1E-12

*CDBA CALLING

X_XCO 2 3 4 5 CDBA

X_XC1 6 7 8 9 CDBA

```
V_VIN 1 0 AC 0.03
*****
* AC ANALYSIS
*****
.AC DEC 20000 20000KHZ 40000KHZ
.PROBE
.END
```

Appendix B

```
*THE CIRCUIT OF CDBA AND SMRC BASED INTEGRATOR
*SUBCIRCUIT OF CDBA
*****
```

```
*****
*.SUB CDBA P N Z W
*****
```

```
VF_FP P 1C 0
R_RX1 1C 0 50
VF_FNN N 2C 0
R_RZ1 2C 0 3E6
C_CZ1 2C 0 4.5E-12
F_FP 0 2C VF_FP -1
R_RX2 2C 3C 50
VF_FNN 3C 0 0
F_FNN 0 Z VF_FNN -1
R_RZ2 Z 0 3E6
C_CZ2 Z 0 4.5E-12
E_EW W 0 Z 0 1
.ENDS CDBA
*****
```

```
C_CZ 0 3 2E-9
R_RW 0 4 1T
*****
```

```
*SUBCIRCUIT OF SMRC
*****
```

```
.SUB SMRC SV SP SN SCA SCB
M1 SV SCA SN AA NBB L=4U W=10U
M2 SV SCB SP AA NBB L=4U W=10U
.MODEL NBB NMOS(LEVEL=2 LD=0.414747U TOX=505.0E-10
NSUB=1.35634E16
+VTO=0.864893 KP=44.9E-6 GAMMA=0.981 PHI=0.6 UO=656 UEXP=0.211012
+UCRIT=107603 DELTA=3.53172 VMAX=100000 XJ=0.4U
LAMBDA=0.0107351
+NFS=1E11 NEFF=1.001 NSS=1E12 TPG=1 RSH=9.925 CGDO=2.83588E-10
+CGSO=2.83588E-10 CGBO=7.968E-10 CJ=0.0003924 MJ=0.456300
+CJSW=5.284E-10 MJSW=0.3199 PB=0.7 XQC=1
V_VAA AA 0 DC -5
.ENDS SMRC
```



```
*****SECOND DC CONTROL VOLTAGE*****  
*CALLING SMRC AND CDBA CIRCUITS*  
*****  
X_X2 5 1 2 6 7 SMRC  
X_X1 11 12 3 4 CDBA  
*****  
VF_FIP 1 11 0;FOR MEASURING Ip  
VF_FIN 2 12 0;FOR MEASURING In  
*****  
*AC ANALYSIS  
*****  
.TRAN 2Us 20Us 0 0.008Us  
.FOUR 100KHZ I(C_CZ),I(VF_FIP),I(VF_FIN)  
.END
```


BIOGRAPHY

M. Abdulbaki Ibrahim was born in Iraq-Erbil, in 1969. He graduated from Rezgari Secondary School in 1986. In 1990 he received B.Sc. degree in Electronics and Communication Engineering from Salahaddin University (Iraq-Erbil). He is a graduate student at Istanbul Technical University in the department of Electronics and Communication Engineering. He is currently working as a research assistant in Department of Electrical Engineering at Salahaddin University.