ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

8-BIT 2 GSPS TIME-INTERLEAVED SAR ADC DESIGN FOR PORTABLE MEASUREMENT DEVICES

M.Sc. THESIS

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

TAŞINABİLİR ÖLÇÜ ALETLERİ İÇİN 8-BİT 2 GSPS AYRIK ZAMANLI ARDIŞIK YAKLAŞIMLI ANALOG SAYISAL ÇEVİRİCİ TASARIMI

YÜKSEK LİSANS TEZİ

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ARALIK 2015

Büşra TAŞ, a **M.Sc.** student of ITU **Graduate School of Science Engineering and Technology** 504121381, successfully defended the thesis entitled "8-BIT 2 GSPS TIME-INTERLEAVED SAR ADC DESIGN FOR PORTABLE MEASUREMENT DEVICES", which she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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Date of Defense : 23 December 2015

To my family and friends,

FOREWORD

I would like to thank my thesis supervisor Assoc. Prof. Dr. Metin Yazgı for his guidance and encouragement.
I thank my family and all my friends who helped me with the problems I encountered during my studies. I would never succeeded without their help and support.

December 2015

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(Electronics Engineer)

TABLE OF CONTENTS

Page

ABBREVIATIONS

ADC : Analog to Digital Convertor
BER : Bit Error Rate
DAC : Digital to Analog Convertor
DFF : D-type Flip Flop
DNL : Differential Nonlinearity
ENOB : Effective Number Of Bits
FoM : Figure of Merit
INL : Integral Nonlinearity
LSB : Least Significant Bit
LTE : Long Term Evaluation
MSB : Most Significant Bit
PVT : Process Voltage Temperature
PWL : Piecewise Linear
SAR : Successive Approximation Register
SFDR : Spurious Free Dynamic Range
SINAD : Signal to Noise and Distortion
SNR : Signal to Noise Ratio
TI : Time Interleaved
UWB : Ultra Wide Band

LIST OF TABLES

Page

LIST OF FIGURES

Page

8-BIT 2 GSPS TIME-INTERLEAVED SAR ADC DESIGN FOR PORTABLE MEASUREMENT DEVICES

SUMMARY

A successive approximation register analog to digital convertor (SAR ADC) is a type of ADC that converts a continuous analog signal into a discrete digital representation for all the quantization levels as possible. For this thesis the SAR ADC is consist of a gain stage, a split capacitor array digital to analog convertor (DAC) block, and a SAR block to supply the requirements for high bandwidth real-time oscilloscopes.

As soon as the bandwidth requirements extend beyond the sample rate capability of the available ADC, it becomes necessary to find other techniques to utilize available ADCs to meet those extended requirements or design a new generation ADC. Time interleaving (TI) is a common technique to extend the performance of existing designs. The ADCs are used as parallel. Each ADC provides a sample rate at least half the total sample rate required to meet the Nyquist requirement. The time interleaved SAR ADC is separated in 10 sub-ADC blocks, each sub-ADC is consist of 10 SAR ADC and clocked 36° out of phase. Data is stored in the memory behind each ADC, and once the acquisition is completed, the complete $2GS/s$ representation of the signal could be reconstructed by demuxing the data. The time interleave technique has been used by all the major oscilloscope structures to get the performance up into the GHz range.

The real-time oscilloscope needs a fast and high bandwidth ADC. Based on this purpose, an 8-bit $2GS/s$ time interleaved SAR ADC is designed as usable in high bandwidth portable measurement devices especially real-time oscilloscopes.

In this thesis, a reliable and feasible 8-bit $2GS/s$ SAR ADC with $2GHz$ bandwidth is presented using $180nm$ CMOS technology. A comparator consists of a latch and 5 amplifier with 3 of them are offset cancelled. The simulation results of the comparator is available in the relevant section. A fully differential DAC is consist of a sample & hold circuit and it is generated as split capacitor array DAC. The simulation results of

the DAC is available in the relevant section. The DAC is driven by the SAR logic. The SAR block consist of a phase shifter with 9 D flip flops, a register array with 9 D flip flops, and one more register array with 8 D flip flops. The simulation results of the SAR logic is available in the relevant section.

The SAR ADC processes with the overdrive-recovered amplifiers, offset cancelled comparator, and charge injection rejected split capacitor array DAC. Also the sample and hold procedure is completed by DAC block. The designed TI-SAR ADC is simulated and all the differential non-linearity (DNL), integral non-linearity (INL), signal to noise ratio (SNR), spurious free dynamic range (SFDR), signal to noise and distortion (SINAD), effective number of bits (ENOB) characterizations are determined.

TAŞINABİLİR ÖLÇÜ ALETLERİ İÇİN 8-BİT 2 GSPS AYRIK ZAMANLI ARDIŞIL YAKLAŞIMLI ANALOG SAYISAL ÇEVİRİCİ TASARIMI

ÖZET

Dış dünyada analog olan işaretleri kullanan sayısal cihazlar analog işaretlerle işlem yapamazlar. Analog verilerin elektronik cihazlar tarafından algılanması için bu işaretlerin sayısal işarete dönüştürülmesi gerekmektedir. Üzerinde işlem yapılan sayısal işaret de gerekli durumlarda tekrar analog işarete dönüştürülmelidir. Yüksek performanslı elektronik cihazların kullanımının artmasıyla yüksek hızlı ve yüksek doğruluklu veri dönüştürücülere olan ilgi de artmıştır.

Sayısal analog veri dönüştürücü (Digital to Analog Converter – DAC); bilgisayarlar taraından üretilen sayısal işaretleri analog işarete dönüştürmektedir. Analog sayısal veri dönüştürücüler (Analog to Digital Convertor – ADC) analog sinyallerin bilgisayarlar tarafından işlenebilmesi için sayısal forma dönüştürülmesini işlemini gerçekleştirmektedir.

Belirli bir amaç doğrultusunda büyük sistemler tasarlanırken sistemin çalışma hızına önem verilmelidir. Örnek olarak yüksek hızlı veri aktarımı sağlayan bir sistem verilirse, sistemde bulunan alt blokların her birinin sağlaması gereken hız kriteri en az sistemin çalışma hızı kadar olmalıdır. Sürekli artan çalışma hızına veri dönüştürücüler de uyum sağlamalıdır.

Veri dönüştürücülerin hassasiyeti de hangi uygulamada kullanılabileceğine dair belirleyici rol oynamaktadır. Bir analog sayısal dönüştürücünün hassasiyeti; algılayabileceği en küçük değişimdir ve en az anlamlı bit (Least Significant Bit – LSB) olarak bilinmektedir. Veri dönüştürücünün algılayabileceği en küçük değere ve kullanım alanına göre bit sayısı belirlenmelidir.

Tasarlanmak istenen büyük ve yüksek hızlı sistemlerin içerdikleri alt blokların sayısı arttıkça, bu blokların güç tüketimleri de artmaktadır. Alt blokların tasarımı yapılırken

tükettiği güce önem verilerek tasarım yapılmalı ve güç tüketimini azaltacak yöntemlere başvurulmalıdır.

Veri dönüştürücülerde en çok güç tüketimi karşılaştırıcı (comparator) blokları tarafından yapılmaktadır. Devre az güç tüketecek şekilde tasarlanmalı ve olabildiğince az adet karşılaştırıcı kullanılmalıdır. Bunun için de ADC çeşitlerinden ardışık yaklaşımlı analog sayısal dönüştürücüler (Successive Approximation Register Analog to Digital Convertor – SAR ADC) tasarlanmalıdır.

ADC yapılarının çalışma aşamalarında çok yüksek hız değerlerine ulaşılırken güç tüketiminin de çok arttığı görülmektedir. Fakat tüketilen gücün minimum seviyelerde olması gereken sistemlerde büyük frekans değerine ulaşılması zorlaşmaktadır. Hem hızın çok artmasını hem de güç tüketiminin az seviye kalmasını sağlayan ayrık zamanlı analog sayısal veri dönüştürücü (time interleaved analog to digital convertor – TI-SAR ADC) tasarımları mevcuttur. TI-ADC yapılarının genel çalışma prensibi; girişe gelen analog sinyal belirli zaman gecikmesi ile paralel olarak çalıştırılan n adet ADC tarafından örneklenmesi esasına dayanmaktadır. Bir kontrol devresi ile her bir ADC'nin çevrimi farklı zaman dilimlerinde başlatılır, n adet ADC sonucu da aynı sıra ile çıkışa yönlendirilir ve sonuçlar birleştirilerek girişteki analog işaretin sayısal çevrimi elde edilmiş olur. Sonuca tek bir ADC ile t kadar sürede ulaşılacakken t/n sürede ulaşılmaktadır.

Güç tüketimi, çözünürlük (hassasiyet), örnekleme frekansı (hız) ve bantgenişliği özelliklerine özen gösterilerek üretilen TI-SAR ADC için çok çeşitli kullanım alanları mevcuttur. Hızı GHz mertebesinde olan ölçüm cihazları tasarımlarında kullanılan SAR ADC yapıları hızlı ve yüksek bantgenişlikli olmalıdır. Özellikle taşınabilir osiloskop sistemleri az güç tüketmelidir.

Tasarlanan sistem portatif osiloskoplarda kullanılmak üzere hazırlanmıştır. $180nm$ CMOS teknolojisi kullanılanılarak $2GS/s$ hızına sahip TI-SAR ADC yapısı taşınabilir ölçüm cihazlarıda kullanılmaya uygun tasarlanmıştır. 100 adet $18.5MS/s$ hızında 8-bit SAR ADC zamanda paralel olarak çalıştırılarak yapı elde edilmektedir. SAR ADC yapısı bir karşılaştırıcı, bir DAC ve bir SAR mantık bloğu içermektedir.

Karşılaştırıcı bloğunun dengesizliği devrenin doğru karşılaştırma yapmasını çok etkilemektedir. Bunun için çıkışta dengesizliği ortadan kaldıracak şekilde

kuvvetlendiriciler arasında hata (offset) kapasitesi yöntemi uygulanarak karşılaştırıcı bloğu tasarlanmıştır. Büyük kapasiteler devrenin kapladığı alanı çok artırdığı için DAC bloğunun tasarımında kapasiteleri küçültecek bir yapı kullanılmıştır (split capacitor array DAC). Yapıda bulunan anahtarların (switch) oluşabilecek problemlerini önleme methodlarına başvurulmuştur. Aynı zamanda örnekleme (sample&hold) işlemi de DAC bloğunun içerisinde yapılmaktadır. SAR bloğu karşılaştırıcıdan aldığı veriye göre karar verip sayısal sonucu üretmektedir.

SAR mantık devresi tarafından sürülen bir tamamen farksal kapasitif TI-SAR ADC hesaplamaları yapılmıştır. Yapılan hesaplamalara göre tasarım gerçeklenmiş ve benzetim yoluyla karakterize edilmiştir. Oluşabilecek hataları en aza indirmek için karşılaştırıcı devresinde aşırı yüklenmeyi engelleme (overdrive recovery) ve çıkış hatasını engelleme (output offset cancellation) metotları kullanılmıştır. DAC yapısınnda direnç ve kapasite değerleri seçerken ısıl hata, zaman sabiti, bantgenişliği hesaplamaları ele alınmıştır ve anahtarlamada oluşan şarj oluşumu (charge injection) ve sinyalin girişi etkilemesi (clock feedthrough) hatalarını engellemek için de anahtarlar için analog girişi örnekleme anahtar (analog input sampling switch) yapısı kullanılmıştır.

TI-SAR ADC sisteminin dengesizlik (offset), farksal lineerlik (Differential Nonlinearity – DNL), toplam lineerlik (Integral Nonlinearity – INL), parazitik devingen aralık (Spurious Free Dynamic Range – SFDR), işaret gürültü ve saptırma oranı (Signal to Noise And Distortion – SINAD), işaret gürültü oranı (Signal to Noise Ratio – SNR) ve etkin bit sayısı (Effective Number Of Bits – ENOB) karakteristikleri belirlenmiştir.

Benzetim sonuçlarında sistem, Nyquist frekans bölgesinin tamamında, süreç, proses, kaynak gerilimi, sıcaklık ve yongadan yongaya değişimler boyunca 7 $ENOB$ değerini aşmaktadır ve etkin durumda 7.5 $ENOB$ değerine ulaşmaktadır. Sistemin çalışması sırasında çekilen akımın $10mA$ ve toplam tüketilen güç $15mW$ olduğu bilgisine hesaplamalardan ve analiz sonuçlarından ulaşılmaktadır. Toplam devrenin köşe (corner) ve monte carlo benzetim sonuçları verilmektedir.

Özellikleri, çalışma şekli ve sonuçları ayrıntılı olarak aktarılan TI-SAR ADC yapısı taşınabilir ölçüm cihazlarına uygun şekilde tasarlanmıştır.

1. INTRODUCTION

Applications of Analog to digital converters (ADC) include wide range from wired and wireless communications, data acquisition systems to signal processing applications and medical applications. According to the area of application, ADCs specifications differ as an example, in LTE (Long Term Evaluation) wireless receivers $50Ms/s$ sampling speed and 8 bits of effective resolution are needed (Verbruggen, Iriguchi, & Craninckx, 2012). On the other hand, for ultra-wideband (UWB) radio short distance wireless communications it is required to have high speeds like $500MS/s$ but low resolutions about 4 or 5 bits (Ginsburg & Chandrakasan, 2007).

1.1 ADC Architectures

ADCs are designed in much different kind of structures depending on the specification of the requirements for those applications. Main ADC architectures are flash, successive approximation register, pipeline and sigma-delta.

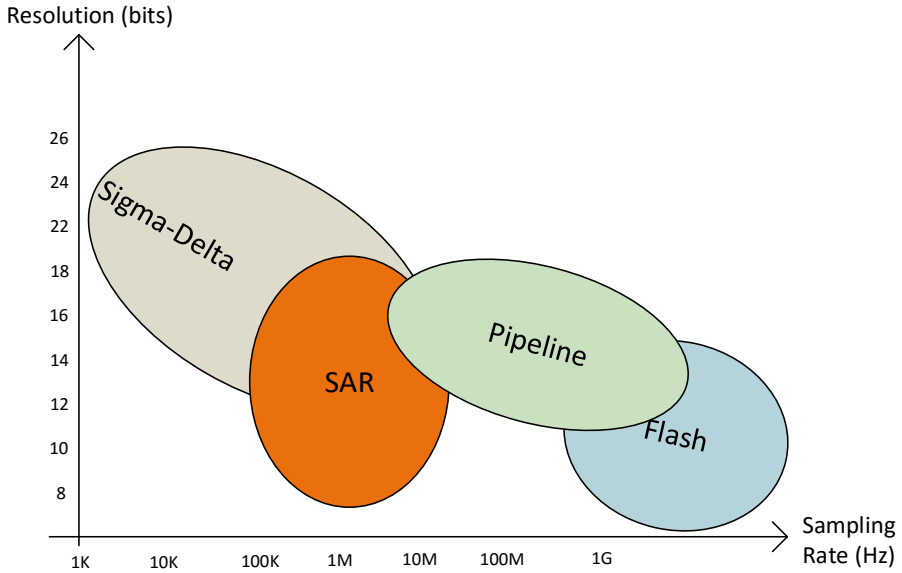

Figure 1.1: Comparison to speed and resolution ADC architectures.

A comparison of architectures in terms of speed and resolution can be seen in Figure 1.1. To come to power and size, the flash ADC has most power dissipation type

with its largest size. The pipeline ADC is the highest one with its high power consumption and large size. The sigma-delta ADC consumes medium power compared to others with its large size. Finally, the SAR ADC has lower power dissipation and smaller size.

1.1.1 Flash ADC

Flash ADC is the fastest and the simplest design among all low resolution ADC structures. For an n-bit flash ADC, an n-bit resistor stream and $(2^n - 1)$ comparator are needed which denotes that the number of comparators and resistors increase exponentially with linearly increasing the resolution. As it can be seen, the huge number of comparators cause the high power dissipation and large chip area.

1.1.2 Pipeline ADC

The pipeline ADC has cascaded structure. Each cascaded stage includes a number of bits of the digital output according to analog input voltage. The structure has high speed with moderate precision converters. Main inconvenience of this architecture is the designing complexity. The design can become very hard for the most modern pipeline ADCs.

1.1.3 Sigma-Delta $(\Sigma - \Delta)$ ADC

The sigma-delta ADC is basically based on the noise shaping. The fraction of noise falls into the Nyquist band that is reduced by oversampling the input signal. Then the noise falling out of the band of interest can be digitally filtered out. The structure is generally used in low bandwidth with high precision applications. The main drawback of the architecture is the slow settling.

1.1.4 SAR ADC

SAR ADC has the range of 8-16 bits resolution and several MS/s speed, which categorize it between sigma-delta and pipeline ADC architectures. In addition, the main advantage of SAR ADC is its lower power consumption in general. The more detailed explanation is stated in the next chapters.

1.2 Purpose of Thesis

For handheld measurement devices like oscilloscope, sampling rate of $2GS/s$ is necessary and for such a high speed ADC only a time interleaved structure is applicable, because a single channel ADC is too power inefficient. Therefore, a time interleaved ADC is chosen for this design.

Furthermore, the ADC resolution is selected to be 8-bits. Normally, three types of non-idealities limit an ADC's effective resolution. First, thermal noise, which is not a big issue for an 8-bit resolution and the capacitor can be chosen large enough to make sure that the thermal noise is more less than the LSB. Second one is non-linearity due to mismatch within a sub-ADC or between different sub-ADCs which will be improved with calibration and design techniques. Finally, performance degradations can be caused by clock jitter (Shinagawa, Akazawa, & Wakimoto, 1990). Sampling jitter causes a voltage noise that is proportional to the input frequency and amplitude, and the maximum achievable signal-to-noise ratio (SNR) for a given random clock jitter standard deviation Δt and input frequency f_{in} is

$$SNR_{max} = -20\log_{10}(2\pi f_{in}\Delta t) \tag{1.1}$$

And the effective number of bits (ENOB) versus SNR is calculated in equation 1.2.

$$ENOB = \frac{SNR(dB) - 1.76}{6.02} \tag{1.2}$$

By assuming $f_{in} = 1GHz$, which is the Nyquist frequency for a $2GS/s$ ADC.

For the sub-ADC topology, a SAR architecture is chosen since it offers the best combination of power and speed for converters with an effective resolution of approximately 8 bits. For the capacitive DAC implementation, the segmented binary weighted capacitor array DAC is chosen over simple binary weighted because of its smaller capacitor values, which improve power consumption and die area as well.

Roughly, the time-interleaved SAR ADCs are required to achieve a total sampling rate of $2GS/s$. If the classical time-interleaving methodology is used, it would create a severe bandwidth limitation on the input due to interconnect parasitic capacitances. Also timing mismatch calibration will be difficult. Therefore a two-level time-

interleaving architecture is proposed (Greshishchev, et al., 2010), (Schvan, et al., 2008), (Tabasy, Shafik, Lee, Hoyos, & Palermo, 2013). Instead of interleaving all 100 SAR ADCs in one hierarchy, they will be divided into 10 sub-ADCs each running at $166.5MS/s$. Each sub-ADC further time interleaves 10 SAR ADCs running at $18.5MS/s$ each. The system and its clock diagram are shown in Figure 1.2.

Firstly, designing a single-ADC, which corresponds to $18.5MSPS$ input sampling rate. Then using the single-ADC in a sub-ADC, which includes 9 single-ADCs. The 9 single-ADCs run in parallel with properly shifted clock to achieve $18.5MSPS \times 9 = 166.5MSPS$ sampling rate for the sub-ADC. The last operation for the thesis is creating a time interleaved $2GSPS$ SAR ADC which obtains 10 sub-ADCs. Each one of these steps are needed to be supported by designs, calculations, simulations and test benches.

This thesis focuses on the design of the $20MS/s$ SAR ADC core, Note that sub-ADC is essentially a sub-sampling ADC where the maximum input frequency is 9 times its Nyquist frequency.

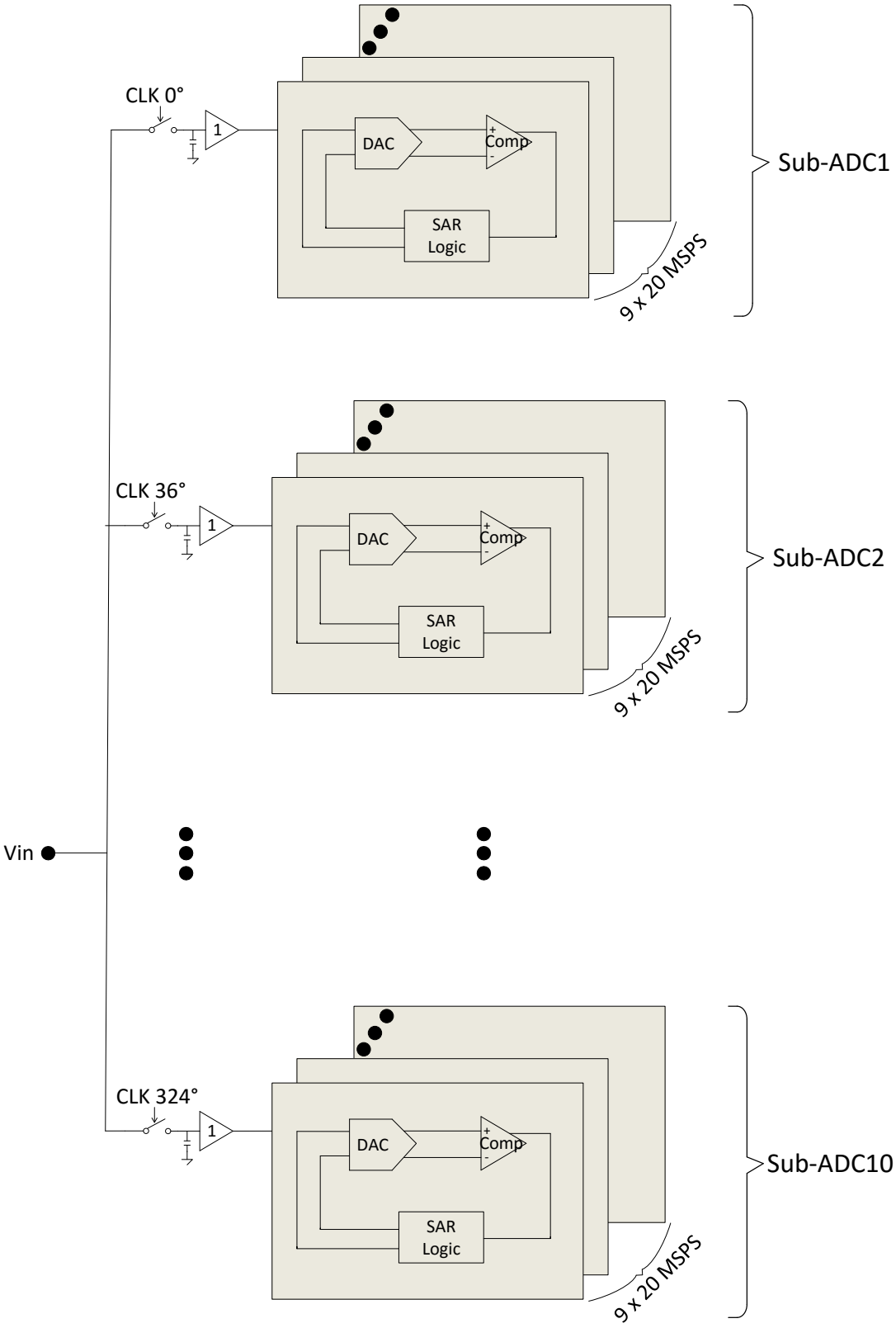

Figure 1.2: Top level block diagram of the proposed 2GS/s 8-bit two-level time-interleaved SAR ADC.

2. BASICS OF SAR ADC

2.1 Literature Review

Among a vast literature research on successive approximation register analog to digital converters, a few relevant examples are provided in this section. The studies are sorted by the date of submission.

An 8-bit current mode TI-SAR ADC is proposed in (Dlugosz & Iniewski, 2007). It is designed in $180nm$ CMOS technology, it has $2MHz$ input frequency and the $0.55V$ supply voltage. A 5-bit $500MSPS$ time interleaved ADC for ultra-wide bandwidth (UWB) applications is realized in $65nm$ CMOS technology with $1.2V$ supply (Ginsburg & Chandrakasan, 2007). It makes use of attenuation capacitor array in order to reduce the capacitor sizes and adjustable latch strobe instant in order to use the time for settling more effectively.

An 8-bit $50MSPS$ with $1.2V$ power supply voltage SAR ADC is realized $65nm$ CMOS technology (Chen, et al., 2009). It is considered that an attenuation capacitor larger than conventional design allows a tunable capacitor in this reference.

A 4-bit $700MSPS$ TI-SAR ADC is designed for UWB application in $180nm$ CMOS process in (Talekar, Ramasamy, Lakshminarayanan, & Venkataramani, 2009). Using Gilbert cell preamplifier reduces the power consumption by approximately 33%. It achieves $23.3mW$ power consumption at $700MS/s$ for an input swing $1V$ peak to peak. The ADC gives SINAD of $23.9dB$ and SFDR of $32.6dB$.

A 6-bit $2.5GS$PS ADC that is supplied by $1V$ is presented in (Greshishchev, et al., 2010). It is used for optical receiver systems. It achieves $40mW$ power consumption and 4.5 $ENOB$ with $65nm$ CMOS technology. An 8-bit $100KSPS$ SAR ADC with $1V$ supply voltage is presented in (Arian, Saberi, & Hosseini Khayat, 2011). Generalized non-binary search algorithm is proposed to reduce the complexity and the power consumption overhead of the digital circuitry.

A 7-bit $1.5GSPS$ TI-SAR ADC is presented in (Akita, Furuta, Matsuno, & Itakura, 2011). It is designed in $65nm$ CMOS technology and it consumes $36mW$ from $1.2V$ supply. The achieved SFDR as $52.4dB$, SINAD as $39.6dB$. An 11-bit $3.6GSPS$ TI-SAR ADC is designed in $65nm$ CMOS (Janssen, et al., 2013). It achieves $54dB$ SNR, $54dB$ SINAD and it consumes $795mW$ power.

A 12-bit $1MS$PS SAR ADC with $1.2V$ power supply is presented in (Du, Ning, Zhang, Yu, & Liu, 2013). A calibration method is presented for the proposed ADC. A TI-SAR ADC is designed in $65nm$ CMOS process and it enables timing skew calibration (Lee, Chandrakasan, & Lee, 2014). $51.4dB$ SINAD, $59.1dB$ SFDR, and $\pm 1.0\ LSB$ INL/DNL are achieved at $1GS/s$ with Nyquist rate input signal. The power consumption is $18.9mW$ from a $1.0V$ supply.

An 8-bit TI-SAR ADC is presented in (Kundu, et al., 2014). It achieves a sampling rate of $2.64GS/s$ while maintaining an ENOB of over 6 bits in the entire Nyquist band. The $40nm$ LP CMOS design dissipates $39mW$ from $1.2V$.

A 6-bit $10GSPS$ TI-SAR ADC is presented in the reference (Tual, Singh, Curis, & Dautriche, 2014). It is based on a master track and hold followed by a time interleaved synchronous SAR ADC, thus avoiding the need for any kind of skew or bandwidth calibration. $28nm$ CMOS technology is used. The core ADC consumes $32mW$ from $1V$ supply and shows $5.3\ ENOB$.

A 10-bit $5GSPS$ TI-SAR ADC is presented in (Fang, et al., 2015). It aims to tolerate decision errors arising from noise, reference settling error, etc. It is designed in $28nm$ CMOS process and achieves $49dB$ SNR, $52dB$ THD and $42dB$ SINAD. It consumes $76mW$ from $1V$ supply.

2.2 Analog to Digital Conversion

Analog to Digital Converters (ADC) convert continuous analog signals to digital data. A continuous analog signal that can take infinite values needs to be quantized for being converted into a digital form. For a proper quantization without any information losses, these infinite values can be sufficiently sampled discrete and finite amounts of values. According to Nyquist's theorem; a continuous time signal has to be sampled by at least twice the maximum frequency to allow accurate reproduction of the original signal

without any information losses (Maloberti, 2007) (Razavi, 1995). In Figure 2.1 is shown an example of 3-bit conversion.

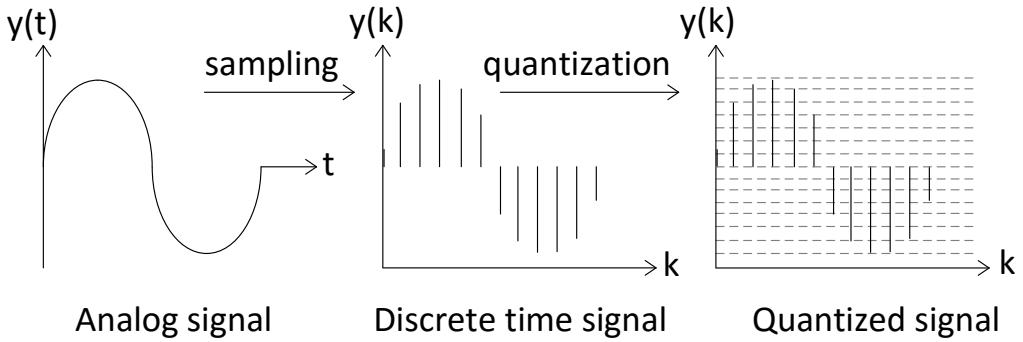

Figure 2.1: Converting analog signal to digital signal.

Quantization is the process of constraining continuous magnitude values into discrete and finite amount of values, which can be represented by digital codes. Resolution of the quantization depends on the number of codes.

2.2.1 SAR ADC

The trade of between speed, resolution and power consumption is the key factor when choosing the most suitable topology. To supply higher resolution and lower power consumption, SAR ADC topology is the most sufficient choice for portable devices which the battery life is one of the major concerns.

Comparing SAR ADC with the other topologies, SAR ADC shows the lowest power consumption with larger resolution and slower sampling rate. Also with the binary search algorithm, the architecture is simple enough to implement.

In Figure 2.2, the binary search algorithm for a 4-bit SAR ADC is depicted. The DAC inside SAR ADC contains sample and hold stage to sample the continuous analog input voltage. An N-bit register that has MSB as ’1’ and all the other bits ‘0’ as firstly, the sampled data of DAC are sent to comparator to determine if sampled input value is higher than half of the reference voltage. Comparator output is logic 1 means that the sampled data is higher. Otherwise, it is lower than $V_{ref}/2$ and MSB of the N-bit shift register cleared to ‘0’. Then the N-bit shift register shifts to the next bit and another comparison is done.

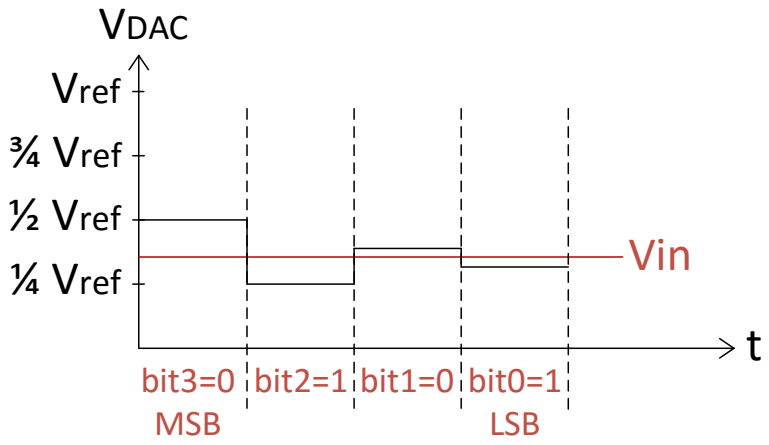

Figure 2.2: SAR operation for 4-bit example.

The conversion continues until all the N-bit is shifted, that means the first value at the beginning of conversion process is LSB now and so on. At the end of the N comparison, the N-bit digital word is predicted by binary weight search algorithm. The final data is resulted from sampled analog input value is available in the shift register until the next N-bit digital word comes.

It is clear that the sampled analog input value is compared with the output of the DAC. Then the digital output word is completed as shown in the Figure 2.2, the converted word is as closed as possible the sampled input as $V_{IN} \pm LSB$. The conversion result is the final output of binary search logic. For all this process, a SAR ADC consists a DAC, a comparator, and a binary search logic.

2.2.2 Design goals

The main aim of this thesis is to design a modest SAR ADC for a high-speed time interleaved ADC. To reach this goal a high speed, low power, high resolution SAR ADC is needed. Therefore, minimum speed is calculated 18.5$MSPS$ and answering the purpose of resolution 8-bit design is applied. Under favor of designed amplifier, power consumption is considered about several mW.

The total consumed current is around 3.5mA. Thanks to the designed amplifier, each one consumes 0.5mA current. Using 180 nm CMOS technology allows 1.8V supply voltage. With this supply voltage, input range is determined around the 1.1V common mode voltage $\pm 500mV$. Finally the time interleaved SAR ADC achieves 2$GSPS$ sampling rate.

3. DESIGNED BUILDING BLOCKS

SAR ADC allows the low power consumption and high resolution, but paying the price with the slow sampling rate (Dlugosz & Iniewski, 2007). To realize the structure it is designed that a fully differential comparator, a binary weighted split switched capacitor array digital to analog converter (DAC), and a successive approximation register (SAR) logic blocks. The designed architecture is shown in the Figure 3.1 as a summary.

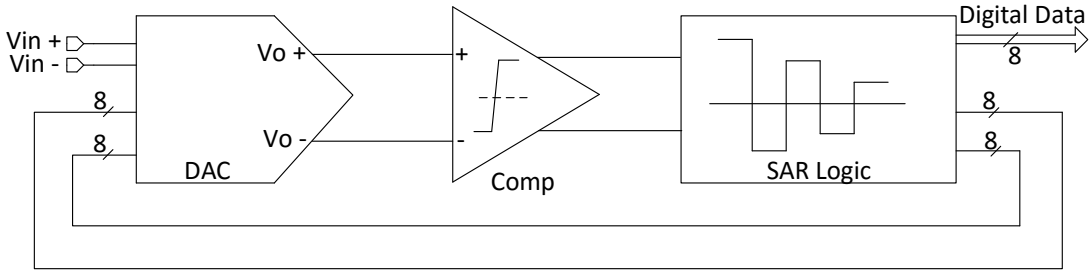

Figure 3.1: Designed SAR ADC architecture.

3.1 The Comparator

A fully differential amplifier has 180° phase shifted two inputs and it amplifies the difference between these input voltages, in Figure 3.2. Fully differential signaling provides a significant cancellation of noise voltage on differential input signals. When the same noise voltages affect two differential input signals on sampling process, common mode change shows up and it is suppressed by common mode rejection of the differential comparator (Maloberti, 2007).

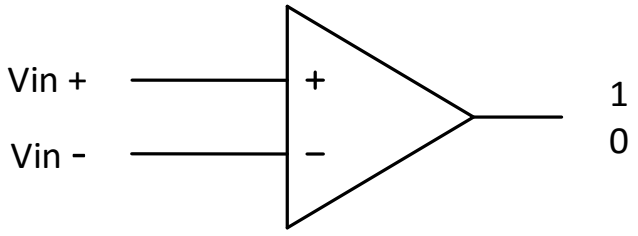

Figure 3.2: Simple comparator.

In general, there are noise voltage and the input voltages at the input of the comparator. The output of the comparator could be V_{FS} or reference voltage.

For an amplifier from the stage of the comparator, if the inputs are $V_{in+} + V_{\text{noise}}$ and $V_{in-} + V_{\text{noise}}$, the output is equal to equation 3.1.

$$V_{out-} = A \times \left((V_{in+} + V_{\text{noise}}) - (V_{in-} + V_{\text{noise}})\right) = 2 \times A \times V_{in+} \qquad (3.1)$$

Moreover, the output is the difference between the two voltages where A is the gain of the amplifier. With differential amplifier, both input voltage is multiplied and noise voltage is subtracted. If the amplifier has differential output, the output voltage also could be $V_{out-} = 2 \times A \times V_{in-}$ as well.

The comparator represents the only analog circuit in the SAR ADC. It determines the speed, resolution, and power consumption. So, these should be analyzed deeply. The trade-off between them shows they have to be evaluated together.

The comparator structure includes cascaded preamplifiers ended with a latch as in Figure 3.3. The signals, which are amplified by cascaded fully differential amplifiers, are conveyed to input of the latch to achieve binary logic levels as soon as possible. However, latch usually has an input offset voltage that is not ignorable. For reliable result, it is common to use a number of cascaded preamplifiers. In addition, this solution will supply the quick decision by latch. The total gain of preamplifiers will reduce the input referred offset of the latch, and the response time of the latch will be smaller for an amplified signal (Razavi & Wooley, 1992).

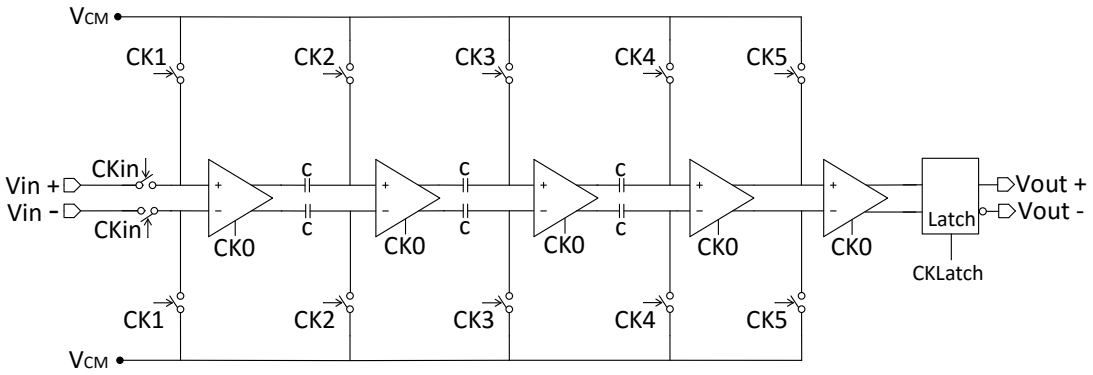

Figure 3.3: Designed comparator structure.

Since the offset voltage affects the linearity of the overall system, it should be cancelled. For the designed comparator, output offset cancellation method is used to decrease the offset voltage which gets on the input voltage of the latch.

3.1.1 The preamplifier stage

Preamplifier is the gain stage for comparator, and the gain should be as high as possible. Among fully differential structures, resistive loaded amplifier has common usage. For this work, between the resistive loaded and active loaded amplifiers a simple one is chosen, as shown in Figure 3.4. Resistive loads supply higher speed than active ones. Gain for the common source resistive load differential pair amplifier is shown in equation 3.2.

$$A_d = g_m \times R_L \tag{3.2}$$

where

$$g_m = \frac{2I_D}{V_{GS} - V_{th}} \tag{3.3}$$

The gain changes with transconductance and/or resistance. Transconductance of the input transistors depend on the tail current. It is clear that there is a trade-off between power consumption and gain. Considering the trade-off, the input resistor sizes and resistor values should be decided carefully. As it included in Table 3.1, the transistor sizes are set to $W/L = 10\mu m/0.18\mu m$, load resistors selected as $2.5K\Omega$, the tail current is set to $500\mu A$ and the $V_{ON} = V_{GS} - V_{th}$ set to $250mV$, which results in a gain approximately 5.

Table 3.1: W/L ratios for preamplifier.

	L (nm)	W (um)	Finger
MN1, MN2	0.18	1	10
MN3, MN4	0.5	3	10
MN5, MN6	0.18	1	10
MN0	0.18	4	1

One of the disadvantage of using resistive load is in matching difficulties, which we cannot achieve a very good matching in layout of resistor in contrast with active load

This matching problem causes current stabilization problem in two branches of differential pair, which must be considered in layout. Furthermore, tail current mismatch is another issue, which a small change in tail current will cause a change on the output common mode voltage due to resistive load, so to solve the problem we need to use the cascade current source to stabilize the tail current node.

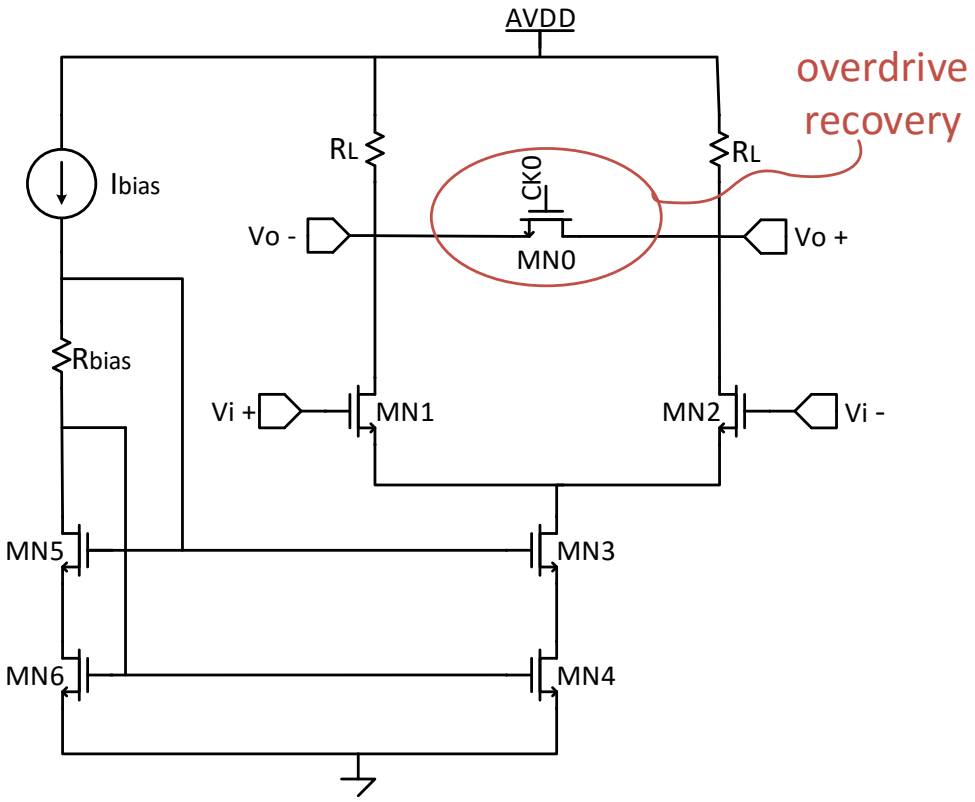

Figure 3.4: Preamplifier schematic.

An amplifier test bench is seen in Figure 3.5, and a graph of transient waveforms of the designed amplifier is seen in Figure 3.6. Amplifier settling time results can be seen in Figure 3.7.

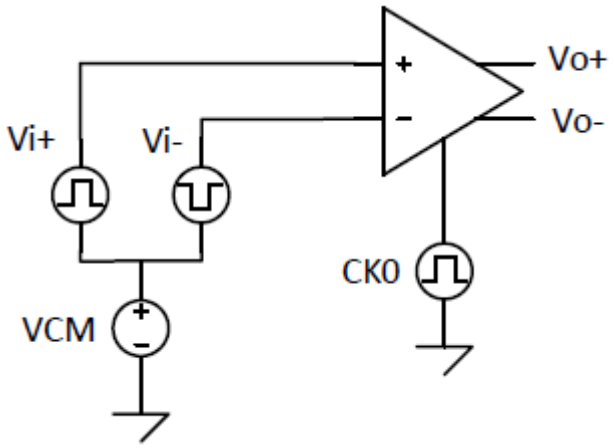

Figure 3.5: Preamplifier test bench.

According to Figure 3.6, a differential square wave of $\pm 2.5mV$ (which is smaller than ADC's LSB value of $3.9mV$) around a common mode voltage of $1.1V$ is given to the inputs of the amplifier and the outputs are depicted. Amplifier gain can be calculated as in equation 3.4,

$$A = \frac{V_{o+} - V_{o-}}{V_{i+} - V_{i-}} = \frac{1.171909 - 1.14704}{0.005} = \frac{24.87mV}{5mV} = 4.97 \qquad (3.4)$$

So, in ideal conditions we can expect the five stage amplification gain as,

$$A_{5-stage} = 4.97^5 = 3032 \qquad (3.5)$$

$$A_{5-stage} = 69\ dB$$

It is needed to have at least $50dB$ gain before latch, because the offset voltage of the latch is around $150mV$. $(V_{off,latch}/gain) < LSB$ is the limitation rule for the gain.

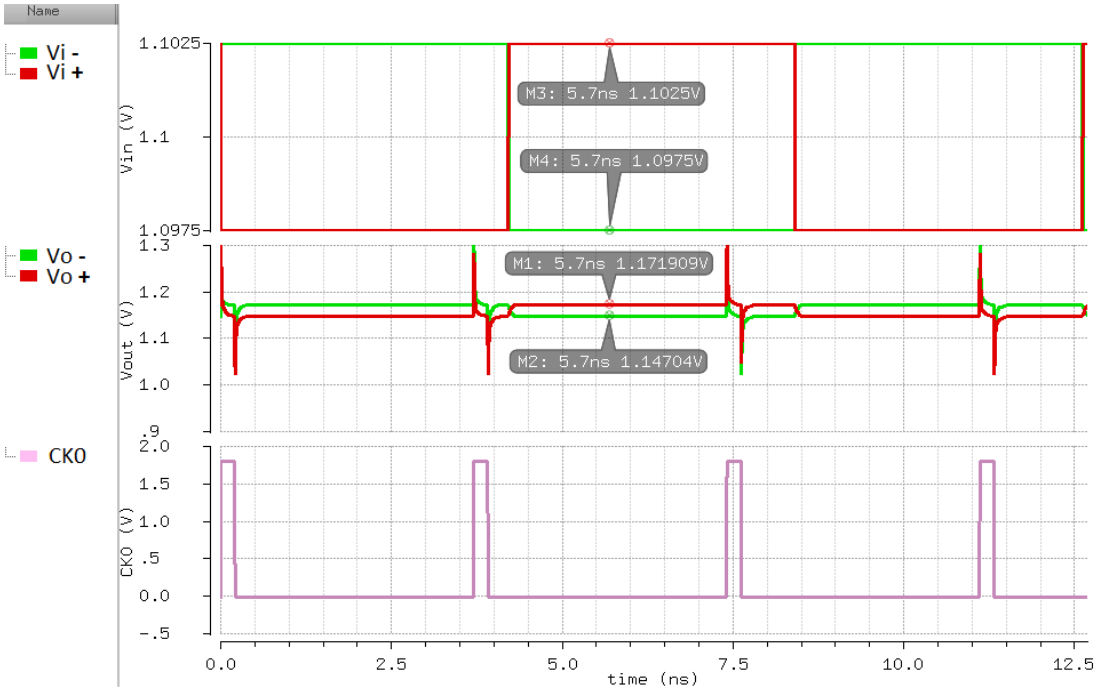

Figure 3.6: Preamplifier gain test results.

This gain value will be affected by the parasitic capacitance between gate of the input differential pair and common mode voltage source, which forms a voltage divider over offset storing capacitor $[C_{os}/(C_{os} + C_{Gp})]$. In order to keep this attenuation fair enough, we need to use a large offset storing capacitor, on the other hand, this will limit the speed of the amplifier, according to the simulation results $100fF$ of storing capacitors will be an optimum point.

Amplifier settling time can be measured as Figure 3.7, it can be seen that output of the amplifier settles to the %90 of its value at $85ps$.

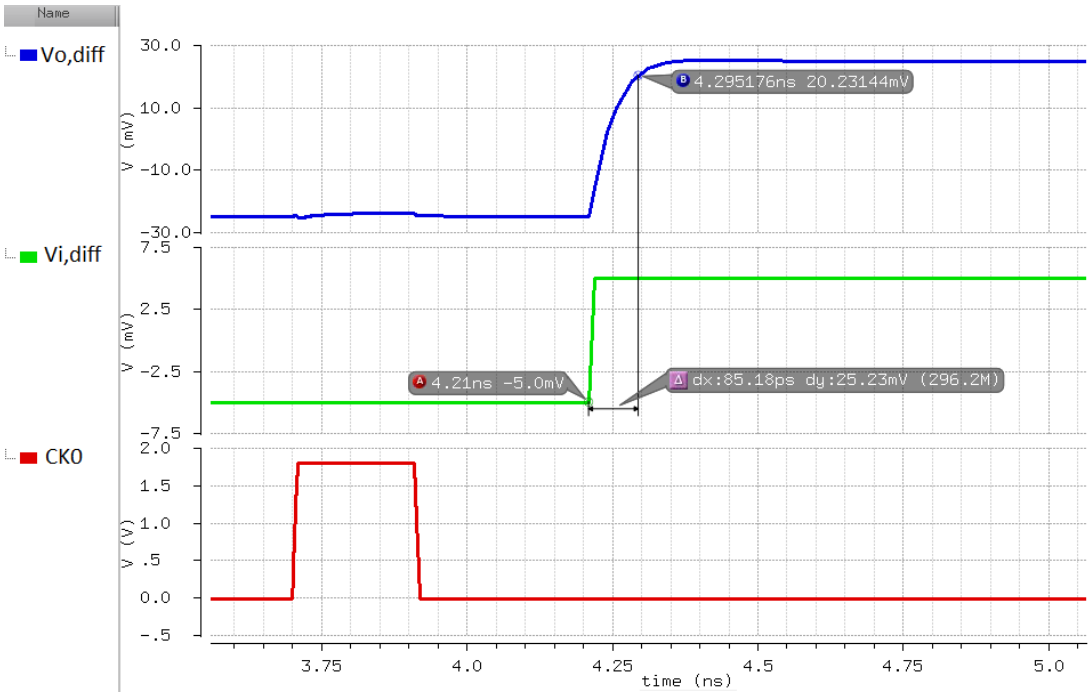

Figure 3.7: Preamplifier settling time test results.

3.1.2 Overdrive recovery

In preamplifier circuits, some effects create reliability or speed problems. One of them is about overdrive. Firstly, when inputs of the amplifier are set to large differential voltage, effecting on the gain of the comparator resulting the output of the gain stage to settle to either supply voltage (AVDD) or ground voltage (AGND). After this situation, if an input differential signal changes its phases, the amplifier requires a pre charging time to enable comparator to produce necessary output logic. To activate this operation the comparator takes a bit longer time in compare to its natural time. This extra time generally mentioned as comparator overdrive recovery time (t_{ov}).

To solve the overdrive recovery problem, a simple NMOS switch could be impacted between the differential outputs. When the switch is reset, outputs of the amplifier will be settled to output common mode voltages.

3.1.3 Offset cancellation

One of the effects, which is related to reliability of comparator, is offset voltage. For an amplifier, offset is a big issue. If there is a small voltage difference between the inputs and the offset voltage can get on the smaller input of the amplifier then the smaller input could be larger than the other input. After the amplification, the wrong

distance between the inputs will be higher and unrecoverable because the comparator will be wrong compare. For this problem, there are many cancellation techniques in the literature to cancel the effect of the offset, and it is chosen that cancelling via offset storage method for this work because of its lowest power dissipation.

Offset storing methods based on storing the offset voltage on a capacitor and add it to the signal to cancel the effects of the offset. Using output offset storing model instead of input model, allows using smaller capacitances. Offset cancellation is implemented to first three stage of the comparator, neither to last two amplifiers nor to latch. As suggested in (Gregorian, 1999), offset of the last two stages are not canceled, since their contribution on input referred offset voltage is negligible according to,

$$V_{in,off,n} = \frac{V_{off,in}}{A^n} \tag{3.6}$$

Where $V_{in,off,n}$ is input referred offset voltage of nth amplifier, $V_{off,in}$ is offset voltage of the nth amplifier and A is the gain of the amplifier.

The dummy switches without offset storing capacitors are used to prevent the asymmetry on layout for the latter two phases without offset storing capacitors.

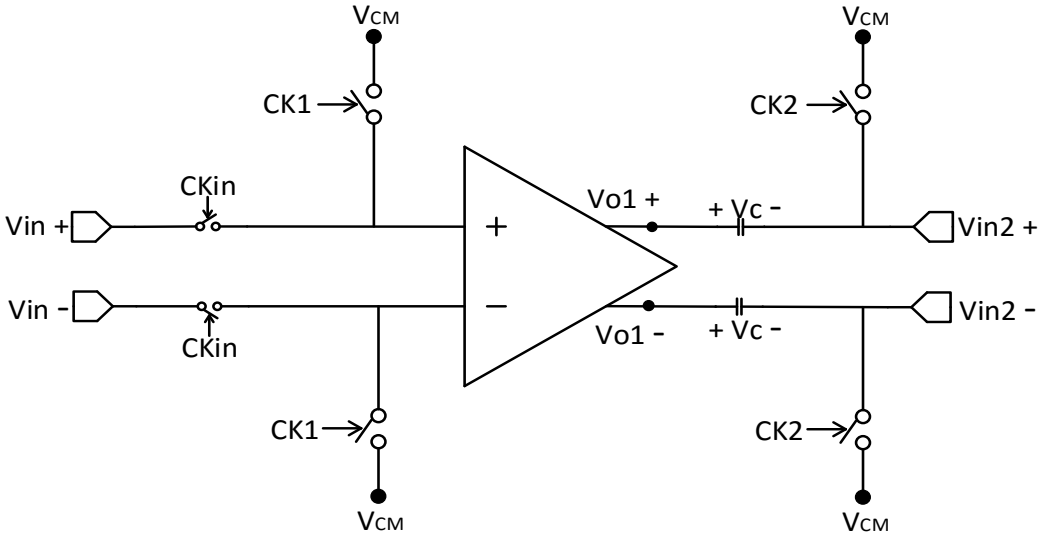

Figure 3.8: Output offset cancellation structure.

Output offset storing method cancels the offset at the output of each gain stage. In the Figure 3.8, it is shown that there is two phase. In the first phase, inputs of the whole preamplifiers are connected to the common mode voltage. This stage helps storing the

amplified input offset in the capacitors, which are at the output of the each preamplifiers. It is shown in the Figure 3.9 V_C is stored as

$$V_C = A \times V_{OFF} \tag{3.7}$$

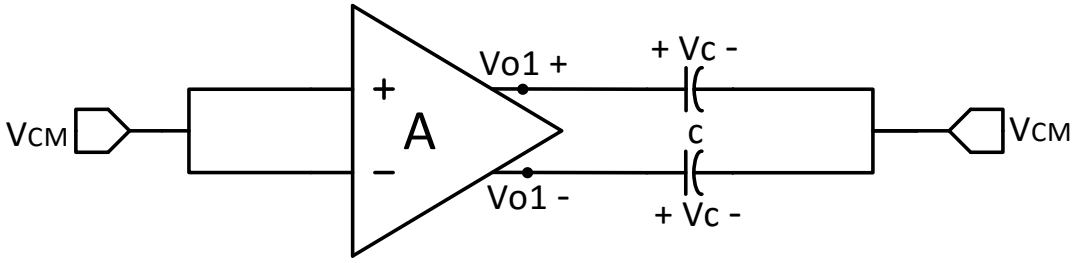

Figure 3.9: Offset cancellation first phase.

The second phase is comparison phase for the comparator. Therefore, the inputs of the first amplifier is connected to the input voltage V_{in+} and V_{in-} as Figure 3.10.

After calculated output voltage of the first amplifier, the input voltage of the second amplifier. V_{in2+} is calculated as in equation 3.8.

$$V_{in2+} = -V_C + V_{O1}$$

$$V_{in2+} = -A \times V_{OFF} + A \times (V_{in+} + V_{OFF})$$

$$V_{in2+} = -A \times V_{OFF} + A \times V_{in+} + A \times V_{OFF}$$

$$V_{in2+} = A \times V_{in+} \tag{3.8}$$

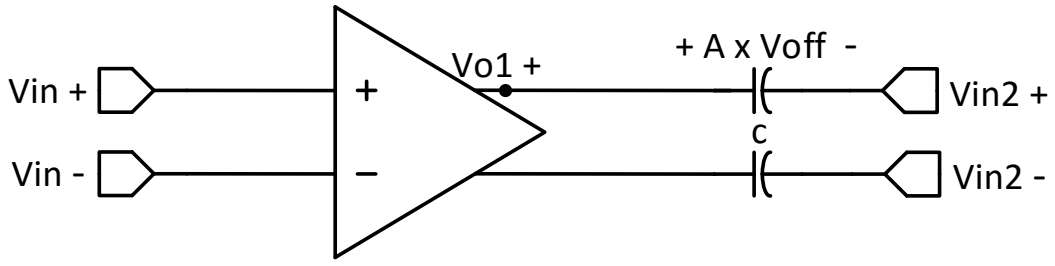

Figure 3.10: Offset cancellation second phase.

As it seen from this procedure, the offset voltage of first stage is clearly removed. This solution will be impacted to other stages and the offset voltage will be out of question for the preamplifier stages.

3.1.4 The latch

Latch block is used in order to be sure that the output of the comparator saturates to logical levels for any input values difference. As in Figure 3.11, the latch is a high gain stage with its logical level outputs and positive feedback. The preamplifier stages amplify the difference between the inputs, then the latch saturate to the logic level corresponding to the V_{in+} and V_{in-}. Small input signals of the latch always cause wrong decision at the output because the latch has a large input referred offset voltage. The decision time of the latch is related with the input magnitude. To avoid longer decision time, preamplifier stages are needed to increase the magnitude of the signal as much as possible.

Latches are used as data storage elements. Previous state of the latch causes the memory effect and changing the current state takes more time. In addition, this effect causes the harmonic distortion. Delay of the whole system is determined by latch stage, so it is needed to create results at the right logic level and at the right time as well. The systematic errors are needed to avoid, which caused by latch.

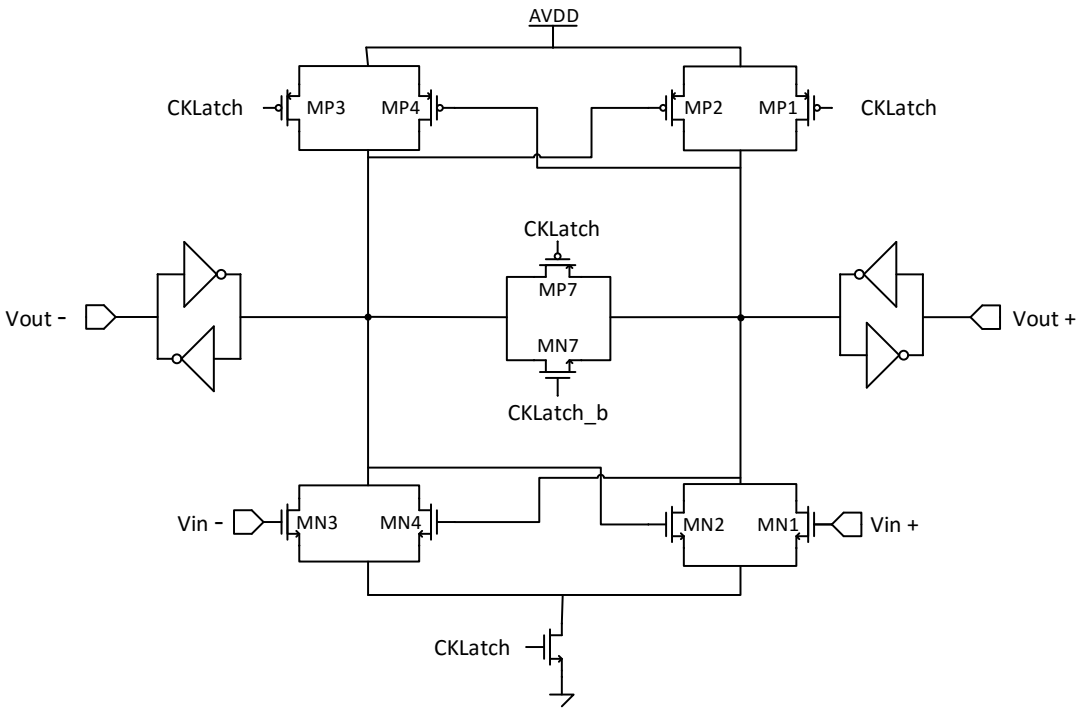

Figure 3.11: Latch structure.

The most important situation for the latch is when a large differential input voltage is applied after a small one. At that moment, the latch could not set itself easily so it is mentioned to test critical points at the next section, included in comparator test results.

As it stated before, there are two positive feedbacks. One of them is easily seen from the Figure 3.11 that is between a cross-connected PMOS transistor couple and a cross-connected NMOS transistor couple. Moreover, the other positive feedback is seen at the outputs that two cross-connected inverters, which can quickly drive next stage.

3.1.5 Comparator operation and test

The test bench of the comparator is designed as in Figure 3.12, its clock signals are determined as Figure 3.13, and the simulation of the comparator is performed.

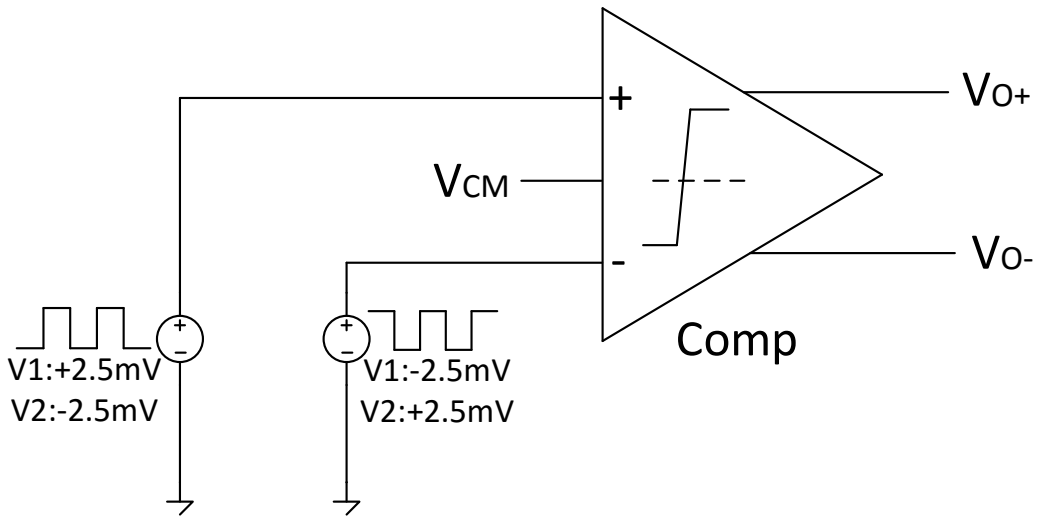

Figure 3.12: Comparator test bench.

The investigated schematic of the comparator is given in Figure 3.3. During the reset phase that is also sampling phase of the DAC and offset cancellation phase of the comparator at the same time, the $CK0$ signal rises to recover the differential output overdrive firstly. Shortly after each $500ps$, the offset is stored by output referred capacitors one by one with the rising edge of $CK1, CK2, CK3, CK4, CK5$ input clock signals. All the overdrive recovery and offset cancellation operations are performed within reset phase. After the sampling phase of the DAC, comparison of the SAR logic is started and the following 8 clock cycles with $6ns$ period time for each are used for data comparison of 8-bit data. At the beginning of the comparison phase, the $CKin$ signal rises to connect the output of the DAC to input of the comparator. After some

time to allow pre amplification process, the latch stage is activated by $CKLatch$ signal. Then the output of the latch is sent to the SAR logic block.

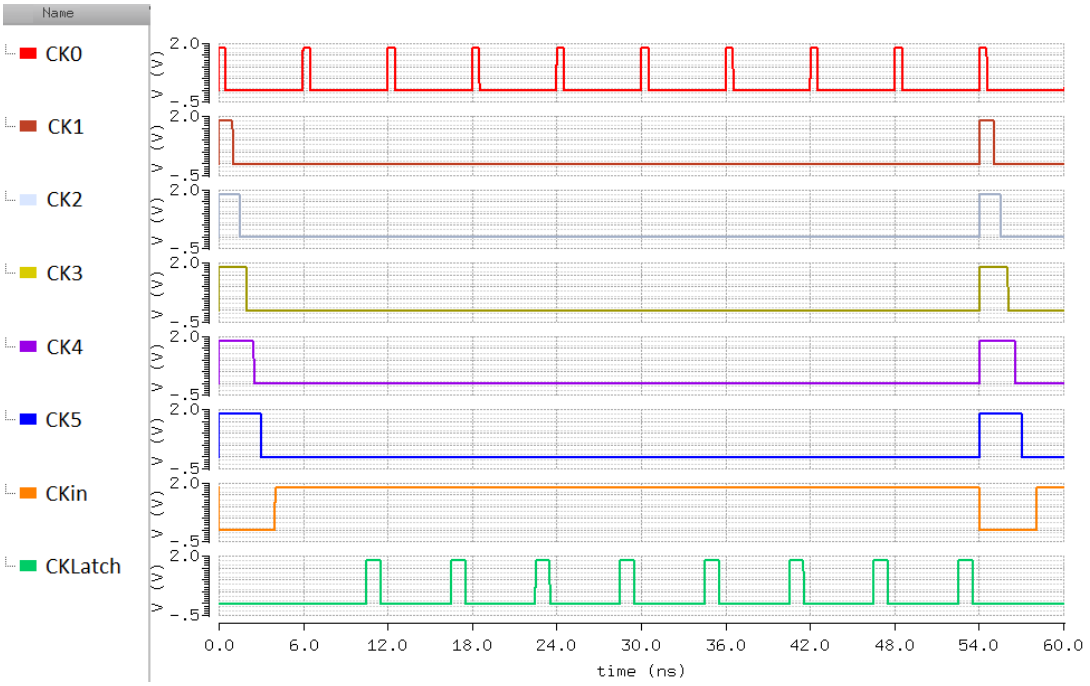

Figure 3.13: Comparator clock signals.

In order to test the offset cancelation circuit, an offset of $0.2\mu m$ is added to the width of amplifier differential pair intentionally. It is applied by making the $W_1/L_1 = 10.2\mu m/0.18\mu m$ and $W_2/L_2 = 9.8\mu m/0.18\mu m$, as it can be seen from Figure 3.14. A $19.69mV$ offset is appeared at the output of the amplifier. After applying the $CK1$ and $CK0$, the offset at the input of the second amplifier is basically zero volt.

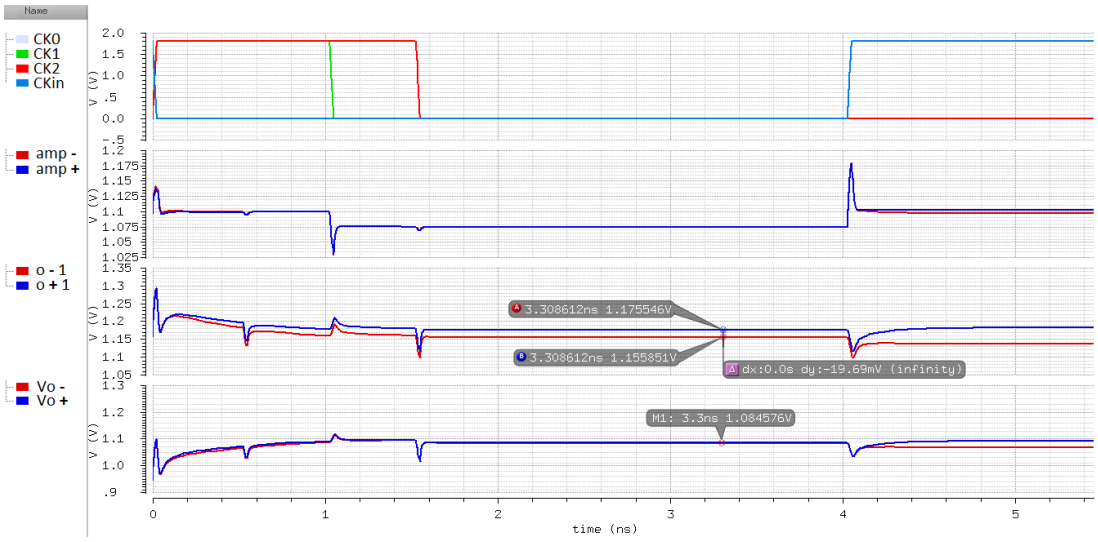

Figure 3.14: Comparator offset cancelation process.

As it represented in Figure 3.13, the $CK0$ signal is switch control signal of the overdrive recovery. Each cycle of the comparator is made ready by $CK0$ signal. $CK1, CK2, CK3, CK4, CK5$ are control signals of the offset cancellation switches. These signals are short circuited to the input and output nodes of the preamplifiers. The common mode voltage V_{CM} and the cancellation method is done in one conversion, which takes 9 cycles. The reason is, during the ADC operation phase, new input signal is not applied to the comparator so the offset is constant and there is no need to re-store it over offset storing capacitors anymore. $CKin$ controls the input voltages $V_{in\pm}$. In addition, the $CKLatch$ signal controls the latch stage as well.

Comparator is tested in PVT corners and Monte-Carlo analysis. Monte-Carlo at PVT corners of $(SS, TT, FF, 1.71V, 1.8V, 1.89V, -40°C, 0°C, 27°C, 85°C, 105°C, 125°C)$ are tested and comparator passed these corners completely with zero bit error rate. Comparator output voltage across corners can be seen in Figure 3.15.

According to further Monte-Carlo analyses, the comparator found to operate properly with zero bit error rate (BER) up to 510 MHz speed. In addition, it is analyzed at 125°C with a precision of $4mV$ differential input voltage.

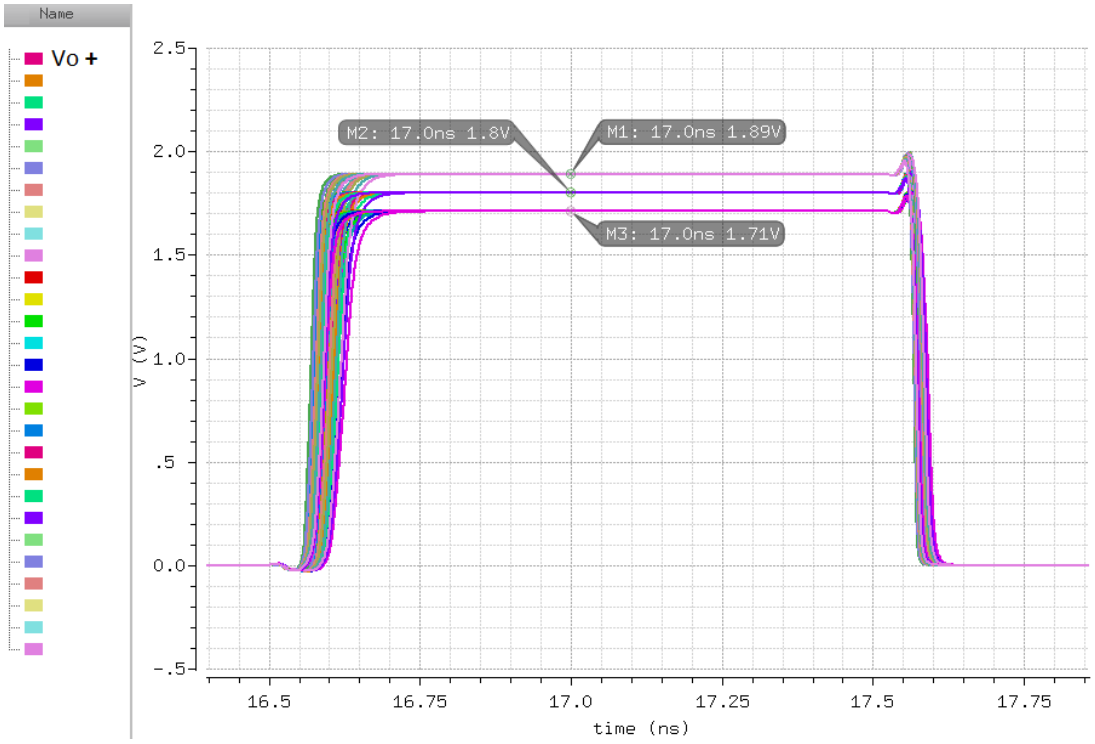

Figure 3.15: Comparator corner simulation.

With the explained signals, the comparator is analyzed for the most critical points of the input voltages. The small differential input signals are applied to inputs of the comparator about $5mV$ and $25mV$, then large signals are applied around V_{FS} voltages. The output waveform shows that comparator can toggle easily and correctly as shown in Figure 3.16. Total gain of the five stage amplifier before the latch stage can be calculated as below,

$$A_{5\,stage} = \frac{latch\_in_{+} - latch\_in_{-}}{V_{i+} - V_{i-}} = \frac{1.81 - 0.243}{0.005} = 313.4 \qquad (3.9)$$

$$A_{5\,stage} = 49.92\ dB$$

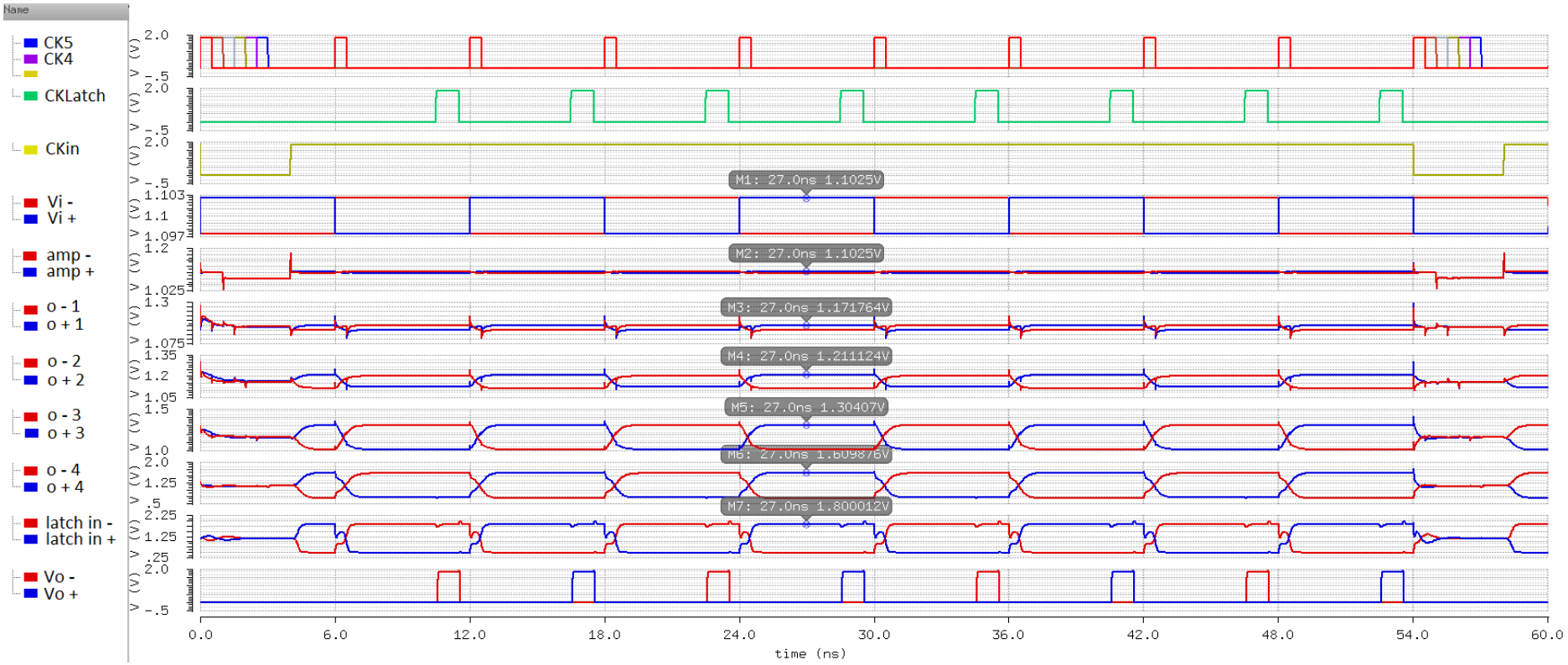

Figure 3.16: Comparator stages input, outputs waveforms.

3.2 The DAC

In a SAR ADC, DAC is one of the main blocks, because the linearity of the SAR ADC depends on the linearity of the DAC and the DAC has so much power consumption (Liu, Chang, Huang, & Lin, 2009) (Chen, et al., 2009). To reduce the power dissipation, resistor based DAC is not used. Capacitor array DAC has much lower power consumption in comparison to the resistor based DACs. However, power consumption of the capacitive array DAC is still high. In addition, in high resolution SAR ADCs, values of the DAC's capacitors increase exponentially with the number of bits. For an n-bit binary weighted capacitor array DAC, the capacitor value is calculated as

$$C_i = 2^{i-1} \times C \tag{3.10}$$

where $i = \{1, \dots, n\}$. As it seen from the equation 3.10 and Figure 3.17, for each bit the value of the capacitor increases. The total capacitance for the DAC is calculated as

$$C_{total} = (1 + 1 + 2 + 4 + \cdots + 2^{n-1}) \times C \tag{3.11}$$

$$C_{total} = 2^n \times C$$

where the total capacitance is C_{total} and the unity capacitance of the DAC array is C. As we can see from total capacitance equation 3.11, the method is not practical to use binary weighted capacitor array structure for more than 5-bits (Yee, Terman, & Heller, 1979).

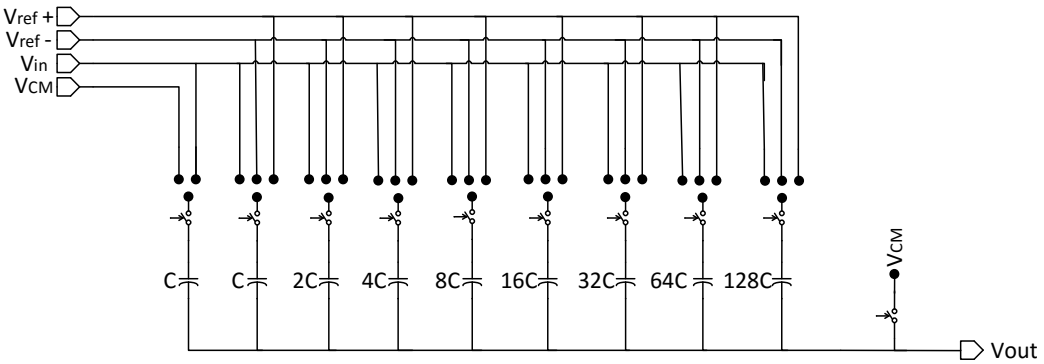

Figure 3.17: Binary weighted capacitor array DAC structure.

The different types of binary weighted capacitor array structure are mostly popular, which is used in SAR ADCs as reported in (McCreary & Gray, 1975) (Suarez, Gray,

& Hodges, 1975). It has two operation phases, first one is reset phase, top plate and bottom plates are short circuited to common mode voltage to discharge the capacitor array in this phase. Second, is conversion mode, during this phase, top plate is open circuited and bottom plates are short circuited to either common mode or reference voltage according to digital input code. The equation 3.11 is implemented in Figure 3.17. The value of capacitor is increased by increasing the number of bits. Therefore, disadvantages of this structure are high switching power dissipation, large chip area because of the bigger capacitors, long settling time to drive bigger capacitors.

Unity capacitor value is determined by not only technological limits but also matching and noise requirements. It is impossible to reduce it further below a limit value. In addition, split capacitor array structure is used to reduce the large capacitors without decreasing unity capacitor value.

3.2.1 Split capacitor array

Among capacitive DACs' structures, split capacitive array architecture is used commonly such as (Du, Ning, Zhang, Yu, & Liu, 2013) (Liu, Chang, Huang, & Lin, 2010) (Arian, Saberi, & Hosseini Khayat, 2011). The split capacitor array reduces the total area of the capacitors required for high resolution DACs. As shown in Figure 3.18 a serial attenuation (bridge) capacitor separates the binary weighted DAC in two arrays as MSB array and LSB array (Yee, Terman, & Heller, 1979). In split capacitor array DAC structure, the equivalent capacitances are seen by the MSB array side as unity capacitance of the DAC. With this structure, the total capacitance of the DAC is reduced.

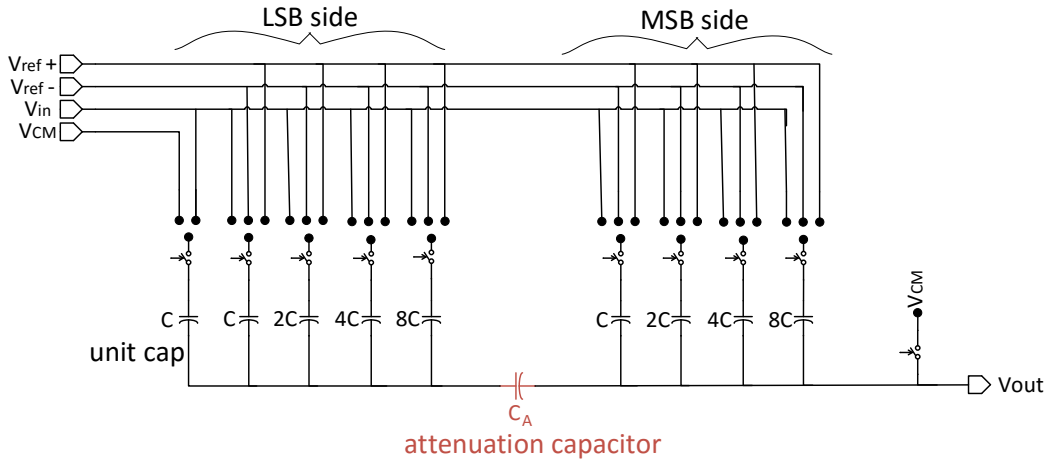

Figure 3.18: Split capacitor array DAC structure.

In this structure, the equivalent capacitance on the LSB side with attenuation capacitor should be equal to unity capacitance C. So calculating the total capacitance of the split array DAC shows

$$C_{total} = (LSB\ side\ cap\ series\ to\ Attenuation\ cap)//\ (MSB\ side\ cap) \quad (3.12)$$

$$C_{total} = C//\left[(1 + 2 + 4 + \cdots + 2^{(n/2)-1}) \times C\right]$$

$$C_{total} = 2^{n/2} \times C$$

The total capacitance is decreased to square root of binary weighted form as it seen from the equation 3.12. For an 8-bit split array DAC, the total capacitance equal to

$$C_{total} = 2^{8/2} \times C = 16 \times C$$

The designed DAC converts 8-bit data as it seen in Figure 3.19, it is formed as a fully differential binary weighted split switched capacitor array DAC. With fully differential operation, two different split array come up for positive and negative outputs.

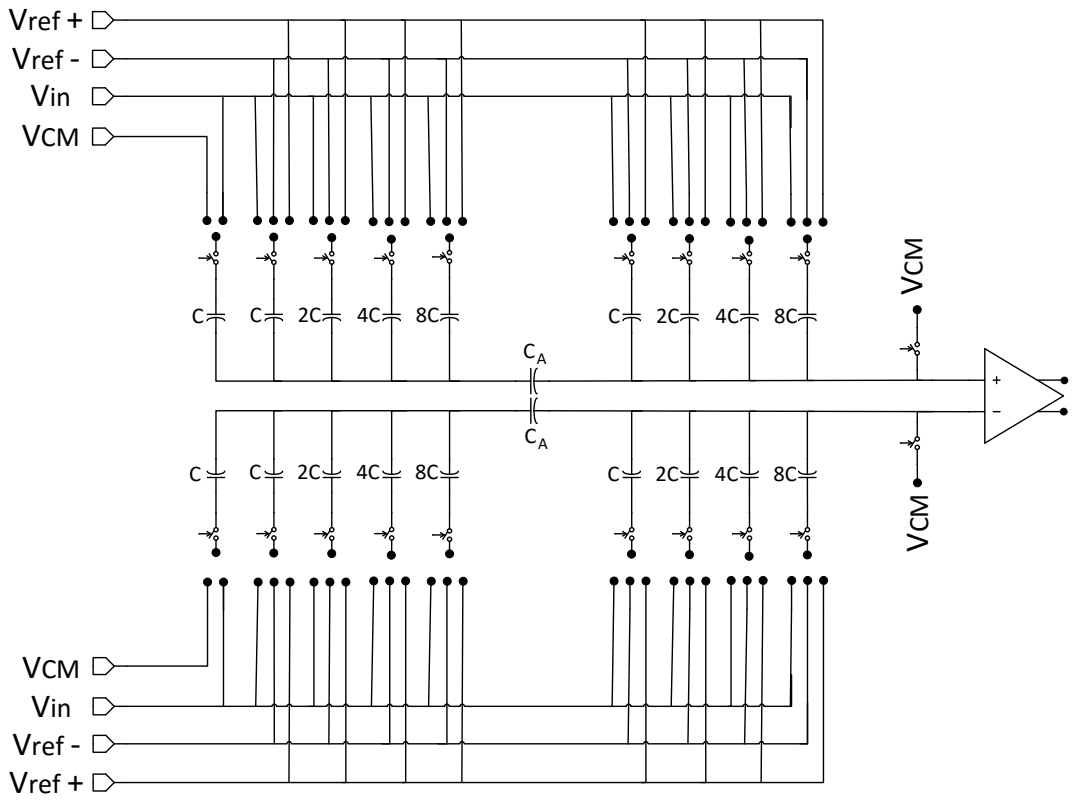

Figure 3.19: Designed fully differential DAC structure.

If the fully differential binary weighted split switched capacitor array DAC structure is investigated in detail, two phases of operation are seen as reset and conversion. In addition, the reset operation is realized as sample&hold function. Before a deep explanation for these phases, it is needed to determine unity capacitance C and attenuation capacitance C_A according to thermal noise and time constant.

The unity capacitance value is decided according to thermal noise, time constant, and bandwidth. Also, it is related to resistor value of the switch (transistor R_{ON}). Thermal noise ($\overline{V_n}$) is also called as Johnson-Nyquist noise. It is the electronic noise, which occurs because of the thermal incitement of electrons, which happens without applied any voltages. The most noise sensitive operation of an analog to digital conversion is sampling function. Moreover, the noise affects the accuracy drastically. The value of the sampling capacitor is reversely rational to input referred thermal noise, and the thermal noise is needed to be as small as possible. It is useful to investigate the thermal noise deeply.

$$\frac{1}{2}\,LSB = \overline{V_n} \tag{3.13}$$

$$\overline{V_n}^2 = \frac{kT}{C} \tag{3.14}$$

Where LSB for the designed DAC is $3.9mV$ for each branch, k is the Boltzmann constant, T is the temperature in $°K$ and C is the sampling capacitor's value in Farad. Therefore, the minimum C value can be calculated as equation 3.15 to overcome thermal noise where the maximum operation temperature is expected to be 125°C equals to 398°K,

$$\left(\frac{1}{2}\,LSB\right)^2 = \frac{k \times T}{C_{min}}$$

$$\left(\frac{1}{2}(3.9 \times 10^{-3})\right)^2 = \frac{1.38 \times 10^{-23}.398}{C_{min}}$$

$$C_{min} = 1.44\ fF \tag{3.15}$$

The minimum $1.44fF$ capacitance is needed to overcome the thermal noise while sampling operation. With these calculations, it is known that the thermal noise is not an issue for designed 8-bit DAC.

It is clear that the thermal noise power rises with increasing temperature and decreasing sampling capacitance. When the C needs to be as large as possible, the noise voltage would stay below $half\ LSB$ and it would not affected from the thermal noise power. Beside thermal noise, the C needs to be as small as possible to make the time constant small. It is important with restricting the maximum frequency.

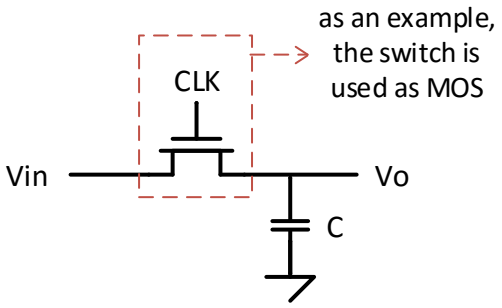

Figure 3.20: Equivalent circuit for the sampling network.

As shown in Figure 3.20, when an input voltage loads a capacitor through a switch, settling to desired voltage level takes time. In the modelled switched-capacitor serial RC network, the channel resistance of the transistor is assumed R_{ON}, the voltage on the capacitor is shown in equation 3.16 as time domain solution.

$$V_C(t) = V_{in}(1 - e^{-(t/\tau)}) \tag{3.16}$$

where $\tau = R_{ON} \times C$. The equation 3.16 is rearranged to get settling time as in equation 3.17.

$$\frac{V_C}{V_{in}} = (1 - e^{-(t/\tau)})$$

$$\ln(\frac{V_C}{V_{in}}) = 0 - (-\frac{t}{\tau})$$

$$t = \ln(\frac{V_C}{V_{in}}) \times \tau \tag{3.17}$$

The settling time is calculated as seen in equation 3.17. It is clear that the settling time is related time constant and logarithmic function of the voltage of input and capacitance. For an 8-bit settling accuracy for an RC network, settling time can be calculated as equation 3.18.

$$t = \ln\left(\frac{1}{1/(2^8 - 1)}\right) \times \tau = 5.5 \times \tau \tag{3.18}$$

If we choose the unit capacitance value $50fF$, the total sampling capacitor of capacitor network is equal to

$$C_{total} = 2^4 \times C = 16 \times 50fF = 800fF \tag{3.19}$$

The total sampling capacitor C_{total} is equal to $800fF$ for each two side capacitive array. The sampling capacitor value is also beyond the needed thermal noise value. Furthermore, $R_{ON} = 1K\Omega$ can be assumed as a start point, then the settling time can be calculated using equation 3.18,

$$t = 5.5 \times R_{ON}C = 4.4\, ns \tag{3.20}$$

This settling time limits the speed of the ADC and need to be reduced, the time that can be logical according to the whole system timing plan is $3.5ns$, in order to have $3.5ns$ settling time it is needed to have $R_{ON} = 800\Omega$.

Nevertheless, it must be remembered that there is a tradeoff between thermal noise and time constant as it seen from the previous equations. Moreover, reaching the desired bandwidth helps to detect maximum R_{ON} related to C.

$$BW = \frac{1}{2\pi R_{max}C} \tag{3.21}$$

According to all these limitations, if it is assigned as $1GHz$ bandwidth and $50fF$ to C capacitance, the maximum resistance value could be calculated as;

$$BW = \frac{1}{2\pi R_{max}50fF} \tag{3.22}$$

$$R_{max} = 200\Omega$$

With the $1GHz$ bandwidth and $50fF$ capacitance, the maximum value of the resistor is defined as 200Ω. Therefore, the settling time for the designed system is equal to

$$t = 5.5 \times R \times C = 5.5 \times 200 \times 0.8pF = 0.88\,ns \tag{3.23}$$

To propose the fully differential binary weighted split switched capacitor array DAC structure, it is needed to divide the architecture in two sides, as it explained before. The attenuation capacitor is stated between these sides. The value of attenuation capacitor is very important to achieve a good linearity for DAC. It is proved that the C_A almost equal to unity capacitance (Ozkaya, 2010). It is calculated for 8-bit as

$$C_A = \frac{sum\ of\ the\ LSB\ array\ capacitors}{sum\ of\ the\ MSB\ array\ capacitors} \times C = \frac{16}{15}C \tag{3.24}$$

Here the sum of the MSB array capacitors equal the sum of the LSB array capacitors minus C (Bekal, Goswami, Singh, & Pal, 2014). The attenuation capacitor C_A introduces top and bottom plate parasitic. The systematic error caused by parasitic capacitances of C_A is needed to be corrected for more than 10-bit resolution. For higher resolutions, the calibration becomes necessary.

3.2.2 The switches

The MOS switches' current flow through the transistors are shown in Figure 3.21 to compare the working voltage levels of switch types. If the input signal changes from ground to supply rail, using a transmission gate switch is convenient. This type of switch is formed from parallel connected an NMOS and a PMOS transistors. With this way, parallel-connected R_{ON} resistances of the transistors are in low ranges in whole swing levels.

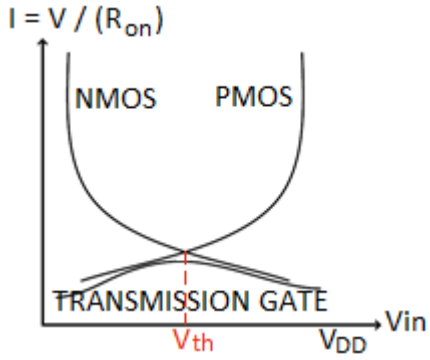

Figure 3.21: Different switch topologies R_{ON}.

The on resistance of an NMOS transistor in the linear region is given in equation 3.25.

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{in} - V_{th})} \tag{3.25}$$

It is seen from the equation 3.24 to achieve a lower on resistance, the bigger size of transistor is needed. Because of bigger transistor, threshold voltage is getting higher. To improve the dynamic range of the input, $3.3V$ transistors are implemented for sampling switches. To be able to sample both the lower and higher regions of the analog input voltage swing, the sampling switches are designed as transmission gate switches. At the same time, the R_{ON} is decreased automatically because of the parallel transistors connections.

There are always some drawbacks, so making them minimum is important to achieve systems that are more reliable. For the CMOS switches, charge injection and clock feedthrough effects are major error sources.

Clock feedthrough mechanism occurs when the switch is turned off, dispersing the charge in the inversion channel, forcing current to flow either into the substrate or the load capacitor at the MOSFET drain or source (Xu & Friedman, 2002).

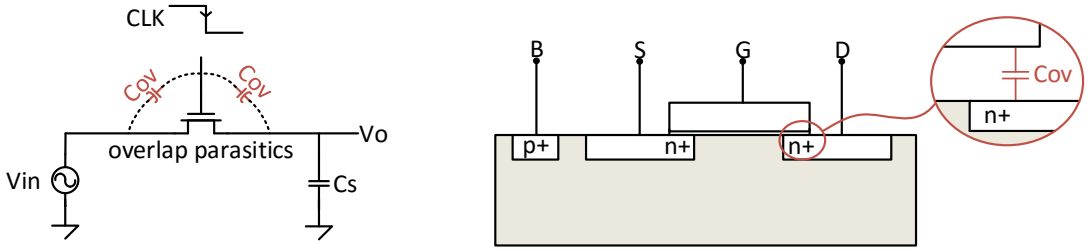

Figure 3.22: Overlap capacitances.

The effect is caused by the gate-drain or gate-source overlap capacitances C_{OV}, the signal on gate terminal which controls the switch feeds the input through the overlap capacitance (Xu & Friedman, 2002). An NMOS switch is shown as an example in Figure 3.22, when the clock signal goes to ground from supply voltage, for capacitance the total change of sampled voltage is equal to

$$\Delta V = -V_{DD}\frac{WC_{OV}}{WC_{OV} + C_S} \tag{3.26}$$

where C_S is the sampling capacitance. As it seen from the equation 3.26, clock feedthrough causes the voltage change, but it is independent from the input signal. It means that the clock feedthrough causes voltage offset. The offset depends on dimensions of the switches (Razavi, 2001).

On the other hand, charge injection is more critical effect, because it creates an input signal dependent sampling error, which is a source of nonlinearity. Firstly, a MOS transistor is turned on and a channel is formed by absorbing certain amount of channel charge from its terminals. Then the transistor is forced to turn off by a slowly decreasing voltage and the charge has to be injected outside through the terminals of transistor and the channel disappears. With this process, there is no important situation on sampling capacitor. However, if the formed channel is forced to cut-off very quickly, the channel could not disappear as quickly as wanted. Moreover, the channel charge continues to be injected to the sampling capacitor. This effect is too complex to be modeled adequately, but it is assumed that half of the channel charge is injected through drain terminal, remained channel charge is injected through source side (Razavi, 2001).

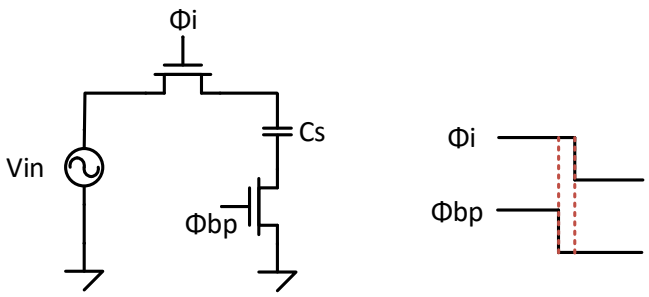

Figure 3.23: Bottom plate sampling.

There are some solutions for the charge injection effect. To mention one of them, it is called as bottom plate sampling method. As it presented in Figure 3.23, an additional switch (bottom plate sampling switch) is put after the sampling capacitor. Slightly before to turn off the sampling switch, the bottom plate switch is turned off to make floating sampling capacitor to not be injected the channel charge onto the sampling capacitor when sampling switch gets off (Maloberti, 2007).

In addition, there is another way to eliminate the charge injection. In analog input sampling switch method, a second transistor with half in dimension is connected in series with the main switch, source and drain terminals of the dummy switch are shorted, and clocked inversely. The dummy switch has the same channel length. When the transistor goes to off state from the on state, the channel charge continues to flow over the capacitance and tries to be disappeared. While the channel is disappearing, the channel of the serial transistor is formed and pulled the charge injected from the switch to be cleared away its channel. By selecting half width of the original transistor for the dummy transistor, a large part of the charge injection is cancelled. Because, when the dummy switch needs to establish its channel, the same amount of charge is injected through sampling switch and absorbed by dummy switch. The expression is given for a simple NMOS or PMOS switch, so it is needed to tend on the transmission gate switch. The analog input sampling method for transmission gate switch is shown in Figure 3.24.

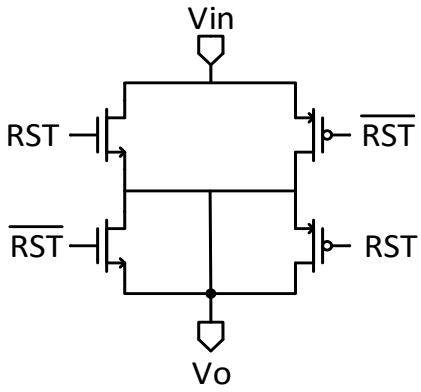

Figure 3.24: Analog input sampling transmission gate switch.

At the end, the total resistance of the series connected bottom plate and top plate sampling switches has to be less than 200Ω as calculated in equation 3.22. So the R_{ON} resistance is assumed 100Ω for each switch. The 16 parallel switches are included as the input sampling switch. It is obvious that to reach the desired R_{ON} is sufficient if each of these parallel switches has $1.6k\Omega$ R_{ON} resistance. A figure of R_{ON} across the full scale voltage range can be found in Figure 3.25. The selected switch on resistances have a margin to pass the corners simulations, too. A result of PVT corners simulation is available in Figure 3.26. Since SS corner is rare, having a slightly larger resistance is not considered as a big problem at that corner.

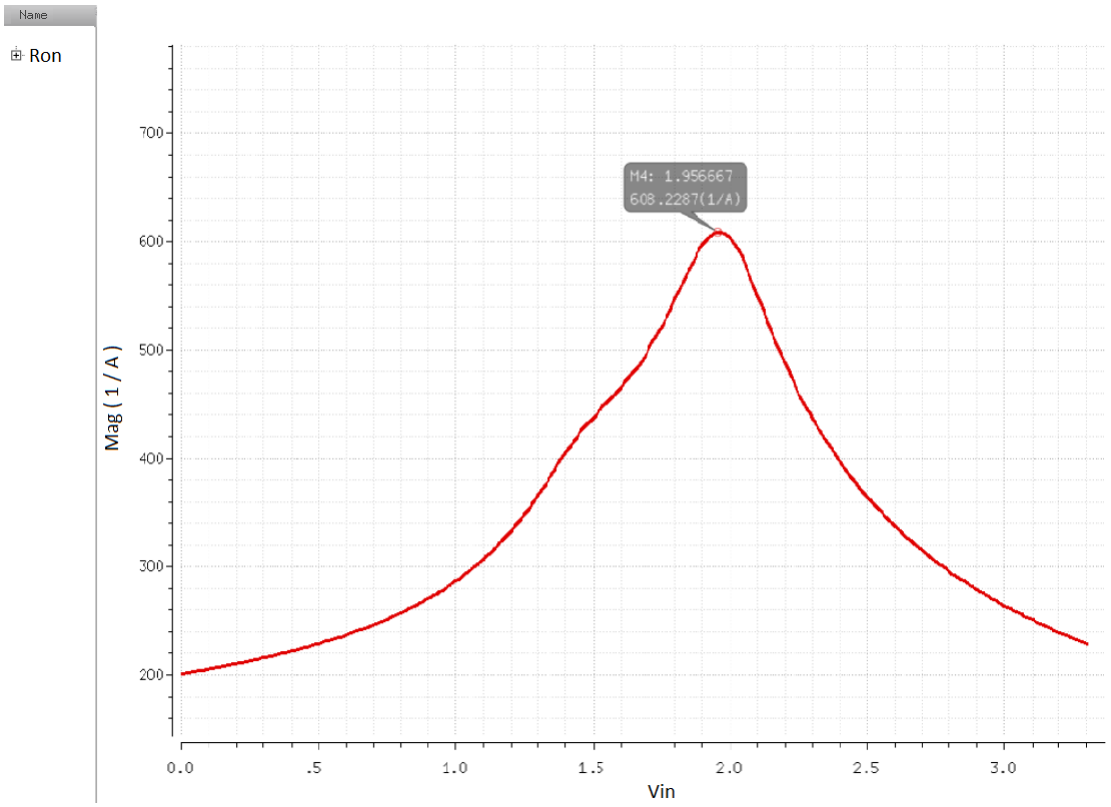

Figure 3.25: Input sampling switch R_{ON}.

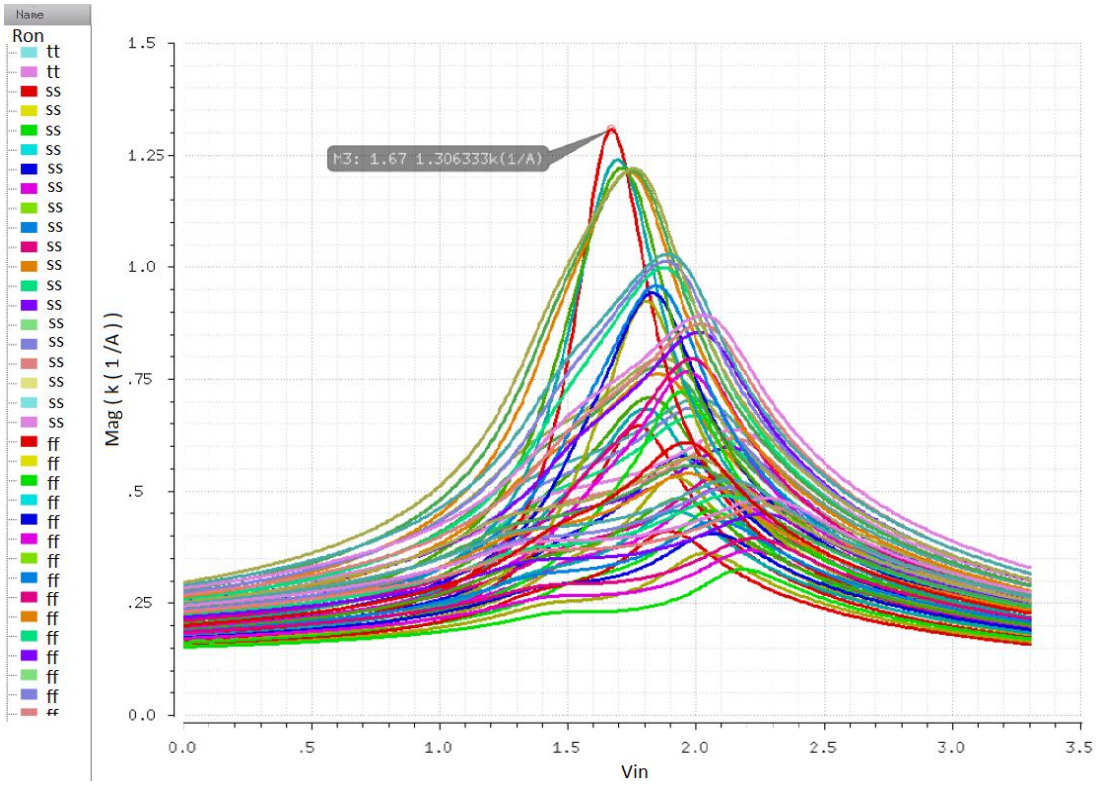

Figure 3.26: Input sampling switch R_{ON} across PVT corners.

For the designed DAC, it is needed to create single, double, and triple switches. For the switch, which is stated at the output of the DAC, is designed as single analog input

sampling switch. The redistribution capacitance is connected to the double analog input sampling switches. Remaining switches are renamed as bottom plate sampling switches and they are designed as triple analog input sampling switch. The triple analog input sampling switch is used for it because the bottom plate capacitances need to connect three different voltages according to the input voltages. As an example, the triple analog input sampling switch is showed in Figure 3.27.

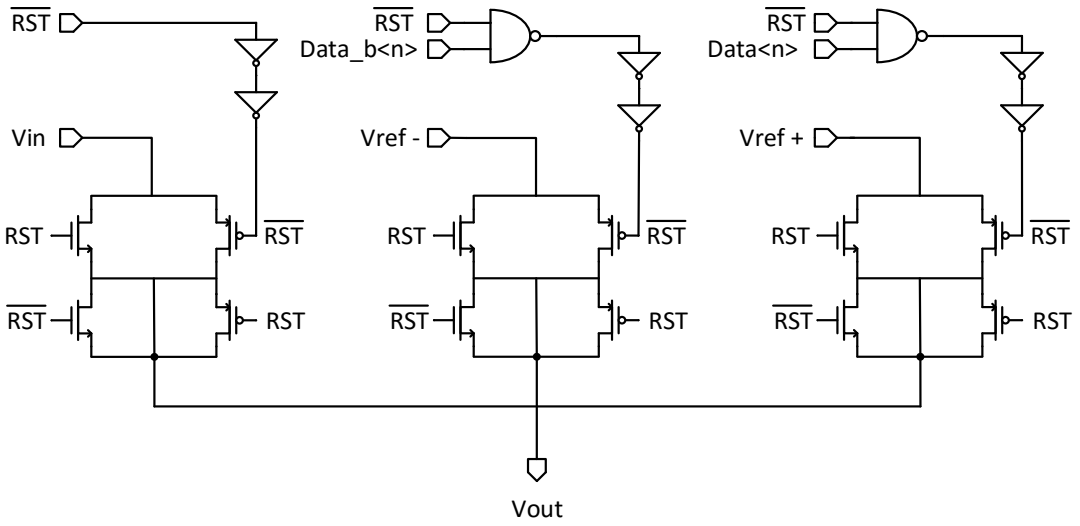

Figure 3.27: Triple switch schematic.

3.2.3 DAC operation and test

The split capacitor array DAC serves two aims in a SAR ADC. Firstly, it samples the input signal. Secondly, it generates a voltage between the input signal and current digital data comes from SAR logic block.

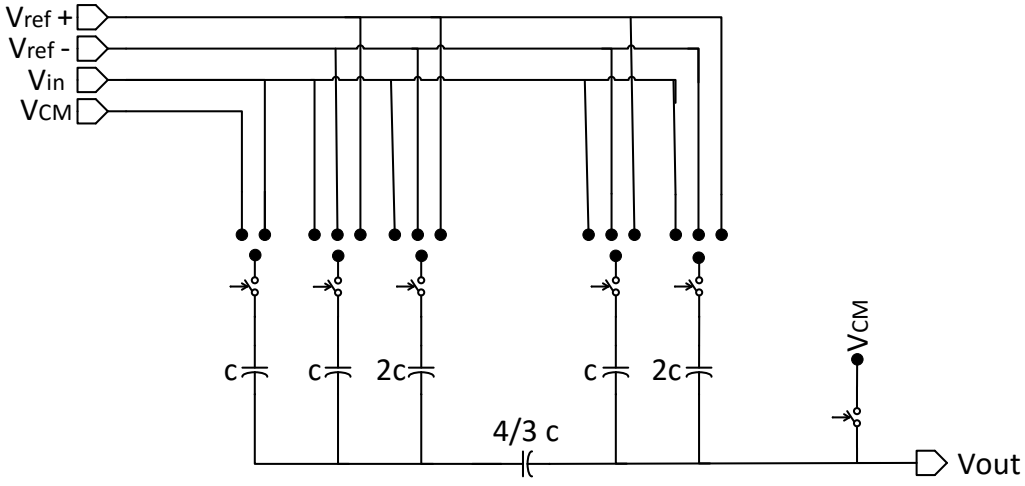

Figure 3.28: 4-bit example of split array DAC.

To demonstrate the operation, a conversion of 4-bit split capacitor array is presented in Figure 3.28 as an example. During the sampling phase, top plate is connected to common mode voltage V_{CM} and the bottom plates are connected to input voltage V_{in}. On this phase, the stored input voltage is obtained on the top plate (Son, Majid, & Musa, 2012). Then the conversion mode comes up. During this phase, top plate is connected to output as a floating node, bottom plate of unity capacitance is shorted to common mode voltage and bottom plates of remaining capacitance are connected to either positive or negative reference voltage according to digital input code. For the first bit decision after sampling phase, just the MSB capacitor is connected to reference voltage $V_{ref\pm}$ to establish the 1000 as initial value. At the same time, the comparator compares the sampled data and common mode voltage, it decides that the sampled data (1000) is higher or lower. After the decision of first bit, the output voltage is calculated as

$$V_O = V_{CM} \pm \frac{V_{ref\pm} \pm V_{CM}}{2} \tag{3.27}$$

During the second bit cycle, according to output of the comparator

$$V_O = V_{CM} \pm \frac{V_{ref\pm} \pm V_{CM}}{2} \pm \frac{V_{ref\pm} \pm V_{CM}}{4} \tag{3.28}$$

Then the remaining bits continue as

$$V_O = V_{CM} \pm \frac{V_{ref\pm} \pm V_{CM}}{2} \pm \frac{V_{ref\pm} \pm V_{CM}}{4} \pm \frac{V_{ref\pm} \pm V_{CM}}{8} \pm \frac{V_{ref\pm} \pm V_{CM}}{16} \tag{3.29}$$

One conversion is completed for 4-bit split array DAC. If an 8-bit DAC is considered, the process will continue as well.

The references voltages are selected as $V_{ref+} = 1.6V$ and $V_{ref-} = 0.6V$ around the common mode voltage $V_{CM} = 1.1V$. V_{in+} and V_{in-} are given as a ramp to define different voltages for different on times, because DAC needs to sample the input successfully. $Reset$ and $Reset\ Common\ Mode$ signals control the switches, which are enrolled in the DAC and generate to charge the capacitors. Pulse width of the $Reset$ signal is larger because of creating floating capacitor, as it stated before. 8-bit data should input from SAR logic block, as it seen in the test bench. The data are generated by different 8-bit data inputs.

A schematic of the DAC test is presented in Figure 3.29. DAC input bits are produced with PWL sources in order to simulate both the DAC conversion and the ADC input sampling phase. All the input bits are '0' at the beginning, one LSB is counted up at each period, up counting is paused for one period after each 8 periods. After 256 periods of conversion and 32 periods of ADC analog input sampling periods, the full scale output is acquired. DNL and INL tests are applied to this output voltage, excluding the sampled ADC analog input voltage. DAC output is sampled and exported to MATLAB where DNL and INL calculations are performed. DNL and INL plots for the DAC at TT (Typical-Typical) $105°C$ are presented in Figure 3.30 and Figure 3.31 respectively.

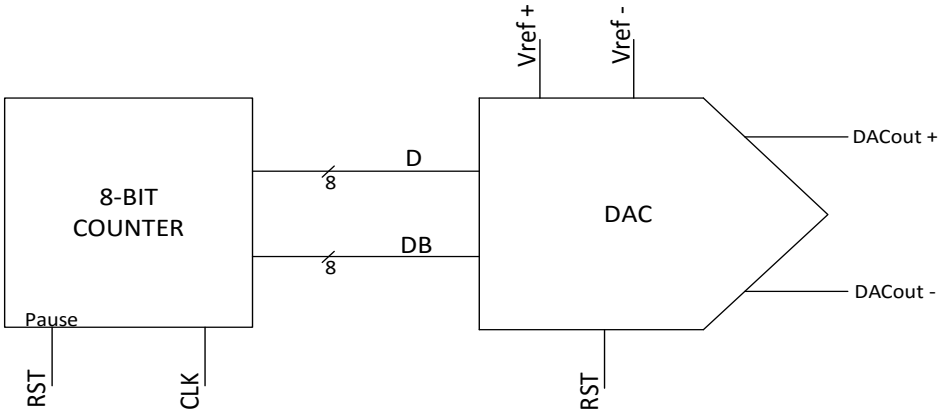

Figure 3.29: DAC Test bench.

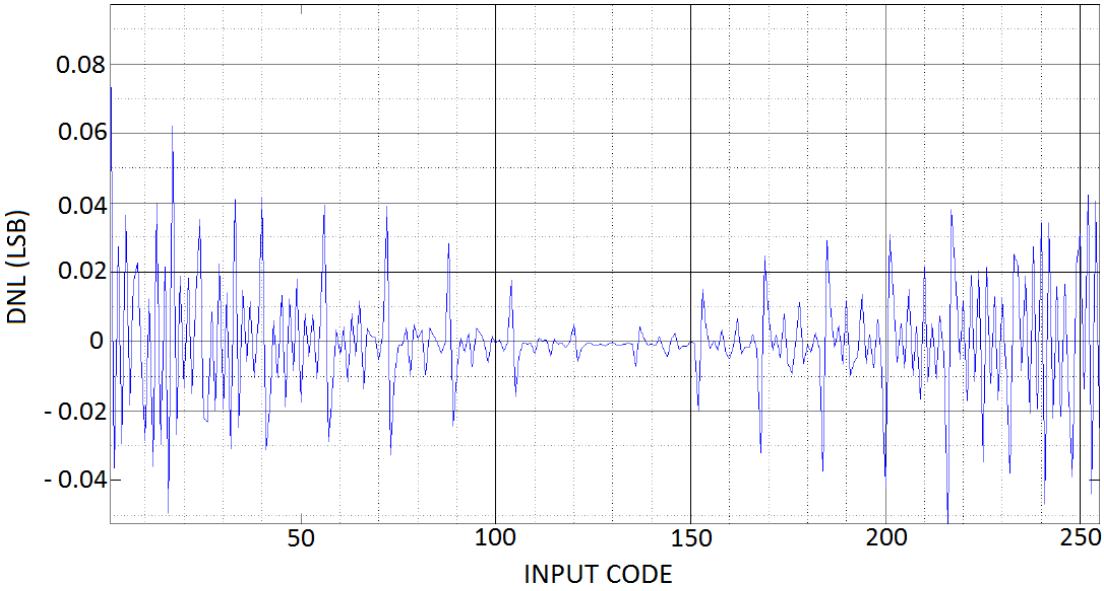

Figure 3.30: DAC DNL plot.

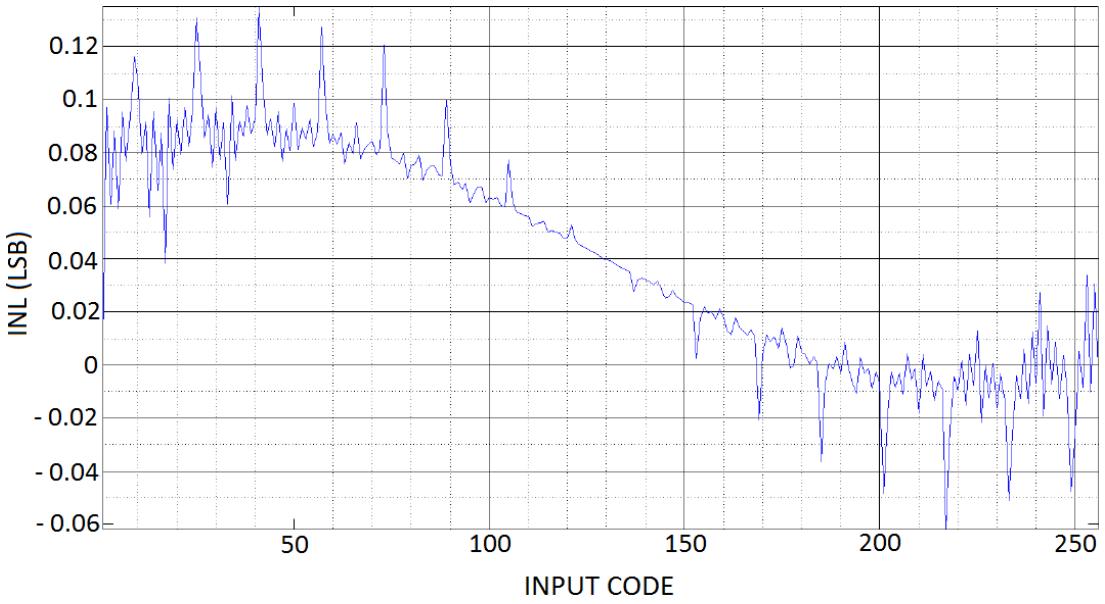

Figure 3.31: DAC INL plot.

In Figure 3.30 and Figure 3.31, the INL and DNL results are calculated by designed circuit in Figure 3.29. These results shows the DNL and INL value of the DAC block. It is obvious that DAC has both DNL and INL properties well below $0.5LSB$, which assures the linear operation and no missing codes respectively.

3.3 The SAR Logic

The SAR logic block collects the data in the 9-bit data array, given from output of the comparator while the block shifts the first shift register. Then the inverted output data set the other 8 D flip-flops to prepare the 8-bit word for the DAC block.

The last task of the SAR logic is determined as a storage, the 8-bit data are stored for one conversion period in the last register array and this data represent the output word for the SAR ADC in one conversion period.

The designed SAR logic block is shown in Figure 3.32. As it explained before, the logic control block of the ADC is based on D flip-flop structure. It consists of a 9-bit shift register to prepare the initial state for the SAR logic, a data array that includes 9 D flip-flops to collect the comparator's results, and a register array that consists 8 D flip-flop to store the 8-bit data as output of the whole system.

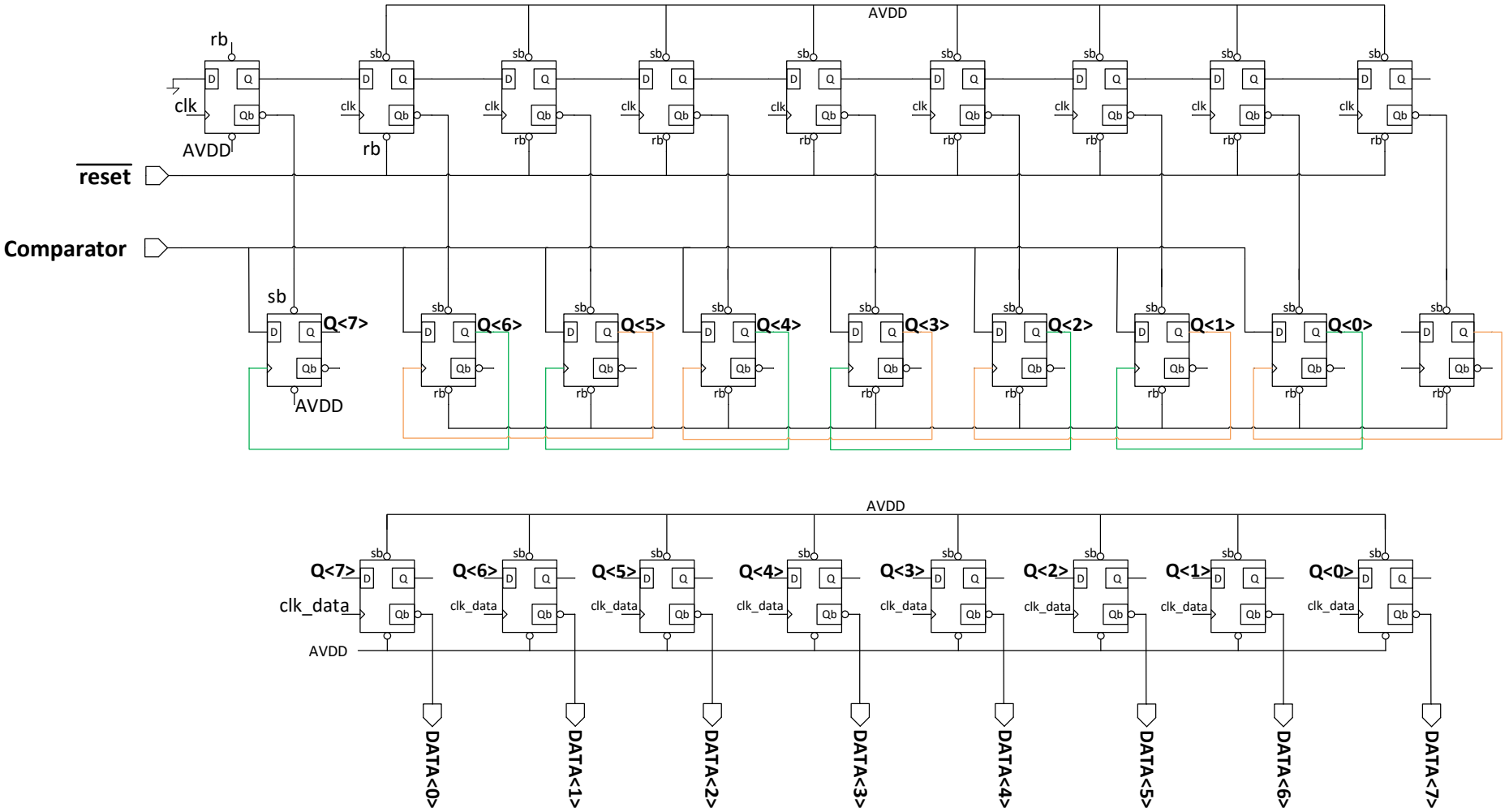

Figure 3.32: SAR structure.

3.3.1 The D flip-flop with set and reset

The designed D Flip Flop (DFF) is based on transmission gated master-slave latch. As showing in Figure 3.33, the master-slave structure is triggered by rising edge of the clock. During the falling edge of the clock, the master latch follows the input and the slave latch holds its previous weight. When the rising edge of the clock comes up, vice versa.

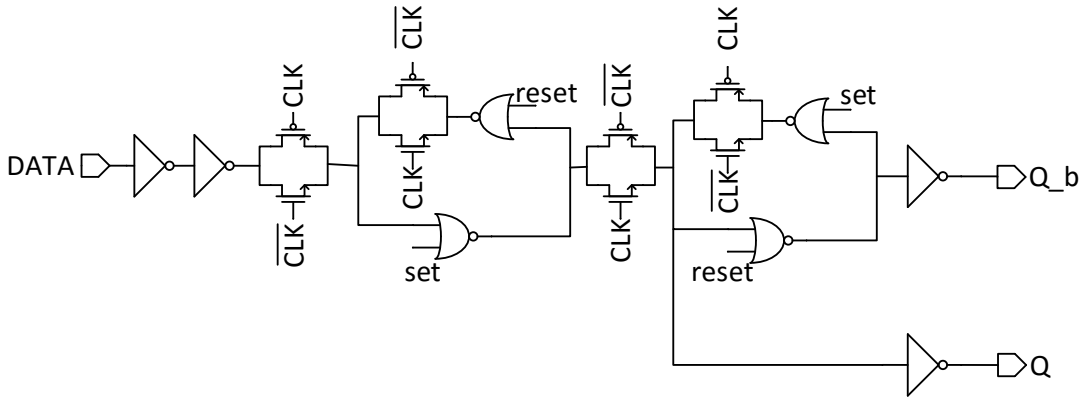

Figure 3.33: D flip flop structure.

Generally, not only the master-slave structure is triggered by rising edge of the clock, but also it requires the inverted clock. With the considering on the set and reset mechanism, the structure shows the high active set or $reset$ signal controls the NOR gates and the output. If the low $\overline{set}$ signal comes up, the logic output will be high. When the $\overline{set}$ signal is high and the $\overline{reset}$ signal is low, the output will be logic low. The signals are indicated in the Table 3.2 that applying logic low for both $\overline{set}$ and $\overline{reset}$ signals, ends up with undefined result for the transmission gated master-slave latch.

Table 3.2: Truth table of D flip flop.

$\overline{set}$	$\overline{reset}$	Q
0	1	1
1	0	0
0	0	Undefined

In Figure 3.33 shows that the successively connected inverters supply sharper signal waveform. The transmission gated switches are controlled by CLK and $\overline{CLK}$ signals. Moreover, the NOR gates are used as inverter stage.

3.3.2 Operation and test

SAR logic operation begins with the low active $\overline{reset}$ (rb) signal. First bit of the 9-bit shift register's output is forced to set high level by the low active $\overline{reset}$ signal. With this, the inverted output of the first bit of the shift register is forced to set low so on, and it is connected to $\overline{set}$ (sb) of the leftmost (8^{th}) DFF of the 9-bit data array. After loading the initial values, data output becomes 1000 0000. Then with the rising edge of the clock, the second period starts. At that time, shift register sets the $\overline{set}$ of 7th data bit of the data array to logic one. With rising the data, the eighth data bit of the data array takes its data from the Comparator. Moreover, the data is conserved by the last DFF of the data array. The conversion continues for seven remaining periods. too. At the end of the all processes, the conserved data are transferred to the register array to store all the data as output of the SAR ADC. Then the low active $\overline{reset}$ signal starts the whole procedure again.

Table 3.3 demonstrates the algorithm how SAR logic works on each clock period. For two conversion period, the table is created. It includes $\overline{reset}$ signal, the comparator, the SAR logic output (that is also an input of the DAC block), and the Data (that is output of the SAR ADC system). Firstly, sampling phase (zeroth period) is begun by delivering active-low reset signal to all SAR logic registers. At this moment, input of the DAC includes the data as $Q < 7{:}0 > =$ 1000 0000. Then the DAC block samples the input voltage by connecting the bottom plates to input voltage and top plate to common mode voltage. At the first period p1, $Q < 7 >$ contains the $COMP\_OUT$ and $Q < 6 >$ rises logic one. Then the second period (p2) comes up and, $Q < 6 >$ contains the $COMP\_OUT$ and $Q < 5 >$ rises to logic one. The other steps continue with the same fashion. During these steps, Q registers contain their compared data inside when the settled rising edges come. Before another reset and sample phase, the Q registers transfer their data to register array (8-bit register $D < 7{:}0 >$). Output $D < 7{:}0 >$ registers of the SAR ADC conserve the new transferred values for 9 cycles. In other words, during the second conversion output $D < 7{:}0 >$ registers of the SAR ADC remain the same and then when another reset and sample phase comes up, the registers take new values. The input registers' data of the DAC are changed systematically. At the end of the each period, the current form of the changed data are transferred to the 8-bit register array to preserve for one conversion.

The ADC's main clock frequency is $166.5MHz$, which corresponds to a period of $6ns$, but its sampling frequency is 9 times higher than this period because of the binary search procedure. So the achieved sampling frequency is $18.5MHz$.

As seen in Figure 3.34, the SAR logic is controlled by Clk, $\overline{reset}$ and $Data\_Clk$ signals. Clk shows the each period of the system and the $Data\_Clk$ controls the output data of the whole system. $\overline{reset}$ signal is for resetting the flip flops. The compared data comes to $Comparator$ input of the SAR logic.

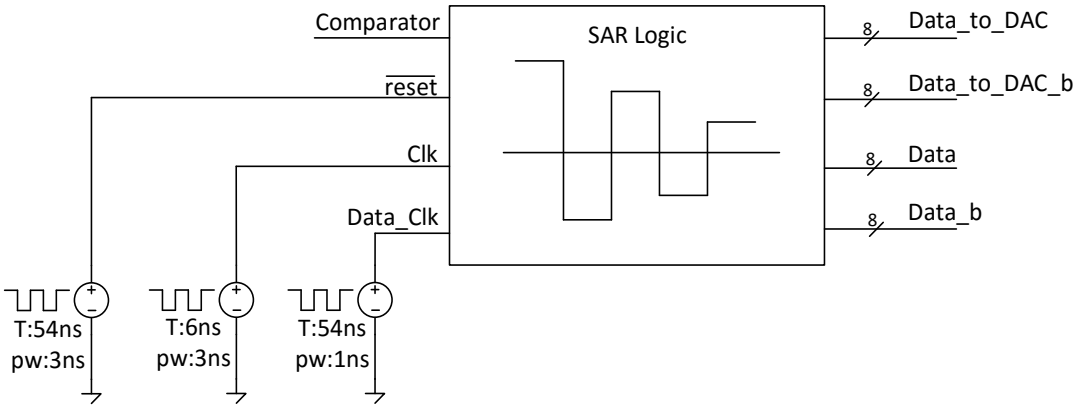

Figure 3.34: SAR logic test bench.

As it can be understood from their names, the control voltage ($V_{ref\pm}$) of the DAC is generated by 8-bit $Data\_to\_DAC$ and 8-bit $Data\_to\_DAC\_b$ outputs of SAR logic. In addition, the $Data$ and $Data\_b$ (8-bit outputs) show the converted data from analog to digital.

Table 3.3: Operation results of SAR logic for 2 conversion.

		First conversion									Second conversion								
period		R&S	p1	p2	p3	p4	p5	p6	p7	p8	R&S	p1	p2	p3	p4	p5	p6	p7	p8
	$\overline{reset}$	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
DAC input	Q<7>	1	C7a	C7a	C7a	C7a	C7a	C7a	C7a	C7a	1	C7b	C7b	C7b	C7b	C7b	C7b	C7b	C7b
	Q<6>	0	1	C6a	C6a	C6a	C6a	C6a	C6a	C6a	0	1	C6b	C6b	C6b	C6b	C6b	C6b	C6b
	Q<5>	0	0	1	C5a	C5a	C5a	C5a	C5a	C5a	0	0	1	C5b	C5b	C5b	C5b	C5b	C5b
	Q<4>	0	0	0	1	C4a	C4a	C4a	C4a	C4a	0	0	0	1	C4b	C4b	C4b	C4b	C4b
	Q<3>	0	0	0	0	1	C3a	C3a	C3a	C3a	0	0	0	0	1	C3b	C3b	C3b	C3b
	Q<2>	0	0	0	0	0	1	C2a	C2a	C2a	0	0	0	0	0	1	C2b	C2b	C2b
	Q<1>	0	0	0	0	0	0	1	C1a	C1a	0	0	0	0	0	0	1	C1b	C1b
	Q<0>	0	0	0	0	0	0	0	1	C0a	0	0	0	0	0	0	0	1	C0b
SAR ADC output	D<7>	0	0	0	0	0	0	0	0	**C7a**	C7a	C7a	C7a	C7a	C7a	C7a	C7a	C7a	**C7b**
	D<6>	0	0	0	0	0	0	0	0	**C6a**	C6a	C6a	C6a	C6a	C6a	C6a	C6a	C6a	**C6b**
	D<5>	0	0	0	0	0	0	0	0	**C5a**	C5a	C5a	C5a	C5a	C5a	C5a	C5a	C5a	**C5b**
	D<4>	0	0	0	0	0	0	0	0	**C4a**	C4a	C4a	C4a	C4a	C4a	C4a	C4a	C4a	**C4b**
	D<3>	0	0	0	0	0	0	0	0	**C3a**	C3a	C3a	C3a	C3a	C3a	C3a	C3a	C3a	**C3b**
	D<2>	0	0	0	0	0	0	0	0	**C2a**	C2a	C2a	C2a	C2a	C2a	C2a	C2a	C2a	**C2b**
	D<1>	0	0	0	0	0	0	0	0	**C1a**	C1a	C1a	C1a	C1a	C1a	C1a	C1a	C1a	**C1b**
	D<0>	0	0	0	0	0	0	0	0	**C0a**	C0a	C0a	C0a	C0a	C0a	C0a	C0a	C0a	**C0b**

4. ADC OPERATION AND SIMULATIONS

ADC in this work is designed as a fully differential 8-bit SAR ADC with the components described in the previous sections, using $0.18\mu m$ CMOS technology. The converter has $\pm 1V$ input voltage range and is supplied by $1.8V$ where input sampling switches are supplied with $3.3V$ voltage source. Each conversion is performed in 9 clock cycles. The minimum change in differential input voltage that ADC is able to sense and convert (Least Significant Bit - LSB) is equal to

$$LSB = \frac{input\ voltage\ range}{2^n} = \frac{1}{2^8} = 3.9\ mV \tag{4.1}$$

A block diagram of the designed SAR ADC is seen in Figure 4.1. As seen in the block diagram, no external sample and hold circuit is used, instead, the DAC capacitors are used as sample and hold capacitors. This way, need for extra circuitry for the sample and hold is avoided, which probably would include a voltage buffer too.

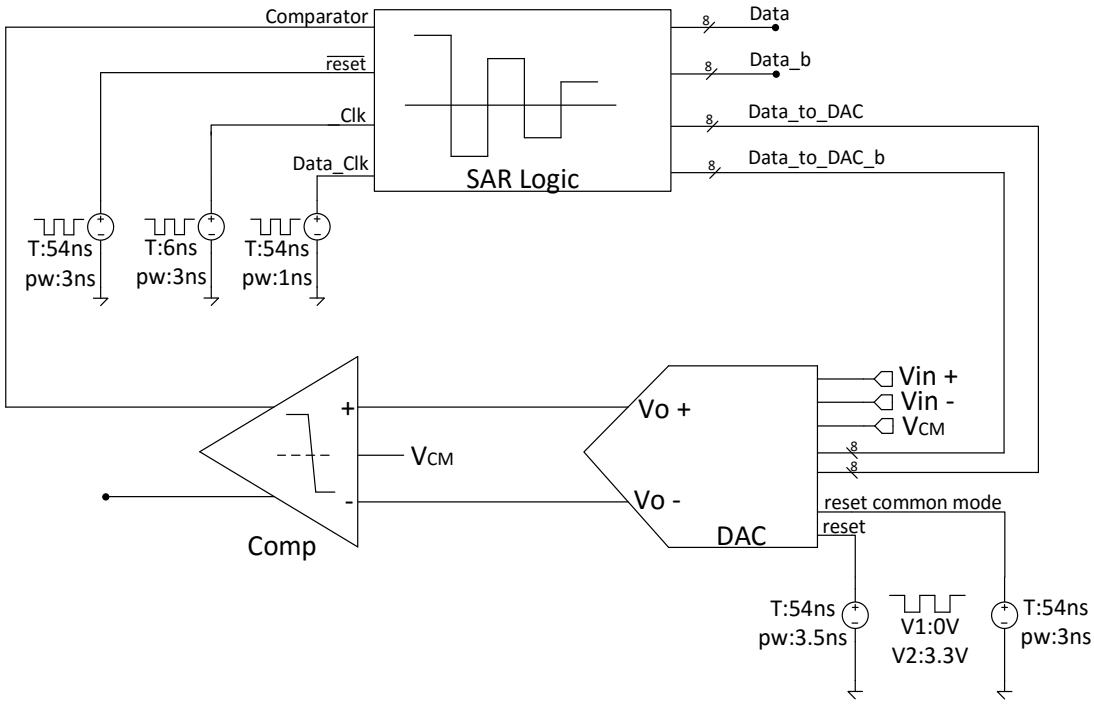

Figure 4.1: SAR ADC test bench.

A figure of ADC clock signals and internal voltages of ADC are shown in Figure 4.2. Considering clocks and internal voltages lead us to understand ADC working principle easily.

The main clock signal (Clk) runs 9 periods per ADC's one conversion, therefore, $9 \times 6ns = 54ns$ conversion period.

Appling the rising edge of the first clock to the input of the ADC starts the whole system operation. Comparator inputs connected to common mode voltage (V_{CM}), bottom plate sampling switch also connected to the common mode voltage and all DAC capacitors are connected to the ADC's input.

First half cycle of the clock period is for the analog input sampling also inside this half cycle period there is comparator offset cancelation operation, which mentioned in comparator section. Bottom plate sampling switch of DAC is turned off at $3ns$ falling edge, sampling switch of DAC disconnects from input voltage at $3.5ns$ and connected to the common mode voltage. Finally, at $4ns$, DAC's output voltage connected to the comparator input and sampling phase is completed.

In the second clock cycle, as mentioned in SAR section, SAR output is actually denotes half of the reference voltage. $4.5ns$ after the rising edge, comparator and DAC outputs settles and Latch get strobes for $1ns$. At $5ns$, latch output clocked into a flip-flop, this clock is named as data clock, it has also $1ns$ period.

Continuing these steps for 8 main clock periods, output data of the first conversion is ready at the output of the SAR logic. At the end of conversion, the signals are synchronized with the next conversion start. The comparator inputs are disconnected and connected to V_{CM}, the bottom plate sampling switches are connected to V_{CM}, and the capacitors of the DAC are connected to input comes from ADC input on the rising edge of first clock (Clk).

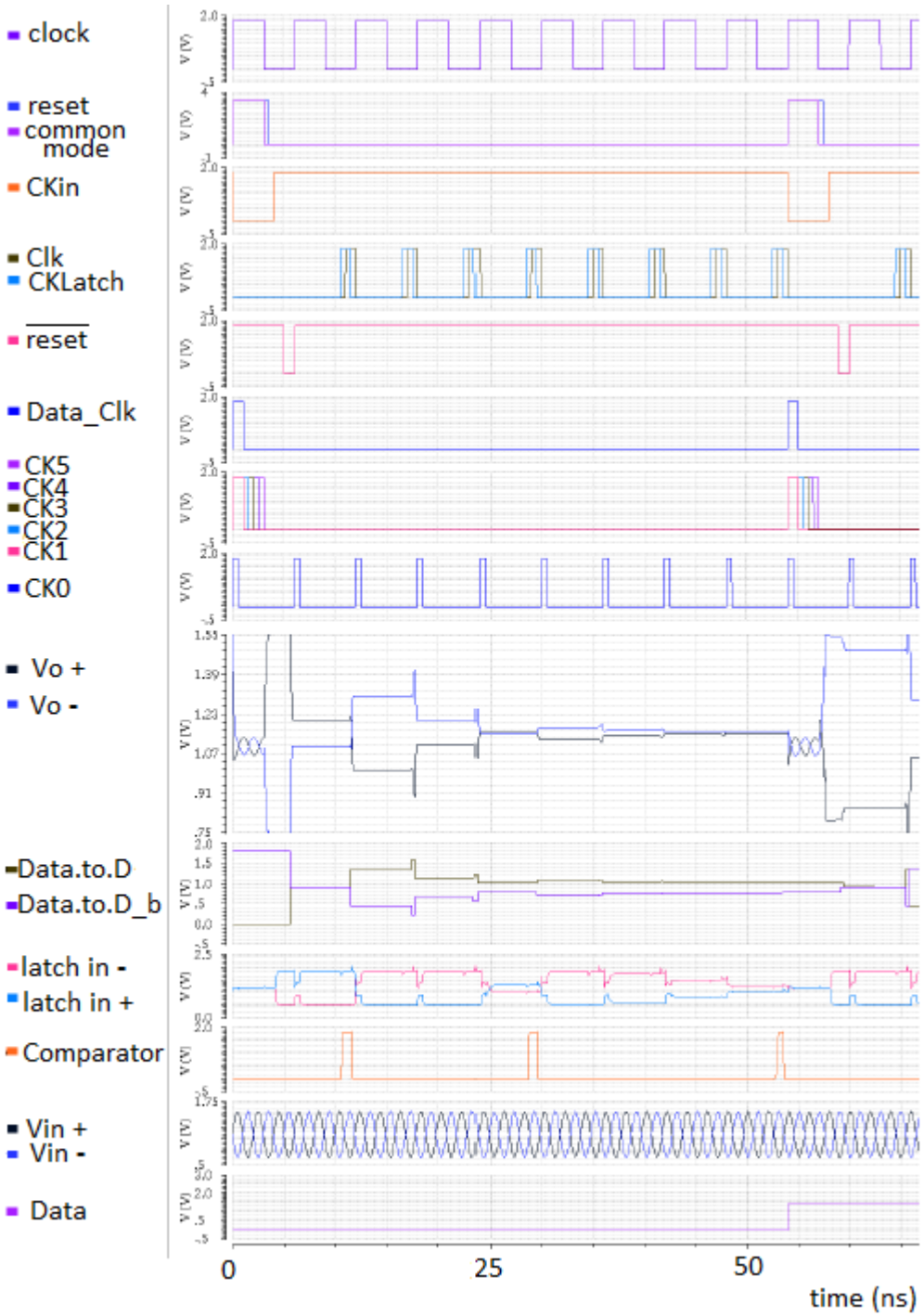

Figure 4.2: SAR ADC clocks and internal voltages.

5. ADC PERFORMANCE EVALUATION

The Figure 5.1 represents the test bench of designed ADC simulation. It is figured with the input signal sources, ADC under test, an ideal DAC following the ADC under test, the ideal sample and hold, and MATLAB to process the data. Ideal DAC converts the digital bits at the output of the ADC into analog voltage levels. This output is sampled periodically at necessary points and it is exported to a .csv file. Further processing like linearity test on the exported data is performed in MATLAB environment.

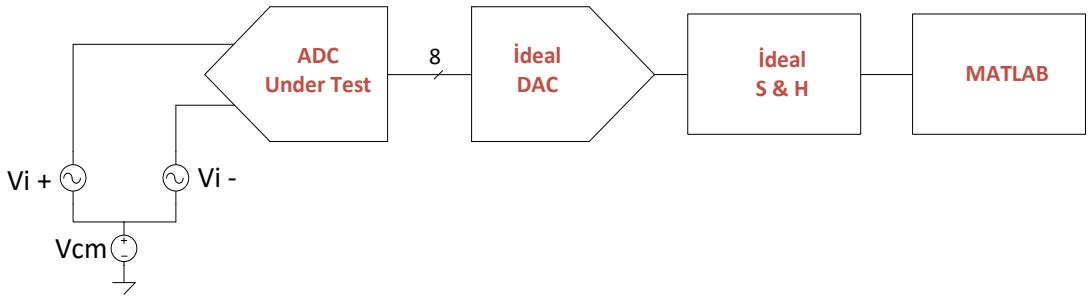

Figure 5.1: SAR ADC test bench for performance evaluation.

5.1 Static Performance

5.1.1 Simulation setup

By using the test bench in Figure 5.1, the static performance of the ADC is evaluated. Input signals are given as 8 times slower linear ramp voltages so that each code at the output should occur 8 times (8 hits per code - HPC) for an ideal ADC. When the negative input voltage decreases, the positive input voltage increases so on. ADC output words are ideally converted to analog ideally, and then it is sampled at the end of each conversion and finally it is exported to a .csv file in order to calculate static performance metrics in MATLAB.

5.1.2 DNL

Firstly, the Differential Non-Linearity (DNL) test is applied. DNL can be defined as the difference between ideal and real value of a code for ADC. When an input voltage corresponds to a given code applied at the input h times and the given code occurred

at the output h_R times the DNL could be calculated by using equation 5.1 for this given code.

$$dnl(i) = \frac{h_R - h}{h} \tag{5.1}$$

Where $dnl(i)$ is the DNL at the ith code, h represents the ideal $hits\ per\ code$ number, h_R represents the obtained number of ith code. Total DNL is usually reported as the absolute maximum value of the dnl array.

The given code in equation 5.1 is implemented in MATLAB and the exported data from CADENCE simulation is used for DNL calculation. Appendix B presents the MATLAB code for DNL calculation. DNL plot of the ADC is given in Figure 5.2.

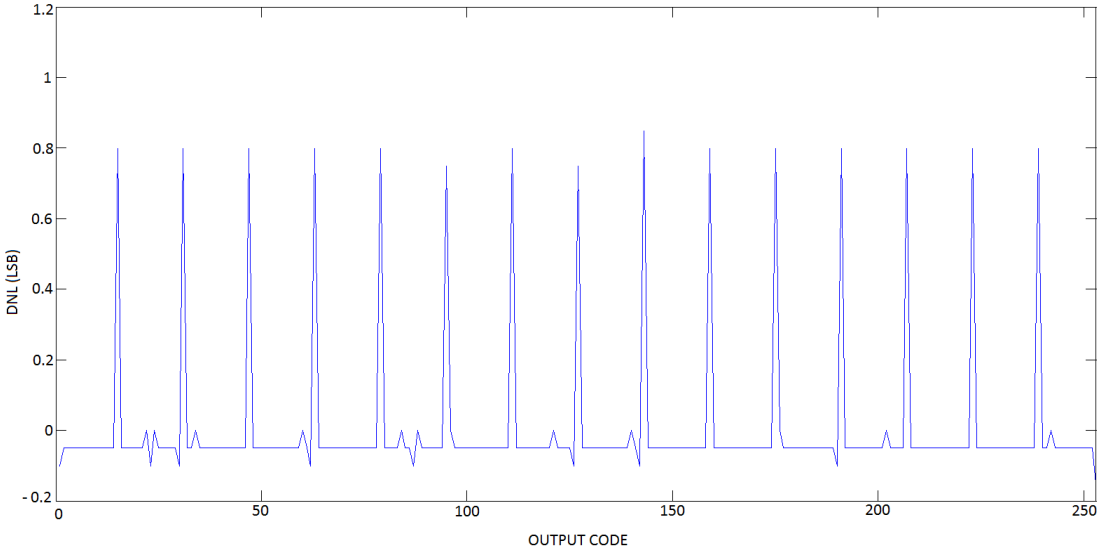

Figure 5.2: SAR ADC DNL plot.

The total DNL error is the difference of the maximum and minimum resulted DNLs of all codes. A DNL error higher than $1LSB$ corresponds to a loss of 1 bit. The lower DNL than $1LSB$ is achieved by the designed ADC.

5.1.3 DNL across PVT corners

DNL analysis is performed across PVT corners, too. Simulation results show that the worst case DNL is just a little over $0.8LSB$. DNL plots for the FF, TT, SS (Fast-Fast, Typical-Typical, Slow-Slow) and total of corner simulations are given in Figure 5.3 respectively.

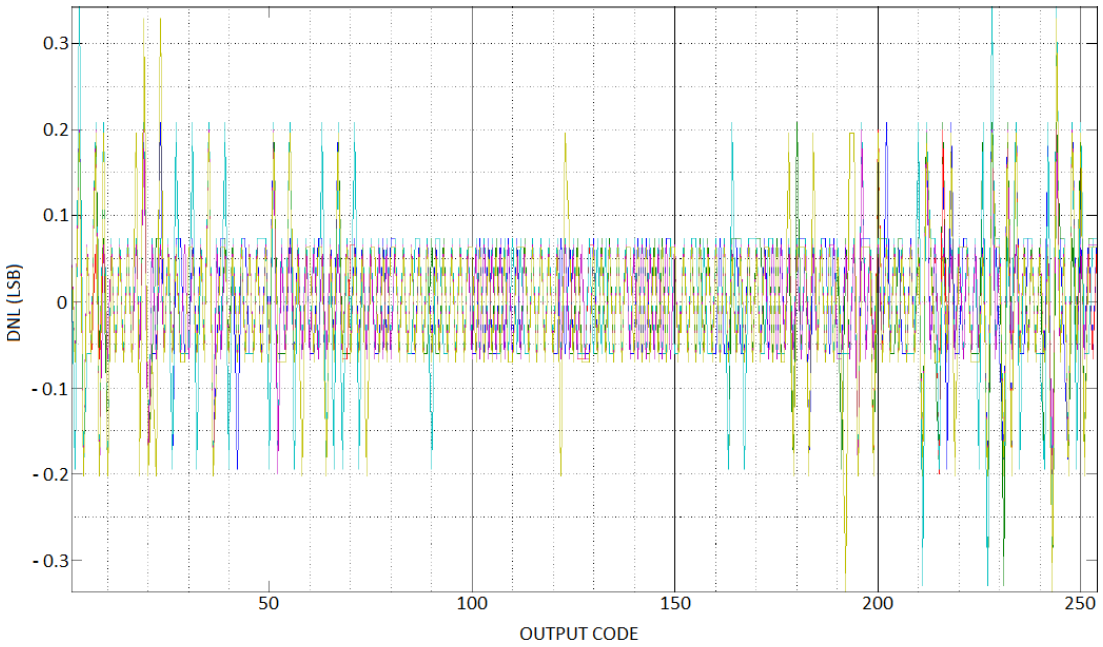

Figure 5.3: SAR ADC DNL plot over PVT corners.

5.1.4 INL

Integral nonlinearity (INL) is the difference of the resulted line and the ideal line for a full scale ramp input. INL is described as cumulative sum of the DNL array for the ADC.

$$inl(i) = \sum_{f=1}^{i} dnl(f) \tag{5.2}$$

where $inl(i)$ is the INL at the ith code, $dnl(f)$ is the DNL for fth code and $1 \leq i \leq 2^n$.

The DNL and INL are measured by applying a full scale sinusoidal input signal and collecting the output histogram.

The given equation 5.2 depends on the DNL results. With the array of dnl are implemented in MATLAB then the exported data from CADENCE simulation is used for INL calculation. In addition, the Appendix B presents the MATLAB code for INL calculation.

Total INL is usually reported as the absolute maximum value of the inl array. INL plot of the ADC is given in Figure 5.4.

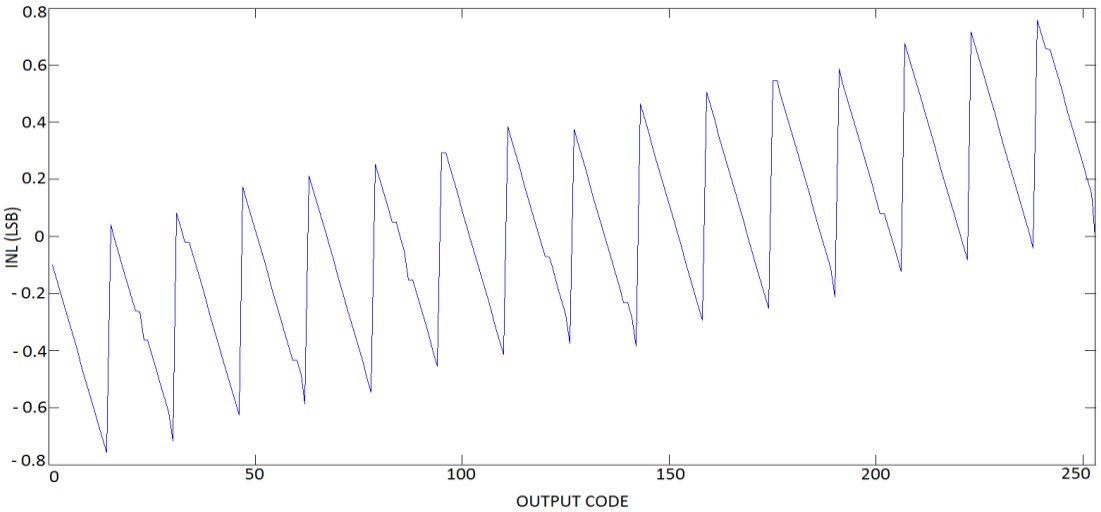

Figure 5.4: SAR ADC INL plot.

5.1.5 INL across PVT corners

INL analysis is performed across PVT corners too. Simulation results show that the worst case INL is just a little over $0.8LSB$ for some rare SS (Slow Slow) corners. INL plots for the FF, TT, SS and total of corner simulations are given in Figure 5.5.

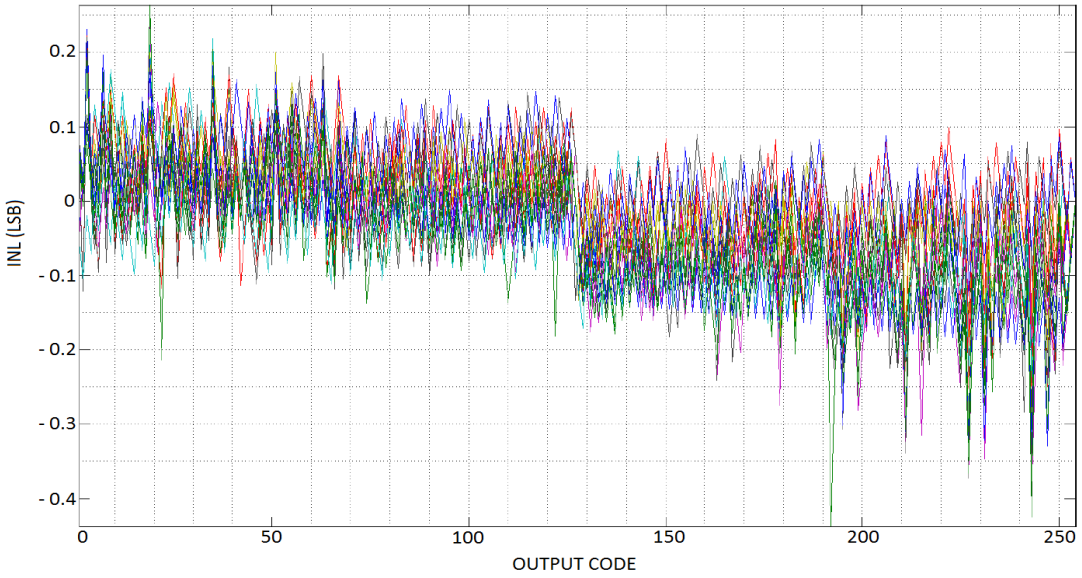

Figure 5.5: SAR ADC INL plot over PVT corners.

5.1.6 Offset error

ADC offset error is measured at mid-code output. A very slow input ramp signal is applied and the output of the ADC is observed. The difference between common mode voltage ($1.1V$) and the input voltage level at which the output code turns mid-code plus one (127 to 128 in this case) is the offset error of the ADC. The 30 run Monte-Carlo simulation is performed. Offset error results are presented in Figure 5.7.

Observing offset error Monte-Carlo analysis results shows that 16 runs give $0V$, 12 runs gives $2mV$, and 2 runs give $4mV$ offset error. Mean offset error can be calculated as $16 \times 0 + 12 \times 2mV + 2 \times 4mV = 533mV$. Variance for the offset error is calculated as 1.53μ, standard deviation is calculated as $1.236 \times 10^{-3}$and 3σ sigma is calculate as $3 \times 1.236 \times 10^{-3} = 3.71mV$

5.2 Dynamic Performance

SFDR, SNR, SINAD, and ENOB create the dynamic performance of an ADC. All the dynamic specifications of the ADC are discussed in this section.

5.2.1 Simulation setup

Input voltages are given as sine waves with frequencies that allow coherent sampling. Dynamic performances are obtained by running transient simulations allowing the ADC to convert 64 samples of the input. Corresponding cadence calculator functions are used in order to find dynamic performance specifications. Also, FFT of the resulting data is plotted to visually observe the SFDR, harmonics and noise level.

5.2.2 SFDR

Spurious free dynamic range (SFDR) is measured for $500MHz$ input signal in all PVT corners for the designed ADC. The SFDR result for the $500MHz$ input shows the undersampling performance of designed ADC. Worst corner SFDR result is seen in Figure 5.6.

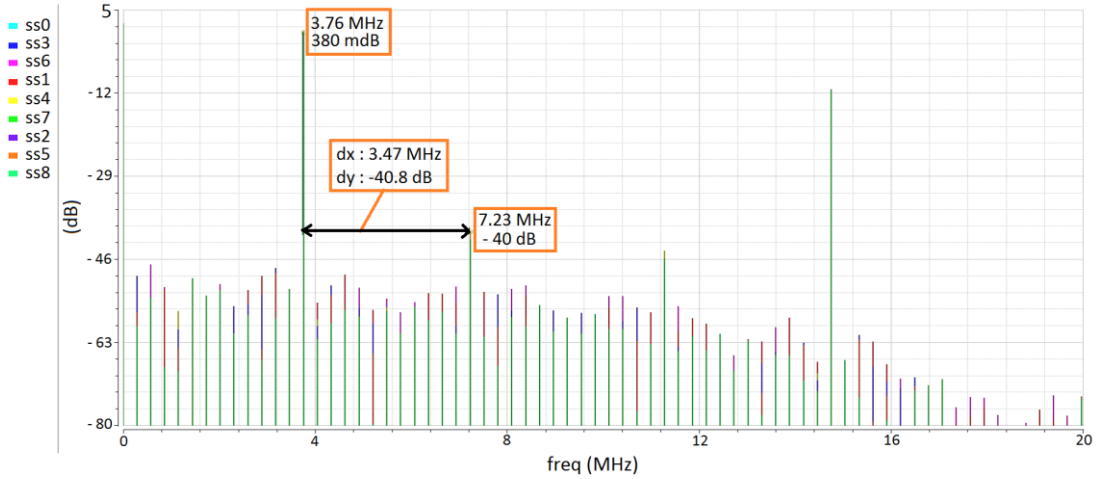

Figure 5.6: SAR ADC SFDR for 500MHz input signal.

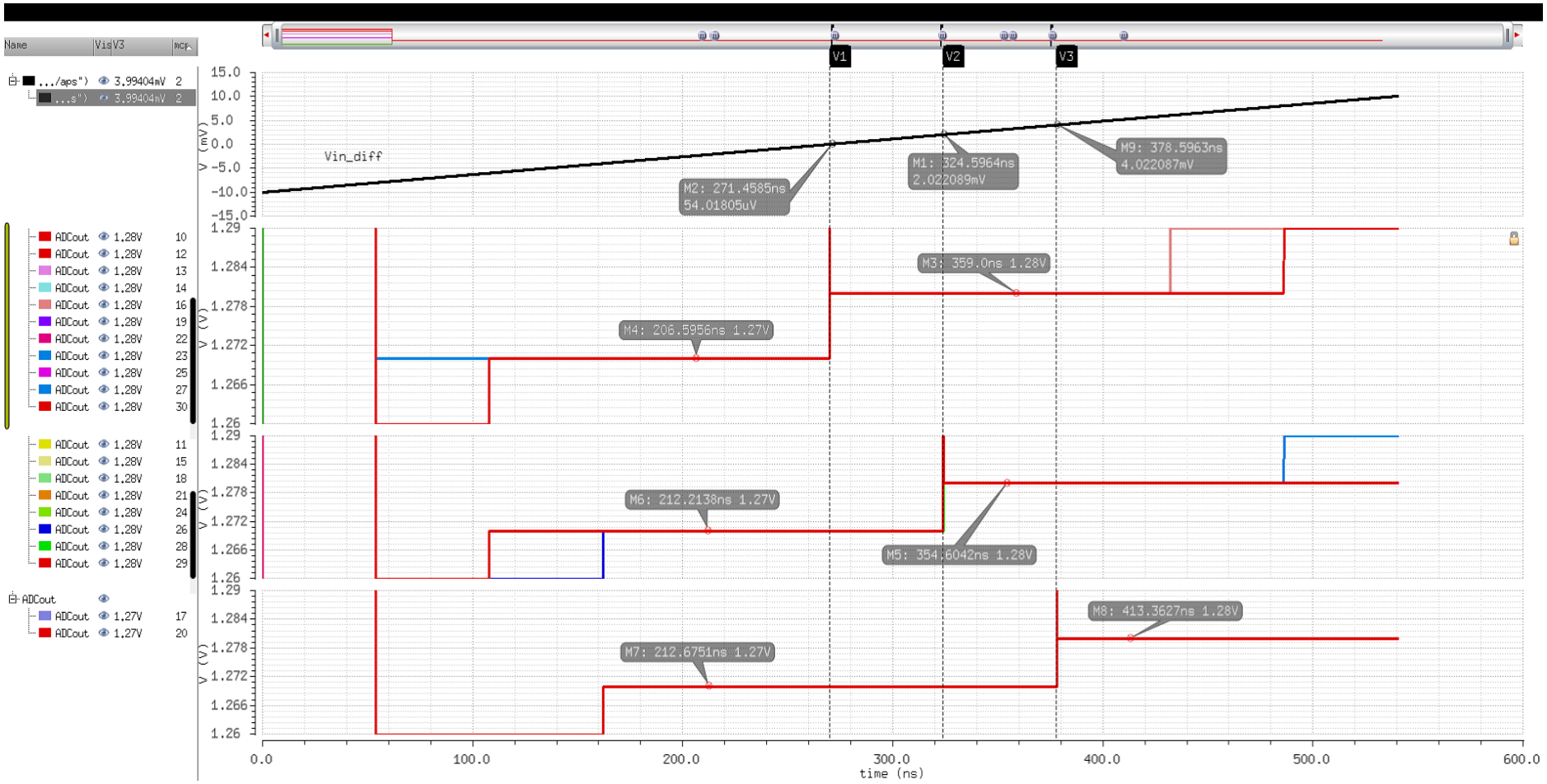

Figure 5.7: SAR ADC offset voltage.

5.2.3 SNR

Signal to noise ratio (SNR) is defined as the ratio of the signal power to the noise power and can be formulated as

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{5.3}$$

where P_{signal} is the signal power and P_{noise} is the noise power.

Signal to noise and distortion (SINAD) ratio is defined as the ratio between the signal power and the noise power plus distortion and can be formulated as

$$SINAD = \frac{P_{signal}}{P_{noise} + P_{distortion}} \tag{5.4}$$

where $P_{distortion}$ is the distortion power.

Effective number of bits (ENOB) has a relation with signal to noise and distortion ratio (SINAD) as in equation 5.5. Effective number of bits is a metric for total dynamic performance. In theory, one bit precision leads to an increase of $6.02dB$ in the SINAD for data converters. It is easy to achieve the non-ideal resolution from the calculated SINAD value by the formula given in

$$SINAD = 6.02\,ENOB + 1.76 \tag{5.5}$$

So it is obvious that one can easily be calculated when the other is known.

A table of SNR, SFDR, SINAD and ENOB versus input signal frequency at nominal corner is given in Table 5.1.

Table 5.1: ADC SNR, SFDR and ENOB results across the input signal at PVT corners.

Base frequency	Prime number	fin (Hz) (fbase*prime)	SNR (dB)	SFDR (dB)	SINAD (dB)	ENOB (bit)
$\frac{1}{54ns \times 64sample}$ $= 289.352KHz$	3	868.056 K	47.88	55.02	46.78	7.48
	11	3.183 M	46.56	56.16	46.52	7.43
	19	5.497 M	48.67	53.46	48.67	7.79
	31	8.97 M	43.5	50.33	43.5	6.93

A table of SNR, SFDR, SINAD, ENOB versus input signal frequency at nominal corner is given in Table 5.1.

A table of SNR, SFDR, SINAD and ENOB across PVT corners for the $500MHz$ input signal is given in Table 5.2.

Table 5.2: ADC SNR, SFDR and ENOB results across the PVT corners.

Process	Supply (V)	Temperature (°C)	SNR (dB)	SFDR (dB)	SINAD (dB)	ENOB (bit)
TT	1.71	-40	47.64	54.56	46.5	7.43
	1.71	27	48	54.11	46.8	7.48
	1.71	85	48.15	54.72	47.29	7.56
	1.71	125	49.94	58.2	48.36	7.74
	1.8	-40	47.86	54.18	46.75	7.47
	1.8	27	48.09	55.02	46.94	7.51
	1.8	85	48.38	55.56	47.38	7.58
	1.8	125	49.15	57.88	47.77	7.64
	1.89	-40	47.78	53.48	46.8	7.48
	1.89	27	48.5	53.81	47.13	7.54
	1.89	85	49.53	56.89	47.98	7.68
	1.89	125	48.38	54.92	47.22	7.55
SS	1.71	-40	47.64	54.56	46.5	7.43
	1.71	27	48	54.11	46.8	7.48
	1.71	85	44.99	53.67	43.48	6.93
	1.71	125	44.68	52.7	43.14	6.87
	1.8	-40	47.86	54.18	46.75	7.47
	1.8	27	48	54.11	46.8	7.48
	1.8	85	48.02	53.36	46.8	7.48
	1.8	125	45	52.99	43.25	6.89
	1.89	-40	47.86	54.18	46.75	7.47
	1.89	27	47.55	53.71	46.53	7.44
	1.89	85	48.02	53.36	46.8	7.48
	1.89	125	48.61	55.49	47.32	7.57
FF	1.71	-40	48.06	54.63	47.07	7.53
	1.71	27	48.3	54.87	47.05	7.52
	1.71	85	48.97	55.35	47.43	7.59
	1.71	125	49.24	56.4	47.77	7.64
	1.8	-40	47.8	53.67	46.81	7.48
	1.8	27	48.69	55.29	47.28	7.56
	1.8	85	48.38	54.92	47.22	7.55
	1.8	125	49.99	57.5	48.28	7.73
	1.89	-40	47.84	53.93	46.72	7.47
	1.89	27	49.1	56.58	47.62	7.62
	1.89	85	48.67	56.14	47.57	7.61
	1.89	125	49.93	55.86	48.92	7.84

Table 5.3: ADC SNR, SFDR and ENOB Monte Carlo simulation results across the input signal at PVT corners.

MC run number	SNR (dB)	SFDR (dB)	SINAD (dB)	ENOB (bit)
1	50.13	46.38	44.59	7.11
2	49.94	58.2	48.36	7.74
3	47.86	54.18	46.75	7.47
4	48.09	55.02	46.94	7.51
5	48.38	55.56	47.38	7.58
6	49.15	57.88	47.77	7.64
7	47.78	53.48	46.8	7.48
8	48.5	53.81	47.13	7.54
9	49.53	56.89	47.98	7.68
10	49.93	55.86	48.92	7.84
11	48.86	54.08	47.75	7.37
12	48.02	53.36	46.8	7.48
13	45	52.99	43.25	7.19
14	47.86	54.18	46.75	7.47
15	47.55	53.71	46.53	7.44
16	48.02	53.36	46.8	7.48
17	48.61	55.49	47.32	7.57
18	48.97	55.35	47.43	7.59
19	49.24	56.4	47.77	7.64
20	48.67	56.14	47.57	7.61

A 20 run of Monte Carlo simulation with 500MHz input signal at TT 105°C corner is performed and results are provided in Table 5.3.

5.3 Undersampling Performance

Achieving a single-ADC for a high speed time interleaved ADC is the main purpose of the thesis. In the high speed design, the input signal will be well beyond the sampling frequency of the sub-ADCs. Because of this, single-ADC designs have to show good harmonic performance under high input frequencies. It is normally expected that the signals that are the exact multiples of the sampling frequency have

to be undersampled around the sampling frequency. This process could be represented as folding of the spectrum in respect to the sampling frequency on every exact multiple of it. However, because of the cumulative folding the harmonics would increase depending on the maximum frequency component.

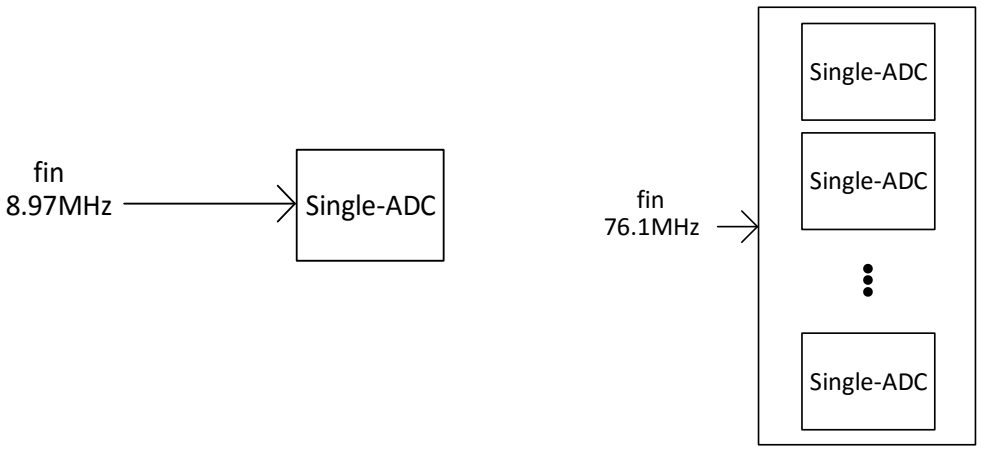

Figure 5.8: Undersampling method.

Figure 5.8 is created under the control of input frequency, which is calculated as in equation 5.6. The Single-ADCs are generated by the undersampling input frequency, which is $f_{in} = 76.1\ MHz$

$$f_{in} = M \times \frac{f_s}{N} \tag{5.6}$$

$$f_{in} = M \times f_{base} = M \times \frac{1/54ns}{2^6} = M \times 289.352KHz$$

$$f_{in} = 8.97MHz$$

where M prime number is equal to 31. Due to the fact that the dynamic performance of the designed SAR ADC for $8.97MHz$ input frequency is already known and the sampling frequency is $18{,}5MSPS$.

$$f_{in} = M \times 289.352KHz = 76.1MHz$$

where M prime number is equal to 263. The results for $8.97MHz$ and $76.1MHz$ frequencies are listed in Table 5.4.

Table 5.4: Undersampling performance.

Frequency	8.97MHz (Nyquist rate)	76.1MHz (Undersampling frequency)	2.001GHz (Undersampling frequency)
SNR (dB)	43.5	48.9	37.2
SFDR (dB)	50.33	56.53	43.78
SINAD (dB)	43.5	48.6	36.65
ENOB (bit)	6.93	7.78	5.8

As it understood from the table, the dynamic values of the ADC does not changes linearly.

5.4 Time Interleaved Performance

When simulating the undersampling performance of the design, time interleaved performance is also tested. To show performance of the time interleaved ADC, 9 single-ADCs run in parallel with all clock signals are shifted properly to achieve $18{,}5MSPS \times 9 = 166.5MSPS$ rate.

On the created Table 5.5, the time interleaved performance results are shown.

Table 5.5: Time interleaved performance.

Frequency	76.1MHz
SNR (dB)	40.78
SFDR (dB)	48.4
SINAD (dB)	40.78
ENOB (bit)	6.48

5.5 Power Consumption Performance

Table 5.6 shows the power consumption for the sub blocks of the designed ADC

Table 5.6: Power consumption performance.

Power of comparator	4.68mW
Power of DAC	4.94mW
Power of SAR logic	1.38mW
Total Power of ADC	11mW

Total power consumption is $11mW$ for the whole ADC as shown in the previous table. With the calculated power consumption, the Table 5.7 is created for comparison the differences between some TI-SAR ADCs.

Table 5.7: Comparison for some TI-SAR ADCs.

	Talekar et al. (2009)	Akita et al. (2011)	Kundu et al. (2014)	Fang et al. (2015)	This Thesis
Technology	180 nm	65 nm	40 nm	28 nm	180 nm
Resolution	4-bit	7-bit	8-bit	10-bit	8-bit
Speed	700 MS/s	1.5 GS/s	2.64 GS/s	5 GS/s	2 GS/p
Power Consumption	23.3 mW	36 mW	39 mW	76 mW	11 mW

In the (Lee, Chandrakasan, & Lee, 2014) $\pm 1LSB$ INL/DNL levels are achieved at $1GSPS$ and SINAD is achieved $39.6dB$ in the (Akita, Furuta, Matsuno, & Itakura, 2011). The (Kundu, et al., 2014) achieves $39mW$ power consumption for 8-bit TI-SAR ADC. Low power structure is designed and the desired target is reached according to results.

5.6 Figure of Merit

For data converters, a figure of merit (FoM) is defined to compare the power performances with different precision and speed. FoM of the designed ADC is calculated in equation 5.7.

$$FoM = \frac{P_{tot}}{2^{ENOB} \times F_S} = 2.3\ pJ/conversion \qquad (5.7)$$

6. CONCLUSION

In this thesis, low power 8-bit $2GS/s$ TI SAR ADC architecture is designed in $180nm$ $1.8V$ CMOS process. This TI-SAR ADC is suitable to be used in portable measurement devices.

The simulation across 36 corners and Monte Carlo analyses indicate that the TI SAR ADC achieves DNL level of $0.3LSB$, INL level of $0.4LSB$, $47dB$ SNR, $55dB$ SFDR, $47dB$ SINAD, 7.55 ENOB at 2 GHz input frequency. It consumes $11mW$ power.

With the created ADC, the desired goal is achieved. The used $180nm$ CMOS technology and the achieved results show the designed low power TI-SAR ADC is compatible for portable measurement devices.

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APPENDIX A - MATLAB CODE FOR DAC INL&DNL CALCULATION

```
dacoutfile = 'dacinldata.csv';
 A = csvread(dacoutfile);
dacout=[];
for i=1:15:size(A,1)
for j=i:i+7
dacout=[dacout;A(j,2)];
end
end
n=8;
bincountup=dec2bin(0:2^n-1)-'0';
%%--------------------IDEAL ...
DAC-----------------------------------------------
for i=1:n
index(i,1)=2^(n-i);
end
deccountup=bincountup*index; %calculate adc decimal output
lsb=(((dacout(end)-(dacout(1))))/((size(dacout,1)-1)));
idealout=(deccountup*lsb)+dacout(1);
difference=idealout-dacout;
inl=difference/lsb;
dnl=diff(inl);
```

APPENDIX B - MATLAB CODE FOR ADC INL&DNL CALCULATION

```
clc
clear all

adcoutfile = './adcinldata.csv';

adcout = csvread(adcoutfile,1,1); %read sim results from file
adcout=adcout/3.90625e-3;
dnl = hist(adcout,min(adcout):max(adcout)) /
(numel(adcout)/(max(adcout)-min(adcout)+1)) - 1;

inl=cumsum(dnl); %calculate INL

figure(1);
plot(dnl,'DisplayName','dnl','YDataSource','dnl');figure(gcf);


figure(2);
plot(inl,'DisplayName','inl','YDataSource','inl');figure(gcf);
```

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