ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

SINGLE-INDUCTOR DUAL-OUTPUT DC-DC CONVERTER WITH MULTIPLE FLYING CAPACITORS

M.Sc. THESIS

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Department of Electronics and Communication Engineering

Electronics Engineering Programme

JUNE 2023

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ LİSANSÜSTÜ EĞİTİM ENSTİTÜSÜ

ÇOKLU UÇAN KAPASİTÖR KULLANAN TEK-İNDÜKTÖR ÇİFT-ÇIKIŞ DC-DC DÖNÜŞTÜRÜCÜ

YÜKSEK LİSANS TEZİ

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Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

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HAZİRAN 2023

Hale YILMAZ, a M.Sc. student of ITU Graduate School student ID 504201219 successfully defended the thesis entitled "SINGLE-INDUCTOR DUAL-OUTPUT DC-DC CONVERTER WITH MULTIPLE FLYING CAPACITORS", which she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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Date of Submission : **22 May 2023**
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to Hailey,

FOREWORD

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June 2023

Hale YILMAZ
Analog Design Engineer

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ABBREVIATIONS

AC	**:** Alternating Current
AMOLED	**:** Active-Matrix Organic Light-Emitting Diode
CCM	**:** Continuous Conduction Mode
CMOS	**:** Complementary Metal Oxide Semiconductor
DC	**:** Direct Current
DCM	**:** Discontinuous Conduction Mode
DCR	**:** DC Resistance
EMI	**:** Electromagnetic Interference
ESR	**:** Equivalent Series Resistance
FET	**:** Field Effect Transistor
LDO	**:** Low Drop-out
MCU	**:** Microcontroller Unit
MOSFET	**:** Metal Oxide Semiconductor Field Effect Transistor
NFC	**:** No Flying Capacitor Topology
NMOS	**:** N Channel Metal Oxide Semiconductor
OTA	**:** Operational Transconductance Amplifier
PCB	**:** Printed Circuit Board
PMIC	**:** Power Management Integrated Circuit
PMOLED	**:** Passive Matrix Organic Light Emitting Diode
PMOS	**:** P Channel Metal Oxide Semiconductor
PWM	**:** Pulse Width Modulation
SIDO	**:** Single-Inductor Dual-Output
SIMO	**:** Single-Inductor Multiple-Output
SoC	**:** System on Chip
SR FF	**:** Set-Reset Flip Flop
1FC	**:** 1 Flying Capacitor Topology
2FC	**:** 2 Flying Capacitors Topology

SYMBOLS

$\mathbf{B}$	: Magnetic Flux Density
$\mathbf{C_{F1}}$	: First Flying Capacitor
$\mathbf{C_{F2}}$	: Second Flying Capacitor
$\mathbf{C_{gn}}$	: Gate Capacitance of NMOS
$\mathbf{C_{gp}}$	: Gate Capacitance of PMOS
$\mathbf{C_{ox}}$	: Oxide Thickness of the MOSFET
$\mathbf{D}$	: Duty Cycle
$\mathbf{F_{CLK}}$	: System Clock
$\mathbf{F_{sw}}$	: Switching Frequency
$\mathbf{g_N}$	: Gate Control Signal of Switches
$\mathbf{I_{in}}$	: Input Current
$\mathbf{I_{L(avg)}}$	: Average Inductor Current
$\mathbf{I_{lim}}$	: Inductor Current Sense Signal
$\mathbf{I_{out}}$	: Output Current
$\mathbf{I_{pk}}$	: Peak Inductor Current
$\mathbf{I_{ripple}}$	: Inductor Current Ripple
$\mathbf{I_Q}$	: Quiescent Current
$\mathbf{R_{ESR}}$	: Equivalent Series Resistance of Capacitor
$\mathbf{R_{DCR}}$	: Direct Current Resistance of Inductor
$\mathbf{R_{ON}}$	: On Resistance of Switches
$\mathbf{t_{NOL}}$	: Non-overlapping Time
$\mathbf{t_{OFF}}$	: Off Time of the Switch
$\mathbf{t_{ON}}$	: On Time of the Switch
$\mathbf{t_S}$	: Switching Period
$\mathbf{V_{DIO}}$	: Diode Forward Voltage
$\mathbf{V_{DO}}$	: Drop out Voltage
$\mathbf{V_{err}}$	: Error Voltage
$\mathbf{V_{IN}}$	: Input Voltage
$\mathbf{V_L}$	: Inductor Voltage
$\mathbf{V_{OUT}}$	: Output Voltage
$\mathbf{V_{NEG}}$	: Negative Output Voltage
$\mathbf{V_{POS}}$	: Positive Output Voltage
η	: Efficiency

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SINGLE-INDUCTOR DUAL-OUTPUT DC-DC CONVERTER WITH MULTIPLE FLYING CAPACITORS

SUMMARY

Over the past years, there has been extensive research in the literature to develop more robust converter designs in terms of area and efficiency. Owing to their high efficiency operation, DC-DC converters have been an essential role in power management integrated circuits (PMICs). In the application of portable devices, the power management system supplies voltage to the different circuits therefore, the power management system requires the need to provide different output voltage levels with high efficiency. One of the most important specifications of DC-DC converters is efficiency, which is the measure of how much power is dissipated by the converter, without being delivered to the output. In the context of mass production, the cost of the components plays a massive role, considering inductors and capacitors. They should not occupy large areas in the system in order not to increase development and production costs. In the literature and in the market, converters using single power inductors to generate dual outputs have been presented. They are so-called Single-Inductor Dual-Output(SIDO) DC-DC converters. SIDO converter is able to support double output based on the application, having only one inductor which significantly relaxes the board area constraints and development costs. Therefore, SIDO converters have been seen in the market as cost-effective, taking the attention of most manufacturers with various applications in portable devices.

The thesis focuses on improving SIDO DC-DC converter efficiency and relaxing coil constraints. This thesis presents a novel Single-Inductor Dual-Output (SIDO) DC-DC converter topology with two flying capacitors. The two flying capacitors are located in the same current path, targeting an enhanced voltage drop reduction on the inductor, and a decrease in the inductor current slope, aiming for improved power efficiency and relaxed coil current constraints. For the completeness of the work and to show improvements compared to previous designs that are present in the literature, conventional SIDO topology, the SIDO topology with one flying capacitor, and the proposed SIDO converter with two flying capacitors have been simulated. The efficiency results include all possible loss contributors, as well as core loss caused by the inductor. The core loss estimation method is also used in this work to model magnetic losses that are contributed by the inductor. The method estimates the B-H loop with a proper model of the inductor according to the core parameters of the coil. The core loss estimation method also considers the difference between the operation mode of the converter and gives more accurate core loss data.

Using specifications addressing battery-powered display driver applications, for the negative output regulation, simulation results show up to 8.3% efficiency improvement compared to the conventional SIDO converter and up to 4.9% efficiency improvement compared to the SIDO converter with one flying capacitor topology. For the positive

output regulation, simulation results show up to 8.8% efficiency improvement compared to the conventional SIDO converter and up to 3.6% efficiency improvement compared to the SIDO converter with one flying capacitor topology. In addition, a reduction in inductor peak current and ripple can be achieved, along with a lower duty cycle operation, which all lead to relaxed coil selection criteria and relaxed converter stability constraints. Owing to reduced voltage drop over the inductor, the core loss has been improved. Having two flying capacitors in the same current path helps decrease voltage stress on the switches and makes it available for the utilization of more resilient devices.

ÇOKLU UÇAN KAPASİTÖR KULLANAN TEK-İNDÜKTÖR ÇİFT-ÇIKIŞ DC-DC DÖNÜŞTÜRÜCÜ

ÖZET

Geçtiğimiz yıllarda, silikon alanı ve verimlilik açısından daha efektif DC-DC anahtarlamalı dönüştürücü tasarımları yapabilmek için literatürde çeşitli araştırmalar sunulmuştur. Düşük güç kaybı ile çalışmaları sebebiyle, anahtarlamalı dönüştürücüler yüksek verim ihtiyacı içeren sistemlerde vazgeçilmez bir yer almıştır. Bu uygulamaların başında güç yönetimli entegre devreleri gelmektedir. Teknolojinin gelişmesi ile daha az yer kaplayan ve daha uzun kullanıcı süresine sahip taşınabilir elektronik ürünler ilgi görmeye başlamıştır. Bu sebeple, telefon, tablet ve akıllı saat gibi taşınabilir kullanıcı elektronik ürünlerin geliştirilmesi için endüstride düşük güç tüketimli ve az silikon alanı kaplayan entegre devreleri sunulmuştur. Teknolojinin gelişmesi ve ihtiyaçların değişmesi ile beraber düşük güç tüketimli entegre devrelerinin araştırılmasına ve çeşitli iyileştirmelerin sunulmasına devam edilecektir.

Taşınabilir elektronik ürünlerde, düşük güç tüketim entegre devresi bulunduğu sisteme farklı gerilim değerlerinde çıkış sağlar. Aynı zamanda, düşük güç tüketimli entegre devre bu devrelere yüksek verimde çıkış gerilimi sağlamaya devam etmelidir. DC-DC anahtarlamalı dönüştürücü devrelerde en önemli tasarım spesifikasyonlarından birisi de verimliliktir. Verimlilik, çıkışa aktarılan gücün, girişe uygulanan güce oranı ile hesaplanır. En yüksek güç verimliliği, sistemde harcanan güç tüketiminin olabildiğince azaltılıp girişe uygulanan gücün çıkışa aktarılması ile elde edilir. Anahtarlamalı dönüştürücülerde bir diğer önemli nokta sistemde kullanılan pasif ve aktif devre elemanlarının kapladığı alandır. Seri üretim düşünüldüğünde, özellikle çok fazla yer kaplayan güç indüktörü ve kapasitörler üretim ve geliştirme maliyetini arttırırlar. Dolayısıyla, tasarımda dikkat edilmesi gereken en önemli unsurlardan biri de olabildiğince az alan kaplayarak yüksek verimli dönüştürücü spesifikasyonları belirlemektir.

Buna bağlı olarak, hem literatürde, hem de endüstride, tek indüktör kullanan çift çıkışlı DC-DC anahtarlamalı dönüştürücüler sunulmuştur. Tek indüktör içeren bu sistem, ihtiyaca bağlı olarak, çift çıkış gerilimi veya çoklu çıkış gerilimi sağlayabilir. Çoklu çıkış gerilimi üretmek için sadece bir tane güç indüktörünün bulunması, sistemde kullanılan alanın azalmasını sağlayarak üretim ve geliştirme maliyetinin de azalmasına olanak sağlar. Tek indüktor çift çıkış DC-DC anahtarlamalı dönüştürücüler, literatürde var olan aynı amaçla kullanılabilecek devrelere kıyasla uygun maliyetli olmasından ötürü üreticilerin dikkatini çekmekte ve çeşitli taşınabilir elektronik ürünlerde kullanılmaktadır. Literatürdeki en temel tek indüktör çift çıkış DC-DC anahtarlamalı dönüştürücü buck-boost anahtarlama sekansında çalışan bir topolojidir. Fakat özellikle negatif çıkış geriliminin üretilmesinde bu topoloji bazı tasarım problemlerine sahiptir. Güç indüktörünün çıkış gerilimine yaklaşık bir gerilim görmesinden ötürü

üzerindeki gerilim stresi fazladır. Buna bağlı olarak, indüktör dalga akımı fazladır ve bu verimlilikte negatif bir etki oluşturur. Bunun yanında indüktör dalga akımının fazla olmasından ötürü indüktörden kaynaklanan manyetik kayıplar fazladır. Devrede bulunan negatif çıkış gerilimi anahtarı, çıkış gerilimi kadar V_{DS} gerilimi görür ve daha negatif çıkış gerilimlerinde bu anahtarın üzerinde çok fazla gerilim stresi oluşturarak bu anahtarın işlevsiz kalmasına neden olabilir. Bütün bu noktalara geliştirme olması amacıyla hibrit devreler önerilmiş ve devreye uçan kapasitör eklenmiş tasarımlar literatürde yer almıştır.

Bu tez çalışması, devreye uçan kapasitörün eklenmesiyle oluşan iyileştirmelerin daha da vurgulanması amacı ile devreye ikinci uçan kapasitörü ekler ve hibrit topolojinin avantajlarını optimize eder. Bu tez çalışmasında bir güç induktorü içeren çift çıkışlı DC-DC anahtarlamalı dönüştürücünün veriminin iyileştirilmesi üzerine yeni bir topoloji önerilmiş ve literatürde yer alan DC-DC anahtarlamalı dönüştürücü topolojileri ile beraber simüle edilerek performans iyileştirilmeleri vurgulanmıştır. Sonuçlar bölümünde hem pozitif çıkış gerilimi hem de negatif çıkış gerilimi üretimi sonuçları, farklı çıkış yükü değerlerinde ve farklı giriş gerilimi değerlerinde sunulmuştur. Tasarımlar makro model olarak gerçeklenmiş, benzetimde devreyi ideallikten uzaklaştıracak etkenler (anahtarların ve pasif elemanların iç dirençleri gibi) eklenerek ve tüm güç kayıp unsurları hesaplanarak çalışmada bütünlük sağlanması amaçlanmıştır.

Bu tez çalışması, akım yoluna iki tane uçan kapasitör ekleyerek hem negatif çıkış gerilimi hem pozitif çıkış gerilimi üretilmesinde avantaj sağlar. Her bir uçan kapasitör, yaklaşık olarak giriş gerilimine kadar şarj edilerek hem güç indüktörünün hem de anahtarlama elemanlarının üzerindeki gerilim stresini azaltır. Anahtarlama elemanlarının üzerindeki gerilim stresinin azalması, tasarım aşamasındaki kısıtlamaları azaltıp anahtarların boyut tasarımı konusunda esneklik sağlar. İndüktör üzerindeki gerilimin azalması, indüktör dalga akımının azalmasını da beraberinde getirerek dönüştürücü veriminde iyileştirme sağlar. İndüktör dalga akımının azalmasına bağlı olarak, indüktörün manyetik kayıplarında azalma gözlenir.

Dönüştürücü veriminin gerçeğe yakın elde edilmesi ve çalışma bütünlüğünün sağlanması amacıyla indüktör manyetik kayıpları bir indüktör modeli yardımıyla hesaplanmıştır. Bu model indüktör B-H döngüsünü, indüktör akımı üzerinden elde eder. Literatürde kullanılan bu model, indüktör çekirdek parametreleri ile döngüden elde edilen manyetik akıyı matematiksel bir denkleme yazarak nümerik bir çekirdek güç kaybı hesaplar. Benzetim sonuçları, devreye uçan kapasitör ekleyerek çekirdek güç kayıplarının azaldığını ve verimliliğe olumlu etki yaptığını göstermektedir.

Kararlı bir operasyon sağlanarak regüle edilmiş çıkış geriliminin elde edilmesi amacıyla indüktör tepe akım kontrollü devre gerçeklenmiştir. Devredeki anahtarlama sekansına bağlı olarak, tepe akımına ulaşan indüktör akımı algılanarak indüktör akımının daha fazla artmaması ve indüktörün deşarj olması sağlanır. İndüktör tepe akımının ulaşabileceği nokta, referans gerilimi ve çıkış gerilimin farkından elde edilen hata gerilimi ile belirlenir. Sistem anahtarlama frekansına bağlı olarak bir sonraki faz başlayarak indüktör akımı artmaya başlar. Devrede hem çıkış gerilimi hem indüktör akımı kontrol edilerek kararlı bir operasyon sağlanır. Simülasyon sonuçları, taşınabilir elektronik ürün spesifikasyonlarını hedef alan geniş input gerilimi menzilinde(giriş gerilimi 2.5V ve 4.9V arasında iken) dönüştürücünün kararlı operasyon ile regüle edilmiş bir çıkış gerilimi sağladığını göstermektedir.

Buck-boost anahtarlama sekansında çalışan devrelerde, çıkışa akım ikinci faz olan indüktör deşarj fazında aktarılır. Dolayısıyla, çıkışa olabildiğince fazla akım aktarmak için bu fazın uzun tutulması istenir. Anahtarın iletimde olma zamanının toplam sistem periyoduna oranının ifadesi olan görev döngüsünün azalması bu isteğe cevap vermektedir. Devreye eklenen uçan kapasitör, indüktör üzerindeki gerilim düşümünün azalmasına bağlı olarak , indüktör akım deşarj eğiminin azalmasına ve deşarj olma süresinin artmasına olanak sağlar. Böylelikle, görev döngüsü azalır ve çıkışa akım sağlanan süre artmış olur. Simülasyon sonuçları devreye uçan kapasitör ekledikçe görev döngüsünün azaldığını göstermektedir. Görev döngüsünün azalması, çıkışa akım sağlanan sürenin artmasının yanı sıra, sistemin kararlı olabilmesi noktasında tasarım kolaylığı sağlar.

Bu çalışmanın bir diğer avantajı, bobin seçim kriterlerinde de esneklik sağlamaktır. Bahsedildiği gibi, devreye uçan kapasitörler eklenerek her bir kapasitörün giriş gerilimine kadar şarj edilmesi amaçlanır. Bu sayede indüktör daha az gerilim stresine maruz kalır. Böylelikle, indüktör tepe akımı, indüktör dalga akımı azalır. İndüktör tepe akımının azalması bobin seçiminde esneklik sağlar ve oluşabilecek indüktör saturasyonunu engelleyerek, sistemin doğru bir şekilde çalışmasını sağlar. Simülasyon sonuçları, devreye uçan kapasitör ekledikçe indüktör tepe akımı ve indüktör dalga akımı azaldığını göstermektedir.

Bir anahtarlamalı dönüştürücünün en önemli spesifikasyonlarından biri olan verimlilik, her bir anahtarın iletim kaybı, indüktör ve kapasitörlerin iç direnç iletim kayıpları, indüktör manyetik kaybı , gövde diyotları iletim kaybı ve kapı kapasiteleri kayıplarının modellenmesiyle hesaplanmıştır. Simülasyon sonuçları, negatif çıkış gerilimi için aynı giriş gerilimi ve aynı çıkış yükü değerinde, devreye uçan kapasitör ekledikçe verimliliğin arttığını göstermektedir. Önerilen topoloji için tepe verimlilik, çıkış yükü 0.5A ve giriş gerilimi 3.8V iken gözlenmiştir. Giriş gerilimi 2.5V ve çıkış yükü 1A olduğu durumda, negatif çıkış gerilim üretimi için, önerilen topoloji konvensiyonel topolojiye göre %8.7, tek uçan kapasitör içeren topolojiye göre %4.9 oranında verimlilik iyileştirmesi göstermiştir. Giriş gerilimi 3.8V ve çıkış yükü 1A olduğu durumda, negatif çıkış gerilim üretimi için, önerilen topoloji konvensiyonel topolojiye göre %4.7, tek uçan kapasitör içeren topolojiye göre %1.8 oranında verimlilik iyileştirmesi göstermiştir. Giriş geriliminin 4.9V ve çıkış yükünün 1A olduğu koşulda, önerilen topoloji için verimlilik sonuçları ile tek uçan kapasitör içeren topolojinin sonuçları benzer olsa da, önerilen topoloji iyileştirilmiş bobin seçme kriterleri ve azaltılmış görev döngüsü avantajlarını hala içermektedir. Uçan kapasitörler sayesinde anahtarlar ve indüktör üzerindeki gerilim stresi azalmış ve daha dayanıklı anahtarlama elemanı seçme olanağı sağlanmıştır.

Pozitif çıkış gerilim üretimi için, önerilen topoloji için tepe verimlilik çıkış yükü 0.5A ve giriş gerilimi 3.8V iken gözlenmiştir. Giriş gerilimi 2.5V ve çıkış yükü 1A olduğu durumda, pozitif çıkış gerilim üretimi için, önerilen topoloji konvensiyonel topolojiye göre %8.8, tek uçan kapasitör içeren topolojiye göre %3.6 oranında verimlilik iyileştirmesi göstermiştir. Giriş gerilimi 3.8V ve çıkış yükü 1A olduğu durumda, pozitif çıkış gerilim üretimi için, önerilen topoloji konvensiyonel topolojiye göre %1.7 oranında verimlilik iyileştirmesi göstermiştir. Pozitif çıkış gerilimi üretimi için giriş geriliminin en fazla olduğu koşulda iletim kayıpları artmaya başlamış ve konvensiyonel topoloji ile tek uçan kapasitör içeren topolojiye göre verimlilik değerleri aşağıda kalmıştır. Buna rağmen, devrenin düşük görev döngüsü

ile çalışabiliyor olması ve indüktör kısıtlamalarının azalmış olmasından ötürü önerilen topoloji uygulamalarda tercih edilebilir. Bu tez çalışması bir anahtarlamalı dönüştürücüdeki temel parametreleri inceleyerek önerilen iki uçan kapasitör içeren devre topolojisi için iyileştirme olan yönleri vurgulamıştır. Bu çalışma tek indüktör kullanarak çift çıkış gerilimi sağlasa da, tek indüktör kullanarak çoklu çıkış gerilimi sağlanan yapı, önerilen iki uçan kapasitör devre ile gerçekleştirilebilir.

1. INTRODUCTION

Together with the increasing demand for portable applications, display drivers necessitating large positive and negative power supply voltages have become popular, such as active-matrix organic light-emitting diode (AMOLED) and passive-matrix organic light-emitting diode (PMOLED) drivers. Due to the growing need to reduce both in number and size of unnecessary board components to allow manufacturers of smart mobile solutions to integrate additional features and reduce the cost of material, the market for mobile applications has seen in the recent past an increase in the demand for compact voltage regulators.

The positive and negative power supply voltages were typically provided by two independently regulated DC-DC converters, a boost converter, and an inverting buck-boost converter, respectively. However, the mentioned configuration requires two inductors, leading to an increase in the development cost and an increase in the board area. Similarly, recent years have seen growth, visible in the literature and in the products released in the mobile market, of solutions based on hybrid topologies for power switching converters. They employ flying capacitors to reduce the constraints on the coil, generally limited in thickness and physical dimensions. Thus, the combination of coils and capacitors in hybrid topologies is able to increase performances like efficiency, ripple, etc. Hybrid solutions are not only often considered advantageous because they enable the use of smaller coil sizes but also, they permit the reduction of the voltage stress on the active switching components hence allowing the use of less resilient devices which are more efficient in terms of silicon area vs. series resistance.

1.1 Purpose of Thesis

This thesis investigates the Single-Inductor Dual-Output(SIDO) structure using two flying capacitors, utilizing the benefits of hybrid converter topology by further relaxing coil constraints and achieving better power efficiency and lower duty cycle, both

for negative and positive output voltage generation. A hybrid topology using two flying capacitors is proposed, aiming to reduce voltage stress on active switching components, hence allowing design with less resilient devices that are more efficient in terms of silicon area. By further reducing the voltage drop over the coil during the de-magnetization phase, the flying capacitor also helps decrease the inductor current ripple, the average inductor current, and the maximum inductor current. Consequently, lower core losses and AC losses can be obtained. These advantages lead to the flexibility of using smaller coils. Besides, decreasing the maximum inductor current enables converter operation at higher ambient temperatures due to lower losses. This will prevent saturation of the core and possible damage to the regulator.

Another advantage of the proposed topology is that, the switching converter operates with a lower duty cycle for the given load current, which relaxes the system stability requirements considering sub-harmonic oscillation and the output voltage collapse issue [1]. Reduction in the inductor current ripple will also alleviate the Electromagnetic Interference (EMI) noise generated by the converter. The trade-off of adding the flying capacitor is increasing in switching and resistive losses introduced by the additional switches to the topology. Although the thesis focuses on a SIDO, the generation of output rails with the introduced hybrid topology can be naturally extended to a single negative rail or to multiple negative and/or positive rails. Also in terms of applications supported, it is not limited to the generation of voltages down to -23V, but more in general of negative voltages, for instance also in a different range -5V to -9V.

1.2 Organization of Thesis

The thesis is organized as follows: Section II renders general switching converter concepts and the operation principle of switch mode regulators in comparison with linear regulators. To ensure the integrity of the work, the conduction modes of switching converters and control of the converters are explained briefly, since these concepts are processed in the thesis. As the last part of the switching converter background, loss contributors of the switching converters are described.

Section III introduces the power stage of the proposed SIDO converter with two flying capacitors and shows operation phases for both negative voltage and positive voltage generation, as well as with conventional topology and SIDO regulator with one flying capacitor topology. Section IV presents the circuit design, control loop design, and core loss modeling used in this work. Section V demonstrates the simulation results together with an evaluative comparison with no flying capacitor (NFC), one flying capacitor (1FC), and two flying capacitors (2FC) topologies. Finally, Section IV presents the conclusions and future works.

1.3 Literature Review

In portable electronic devices, AMOLED and PMOLED displays are mostly used, since they have such advantages as low current consumption, cost-effectiveness, and superior image quality. To be compatible with the analog control voltage domain, bipolar supply rails are usually necessary. Therefore, having a DC-DC converter with bipolar output voltages becomes important [2].

Apart from AMOLED and PMOLED display drive applications, the PMICs that supply power to all circuits in the system, are required to generate several voltage outputs with high efficiency in a small area. The challenge of designing power management circuits is providing enough energy to different kinds of circuits in their type of functioning. This may require high efficiency at high loads, low quiescent current, and high performance in a wide load range.

It has been seen in the literature and in the market, the requirement of having two different voltage rails have been attained by using two different DC-DC converter in a single chip, presented in [3,4]. The work given in [3], uses two different DC-DC converters for bipolar outputs for the AMOLED application. In this work, the positive output voltage is regulated by a buck DC-DC converter, and the negative output voltage is regulated by an inverting buck-boost DC-DC converter. Using two converters for generating two different voltage rail may be beneficial for generating quiet output voltage, where two different switching scheme does not affect each other. However, this solution suffers from the increased area and high-cost development due to two inductors.

Single-Inductor Dual-Output (SIDO) structures with bipolar output voltage rails (generating both positive and negative supply) are preferred in portable applications, as a single inductor offers reduced Electromagnetic Interference(EMI) and board area. Several studies have been presented in literature about SIDO converters given by [5]–[9]. The SIDO regulators have also started to stand high in the market due to their ultra-compact size and low bill of materials to generate double outputs. Many technology companies design and manufacture SIDO regulators as present in [10]–[12].

The most important design specification of the switching converter is efficiency. There were many attempts to increase the efficiency of the SIDO converters with proper switching techniques [13]. Another attempt of increasing the efficiency is to add a flying capacitor into the circuit, presented in [14]. The work suggests adding a flying capacitor into the circuit to decrease the voltage applied to the inductor, therefore, decreasing the inductor current ripple. Owing to the decreased inductor current ripple, conduction loss decreases. [2] proposes a hybrid SIDO DC-DC converter for AMOLED displays. To overcome the large inductor current ripple, the work [2] uses a flying capacitor to form a hybrid SIDO converter. Due to the flying capacitor added into the charging path, now the voltage stress across power switches is decreased, allowing to use standard 5V CMOS process and increasing power efficiency.

The structure can be extended to the generation of multiple outputs by using a single power inductor, given by [15]–[17]. [15] presents Single-Inductor Multiple-Output(SIMO) hybrid DC-DC converter with an integrated flying capacitor for SoC(System on Chip) applications. The work proposes a hybrid power stage that can improve conversion efficiency by reducing inductor current while extending the output voltage range.

Naturally, there are pros and cons for each topology, as in any engineering solution. The drawback of the SIDO converter is increased control complexity and cross-regulation. Cross-regulation issue is often observed in converters that have more than one output, during load transient applied to one of its outputs. The load transient applied to one of the outputs of the converter affects the other outputs is called cross-regulation. The issue arises from the nature of the SIMO converters since

they have multiple outputs sharing one power inductor. There are several works in the literature that discuss proper solutions for cross-regulation and for better transient responses [18]–[20].

[21] explores the theoretical limit of the cross-regulation in the example of three outputs boost converter. The method proposed in the paper can be used to optimize the control mechanism to deliver enough current to all outputs and have improved transient operation.

In this thesis work, the advantages of hybrid topology are emphasized by doing modifications in the conventional SIDO circuitry. Control circuitry is kept simple yet the converter is still able to provide regulated output. This thesis work puts the idea of having a flying capacitor beyond further and takes advantage of the hybrid topology, by using multiple flying capacitors in the context of buck-boost topology.

2. SWITCHING CONVERTER CONCEPTS

The switching converters are designed to provide a regulated output voltage while stepping down or stepping up the input voltage, as an example of delivering voltage to the sub-blocks in Li-ion-powered portable devices. The switching regulator uses a switching device such as FET(Field Effect Transistor) or diode and generates pulsating voltage, then smoothes that pulsating voltage with output filtering. The energy storage element in switching converters is the inductor which is the key factor of better efficiency. The voltage regulation can also be maintained by the Low-Dropout(LDO) regulator. They use a pass device to create a voltage drop which determines the output voltage regulation level by implication of dropout voltage, as is one of the critical design parameters of the LDO.

LDO regulators are able only to drop the input voltage as the dropout voltage allows. Dropout voltage is the minimum difference voltage between the input supply V_{IN} and the output voltage V_{OUT} to attain proper regulation. The dropout voltage is defined by Eq. 2.1.

$$V_{DO} = V_{IN} - V_{OUT} \tag{2.1}$$

The general scheme of the LDO regulator is illustrated in Fig. 2.1. The basic scheme of LDO consists of a pass device, an error amplifier, and a feedback network. The pass device creates a voltage drop proportional to $R_{DS(ON)}$ and load current, where $R_{DS(ON)}$ is the on-resistance of the pass device. The error amplifier differentiates between the output voltage and the reference voltage, creating an error voltage to drive the pass device.

The linear regulators have higher heat losses dissipated by the pass element, and become less efficient as dropout voltage increases. The LDO regulators do not serve high efficiency unless the dropout voltage is small enough. For instance, in an application that uses an LDO regulator, the input supply voltage can be 5V, and the

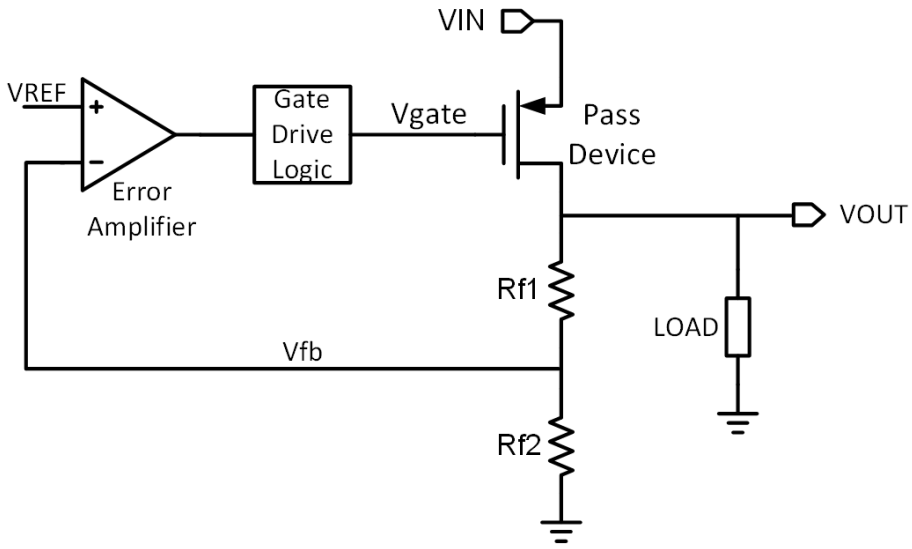

Figure 2.1 : General circuit scheme of LDO regulator.

regulator's output voltage can be 3.3V to supply MCUs. Linear regulators carry the advantages of being low cost, design simplicity, and having less output noise compared to the switching converter, but they stand back in terms of efficiency. Linear regulators are a powerful choice if the application is based on providing very low power to the device or in applications where the input and output voltage difference is small. If higher efficiency is required, unless the difference between the input and output voltage is small, switching regulators are preferred over linear regulators, as they can provide output voltages higher or lower than the input voltage.

The switching converter operating principle is based on the switching ON and OFF of the switching element. During the ON time, the energy is stored in the storage element, which is the inductor. During the OFF time, the energy is released to the output. The total period of the switching is the sum of ON time and OFF time; however, this summation is only valid in Continuous Conduction Mode(CCM), as will be explained in the next section. For now, it is assumed as a direct summation for the sake of simplicity. The amount of charge desired to transfer to the load is determined by the duty cycle D, which defines as the ON time of the switch over the total period. Since the switching element is either fully ON or fully OFF, ideally, there is no power dissipated by the switching element, making the switching converters more efficient. The general scheme of the switching converter is given by Fig. 2.2.

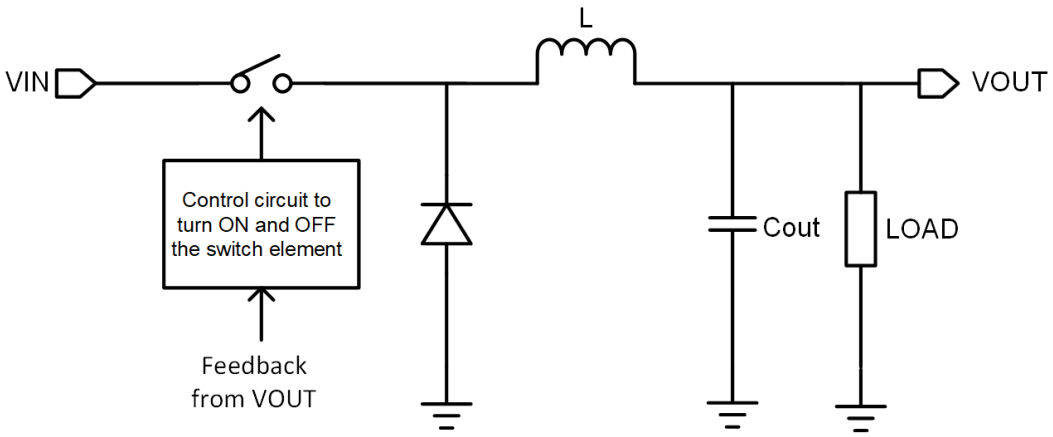

Figure 2.2 : Switching converter general circuit scheme.

There are common specifications of the regulators, whether it is switch mode or linear, that define the performance of the regulator. Their definition is the same for each type, but the specifications will be explained in the context of switch mode regulators. Efficiency is the measure of how much input power has been delivered to the output by the regulator during the operation. The total power loss incorporates several loss contributors that limit efficiency. These possible losses will be explained later in the chapters. The equation of power efficiency η, given by Eq. 2.2. Parameters in the equation are defined as follows; V_{out} is the steady state output voltage, I_{out} output load, V_{in} input supply voltage, and I_{in} input current.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}I_{in}} \tag{2.2}$$

There exists output filtering in the switch mode converters to obtain smooth output voltage by the output capacitor. Considering the equivalent series resistance (ESR) of the capacitor, this resistance directly affects the switching performance. Some of the affected parameters are output voltage ripple, efficiency, and loop stability. If the ESR increases, the output voltage ripple will be increased consequently. Since the output load flows into and out of the capacitor, the current also flows through the ESR, creating resistive loss and directly decreasing efficiency. The proper type of capacitor should be selected considering the above points.

One of the most critical concerns in switch mode converters is Electromagnetic Interference (EMI). Switching ON and OFF at higher frequencies creates higher switch voltage and current slew rates, creating a broad spectrum of emissions. The unwanted electromagnetic noise may get involved in the electrical path and may cause the corruption of the overall system. This work also points to mitigating EMI issues directly with the structure since only one inductor is used in the design for double outputs. Besides, the voltage drop over the coil decreased with the addition of the flying capacitor, which means that the inductor current slew rate decreased based on the formula given in Eq. 2.3.

$$V_L = L * \frac{\partial I_L}{\partial t} \tag{2.3}$$

As mentioned earlier at the beginning of the chapter, there are various types of DC-DC switching converters, such as buck(step-down), boost(step-down), buck-boost(either step-up or step-down), etc. The different converter topologies can be used together if the application requires two different voltage levels in the system, such as AMOLED and PMOLED display drivers in portable devices. Nonetheless, this means doubling the inductor and the number of the pass devices and the output filtering, which creates an excessive footprint area. This work focuses on generating two different voltage levels using one structure, later explained as Single-Inductor Dual-Output (SIDO) structure. Therefore, only one inductor is required to generate two outputs.

Of course, the work can be extended to using more than two outputs as suggested in [23], but it comes with design issues such as stability problems and increased complexity but the reduced board area. Fig. 2.3 shows an example structure of a Single-Inductor Multiple-Output circuit generating multiple outputs and a conventional scheme generating multiple outputs with each individual DC-DC converter. This work tackles the advantages of the SIDO structure, such as increased efficiency for both outputs thanks to the flying capacitor added into the circuit.

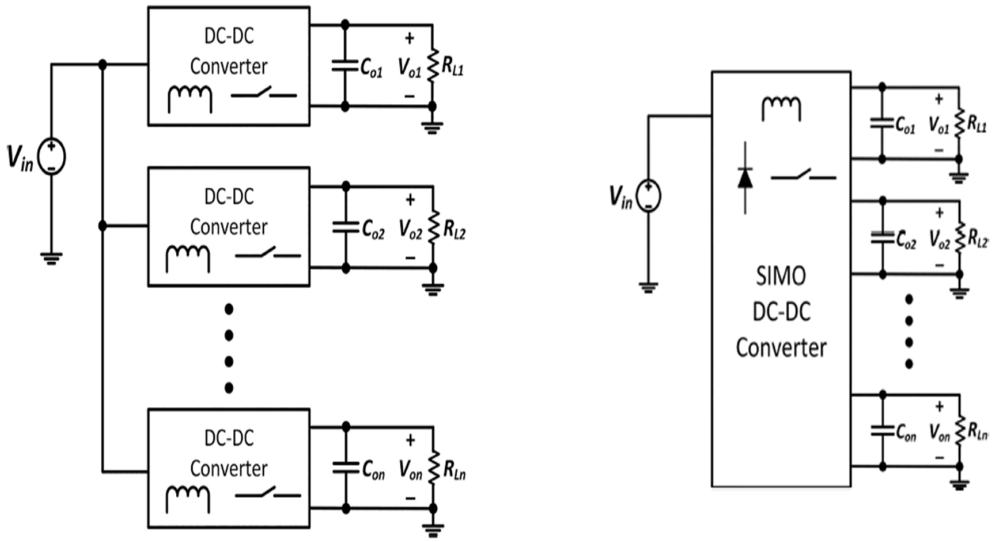

Figure 2.3 : Comparison circuit schemes of multiple DC-DC converter generating multiple outputs and SIMO DC-DC converter [22].

2.1 Conduction Modes of the Switching Converters

The conduction mode of the switching converters differs based on the inductor current behavior within the switching period. If the inductor current never falls below zero, this means that the inductor does not completely discharges within a switching cycle; this operation is called Continuous Conduction Mode (CCM). On the contrary, if the inductor current falls below zero or stays at zero for a time period(dead time), this means that the inductor completely discharges before the next switching cycle starts; this operation mode is called Discontinuous Conduction Mode (DCM). The inductor current waveform and the voltage drop over the inductor in both CCM and DCM operation are illustrated in Fig. 2.4.

Each operation mode has its own advantages and disadvantages. The operation mode of the converter can be important for high-load or low-load efficiency. Even though the operation mode depends on the application, DCM is preferred for better efficiency at low loads and low-power applications. The CCM is preferred where better power efficiency is required at high loads and high power. The energy stored in the inductor is determined by the output loads so that the output load can define the operation mode. That is to say when the load changes converter changes its operating mode.

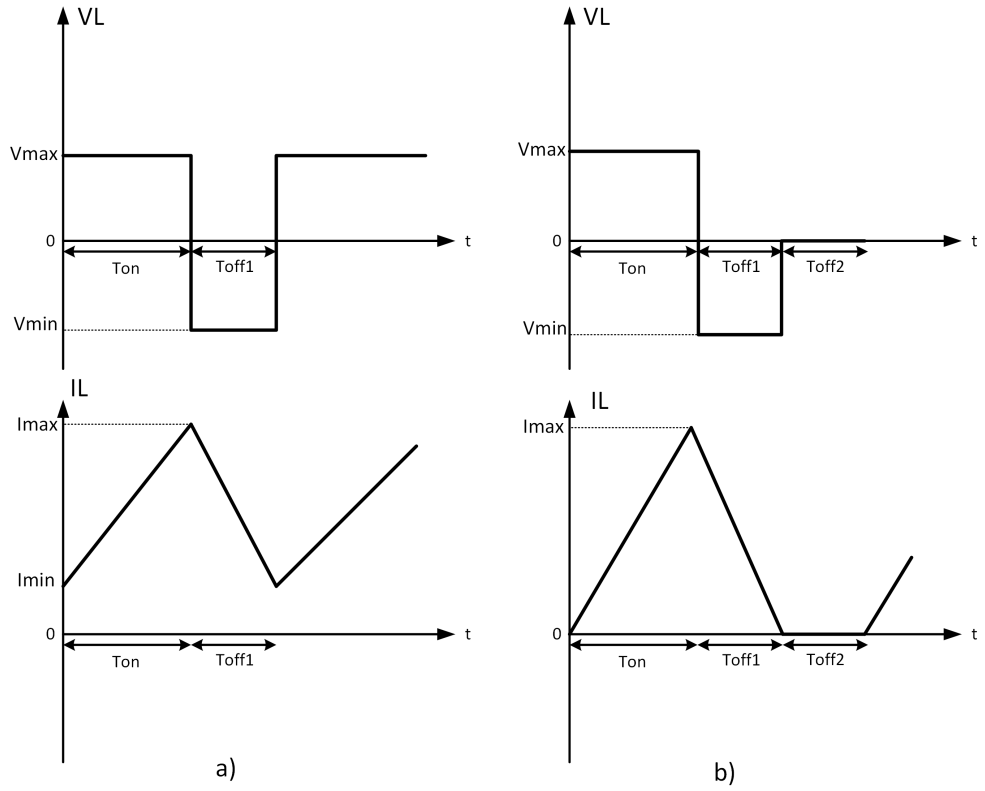

Figure 2.4 : Inductor voltage and inductor current waveform
a) CCM operation b) DCM operation.

Another aspect is the value of inductance, the ability of an inductor to store energy in the form of a magnetic field, which sets the operation mode. The inductor current ripple in DCM operation is higher since the inductor completely charges and discharges, which translates to higher core losses. Also in DCM operation, a higher output voltage ripple occurs. Another result of the inductor current is completely charged and discharged in each switching cycle is the peak currents create significant EMI. The extreme level of EMI should be suppressed with proper filtering, which requires larger capacitors in the system. In DCM operation, a lower inductance value can be used compared to CCM since lower inductance implies a higher inductor current ripple. The voltage conversion ratio M, the ratio of V_{out} and V_{in}, does not depend on the output load in CCM. This means the duty cycle defines the output voltage in CCM. On the contrary, in DCM operation, the output voltage is defined by the duty cycle and the output load.

2.2 Control of the Converters

Each converter requires a control loop to deliver regulated voltage to the output. That makes loop stability one of the main concerns of switching converters. Switching converters use negative feedback loop to keep the output voltage at the desired voltage level. The control of the converters can be maintained in many different approaches based on the requirements. The general control methods used in the switching converters will be explained in this section.

2.2.1 Voltage mode control

The most common control method used in regulators is voltage mode control. The general scheme of the voltage mode control is demonstrated in Fig. 2.5. In the conventional voltage mode control, the output voltage is compared with the reference voltage. Then, the differential voltage called V_{err}, created by the error amplifier, is compared with a constant ramp waveform by PWM (Pulse Width Modulation) comparator. The duty cycle of the PWM comparator changes based on the generated error voltage, V_{err}. In other words, when the output voltage exceeds the reference voltage, the V_{err} increases, and the PWM comparator generates an increased duty cycle signal to compensate for the error voltage. The output state of the PWM comparator goes through a logic circuit that sets one or more parameters(on-time, off-time, frequency,peak-to-peak ripple voltage, etc.) of the converter [24].

The advantage of voltage mode control is that it requires only one feedback loop, so the feedback network design is relatively simple. On the contrary, the output filter adds two poles to the control loop, making the compensation network more complicated and harder to stable. In this control method, any line or load change is first sensed as an output change and then corrected by the loop, showing a slow transient response to the disturbances.

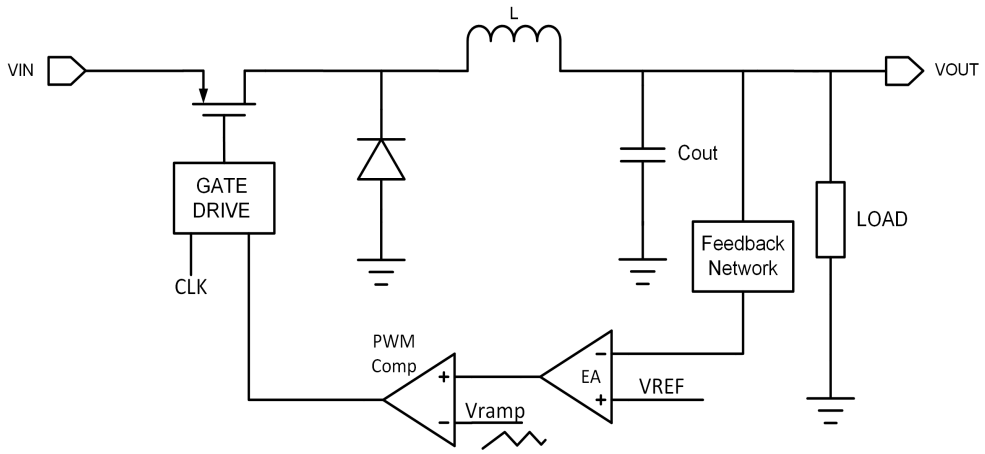

Figure 2.5 : General voltage mode control scheme.

2.2.2 Current mode control

Different than the voltage mode control, the current mode control scheme uses inductor current as part of the feedback loop. Similar to the voltage mode control, V_{err} voltage is still part of the feedback loop. The inductor current sense signal and V_{err} voltage are now two inputs of the PWM comparator. Therefore, current mode control requires two feedback loops. The controller takes the output voltage error as the outer loop and the inductor current information as the inner loop. The output voltage of the error amplifier V_{err} sets the desired inductor peak level. The sensed inductor current is compared with V_{err} then the output of the PWM comparator is obtained. The general current mode control scheme is given by Fig. 2.6. In the scheme given for the current mode control, the inductor current is sensed with the series resistance of the inductor. Other feedback mechanisms for sensing the inductor current can be employed as well such as sensing from power FET, given by [25].

The most important advantage of the current mode control is that the phase compensation of such a controller is easier compared to voltage mode control. Current mode control has a single pole at the resonant frequency in contrast the voltage mode control shows double poles at the resonant frequency. This means, in voltage mode control, two zeros from the compensator network are required the cancel out the double pole at resonant frequency but only one zero to cancel out the single pole of current

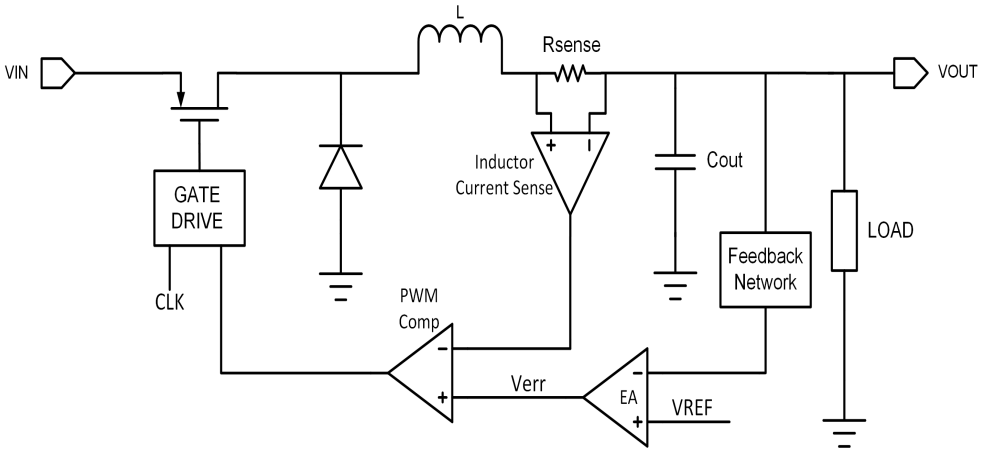

Figure 2.6 : General current mode control scheme.

mode control. Generally, a Type 2 compensator based on a transconductance error amplifier can be used in current mode control, whereas voltage mode control needs a more complicated Type 3 compensator. The other issue, apart from the cancellation of the double pole arising from the characteristics of the voltage mode control, is that there can be a phase shift which may lead to stability problems [26].

Apart from the advantages of the current mode control, the phenomenon of sub-harmonic oscillation stands out as one of the primary drawbacks. If a sudden line or load disturbances occur and the inductor current can not return back to its initial value at the beginning of the switching cycle, the sub-harmonic oscillation occurs. Even though the converter is already in the sub-harmonic oscillation condition, the behavior can not be observed in a steady state unless perturbation is applied to the converter. This phenomenon is seen where the duty cycle is greater than 50% and in CCM operation. The instability is not present in DCM operation. In the case of a higher duty cycle than 50%, the perturbation grows in each switching cycle and shows instability. For duty cycles lower than 50%, the perturbation damps and returns back to steady-state conditions. The visual representation of the sub-harmonic oscillation is given in Fig. 2.7.

The method called slope compensation is present as one of the solutions to this problem. By adding a compensating ramp equal to the falling slope of the inductor current, any disposition toward sub-harmonic oscillation is damped within one switching cycle [27]. The methods applying proper slope compensation for stable

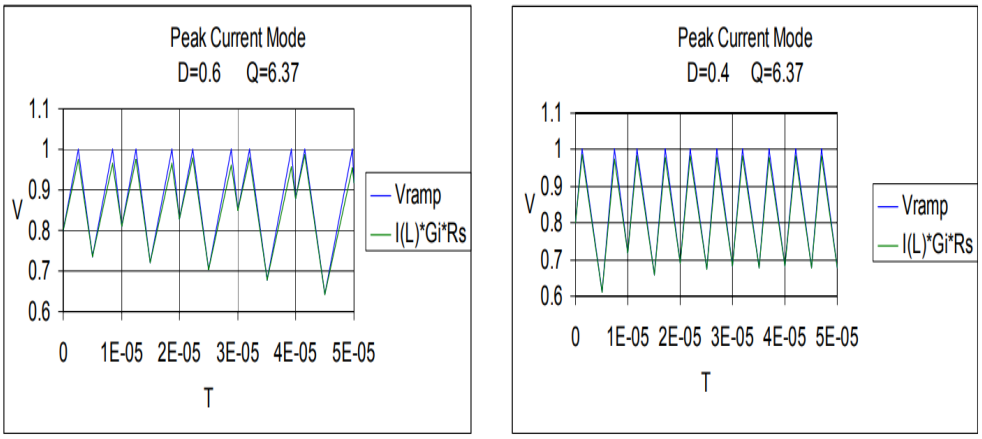

Figure 2.7 : Visual representation of sub-harmonic oscillation. For D<0.5, sub-harmonic oscillation is damped. For D>0.5, instability grows in each cycle [27].

converter operation are still under research in the literature [28]–[30]. The other design methods for eliminating the sub-harmonic oscillation are increasing the inductance or reducing the loop bandwidth as per pre-defined design limits.

One of the disadvantages of the current mode control is this noise sensitivity. The current mode control suffers from noise sensitivity because, in this method, the control loop relies on the small sensed inductor current to generate a voltage ramp to the PWM comparator. Switching the power devices *ON* and *OFF* generates a lot of noise. Therefore, a time duration needs to be introduced to avoid false triggering of the comparator after the switch turns *ON*. Introducing this blank time leads to establishing a minimum *ON* time pulse width also the amount of the blank time. This situation creates limitations in the high-voltage to low-voltage conversion applications due to the limited duty cycle. Therefore, compared to current mode control, voltage mode control is more robust in design and noise resistant.

2.2.3 Hysteretic control

Instead of generating the V_{err} by differentiating the output voltage and the reference voltage by using an error amplifier, the hysteretic control directly monitors the output voltage level (voltage mode hysteretic control) or the inductor current sense signal (current mode hysteretic control), then this information constitutes two inputs of the hysteretic comparator together with the reference voltage.

The example scheme of the hysteretic control is given in Fig. 2.8. In this control method, the ON and OFF states of the switch are determined by the pre-set threshold levels. There are two different threshold levels to determine when power switches are in the ON or OFF state. A control signal is used with a hysteresis band to determine the turn-on and turn-off times of the switch. The hysteresis band of the comparator is indicated as V_H which is the difference between the upper threshold level and the lower threshold level.

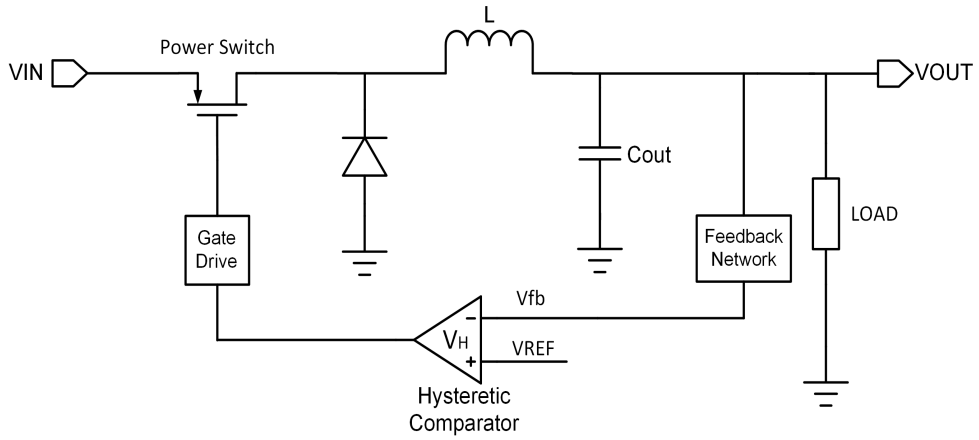

Figure 2.8 : General scheme of hysteretic control.

When the switch turns ON and the inductor current increases, the inductor current flows into the output capacitor and increases the output voltage. When feedback voltage V_{fb}, exceeds the upper threshold of the comparator, the output of the hysteretic comparator goes low and causes the turn OFF the switch. Afterward; the inductor current starts to decrease, causing a decrease in output voltage and feedback voltage. While the inductor current is decreasing, eventually feedback voltage drops below the lower threshold of the hysteretic comparator and changes output state to high and causing the turn ON the switch. Although voltage and current mode control require the clock to ensure constant frequency, no external clock or ramp is needed in hysteretic control [24]. Since hysteretic control does not need any clock, error amplifier, or compensation circuitry, this control method is suitable for low-IQ applications. The drawback of hysteretic control is ensuring constant frequency. Since there is no clock needed, there may be a lot of irregular pulses, which should be avoided. The constant on-time method can be employed to ensure almost constant frequency operation in

hysteretic control. In this method, a well-defined switching frequency is ensured by placing a timer into the circuit to define switch *ON* time.

Although Fig. 2.8 shows an example of voltage-mode hysteretic control, the current mode hysteretic control is also present in literature, such as [31]–[33]. The work presented in [33] proposes a hysteretic current control scheme for buck-boost SIDO converter.

2.3 Loss Contributors of the Switching Converters

The most important design specification of the switching converters is efficiency, which is the measure of how much power has been dissipated by the converter without being delivered to the output. Therefore, all the possible loss contributors should be carefully identified for a better assumption of the converter performance in the first design phase. Moreover, they should be eliminated as much as possible with proper design techniques. The major loss contributors of the switching converter are illustrated in Fig. 2.9, in the example of a buck converter.

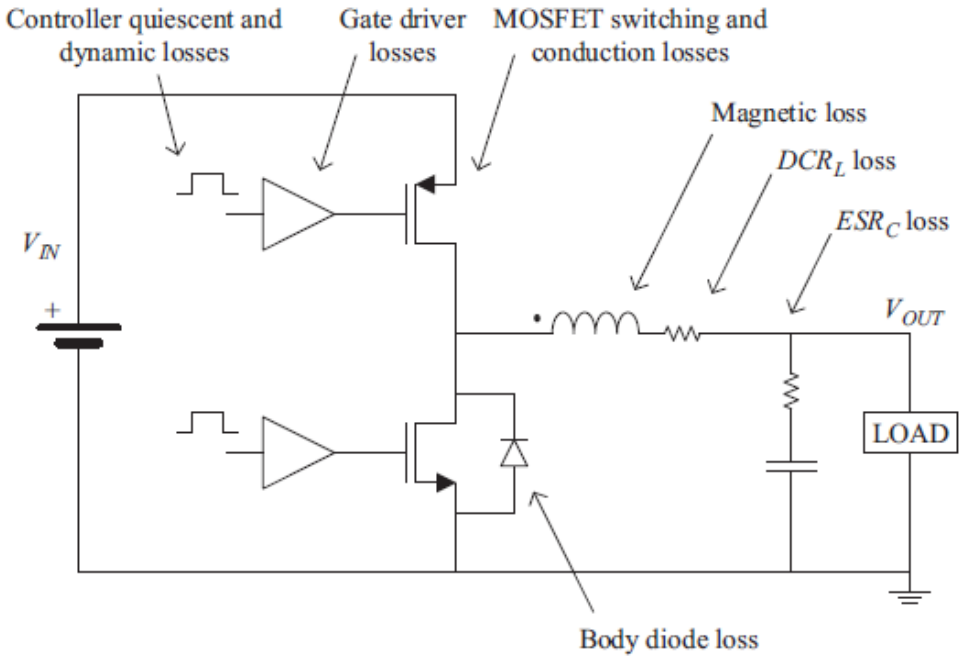

Figure 2.9 : Mechanism of power losses in the example of Buck Converter [34].

FETs tend to occupy the highest power losses in any converter circuits. They contribute to conductive(resistive) and switching(capacitive) losses among the total loss. The conduction losses dominate the power losses at high load currents. The conduction losses are caused by the R_{ON} resistance of the devices and the time they conduct current. The conduction losses MOSFETs create can be defined in Eq. 2.4. In the formula, D represents the duty cycle, $R_{DS(ON)}$ represents the on-resistance of the switch, and $I_{MOSFET(avg)}$ represents averaged MOSFET current.

$$P_{cond(mos)} = I^2_{MOSFET(avg)} R_{DS(ON)} D \tag{2.4}$$

Switching losses dominate at low loads and occur due to switching of the pass devices, pass device drivers, and the parasitic capacitances at the other switching nodes [34]. In the formula given by Eq. 2.5, capacitance, C is the sum of the corresponding pass device capacitors, pass device driver capacitors, and printed circuit board(PCB) parasitic capacitors. Here, f_s donates switching frequency, and V_{DD} is the input supply voltage of the converter.

$$P_c = C f_s V^2_{DD} \tag{2.5}$$

The pass devices in the switching converters are generally designed wide to carry a huge amount of current. This sizing creates the large capacitance associated with the pass devices. The capacitors will be charged and discharged as pass devices switch, creating another loss contributor. The gate drive power loss can be defined in Eq. 2.6. In the formula, V_{GS} is the gate-source voltage of the MOSFET switch.

$$P_{gate} = (C_{gp} + C_{gn}) f_s V^2_{GS} \tag{2.6}$$

The PMOS gate capacitance($C_{gp)}$ and NMOS gate capacitance($C_{gn)}$ are given in Eq. 2.7 and Eq. 2.8, respectively. Here C_{ox} and C_o are process parameters [35].

$$C_{gp} = C_{ox} w_p l + 2 C_o w_p \tag{2.7}$$

$$C_{gn} = C_{ox} w_n l + 2C_o w_n \tag{2.8}$$

The analog sub-blocks in the chip consume current during the operation, which translates to another loss contributor. In general, the analog sub-blocks are designed to be low I_Q; therefore, the loss coming from the analog sub-blocks and the control circuitry dominate the power losses at low load currents. In the formula given by Eq. 2.9, I_Q stands for the quiescent current, which is the current consumed by the sub-blocks when the switching converter is functioning.

$$P_q = I_Q V_{DD} \tag{2.9}$$

The non-overlapping time scheme is used by many converters, mostly in synchronous converters, to prevent shoot-through current and possible damage to the pass devices. A suitable amount of time is inserted intentionally between the switching sequence of the pass devices; during this time converter is in tri-state, and pass devices are not conducting. As a consequence, during non-overlapping time, body diode conduction occurs. The current flowing through the body diode creates loss defined as in Eq. 2.10. V_{dio} is the diode forward-bias voltage, T_{nol} is the non-overlap time, I_{out} is output load. The amount of non-overlap time should be properly selected such that the time duration balances the risk of shoot-through and the power loss dissipated by the body diode of the switches.

$$P_{NOL} = V_{dio} T_{nol} I_{out} f_s \tag{2.10}$$

The output capacitor's internal resistance, known as equivalent series resistance R_{esr}, contributes to resistive losses. The power dissipated by the,R_{esr} can be derived as in Eq. 2.11. I_{ripple} represents the inductor current ripple.

$$P_{ESR} = R_{ESR} I_{ripple}^2 \tag{2.11}$$

The internal resistance of the inductor is due to the resistance of the coil called direct current resistance. However, this also creates another resistive loss. The power

dissipated by the DCR of the inductor can be calculated as in the Eq. 2.12. In the formula, $I_{L(avg)}$ denotes the average inductor current.

$$P_{DCR} = R_{dcr} I^2_{L(avg)} \tag{2.12}$$

The inductors are created by the core material winded by a conductor in turns. The core material is manufactured of ferromagnetic material to store magnetic energy temporarily by creating magnetic flux. Magnetic loss occurs from the core and the windings. The core losses can be calculated by Steinmetz Equations given by Eq. 2.13. In the formula given by Eq. 2.13, α,m,n are the core coefficients, V is the volume of the core, and ΔB is magnetic flux density change.

$$Pcore = \alpha V \Delta B^m f_s^n \tag{2.13}$$

However, this equation has some practical issues in the context of switching converters. The equation assumes that the core material is subjected to a sinusoidal wave. However, the inductor in the switching converter sees a square wave, which creates an error in the core material coefficients. A detailed core loss estimation method used in this work will be presented later in the chapter.

3. SINGLE-INDUCTOR DUAL-OUTPUT VOLTAGE REGULATORS

A conventional Single-Inductor Dual-Output (SIDO) regulator topology with positive and negative output voltage rails is given by Fig. 3.1. The topology is indeed a buck-boost converter, which converts positive input supply V_{IN} to a higher positive output voltage V_{POS} by non-inverting buck-boost switching sequence, or lower negative output voltage V_{NEG} by an inverting buck-boost switching sequence. An operating principle is first storing the energy on the inductor and releasing the energy to the output capacitor. Therefore, the output is charged only when the inductor is discharging.

The switching scheme of conventional topology(NFC), SIDO with one flying capacitor topology(1FC), and proposed SIDO topology with two flying capacitors(2FC) will be demonstrated in this chapter for negative and positive output voltage generation.

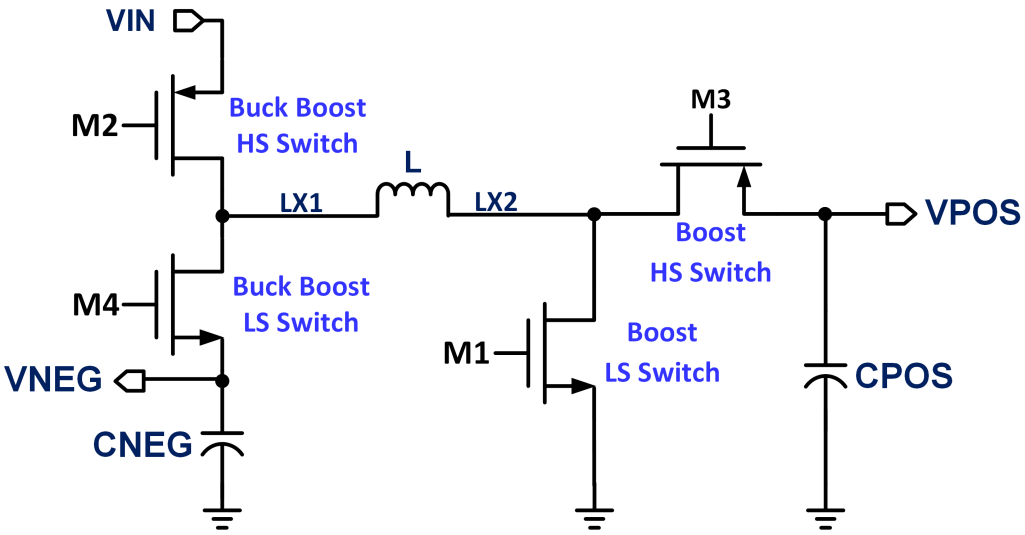

Figure 3.1 : Power stage of conventional SIDO converter.

3.1 Negative Output Regulation

Given by the topology in Fig. 3.1, to generate the negative output voltage V_{NEG}, the switching sequence of the regulator is as follows: in the first phase, when

magnetizing the inductor, M_1 and M_2 are ON, the inductor current is increasing with a slope of V_{IN}/L, where V_{IN} is the input supply voltage. In the second phase, when de-magnetizing the inductor, M_1 and M_4 are ON, the inductor current is decreasing with a slope of -V_{NEG}/L. Current stored in the inductor is flowing to the ground through M_1 while reducing the voltage on C_{NEG} through M_4, thus generating a negative voltage at the output V_{NEG}. According to inductor volt-second balance and power balance equations, the converter voltage conversion ratio and average inductor current can be derived in terms of duty cycle D, in Eq 3.1 and in Eq. 3.2, respectively. All of the voltage conversion ratios for each topology given in this work assume there are no inductor loss and power loss across the pass devices. The loss effect on the ratio will be examined in the results section.

$$\frac{Vout}{Vin} = -\frac{D}{1-D} \tag{3.1}$$

$$I_{L(avg)} = \frac{1}{1-D} I_{out} \tag{3.2}$$

There exist various topology limitations of this converter regarding negative output voltage generation: during the de-magnetization phase, the inductor observes a voltage drop close to V_{NEG}. For significantly low values of V_{NEG} (e.g., $-20V$ for an AMOLED application), this voltage drop will result in high inductor current ripple and core losses [34], leading to a decrease in power efficiency. Higher $\partial I_L/\partial t$ during this phase also results in increased reverse recovery loss for MOSFET switches. In addition to that, during the magnetization phase of the inductor, M_4 observes a V_{DS} of $|V_{NEG}| + V_{IN}$, which sets a relatively high voltage constraint on the switch device safe operating region.

To address the mentioned performance improvements, a SIDO converter with a flying capacitor has been presented in the literature, such as [2]. In this topology, a flying capacitor C_F and a switch M_C are added to reduce the voltage drop on the inductor and M_4, thus addressing the mentioned issues. Fig. 3.2 shows the topology of a SIDO converter with one flying capacitor (1FC).

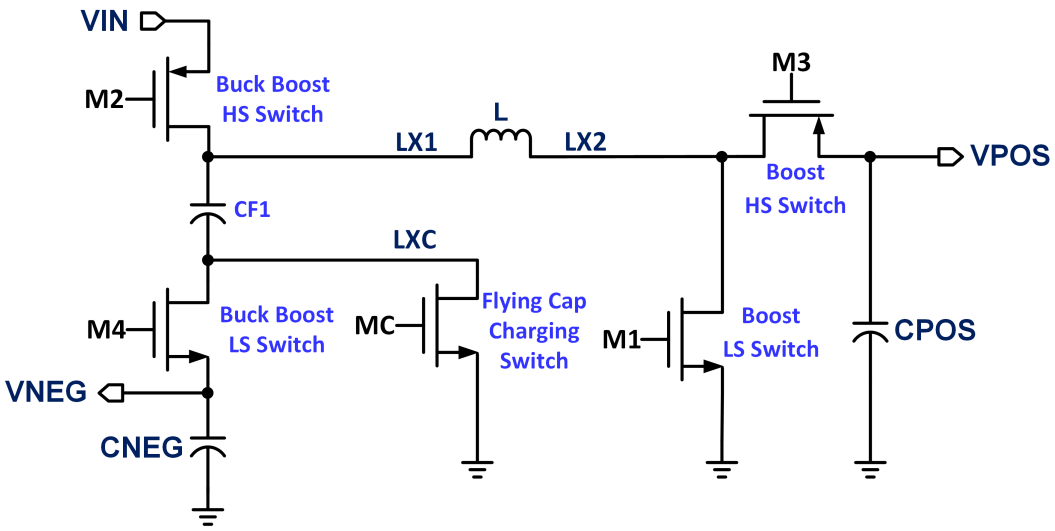

Figure 3.2 : Power stage of SIDO converter with one flying capacitor.

The operating principle is described as follows: in the first phase, when magnetizing the inductor, M_1, M_2, and M_C are ON. The inductor current is increasing with a slope of V_{IN}/L and C_{F1} is charged to V_{IN} through the input supply and M_C. During this phase, the V_{DS} voltage drop on M_4 is reduced to $|V_{NEG}|$, which relaxes the voltage constraint on the switch by a V_{IN}, with respect to the conventional SIDO converter given by Fig. 3.1. In the second phase, when de-magnetizing the inductor, M_1 and M_4 are ON. Voltage drop on the inductor is reduced to V_{NEG}+V_{IN}, thus the $\partial I_L/\partial t$ slope is decreased. Fig. 3.3 shows control signals as well as inductor voltage drop illustrations for the SIDO with one flying capacitor topology.

According to the inductor-volt second balance and power balance equations, the voltage conversion ratio and average inductor current can be obtained as given by Eq. 3.3 and in Eq. 3.4, respectively.

$$\frac{Vout}{Vin} = -\frac{1}{1-D} \tag{3.3}$$

$$I_{L(avg)} = \frac{1}{1-D} I_{out} \tag{3.4}$$

Reducing the voltage drop on the negative rail switch M_4, enables to extension output voltage range to values beyond process limitations. Another advantage of this topology presented in Fig. 3.2 is that LX_1-LX_C voltage difference is always close to V_{IN} meaning

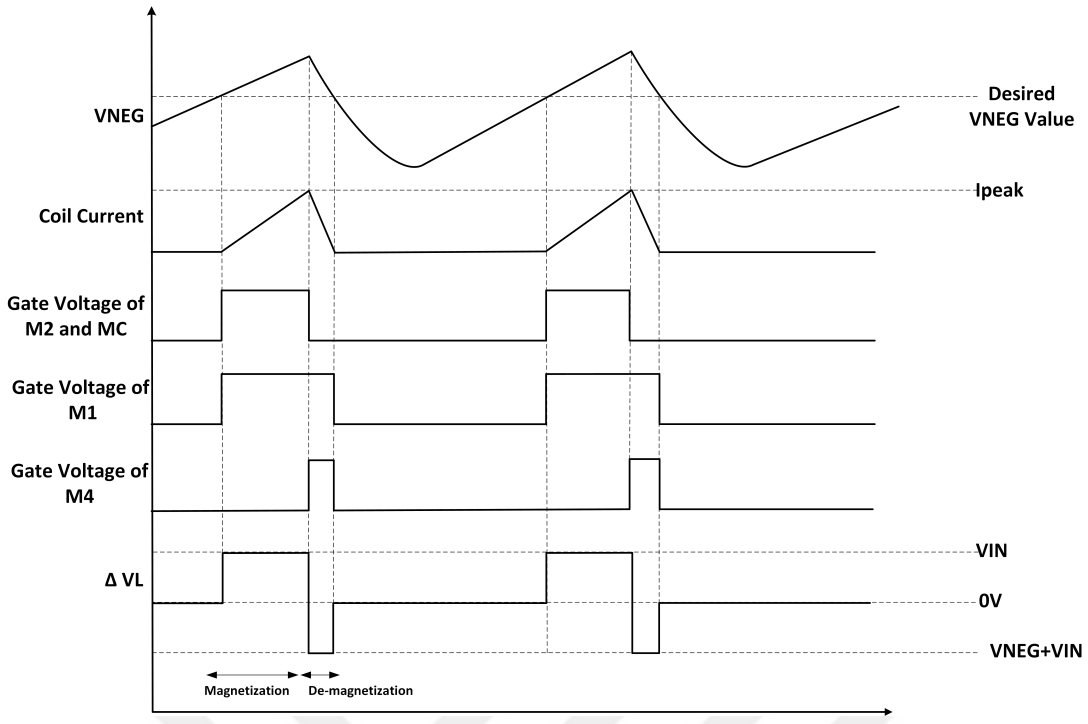

Figure 3.3 : Control signals of SIDO with Flying Capacitor.

that the newly added flying capacitor does not see any high voltage hence derating of the capacitor is minimum, making available to use of smaller capacitors.
Multiple flying capacitors can be stacked in the topology, allowing further reduction on the voltage drop over the inductor during the de-magnetization phase by $n \cdot V_{IN}$, where n is the number of flying capacitors.

A second flying capacitor is introduced to the SIDO converter topology to alleviate the aforementioned issues and improve the switching converter performance. The proposed SIDO converter is given in Fig. 3.4. The second flying capacitor, C_{F2}, is introduced to the circuit in series with the first flying capacitor and M_2. M_{C2} is added to the circuit to create the path from V_{IN} to the ground while charging the second flying capacitor C_{F2}, to the supply voltage V_{IN} at the first phase. The bypass switch M_5 creates the path from V_{IN} when charging the second flying capacitor. The coupling switch M_2 allows to connection of two flying capacitors in series when the inductor current is discharging, therefore improving the inductor voltage drop at the de-magnetization phase by $2 \cdot V_{IN}$.

In the application, the negative voltage can be as low as -10V at an output load condition of 1A. This requires a big-sized coil or multiple phases to provide enough current to the output in the case of high-power applications. Because the negatively boosted maximum voltage is dependent on the maximum current that can be delivered to the output and the on-resistance of the switches on the current path. Therefore, reducing the voltage drop of the inductor by a factor of V_{IN} positively affects the design in terms of efficiency and relaxes the constraints on the coil. A design option to switch between 1FC topology and 2FC topology also exists, by connecting the source terminal of M_5 to $LX1$ node, providing modularity to the topology.

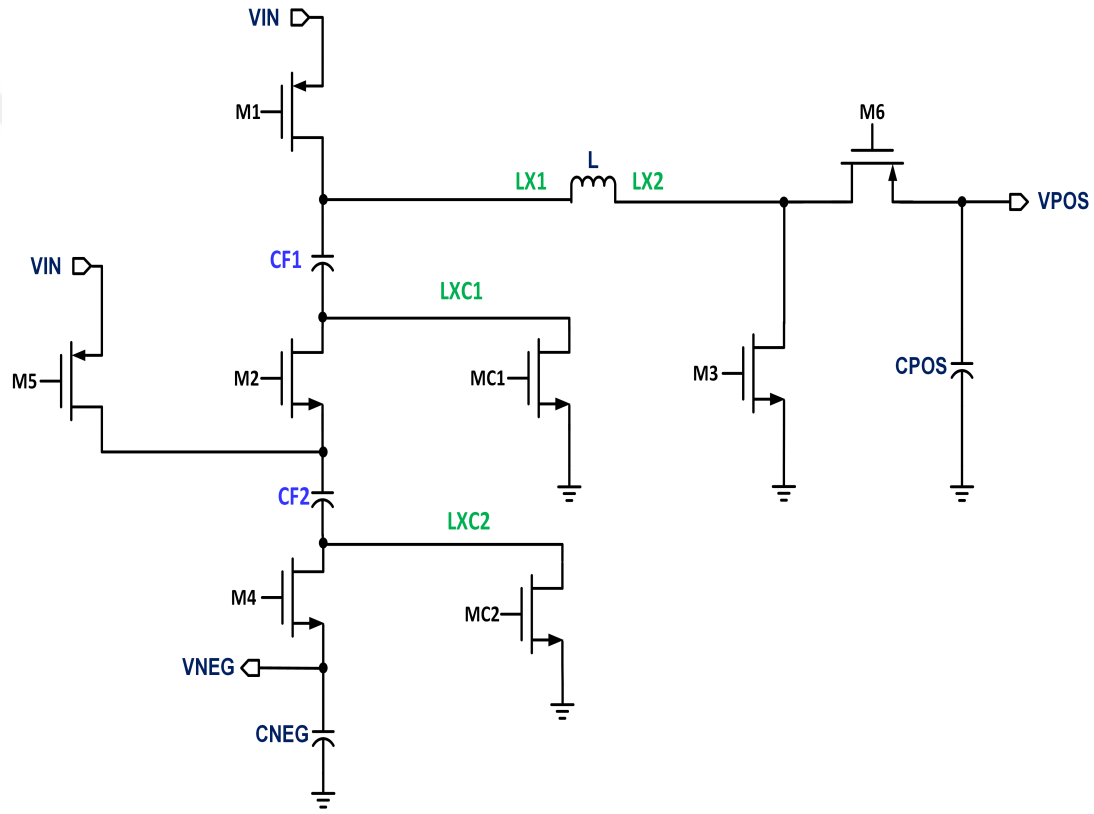

Figure 3.4 : Power stage of SIDO converter with two flying capacitors.

To generate a negative output voltage, switch states are as follows: in the first phase, when magnetizing the inductor, M_1, M_{C1}, M_{C2}, M_5, and M_3 are ON. The inductor current is increasing with a slope of V_{IN}/L. During this phase, the two flying capacitors are charged up to V_{IN}. When de-magnetizing the inductor, M_3, M_4, and M_2 are ON. The inductor current is decreasing with a slope of $(V_{NEG} + 2 \cdot V_{IN})/L$.

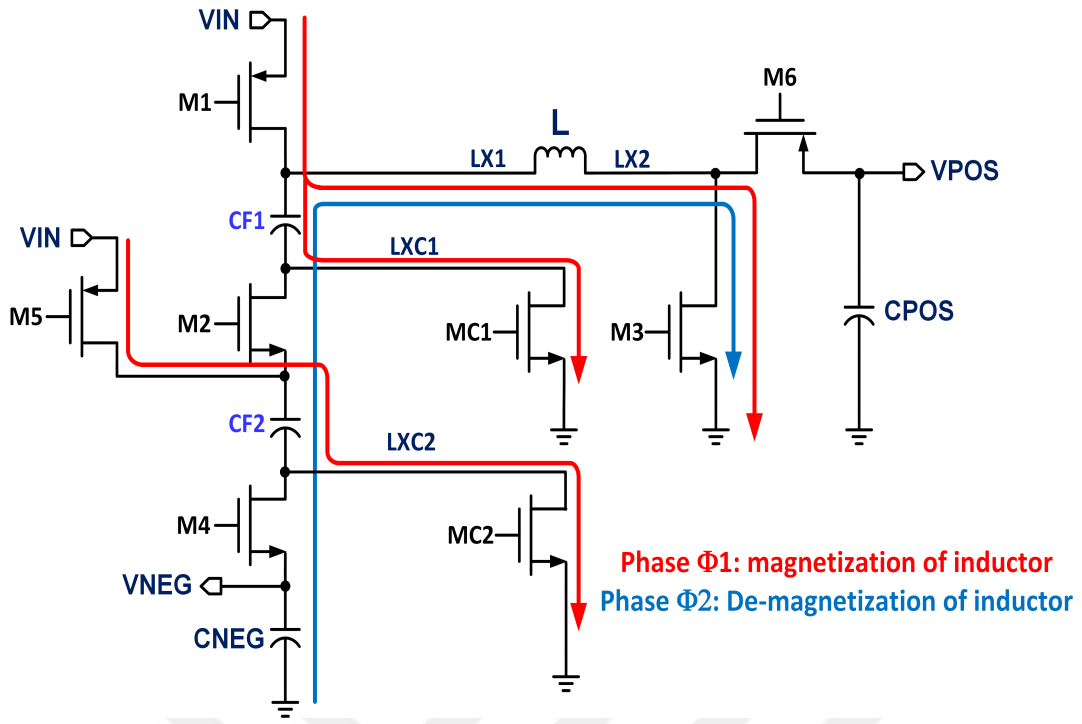

Figure 3.5 : Proposed SIDO converter, power flow in one switching cycle for negative output voltage generation.

The operation phases for the proposed converter are illustrated in Fig. 3.5. According to inductor volt-second balance and power balance equations, the voltage conversion ratio and the average inductor current of the converter can be obtained by Eq. 3.5 and Eq. 3.6, respectively.

$$\frac{Vout}{Vin} = -\frac{(2-D)}{(1-D)} \tag{3.5}$$

$$I_{L(avg)} = \frac{1}{(1-D)} I_{out} \tag{3.6}$$

Fig. 3.6 shows control signals as well as inductor voltage drop illustrations for the SIDO with two flying capacitor topology. By charging up the two flying capacitors approximately to V_{IN}, now the inductor observes a voltage drop of $V_{NEG}+2\cdot V_{IN}$ during the de-magnetization phase; consequently, the proposed SIDO converter achieves less average inductor current with less ripple and improved core losses. Eq. 3.5 also shows that for the same voltage conversion ratio, the SIDO 2FC topology can operate with lower duty cycles compared to 1FC and NFC topologies.

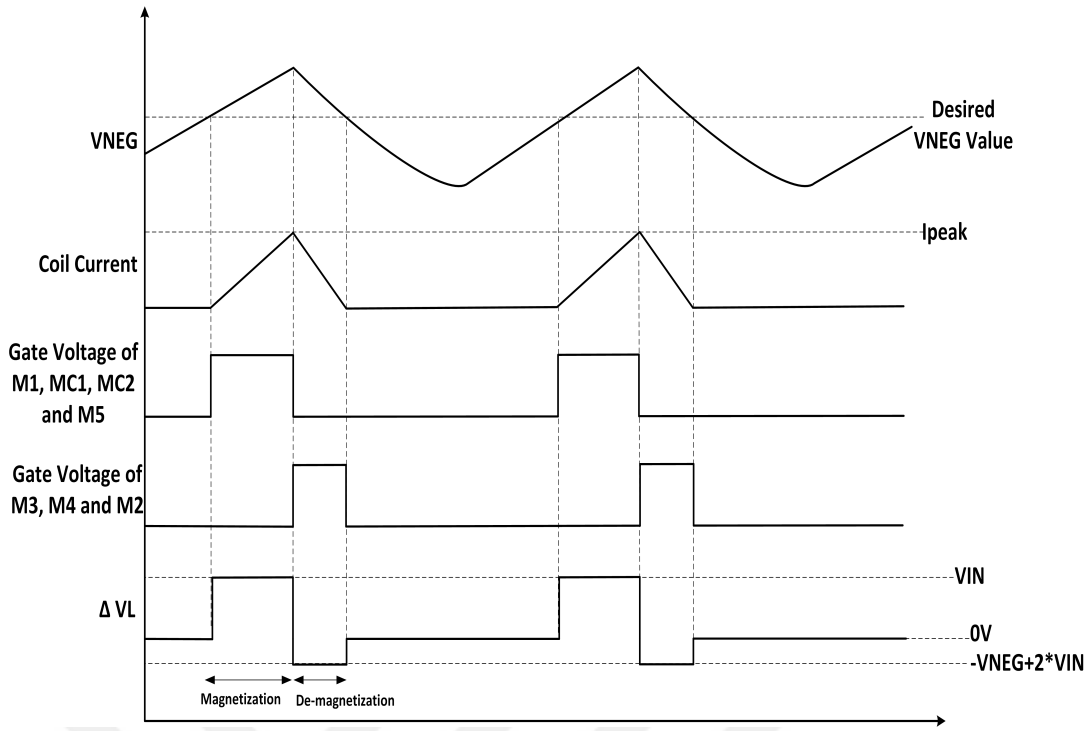

Figure 3.6 : Control Signals of SIDO with 2 Flying Capacitors.

Even though two more flying capacitors are required for the proposed topology, the area caused by the additional capacitors is insignificant compared to previous topologies, which require multiple inductors for generating separate outputs. The proposed method fits best for the high voltage SIDO converter applications. However, the proposed scheme can apply to any application, which includes negative output regulation that combines the need for a smaller coil and high efficiency.

Fig. 3.7 illustrates the voltage conversion ratio of each converter with respect to duty cycle. As seen in the figure, at the same duty cycle, the proposed 2FC topology can provide more negative voltage compared to conventional SIDO topology and SIDO topology with one flying capacitor. As of only comparing the voltage conversion ratio of the three converters, it can be said that the proposed SIDO converter can operate with a lower duty cycle, keeping the V_{OUT} and V_{IN} values same for each topology. This can be interpreted as a relaxation of system stability requirements and relaxed coil selection constraints.

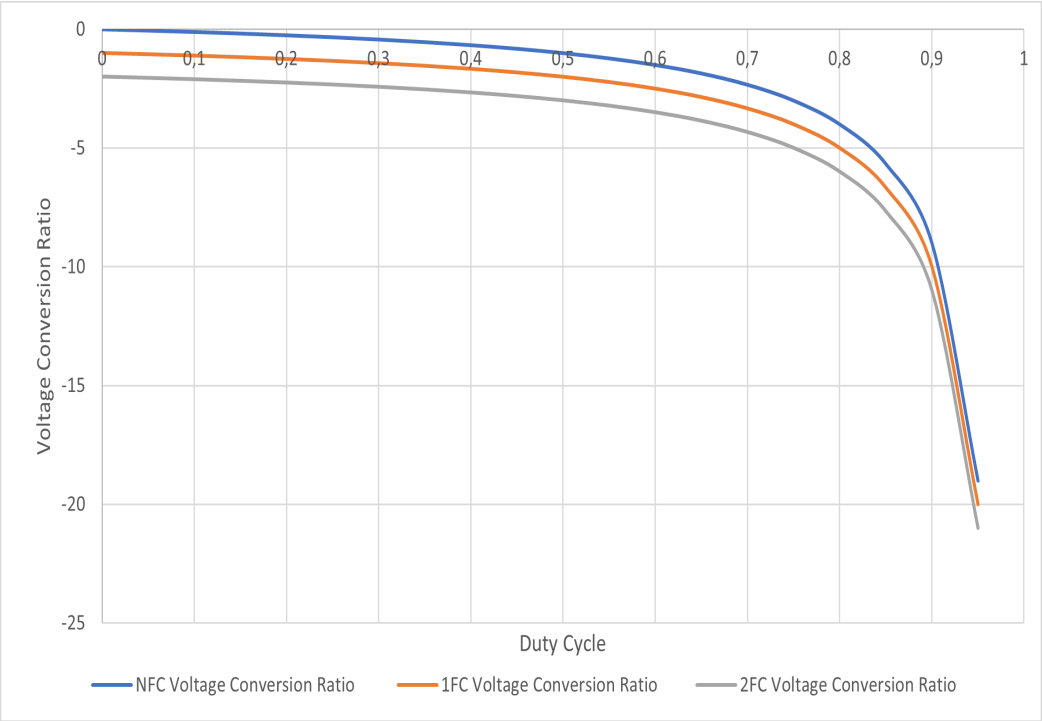

Figure 3.7 : Voltage conversion ratio of the topologies.

3.2 Positive Output Regulation

The mentioned improvements also apply to positive output voltage generation using a positive buck-boost switching sequence. In this section, conventional topology, the previous art which is the SIDO converter with one flying capacitor, and the proposed SIDO converter with two flying capacitors will be examined for an evaluated comparison between the topologies.

The slight modification should apply to conventional topology for a correct comparison between topologies. The SIDO converter with one flying capacitor and the proposed SIDO converter with two flying capacitors use a buck-boost switching sequence. This means, in the second phase, when the inductor current is decreasing, current flows through to V_{POS} output from the ground. However, in the current topology given by Fig. 3.1, in the second phase, current flows through to V_{POS} output from V_{IN}. The inductor voltage drop when the inductor current is decreasing will be V_{IN}-V_{POS} by using a boost sequence and the comparison will not be quantitatively identical.

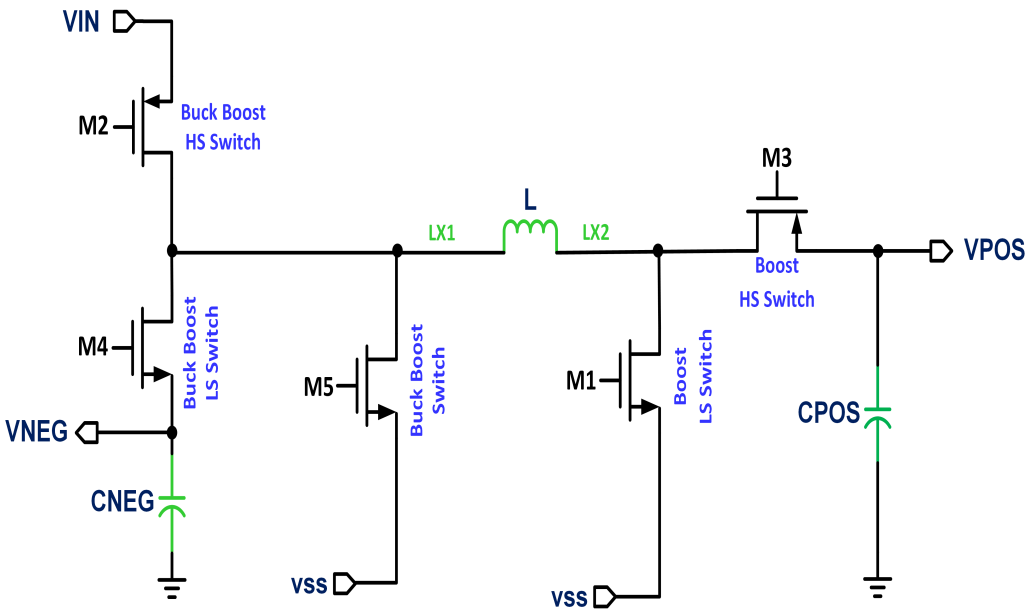

Figure 3.8 : Power stage of conventional SIDO topology for positive output voltage generation.

For positive output voltage generation, a conventional topology given by Fig. 3.1 adjusted such that a switch, M_5 is added between the inductor and the ground now inductor current can flow through to V_{POS} from the ground in the de-magnetization phase, as given with Fig. 3.8. This newly added switch does not affect negative output voltage generation, therefore M_5 switch can be biased in the cut-off region for this operation mode.

Referring to Fig. 3.8, to generate a positive output voltage, the switching sequence should be as follows; in the first phase, when magnetizing the inductor, M_1 and M_2 are ON, the inductor current is increasing with a slope of V_{IN}/L. In the second phase, when de-magnetizing the inductor, M_5 and M_3 are ON, the inductor current is decreasing with a slope of -V_{POS}/L. All the charge stored in the inductor is transferred to the output capacitor C_{POS}. Therefore, the positive output voltage can be generated by charging the output capacitor C_{POS} using a buck-boost sequence.

According to inductor volt-second balance and power balance equations, the converter voltage conversion ratio and average inductor current can be derived in terms of duty cycle in Eq 3.7 and in Eq 3.8, respectively.

$$\frac{Vout}{Vin} = \frac{D}{1-D} \tag{3.7}$$

$$I_{L(avg)} = \frac{1}{1-D} I_{out} \tag{3.8}$$

Similarly for the SIDO converter with one flying capacitor given with Fig. 3.2, the switching sequence is as follows; in the first phase, when magnetizing the inductor M_1, M_2 and M_C are ON. The inductor current is increasing with a slope of V_{IN}/L, meanwhile, the flying capacitor C_{F1} is being charged up to V_{IN}, as in the negative voltage operation. In the second phase, when de-magnetizing the inductor, M_C and M_3 are ON and inductor current flows through C_{POS}, thus generating positive output voltage. The inductor current is decreasing with a slope of $(V_{IN}\text{-}V_{POS})/L$. Referring to the circuit given by Fig. 3.2, the control signals of the SIDO with a flying capacitor for generating positive output voltage are given with Fig. 3.9.

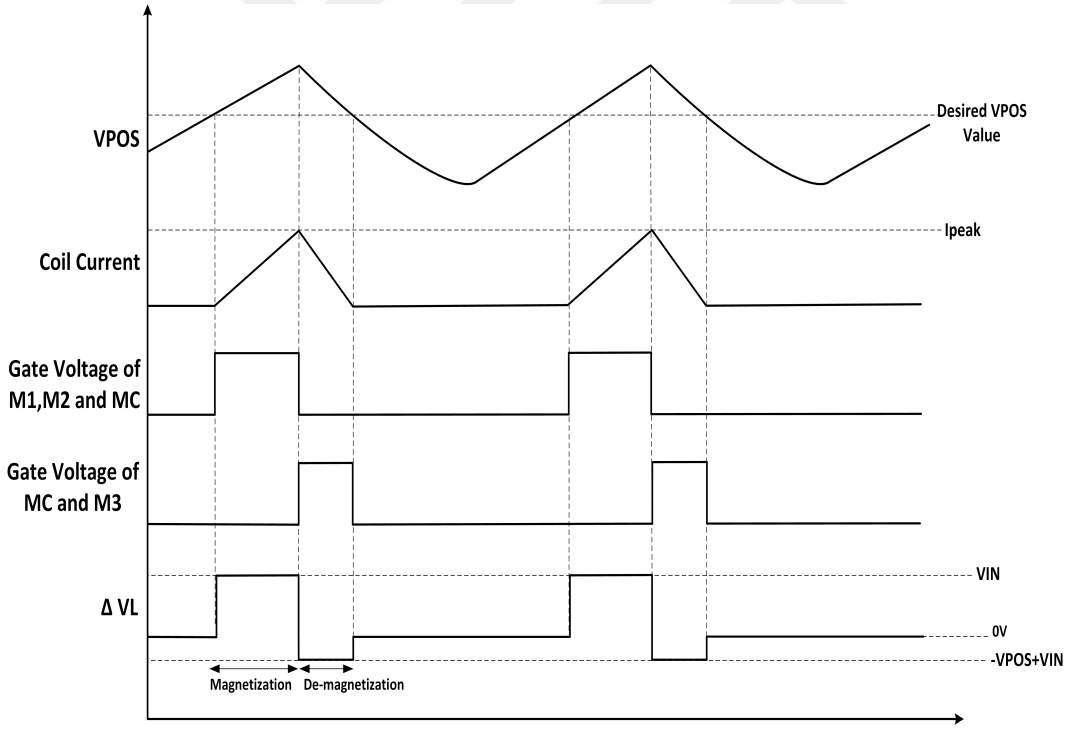

Figure 3.9 : Control Signals of SIDO with flying capacitors.

According to the inductor-volt second balance and power balance equations, the voltage conversion ratio and average inductor current can be obtained as given by Eq. 3.9 and Eq. 3.10, respectively.

$$\frac{Vout}{Vin} = \frac{1}{1-D} \tag{3.9}$$

$$I_{L(avg)} = \frac{1}{1-D} I_{out} \tag{3.10}$$

Referring to SIDO converter with two flying capacitors given in Fig. 3.4 to generate the positive output voltage V_{POS}, the switching sequence of the regulator is as follows: in the first phase, when magnetizing the inductor, M_1, M_3, M_5, M_{C1}, and M_{C2} are ON. The inductor current is increasing with a slope of V_{IN}/L. Meanwhile, the two flying capacitors are charged up to V_{IN}, similar to the negative voltage operation. In the second phase, when de-magnetizing the inductor, M_{C2}, M_2, and M_6 are ON. The inductor current is decreasing with a slope of $(2 \cdot V_{IN} - V_{POS})/L$. Thus, by using the 2FC topology, the voltage drop on the inductor is reduced by $2 \cdot V_{IN}$, with respect to the NFC topology. Fig. 3.10 presents the operation phases for the positive output voltage generation according to switch states. Fig. 3.11 illustrates the control signals of the switches as well as inductor voltage drop illustrations for the SIDO with two flying capacitor topology for positive output voltage generation.

According to inductor volt-second balance and power balance equations, the voltage conversion ratio and the average inductor current of the converter can be obtained by Eq. 3.11 and Eq. 3.12, respectively.

$$\frac{Vout}{Vin} = \frac{(2-D)}{(1-D)} \tag{3.11}$$

$$I_{L(avg)} = \frac{1}{(1-D)} I_{out} \tag{3.12}$$

Fig. 3.12 illustrates the voltage conversion ratio of each converter with respect to the duty cycle. Similar to V_{NEG} operation, comparing the topologies at the same duty cycle, the proposed 2FC topology is able to provide more positive voltage. As of only comparing the voltage conversion ratio of the three converters, it can be said that the proposed SIDO converter is able to operate with a lower duty cycle, keeping the V_{OUT}

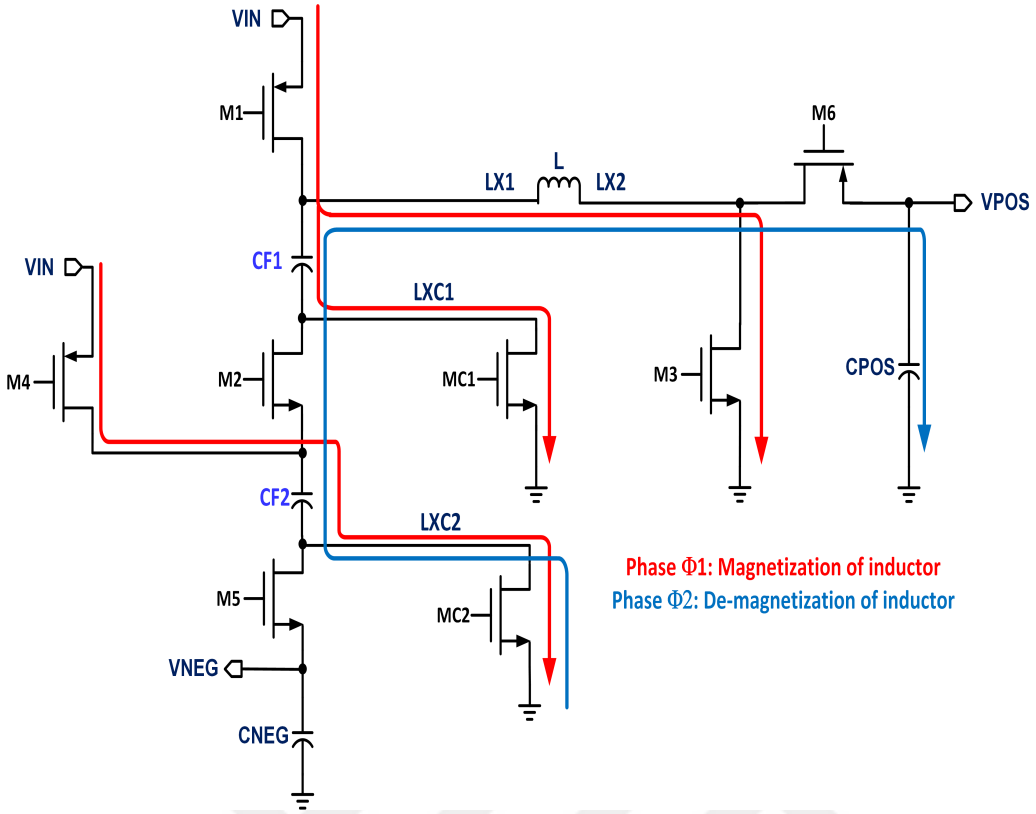

Figure 3.10 : Proposed SIDO converter, power flow in one switching cycle for positive output voltage generation

and V_{IN} values same for each topology. As a consequence, this leads to the relaxation of system stability requirements and relaxed coil selection constraints.

Even though the proposed method fits best for the high voltage SIDO converter applications, the proposed scheme can apply to any application which includes positive output regulation that combines the need for a smaller coil and high efficiency. Besides, the converter can comprise more positive output rails by using a single power inductor. Each positive output requires a respective boost high-side switching device(M_3 in Fig. 3.10). In the case of using more than one positive output, the boost high-side switching device should be formed by two transistors in the cascode configuration to avoid cross-conduction between multiple output rails [23].

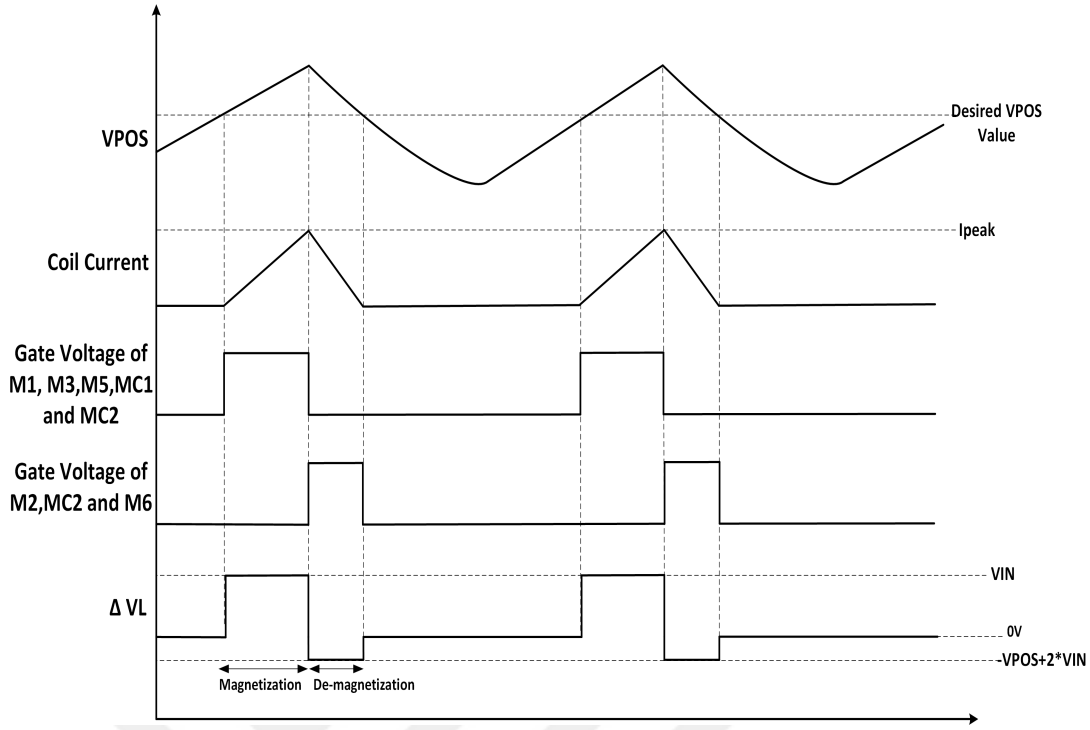

Figure 3.11 : Control Signals of SIDO with 2 Flying Capacitors.

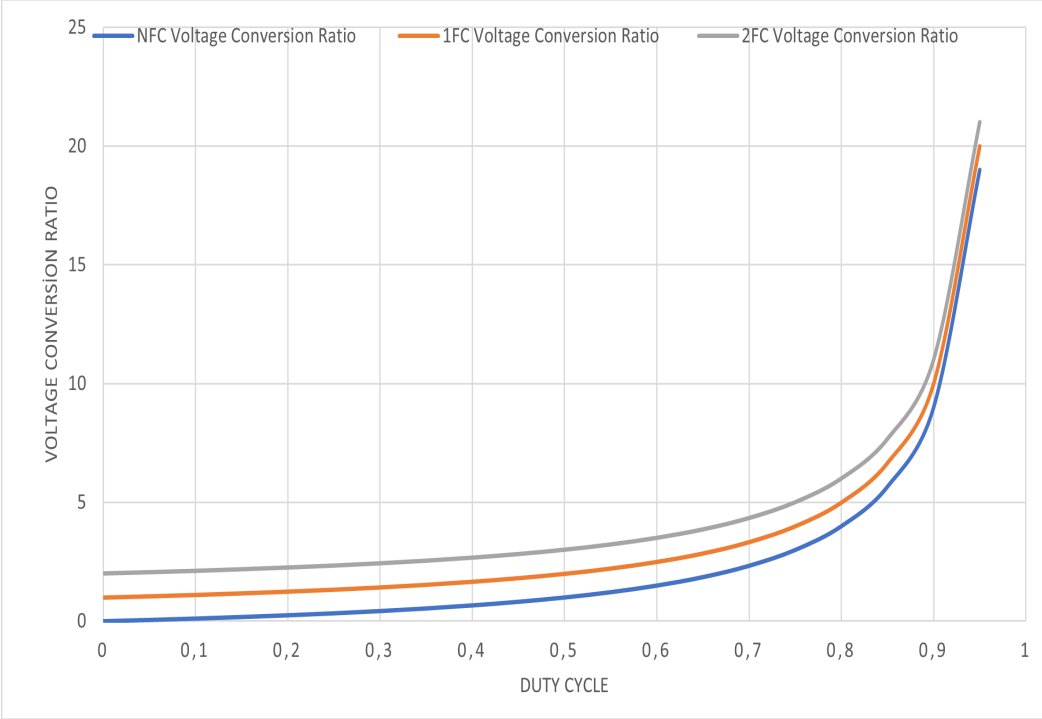

Figure 3.12 : Voltage conversion ratio of the topologies, VPOS operation.

4. DESIGN OF SINGLE-INDUCTOR DUAL OUTPUT VOLTAGE REGULATOR WITH MULTIPLE FLYING CAPACITORS

4.1 Design Structure

The power stage and the control scheme of the 2FC SIDO converter are given by Fig. 4.1. The switch elements in Fig. 4.1 are modeled with on-resistance given by Table. 4.1, with $10pF$ gate capacitance and body diodes. The on-resistances are optimized for the best power efficiency.

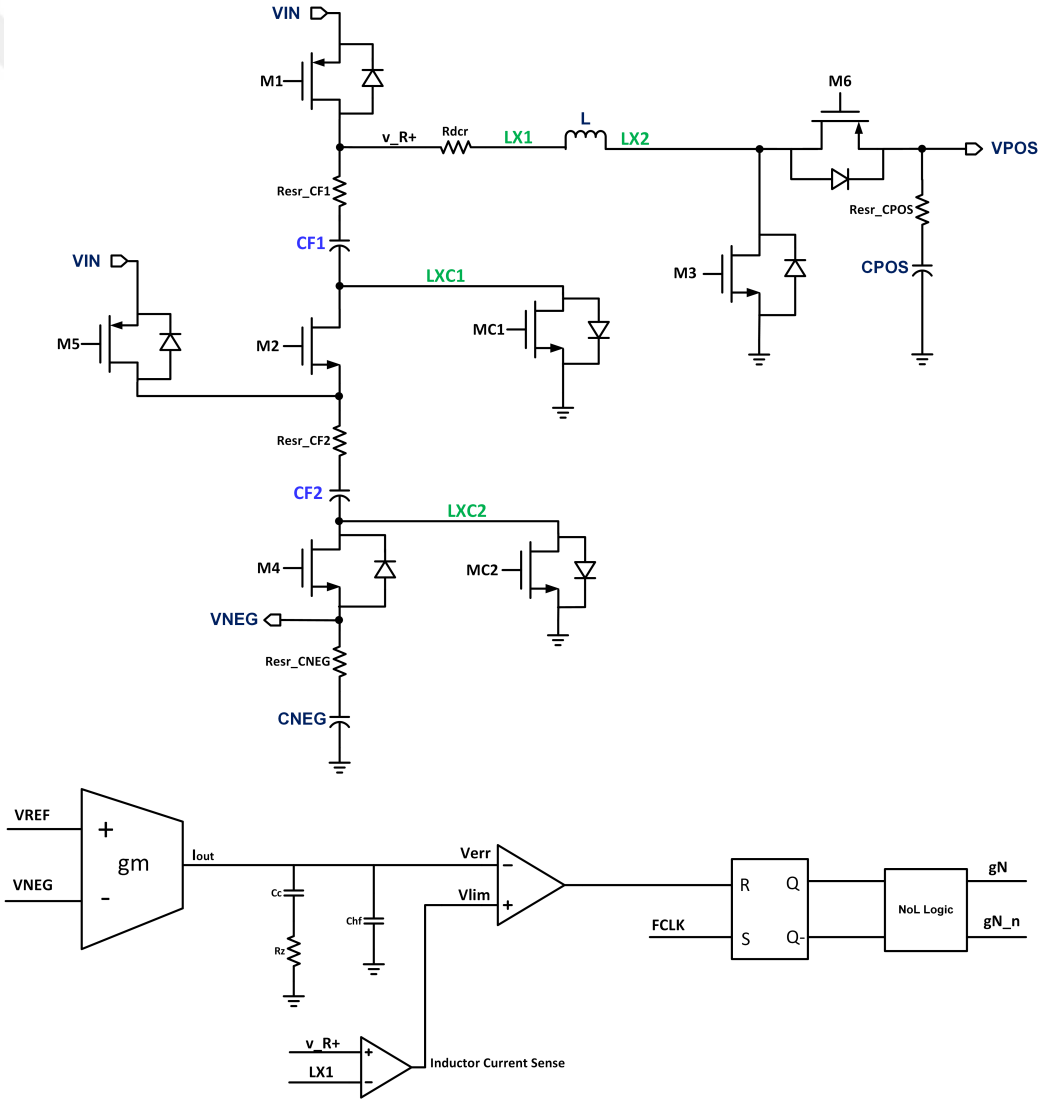

Figure 4.1 : Power stage and control loop of the 2FC SIDO converter.

Table 4.1 : On-Resistance of Switches.

Switch No	On-resistance
M_2, M_3, M_4, M_6	$50m\Omega$
M_1, M_{C1}, M_{C2}	$30m\Omega$

Non-overlap logic is introduced during the switching sequences to prevent shoot-through. The non-overlap scheme is given by Fig. 4.2. In this figure, Q and $Q-$ are outputs of the SR FF. The gate drive signals of the switches are represented as gN and $gN-$. The non-overlapping circuit generates two output signals at the same frequency but not in the same phase, owing to the delay elements. The delay elements, which are inverters in the scheme, insert a delay of 100ps between each sequence. During the non-overlapping time, none of the switches are conducting, and current flows through the body diode of the switches.

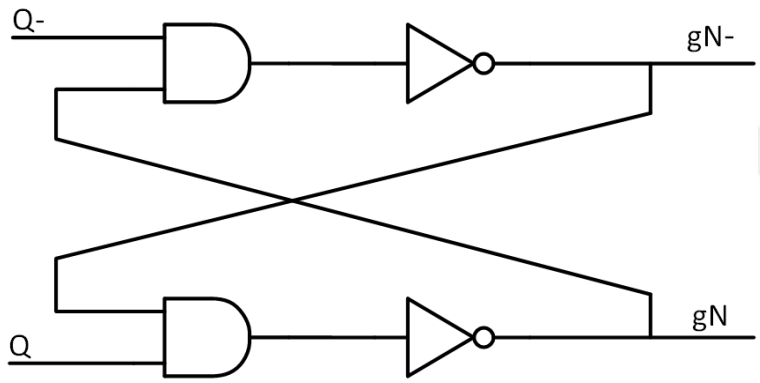

Figure 4.2 : Non-Overlap circuit.

4.2 Selection of Passive Components

The passive components used in the simulation setup are as follows: $L = 1\mu H$ with R_{DCR}=10mΩ (VCMT053T-1R0MN52M), C_{F1}=C_{F2}=1μF with R_{ESR}=6mΩ (GRM219B31E105KA88), C_{out}=30μF with R_{ESR}=3mΩ (GRM155R61A106ME18). The output capacitor should be selected with a low ESR since, in the first phase, the magnetization phase of the inductor, only the capacitor is sourcing the load.

The inductor part is selected from the manufacturer given in [35], which provides an applet for determining core material, as explained in the next chapter. The inductor is chosen such that it can carry the maximum inductor current in a sense that it does not

exceed saturation current and also has low DCR for efficiency concerns at high loads. Another selection criteria for the inductor is the inductor current ripple. There is a rule of thumb, generally, inductor current ripple should be kept less than %20 to %30 of the load current. Therefore, the inductor should be selected large enough to carry this ripple. In general, the inductance of the inductor can be determined based on the formula given by Eq. 4.1, which is derived from the rising slope of the inductor current and duty cycle.

$$L = \frac{D \cdot V_{IN}}{F_{sw} \cdot \Delta i_L} \tag{4.1}$$

The selection criteria for the flying capacitor value is as follows; using higher capacitance helps decrease conduction losses, increasing efficiency. On the other hand, higher capacitance decreases inductor current ripple since the voltage drop over the coil is reduced, which helps improve core loss. The power loss caused by the flying capacitor is inversely proportional to the capacitance. Based on this, both flying capacitors are selected C_{F1}=C_{F2}=1μF as the sweet spot. The loss caused by the flying capacitor can be formulated as given in Eq. 4.2. C_{FCAP} in the equation represents the capacitance of the flying capacitor used in the circuit.

$$P_{flyingcap} = \frac{1}{2} \frac{I^2 D^2}{F_{sw} C_{FCAP}} \tag{4.2}$$

The capacitor part number was selected from the manufacturer in [36]. On the manufacturer page, the frequency-resistance curve is obtained. The curve shows 6$m\Omega$ ESR at the operating frequency given by Fig. 4.3, which is used for the flying capacitors C_{F1} and C_{F2} in the design. Considering the selected flying capacitor part dimensions for this work, the area occupied by the introduced capacitors is smaller than one inductor area. Hence, the proposed topology does not show area drawbacks by adding the flying capacitors.

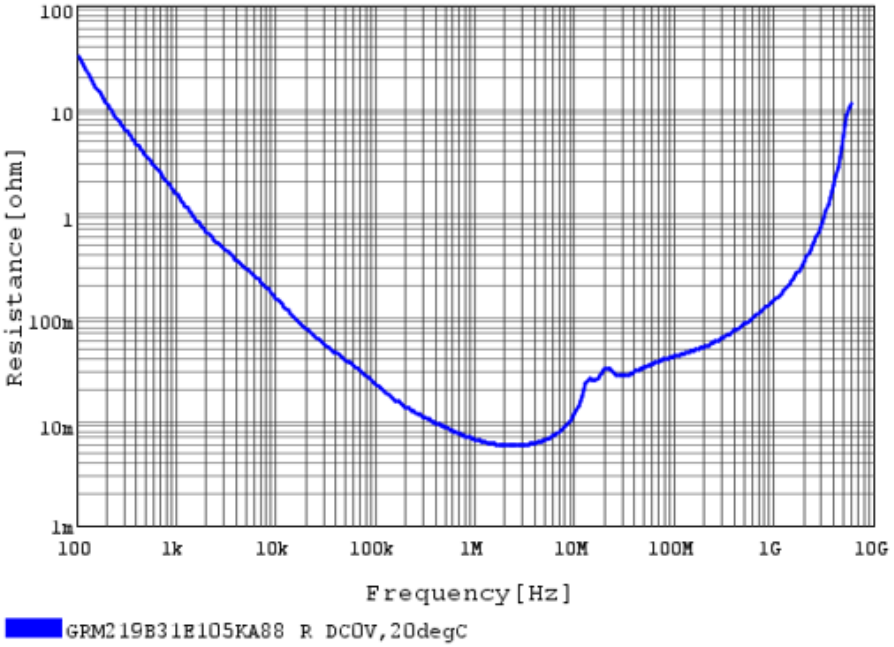

Figure 4.3 : Resistance - Frequency curve of the flying capacitors [36].

4.3 Control Loop Design

The control method used in this work is continuous conduction mode (CCM) with peak current control at 3MHz system clock frequency. The CCM operation is chosen in this work because of the output power limitations of DCM operation. The work focuses on high loads according to specifications given by Table 5.1, intending to address mobile AMOLED, PMOLED, and Light Sensor battery-powered applications. DCM operation should be avoided at higher loads because the peak current in DCM operation is higher than that in CCM with the same output power level. Consequently, the current stress on the power switches and the inductor is also higher which is not a desirable situation.

For the control method, the operating principle is as follows; with the rising edge of the system clock *CLK*, the first phase switch control voltage *gN* is set to high, and the inductor current I_L starts to increase. When V_{LIM} (the inductor current sense signal) hits V_{err}, the second phase starts, and the inductor current starts to decrease. In this case, V_{err} sets the peak inductor current. Once the system clock toggles to high again, the next switching cycle starts. ΔV_{CF1} and ΔV_{CF2} demonstrate the voltage drop on the

first flying capacitor C_{F1}, and the second flying capacitor C_{F2} which are charged to V_{IN} during the first phase. ΔB shows the estimated magnetic flux density obtained with the model proposed in [37] to calculate core losses. V_{NEG} is the output voltage settling at an average target value of -10V. The illustration of the control signals is given in Fig. 4.4.

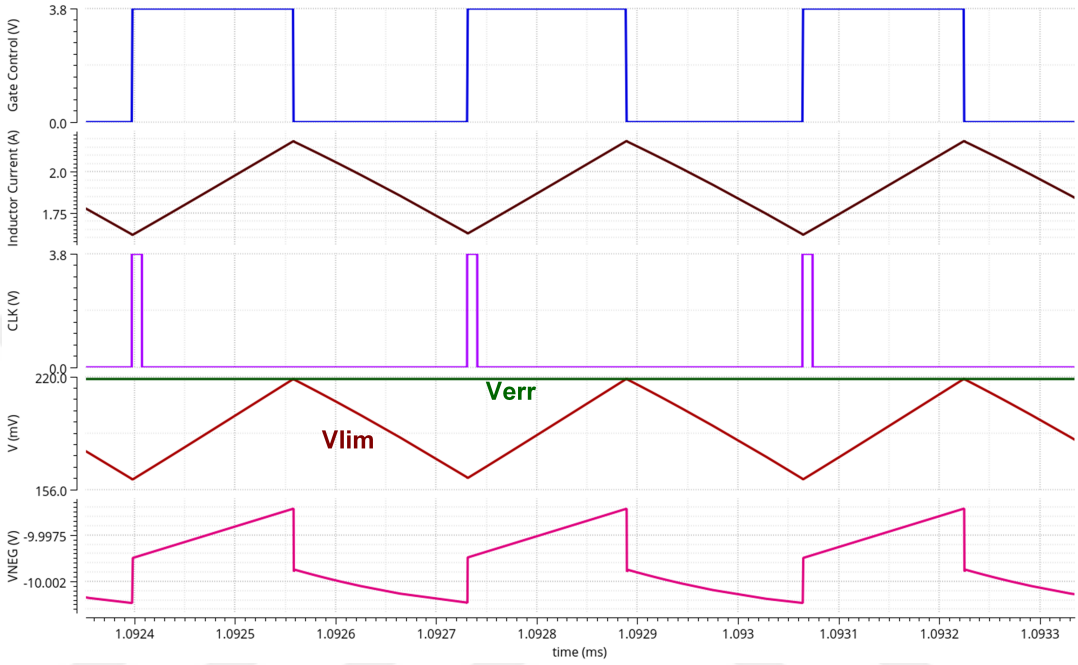

Figure 4.4 : Control loop signals.

The stability of the regulator is achieved with proper compensation capacitors and resistor. The structure is an example of a Type II compensator with OTA(Operational Transconductance Amplifier). The corner frequency of the converter is given by Eq. 4.3. The corner frequency should be chosen to be less than the switching frequency so that the output filtering essentially passes only the DC components, not the switching harmonics.

$$f_0 = \frac{1}{2\pi\sqrt{L_{ind}C_{out}}} \tag{4.3}$$

The zero frequency contributed by the resistor is given by Eq. 4.4. According to chosen output capacitor and inductor values based on the requirements, the resultant of the

Eq. 4.3 is equalized to Eq. 4.4, in order to find compensation capacitor and resistor.

$$f_{zea} = \frac{1}{2\pi R_c C_c} \tag{4.4}$$

According to formulas given by Eq. 4.3 and Eq. 4.4, control loop parameters are obtained as in Table 4.2. The transconductance of the OTA chosen as 10mS to ensure stable operation over V_{IN} and I_{LOAD} range.

Table 4.2 : Control Loop Design Parameters.

Parameter	Value
R_c	1.368Ω
C_c	4 μF
C_{hf}	1 μF
g_m	10 mS

4.4 Core Loss Estimation

In this work, the core loss estimation method proposed in [37] is used, in order to maintain the integrity of the work and present more accurate efficieny data. The proposed method is modeling the B-H loop to determine the energy loss per unit volume of a core in one switching cycle. The typical B-H loop of the magnetic material in one switching cycle is illustrated in Fig. 4.5. The area enclosed by the B-H loop is proportional to $\partial B/\partial t$. As a result, a higher core loss can be observed when $\partial B/\partial t$ is increasing.

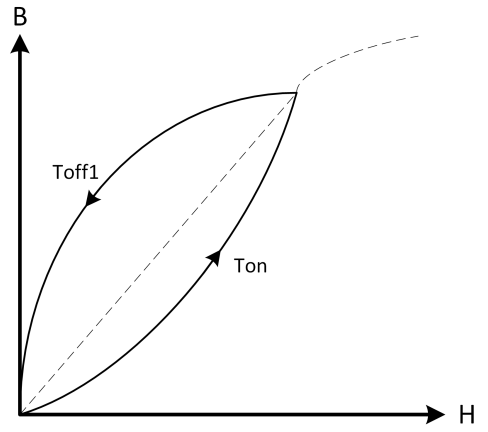

Figure 4.5 : Typical B-H loop of the magnetic material in switching converters [37].

According to that information, [37] proposes the formula that is given by Eq. 4.5 to obtain core loss. The formula is embedded into Cadence Analog Design Environment in this thesis work.

$$Pcore = \alpha V[(\frac{\Delta B^m}{(2Ton)^n})\frac{Ton}{Ts} + (\frac{\Delta B^m}{(2Toff1)^n})\frac{Toff1}{Ts}] \tag{4.5}$$

The equation coefficients are defined as follows; T_{on} is the internal where inductor current is increasing, and flux density B is increasing. T_{on} is the internal where inductor current is decreasing, and flux density B is decreasing. T_{on} is the zero-voltage time, the interval to distinguish DCM operation, where inductor current is zero, and flux density is not changing. T_s is the switching period, which is the sum of the mentioned time periods above. V is the volume of the core material.

α, m and n are constants for each core material, and they can be obtained in the lab environment by subjecting the core material to a square wave and then corresponding curve fitting. In this work, the core loss material coefficient was obtained with the applet [38] provided by the manufacturer for the selected inductor with the help of the simulator environment. The equation given by Eq. 4.5 is derived from the Steinmetz equation, given by Eq. 2.13.

The improvement in this modeling is that the equation proposed in Eq. 4.5 also takes into consideration of the converter operation mode, whether the converter operates in CCM or DCM. Therefore, the equation reflects the core loss difference caused by the different duty cycles for each switching, or in DCM operation, the core loss difference caused by the different time-off duration. The magnetic flux density change and the inductor voltage waveforms are depicted in Fig. 4.6.

After deriving the core loss calculation formula, the accurate modeling of the inductor is needed to obtain time-domain flux density data, since it reflects the magnetic behavior of the inductor. The inductor model should include flux density as one of its variables so that the time domain flux density data can be obtained through simulations [37]. The proposed inductor model is given by Fig. 4.7.

A voltage-controlled current source is placed in the model with the transconductance of 1mS, and the voltage control inputs are the inductor terminal voltages. The capacitance of the capacitor in the model is defined in Eq. 4.6 [37], where N is the number

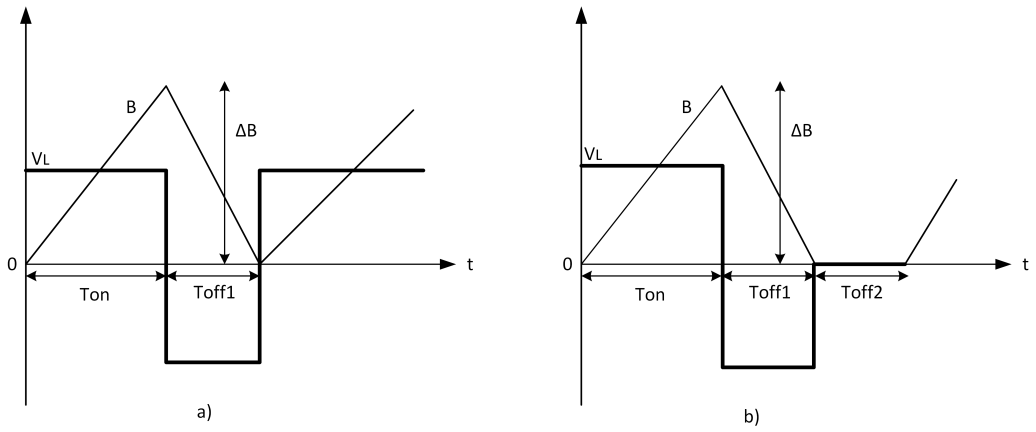

Figure 4.6 : Inductor voltage and flux density waveform in switching converters a) CCM operation b) DCM operation [37].

of turns of the winding and A is the core area. The capacitor helps to mimic the magnetic flux density. By charging and discharging that capacitor with the current that is generated proportional to inductor voltage, the time domain magnetic flux density can be obtained.

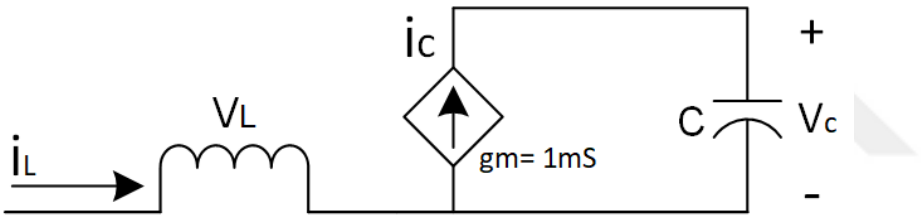

Figure 4.7 : Proposed inductor model to obtain magnetic flux density [37].

$$i_c = V_L, and \qquad C = NA \tag{4.6}$$

$$v_c = \frac{1}{C}\int i_c dt = \frac{1}{NA}\int v_L dt = B \tag{4.7}$$

The core material parameters used in this work according to the selected inductor are presented in Table. 4.3.

The mathematical expression of the flux density is given by Eq. 4.7 [37]. The equation derives the magnetic flux density of the core in terms of inductor voltage, number of turns, and the core area. The equation means the voltage over the capacitor v_c in the

Table 4.3 : Core Material Parameters.

Parameter	Value	Unit
Number of turns	50	
Core volume	85.83	mm^3
Core area	28.61	mm^2
α	0.75	
n	2.32	
m	2.42	

model given by Fig. 4.7 is numerically equal to the flux density of the core in Tesla. In the model given by Fig. 4.7 used in the simulations, the magnetic flux density is obtained with the help of the model in the time domain for each switching cycle.

The thesis work uses constant frequency operation; the variables ΔB, T_s, t_{on}, t_{off} can be read out from the simulation or directly from the flux density waveform that is obtained with the inductor model. Since the core material is already obtained with the applet and the dimensions of the inductor are already present in the manufacturer site, all the parameters are embedded into the formula then the core loss of the inductor is obtained.

The proposed method mimics the behavior of magnetic flux change of the inductor by using the core parameters and the coil properties. As a result of the proposed core loss formula given by Eq. 4.5, a numerical result is obtained for the core loss. In the efficiency calculations, the resultant is added to the input power for the correct estimation of the efficiency. The reason is that the modeling does not consume any power, and does not take any current from the circuit in case of the simulation purposes. Since in real life, this will contribute directly to input current, the estimated core loss is included in input power for correct estimation of efficiency.

Several works are presented in the literature for the estimation of core loss in power switching converters, such as [39,40]. The work presented in [39] proposes an inductor model for better core loss estimation for power converters, which also identifies the hysteresis loss part. The core loss model in [37] is chosen for this work because it enables the mathematical calculation of the core loss based on the proper inductor model for deriving the magnetic flux that can be embedded into any simulation environment.

5. SIMULATION RESULTS

To evaluate the mentioned topologies, conventional SIDO topology, SIDO converter with one flying capacitor topology and proposed topology with two flying capacitors designs are modeled and simulated in Cadence Virtuoso Analog Design Environment. Simulation test benches are given in Fig. A.2 for NFC topology, in Fig. A.3 for 1FC topology, and in Fig. A.4 for 2FC topology. The expressions to obtain power loss contributors and other necessary expressions used in this work are presented in Fig. A.1.

An example of target specifications for the converter, intending to address mobile AMOLED, PMOLED, and Light Sensor battery-powered applications are given by Table 5.1. The batteries degrade some over time based on usage. Considering this, the input supply voltage V_{IN}, is determined as a wide range to ensure the system still provides stable output voltage.

Table 5.1 : System Specifications.

Parameter	Value
V_{IN}	2.5V / 3.8V / 4.9V
V_{NEG}	-10V
V_{POS}	8V
F_{CLK}	3MHz
I_{Load}	0.5A / 1A / 2

5.1 Negative Output Voltage Regulation

Fig. 5.1 shows the simulated waveform of conventional topology at a load current of 1A when V_{IN} is 3.8V. The first issue related to this design is, when the inductor is discharging, the inductor observes a voltage drop close to V_{NEG}. For significantly low values of the output voltage, such as -10V to -15V, this voltage drop will result in a higher inductor current ripple, since the ripple is proportional to a voltage drop of the inductor. The high inductor ripple comes with efficiency drawbacks and other system issues. The higher $\partial i/\partial t$ during inductor current discharge results in increased

recovery loss for the MOSFET switches and increased EMI on the system.

Given by the topology in Fig. 3.1, the negative rail switch M_4, observes V_{DS} voltage of $V_{IN} + |V_{NEG}|$ during inductor discharging, which can easily exceed process limitations in the application. Reducing the voltage drop on the negative rail switch helps eliminate the need for cascode devices which leads to increased power efficiency and silicon area. The other benefit of reducing the voltage drop of the negative switch is reduced body diode conduction. As shown in Fig. 5.1, the V_{DS} of the negative rail switch device is around 13.5V, and already put high voltage constraints on the switch. This amount of voltage is not practical in terms of safe operating area constraints.

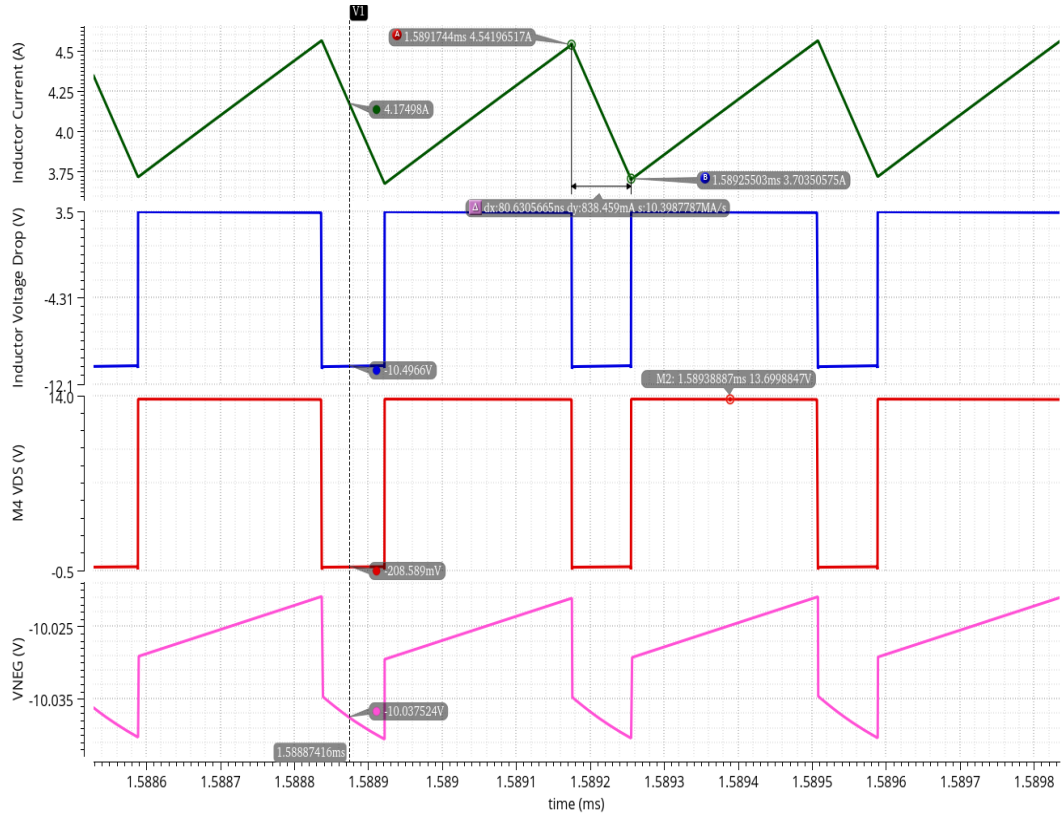

Figure 5.1 : Conventional SIDO topology, I_L, ΔV_L, V_{DS} of M_4 and output voltage V_{NEG} presented respectively.

The conventional SIDO topology is improved by adding a flying capacitor into the circuitry, as presented in the literature [14]. Fig. 5.2 shows the simulated waveform of SIDO with one flying capacitor topology at a load current of 1A when V_{IN} is 3.8V. The improvement is visible in the voltage drop of the inductor. Now, the inductor observes less voltage by the amount of V_{IN}. This results in a decreased inductor current

ripple. On the same output voltage and the output load, the inductor current ripple of the conventional topology is 840mA while for the SIDO converter with one flying capacitor, the ripple is 787mA. This improvement translates as reduced core losses in the system and positively impacts efficiency.

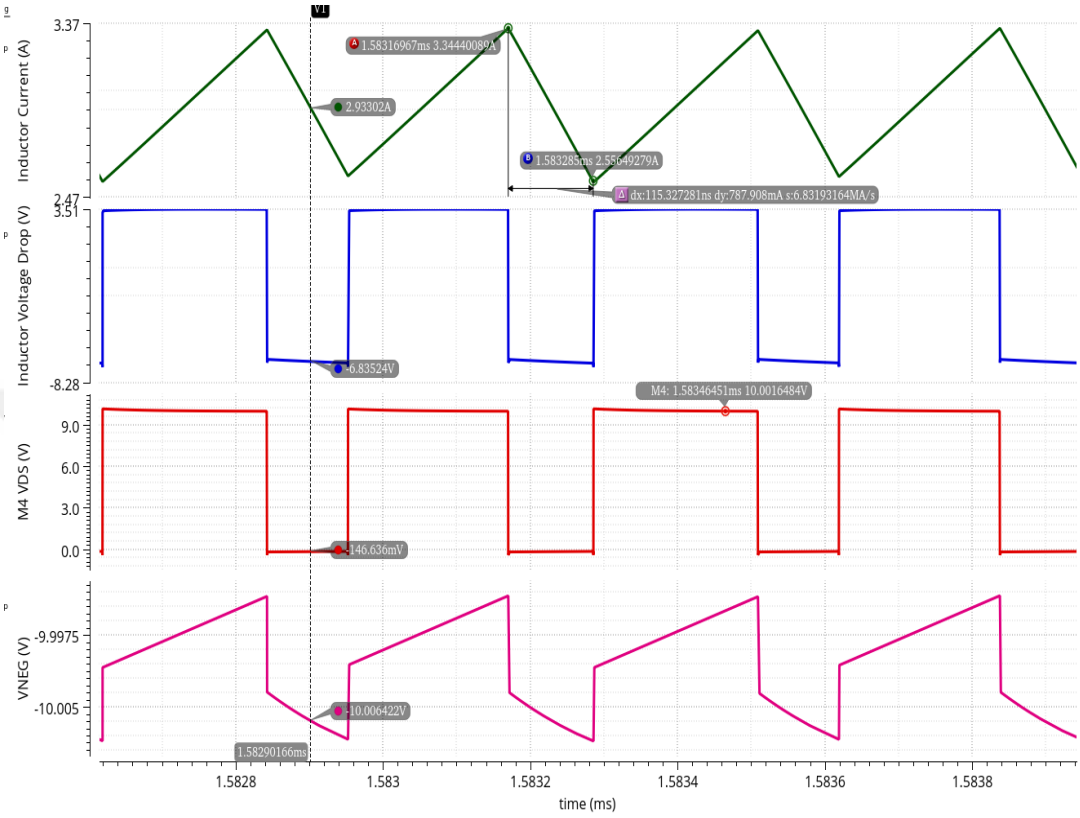

Figure 5.2 : SIDO with one flying capacitor, I_L, ΔV_L, V_{DS} of M_4 and output voltage V_{NEG} presented respectively.

Buck-boost converters store energy in the first phase when the inductor is charging and, release current to output only when the inductor current is discharging. The de-magnetization phase of the inductor is the time window that the inductor is supplying current to V_{NEG} output. It is desired to have a longer time window to support load current at negative output rail. Thus, as another improvement, the time duration inductor is supplying negative current is increased compared to the conventional topology. Also, by adding a flying capacitor, the inductor discharge slope decreased under the same design variables. This helps enabling the use of smaller coils and increases power efficiency.

Another improvement related to this topology is that decreased voltage drop of the negative rail switch, M_4. During the magnetization phase, now the negative rail switch observes $|V_{NEG}|$ which is an improvement close to V_{IN} compared to the previous value, $V_{IN}+|V_{NEG}|$. This improvement relaxes the switch and prevents possible breakdown issues.

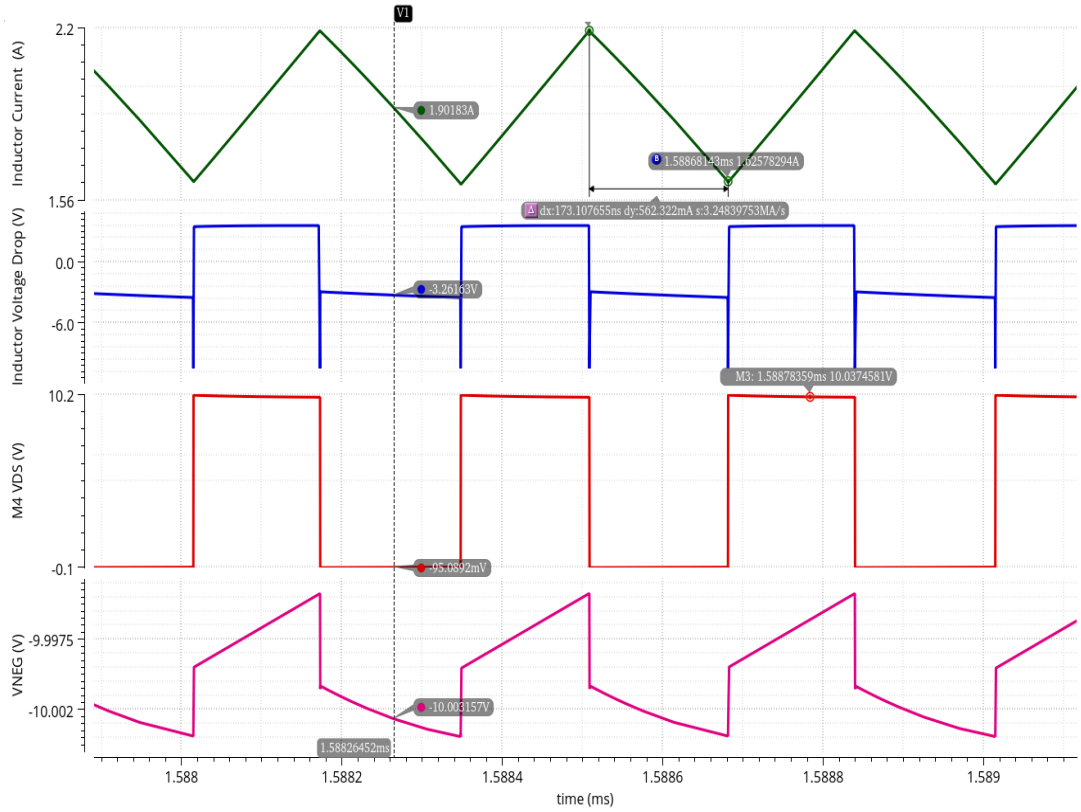

Figure 5.3 : SIDO with two flying capacitors, I_L, ΔV_L, V_{DS} of M_4 and output voltage V_{NEG} presented respectively.

Fig. 5.3 shows the simulated waveform of the proposed SIDO converter with two flying capacitors, at a load current of 1A when V_{IN} is 3.8V. The proposed topology uses the advantage of having two flying capacitors on the same path and proves improvements in many aspects. The idea of adding a flying capacitor into the circuit was to relax coil constraints and increase efficiency. The proposed topology carries a step forward in this advantage by using two flying capacitors on the same path. The improvement in the voltage drop of the inductor is visible. Now, the inductor observes less voltage by the amount of $2{\cdot}V_{IN}$ compared to conventional topology and less voltage close to

V_{IN} compared to SIDO with one flying capacitor topology. As a result of decreasing voltage drop over the inductor, the inductor current ripple is reduced to 562mA.

Moreover, Fig. 5.3 shows that the inductor current discharging slope decreased and the time window supplying negative current to the output increased, compared to the conventional topology as shown in Fig. 5.2 and SIDO with one flying capacitor topology as shown in Fig. 5.1. As stated earlier, the higher inductor discharge slope is not desirable since fast discharging may lead to increased recovery loss for the switches and increased EMI on the system.

The other critical improvement is decreasing the inductor peak current. The maximum current of the inductor is generally a design concern because of the saturation current defined in the inductor datasheet provided by the manufacturers. The proposed topology reduces the maximum inductor current and shows another design flexibility. This can be beneficial if the inductor has a risk of entering a saturation region. In addition to that, mentioned improvement is also beneficial due to decreasing current stress on the switches and preventing excessive heating in the system.

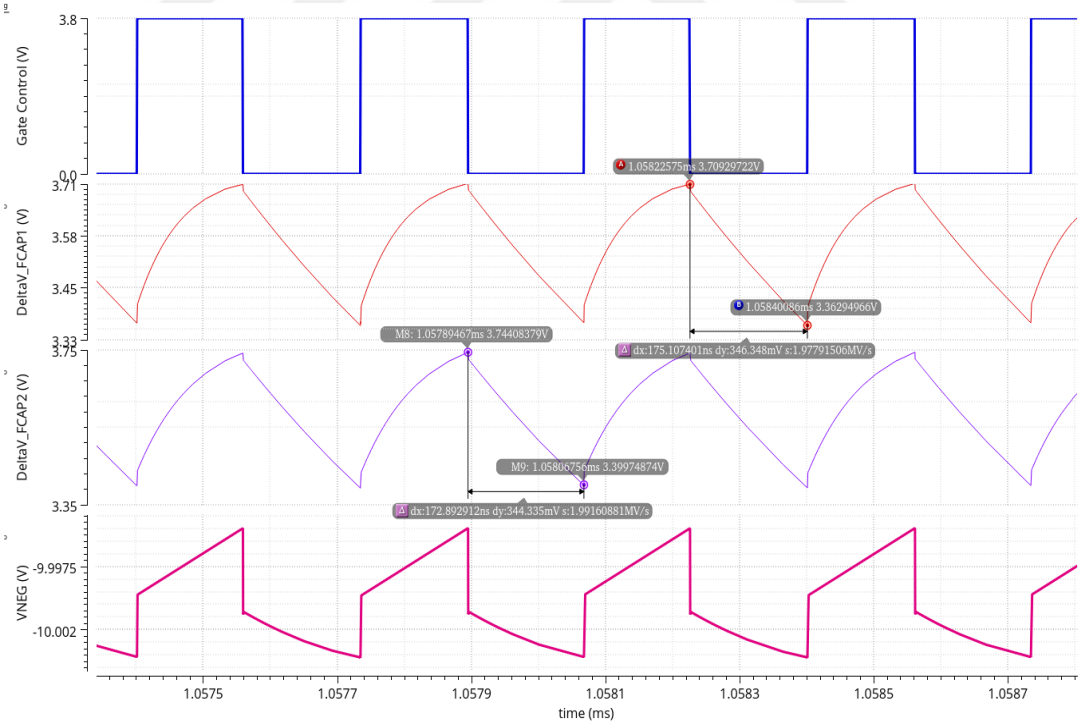

Figure 5.4 : Flying capacitor voltages of the proposed topology.

The voltage drop of the flying capacitors is given by Fig. 5.4. The flying capacitors are being charged close to V_{IN} when the inductor is magnetized. There are conduction losses caused by the switches; therefore, they can not completely charge to V_{IN}. As seen in Fig. 5.4, they are not completely discharging; thus, they still have some voltage stored while the inductor current is discharging. This helps the inductor voltage drop to be more positive since two flying capacitors keep the voltage during the de-magnetization phase. As a consequence, this relaxes coil constraints and voltage stress on the switches.

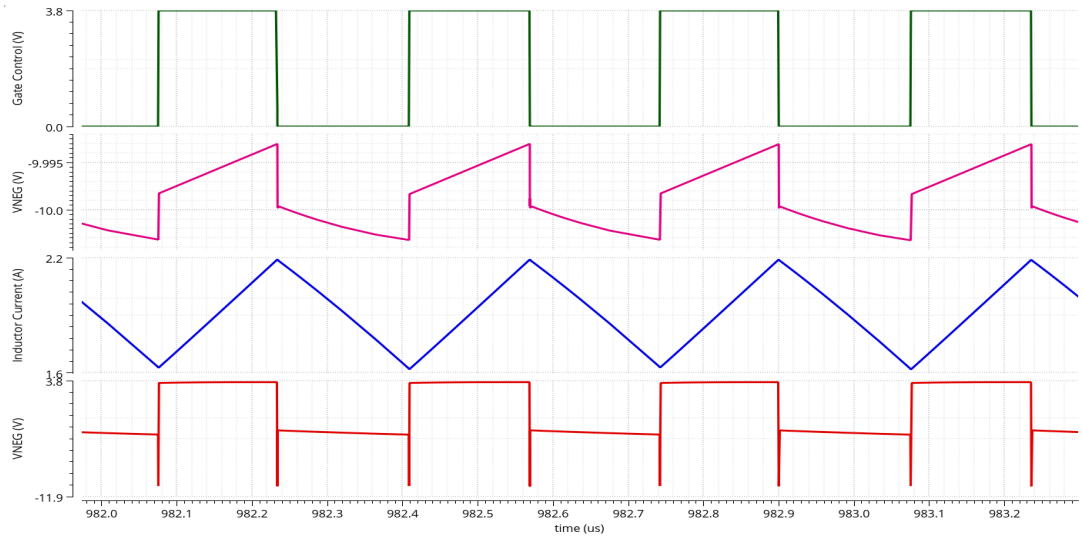

Figure 5.5 : Body diode conduction.

As seen in Fig. 5.5, in the ΔV_L signal, negative peaks are visible between switching sequences. This is because of a non-overlapping scheme that is introduced in the circuit. During this time, the inductor current decreases with a very high slope and body diode of the switches conduct, therefore, this sudden change results in an excessive change in voltage over the inductor, which complies with the formula given by Eq. 2.3. During the non-overlapping time, the inductor current flows through the body diode of the switches. Since the negative peaks last very short, in the order of 100ps, this issue has no significant effect on the system performance and this behavior can be witnessed in real-life applications.

Since designs are simulated with different load conditions, Fig. 5.6, Fig. 5.7 and Fig. 5.8 show the steady state operation of the proposed topology with 500mA, 1A

and 2A, respectively. All of the waveforms show 2FC SIDO converter settles desired V_{NEG} voltage and is able to provide stable output over a wide load current range.

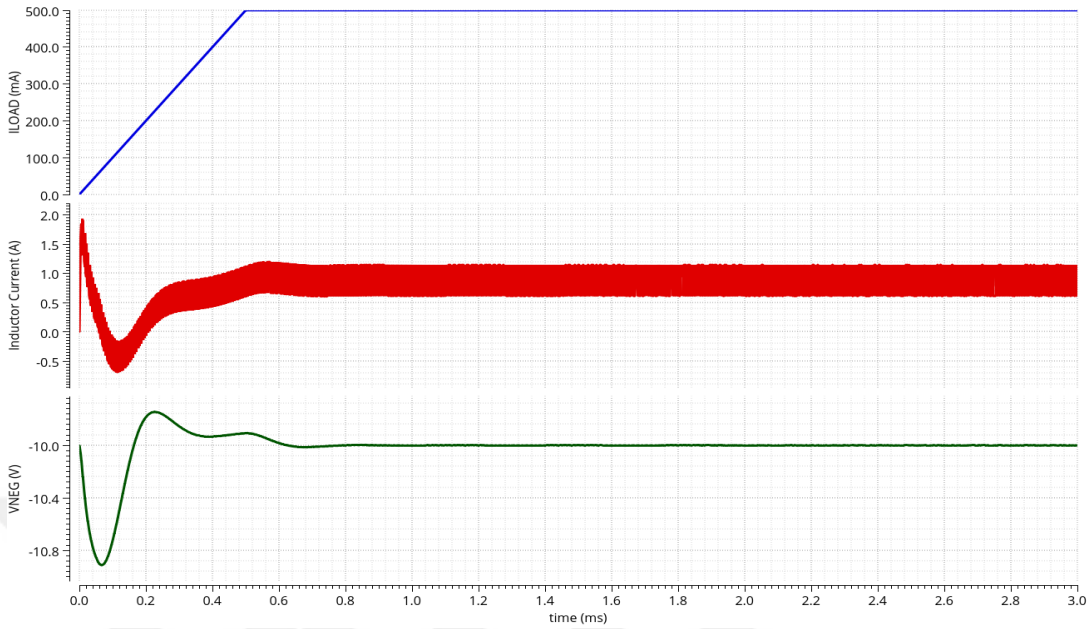

Figure 5.6 : Simulated waveform of I_{LOAD}, I_L and V_{NEG} in the steady state at a load current of 500mA when V_{IN} = 3.8V.

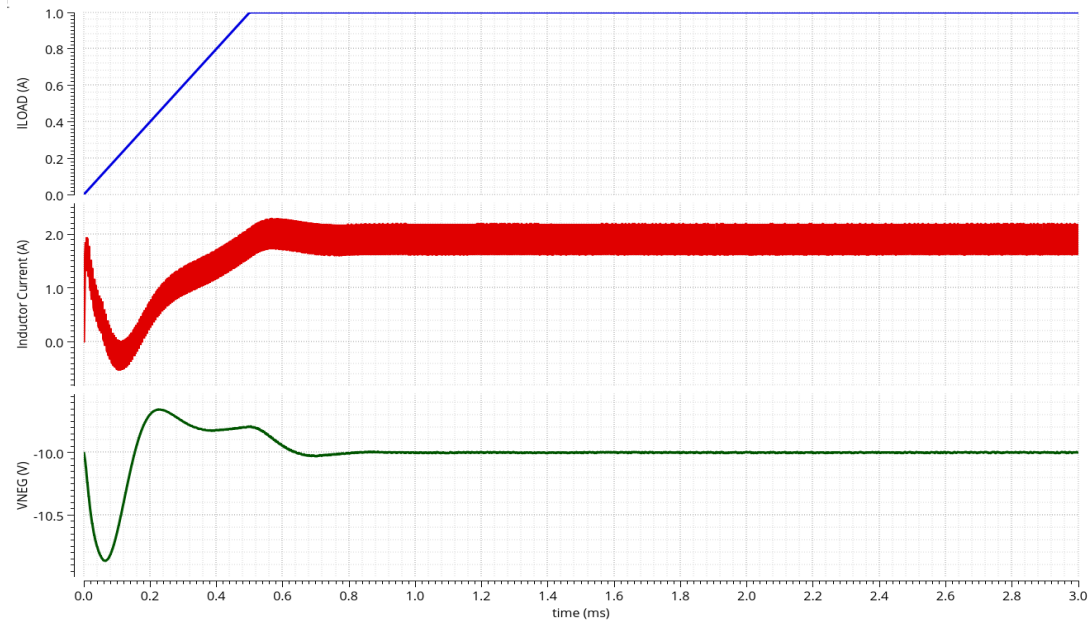

Figure 5.7 : Simulated waveform of I_{LOAD}, I_L and V_{NEG} in the steady state at a load current of 1A when V_{IN} = 3.8V.

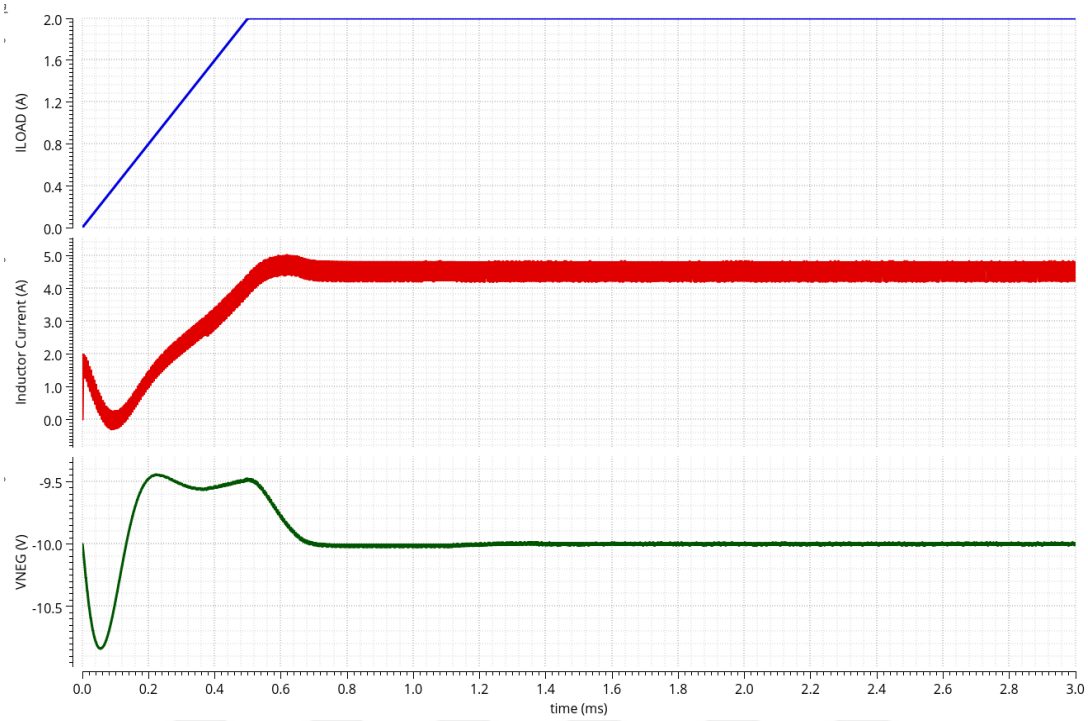

Figure 5.8 : Simulated waveform of I_{LOAD}, I_L and V_{NEG} in the steady state at a load current of 2A when V_{IN} = 3.8V.

Fig. 5.9 shows switch currents for the proposed topology when the converter reaches a steady state. The waveform proves the functionality of the non-overlapping scheme, no excessive current is observed in any of the switches in the path, and non-overlapping time is enough to balance the risk of shoot-through and the body diode conduction losses.

The charging and discharging phases are also illustrated, according to the operation phases of the 2FC converter given by Fig. 3.5. Once the gate control signal goes high, M_1, M_{C1}, M_{C2}, M_5 and M_3 start to conduct. M_1, M_{C1}, M_{C2} currents increase through capacitive current. Therefore, they show exponential behavior. Once the gate control signal goes low, M_4 starts to conduct and discharges the output capacitor C_{NEG} to generate the negative output voltage.

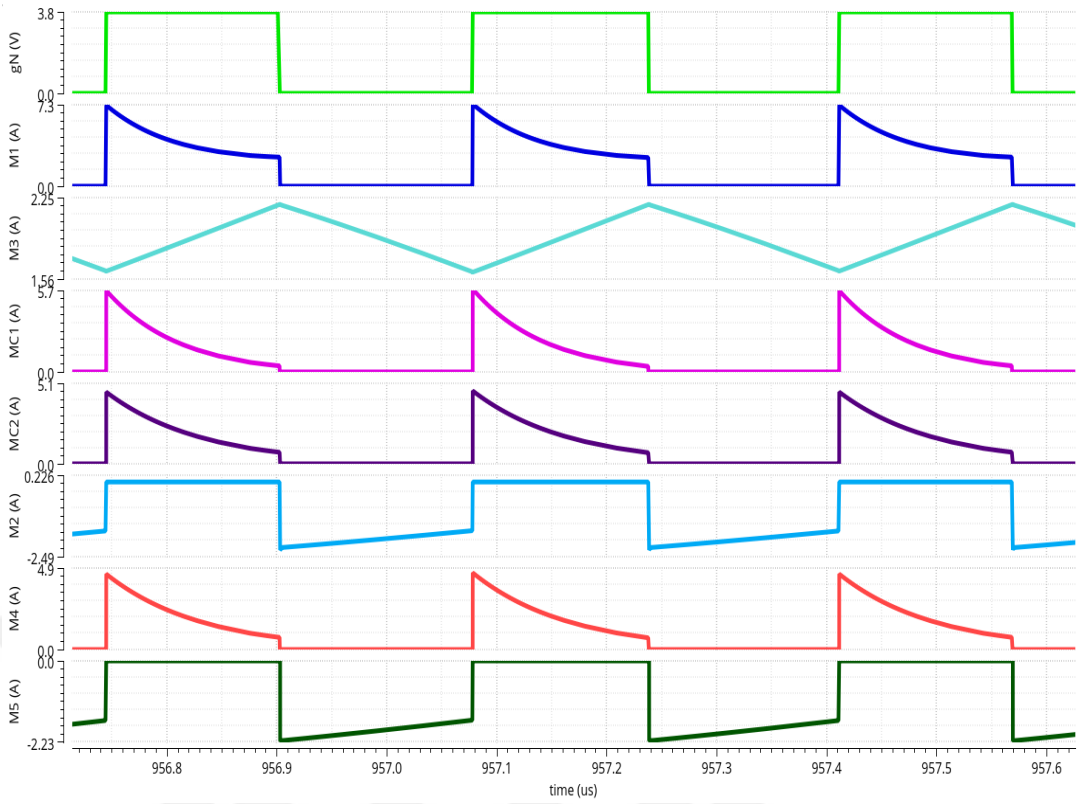

Figure 5.9 : Simulated waveform of switch currents when V_{IN} = 3.8V at a load current 1A for the proposed topology.

5.1.1 Duty cycle

Table. 5.2 presents the duty cycle results of three topologies with given conditions. Adding a flying capacitor into the circuit induces a reduction in the duty cycle. As desired, the time window supplying negative current to the output increases as a flying capacitor is inserted into the circuit since the duty cycle is decreased and the converter has more time to supply current to the output. There is a slight mismatch between theoretical duty cycle calculation and simulated duty cycle results. Due to the resistive losses caused by the on-resistance of the MOSFETs and DCR of the inductor, the simulated duty cycle is larger to compensate for the voltage drop to regulate the desired output voltage. The proposed topology shows a significant advantage at higher output loads. For instance, there might be a case that the conventional topology can not regulate desired output voltage because of the high duty cycle. If so, the topologies with a flying capacitor can be preferred.

Table 5.2 : Duty Cycle(%) - VNEG.

	V_{IN}=2.5V			V_{IN}=3.8V			V_{IN}=4.9V		
I_{Load}(A)	NFC	1FC	2FC	NFC	1FC	2FC	NFC	1FC	2FC
0.5	82	78	70	73	64	43	68	53	20
1	84	80	74	75	66	47	69	54	22
2	89	86	83	77	70	55	71	58	30

Another observation is that the circuit requires a higher duty cycle at higher loads and a lower duty cycle at lower loads, keeping the V_{IN} same for correct comparison. This is because the topologies only provide charge to the output in the second phase. Another advantage of the proposed hybrid converter is that relaxing system stability requirements, preventing issues such as sub-harmonic oscillation and the output voltage collapse issue, thanks to lowered duty cycle.

Fig. 5.10 shows the *ON* time of the switch in one switching period to calculate the duty cycle. The time duration of the high state of the gate control signal is defined as *ON* time of the switch. Since the duty cycle is calculated by dividing on time of the switch by the total switching period, the simulated waveform proves the duty cycle is equal to 47% for the proposed topology at a load current of 1A and V_{IN}=3.8V, as tabulated in Table. 5.2.

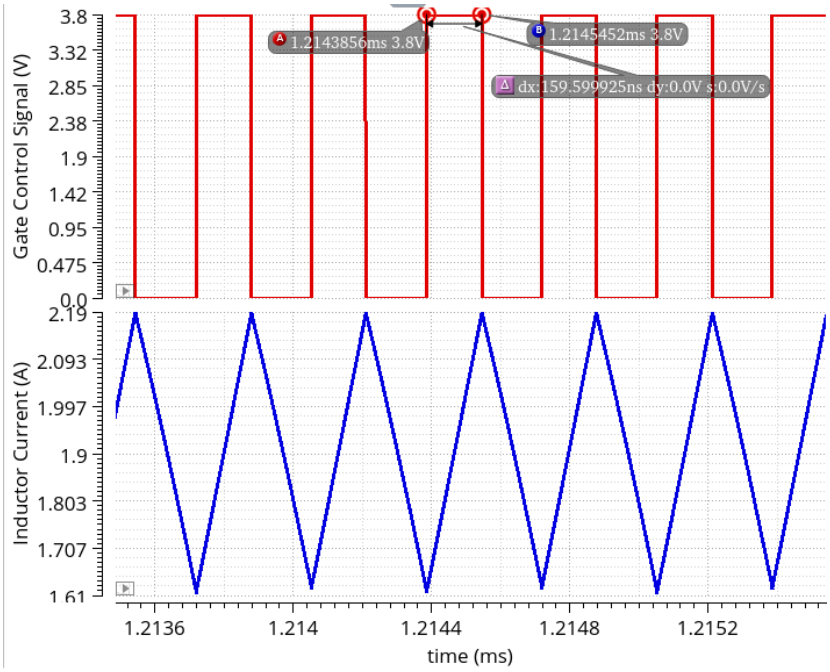

Figure 5.10 : Duty cycle measurement, I_{Load}=1A and V_{IN}=3.8V.

5.1.2 Efficiency

Table 5.3 tabulates the efficiency results of negative output voltage generation for the given specifications. The power efficiency results include modeled conduction losses, core losses, parasitic gate capacitance losses, and body diode conduction losses. Efficiency is calculated with the formula given at Eq. 2.2 in the steady state. Other loss contributors are calculated based on the expressions presented in Fig. A.1. It is observed that the power efficiency increases from NFC topology to 1FC topology and increases further with using 2FC topology.

When the input supply voltage is minimum($V_{IN} = 2.5V$), the proposed 2FC SIDO converter shows an efficiency improvement of up to 4.9% compared to 1FC topology and 8.3% efficiency improvement compared to the conventional topology. When the input supply voltage is $V_{IN} = 3.8V$, up to 1.8% improvement with the 1FC topology and 4.7% improvement with the 2FC topology is observed, compared to the conventional NFC topology. The peak efficiency of the 2FC converter is observed at minimum load and when $V_{IN} = 3.8V$. At maximum input voltage condition, the conduction losses start to dominate power loss and the proposed converter has slightly lower efficiency than NFC and 1FC topologies. However, the 2FC topology still has extensive advantages such as lower inductor current ripple, lower peak inductor current, and lower duty cycle owing to relaxed coil constraints.

Fig. 5.11 presents the breakdown of the contributions to the power losses for the proposed topology. The major loss contributors are the introduced switches M_{C2}, M_2, and M_4 which contribute approximately 30% of the total power loss. The loss contributors that are not listed in the pie chart have no significant effect on power loss; therefore, they are not written in the pie chart.

Table 5.3 : Efficiency (%) - VNEG.

	V_{IN}=2.5V			V_{IN}=3.8V			V_{IN}=4.9V		
I_{Load}(A)	NFC	1FC	2FC	NFC	1FC	2FC	NFC	1FC	2FC
0.5	85.7	88.1	90.6	91.8	93.6	94.8	93.4	95.2	93.6
1	72.7	76.1	81	85.8	88.7	90.5	89.8	92	90
2	48	52	54.6	74.1	76.9	80.9	81.1	84.2	83.9

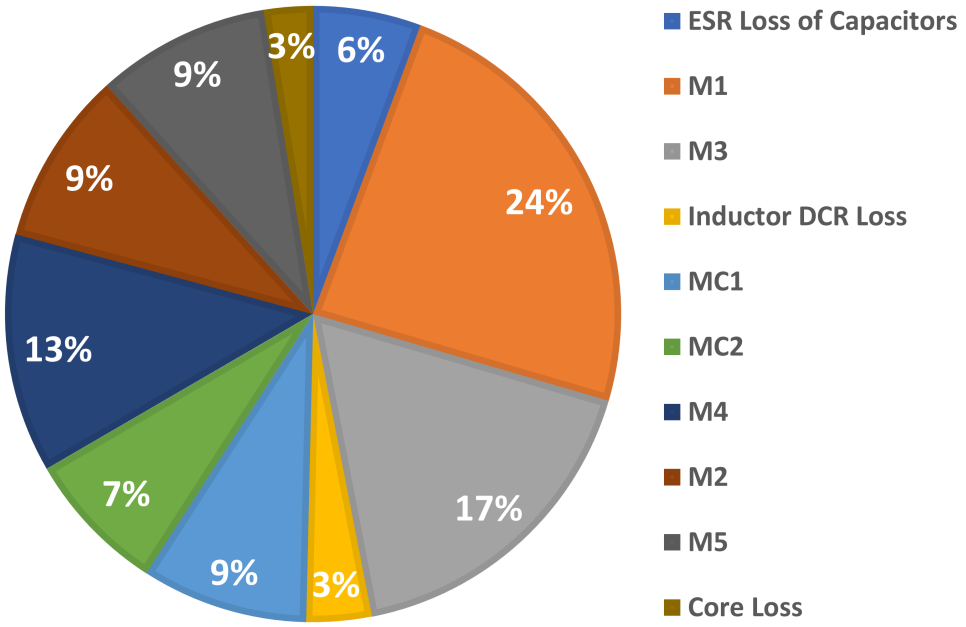

Figure 5.11 : Simulated power loss breakdown for negative output voltage generation for V_{IN}=3.8V at 1A.

5.1.3 Coil current constraints

In modern applications, inductor power efficiency affects the system performance as the demand for high-efficiency systems increases day by day. This demand results from reducing inductor power loss and the heat dissipation caused by it. The inductor in the system should be able to store enough current to provide output without saturating the core or excessively heating the winding.

Table 5.4 shows the inductor current ripple decreases similarly as a result of decreasing voltage drop over the coil. Coil constraint relaxation lead to the flexibility of using smaller coils. Reduction in the inductor current ripple will also alleviate the EMI noise generated by the converter. The flux density depends on the inductor current ripple, so reducing the flux density will prevent saturation of the core. As stated in Eq 4.1, the inductance of the inductor is directly proportional to the duty cycle while inversely proportional to the inductor current ripple. The inductance range in the system required is generally specified in the design phase, so the other design parameters come into play to ensure the required inductance range. For instance, there can be trade between lowered inductance, thus board area, and increased inductor

current ripple, as the specified inductance range allows. As advantages remarked, such as lowered duty cycle and decreased inductor current ripple, those advantages provide flexibility when choosing an inductor. That is to say, there is more headroom to trade between inductance and the ripple or the duty cycle, which allows flexibility.

Table 5.4 : Inductor Current Ripple(A) - VNEG.

	V_{IN}=2.5V			V_{IN}=3.8V			V_{IN}=4.9V		
I_{Load}(A)	NFC	1FC	2FC	NFC	1FC	2FC	NFC	1FC	2FC
0.5	0.96	0.93	0.75	1.04	0.87	0.53	1.11	0.88	0.24
1	0.71	0.66	0.55	0.86	0.77	0.57	1.19	0.85	0.32
2	0.55	0.51	0.49	0.84	0.78	0.62	1.42	0.88	0.45

The 2FC topology also achieves less inductor peak current as presented in Table 5.5, which helps in relaxing the magnetic core saturation constraints and alleviates possible die-heating issues. Decreasing the maximum inductor current also enables converter operation at higher ambient temperatures due to lower losses. Apart from that, the heat dissipated by the inductor decreases due to lowered peak inductor current. This will prevent saturation of the core and possible damage to the regulator. Keeping the output load the same and reducing the maximum current flowing in the circuit eliminates the risk of breakdown of the switches.

Table 5.5 : Max Inductor Current(A) - VNEG.

	V_{IN}=2.5V			V_{IN}=3.8V			V_{IN}=4.9V		
I_{Load}(A)	NFC	1FC	2FC	NFC	1FC	2FC	NFC	1FC	2FC
0.5	3.18	2.63	2.01	2.38	1.79	1.14	2.38	1.48	0.71
1	6.66	5.54	4.21	4.49	3.34	2.18	3.71	2.63	1.42
2	13.73	11.6	8.8	9.49	7.22	4.81	7.61	5.22	3.08

Another implication of selecting proper topology is the inductor saturation current limitation. For instance, the NFC and 1FC topologies exceed the saturation current I_{SAT} of the selected inductor at minimum input supply and maximum I_{LOAD} condition, which causes inductance degradation and possible system issues. Due to this advantage, the proposed topology with two flying capacitors may be the only option according to the specifications, since the topology allows operating at a lower peak inductor current.

The peak inductor current can be defined as the summation of the average inductor current and inductor current ripple as given by Eq 5.1.

$$I_{L(max)} = I_{L(avg)} + \Delta I_L \tag{5.1}$$

The inductor peak current shows a reduction because of the two components in the equation. First, the average inductor current decreased due to lowered duty cycle as defined by Eq. 3.12. Second, the inductor ripple current is decreased due to the reduced voltage drop of the inductor given by Eq. 2.3. Both effects come into sight by virtue of the flying capacitor and show a significant reduction in the proposed topology.

5.1.4 Core loss

The other benefit of the proposed topology is improved core loss as a result of decreasing voltage drop over the coil. Since the inductor current ripple directly affects the core loss based on the formula given by Eq. 4.5 and reduces the magnetic flux density, significant improvement is observed in the core loss. Table 5.6 tabulates the estimated core loss for each three topologies. Results are showing core loss decreases as a flying capacitor is inserted into the circuit. The proposed 2FC topology serves the lowest core loss.

Table 5.6 : Inductor Core Loss (mW) - VNEG.

	V_{IN}=2.5V			V_{IN}=3.8V			V_{IN}=4.9V		
I_{Load}(A)	NFC	1FC	2FC	NFC	1FC	2FC	NFC	1FC	2FC
0.5	86	68	32	83	47	24	101	45	26
1	55	39	21	65	39	18	90	41	19
2	28	22	9	55	29	13	70	46	14

Fig. 5.12 shows the simulated waveform of important signals that are used in Eq. 4.5 to obtain core loss. The theoretical observations are given in Eq. 4.6 and Eq. 4.7. The capacitor used in the inductor model given by Fig. 4.7 uses the inductor current information, and by charging and discharging that capacitor, the magnetic flux density can be modeled as given by Eq. 4.7. Therefore, the magnetic flux density increases as the inductor current increases, and the magnetic flux density decreases as the inductor current decreases. The red line in the waveform shows the estimated magnetic flux

density based on the inductor current and the core material parameters. The waveform also shows that the voltage drop over the coil V_L, equal in magnitude to capacitor current I_c in the inductor model given in Fig. 4.7. The findings from the model, as well as the core material coefficients, are embedded into Eq. 4.5 to estimate the core loss in the unit of Tesla.

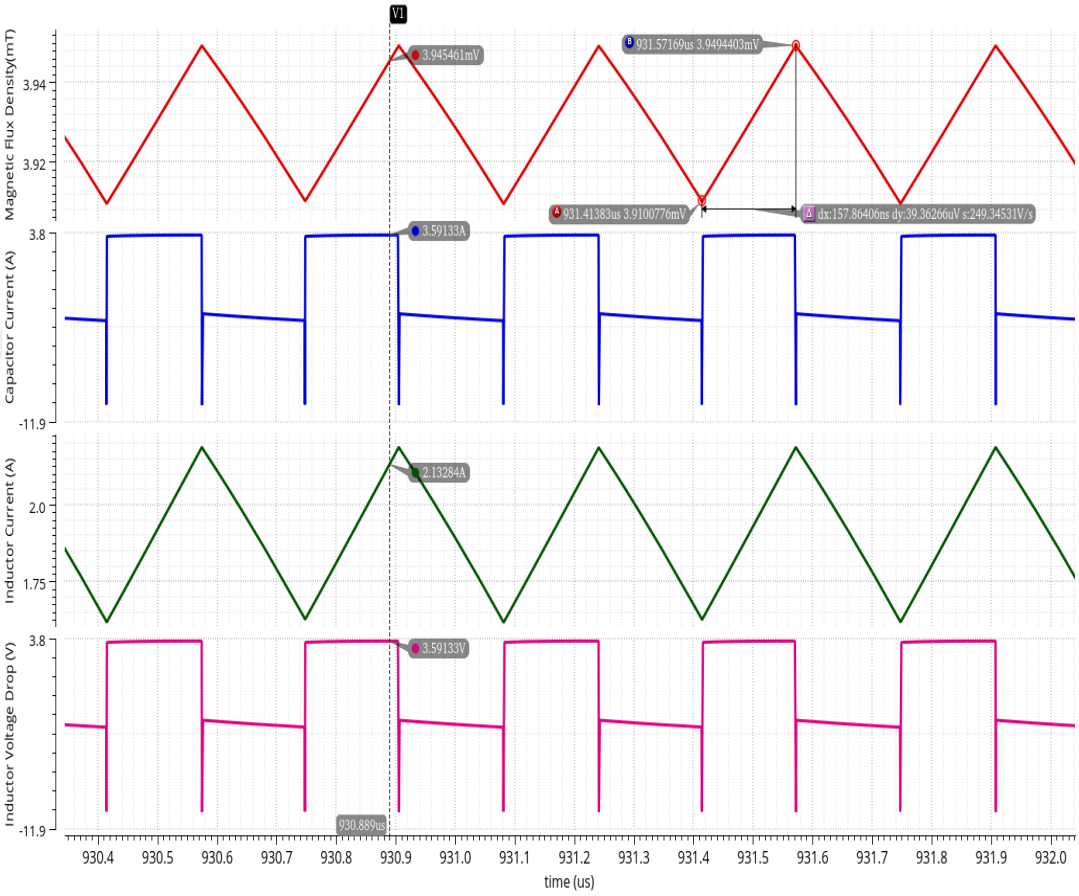

Figure 5.12 : Simulated waveform of important signals needed to define inductor model for core loss estimation.

Magnetics are the most critical part of switching converters, correct estimation of the magnetic losses in switching converters is an ongoing and growing research area. The method used in this work helps the estimation of the core loss in a simulation environment and enables the estimation of the magnetic losses in the earlier design phase for correct magnetic component selection.

5.2 Positive Output Voltage Regulation

The previously mentioned performance improvements apply to positive output voltage generation. In general, better power conversion efficiency with relaxed coil current constraints is achieved with the proposed multiple-flying capacitor topology.

Since designs are simulated with different load conditions, Fig. 5.13, Fig. 5.14 and Fig. 5.15 show the steady state operation of the proposed topology with 500mA, 1A and 2A, respectively. All of the waveforms show 2FC SIDO converter settles desired V_{POS} voltage and can provide stable output over a wide load current range.

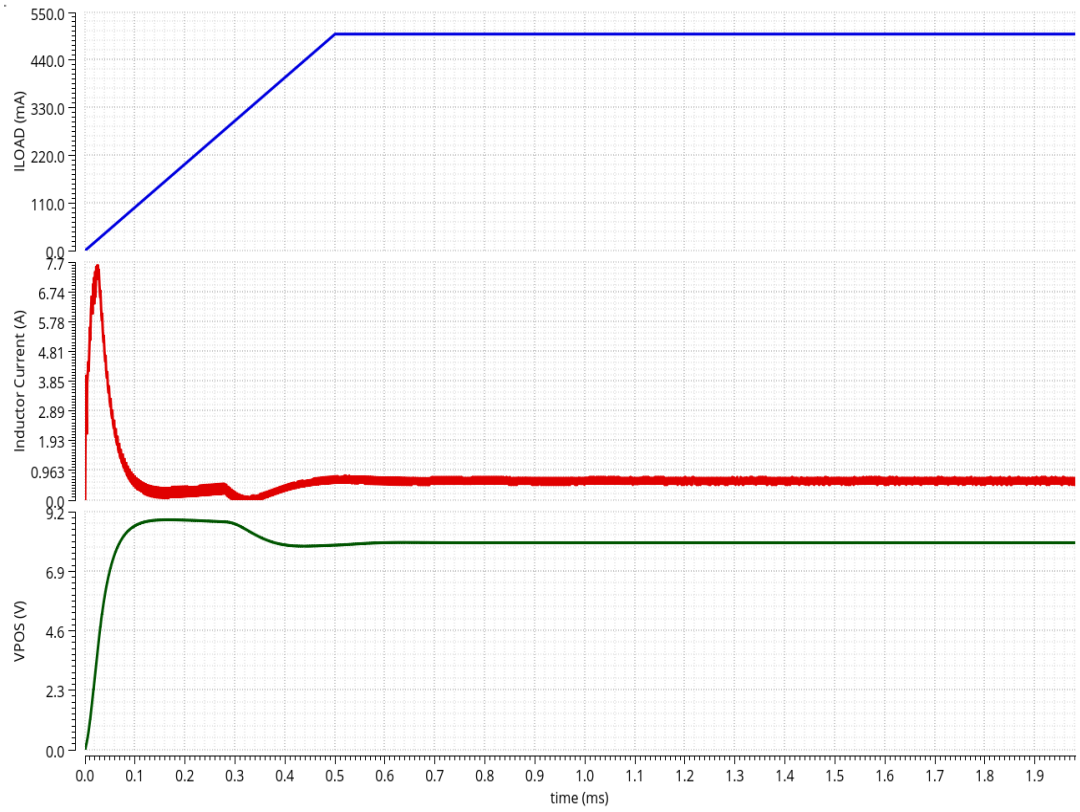

Figure 5.13 : Simulated waveform of I_L, ΔV_L and V_{POS} in the steady state at a load current of 500mA when V_{IN} = 3.8V.

The ΔV_L improvement between the topologies is demonstrated given by Fig. 5.16 for the V_{POS} operation. The simulated waveform compares the inductor voltage drop of the NFC, 1FC, and 2FC topologies at a load current of 1A and at the input supply voltage of 3.8V. As proposed, introducing the flying capacitor into the circuit decreases the voltage drop of the inductor at the de-magnetization phase of the inductor and

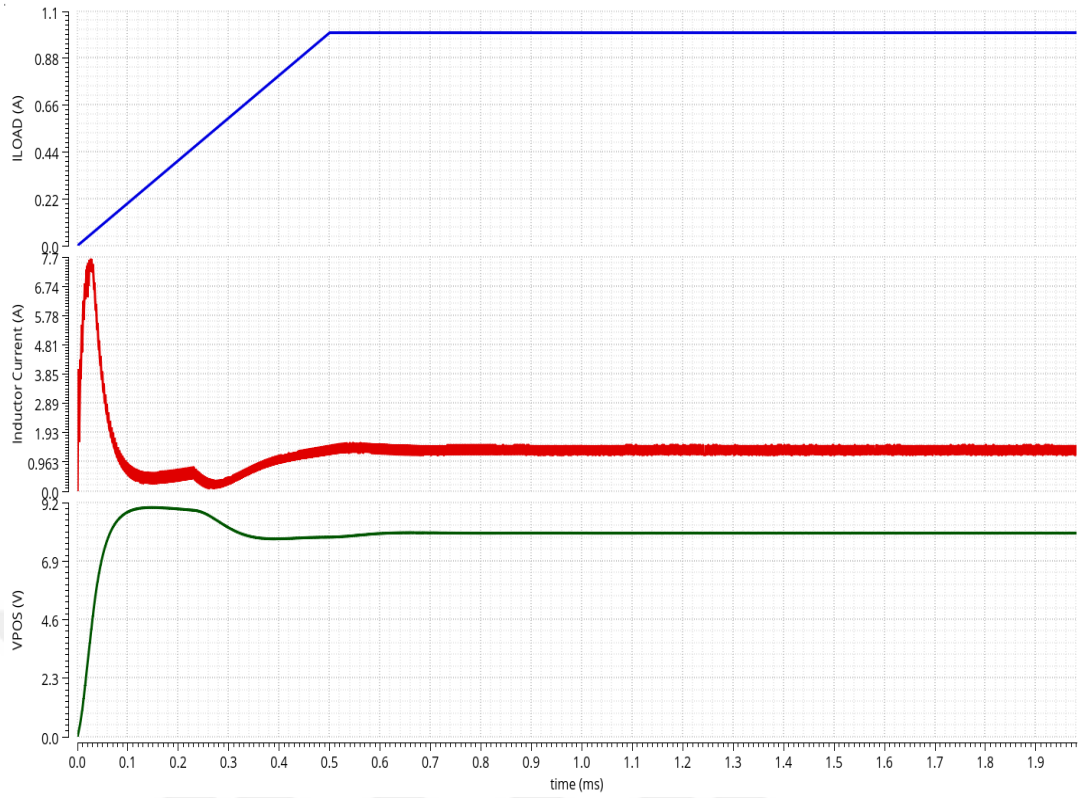

Figure 5.14 : Simulated waveform of I_L, ΔV_L and V_{POS} in the steady state at a load current of 1A when V_{IN} = 3.8V.

provides an improvement in many aspects. The waveform also depicts how the de-magnetization phase duration is increased and the discharging slope decreased for the operation.

Fig. 5.17 shows switch currents for the proposed topology when the converter reaches a steady state. Similar to the negative output voltage operation, no excessive current is observed in any of the switches in the path thanks to the non-overlapping circuit, and non-overlapping time is enough to balance the risk of shoot-through and the body diode conduction losses.

The switch currents presented in Fig. 5.17 also show the operation phases of the proposed converter, as already depicted in Fig. 3.10. Once the gate control signal goes high, M_1, M_{C1}, M_{C2}, M_4 and M_3 start to conduct. M_1, M_{C1}, M_{C2} currents increase through capacitive current, therefore, they show exponential behavior. Once the gate control signal goes low, M_6 starts to conduct and charges the output capacitor C_{POS} to generate the positive output voltage.

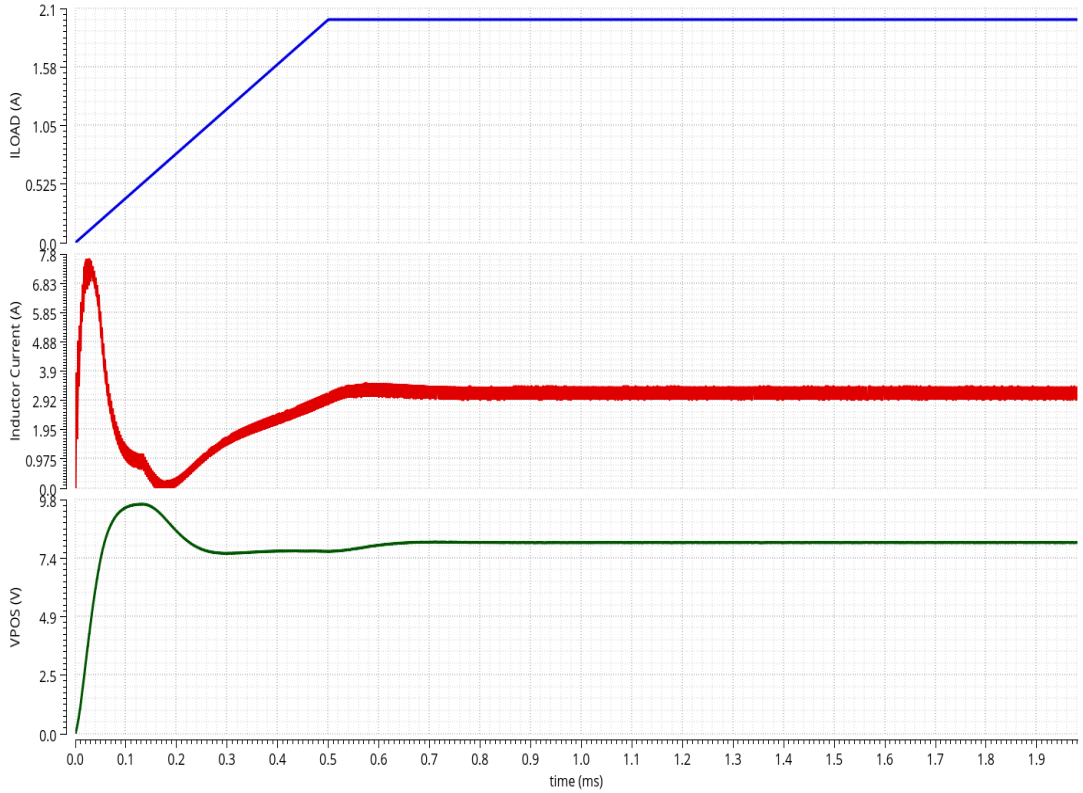

Figure 5.15 : Simulated waveform of I_L, ΔV_L and V_{POS} in the steady state at a load current of 2A when V_{IN} = 3.8V.

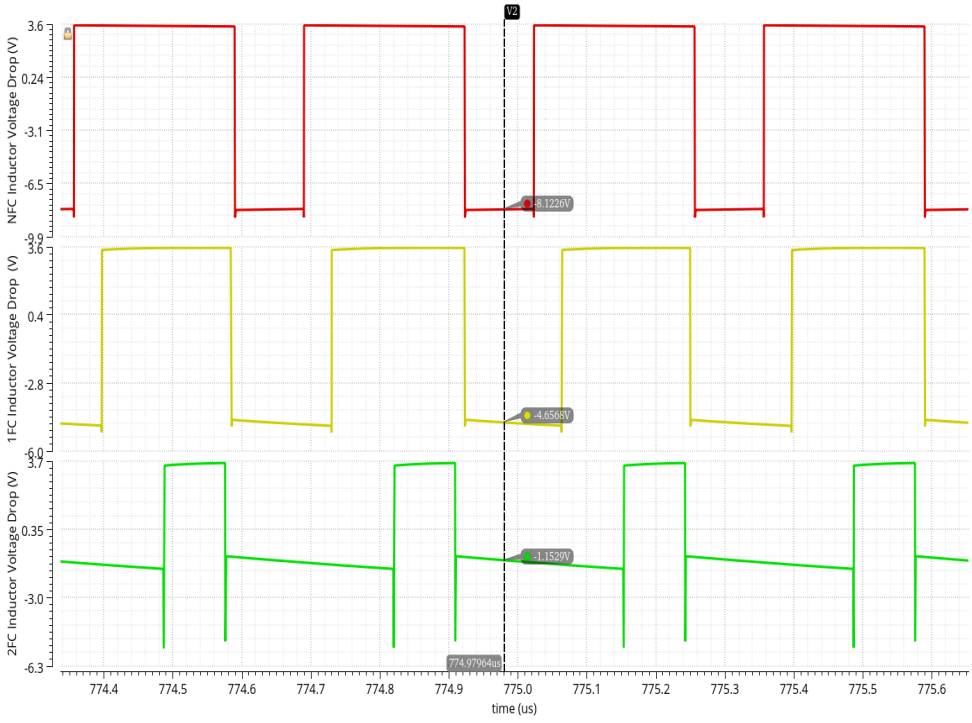

Figure 5.16 : Inductor voltage improvement between topologies.

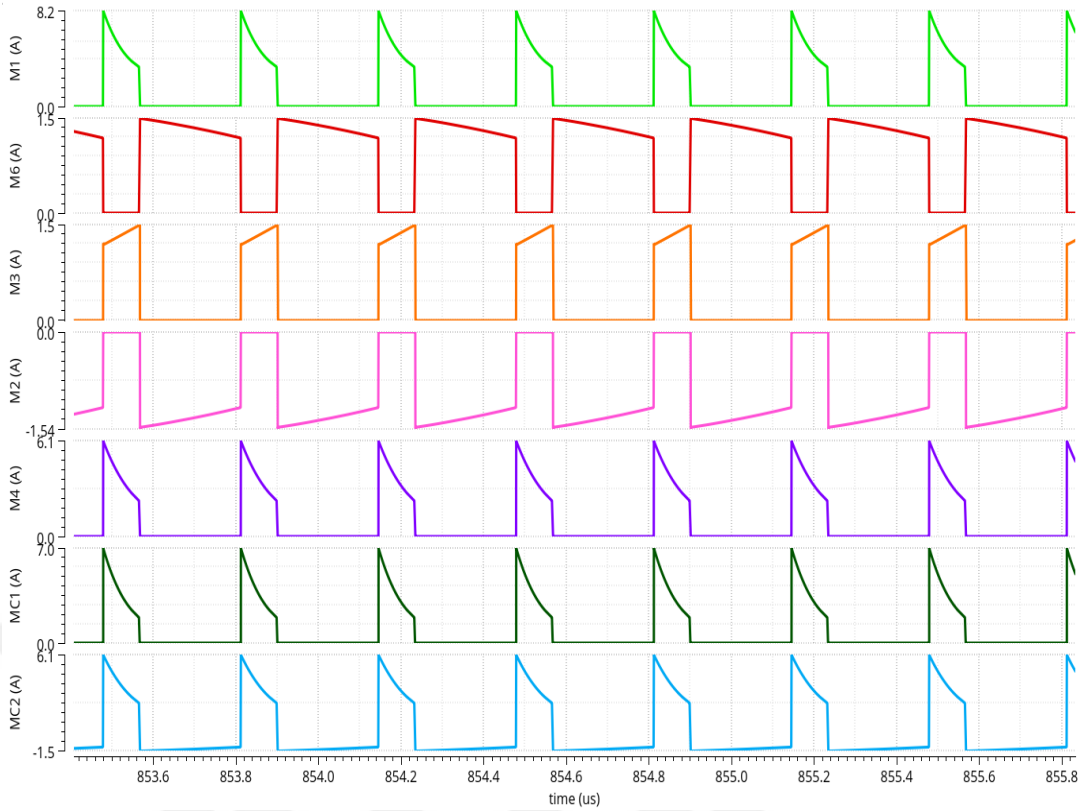

Figure 5.17 : Simulated waveform of switch currents when V_{IN} = 3.8V at a load current 1A for the proposed topology, VPOS.

The voltage drop of the flying capacitors is given by Fig. 5.18. The flying capacitors are being charged close to V_{IN} when the inductor is magnetized. There are conduction losses caused by the switches therefore, they can not completely charge to V_{IN}. As seen in Fig. 5.18, they are not completely discharging; thus, they still have some voltage stored while the inductor current is discharging. As stated in the V_{NEG} operation, this helps the inductor voltage drop to be more positive since two flying capacitors keep the voltage during the de-magnetization phase. Consequently, this relaxes coil constraints and voltage stress on the switches.

5.2.1 Duty cycle

Table 5.7 tabulates duty cycle results of three topologies based on specifications given by Table 5.1. The first thing seen on the table is that duty cycle information is not present when I_{LOAD} is 2A and at minimum V_{IN} condition for the conventional topology and the 1FC SIDO topology. The reason is that the conventional topology and the

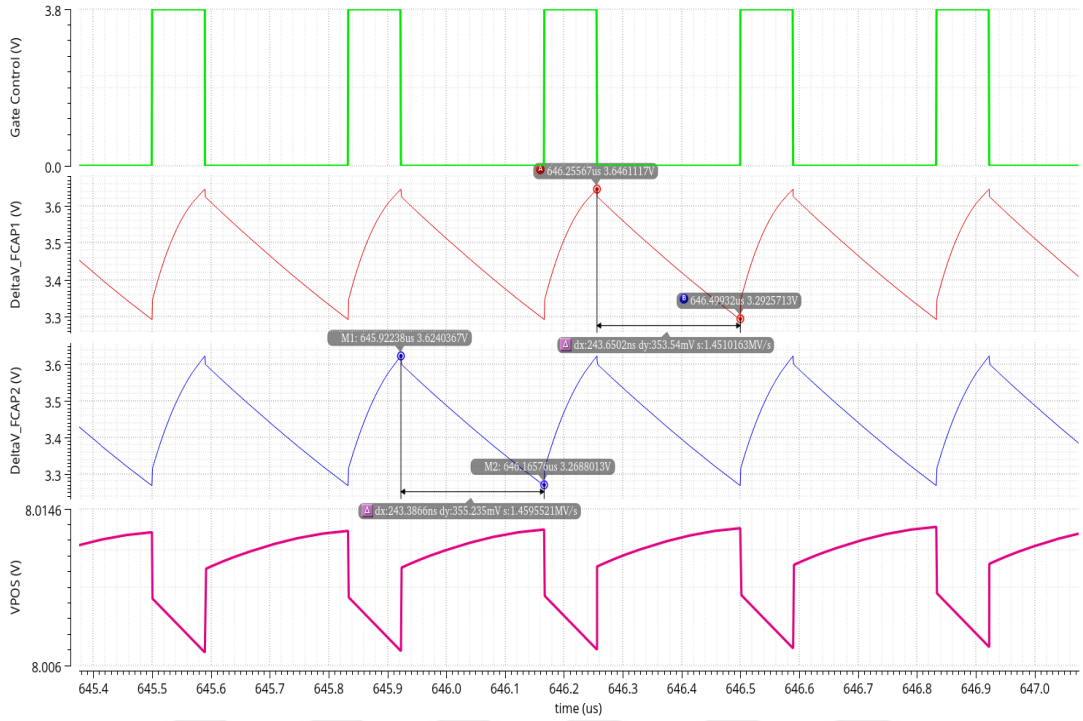

Figure 5.18 : Flying capacitor voltages of the proposed topology, VPOS operation.

SIDO topology with one flying capacitor topology are not able to regulate to desired V_{POS} in the switching period. In the conditions, the duty cycle is so high that there is less time interval, and almost no time interval available for the stored inductor current being transferred to the output. For V_{POS} operation, the proposed topology clearly shows an advantage at higher loads and minimum V_{IN} due to its ability to provide regulated output thanks to the multiple flying capacitors.

Similar to the negative output voltage operation, introducing a flying capacitor helps to decrease the duty cycle and shows the same benefits as in the negative output voltage operation. The duty cycle is decreased and the converter has more time to supply current to the output load. Decreased duty cycle also relaxes system stability requirements and output voltage collapse issue [1]. Similar to the V_{NEG} operation, there is a slight mismatch between theoretical duty cycle calculation and simulated duty cycle results. Due to the resistive losses caused by the on-resistance of the MOSFETs and DCR of the inductor, the simulated duty cycle is larger to compensate for the voltage drop in order to regulate the desired output voltage.

Table 5.7 : Duty Cycle(%) - VPOS.

	V_{IN}=2.5V			V_{IN}=3.8V			V_{IN}=4.9V		
I_{Load}(A)	NFC	1FC	2FC	NFC	1FC	2FC	NFC	1FC	2FC
0.5	78	70	62	69	58	40	65	42	20
1	83	75	66	71	57	30	64	43	27
2	-	-	75	72	60	42	66	48	25

5.2.2 Efficiency

Table 5.8 presents efficiency results for the positive output voltage generation. When the load current is 2A, NFC, and 1FC topology efficiency results are not present since these topologies are not able to provide regulated output voltage due to high duty cycle, since there is not enough OFF time to deliver current to the output. The information related to these topologies under given conditions will be left blank in the table given by Table 5.8.

The proposed topology shows a significant advantage at minimum input voltage ($V_{IN} = 2.5V$) condition, especially at the highest load. At that condition, the 2FC SIDO converter is the only option due to its lowered duty cycle and can regulate to desired output voltage level. For the $V_{IN} = 3.8V$ case, even though the efficiency numbers for 1FC and 2FC topologies are observed to be similar, the 2FC topology still can be the preferred option owing to the advantage of lower duty cycle operation with relaxed coil current constraints.

Similar to the negative output voltage operation, conduction losses become dominant at maximum input voltage therefore efficiency of the 2FC topology is lower than the 1FC and NFC topologies. However, all of the other advantages are still present for the 2FC topology. At maximum input supply voltage ($V_{IN} = 4.9V$), the efficiency of the proposed 2FC converter drops because of the dominance of the conduction losses. Similarly, other advantages are still present for the proposed topology and the trade-off can be made between efficiency and the relaxed coil constraints based on the application requirements.

Fig. 5.19 presents the breakdown of the contributions to the power losses for the proposed topology at positive voltage operation. The major loss contributors are the

Table 5.8 : Efficiency(%) - VPOS.

	V_{IN}=2.5V			V_{IN}=3.8V			V_{IN}=4.9V		
I_{Load}(A)	NFC	1FC	2FC	NFC	1FC	2FC	NFC	1FC	2FC
0.5	88.3	90.7	91.1	92.8	94.4	93.4	94.3	95.7	80.1
1	74.9	80.1	83.7	87.2	89.2	88.9	90.3	92.6	78.4
2	-	-	63.2	75.4	80.6	81.3	82.7	86	75

M_{C2}, M_1, and M_4 which contribute approximately half of the total power loss. The loss contributors that are not listed in the pie chart have no significant effect on power loss; therefore, they are not written in the pie chart. M_1 has the highest conduction loss but this is the high-side buck-boost switch and is naturally present in all of the configurations therefore, this should not be considered a drawback of the proposed topology.

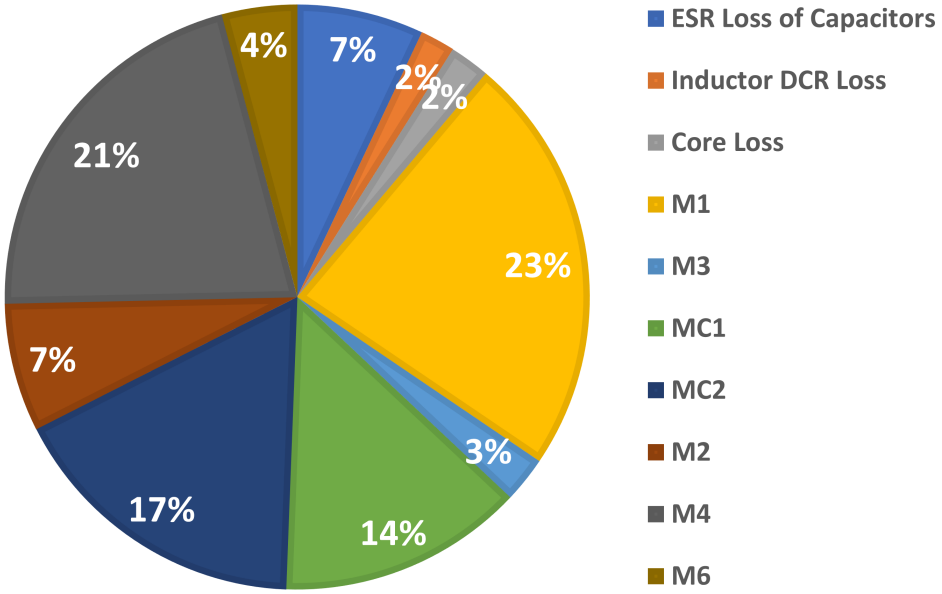

Figure 5.19 : Simulated power loss breakdown for positive output voltage generation for V_{IN}=3.8V at 1A.

5.2.3 Coil current constraints

Table 5.9 lists inductor current ripple for all of the topologies. The same benefit is also present when generating positive output voltage, thanks to the flying capacitors added into the circuit, the inductor observes less voltage and this translates to a reduction in inductor current ripple. Due to the insufficient de-magnetization phase duration, NFC

and 1FC topologies are not able to provide regulated output voltage when V_{IN}=2.5V and at a load current of 2A. Therefore, information related to these topologies in Table 5.9 and Table 5.10 are left blank.

Table 5.9 : Inductor Current Ripple(A) - VPOS.

	V_{IN}=2.5V			V_{IN}=3.8V			V_{IN}=4.9V		
I_{Load}(A)	NFC	1FC	2FC	NFC	1FC	2FC	NFC	1FC	2FC
0.5	0.67	0.62	0.49	0.89	0.78	0.34	1.31	0.65	0.27
1	2.06	1.03	0.67	1.38	1.23	0.35	1.27	0.67	0.22
2	-	-	0.67	0.95	0.73	0.43	1.26	0.71	0.35

Table 5.10 tabulates peak inductor currents for each topology. Overall, the same performance is obtained for the positive output voltage generation considering the relaxation of the coil constraints.

Table 5.10 : Max Inductor Current(A) - VPOS.

	V_{IN}=2.5V			V_{IN}=3.8V			V_{IN}=4.9V		
I_{Load}(A)	NFC	1FC	2FC	NFC	1FC	2FC	NFC	1FC	2FC
0.5	2.64	2.07	1.48	2.11	1.48	0.74	1.95	1.21	0.54
1	5.97	4.3	3.13	3.95	2.84	1.52	3.37	2.13	1.12
2	-	-	8.42	8.03	5.58	3.38	6.51	4.17	2.46

For the V_{POS} operation, the peak inductor current can be defined as the summation of the average inductor current and inductor current ripple as given by Eq 5.1. Similar to the For the V_{NEG} operation, the inductor peak current shows a reduction because of the two components in the equation. First, the average inductor current decreased due to lowered duty cycle as defined by Eq. 3.12. Second, the inductor ripple current is decreased due to the reduced voltage drop of the inductor given by Eq. 2.3. Both effects come into sight by virtue of the flying capacitor and show a significant reduction in the proposed topology.

5.2.4 Core loss

Last but not least, the improvement in magnetic losses applies to positive voltage generation with the proposed 2FC topology. Table 5.11 tabulates the core loss values. Due to the reduction in inductor current ripple which results in decreased magnetic

flux, the core loss decreases, thanks to the flying capacitor introduced to the circuit. Due to the same reason as explained in previous sections, the NFC and 1FC topologies do not include core loss results when V_{IN}=2.5V and at a load current of 2A.

Table 5.11 : Core Loss(mW) - VPOS.

	V_{IN}=2.5V			V_{IN}=3.8V			V_{IN}=4.9V		
I_{Load}(A)	NFC	1FC	2FC	NFC	1FC	2FC	NFC	1FC	2FC
0.5	30	25	11	47	33	14	46	22	10
1	120	90	63	98	75	22	119	65	24
2	-	-	30	66	31	8	68	26	11

6. CONCLUSIONS AND FUTURE WORKS

A novel SIDO DC-DC converter with two flying capacitors is presented. The topology aims to reduce the voltage drop on the inductor compared to the conventional converters, targeting to improve core losses and power efficiency. Besides, the proposed 2FC topology reduces peak inductor current and ripple while operating with lower duty cycles for both negative and positive output voltage generation. Simulation results show a reduction in inductor peak current and inductor ripple, along with low-duty cycle operation, which leads to relaxed converter stability and coil current constraints. Table 6.1 summarizes the proposed 2FC performance specifications for V_{NEG} and V_{POS} operation.

Table 6.1 : Summary of the Converter Performance.

Parameter	Value
Peak Efficiency, V_{NEG}	%94.8
Max efficiency improvement compared to NFC, V_{NEG}	%8.3
Max efficiency improvement compared to 1FC, V_{NEG}	%4.9
Maximum ripple, V_{NEG}	750mA
Peak inductor current, V_{NEG}	8.8A
Peak Efficiency, V_{POS}	%93.4
Max efficiency improvement compared to NFC, V_{POS}	%8.8
Max efficiency improvement compared to 1FC, V_{POS}	%3.6
Maximum ripple, V_{POS}	670mA
Peak inductor current, V_{POS}	8.42A

Simulations with given display driver application specifications show up to 8.3% efficiency improvement compared to the conventional SIDO converter and up to 4.9% efficiency improvement compared to the SIDO converter with one flying capacitor topology, for the negative voltage generation. For the positive voltage generation, simulations show up to 8.8% efficiency improvement compared to the conventional SIDO converter and up to 3.6% efficiency improvement compared to the SIDO converter with one flying capacitor topology. The listed efficiency numbers show maximum efficiency improvement is observed and the maximum improvement is

observed when the input supply voltage is 2.5V at a load current of 1A. Maximum ripple and the peak inductor current values are listed for the worst cases (i.e. where they are maximum) to indicate the performance of the proposed 2FC converter.

Even though the technique is described through the example of a SIDO converter, the proposed technique can be applied to other hybrid switching converter topologies. To our best knowledge, this is the first work in the literature employing multiple flying capacitors on the same voltage rail, presenting performance improvements of the hybrid topology.

The proposed topology is modeled with ideal elements in an effort to showcase the advantages of the topology. Non-idealities are inserted into the macro model to make the model more precise. Transistor-level implementation of the power stage will reveal other design challenges, such as driving the negative rail switch(M_4, buck low-side switch) for negative voltage operation and driving boost high-side switch(M_3) for positive output voltage generation. In negative voltage operation, to turn *ON* the negative rail switch, the negative gate drive signal is required. So, this creates the need for proper design of negative output level shifter to correctly drive the buck low-side switch. As a future work, the transistor-level implementation of the power stage together with the system-level implementation can be utilized.

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APPENDICES

APPENDIX A : Simulation Setup

APPENDIX A

Name	Type	Details	EvalType	Plot
avg_input_current_VNEG	expr	average(clip(IT("/HS_SW_FCAP/N+") VAR("tsettle") VAR("simtime")))	point	☑
avg_inductor_current	expr	average(clip(IT("/L0/PLUS") VAR("tsettle") VAR("simtime")))	point	☑
inductor_current_ripple	expr	(ymax(clip(IT("/L0/PLUS") VAR("tsettle") VAR("simtime"))) - ymin(clip(IT("/L0/PLUS") VAR("tsettle") VAR("simtime"))))	point	☑
max_inductor_current	expr	ymax(clip(IT("/L0/PLUS") VAR("tsettle") VAR("simtime")))	point	☑
%_ripple	expr	((inductor_current_ripple / avg_inductor_current) * 100)	point	☑
output_current	expr	VAR("iload")	point	☑
Pin_VNEG	expr	((avg_VIN * avg_input_current_VNEG) + driving_gate_caps + Ploss_core)	point	☑
Ploss_VNEG_HS	expr	(pow(rms(clip(IT("/HS_SW_FCAP/N+") VAR("tsettle") VAR("simtime"))) 2) * VAR("Ron_sw_hs"))	point	☑
Ploss_VNEG_LS	expr	(pow(rms(clip(IT("/LS_SW_FCAP/N+") VAR("tsettle") VAR("simtime"))) 2) * VAR("Ron_sw_ls"))	point	☑
Ploss_VNEG_LS_BUCK	expr	(pow(rms(clip(IT("/LS_SW_BUCK/N+") VAR("tsettle") VAR("simtime"))) 2) * VAR("Ron_sw_ls"))	point	☑
Ploss_VNEG_MC1	expr	(pow(rms(clip(IT("/CHARGING_SW/N+") VAR("tsettle") VAR("simtime"))) 2) * VAR("Ron_sw_mc"))	point	☑
Ploss_dcr	expr	(pow(rms(clip(IT("/Rsense/PLUS") VAR("tsettle") VAR("simtime"))) 2) * VAR("rsense"))	point	☑
Ploss_diode	expr	average(clip((IT("/G2/PLUS") * (VT("/VNEG") - VT("/LXC"))) VAR("tsettle") VAR("simtime")))	point	☐
Ploss_core	expr	(aV * (on_time_loss + off_time_loss))	point	☑
Ploss_caps	expr	(VAR("n_sw") * VAR("Cgg") * (1 / period) * pow(VAR("vin") 2))	point	☑
Ploss_esr_cout	expr	(pow(rms(clip(IT("/Resr_cout/PLUS") VAR("tsettle") VAR("simtime"))) 2) * VAR("Resr_cout"))	point	☑
Ploss_esr_fcap	expr	(pow(rms(clip(IT("/Resr_fcap/PLUS") VAR("tsettle") VAR("simtime"))) 2) * VAR("Resr"))	point	☑
driving_gate_caps	expr	(average(clip(getData("I10:pwr" ?result "tran") VAR("tsettle") VAR("simtime"))) * VAR("n_sw"))	point	☑
Ploss_hs_body_diode	expr	(- average(clip(((VT("/VIN") - VT("/net4")) * IT("/D1/vp")) VAR("tsettle") VAR("simtime"))))	point	☑
Ploss_ls_body_diode	expr	average(clip(((VT("/VNEG") - VT("/LXC")) * IT("/D0/vp")) VAR("tsettle") VAR("simtime")))	point	☑
Ploss_ls_boost_body_diode	expr	average(clip((VT("/net14") * IT("/D2/vp")) VAR("tsettle") VAR("simtime")))	point	☑
Ploss_charging_sw_body_diode	expr	average(clip((VT("/LXC") * IT("/D3/vp")) VAR("tsettle") VAR("simtime")))	point	☑
Total_loss_VNEG	expr	(Ploss_VNEG_HS + Ploss_VNEG_MC1 + Ploss_core + Ploss_dcr + Ploss_VNEG_LS + Ploss_VNEG_LS_BUCK + Ploss_esr_cout + Ploss_esr_fcap + Plos...	point	☑
Pout_VNEG	expr	(Pin_VNEG - Total_loss_VNEG)	point	☑
Pout_VNEG1	expr	(- (output_current * avg_VNEG))	point	☑
EFF_VNEG_loss_contributors	expr	((Pout_VNEG / Pin_VNEG) * 100)	point	☑
EFF_VNEG1_pout/pin	expr	((Pout_VNEG1 / Pin_VNEG) * 100)	point	☑
delta_B	expr	(ymax(clip(Flux_density 0.00186 0.001863)) - ymin(clip(Flux_density 0.00186 0.001863)))	point	☑
delta_Bm	expr	pow((ymax(clip(Flux_density 0.00186 0.001863)) - ymin(clip(Flux_density 0.00186 0.001863))) VAR("m_param"))	point	☑
aV	expr	(VAR("alfa") * VAR("core_volume"))	point	☑
ton_pow_n	expr	pow((2 * ton) VAR("n_param"))	point	☑
toff_pow_n	expr	pow((2 * toff) VAR("n_param"))	point	☑
d_on	expr	(ton / period)	point	☑
d_off	expr	(toff / period)	point	☑
on_time_loss	expr	((delta_Bm / ton_pow_n) * d_on)	point	☑
off_time_loss	expr	((delta_Bm / toff_pow_n) * d_off)	point	☑

Figure A.1 : Simulation expressions.

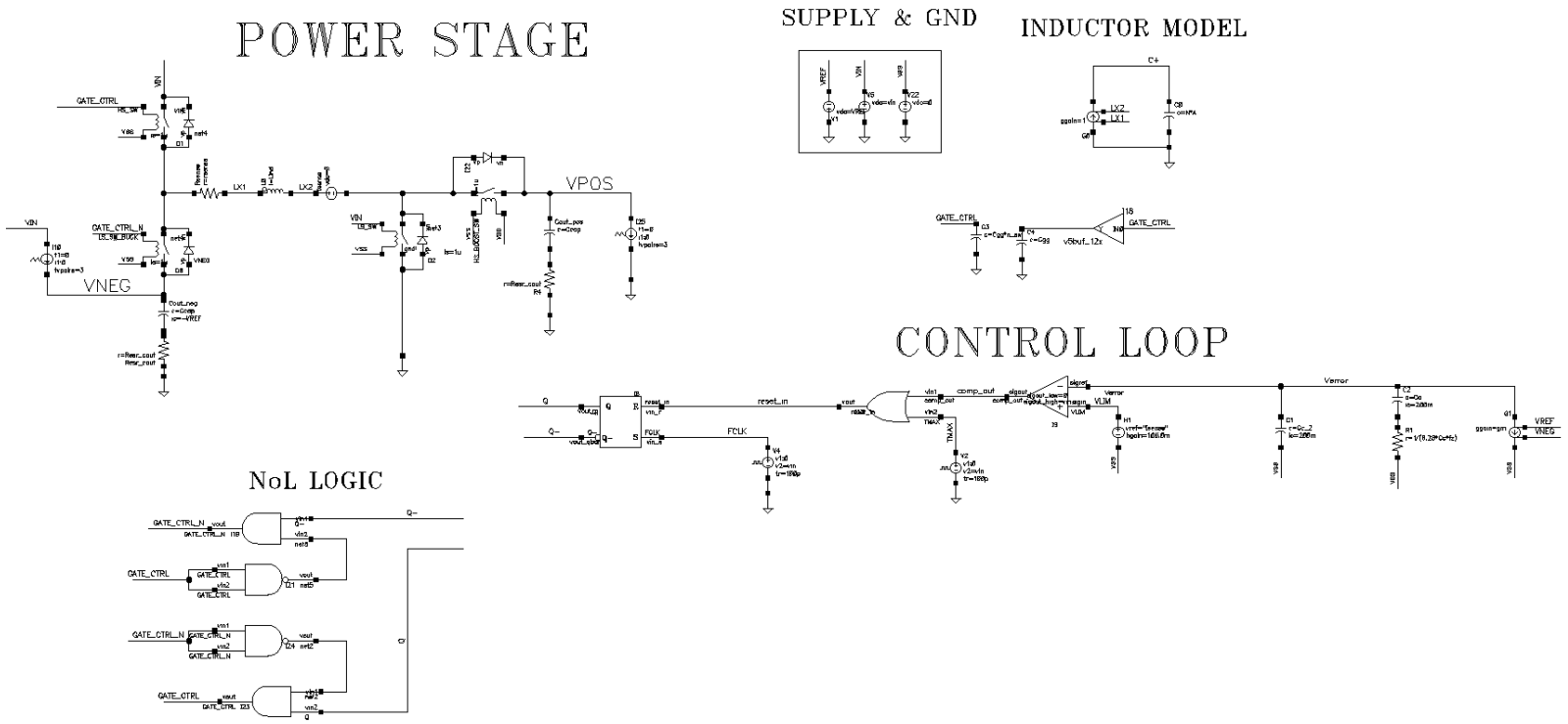

Figure A.2 : Simulation testbench of NFC topology.

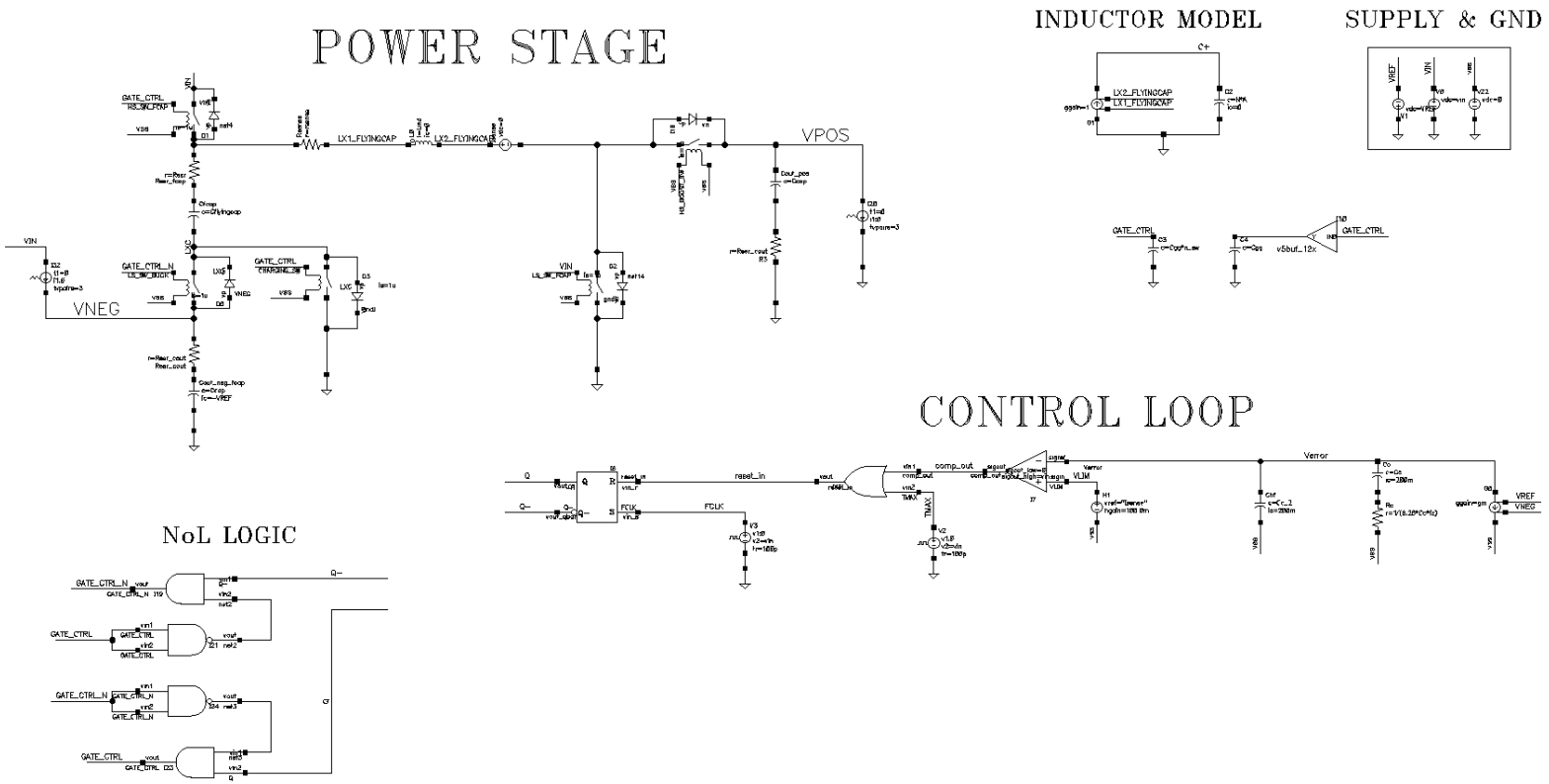

Figure A.3 : Simulation testbench of 1FC topology.

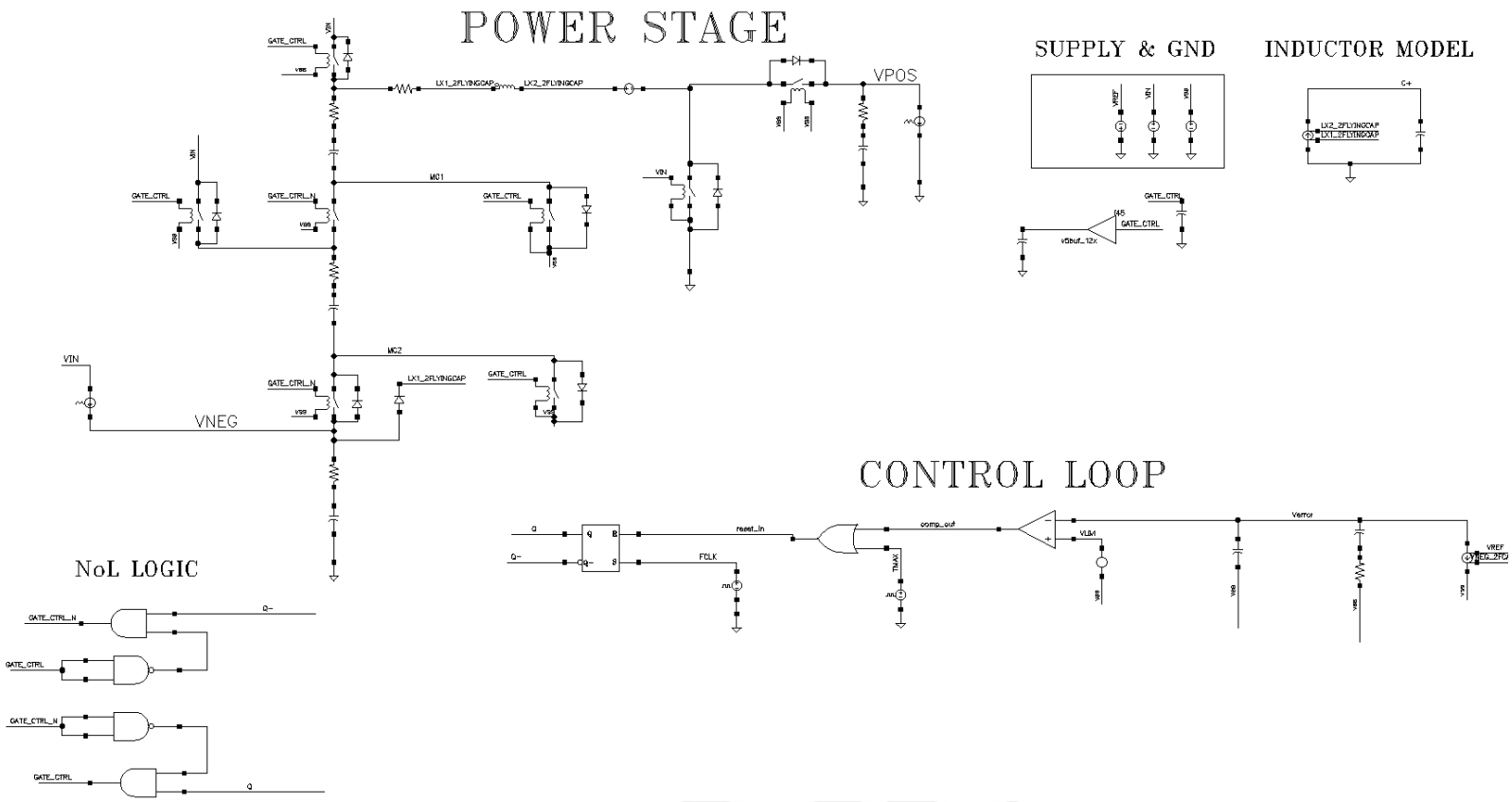

Figure A.4 : Simulation testbench of 2FC topology.

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PUBLICATIONS, PRESENTATIONS AND PATENTS ON THE THESIS:

- **Yılmaz H.**, Ozanoğlu K., Cavallini P. and Yazgi M.."Single-Inductor Dual-Output DC-DC Converter with Multiple Flying Capacitors," 2023 International Conference on Synthesis, Modeling, Analysis and Simulation Methods, and Applications to Circuit Design (SMACD), (2023).