ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

8 Gbps LVDS TRANSMITTER DESIGN IN 22 nm FD-SOI FOR HIGH SPEED CHIP-TO-CHIP COMMUNICATION INTERFACES

M.Sc. THESIS

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Department of Electronics and Communication Engineering

Electronics Engineering Programme

JUNE 2024

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ LİSANSÜSTÜ EĞİTİM ENSTİTÜSÜ

ÇİPTEN ÇİPE YÜKSEK HIZLI HABERLEŞME ARAYÜZLERİ İÇİN 22 nm FD-SOI TEKNOLOJİSİNDE 8 Gbps LVDS VERİCİ TASARIMI

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To my family and my best friend,

FOREWORD

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ABBREVIATIONS

CDR : Clock-Data Recovery
CMFB : Common Mode Feedback
CML : Current-Mode Logic
CMOS : Complementary Metal Oxide Semiconductor
CMRR : Common Mode Rejection Ratio
EMI : Electromagnetic Interference
ESD : Electrostatic Discharging
FDSOI : Fully Depleted Silicon on Insulator
FF : Fast Fast
FS : Fast Slow
Gbps : Gigabit per second
IDE : Integrated Drive Electronics
I/O : Input Output
LVDS : Low-Voltage Differential Signaling
MC : Monte Carlo
OTA : Operational Transconductance Amplifier
PCB : Printed Circuit Board
PCI : Peripheral Component Interconnect
PN : Pseudo Random
PSRR : Power Supply Rejection Ratio
PVT : Process Voltage Temperature
RMS : Root Mean Square
RX : Receiver
SF : Slow Fast
SoC : System on Chip
SS : Slow Slow
SST : Source-Series Terminated
STB : Stability
TRX : Transceiver
TT : Typical Typical
TX : Transmitter

SYMBOLS

C	**:** Capacitance
R	**:** Resistance
L	**:** Inductance
V	**:** Volt
A	**:** Ampere
W	**:** Watt
dB	**:** Decibel
mm	**:** Milimeter
n	**:** nano
p	**:** pico
m	**:** mili
J	**:** Joule

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8 Gbps LVDS TRANSMITTER DESIGN IN 22 nm FD-SOI FOR HIGH SPEED CHIP-TO-CHIP COMMUNICATION INTERFACES

SUMMARY

In recent years, tremendous advancements in the processing speed of microprocessors, motherboards, optical transmission links, and routers have expanded the off-chip data rates. The increasing demand for data bandwidth across electronic systems has led to significant innovations in wireline input/output (I/O) drivers. Various standards have been created by many institutions to manage the difficulties of high-speed wireline data transmission. The aggressive technology scaling not only increased the interest in I/O speed but also it additionally contributed noticeably to the enhancement in data rate and power efficiency of the wireline links. Even though the I/O data rates and data processing power have been improved by the technology scaling, the bandwidth of the copper links has not been scaled in the same manner. Therefore, the requirement for advanced equalization techniques has emerged in recent years to eliminate the corrosive effect of the channel such as inter-symbol interference (ISI) emerging at high frequencies.

LVDS standard have been very popular among other communication standards due to its low power consumption, high noise immunity, high speed point-to-point data transmission, and good electromagnetic interference performance. LVDS is configured as a switched-polarity current generator. Optimum line impedance matching is achieved due to differential termination resistor at the receiver end of the system. Since LVDS transmits differential data, crosstalk and robustness of the link to common mode noise is extremely enhanced. The received digital data is represented with analog voltage swing at the output of the LVDS, which improves the data rate and also reduces power consumption.

The channel is the physical medium that signal passes through from transmitter side to receiver side. Transmitted signal travels through various traces before reaching its destination. With the increase in frequency, line attenuation of this channel increases due to dielectric loss and skin effect. The channel behaves like a low pass filter which deteriorates the signal quality. first pre-cursor and post-cursor samples become very large due to Pulse dispersion from low-pass filtering, which makes detecting the bits that are transmitted in a sequence. This effects also generates intersymbol interference (ISI), which is interference of the transmitted symbol with the subsequent symbol due to distortion at high data rate. As a result, to overcome the corrosive effects of the channel equalization is needed. In general, pre-emphasis technique is used in transmitter side for channel equalization.

In this thesis, 8 Gbps Low-Voltage Differential Signaling (LVDS) transmitter having controllable pre-emphasis and inductive peaking is designed for high speed

chip-to-chip communication links. The transmitter system contains of pre-driver, core LVDS driver with Common Mode Feedback (CMFB) Amplifier, delay lines, auxiliary pre-driver and Pre-emphasis blocks. It has 1.225 V output common mode voltage which is adjustable between 0.98 V and 1.330. The output swing amplitude is between 230 mV and 350 mV. It consumes 20.248 mW power at 8 Gbps data rate which yields 2.531 pJ/bit energy efficiency. LVDS transmitter is implemented in 22 nm Fully Depleted Silicon on Insulator (FD-SOI) technology and the layout occupies 0.036 mm^2 area including layout.

ÇİPTEN ÇİPE YÜKSEK HIZLI HABERLEŞME ARAYÜZLERİ İÇİN 22 nm FD-SOI TEKNOLOJİSİNDE 8 Gbps LVDS VERİCİ TASARIMI

ÖZET

Günümüzde, mikroişlemcilerin işleme hızındaki, anakartlardaki, ve optik iletim hatlarınındaki önemli gelişmeler, çip dışı veri hızının artmasına sebep olmuştur. Bu artış elektronik sistemlerde daha geniş bant-aralığına sahip olma talebini arttırmış ve kablolu giriş çıkış (I/O) sürücüleri teknolojilerinde birçok farklı yeniliği teşvik etmiştir. Yüksek hızlı kablolu veri iletimindeki güçlüklerle başa çıkabilmek için birçok farklı kuruluş tarafından çeşitli standartlar geliştirilmiştir.

Çip üretim teknolojilerindeki agresif ilerlemeler sadece yüksek hızlı giriş çıkış devrelerine olan ilgiyi arttırmamış, ayrı zamanda da veri hızı ve güç verimliliğindeki gelişmelere önemli ölçüde katkı sağlamıştır. Çip teknolojilerinin giderek küçülmesi ve daha hızlanması sayesinde giriş çıkış veri hızların artmasına ve veri işleme gücündeki artışa rağmen, bakır iletim hatlarının bant genişliği bu ilerlemelerle aynı oranda gelişmemiştir. Bu durum verinin iletildiği kanalın davranışının da hesaba katılması gerektiğini ortaya koymuştur. Sonuç olarak, verinin içerisinden geçtiği bu kanalın yıpratıcı etkilerini yok edecek, gelişmiş bir kanal dengeleme (channel equalization) tekniğinin gerekliliği geçtiğimiz yıllarda ortaya çıkmıştır. Kanalın sahip olduğu yüksek frekanslardaki yıpratıcı özelliklerden bir tanesi de semboller arası girişimdir (inter-symbol interference).

Sahip olduğu düşük güç tüketimi, yüksek gürültü bağışıklığı (noise immunity), yüksek hızlı bir noktadan diğer noktaya veri iletimi ve iyi elektromanyetik girişim performansı sayesinde LVDS standartı diğer standartlar arasında oldukça yaygın kullanılmaktadır. LVDS ürettiği akımı anahtarlayarak yönünü tayin eder. Akan akımın yönüne göre sonlandırma direnci üzerinde pozitif ve negatif bir potansiyel farkı oluşturur. Bu potansiyel farkı, LVDS'in girişinde sayısal olarak alınan verinin analog bir şekilde ifade edilmesidir. Bu potansiyel farkı sayısal sinyalin genliğinden çok daha az ve bir ortak mod voltajı üzerinde olduğundan sinyal yüksek hızlarda ve görece düşük güç tüketimlerinde gönderilebilmektedir.

İletişim sisteminin alıcı (receiver) tarafına diferansiyel (Differential) bir şekilde sonlandırma direnci yerleştirildiği için optimum bir empedans eşleşmesi sağlanabilir. LVDS vericisi (transmitter) veriyi diferansiyel bir şekilde ilettiği için çapraz karışımına (Crosstalk) ve bağlantının ortak mod gürültüsüne önemli ölçüde dayanıklıdır.

Kanal, sinyalin verici tarafından alıcı tarafına doğru içinden geçtiği fiziksel ortamdır. İletilen sinyaller, varacakları yerlere varmadan önce birçok farklı yapıdaki, uzunluktaki ve açıdaki hatlardan geçerler. Bu hatlar metrelerce uzunluğundaki bir kablo veya PCB hattı olabilir. Verinin iletim frekansı arttıkça, kanalın sönümleme oranı da dielektrik kaybı (dielectric loss) ve yüzey katmanı etkisi (skin effect) yüzünden

artmaktadır. Kanal, sinyalin kalitesini düşüren bir alçak-geçiren filtre (lowpass) gibi davranır. Kanalın yıpratıcı etkileri özellikle arka arkaya hızlıca gönderilen verileri almayı güçleştirir. Bu etkiler ayrıca semboller arası girişime sebep olur. Semboller arası girişim, iletilen bir sinyalin kendinden bir önce veya bir sonra iletilen sinyale girişmesine denir. Sinyalin özellikle yüksek frekanslarda doğru bir şekilde alınmasını engeller. Bu yüzden, kanalın yıpratıcı etkilerini ortadan kaldıracak bir kanal dengeleme tekniği gerekmektedir. Vericiler ve alıcılar için farklı farklı dengeleme yöntemleri olmakla beraber, genelde verici tarafında ön vurgu (pre-emphasis) tekniği kullanılır.

Kanalın yüksek frekanslardaki filtre özelliği en çok sinyalin yükselme ve düşme köşelerinde (rising and falling edges) gözlemlenmektedir. Bu köşeler sinyalin kendisinden daha hızlı hareket etmektedir. Bu yüzden alçakgeçiren bir kanalın içerisinden geçtikten sonra bu köşelerde bozulmalar ve bükülmeler meydana gelir. Bu bozulmaları dengelemek için tam olarak yükselme ve alçalma köşelerine müdahalede bulunmak gerekmektedir. Bu müdahale, ön vurgu devresi sayesinde gerçekleşir. Bu devre, sinyalin yükselen ve alçalan köşelerini, sinyalin kendi genliğinden daha yükseğe çıkartarak vurgu yapmış olur. Vurgulanan bu köşeler, alçak geçiren bir kanaldan geçtikten sonra güzel ve dar bir kare dalga oluşturur. Sonuç olarak, verinin filtre etkisi sonucu bükületeceği bilinen yükselen ve alçalan köşelerine yapılan vurgu, sinyalin dar bir kare dalga olarak kalmasına olanak tanır. Vurgulama işlemi genellikle, sinyalin yükseldiği ve alçaldığı zamanlarda, belirli bir süre için devreye ek bir akım uygulayarak gerçekleştirilir. Akım uygulanacak zaman aralığı, sinyalin kendisi ve evirilmiş (inverted) halinin geciktirilerek ve belirli sayısal kapılardan geçirilerek belirlenir.

Bu tezin ilk bölümünde LVDS verici tasarımını anlatmaya bir altyapı oluşturacak giriş yapılmıştır. İkinci bölümde ise LVDS tasarımının arka planından bahsedilmiştir. Tezin üçüncü bölümü, öne sürülen LVDS verici tasarımını sistem ve alt blok seviyesinde detaylı bir şekilde anlatmaktadır. Dördüncü bölümde bahsi geçen alt blokların ve sistemlerin simülasyon sonuçlarına yer verilmiştir. Son olarak, beşinci bölüm sonuç bölümü olarak hazırlanmış ve LVDS hakkında bir özet tablosu verilmiştir.

Bu tezde, çipten çipe yüksek hızlı haberleşme arayüzleri için saniyede 8 Gigabit hızındaki veriyi iletebilen, sayısal bir şekilde kontrol edilebilen ön vurgu (pre-emphasis) devresine ve endüktif zirveleme (inductive peaking) devresine sahip bir LVDS vericisi tasarlanmıştır. Verici sistemi, ön-sürücü (pre-driver), ortak mod geribildirim yükseltecine (Common Mode Feedback Amplifier) sahip LVDS sürücüsü, geciktirme hatları (delay lines), yardımcı ön-sürücü, ve ön vurgu devresi olmak üzere farklı alt bloklardan oluşmaktadır. Bütün sistemin çalışması için her bir alt bloğun kendi isterleri içerisinde çalıştığından emin olmak gerekmektedir.

LVDS çıkış ortak mod gerilimi 1.225 V olarak belirlenmekle birlikte sayısal kontrol sayesinde 0.98 V ile 1.33 V arasında değişebilmektedir. Diferansiyel çıkış genliği 230 mV ile 350 mV arasında değişmektedir. LVDS vericisi saniyede 8 Gigabit veri hızında çalışabilmek için 20.248 mW güç tüketmektedir. Bu yüzden, bit başına 2.531 pJ tüketmektedir. LVDS vericisi 22 nm FD-SOI teknolojisiyle tasarlanmıştır. Sistemin indüktör dahil tüm serimi (layout) 0.036 mm^2 alan kaplamaktadır. Bu tez, özellikle

ön vurgu sisteminin yüksek hızlarda veri iletebilmek için ne kadar önemli olduğunu simülasyonlar ile sonuçlar kısmında göstermektedir.

1. INTRODUCTION

The consistently enhancing processing speed of microprocessor, optical transmission links, motherboards, routers and intelligent hubs, etc., is extending the off-chip data rate into the gigabits-per-second range. [1] Within the final decades, increasing demand for data bandwidth across electronic systems has been met by electrical links. By increasing the data rate per pin, advancements in wireline input/output (I/O) systems have led to significant technological innovations in electronic components. [2] Many different standards have been created by various institutions to manage the difficulties of high-speed wireline data transmission. [3]

While aggressive technology scaling expanded the interest in I/O speed, it additionally contributed extremely to the improvement in power efficiency and data rate of wireline links. The use of cutting-edge technology nodes has significantly improved the speed of wireline I/O over the past ten years. [4] Wireline TRX Data rates in publications over the years can be seen in Figure 1.1.

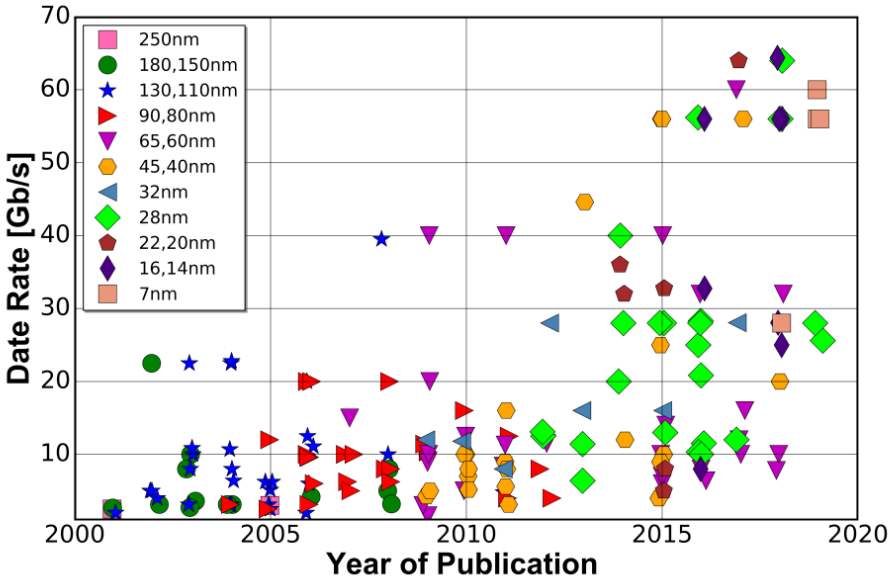

Figure 1.1 : Wireline TRX data rates in publications over years. [4]

While the technology scaling has enhanced the I/O data rates and data processing power over the last years, the bandwidth of the copper links has not been scaled in the same manner. Hence, the requirement for advanced equalization techniques has increased to be able to eliminate the high inter-symbol interference (ISI) emerging at high frequencies. [5]

1.1 Serial vs. Parallel links

Traditional IO buses have been based on parallel links such as the PCI (peripheral component interconnect), IDE (integrated drive electronics) and AGP (accelerated graphics port) interfaces. Each bit of the transmitted data word in these interfaces required one physical conductor, which results in wide data buses that were generally limited in speed to less than 100 Mb/s. [6] In the recent years, increasing microprocessor clock frequencies, the transition to multicore processors and system on chips (SoCs) made it mandatory to access the data quicker than ever before. [7]

Since several high-speed links, such as fiber-optic and coaxial cables, have historically operated serially due to costs associated with cables and synchronization issues with increasing transmission speeds and distances, the switch to serial links was only logical. As well as expanding the IO data transfer capacity, serial links are also efficient in terms of cost, area and power. They likewise take out a few issues faced in parallel links such as data skew, crosstalk, and clock transmission. [8,9] Hence, serial communication has turned into the answer for higher and more efficient data transmission to satisfy the needs and trends of higher capacity of communication technology. [10]

1.2 Serial High-Speed Wireline Link

Typical diagram for a Serial High Speed Wireline link can be seen in Figure 1.2. The serializer serializes the parallel low-speed input into high speed data and sends this data to an output driver. This driver transfers the data to the channel in a certain data format. To obtain the parallel data again on the receiver side, the received signal is transformed back to digital data and deserialized. Transmitter can have its own clock

generation and distribution. The Receiver, can receive the clock from transmitter or clock can be synthesized internally utilizing clock-data recovery (CDR) circuits. [2]

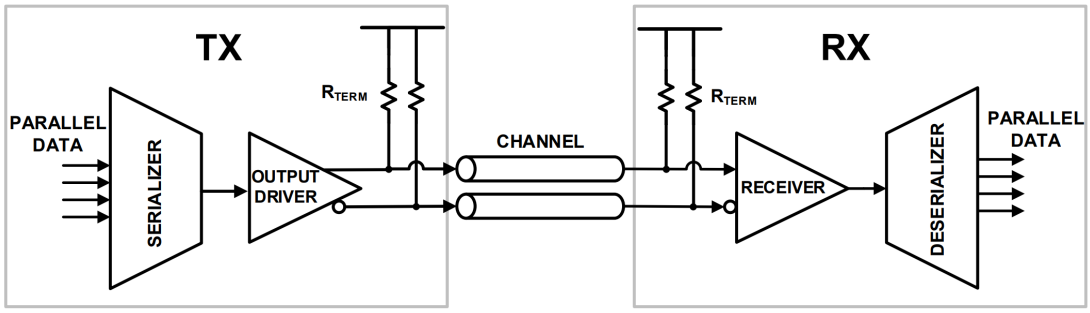

Figure 1.2 : Typical diagram for Serial High Speed Wireline link. [2]

1.3 High Speed Transmitter Driver

There are two fundamental driver types which are current-mode and voltage-mode. In the current-mode driver, load resistance R generally dominates the output impedance of the driver. Therefore, it yields good impedance matching across various output swings. [11]

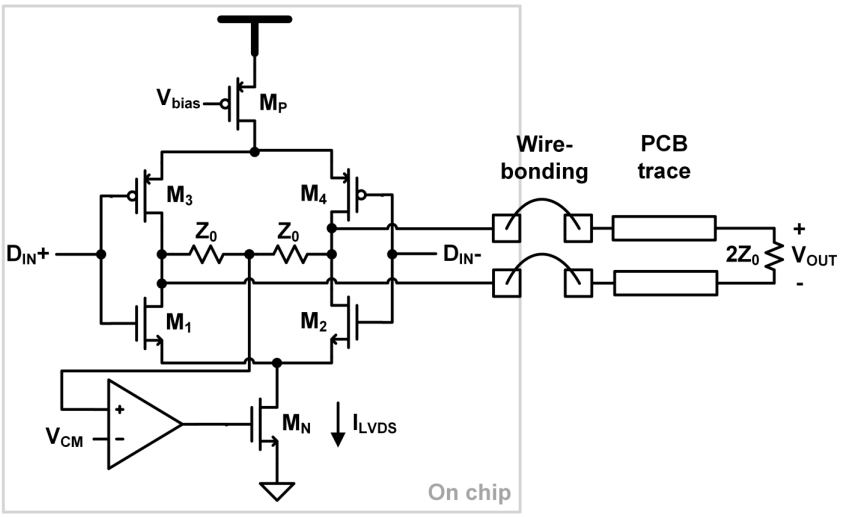

Figure 1.3 : Schematic diagram of LVDS with CMFB amplifier. [21]

On the other hand, since there is no spilt current path, the voltage-mode driver consumes less current. This change in the current consumption mainly occurs due to the location of the termination relative to the signal path. For instance, termination is placed in parallel with signal path in current mode driver. but placed in series with

signal path in voltage-mode drier. As a result, source-series terminated (SST) driver can also be used instead of voltage-mode driver. [11]

One of the current-mode driver architectures is the push-pull driver. This driver is also called LVDS driver, as it is widely used in low-voltage differential signaling (LVDS) standard. A general schematic diagram of the LVDS driver with common mode feedback amplifier can be seen in Figure 1.3.

Another current mode driver is current-mode logic (CML) driver and its schematic diagram can be seen in Figure 1.4. Parallel termination technique is used as it is also a current-mode driver. since the termination resistors are placed between supply voltage and the differential output nodes, common mode voltage of this driver is higher than VDD/2, which helps to provide enough headroom to keep the current source in the saturation region. CML architecture is more suitable for low supply operations compared to LVDS due to having only single current source. However, on the other hand, it has worse PSRR performance compared to LVDS driver. [2]

In summary, LVDS has less power consumption and better PSRR performance compared to CML. On the other hand, CML can operate at higher frequencies and also it can operate at lower supply voltages. However, for this project the supply voltage is 1.8 V. If the CML driver is used, the common mode will be too high. Moreover, power consumption for the same frequency will be higher. Therefore, due to these advantages at this supply voltage and the desired data rate, LVDS was chosen as a driver topology.

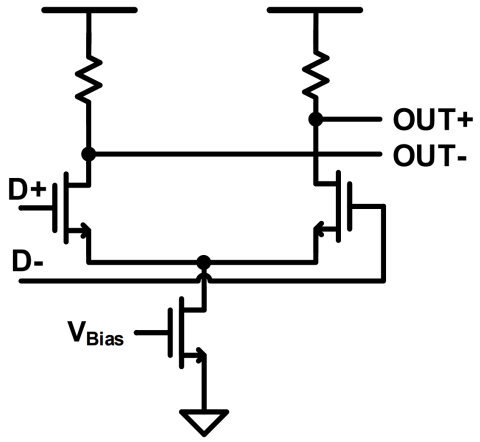

Figure 1.4 : Schematic diagram of current-mode logic (CML) driver. [2]

1.4 Purpose of Thesis

The main purpose of this thesis is to design a LVDS transmitter having digitally controllable pre-emphasis and being capable of operating at 8 Gbps data rate. LVDS transmitters are blocks that transmit high speed signals through a link. This link and the channel that the signals passing through have negative effects on the signal. Therefore. LVDS transmitter can handle the filtering effect of the channel and nonideality coming from the communication link. Moreover, each sub-blocks of the LVDS have their own requirements such as stability, gain and bandwidth. One of the other aim of this thesis is to give system and block level explanations about the proposed LVDS design.

1.5 Literature Review

Due to tremendous increase of high-speed applications and the performance demands on communication systems, higher data rates, more functionality, and processing speeds are needed. Low-voltage differential signaling (LVDS), defined in ANSI/TIA/EIA-644-A [12], is a very popular standard that meets these requirements.

LVDS standard have been very popular among other communication standards since it has low power consumption, high noise immunity, high speed point-to-point data transmission, and good electromagnetic interference performance. Output common mode voltage was defined between 1.125 V and 1.375 V by the this standard. Moreover, Amplitude swing was also defined between 250mV and 450mV, which helps to LVDS consuming less power compared to other topologies. [12]–[14]

LVDS is configured as a switched-polarity current generator utilizing differential data transmission. Optimum line impedance matching is achieved with the help of the differential load termination resistor at the receiver end. [15] Robustness of the link to common mode voltage changes and crosstalk is significantly improved by the differential transmission, which tolerates the reduced noise margin. [1]

LVDS transmitter consist of a pre-driver isolating the internal circuitry from the output driver circuit which can have a very high input capacitance. [16]–[18] and to meet the requirements of the standard, output common mode voltage of the driver should be

controlled by a loop. Hence, common mode feedback amplifiers are mainly used for this purpose. [1,15,17,19]–[22]

LVDS transmitter will transmit the data through a channel which might be a long cable or PCB routing. This is the channel that the signal passes through. Therefore, this channel will limit the bandwidth of the LVDS system. To overcome this problem channel equalization is needed. In general, to equalize the channel in transmitter side, pre-emphasis circuit is utilized. [23]–[27]

1.6 Organization of Thesis

This thesis is organized as follows: In Chapter 2, background of the LVDS is discussed. A brief introduction about LVDS is given. Channel effects and equalization, and pre-emphasis, which is a crucial part for this thesis are explained. In Chapter 3, proposed LVDS transmitter design is discussed. While the Channel model, testbench and digital control scheme of the LVDS are mentioned in system level, each sub-block is explained in detail. In addition, layout of the LVDS is shown. In Chapter 4, post-layout simulations of the LVDS are provided. Finally, a brief conclusion is made and the future work is discussed in Chapter 5.

2. LVDS Background

LVDS technology transmits differential data. Therefore, it has a significant advantage over single-ended scheme since it is less susceptible to common-mode noise. LVDS has been a proper choice for many applications due to its brilliant noise immunity, minimal EMI and low power consumption. [28]

Pre-driver, driver, and amplifier circuitry for common mode feedback are the main blocks of LVDS transmitter. [29] These blocks can be seen in Figure 2.1.

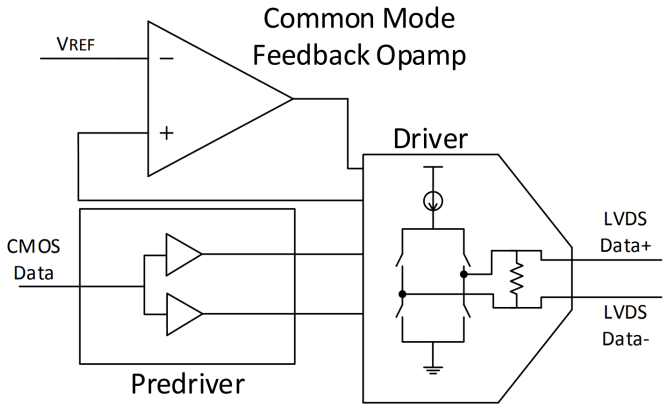

Figure 2.1 : Main blocks of the LVDS transmitter. [29]

Pre-driver might include conversion from single ended data to differential data. It is an amplifier in general which drives the gate capacitance of the core LVDS driver. It isolates the big gate capacitance of the core driver. Driver circuit is the core of LVDS transmitter. Driver is designed as current source with a switched polarity. [30] This nominal current source supplies 3.5 mA in conventional LVDS driver. The Main working principle is to steer the current in different directions so that it generates positive and negative voltage differences across termination resistor. Common mode feedback amplifier is used to keep the output common mode of the LVDS driver constant. It forms a loop with core driver. Therefore, stability of this loop must be considered. In general, compensation methods are used to make this loop stable.

2.1 Channel

The channel is the physical medium that signal is transmitted through from transmitter to the receiver. The signal has to traverse a number of different traces before arriving to destination. When the frequency increases, line attenuation increases as well due to skin-effect and dielectric loss along the long backplane traces. [31] While the signal is lowpass filtered due to line attenuation, sometimes short traces such as vias or connectors can bring more corrosive effects. These short traces can yield huge impedance mismatches and cause reflections that can dramatically deteriorate the signal quality. [32] Figure 2.2 shows a nice example of typical channel attenuation behaviour (S21 parameter). This figure also shows that, via stubs can make the attenuation of the channel even worse.

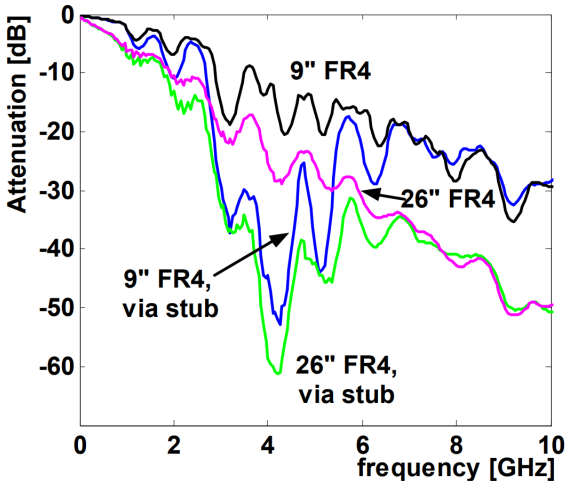

Figure 2.2 : Attenuation of the channel. [32]

The frequency response of the channel can be modeled approximately accurately with all these components in the system. In general, these channels behave like low pass filter, which means narrow pulse signal at the input of the channel will be dramatically attenuated and will be much wider at the output of the channel. This pulse dispersion from low-pass filtering make the first pre-cursor and post-cursor samples very large. These effects would make detecting the bits that are transmitted in a sequence very challenging. [31] This situation also causes intersymbol interference (ISI). [33] ISI is interference of the transmitted symbol with the subsequent symbol because of distortion at high data rates. [34]

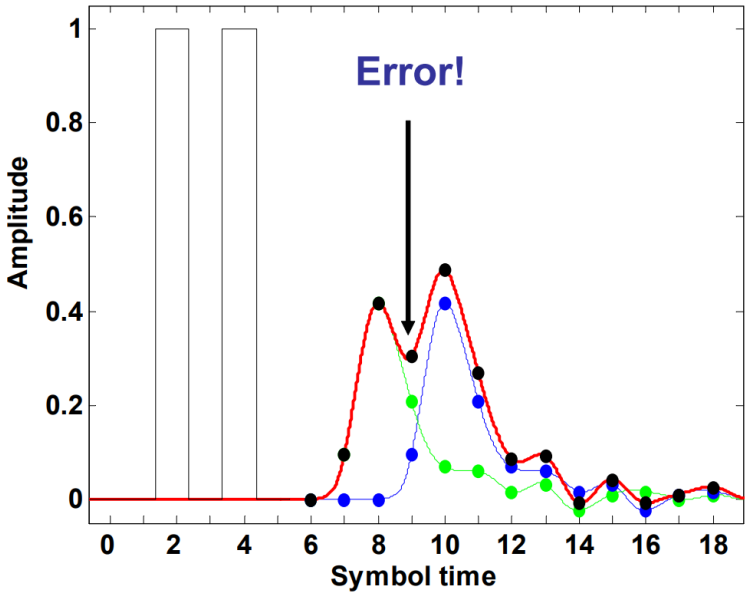

Figure 2.3 : ISI example for two input pulse signal. [35]

A nice example of ISI is shown in Figure 2.3. [35] It can be seen that two separate pulse signal is applied to a channel. The signals are distorted and become wider. If only the first pulse signal was sent, the green signal would be the outcome. Similarly, if only second pulse was sent, the blue signal would be the outcome. However, when two signal are sent together, the post cursors of the green signal interfere with the blue signal, which generates the red signal. the error caused by the intersymbol interference can easily be seen in this figure.

2.2 Pre-emphasis

To overcome the negative effects of the channel equalization is needed. Pre-emphasis is a channel equalization technique that is used in the transmitter side in general. A pre-emphasis circuit is utilized to compensate the attenuation of high-frequency components of signal due to limited bandwidth of the channel. For the channel having less attenuation, or for the slower operating rates of the LVDS this pre-emphasis circuit can be turned off to reduce power consumption. [26]

A pre-emphasis circuit can overcome the negative effects of the channel by providing additional current on each bit transition to speed up rise/fall time of the signal. [25] In other words, pre-emphasis block apply an additional current for specific amount

of time when the signal is rising or falling which emphasis this fast edges. This emphasized edges seems much more like a regular pulse signal after low pass effect of the channel. Schematic diagram of the pre-emphasis can be seen in Figure 2.4. In this figure, additional current path was drawn with red arrows.

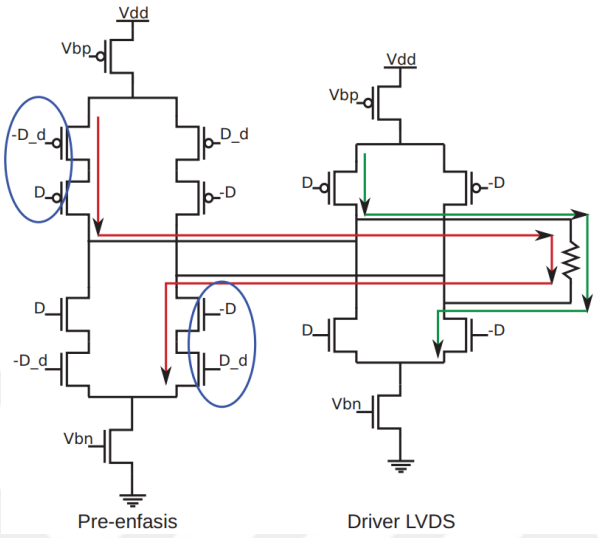

Figure 2.4 : Schematic diagram of the pre-emphasis with LVDS core. [25]

3. Proposed LVDS Transmitter

In this chapter, the proposed LVDS transmitter design will be discussed. Working principals of sub-blocks will be mentioned and schematic diagrams of them will be shown. Each sub-block will be considered in a separate section. layout implementation of each block will be also shown. However, the results of them will be provided in the results chapter. Channel model that was used in the system and the testbench were mentioned before the system level description of LVDS.

3.1 Channel Model

Channel model is crucial for the communication systems. It defines how the transmitted signal will be distorted over this channel. Therefore, It is important to have a proper channel model. The channel is single ended 50 ohm terminated. The s-parameter results for this channel were obtained in the laboratory and lumped element model was generated in the cadence thanks to s-parameter results. 1 inch FR4 Channel Lumped element model can be seen in Figure 3.1.

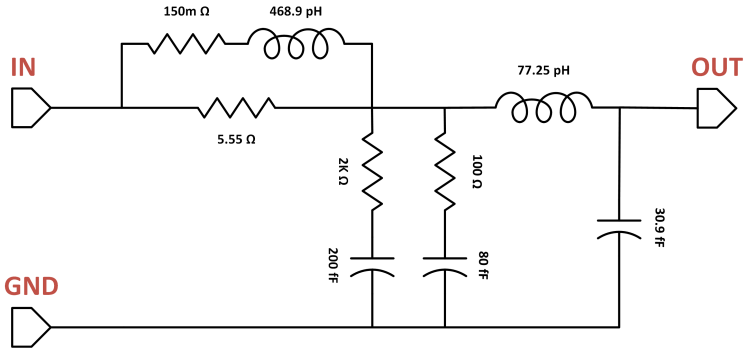

Figure 3.1 : 1 inch FR4 channel model.

It was decided to use 8 inch FR4 channel for our simulations. 8 inches channel was built by adding 1 inch FR4 channels in series. A differential channel was used since the output of the LVDS is differential. Differential 8 inch FR4 channel can be seen in Figure 3.2. The channel was terminated with differential 100 ohm on the RX side.

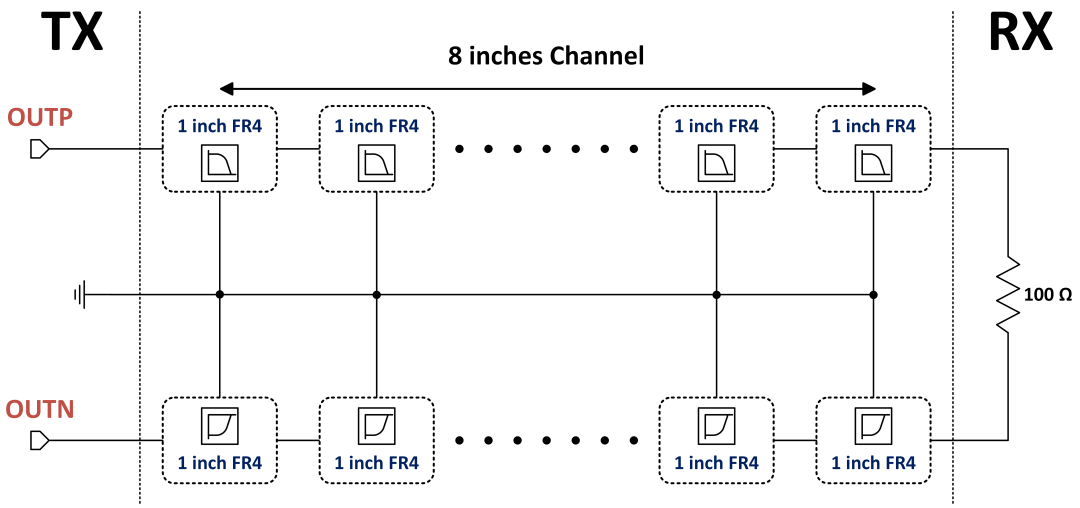

Figure 3.2 : 8 inch FR4 channel.

3.2 Testbench

Testbench of the LVDS TX driver can be seen in Figure 3.3. The testbench can be examined in 3 different sections which are transmitter, channel and receiver side. Transmitter side contains LVDS transmitter driver. controllable peaking inductor, ESD diodes, and pads. Pads are modeled as differential cap in the output. After pads, channel is coming, which distorts the transmitted signal. This 8 inch channel was terminated with the differential 100 ohm. This termination might be off or on chip. A load capacitor was added in parallel to termination resistance to model the pad capacitance and the gate capacitance of receiver.

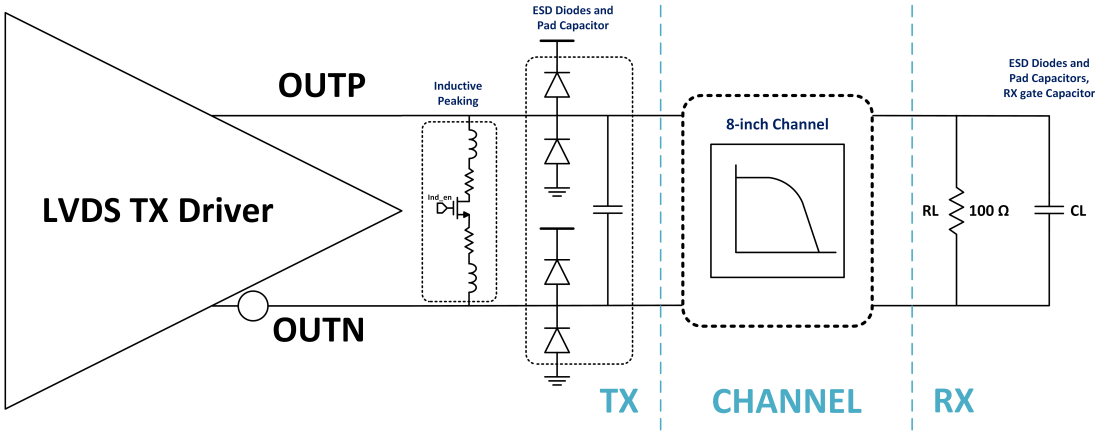

Figure 3.3 : Testbench for LVDS.

3.3 LVDS Digital Control Scheme

LVDS transmitter has lots of different digital bits to control different features. Although this transmitter was designed for 8 Gb/s which is the fastest data rate, it can operate for lower frequencies. Every current source in each sub-block is digitally controllable in order to change the current consumption for various transmitter frequencies. In addition to that, due to the same reason pre-emphasis current sources are also controllable. These current sources can be adjusted to make PVT compensation also. Delay lines in the transmitter have controllable delays to ensure that the signals are well located across the PVT. The digital control bits and their functions can be seen in Table.3.1

Table 3.1 : Control bits for LVDS transmitter.

Control Bits	Function
pd_en	Power down the LVDS transmitter.
ind_peak_en	Enables the inductive peaking
pre-emph_en	Enables the pre-emphasis.
pre_drv_cur_ctr<1:0>	Adjust the current in pre-driver.
lvds_drv_cur_ctr<1:0>	Adjust the current in LVDS driver.
pre-emph_drv_cur_ctr<1:0>	Adjust the current in pre-emphasis.
dly_early_ctr<1:0>	Adjust the delay in delay early stage.
dly_late_ctr<1:0>	Adjust the delay in delay late stage.
vcm_ctr<4:0>	Adjust the the common mode voltage

3.4 Transmitter Design

Schematic diagram of proposed LVDS transmitter can be seen in Figure 3.4. Transmitter have several main sub-blocks which are data path, pre-driver, LVDS driver with common mode feedback amplifier, delay stages, auxiliary pre-driver, pre-emphasis, and controllable peaking inductor. Even though each block is briefly mentioned in this section, they will be discussed in detail in separate sections.

Data is sampled with a clock in the data path sub-block. There are D-type flip flops and dummy mux blocks in order to generate dummy delays, which tries to equalize the delay between data line and pre-emphasis line. Pre-driver is a fully differential amplifier with resistive and cross-coupled load. This stage drives the LVDS core inverters. LVDS core drives the pad capacitance and the channel.

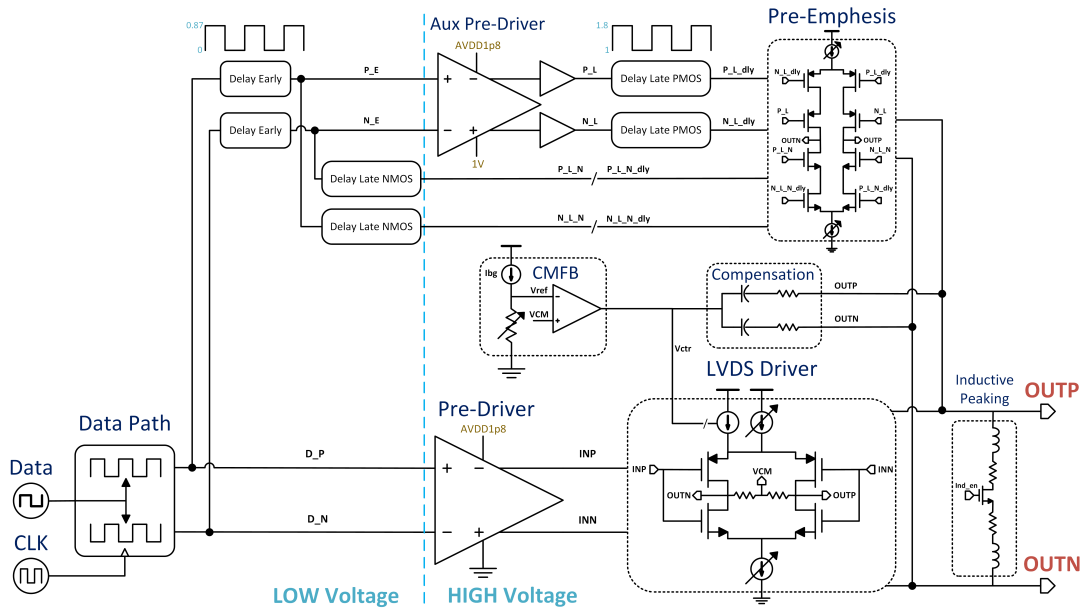

Figure 3.4 : Schematic diagram of proposed LVDS driver.

The Main principle of the core LVDS driver is steering the current across the 100 ohm resistor according to the data. For instance, if the data is "1", the current will be flowing through resistor such that it generates a positive voltage difference between outp and outn nodes. On the other hand, if the input data is "0" the current flows in the opposite direction generating a negative voltage difference between outp and outn nodes. Common mode of the LVDS driver is set by the common mode feedback amplifier (CMFB amplifier). This common mode can be digitally controlled and it is set to 1.225 V, which suits LVDS protocol.

A pre-emphasis is implemented to equalize the effects of the channel. The pre-emhesis block applies an additional current to the output for a specific amount of time which was determined by the delay in the late delay blocks. Pre-emphasis simply injects an auxiliary current at the time that the signal is in the rising edge and the falling edge to decrease the filtering effects of the channel to these edges. Even though it increases the total current consumption, it enhances the eye diagram performance.

However, there was a huge issue specifically for this proposed pre-emphasis block. Core transistors of this process were used in order to minimize parasitic capacitors and maximize the speed of the transmitter. Core transistors in this process have a

limit of 880 mV for their drain-source and gate-source voltage difference due to stress limitations. However, analog supply is 1.8 V for the pre-emphasis block and the digital supply is 0.87 V. Therefore, 0.87 V digital signal was not able to cut off the PMOS transistors in the pre-emphasis block. The solution was adding an auxiliary pre-driver shifting voltage level to 1.8V and 1V, which makes it possible to switch on and off the PMOS transistors in the pre-emphasis. 1 V was generated in the chip. These additions can be seen in Figure 3.4.

A switchable inductor with series resistors was placed to the output of the LVDS transmitter to achieve inductive peaking, which enhances the bandwidth and improve eye diagram performance. Inductor was cut in the middle and a transistor is placed to enable and disable the inductive peaking.

3.4.1 Input data path

Schematic diagram of the data path can be seen in Figure 3.5. Data path consist of 2 D type flip-flop which sample data and inverted version of the data to create differential signal from a single ended data input. In early and late delay cells there is a MUX to select different delay options. This MUX causes also additional delay. Hence, to match the delays between delay lines and data path a dummy MUX is added.

At the final end of the circuit there is a buffer chain to drive the following circuits. Layout of a single D type flip-flop can be seen in Figure 3.6. In addition, layout of the whole data path can be seen in Figure 3.7. Digital cells are placed at the closest location in order to minimize the routing parasitics and dummy cells are added to the layout to establish matching.

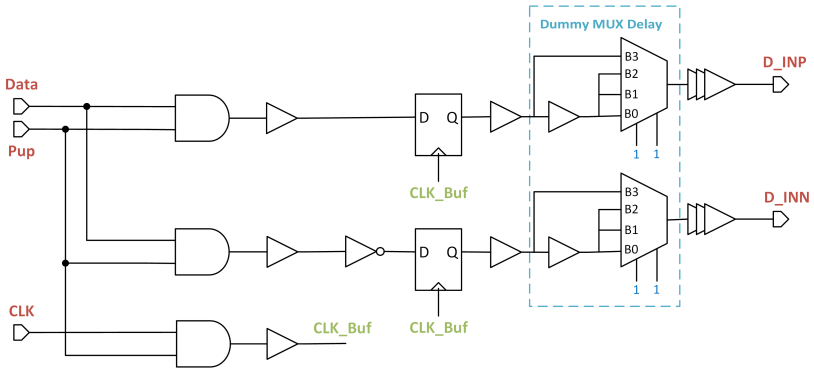

Figure 3.5 : Schematic diagram of data path.

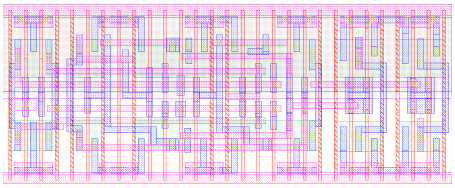

Figure 3.6 : Layout of D flip-flop.

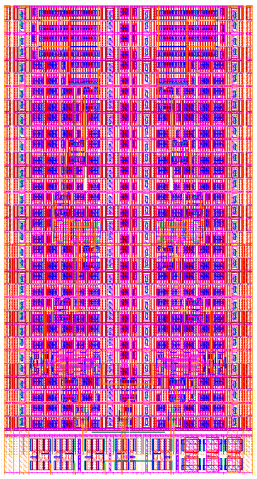

Figure 3.7 : Layout of data path.

3.4.2 Bias voltage generation

Two different bias generation circuits can be seen in Figure 3.8. A biasing topology like in Figure 3.8 a) is commonly used. In this topology, MN1 and MP1 should provide enough gate voltage to have proper headroom for two cascaded transistors. This generated headroom will be shared between two transistors according to the resistor value because resistor defines the how much voltage drop will be for a desired current from the gate voltage of MP1. In summary, while the MP1 and MN1 are deciding the headroom for cascaded transistors, the resistor (and the sizing of the transistors) define the headroom for MP1 or MN1 because headroom for these transistors is just one VGS lower or higher than bias voltages.

This technique is commonly used for regular CMOS processes because there is no chance to play with the bulk (back gate in 22nm FD-SOI) voltage. However, in the 22nm FD-SOI process, it is possible to connect back gate to an arbitrary voltage without concerning the diode between bulk and the source. Hence, threshold of the

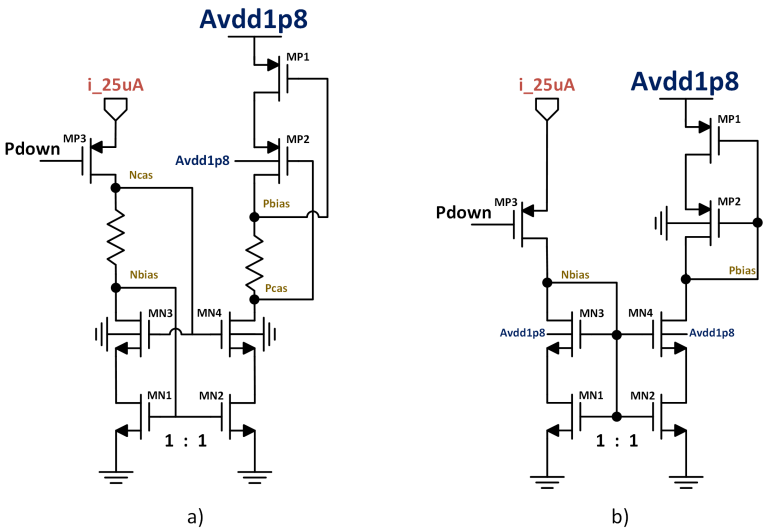

Figure 3.8 : Bias generation circuits

transistors can be adjusted with bulk voltage also. As a result, a virtual resistor can be created thanks to threshold voltage adjustment. It can be seen that in the Figure 3.8 b), back gate of the cascoded NMOS transistors (MN3, and MN4) are connected to Avdd1p8 (1.8 V) to reduce the threshold voltage of these transistors. Similarly, backgate of the PMOS transistor is connected to GND to reduce the threshold voltage. Therefore, the gate of the biasing transistor and the cascoded transistor are connected to each other thanks to this technique which enables a single bias voltage for all current sources rather than having two.

3.4.3 Pre-driver

Schematic of the pre-driver can be seen in Figure 3.9. Pre-driver is a fully differential amplifier with resistive and cross-coupled load. MN1 and MN2 are input differential pairs. MN1, MN2, MN3, MN4, and MN5 transistors are core transistors which have voltage limitations. Therefore, to protect the differential pair a cascode pair was added. To generate a bias voltage for this cascode pair a small amount of current was forced to flow across a diode connected NMOS (MN5) transistor. Therefore, headroom for input differential pair tried to be kept constant across PVT corners. MP4 transistor is added to cut the connection between supply and the circuit. R1 resistor is put to reduce the output common mode voltage. R2 resistors and the MP1 and MP2 transistors are also defining output common mode voltage and defining gain of the pre-driver.

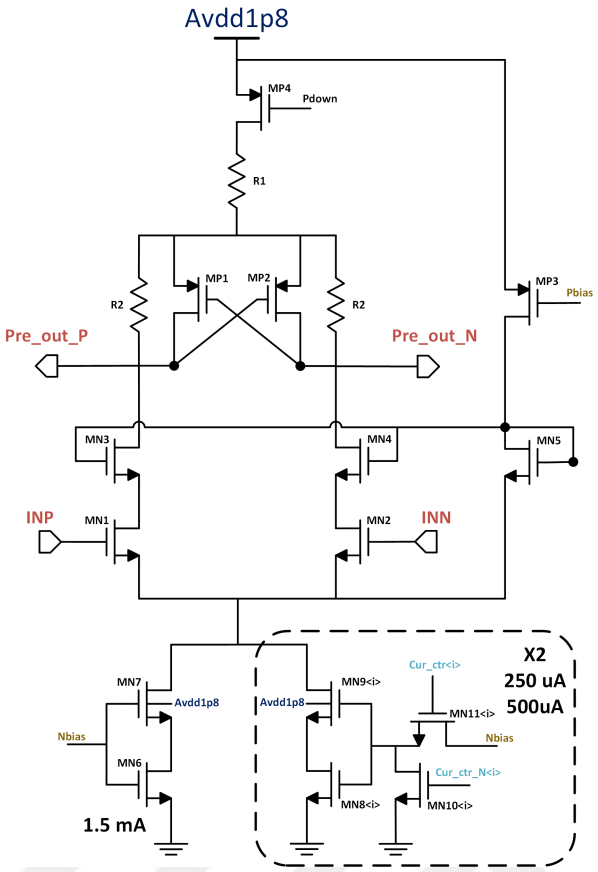

Figure 3.9 : Schematic of pre-driver.

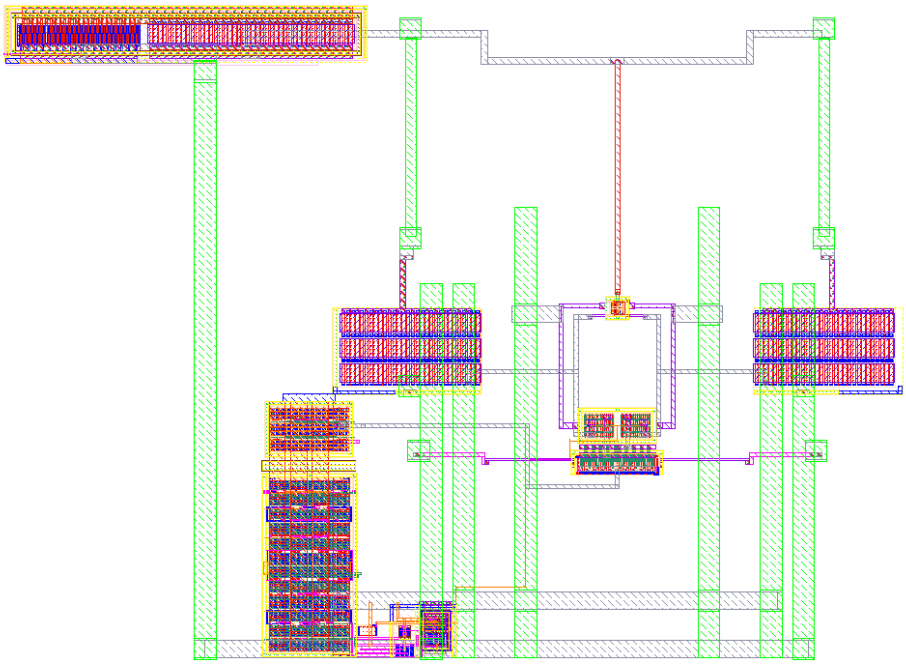

Figure 3.10 : Layout of pre-driver.

Layout of the pre-driver can be seen in Figure 3.10. For each high speed block, in order to minimize the routing parasitics high speed paths (such as input differential pairs etc.) are located very close to each other. To achieve this, the current sources are located in different places rather than locating them as in the schematic. The nodes that current sources are connected to can be assumed as virtual grounds. Hence, these nodes can be assumed as slow nodes which provides an opportunity to place them far places in the layout increasing routing parasitics. However, on the other hand, increasing the capacitance in these virtual grounds reduces CMRR performance which might affect the circuit performance as well.

3.4.4 LVDS core and common mode feedback amplifier

Figure 3.11 shows the schematic of LVDS core driver. Input of this stage comes from pre-driver. Core design is a differential inverter which decides the direction of differential current flow. Fundamental working principle can be understood much more easily with extreme voltages. For instance, if INN voltage is "0" (which means MN1 is completely cut off. In practice, it is more than 0 V. INN voltage can be considered as "0" when V_{INN} < headroom voltage of cascode current sources + V_{GS1}), MN1 is cut off and MP1 became like a shorted switch which passes all of the differential current across itself through OUTP. Similarly, when INP is considered as "1", MP2 is cut off and MN2 passes all of the differential currents across itself. Hence, the current flows through MP1 and MN2 generates positive voltage at the output due to 100 ohm termination.

This analogy helps to understand the working principle of the core LVDS driver. However, in practice, this is an analog circuit rather than digital. Therefore, the input has its own common mode voltage, which was determined by pre-driver and output common mode voltage which was determined by common mode feedback amplifier.

Common mode voltage was sensed from the middle point of two high impedance resistors. The sensed voltage is applied to a CMFB amplifier. Schematic of the CMFB amplifier can be seen in Figure 3.13. A simple 5 transistor OTA topology was used for CMFB amplifier. This amplifier provides an output voltage controlling current source in the LVDS core such that VCM voltage is equal to Vref voltage. This reference

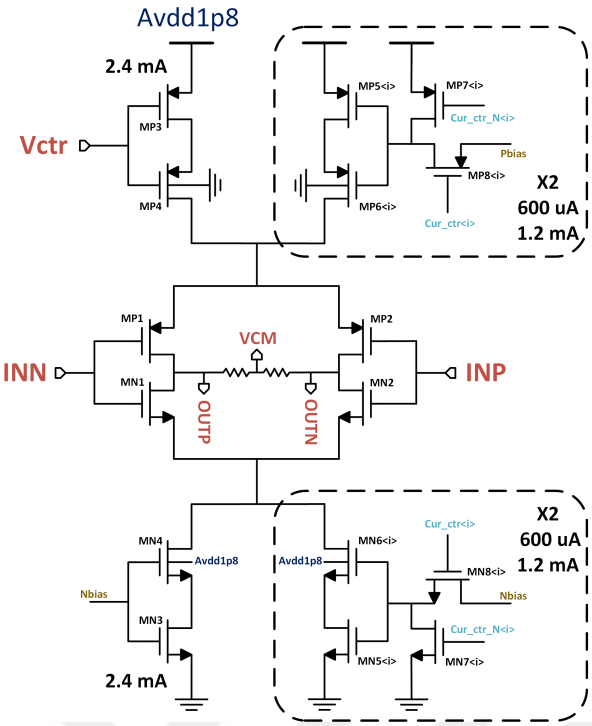

Figure 3.11 : Schematic of LVDS core.

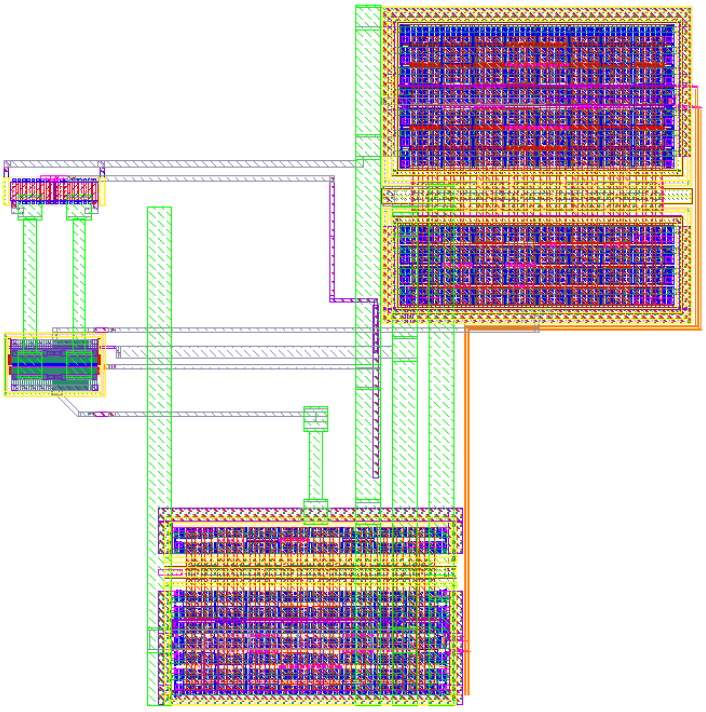

Figure 3.12 : Layout of LVDS core.

voltage was generated by passing a current coming from a bandgap reference circuit through a digitally controllable resistor ladder. Therefore, common mode voltage for LVDS core can be controlled with 5 bits to get 1.225 V for each corner and also to have several output common mode options to obtain the requirements of many receiver in the market.

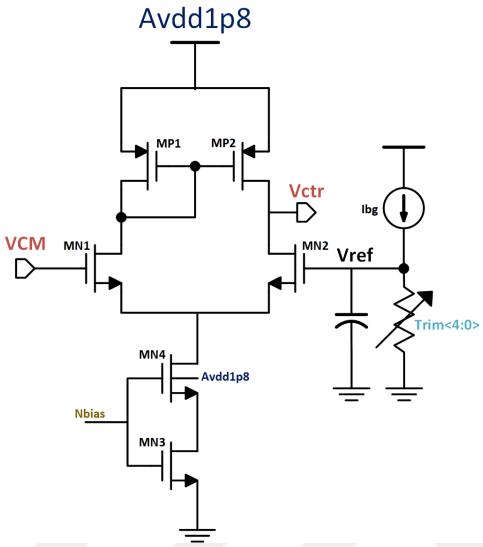

Figure 3.13 : Schematic of CMFB.

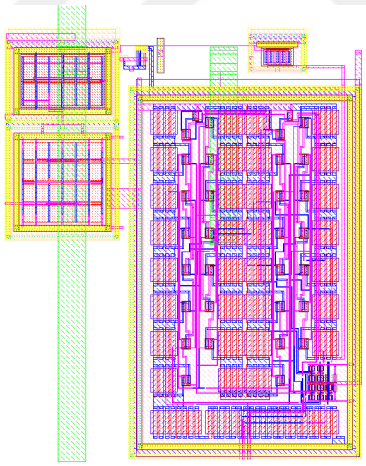

Figure 3.14 : Layout of CMFB.

Stability is one of the main concerns for this CMFB amplifier. Hence series capacitor and resistor are added between Vctr node and differential outputs to add a zero to the loop as in Figure 3.4. Layout of the LVDS core and the common mode feedback amplifier can be seen in Figure 3.12 and Figure 3.14 respectively.

3.4.5 Pre-emphasis

Pre-emphasis is needed in order to neutralize the filtering effect of the channel. The Main motivation of the pre-emphasis is to generate a signal which will look like a perfect square wave after the filtering effect of the channel. If a perfect square wave signal passes through a channel rising and the falling edges of this signal will be distorted. Some of the cosine signals will be filtered out from a perfect square wave increasing the rising and the falling time of the signal. Pre-emphasis is mainly utilized in the transmitter side.

Even though the filtering effects and the behavior of the signal can be examined in the frequency domain, analyzing this proposed pre-emphasis circuit in the time domain will be much more beneficial. The main working principle of this block is to provide an auxiliary current for LVDS core current for a finite period of time at a specific time (at some point in the rising edge and the falling edge of the signal). Therefore, it is needed a circuit such that it will provide a current just for a period of time and after this time it will not affect the system. How the pre-emphasized signal seems can be seen in the Results section. Moreover, it can all be seen how the pre-emphesized signal become much more like a square wave after passing the channel.

Some delay lines are needed to generate finite amount of delays for the pre-emphasis block. In this proposed design, there are two different delay segments such as early and late delay lines. Delay early block is in the low voltage domain. Voltage level is between 0 V and 0.87V. Late delay line defines how long the pre-emphasis current is provided to output.

For the proposed pre-emphasis block there was a crucial problem with voltage levels. Pre-emephesis block is supplied with an analog voltage supply having 1.8 V. However, the digital supply is 0.87 V. Hence, when the digital signal coming from the late delay line comes to the pre-emphasis block, PMOS transistors were never cut off as the 0.87 V signal was not able to cut off the transistors. Using a simple level shifter was also impossible since the transistors that were used in the pre-emphasis block were core transistors having 0.88 V limitations for their VDS and VGS voltages. Therefore, digital signal from 1 V to 1.8 V was needed for PMOS transistors.

To obtain the required digital signal, an auxiliary pre-driver was designed, which shifts the low voltage digital signal to an analog voltage domain changing from 1 V to 1.8 V. Then, special buffers and digital gates were designed having 1 V for their VSS voltages. This 1 V voltage was generated inside of the chip by adding a diode connected NMOS transistor on top of the digital supply. Digital supply comes from a Buck converter inside the chip. As a result, there are two different late delay lines separately for NMOS transistors and PMOS transistors. Each sub-block of the pre-emphasis is discussed separately in each sub-section. Timing diagram of the pre-emphasis block is discussed in sub-section also.

3.4.5.1 Early and late delay lines

Circuit diagram of delay lines can be seen in Figure 3.15. There is a fixed amount of delay in this block which is the summation of AND delay MUX delay and the BUFFER chain delay. In addition, thanks to MUX different delay values can be achieved. There are 4 different delay values for both early and late delay coming from BUFFER delays. The structure for delay lines are similar for both early and late delay lines.

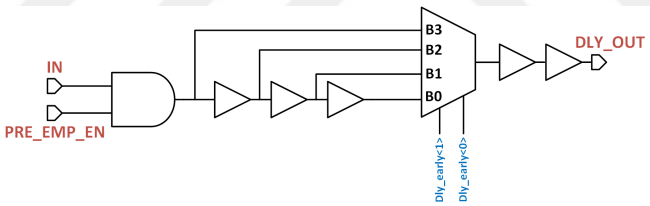

Figure 3.15 : Diagram of delay lines.

3.4.5.2 Auxiliary pre-driver

Figure 3.16 shows the schematic of the auxiliary pre-driver. This block was needed to shift the low voltage digital signal to high voltage analog domain. Output of this block swings between 1.8V and 1V. Similarly to main pre-driver, this is a fully differential amplifier with resistive load. Cascode transistors were added since the input differential pair is core transistor. Core transistors were used in order to minimize the parasitics. 1.1 V was generated inside the chip and applied to the gate of the cascode providing nice headroom for the circuit. This block has also controllable

current sources and the current is less than the main pre-driver current as the gate capacitances of pre-emphasis is less than the gate capacitance of LVDS core drivers.

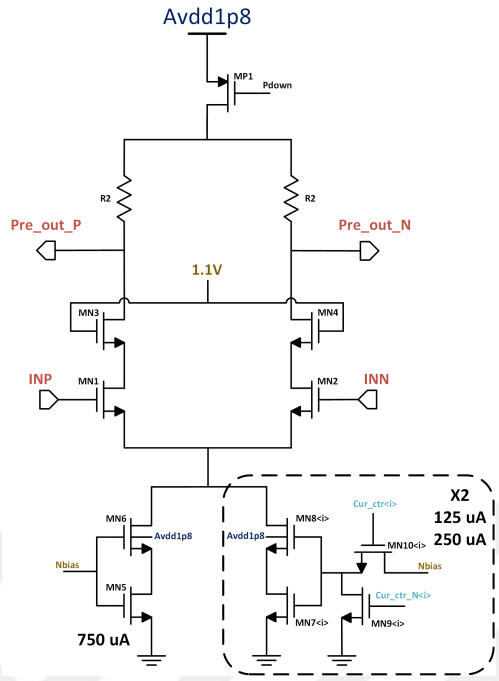

Figure 3.16 : Schematic of auxiliary pre-driver.

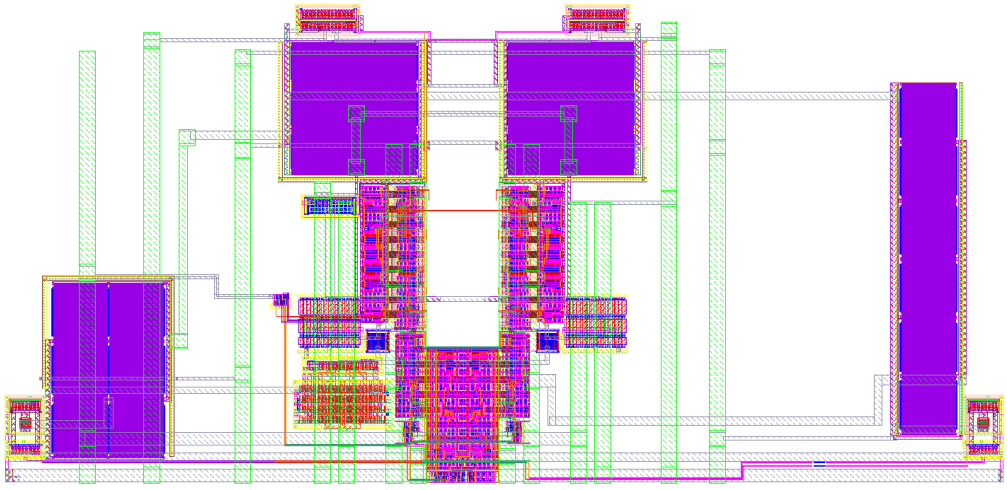

Figure 3.17 : Layout of delay lines, auxiliary pre-driver, and 1V generation.

After low voltage digital signal is shifted to high voltage analog domain, BUFFERS are added in order to sharpen the rising and the falling edge of the signal. These buffers have 1 V instead of 0 V and they are connected to late delay lines for PMOS transistors. Layout of the data path, delay lines, auxiliary pre-driver and diode

connected transistors generating 1 V with capacitors can be seen in Figure 3.17. Delay lines and data path are closely located to minimize the routing parasitics. While current sources in the auxiliary pre-driver are located relatively far distances to delay lines input differential pairs, cascode transistors and resistors (considered as fast nodes) are located as close as possible to the delay lines.

3.4.5.3 Pre-emphasis core

Schematic of pre-emphasis core can be seen in Figure 3.18. This block consists of cascoded NMOS and PMOS pairs having signals at their gates. These signals are inverted and delayed, whose diagrams can be seen in the separate section. Current sources in this block are also digitally controllable.

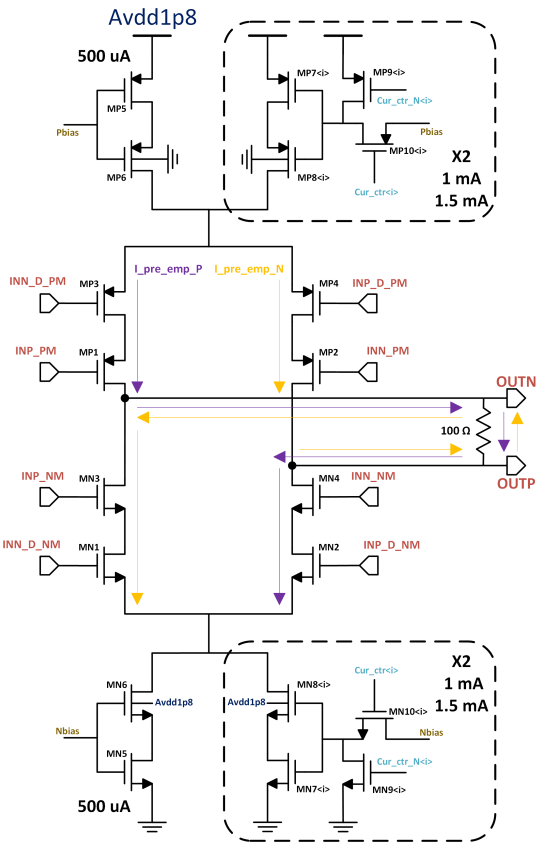

Figure 3.18 : Schematic of pre-emphasis core.

According to the received signals at the gates, for a period of time MP1, MP3, MN4, and MN2 transistors are conducting the current which is drawn with purple in the Figure. For this period of time an auxiliary current is added to the output current which passes through 100 ohm termination resistor. On the other hand, MP2, MP4, MN1,

and MN3 transistors are conducting current which is drawn with yellow arrows in the Figure. Therefore, it can be seen that according to the input signal there are currents are flowing into two different directions and adding up to the core LVDS driver current, which generates positive and negative voltage over 100 ohm termination resistor.

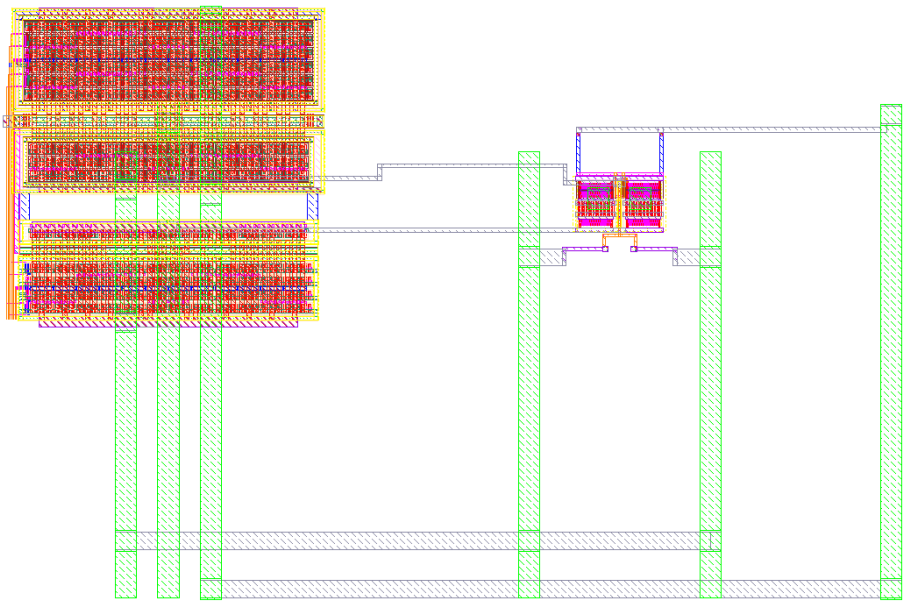

Figure 3.19 : Layout of pre-emphasis.

Layout of the pre-emphasis can be seen in Figure 3.19. High speed path of this sub-block is located closest location to other high speed paths like in other sub-block layouts. Similarly, current sources are located in a appropriate places according to the floor plan.

3.4.5.4 Pre-emphasis timing diagram

Figure 3.20 shows the signal diagram for pre-emphasis. Understanding the signal diagram for pre-emphasis helps to understand the working principle of the pre-empheis itself. Pre-emphasis block with delay lines works like an XOR digital gate. It can be seen that the current only flows when the input signals are all zero for PMOS transistors and all one for NMOS transistors. Therefore, when the pre-emphasis block is considered as a black box and just the function of the block is considered, it is a block that provide a current for a time period that was determined by XOR behaviour.

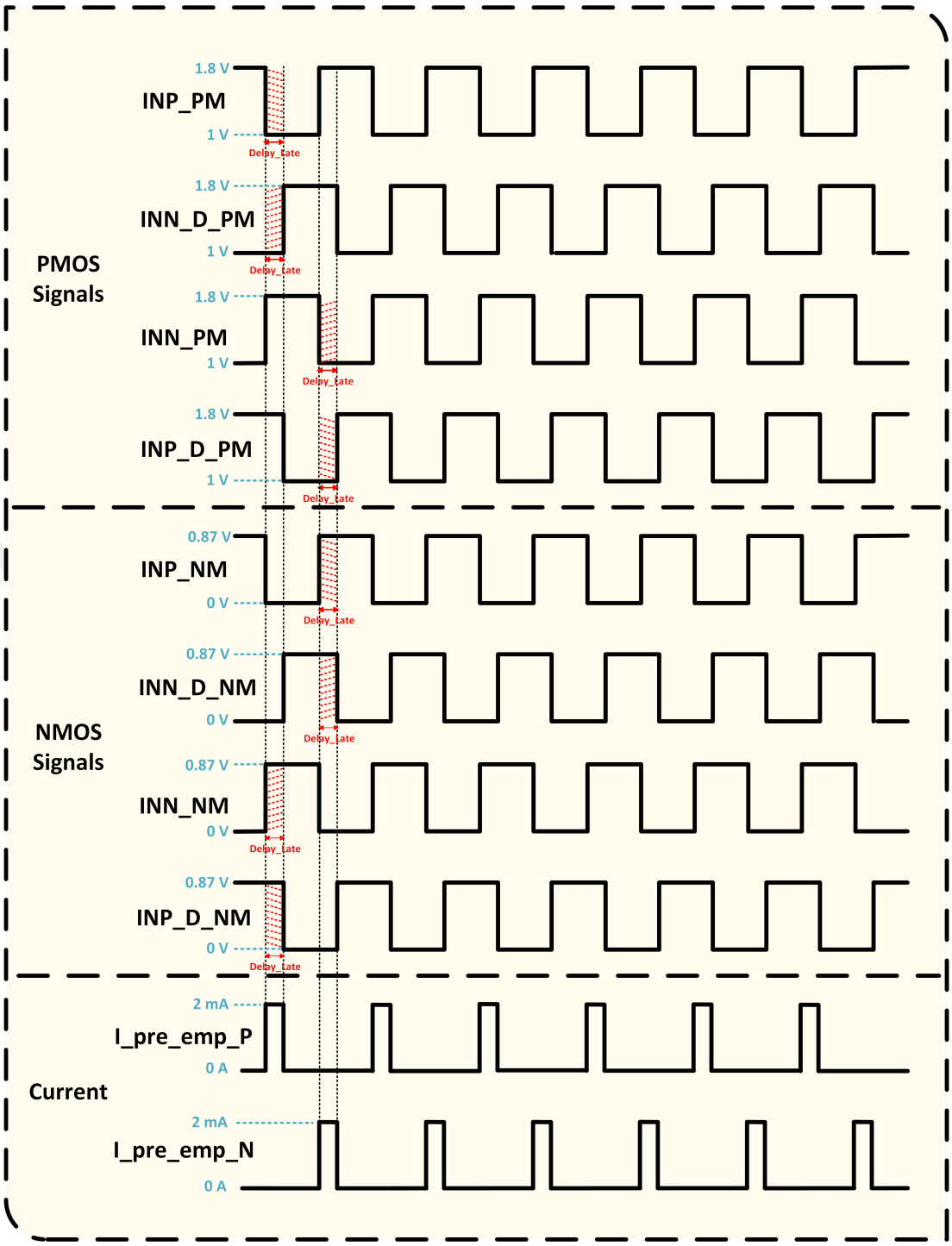

Figure 3.20 : Signal diagram for pre-emphasis.

Figure delightfully shows this behaviour. In addition, it can be seen from the Figure that while the PMOS signals are from 1 V to 1.8 V, NMOS signals are from 0 to 0.87 V, which the reason of it discussed earlier. The amount of time that the current will be applied to the output was determined by the amount of delay chosen in the

late delay line. It can be clearly seen that INN_D_PM is just an inverted and delayed version of INP_PM. When there is larger delay in the delay line, it means the additional current will be provided to the output for a longer period of time. Moreover, having controllable delay options increases the performance of the LVDS transmitter across PVT corners.

There is also an additional delay line called early delay line. Its effect was not shown in the Figure but this delay line simply shifts all of the signal, which means shifting the current. In other words, early delay will shift the current in time domain. Therefore, it helps to the system to have better performance. For instance, for the current having the same period of time, if the current is applied at the time that the signal recently starts to rise, the pre-emphasis current might not affect the original signal at all. similarly, if the current is applied too late, that might cause additional problems. As a result, in addition to having a proper period of time for current, it is important to apply the current at a proper time. The early delay is also beneficial for PVT compensation.

3.4.6 Inductive peaking

In addition to pre-emphasis, Inductive peaking method is used to increase bandwidth of the LVDS transmitter. How the inductive peaking affects the LVDS performance can be seen in Results section. Basic idea of getting a peaking in the frequency domain is to add an inductor between outp and outn nodes.

To be able to enable and disable the inductive peaking a transistor was added in the middle of the inductor. Moreover, series resistors were added to this inductor to make

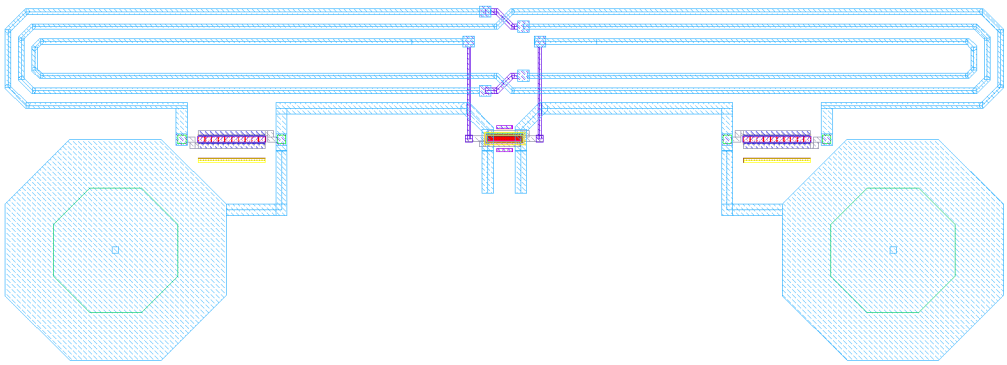

Figure 3.21 : Layout of inductive peaking.

output impedance match. The values for the resistors with an addition of on resistance of the transistor is a parallel load to the output of the LVDS driver. Since the circuit itself is complicated the value for the resistors were not calculated and picked by the help of simulations which provides best performance for eye diagram. Schematic diagram of this inductive peaking block can be seen in Figure 3.4 and also layout of this block can be seen in Figure 3.21. Transistor in the middle and the resistors can easily be seen in this figure.

3.5 LVDS Transmitter Layout

Total area of LVDS occupies 0.036273 mm^2 area having 321 µm width and 113 µm length including inductor. Zoomed version of layout of LVDS without inductor and pads can be seen in Figure 3.22. It can be easily seen that all high speed parts of the circuits are placed in the middle of the layout while current sources are placed in relatively far places. This method significantly increases high speed performance of the layout. Since the high speed path is routed without any turn in the layout the parasitics at these nodes were minimized. The whole layout of the LVDS with inductor and pad can be seen in Figure 3.23. ESD diodes are also placed very close to the pads.

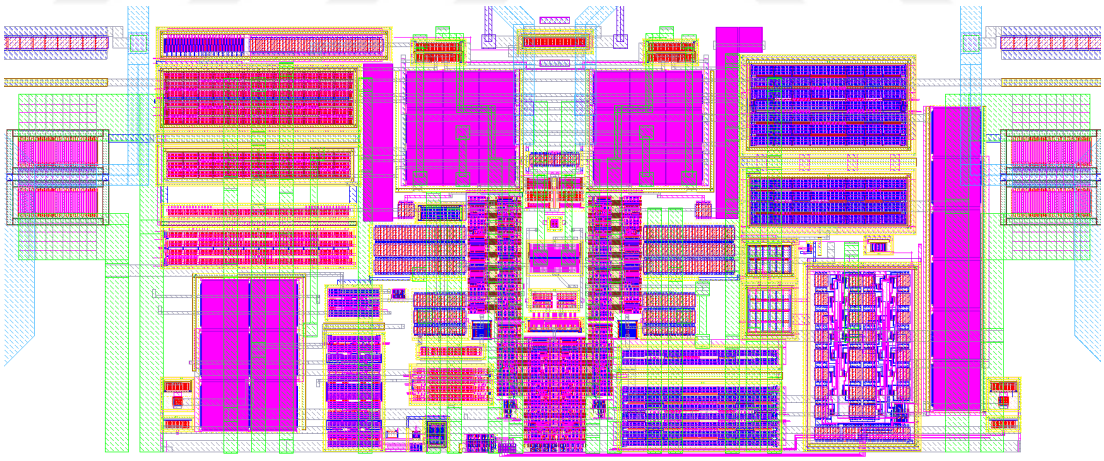

Figure 3.22 : Zoomed layout of LVDS without inductor.

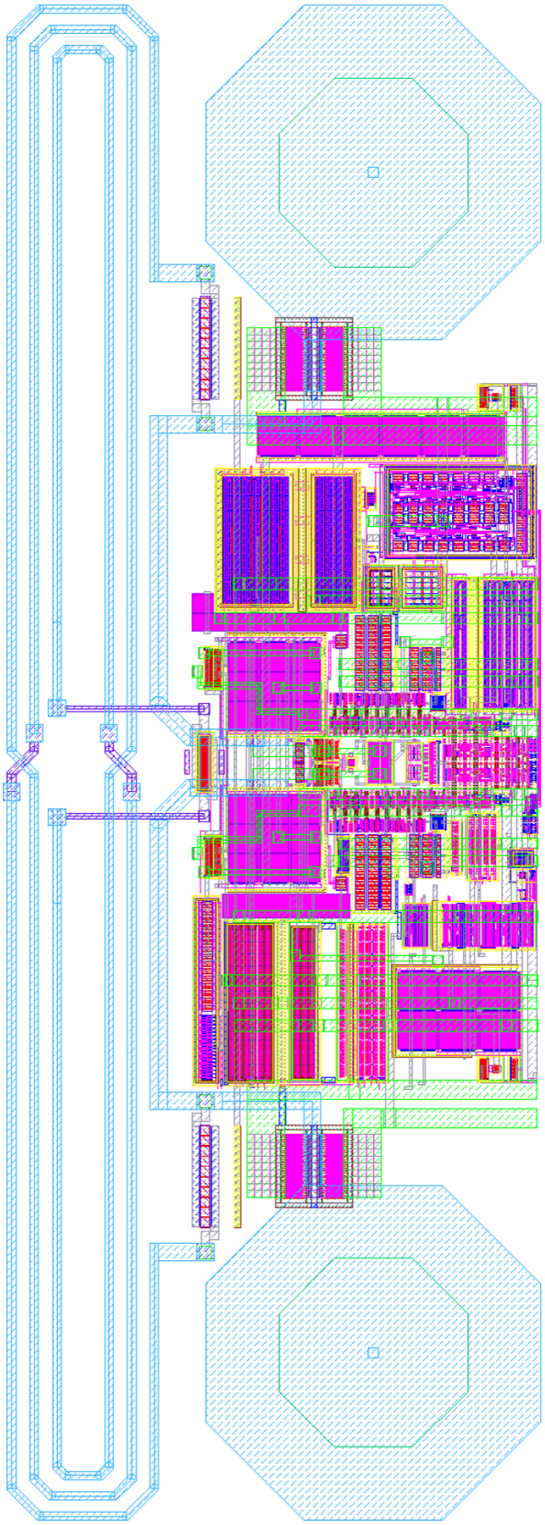

Figure 3.23 : Layout of LVDS transmitter.

4. Results

In this section, post-layout simulations of the LVDS is shown. Simulations can be considered in different sections such as DC results, AC analysis, pulse response and ISI, transient analysis and eye diagrams. Process variations, voltage changes and temperature changes should be consider to verify the performance robustness of the circuits. Therefore, different corner setup naming were achieved. TT, FF, SS , FS and FS corners represent process variations in the corner naming. Temperatures of the corners are 60 C (Nominal Temperature), -50 C (Low Temperature), and 150 C (High Temperature). In addition, supply voltage was assumed to be changed from 1.6 V to 2 V, which are called Low voltage (L) and High Voltage (H). Similarly, 1.8 V is called Nominal Voltage (N). As a result, SS150L corner naming means that this corner has SS process, 150 C temperature and Low voltage supply which is 1.6 V.

4.1 DC Results

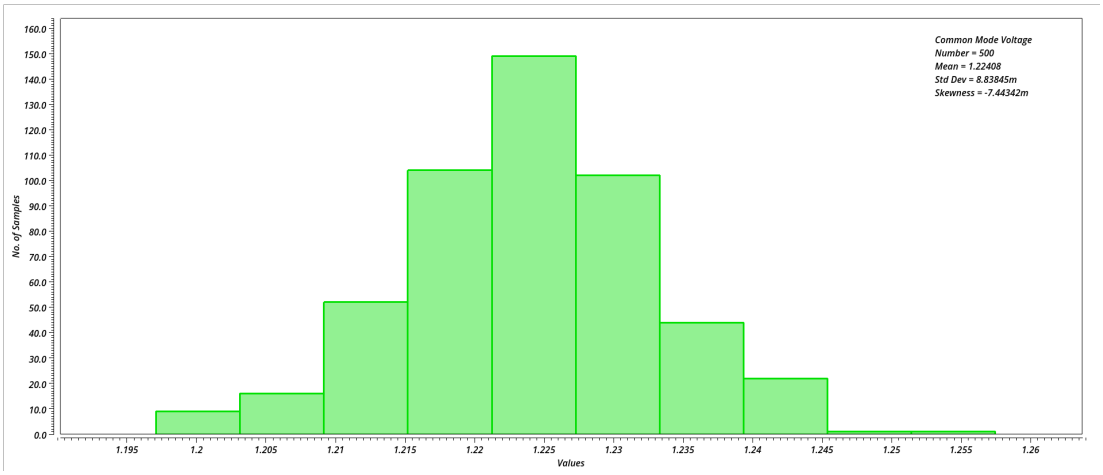

Figure 4.1 : Monte carlo simulation result of output common mode voltage.

Most of the analysis for this block is transient. However, output common mode voltage can be examined in Monte Carlo (MC) simulations to see variation across different random corners. Hence, the Monte Carlo simulation was run with both process and

mismatch. 500 samples were run and the common mode feedback voltage distribution can be seen in Figure 4.1. Output common mode voltage is desired to be 1.225 V and it can be seen that mean value in MC simulation is 1.22408 V having 8.83 mV standard variation.

4.2 AC analysis

LVDS can be considered as high voltage and non-linear block. Therefore, it is hard to make AC analysis and sometimes results might be misleading. Therefore, in order to analyze whole circuit with AC analysis, Common mode feedback amplifier loop was examined. Loop was broken with an iprobe and with the help of STB analysis loop gain and loop phase were analyzed. Loop gain and the phase can be seen in Figure 4.2.

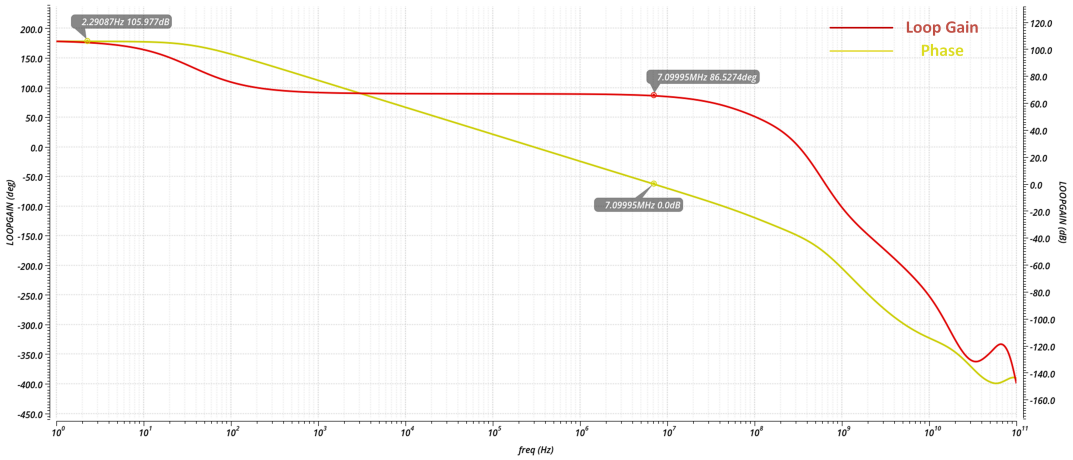

Figure 4.2 : Loop gain and phase of CMFB amplifier.

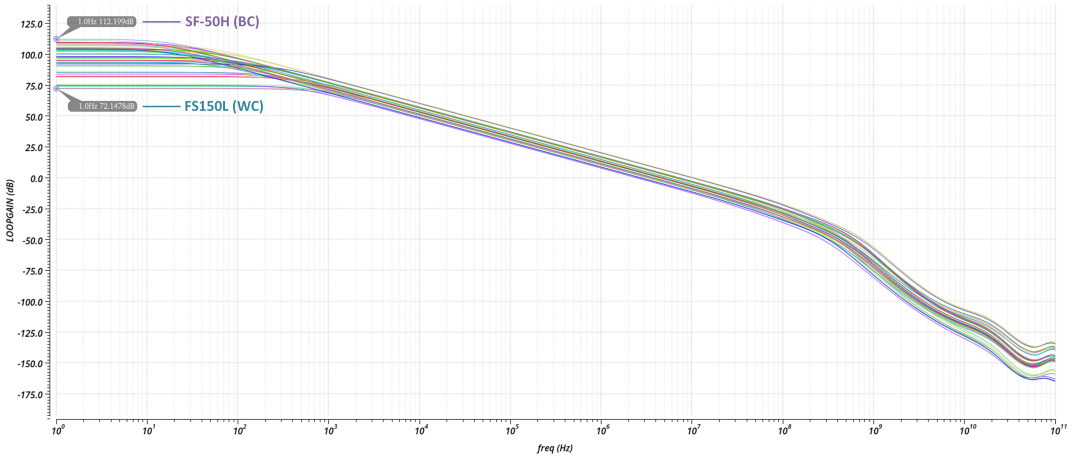

Figure 4.3 : Loop gain and phase of CMFB amplifier (PVT).

Moreover, PVT simulations were made and the results can be seen in Figure 4.3. It can be seen that the minimum loop gain is obtained in FS150L corner, while the most gain is obtained in SF-50H corner. Even for the least gain, it is still enough gain to have a proper loop. These results can be verified with MC simulations shown in Figure 4.1, because if there was a loop gain problem, output common mode voltage might diverge dramatically. In addition to that, phase margin changes between 84.62 and 87.88 which provides enough margin to be stable. Stability of the loop was also tested by applying a sudden voltage pulse to common mode voltage and the loop was able to turn the common mode voltage to desired value without any stability issue.

PSRR for this block was examined with AC analysis. DC voltages were applied to pre-amplfiers and AC voltage was set to 1 and differential outputs of the LVDS were examined. The results for PVT corners can be seen in Figure 4.4. Since this block is not a linear and low swing block just AC analysis might not be enough for PSRR results. Therefore, a sine wave having 20 mV amplitude was added on top of the supply voltage and changes in the output were examined in transient analysis. The results are also similar in transient analysis.

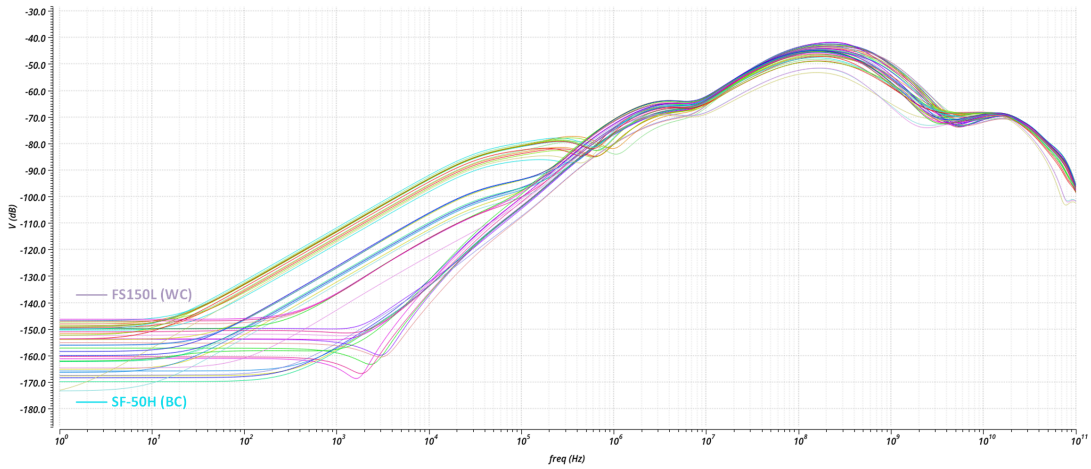

Figure 4.4 : PSRR across PVT.

4.3 Pulse Response and Inter-symbol Interference

Applying a pulse after waiting for a long period relative to data frequency is a proper way to see Inter-symbol Interference (ISI) performance. If a clock signal is sent via this LVDS, ISI might not be a problem or be less problematic. However, when the

data is sent through this LVDS there might be crucial issues. It can be explained such that behaviour of the system to a signal change is different according to the previous signal values. For instance, "1" signal after one "0" signal will be different than having "1" signal after two consecutive "0" signals because the system waits longer and the voltages are settled according to "0" signal. Therefore, the system behaves differently according to the signal itself causing the problem. This problem is called ISI, which means one signal can affect the signal which is before and after it. This problem can be much more visualized when eye diagram analysis is made.

A pulse signal was applied to the system as an input after waiting 3 nS which can be considered as a long period compared to data frequency. The differential output of the LVDS was examined which can be seen in Figure 4.5. In this figure, ISI can easily be seen when inductive peaking and the pre-emphasis were disabled. After becoming "1" it takes too long to turn back to "0" signal which means that it will be mixed to the next signal. However, on the other hand, when pre-emphasis and inductor were enabled the signal settles much faster, which increases the performance of the system.

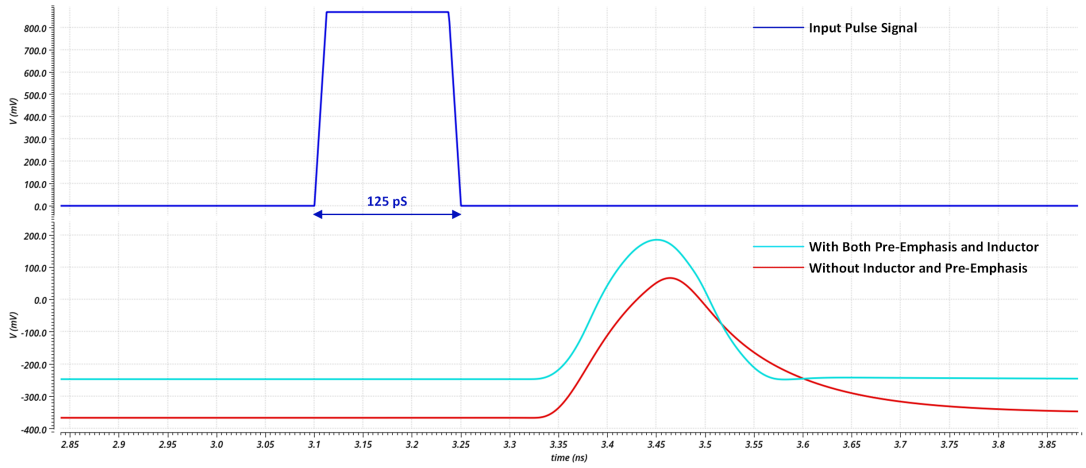

Figure 4.5 : Step response of LVDS.

4.4 Transient Analysis and Eye Diagrams

Functionality of the LVDS can be examined in transient analysis. Periodic pulse signal can be applied to LVDS as an input. This might be real case also like clock signal or data having encoding which always provide ones and zeros periodically. However, to analyze the performance of the LVDS data signal should have random behaviour.

Generating random signal is a major problem and it is not in the scope of this thesis. However, instead of using a full random signal, 12 bit pseudo random sequence (PN Sequence) signal having 8 Gbps data rate (each bit has 125 pS period) was used for this project.

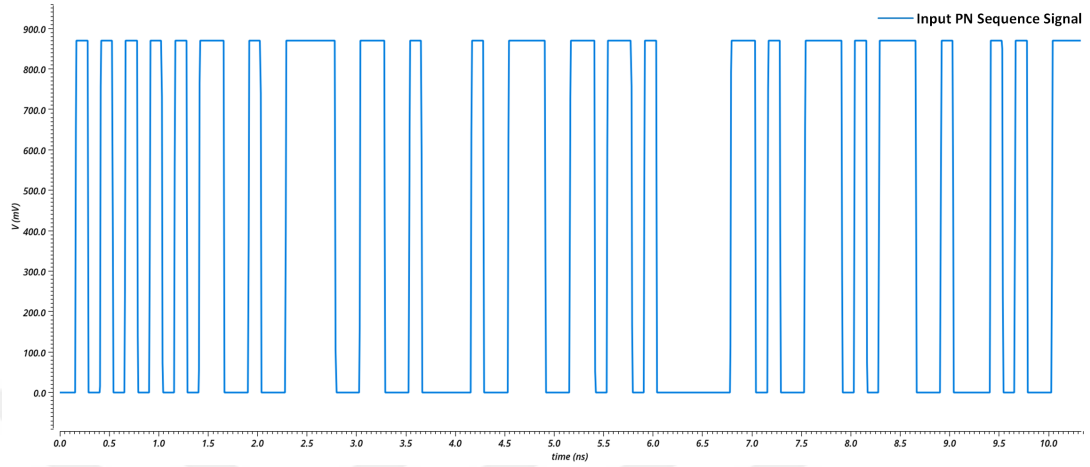

Figure 4.6 : Input PN sequence signal.

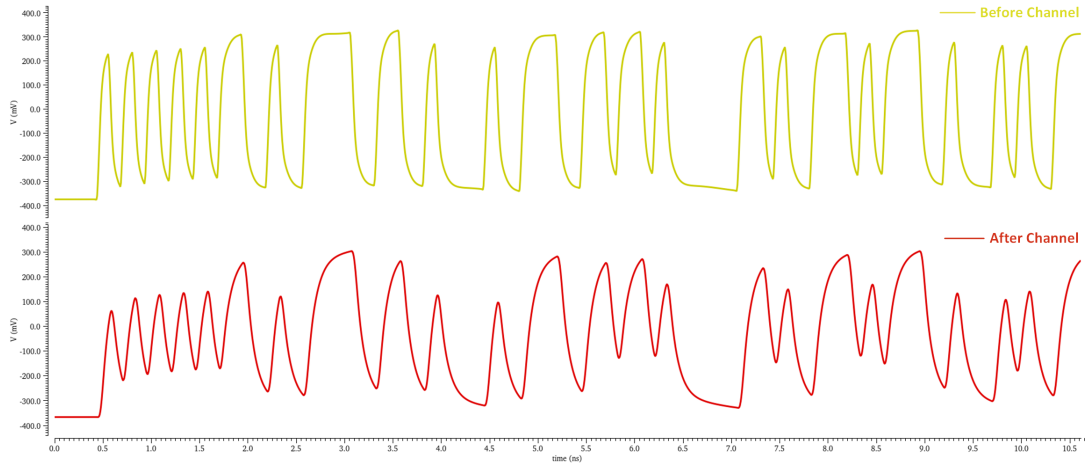

Figure 4.7 : Differential output before and after channel with no feature.

PN sequence signal can be seen in Figure 4.6. This sequence contains different scenarios such as periodic "1" and "0" signals or having multiple times "1" and "0" signals. Therefore, thanks to this signal LVDS behaviour can be examined for different data scenarios. Transient analysis were run for 40 nS to have enough variety of scenarios. Differential output signal of the LVDS when inductive peaking and pre-emphasis were disabled can be seen in Figure 4.7. This figure shows how the digital input sequence is transferred to a differential analog signal thanks to LVDS.

Moreover, the filtering effect of the channel is also shown in this Figure. The yellow signal is the signal before the channel and it becomes like red signal after passing through channel. Even though some of the signals seem like a square pulse before channel it can be seen that especially rising and the falling edges were filtered out. Therefore, this figure also nicely illustrates why pre-emphasis is needed.

Figure 4.8 shows how the pre-emphasis helps to obtain better shaped signals after channel. Effects of the pre-emphasis can be seen especially in the rising and the falling edges of the signals. If there was no filtering effect of the channel this emphasis might distort the signal, however, low pass behaviour of the channel will filter this edges and generate signals having much more like a square shape.

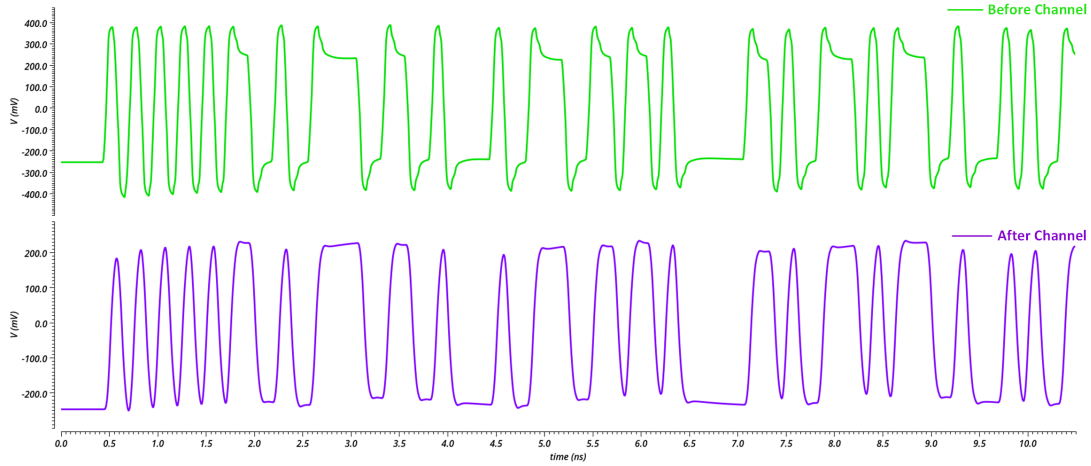

Figure 4.8 : Differential output before and after channel with features.

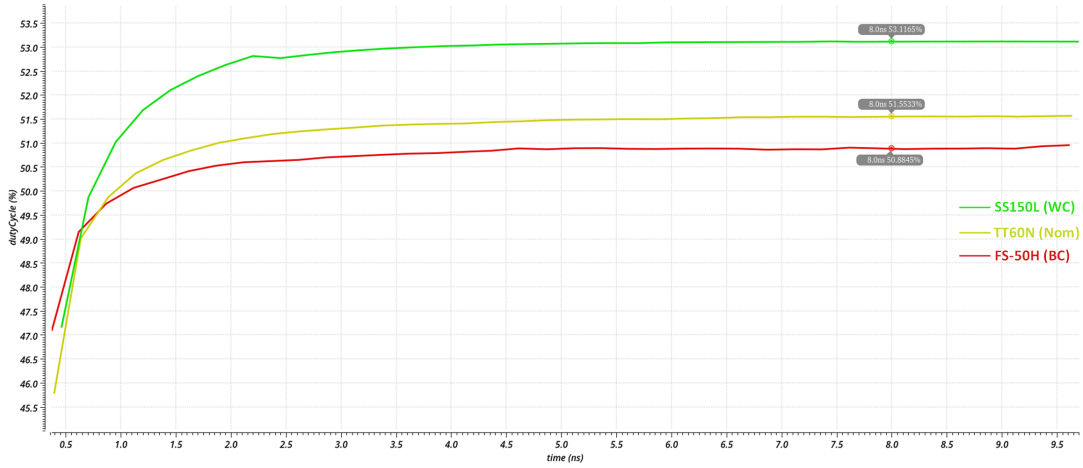

Figure 4.9 : Duty cycle distortion across PVT.

When a periodic signal is applied to LVDS as an input, duty cycle distortion should be considered as well. For this purpose, 8 Gbps periodic input signal was applied to the LVDS and the output duty cycle distortion was examined over PVT corners. Best case and worst case among the corners were shown in Figure 4.9.

The best way to examine the performance of the LVDS is to check the eye diagram. Therefore, the eye diagram was examined when 8 Gbps 12 bit PN Sequence signal was applied to the LVDS as an input for 4 different scenarios which are both pre-emphasis and inductive peaking are disabled, only inductive peaking is enabled, only pre-emphasis is enabled and both pre-emphasis and inductive peaking were enabled. Figure 4.10, incredibly shows how the pre-emphasis and inductive peaking improves the performance.

When both pre-emphasis and inductive peaking are disabled, the eye width and height are not wide enough. This means that there are timing errors for signals and also the "1" and "0" signals are not in the same analog level. This behaviour can easily be seen in Figure 4.7. Each "1" signal has different analog voltage. For instance, if two consecutive "1" is the case, voltage goes up. However, when there is a sudden change in the signal the voltage levels differ. This is a nice presentation of ISI.

When the inductive peaking is enabled, the eye width and height becomes wider which improves the signal integrity since the inductor increases the bandwidth of the system. However, enabling inductive peaking alone does not help too much. On the other hand, when pre-emphasis is enabled it can be seen that eye width and height tremendously become wider.

when both pre-emphasis and inductive peaking are enabled, the best signal integrity is achieved among all these scenarios. It can be seen that eye width and eye height extremely get wider. Also, the signals seem much more symmetric which means it has less duty cycle distortion. Similarly, this improvement in the eye diagram can also be seen in the Figure 4.8. Each "1" and "0" signals have close analog values for various cases. Therefore, these improvements make the behaviour of the LVDS much more data independent which was the purpose from the beginning.

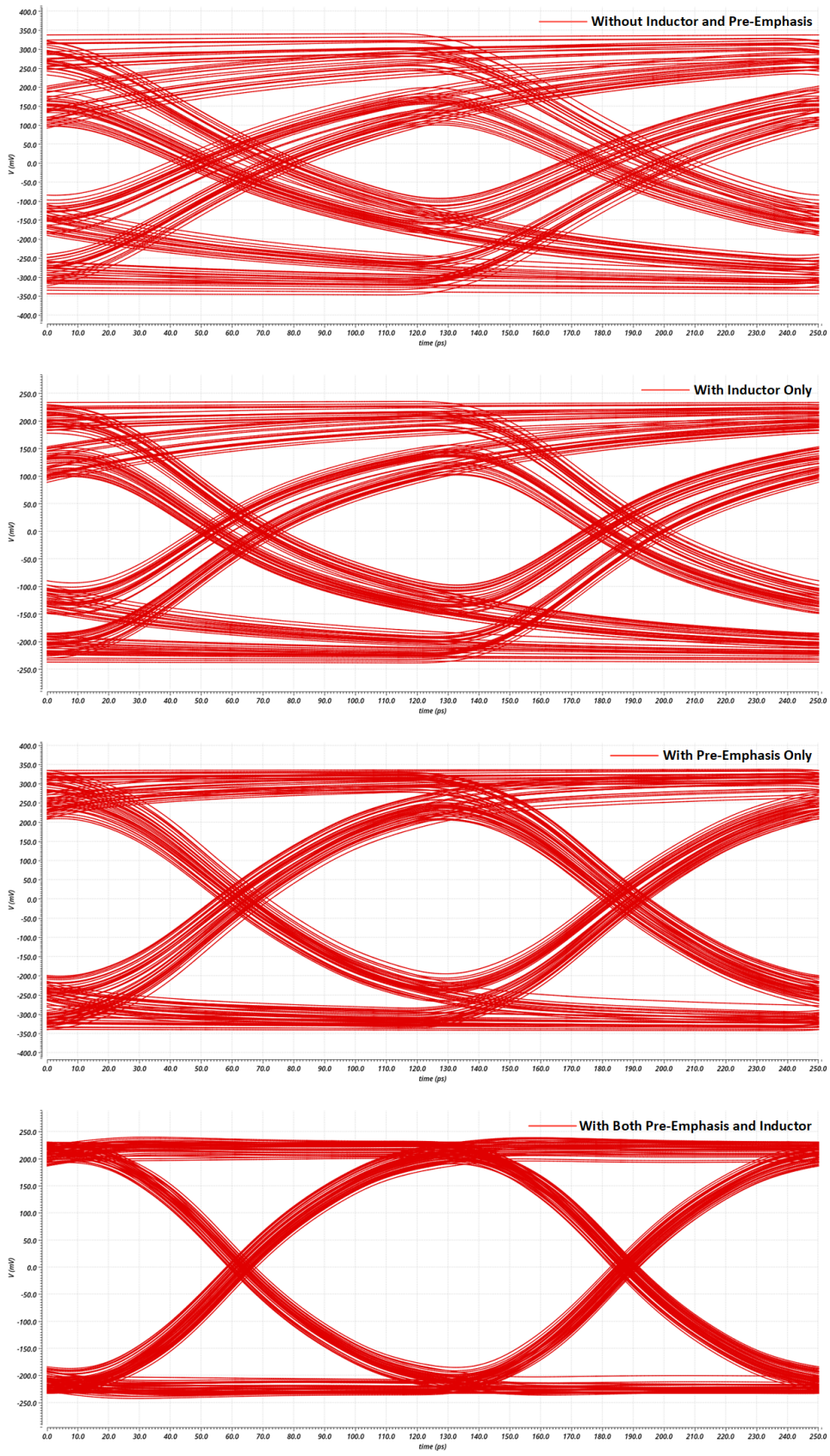

Figure 4.10 : Differential output eye diagrams after channel.

Eye diagrams of some selected corners can be seen in Figure 4.11 when the input PN Sequence signal has 8 Gbps data rate. Especially Low Voltage (L, 1.6 V) corners have worse performance. Eye width and height are wider in SF-50H corner. Hence, it can be seen that LVDS transmitter has verified performance across PVT.

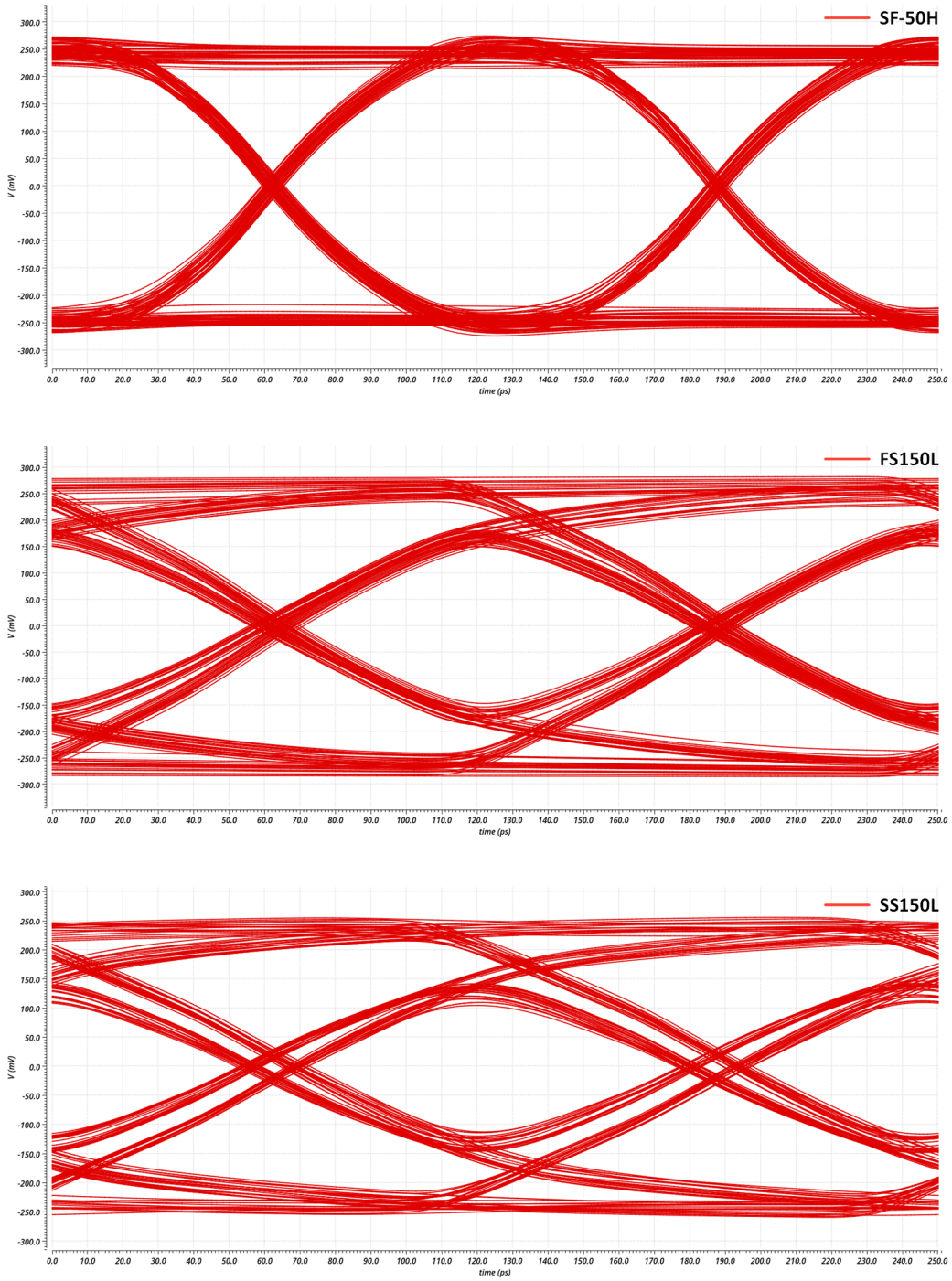

Figure 4.11 : Differential output eye diagrams after channel (PVT).

Thanks to this motivating results in 8 Gbps data rate, the faster data rate is examined. 12.5 Gbps data rate was applied as an input to the LVDS driver and the Eye diagrams for nominal corner and SS150L corner can be seen in Figure 4.12. While eye diagram performance can be considered as proper in Nominal corner, it can be seen that the signal integrity is noticeably poor in SS150L corner. This frequency might be an option after tape-out. It is important to note that also, these results were taken when channel is 8 inch FR4 channel. Therefore, for shorter channel or different PCB materials this frequency might be achieved.

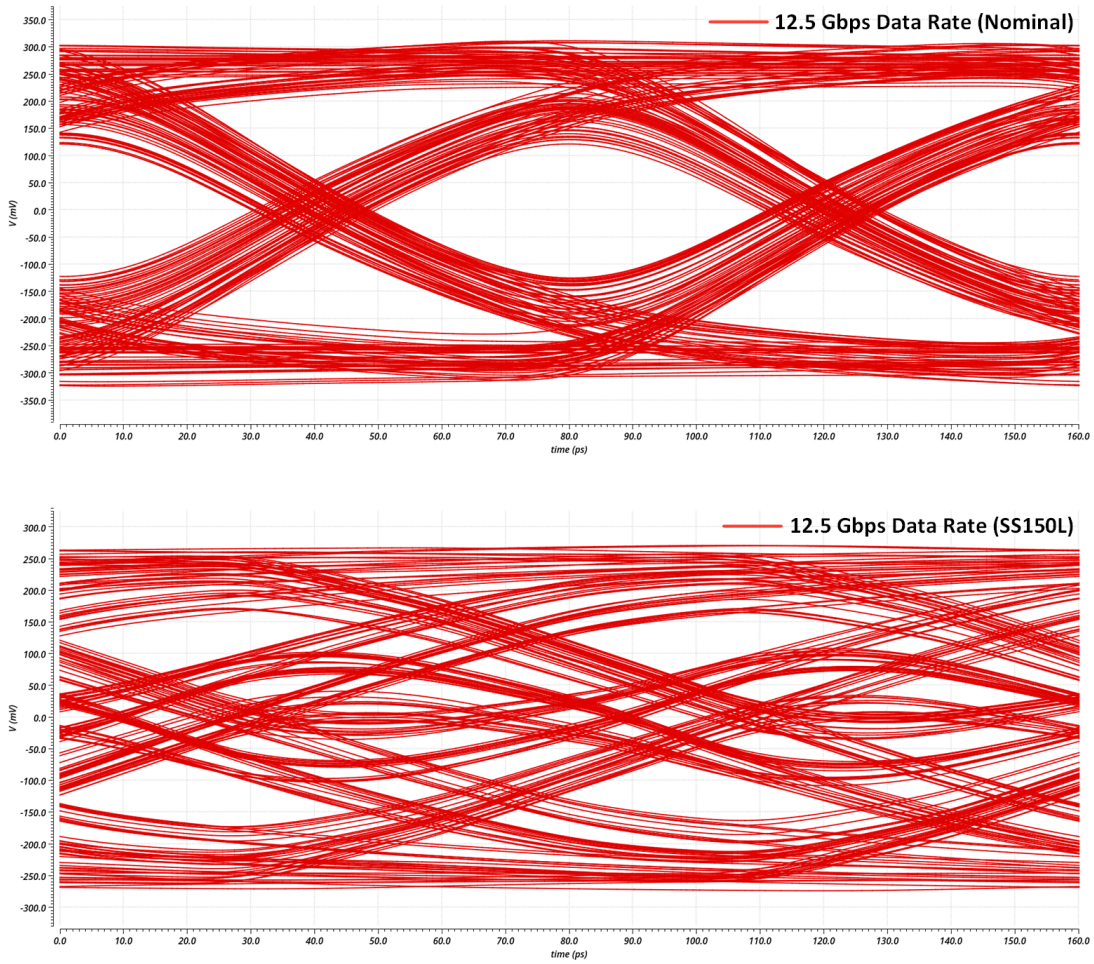

Figure 4.12 : Differential output eye diagrams after channel (12.5 Gbps, PVT).

5. Conclusion

In recent years, higher data rates in wireline communications are demanded. Therefore, LVDS standard has been commonly used since it operates not only at high data rates but it also provides noise immunity due to differential operation and provides low swing at the output, which helps to reduce power consumption. The channel (might be long cable or PCB routing) has corrosive effects on the transmitted signal. Therefore, a channel equalization method is needed. In general, in the transmitter side pre-emphasis is used to equalize the channel effect.

In this thesis, an 8 Gbps LVDS transmitter having controllable inductive peaking and pre-emphasis is designed in 22 nm FDSOI process and post-layout results were verified in Cadence Virtuoso. While supply voltage for analog voltage is 1.8 V, digital supply voltage is 0.87 V. Output common mode voltage of the LVDS controlled by common mode feedback amplifier. It is set to 1.225 V and can be swept from 0.98 V to 1.33 V. Nominal current consumption (total current pulled from analog and digital supplies) is 11.249 mA. The LVDS transmitter has 2.531 pJ/bit energy efficieny and the layout of the LVDS occupies 0.036 mm^2 including inductor and pads. A summary of the LVDS transmitter can be seen in Table 5.1.

Table 5.1 : Summary table of LVDS transmitter.

Description	Min	Nom	Max
Technology	-	22 nm FDSOI	-
Channel Length (inch FR4)	-	8	-
Common Mode Voltage (V)	0.980	1.225	1.330
Swing Amplitude (mV)	230	250	350
Supply Voltage (V)	-	1.8	-
Maximum Data Rate (Gbps)	-	8	-
Current Consumption (mA)	7.283	11.249	12.633
Power Consumption (mW)	13.109	20.248	22.739
Energy Efficiency (pJ/bit)	-	2.531	-
Random Jitter (pS)	1.724	2.037	3.69
Deterministic Jitter (pS)	2.687	5.217	15.77
Layout Area (mm^2)	-	0.036	-

Jitter results were obtained from eye diagram across PVT corners. The Nominal random jitter is 2.037 ps, while minimum and maximum random jitter were 1.724 pS and 3.69 pS relatively. The nominal deterministic jitter is 5.217 pS, while minimum and maximum deterministic jitter were 2.687 pS and 15.77 pS relatively.

Table 5.2 : Comparison table of LVDS transmitter with literature.

Description	This Work	[36]	[37]	[20]
Technology	22 nm	28 nm	40 nm	28 nm
Results	Sim	Meas	Sim	Sim
Supply Voltage (V)	1.8	1.8	1.8	1.8
Data Rate (Gbps)	8	2.5	1	1
Power (mW)	20.25	16.51	7	8.7
Energy Efficiency (pJ/bit)	2.53	6.60	7	8.7
Layout Area (mm^2)	0.036	0.0306	0.0168	0.009

5.1 Future Works

The maximum operating data rate was set to 8 Gbps due to simulation results and the 8 inch channel model. However, the performance of the LVDS will be affected from PCB material quality, length of the routing, pad capacitance and lots of different non-idealities coming from off-chip world. Therefore, for future works, various post silicon verification should be done in order to be confident about the performance of the LVDS. In addition to that, if better PCB materials are used instead of FR4 or if the channel in the PCB is less than 8 inches, this LVDS might also operate in 12.5 Gbps. Post-layout simulations show encouraging results. In addition to that, a nice calibration algorithm should be defined for delay and the current source codes to have the best eye diagram performance after tape-out. The programmability of the LVDS seems enough to handle problems, however, calibration should be verified in post-silicon tests. To sum up, the most important future work will be getting the tape-out and making the tests.

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