İSTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

MINIMUM-NOISE-FIGURE LNA DESIGN PROCEDURE FOR IEEE 802.11a WLAN APPLICATIONS

M.Sc. Thesis by

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IEEE 802.11a WLAN UYGULAMALARI İÇİN MİNİMUM GÜRÜLTÜLÜ LNA TASARIM AKIŞI

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SUMMARY

In this study, the theory of the LNA circuits are examined and the designs and analyses of CMOS and SiGe HBT LNAs with minimum noise figure for IEEE 802.11a WLAN applications are completed. Thesis is focused on inductively-degenerated cascode architecture to take the advantage of both cascode amplifiers such as high stability, reverse isolation and inductive degeneration such as simultaneous noise and input matching. Input matching networks are modified by adding external base-emitter (or gate-source) capacitance C_{ex}, to improve the noise performances of the LNAs. LNAs are designed with and without the capacitance C_{ex} in order to observe the effects of this capacitance for each process, SiGe HBT and CMOS. As a result of this comparison, it has been shown that external base-emitter (or gate-source) capacitance improves the noise performance of the SiGe HBT LNA significantly while does not improve that of the CMOS LNA under the given power consumption budget. In order to maximize the linear output power, output matching is provided by the tapped-inductor matching network which also improves the noise performances of the designed LNAs due to not including any real noisy resistor. Finally, by using Spectre-RF simulator two LNAs were designed and simulated one of which is SiGe HBT and the other is CMOS, operate at 5.8 GHz, since they are intended for IEEE 802.11a WLAN applications.

IEEE 802.11a WLAN UYGULAMALARI İÇİN MİNİMUM GÜRÜLTÜLÜ LNA TASARIM AKIŞI

ÖZET

Bu çalışmada, LNA (düşük gürültülü kuvvetlendirici) devrelerinin teorisi incelenmiş ve IEEE 802.11a WLAN uygulamaları için minimum gürültülü CMOS ve SiGe HBT prosesleri için LNA devrelerinin tasarımları ve analizleri tamamlanmıştır. Endüktans-dejenerasyonlu yapılar gürültü ve giriş uyumunun aynı anda sağlanmasına imkan tanımaktadır. Kaskod kuvvetlendirici devreler ise yüksek karalılık ve giriş-çıkış yalıtımı sağlama açısından bilinen en uygun yapılardır. Bu nedenlerle tezde endüktans-dejenerasyonlu kaskod yapılar üzerine odaklanılmıştır. LNA devrelerinin gürültü performanslarını arttırmak amacıyla giriş uyumlaştırma devrelerine harici baz-emetör (geçit-kaynak) kapasitesi C_{ex} eklenmiştir. Bu harici kapasitenin etkilerini incelemek üzere SiGe HBT ve CMOS proseslerinde LNA devreleri C_{ex} kapasitesiyle ve C_{ex} olmadan tasarlanmıştır. Bu karşılaştırma sonucunda harici baz-emetör (geçit-kaynak) kapasitesinin SiGe HBT LNA devresinin gürültü performansını önemli ölçüde iyileştirdiği görülmüştür. Fakat verilen güç tüketimi kısıtı altında, C_{ex} kapasitesinin CMOS LNA devresinin gürültü performansında aynı iyileşmeyi sağlamadığı gösterilmiştir. Lineer çıkış gücünü maksimize etmek amacıyla çıkış uyumlaştırma devresi olarak kademelendirilmiş edüktans dönüştürücü devre kullanılmıştır. Bu devre lineer çıkış gücünün maksimize edilmesinin yanında dönüştürücü devre gerçek bir direnç içermediğinden LNA devresinin gürültü performansının da iyileşmesi sağlanmıştır. Son olarak, Spectre-RF simülatörü kullanılarak, SiGe HBT ve CMOS prosesleri için IEEE 802.11a WLAN uygulamalarında kullanmak üzere 5.8 GHz frekansında çalışan iki tane LNA devresi tasarlanmış ve benzetimleri yapılmıştır.

1. INTRODUCTION

By transmitting radio signals across the Atlantic Ocean by Guglielmo Marconi in 1901, wireless technology came to existence. The possibility of replacing telegraph and telephone communications with wave transmission through the air result in wireless technologies finding applications in many of the mundane tasks of everyday life. Therefore, today, wireless technologies have widespread use such as cellular phones, aircraft radar, GPS (Global Positioning System) navigation systems.

Radio transceivers have been around since the 1900s, with the invention of AM and FM radio broadcasting. In the 1920s, Armstrong developed the transceiver concept which is still in use. The word transceiver stands for the combination of the words transmitter and receiver, and transceiver is one of the key parts in a wireless communication terminal. With the development of DECT (Digital Enhanced Cordless Telecommunications) and GSM (Global System for Mobile Communications) standards in the 1980s, transceivers have started to appear in wireless communication terminals. In the context of a mobile communication terminal, the signals coming from the antenna are transformed into signals which can be converted into the digital domain by the receiver, whereas the transmitter converts the analog version of the digital data stream at baseband into a signal at radio frequencies, and delivers this signal to the antenna with certain amount of power [1].

The main goal of radio receivers is to extract and detect the desired signal selectively from the electromagnetic spectrum. Since the electromagnetic spectrum is a scarce source, the drive to higher frequencies, encourage the development of more sensitive and selective radio receiver architectures. Since the demand for radio technology grew faster with the advent of television and radio broadcasting in the 1920s and 1930s, the technologies developed along to meet these increasing demands of radio reception such as the vacuum tube, the piezo-electric resonator and later on the transistor and the integrated circuit demonstrate not only the history of radio but also history of electronics in general. To illustrate the increasing level of sophistication to

provide demand for improved selectivity even at high frequencies some of the receiver architectures should be mentioned.

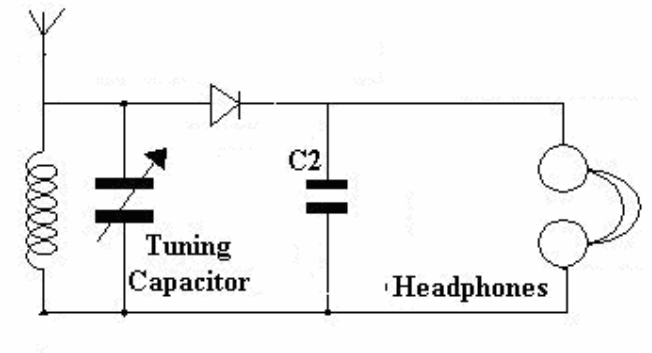


Figure 1.1 : Crystal detector.

The crystal detector shown in Figure 1.1 is one of the earliest radio receivers and in this architecture received the signal from the antenna is bandpass filtered and then rectified by a simple diode. The rectified signal has an audio frequency component that can be heard directly on a high impedance headphone when a sufficiently strong amplitude modulated radio signal is received. The desired radio channel can be selected through a variable capacitor. After the advent of vacuum tube, it is substituted by the rectifying crystal.

Since this architecture has very poor sensitivity and requires strong signal to forward-bias the detector diode, transmission distance or transmitted power required for a given distance is limited. These limitations have disappeared with the advent of the vacuum tube amplifier. Therefore, the development of more sensitive receivers is provided and transmit power requirements are reduced. Additionally this architecture (crystal radio) is not very selective due to including a simple bandpass filter, thus adjacent radio channels may interfere with the desired signal channel. Furthermore, with the increase in frequency, the bandwidth requirements for channel filtering make use of a single RF filter impractical [2].

It can be said that sensitivity and selectivity are the two important limiting factors in radio receiver design. The first limiting factor, sensitivity is increased in heterodyne receiver which is first patented by Professor Reginald Fessenden in 1902 by improving the efficiency of demodulation with the use of local oscillator. The local

oscillator is summed in series with the antenna; thereby rebroadcasting the oscillator is a significant problem of the heterodyne receiver.

Regenerative receiver which is another innovation that sought to improve the sensitivity of radio receivers introduced by Armstrong in 1915, includes the concept of impedance transformation, gain boosting with positive feedback and use of an active device for signal amplification and rectification. Additionally, the selectivity of the system benefits from the use of multiple filters.

The superheterodyne receiver which now forms the basis of all radio receivers made today despite the changes in electronic technologies, was invented by Armstrong in 1918. This architecture employs a heterodyne front end that mixes the incoming radio signal with local oscillator in a vacuum-tube detector to translate the RF signal to intermediate frequency where signal can be amplified and detected and the stability of local oscillator is less important. Since highly selective amplification and filtering can easily be achieved at the lower IF (intermediate frequency) frequency, weak signals can be detected. Furthermore, with the use of multiple frequency conversions, total required amplification can be distributed across several frequencies, thus total possible amplification increased. Finally, different RF signals can be selected for detection by tuning the local oscillator. The concept of using multiple stages of frequency conversion to achieve increased selectivity and extreme sensitivity is a powerful one that is widely used today [2].

In homodyne receivers (or direct conversion or zero-IF), the RF spectrum is directly translated to the baseband in the first down conversion. The simplicity of the homodyne architecture offers two important advantages over a heterodyne architecture. First, since no image filter is required in this architecture, the LNA need not to drive a 50 Ω load. Second, low pass filters and base band amplifiers are suitable for integration when compared to IF filters and subsequent downconversion stages in heterodyne architecture [3]. However, the homodyne receiver presents some unique RF problems, which have important implications at the device and circuit level. First, the downconverted signal is extremely sensitive to DC voltage offsets due to current leakage from the local oscillator entering into the LNA and mixer. This means high requirements on reverse isolation and low substrate coupling.

Moreover, since the downconversion of the RF signal to (nearly) zero IF, the 1/f noise in the oscillator must be minimized. Finally, distortion (linearity) must be kept very low (high) for the LNA and mixer that is a condition trades off with power dissipation.

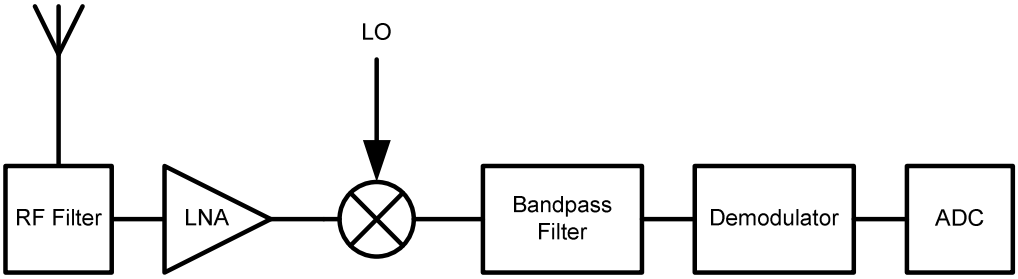


Figure 1.2 : Block diagram of a simplified RF receiver.

The simplified structure of an RF receiver is shown in Figure1.2. In the receive path, the signal is typically filtered, amplified by an LNA (low noise amplifier) and the spectrum is translated to lower frequency with a downconverter (usually mixer) by mixing with a local-oscillator (LO). This downconversion simplifies the subsequent demodulation. Demodulated signal is digitized by an analog-to-digital converter (ADC) as the final step. The digital signal is then processed in digital signal processing units (DSP) [3]. Since the LNA is the first active building block in the receiver front-end, the performance of the LNA can greatly affect sensitivity and noise parameters of the overall receiver. Therefore, LNA should provide considerable gain while minimizing the noise introduced to the system.

The wireless communication industry has experienced strong growth over the last decade. This growth is supported by evolution in standards, to enable increased capacity, by higher data rates and wider compatibility. With designs that provide backward compatibility for existing wireless standards, cost-effective solutions for inter-continental roaming and accessing to different wireless standards, successful transition to future wireless generations can be achieved. On the other hand, the high licensing fees for 3G WAN services (Third Generation Wide Area Network) have motivated increased development of short distance standards like LAN (Local Area Network) and PAN (Personal Area Network) which use unlicensed ISM (Industrial Scientific Medical Band) bands of 2.4GHz and 5GHz. In this frequency band access to the internet for voice-over-IP and other internet applications is possible.

Since IC technologies grow rapidly through the down scaling of the devices and the demand for RFICs (Radio Frequency Integrated Circuits) operating at high frequency bands, WLAN infrastructures must be able to support high data rates of the 802.11a and 802.11g standards. This growing demand for RFICs operating at high frequency bands such as the IEEE 802.11a and HyperLan industry standards which support data rates up to 54 Mbps and operate in the 5-6 GHz band has motivated designers to develop circuits in this frequency range. A brief summary of the technical properties of the IEEE 802.11a standard is given in Table 1 [4].

Table 1.1 : Technical properties of IEEE 802.11a standard.

Standard	**IEEE 802.11a**
Mobile Frequency Range (MHz)	5150-5250 (USA lower band) 5250-5350 (USA middle band) 5725-5825 (USA upper band)
Multiple Access Method	CSMA/CA
Duplex Method	TDD
Users Per Channel	127
Channel Spacing	OFDM: 20 MHz
Modulation	OFDM: QPSK, QAM OFDM: BPSK (5.5 Mb/s) OFDM: 16QAM (24, 26 Mb/s) OFDM: 64QAM (54 Mb/s)
Channel Bit Rate	12 Mb/s symbol rate, 5.5-54 Mb/s

CSMA/CA: Carrier Sense Multiple Access/Collision Avoidance, TDD: Time Division Multiplexing, OFDM: Orthogonal Frequency Division Multiplexing, QPSK: Quadrature Phase Shift Keying, QAM: Quadrature Amplitude Modulation, BPSK:Binary Phase Shift Keying

There have been several reports on 5-6 GHz band SiGe HBT and CMOS based LNAs most of which use the inductively-degenerated LNA architecture, since they are two of the most cost-effective technologies for high frequency wireless applications today [5-11].

The goal of this thesis is to constitute a design procedure for LNAs with minimum noise figure for IEEE 802.11a WLAN applications. Since the inductively-degenerated LNA architecture offers the possibility of achieving minimum noise figure and simultaneous input matching, the design procedure is suited for this architecture.

Chapter 2 includes different LNA architectures and detailed analysis of the inductively-degenerated LNA architecture for SiGe HBT and CMOS processes.

Chapter 3 presents the complete design of a SiGe HBT LNA using IHP 0.25 µm BiCMOS process parameters for IEEE 802.11a standard. Design specifications, design strategy and design steps are defined in detail and simulation results for the designed LNA are demonstrated.

Chapter 4 presents the complete design of a CMOS LNA using UMC 0.13 µm CMOS process parameters for IEEE 802.11a standard. Design specifications, design strategy and design steps are defined in detail and simulation results for the designed LNA are demonstrated.

Chapter 5 includes layout issues and post layout simulation results of the proposed SiGe HBT LNA which is laid out in IHP 0.25 µm BiCMOS process by using the Cadence Virtuoso layout tool.

Chapter 6 provides comparison between two proposed LNAs and concluding remarks.

2. DESIGN CONSIDERATIONS OF LOW NOISE AMPLIFIERS

The first block in most wireless receivers is typically a low noise amplifier (LNA), which is responsible for providing enough gain to overcome the noise of the subsequent blocks (such as mixer) and its noise figure sets a lower bound on the noise figure of the whole system [12]. Besides these, the LNA should amplify signals whose amplitude varies from few nV to tens of mV without any significant distortion. Additionally, sensitivity of the LNA determines the sensitivity of the whole receiver, since the sensitivity of a receiver (or block) is defined as the minimum level of the input signal for which the receiver provides an acceptable signal quality.

LNAs are usually preceded by passive filters to filter out-of-band interferers that impose the requirement of certain input impedance, such as 50 Ω, since the transfer characteristics of such filters is usually sensitive to their quality of termination.

Minimum noise figure can be obtained from a given device by using the optimum source impedance defined by the four noise parameters (R_n, G_{opt}, B_{opt}, F_{min}), as will be shown in the following sections. However, this approach is insufficient because the source impedance that minimizes the noise figure generally differs from the impedance that is required by the preceding stage, e.g. 50 Ω, which maximizes the power gain. This may result in an LNA having a bad input matching hence poor gain and good noise figure or vice versa. Furthermore, power consumption is an important constraint in many applications, but it is not considered in the classical noise optimization approach.

To develop a design strategy for an LNA that optimizes the noise figure while providing high voltage gain, good input match and low power consumption simultaneously, analytical expressions for noise, gain, input matching and linearity must be examined.

2.1 Common LNA Architectures

In the design of an LNA, there are several common goals such as minimizing the noise figure, providing gain with sufficient linearity, providing a stable input impedance (good input matching) and low power consumption that are emphasized earlier. LNA architectures can be divided into four distinct approaches, shown in Figure 2.1, when focused on the requirement of providing stable input impedance [13]. Although the architectures shown in Figure 2.1 are for CMOS devices, similar structures are available for SiGe HBT devices.

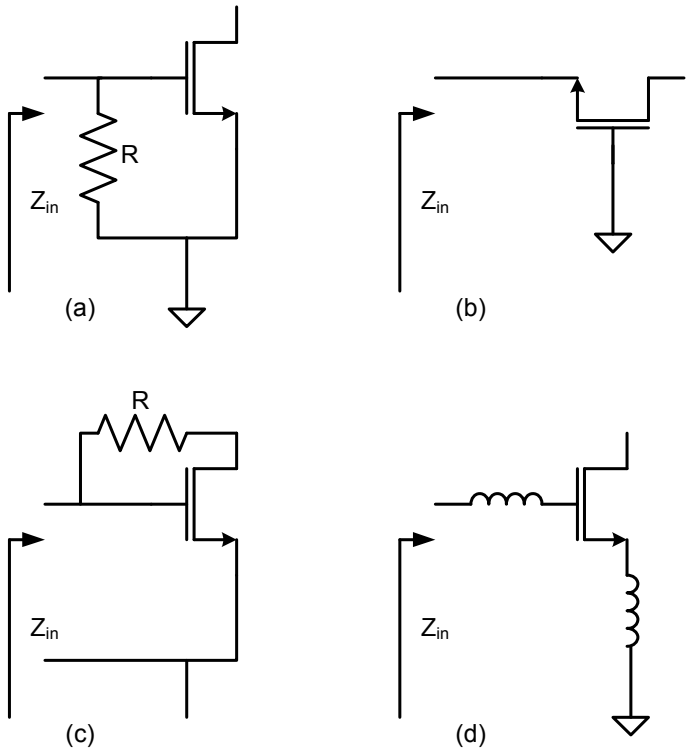


Figure 2.1 : Common LNA architectures. (a) Resistive termination, (b) $1/g_m$ termination, (c) shunt feedback, (d) inductive degeneration.

In the first architecture, resistive termination is used to provide 50 Ω impedance as shown in Figure 2.1 (a). This is the simplest method to obtain matching over a wide range of frequencies; however, the use of real resistors has destructive effects on the amplifier's noise performance (figure) due to the thermal noise of resistive termination. In order to examine the efficiency of this approach, the noise factor

definition is used. Noise factor of the circuit (LNA) with and without resistive termination are shown in equations (2.1), (2.2) respectively.

$$F \equiv \frac{Total\ output\ noise\ power}{Output\ noise\ power\ due\ to\ input\ source} = 1 + \frac{P_{na,i} + kT\Delta f G_a}{kT\Delta f G_a} = 2 + \frac{P_{na,i}}{kT\Delta f G_a} \quad \textbf{(2.1)}$$

$$F = 1 + \frac{P_{na,i}}{4kT\Delta f G_a} \quad \textbf{(2.2)}$$

where G_a is available power gain, $P_{na,i}$ is available noise power at the output due to the internal noise sources only and Δf is bandwidth. A sharp degradation in noise figure (about 6dB) is seen from equation (2.1) and (2.2) with the addition of the terminating resistor. This degradation has two reasons. First one is the added resistors own noise contribution which is equal to the noise contribution of the source resistance. Second one is the attenuation of the input signal causes the factor of 4 in the second term of (2.2). Another shortcoming of the resistive termination is that the input power is attenuated by the resistive divider before reaching the transistor which reduces the maximum power gain.

In Figure 2.1 (b), the second architectural approach is shown which is called $1/g_m$-termination and uses the source (or emitter) of a common-gate (or common-base) stage as the input termination. In common-gate or common-base architecture, the impedance looking into the source or emitter terminal of the active device is $1/g_m$. Therefore, proper bias and sizing of the LNA will result in $1/g_m = 50\ \Omega$ and satisfies the matching requirement. Under matching conditions, this architecture yields the following lower bounds on the noise factor for the cases of bipolar and CMOS amplifiers [13]:

Bipolar: $F = \frac{3}{2} = 1.76dB$

CMOS: $F = 1 + \frac{\gamma}{\alpha} \geq \frac{5}{3} = 2.2dB$

where $\alpha \equiv \frac{g_m}{g_{d0}}$

In the CMOS expression, γ is the coefficient of channel thermal noise, g_m is the device transconductance, and g_{d0} is the zero bias drain conductance. For long-channel devices $\gamma = 2/3$ and $\alpha = 1$. While determining the value of 2.2dB in the CMOS expression, short-channel effects ($\alpha \leq 1$) and excess thermal noise caused by hot electrons ($\gamma \geq 2/3$) are disregarded. The effect of base resistance in bipolar devices is neglected in the bipolar expression.

Figure 2.1 (c) introduces another architecture for achieving the required matching at the input port of the LNA is using shunt feedback. In this approach negative feedback provides the 50Ω impedance at the input port. This architecture also suffers from the thermal noise of the shunt resistor; however, the lower bound on noise factor is usually smaller than that of resistive and $1/g_m$-termination architectures since it does not reduce the signal with a noisy attenuator before amplifying [12]. Modified versions of this architecture that incorporate series feedback is widely used in wideband LNA applications [14-16].

All three preceding architectures suffer noise figure degradation from the presence of noisy resistance in the signal path. Feedback techniques are often used in LNA design to shift the optimum noise impedance Z_{opt} ($1/Y_{opt}$) to the desired point. The fourth architecture seen in Figure 2.1 (d), employs inductive source or emitter degeneration to generate a real term in the input impedance, thus this architecture overcomes the deleterious effects of real resistor on noise factor. Series feedback has been preferred to achieve simultaneous noise and impedance matching that is required at the input port of the LNA to deliver the maximum power from the antenna to the LNA, without degrading the noise performance of the circuit. That is why the series feedback with inductive source (or emitter) degeneration is applied to the common-source (or common-emitter) or cascode topologies in narrow-band applications [13].

On the other hand, conventional cascode amplifier will be used as the LNA, since cascode topology has the advantages of high operating frequency and frequency stability at high gain. Moreover, the common base (or common-gate) transistor of the

cascode topology provides high isolation between input and output terminals by avoiding Miller amplification of the base-collector capacitance of input transistor [17]. However, the common-base (or common-gate) transistor causes the slight increase in the noise figure and decrease in the output swing which are the drawbacks of the cascode topology with respect to the simple common-emitter (common-source) amplifier. Since this architecture offers the possibility of achieving the best noise performance of any architecture, following sections introduce a brief analysis of the inductively-degenerated cascode LNA to establish the principle of operation and the limits on noise performance.

2.2 Noise

In communication systems, noise is defined as any signal other than the desired signal and limits the minimum signal level that a circuit can process with acceptable quality. There are different types of noise sources which generate noise with different mechanisms.

2.2.1 Noise Sources

Noise is basically examined in two categories which are interference noise and inherent noise. Interference noise is due to unwanted interaction between the circuit and the different parts of the circuit itself. Power supply noise or electromagnetic interference between wires are the two most known sources of interference noise. This kind of noise can be significantly reduced by using appropriate circuit wiring or layout techniques.

Inherent noise is a result of fundamental properties of the devices and circuits, and is related to random noise signals which can be reduced but never eliminated. Inherent noise is only moderately affected by circuit wiring or layout, such as using multiple drain contacts or multiple gate transistors to change the resistance value of the drain or gate of a MOS transistor. The dominant inherent noise sources in integrated circuits are thermal noise, shot noise and flicker noise.

Thermally random motion of carriers in a conductor causes thermal noise, since this random motion constitutes fluctuations in the voltage measured across the conductor

even if the average current is zero. The power spectrum density of the thermal noise is exactly proportional to the absolute temperature (T) due to the thermal origin and given by the following quantity known as available noise power

$$P_{NA} = kT\Delta f \quad \textbf{(2.3)}$$

where k is the Boltzman constant (about 1.38 $\times 10^{23}$ J/K), T is the absolute temperature in Kelvins, and Δf is the bandwidth of the noise measured in Hz [12]. Spectral density of the available noise power displays the same value at all frequencies, therefore it is a white noise. The available noise power over 1Hz bandwidth at room temperature is -174 dBm and defined as noise floor of the system [18].

Shot noise is mainly caused by random flow of carriers through a potential barrier. Two conditions must be satisfied for shot noise to occur. There must be a direct current flow and there must also be a potential barrier over which the charge carriers hop [12]. The second condition implies that shot noise is specific to nonlinear devices such as diodes and transistors. Shot noise does not depend on temperature like thermal noise but on the current flow and the bandwidth as seen in the following equation:

$$\overline{i_n^2} = 2qI_{DC}\Delta f \quad \textbf{(2.4)}$$

where $\overline{i_n^2}$ is the rms (root mean square) noise current, q is the electronic charge (about $1.6\text{x}10^{-19}$ C), I_{DC} is the DC current in amperes, and Δf is the noise bandwidth in hertz. Shot noise is also white noise like thermal noise.

No universal mechanism for flicker noise, also known as 1/f noise or pink noise, has been identified. It seems to come from the macroscopic defects of the materials; therefore it describes the quality of the conductive medium. The power spectral density of flicker noise is inversely proportional to the frequency. Flicker noise does not depend on temperature but rather proportional to the current. Flicker noise is caused by randomly trapping and releasing of the charges in the defects and impurities of the channel region in MOS devices [12]. Since MOSFETs are surface

(planar) devices, they exhibit flicker noise much greater than bipolar transistors which are bulk devices. Furthermore, larger MOS devices experience less flicker noise since larger gate capacitance smoothes the fluctuations in the channel charge. The spectral density of this noise for MOS devices is given by:

$$\overline{i_{fn}^2} = \frac{K}{f} \cdot \frac{g_m^2}{WLC_{ox}^2} \cdot \Delta f \qquad \textbf{(2.5)}$$

where K is a device-specific constant, g_m is the transconductance of the MOS device, f is the operating frequency, C_{ox} is the gate-oxide capacitance per unit area, and W and L are the width and length of the MOS device, respectively.

2.2.2 Classical Two-port Noise Theory

Noise performance of a circuit is usually characterized by a parameter called noise factor (F) or noise figure (NF ≡ 10 log F) that represents how much the given system degrades the signal-to-noise ratio [19].

$$F \equiv \frac{\left(\frac{S}{N}\right)_{in}}{\left(\frac{S}{N}\right)_{out}} = \frac{Total\ output\ noise\ power}{Output\ noise\ power\ due\ to\ input\ source} \qquad \textbf{(2.6)}$$

Consider the noisy two port network shown in Figure 2.2 (a).

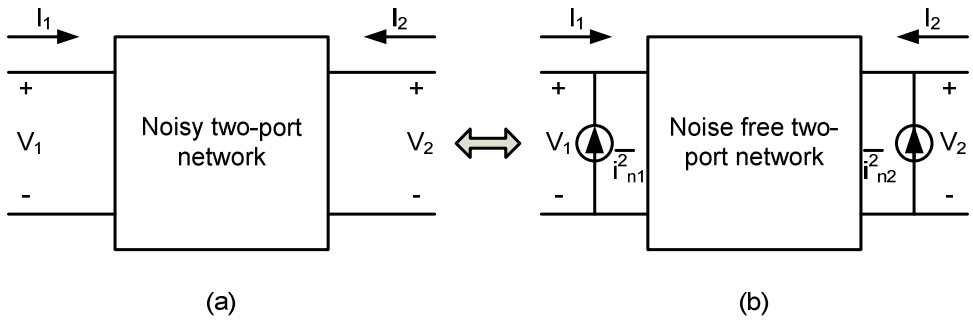


Figure 2.2 : (a) Noisy two-port network, (b) Equivalent network with input and output noise current sources.

The total noise in the network can be represented by two independent noise sources at the input and outputs of the network. So, the admittance matrix representation will be as follows:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} + \begin{bmatrix} i_{n1} \\ i_{n2} \end{bmatrix} \tag{2.7}$$

By rearranging the parameters, the admittance representation can be converted to the inversed hybrid representation:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} + \begin{bmatrix} i_n \\ e_n \end{bmatrix} \tag{2.8}$$

where all the noise sources are transformed to the input of network and are represented by voltage and current noise sources, e_n and i_n:

$$e_n = -\frac{1}{Y_{21}} i_{n2} \qquad and \qquad i_n = i_{n1} - \frac{Y_{11}}{Y_{21}} i_{n2} \tag{2.9}$$

Using this simplification the network model shown in Figure 2.3 is obtained, where the noisy admittance, Y_s, and the corresponding parallel current noise are connected to the input of the network. Assuming that the two-port network and the source noise are uncorrelated, then by using the definition in (2.6) the expression for noise factor of the network can be written as:

$$F = \frac{\overline{i_s^2} + \overline{\left| i_n + Y_s e_n \right|^2}}{i_s^2} \tag{2.10}$$

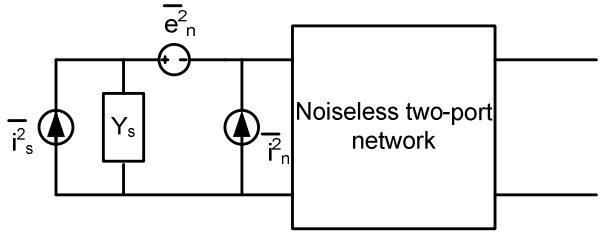


Figure 2.3 : Input referred equivalent noise model.

Note that, (2.10) does not assume that the internal noise sources i_n and e_n are uncorrelated, although the noise of the source and two equivalent noise generators of the two-port-network are assumed to be uncorrelated with each other. To include the correlation between e_n and i_n, i_n can be expressed as the sum of two components:

$$i_n = i_c + i_u \tag{2.11}$$

where i_c is correlated with e_n and i_u is uncorrelated with e_n. Since i_c is correlated with e_n, it can be treated as proportional to e_n through a constant known as the correlation admittance Y_c.

$$i_c = Y_c e_n \tag{2.12}$$

After combining these equations, the noise factor expression can be written as follows:

$$F = \frac{\overline{i_s^2} + \overline{\left|i_u + (Y_c + Y_s)e_n\right|^2}}{i_s^2} = 1 + \frac{\overline{i_u^2} + \left|Y_c + Y_s\right|^2 \overline{e_n^2}}{i_s^2} \tag{2.13}$$

The three independent noise sources in the expression (2.13) can be treated as thermal noise sources and represented by an equivalent resistance or conductance:

$$R_n \equiv \frac{\overline{e_n^2}}{4KT\Delta f} \tag{2.14}$$

$$G_u \equiv \frac{\overline{i_u^2}}{4KT\Delta f} \tag{2.15}$$

$$G_s \equiv \frac{\overline{i_s^2}}{4KT\Delta f} \tag{2.16}$$

The expression for noise factor can be written as follows by substituting these equivalences and decomposing each admittance into the sum of conductance G and susceptance B:

$$F = 1 + \frac{G_u + \left|Y_c + Y_s\right|^2 R_n}{G_s} = 1 + \frac{G_u + \left[\left(G_c + G_s\right)^2 + \left(B_c + B_s\right)^2\right] R_n}{G_s} \quad \textbf{(2.17)}$$

Since the last expression shows the dependence of noise factor on the conductance and susceptance of the source, it can be used to identify the general conditions in order to minimize the noise factor. By taking the first derivative of (2.17) with respect to the source admittance, the optimum values of G_s, B_s and minimum noise factor are obtained as follows:

$$B_{opt} = -B_c \quad \textbf{(2.18)}$$

$$G_{opt} = \sqrt{\frac{G_u}{R_n} + G_c^2} \quad \textbf{(2.19)}$$

$$F_{\min} = 1 + 2R_n\left[\sqrt{\frac{G_u}{R_n} + G_c^2} + G_c\right] \quad \textbf{(2.20)}$$

It is also possible to express the noise factor in terms of F_{min} and the source admittance [18]:

$$F = F_{\min} + \frac{\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right] R_n}{G_s} \quad \textbf{(2.21)}$$

In equation (2.21), the second term has a multiplier consists of the ratio of R_n/G_s. Noise equivalent resistance, R_n shows the relative sensitivity of the noise factor when the source conductance is constant. A large R_n denotes high sensitivity that makes difficult to achieve optimum conditions.

2.2.3 Noise Analysis of the Inductively-Degenerated SiGe HBT LNA

In this part of the study, noise sources of SiGe HBT devices will be introduced at first. Then the design procedure of simultaneous noise and input matching of the inductively-degenerated SiGe HBT LNA will be explained through analytical expressions in detail.

2.2.3.1 Noise Sources of SiGe HBT Devices

The primary RF noise sources in a bipolar transistor are the base current shot noise, the collector current shot noise, and the total base resistance and series emitter resistance thermal noise. The base current shot noise results from the flow of base majority holes across the emitter-base junction potential barrier and expressed as [20]:

$$\overline{i_b^2} = 2qI_B\Delta f \quad \textbf{(2.22)}$$

where I_B is DC base current, , q is the electronic charge (about $1.6\text{x}10^{-19}$ C), and Δf is the noise bandwidth in Hertz. I_B appears in the base shot noise, since the amount of hole current overcoming the emitter-base junction barrier is determined by the minority hole current in the emitter I_B [20]. In a similar manner, the collector current shot noise result from the flow of emitter majority electrons over the emitter-base junction potential barrier, and has a spectral density of

$$\overline{i_c^2} = 2qI_C\Delta f \quad \textbf{(2.23)}$$

The collector-base junction is usually reverse-biased for low noise amplification, therefore transition of carriers across the collector–base junction is a drift process and a DC current passing through such a junction alone does not have intrinsic shot noise. The shot noise observed at the collector is caused by the electron current injected into the collector–base junction from the emitter that already has shot noise [21].

Thermal noises due to the total base resistance and series emitter resistance can be expressed as below respectively:

$$\overline{i_{n,b}^2} = 4kT\frac{1}{r_b}\Delta f \quad \textbf{(2.24)}$$

$$\overline{i_{n,e}^2} = 4kT\frac{1}{r_e}\Delta f \quad \textbf{(2.25)}$$

where r_b is total base resistance and r_e is series emitter resistance. As a result of these analyses, dominant sources of noise in SiGe HBT devices can be demonstrated as in Figure 2.4.

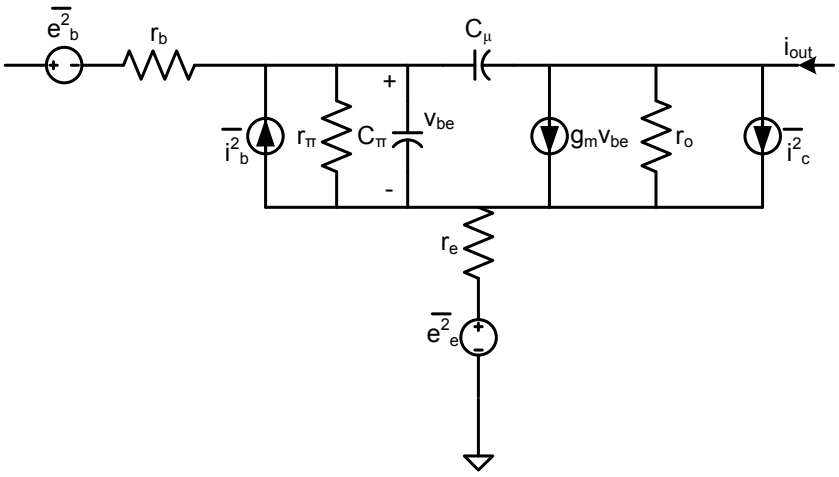


Figure 2.4 : Dominant noise sources of SiGe HBT.

2.2.3.2 Noise Parameters of SiGe HBT Devices

The amount of noise added by the amplifier is a function of the source termination in addition to the details of noise source locations and noise propagation paths inside the amplifier. For a source termination admittance $Y_s = G_s+jB_s$, noise figure reaches its minimum when $Y_s=Y_{opt}$. In Figure 2.5 two-port network model for SiGe HBT device is shown which is used in derivation of noise parameters of the device.

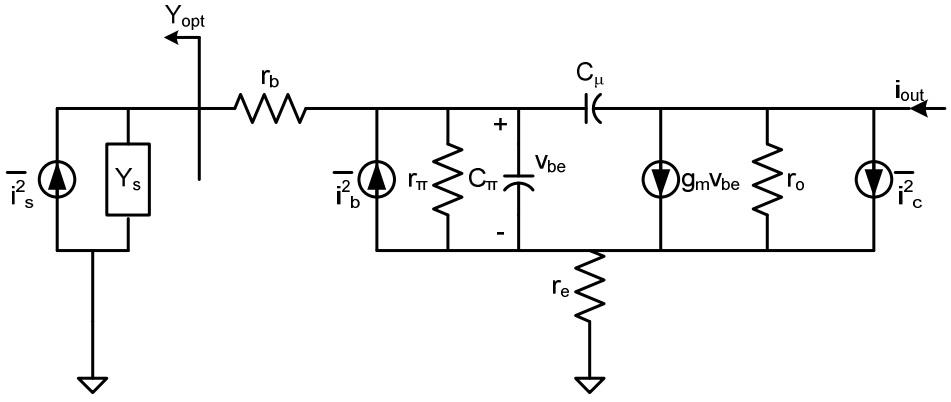


Figure 2.5 : Two-port network model of SiGe HBT devices for noise calculations.

While deriving noise parameter expressions the base and collector current shot noises are assumed to be uncorrelated. Under this assumption, noise parameter equations can be written as:

$$R_n = (r_b + r_e) + \frac{1}{2g_m} \tag{2.26}$$

$$G_{opt} = \sqrt{\frac{g_m}{2R_n}\frac{1}{\beta} + \frac{1}{2R_n}\frac{\omega}{\omega_T}\left(1 - \frac{1}{2g_m R_n}\right)} \tag{2.27}$$

$$B_{opt} = -\frac{\omega C_{in}}{2g_m R_n} = -\frac{1}{2R_n}\frac{\omega}{\omega_T} \tag{2.28}$$

$$F_{\min} = 1 + \frac{1}{\beta} + \sqrt{2g_m(r_b + r_e)}\sqrt{\frac{1}{\beta} + \left(\frac{\omega}{\omega_T}\right)^2} \tag{2.29}$$

where g_m is the transconductance of the transistor, β is the current gain, and C_{in} is the total of base-collector and base-emitter capacitances.

R_n is directly proportional to the base resistance and independent of frequency. The sensitivity of noise factor to deviations of source termination from Y_{opt} is determined by R_n, therefore too keep noise factor close to $F_{min,}$ r_b must be as small as possible. As seen from equation (2.28), imaginary part of the optimum noise admittance is negative. Therefore to provide noise matching of the imaginary part, a series inductance is required. Additionally, the absolute value of B_{opt} increases with frequency. Equation (2.27) indicates that real part of the optimum admittance generally increases with collector current and frequency. Finally, the monolithic increase in the minimum noise factor with frequency is observed from equation (2.29). The frequency $f = f_T / \sqrt{\beta}$ defines a transition of F_{min} from white noise behavior to 10dB/decade increase as the frequency increases [21]. Also equation (2.29) indicates that r_b is the key for reducing F_{min} for frequencies higher than $f_T / \sqrt{\beta}$.

The noise parameters scale with emitter length and biasing current. Noise resistance R_n scales with inverse of emitter length, like r_b. Optimum noise admittance Y_{opt} scales with emitter length. Minimum noise factor F_{min} is only a function of operating current density, thus remains invariant to the changes in emitter length.

2.2.3.3 Simultaneous Noise and Input Matching in SiGe HBT LNA

While minimizing the noise figure of the LNA, the size and biasing of the transistor are important because bipolar transistors show an optimum noise current density ten times smaller than their peak f_T current density, since the thermal noise caused by parasitic emitter and base resistance is dominant at low current densities and shot noise is dominant at high current densities [22]. Therefore, the size and biasing of the transistor is first designed so that the transistor becomes noise matched to the characteristic impedance of the system, typically 50 Ω at the desired frequency. Finally, to complete the circuit, an appropriate passive network is designed to provide input impedance matching with the lowest possible degradation of the overall noise figure. The passive network itself also contributes to noise, hence degrades the noise figure of the circuit.

As the first design step, the optimal noise current density must be determined in order to achieve minimum noise figure. Since the minimum noise figure and optimum noise current density is practically independent from the emitter length, the emitter length of the device is chosen so as to make R_{opt} equal to the real part of the Z_s at given noise current density and desired frequency [22].

Figure 2.6 shows an inductively-degenerated cascode HBT LNA with its simplified small signal equivalent circuit including the intrinsic transistor noise model for noise analysis. Since cascode topology is selected base-collector capacitance and the effects of common-base transistor on the frequency response and noise are neglected as in CMOS case. To understand how the matching network affects the noise performance of the LNA, noise parameters and noise factor of the cascode LNA with and without inductive degeneration will be compared.

Inductive degeneration is required to match the real part of the input impedance expressed in equation (2.30) to the real part of Z_s. Since inductances used in the matching network are assumed to be lossless, emitter inductor L_e does not introduce additional noise to the circuit. Therefore, as can be seen from equations (2.32)-(2.34), the values of noise parameters, R_{opt}, F_{min}, R_n are not changed by the emitter inductor while the value of optimum source reactance X_{opt} is reduced by ωL_e. From now on,

the superscript "ii" in the equations denotes that the parameters are for inductively-degenerated SiGe HBT LNA topology.

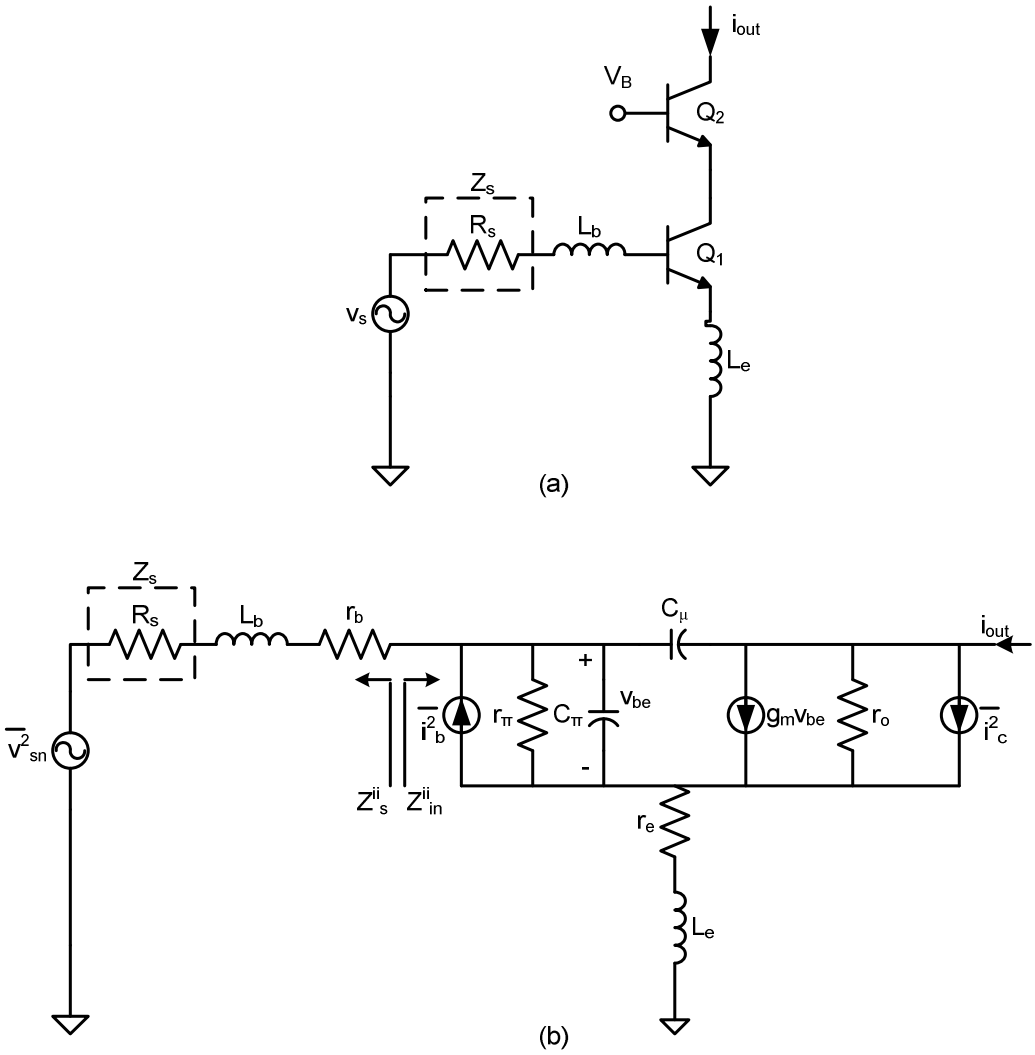


Figure 2.6 : (a) Schematic of inductively-degenerated cascode SiGe HBT LNA topology. (b) Small-signal equivalent of inductively-degenerated cascode SiGe HBT LNA topology

$$Z_{in}^{ii} = \omega_T L_e + j\omega\left(L_b + L_e\right) - \frac{1}{j\omega C_{in}} \qquad \textbf{(2.30)}$$

$$F^{ii} \cong 1+\frac{r_b+r_e}{R_s}+\frac{g_m R_s}{2\beta}\left[1+\left(\frac{\omega(L_b+L_e)}{R_s}\right)^2\right]+\frac{g_m R_s}{2}\left(\frac{\omega}{\omega_T}\right)^2 + \frac{\left[1-\omega^2(L_b+L_e)(C_{in})\right]}{2g_m R_s} \tag{2.31}$$

$$R_n^{ii} = (r_b+r_e)+\frac{1}{2g_m} \tag{2.32}$$

$$Z_{opt}^{ii} = \frac{R_n\frac{\omega_T}{\omega}\sqrt{\frac{g_m}{2}(r_e+r_b)\left(1+\frac{1}{\beta}\left(\frac{\omega_T}{\omega}\right)^2\right)+\frac{1}{4\beta}\left(\frac{\omega_T}{\omega}\right)^2}+j\frac{R_n}{2}\frac{\omega_T}{\omega}}{\frac{g_m}{2}(r_e+r_b)\left(1+\frac{1}{\beta}\left(\frac{\omega_T}{\omega}\right)^2\right)+\frac{1}{4\beta}\left(\frac{\omega_T}{\omega}\right)^2+\frac{1}{4}} - j\omega L_e \tag{2.33}$$

$$F_{\min}^{ii} = 1+\frac{1}{\beta}+\sqrt{2g_m(r_b+r_e)}\sqrt{\frac{1}{\beta}+\left(\frac{\omega}{\omega_T}\right)^2} \tag{2.34}$$

If $\omega >> \omega_T/\sqrt{\beta}$ satisfied, the expression for X_{opt} (2.33) can be simplified to the expression in (2.35). Therefore X_{opt} for inductively-degenerated circuit can be expressed as in (2.36).

$$X_{opt} \cong \frac{1}{\omega C_{in}} \tag{2.35}$$

$$X_{opt}^{ii} \cong \frac{1}{\omega C_{in}} - \omega L_e \tag{2.36}$$

By adding the base inductance L_b that satisfies equation (2.37), simultaneous noise and impedance matching is finally achieved, since base inductance L_b cancels out the reactance due to the input capacitance C_{in} of the device and also it transforms the optimum noise reactance of the amplifier to 0 Ω [22].

$$\omega^2 \left(L_b + L_e\right) C_{in} \cong 1 \tag{2.37}$$

Under matching conditions, noise factors of the cascode LNA with and without input matching network is shown in equations (2.38) and (2.39).

$$F \cong 1 + \frac{r_b + r_e}{R_s} + \frac{g_m R_s}{2\beta} + \frac{1}{2 g_m R_s} + \frac{g_m R_s}{2}\left(\frac{\omega}{\omega_T}\right)^2 \tag{2.38}$$

$$F^{ii} \cong 1 + \frac{r_b + r_e}{R_s} + \frac{g_m R_s}{2\beta} + \frac{1}{2\beta g_m R_s}\left(\frac{\omega_T}{\omega}\right)^2 + \frac{g_m R_s}{2}\left(\frac{\omega}{\omega_T}\right)^2 \tag{2.39}$$

In equation (2.38), the term $\left(r_b + r_e\right)/R_s$ is the thermal noise contribution of the parasitic base and emitter resistances, the following term is due to shot noise of the base current and the remaining two terms are white and frequency dependent components produced by collector shot noise. When these two equations are compared, it can be seen that white noise term due to I_C is disappeared and a new frequency dependent term related to the base current is produced with the addition of the emitter inductor L_e. Although the noise factor is greatly improved, by decreasing the noise contributions caused by base current shot noise and parasitic base and emitter resistances further improve can be provided in [17].

2.2.4 Noise Analysis of the Inductively-Degenerated CMOS LNA

In this part of the study, noise sources of CMOS devices will be introduced at first. Then the design procedure of simultaneous noise and input matching of the inductively-degenerated CMOS LNA will be explained through analytical expressions in detail.

2.2.4.1 Noise Sources of CMOS Devices

MOS devices are fundamentally voltage-controlled resistors; therefore one should expect a thermal noise associated with the carriers in the channel similar to the noise of carriers in a conductor. The following expression for the drain current noise of MOS devices, also known as channel thermal noise, has been derived by Van der Ziel in [23]:

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f \quad \textbf{(2.40)}$$

where g_{d0} is zero-bias drain conductance of the device and γ is bias and technology dependent parameter that takes value between 2/3 and 1, for long-channel devices in saturation and drain-source voltage is zero. In short channel devices operating in the saturation region γ is much greater than 2/3 [13]. For instance, MOS devices with 0.7 μm channel length, the value of γ may be between 2 and 3, depending on the bias conditions [24]. This excess noise due to carrier heating by large electric fields is commonly encountered in short channel devices [12].

Another thermal noise source in MOS devices is associated with the substrate resistance, R_{sub}. Since the channel to bulk capacitance C_{cb}, can be ignored at frequencies low enough, thermal noise due to substrate resistance contribute to noisy drain current by modulating the back gate potential.

$$\overline{i_{nd,sub}^2} = \frac{4kTR_{sub}g_{mb}^2}{1+\left(\omega R_{sub}C_{cb}\right)^2}\Delta f \quad \textbf{(2.41)}$$

As seen in equation (2.41), the substrate thermal noise loses its importance at frequencies well above the pole formed by C_{cb} and R_{sub}. This pole is around 1GHz in many CMOS IC processes [12], therefore excess noise contributed due to this mechanism can be ignored for our operating frequency that is 5.8 GHz.

Distributed resistance of the gate terminal generates additional noise in MOS devices [25]. For noise purposes; the value of this resistance is given by [26]:

$$R_g = \frac{R_{\square}W}{3n^2L} \quad \textbf{(2.42)}$$

where $R_{\square}$ is the sheet resistance of the polysilicon gate terminal, n is the number of gate fingers in the layout of the device, W is the total gate width of the device and L is gate length of the device. The factor 1/3 is the result of distributed analysis of the gate terminal that assumes each gate finger contacted at only one end. Contacting both ends results in reducing of this factor to 1/12. Therefore, by using appropriate

layout techniques, the value of this resistance thus, the noise contribution of this source can be reduced significantly.

The gate resistance plays similar role with base resistance in bipolar devices, however base resistance is much more significant since it can not be minimized without the need for increased power consumption [13].

In addition to the noise sources introduced above, the thermal agitation of channel charge causes fluctuations in the channel potential that leads to a noisy gate current due to the capacitive coupling. For MOS devices operating in the saturation region, this extra noise was modeled by introducing a frequency-dependent gate conductance, g_g, and an equivalent gate current noise is expressed as [23]:

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \tag{2.43}$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \tag{2.44}$$

where δ is the technology-dependent gate noise coefficient that is generally equal to 4/3 for long channel devices. Like drain noise coefficient γ, the value of δ also increases in short channel devices. As seen from equations (2.43) and (2.44), the gate current noise power spectral density is proportional to ω^2, thus gate current noise is not a white noise unlike the drain current noise.

Note that the gate current noise is partially correlated with the drain noise and their correlation coefficient is given by [23]:

$$c \equiv \frac{\sqrt{i_{ng} i_{nd}^*}}{\sqrt{\overline{i_{ng}^2}\,\overline{i_{nd}^2}}} \tag{2.45}$$

where c is a complex number and its value is theoretically computed to be around –0.395j for long channel devices [23], but short channel MOS devices exhibit larger values of correlation coefficient [19]. The purely imaginary value of c indicates the capacitive coupling between the channel and the gate induced noise sources. As a

result of these analyses, dominant sources of noise in MOS devices can be demonstrated as shown in Figure 2.7.

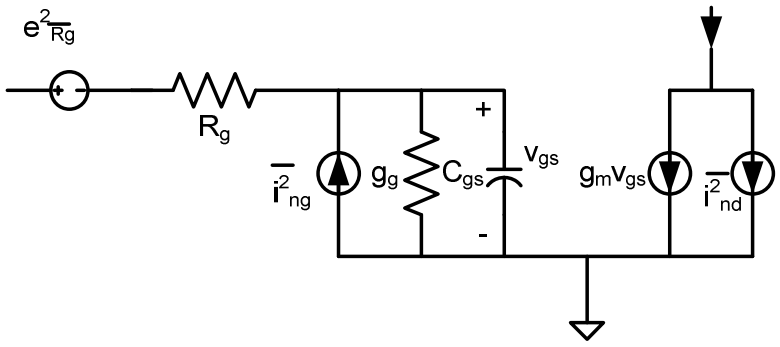


Figure 2.7 : Dominant noise sources of MOS devices

2.2.4.2 Noise Parameters of CMOS Devices

In order to achieve minimum noise figure, the optimum noise admittance Y_{opt} must be equal to the termination admittance, Y_s. The expressions for noise parameters F_{min}, R_n, B_{opt} and G_{opt} can be derived for a MOS device by considering a two-port network model for the MOS device shown in Figure 2.8. While deriving these equations (2.46) - (2.49), it is assumed that drain current noise and gate induced current noises are the dominant noise sources of MOS devices.

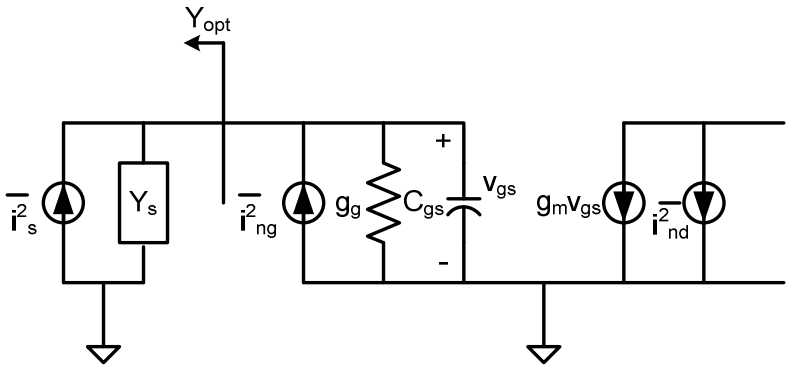


Figure 2.8 : Two-port network model of MOS devices for noise calculations.

$$R_n = \frac{\gamma}{\alpha g_m} \tag{2.46}$$

$$G_{opt} = \alpha\omega C_{gs}\sqrt{\frac{\delta}{5\gamma}\left(1-\left|c^2\right|\right)} \tag{2.47}$$

$$B_{opt} = -\omega C_{gs}\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \tag{2.48}$$

$$F_{\min} = 1+\frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta\left(1-|c|^2\right)} \tag{2.49}$$

where α is the ratio of g_m and g_{d0} and its value is equal to one for long channel devices and decreases with the scaling down of the channel length.

Equation (2.49) indicates that as the channel length of the CMOS devices decreases, noise figure performances of these devices improve since transition frequency ω_T is inversely proportional to the effective channel length. On the other hand, g_{d0}, g_m and C_{gs} scale linearly with the device width W, while noise factors δ, γ and c are width independent. Therefore real and imaginary parts of the optimum noise admittance are proportional to device width W while noise resistance scales inversely with W. Minimum noise factor F_{min} is independent from the device width. Since larger device width results in decrease in the noise resistance R_n, it provides the chance of lowering the noise figure and decreases the sensitivity to the deviation between termination admittance and optimum noise admittance. However, the power constraint is set by the upper limit of the device width.

2.2.4.3 Simultaneous Noise and Input Matching in CMOS LNA

Figure 2.9 shows an inductively-degenerated cascode CMOS LNA with its simplified small signal equivalent circuit including the intrinsic transistor noise model for noise analysis. Since cascode topology is selected, the gate-drain capacitance can be neglected during the analysis. Moreover, the effects of common-gate transistor on the frequency response and noise are neglected, as well as the parasitic resistances of gate, source, drain and bulk terminals [12].

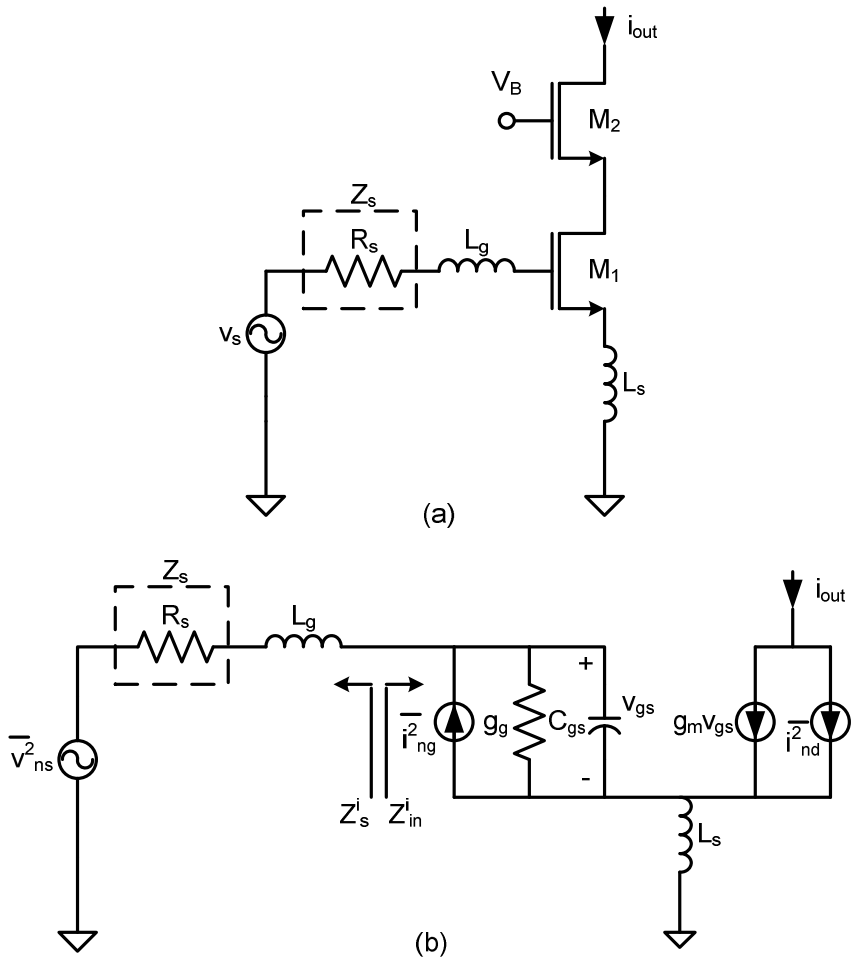


Figure 2.9 : (a) Schematic of inductively-degenerated cascode CMOS LNA topology. (b) Small-signal equivalent of inductively-degenerated cascode CMOS LNA topology.

Assuming inductances are lossless the noise factor and noise parameters can be expressed as in equations (2.50) - (2.53). The superscript "i" in the equations denotes the parameters are for inductively-degenerated cascode CMOS LNA topology. When noise parameter expressions of input transistor without inductive degeneration compared to that of with inductive degeneration, it can be seen that only the optimum noise impedance Z_{opt} is shifted due to the inductive source degeneration, the other noise parameters F_{min} and R_n are not affected from this degeneration.

$$F^i = 1 + \frac{1}{g_m^2 R_s}\left\{\begin{array}{l}\gamma g_{d0}\left\{\begin{array}{l}\left[1-\omega^2 C_{gs}\left(L_g+L_s\right)\left(1+|c|\alpha\sqrt{\frac{\delta}{5\gamma}}\right)\right]^2 \\ +\left(\omega C_{gs} R_s\right)^2\left(1+|c|\alpha\sqrt{\frac{\delta}{5\gamma}}\right)^2\end{array}\right\} \\ +\frac{\alpha\delta}{5}\left(1-|c|^2\right) g_m\left(\omega C_{gs}\right)^2\left(R_s^2+\omega^2 L_g^2\right)\end{array}\right\} \quad \textbf{(2.50)}$$

$$R_n^i = \frac{\gamma}{\alpha}\frac{1}{g_m} \quad \textbf{(2.51)}$$

$$Z_{opt}^i = \frac{\alpha\sqrt{\frac{\delta}{5\gamma\left(1-|c|^2\right)}} + j\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs}\left\{\frac{\alpha^2\delta}{5\gamma\left(1-|c|^2\right)}+\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} - j\omega L_s \quad \textbf{(2.52)}$$

$$F_{\min}^i = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta\left(1-|c|^2\right)} \quad \textbf{(2.53)}$$

As shown in Figure 2.9 (b), the input impedance Z_{in} of the source degenerated LNA is given by

$$Z_{in}^i = j\omega L_s + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} = j\omega L_s + \frac{1}{j\omega C_{gs}} + \omega_T L_s \quad \textbf{(2.54)}$$

The source degeneration generates the real part at the input impedance of the given LNA. Since there is no real part in Z_{in} without inductive degeneration, while there is in Z_{opt}, discrepancy between the real parts of Z_{opt} and Z_{in} can be reduced by the help of appropriately chosen degeneration inductance L_s. Additionally, the imaginary part of Z_{in} is changed by ωL_s, as shown in equation (2.54) and Z_{opt} changes in the same manner. Therefore, from equations (2.52) and (2.54), inductive source degeneration helps to bring Z_{opt} close to complex conjugate of the optimum source

impedance $\left(Z_{in}^{i}\right)^{*}$ that provides possibility of achieving simultaneous noise and input matching without causing any degradation in F_{min} and R_n.

Conditions that must be satisfied for simultaneous noise and impedance matching are given in the following equations. It can be said that conditions in equations (2.55) - (2.56) are satisfied based on the equations (2.52) and (2.54), (2.56) and (2.58), therefore the design parameters gate-source potential of the input transistor V_{gs}, the transistor size W (or C_{gs}) with minimum channel length since minimum channel length maximizes the transition frequency and source degeneration inductor L_s. Since the mismatch in Z_{opt} directly affects the noise performance of the LNA, values of design parameters must be determined such that they satisfy the equations (2.55) - (2.58) for a given value of Z_s.

$$\mathrm{Re}\left\{Z_{opt}^{i}\right\} = \mathrm{Re}\left\{Z_{s}^{i}\right\} \quad \textbf{(2.55)}$$

$$\mathrm{Im}\left\{Z_{opt}^{i}\right\} = \mathrm{Im}\left\{Z_{s}^{i}\right\} \quad \textbf{(2.56)}$$

$$\mathrm{Re}\left\{Z_{in}^{i}\right\} = \mathrm{Re}\left\{Z_{s}^{i}\right\} \quad \textbf{(2.57)}$$

$$\mathrm{Im}\left\{Z_{in}^{i}\right\} = \mathrm{Im}\left\{Z_{s}^{i}\right\} \quad \textbf{(2.58)}$$

Assuming that the source impedance is fixed to a given value (i.e. 50 Ω), the procedure for determining optimum size and biasing of the input transistor and values of passive components of the input matching network can be explained as follows. Firstly, the channel length of the input transistor is chosen as small as possible in the given technology since it yields better noise figure because of the reasons stated before. Secondly, channel width of the input transistor (W) is chosen that satisfies equation (2.55) and the given power constraint at its biasing conditions. Third step is determining the value of the degeneration inductance L_s to ensure equation (2.58). Then for the selected values of W and L_s, gate-source voltage of the input transistor V_{gs}, is determined from equation (2.57). Note that, for given values of L_s, the imaginary part of the optimum source admittance would be approximately

equal to the imaginary part of the input impedance with an opposite sign automatically for typical values of advanced CMOS technology [24]. Finally, the value of series inductance L_g is adjusted to cancel the imaginary part of the input impedance. This design methodology provides obtaining LNA with noise figure approximately equal to the F_{min} of the common-source transistor with nearly perfect input matching.

On the other hand, there is an optimum gate bias voltage (or overdrive voltage) for noise at a specific drain current which is important while determining V_{gs} of the input transistor [19]. This behavior can be explained by the help of the expression below which includes the drain conductance g_{d0}, drain noise coefficient γ, and induced gate noise coefficient δ.

$$F^i \approx 1 + \frac{\gamma g_{d0}}{G_s}\left(\frac{\omega}{\omega_T}\right)^2 + G_s \frac{2}{5}\frac{\delta}{g_{d0}} \qquad \textbf{(2.59)}$$

The drain conductance which is linearly scaled with the device width decreases with the increase in the gate bias voltage for a fixed drain current. The given equation has two independent noise components that have opposite bias dependence to each other. The drain conductance g_{d0} is seen in the numerator of the second term and in the denominator of the third term denotes that drain current noise is dominant at lower levels of the gate bias and induced gate noise is dominant at higher levels of the gate bias. Therefore noise figure has a minimum value where two of the noise components contribute equally to the noise figure.

2.3 Nonlinear Effects

Linearity is an important design consideration for a LNA in addition to noise figure, gain and input matching to guarantee that it remains linear when receiving weak signals in the presence of strong interferers [12]. Since the dynamic range (DR) is usually defined as the ratio of the maximum input signal level that the circuit can tolerate to the minimum input signal level while providing reasonable signal quality, the LNA must have a large DR [3]. The maximum input power that the circuit can maintain its nearly linear operation is usually defined as the upper limit of DR in

low-frequency applications. However, in high-frequency applications, nonlinear effects such as intermodulation distortion or signal gain compression may limit this upper bound.

The most commonly used measures are the 1-dB compression point (P_{1dB}) and third order intercept point (IP_3) [12]. When a sinusoid $x(t) = A\cos(\omega t)$ is applied to a nonlinear system with an input-output relation as seen in equation (2.60), the system generates frequency components that are integer multiples of the input signal frequency at the output called as harmonics seen in equation (2.61).

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \tag{2.60}$$

$$\begin{aligned} y(t) &= a_1 A\cos(\omega t) + a_2 A^2 \cos^2(\omega t) + a_3 A^3 \cos^3(\omega t) \\ &= a_1 A\cos(\omega t) + \frac{a_2 A^2}{2}\left(1 + 2\cos(2\omega t)\right) + \frac{a_3 A^3}{4}\left(3\cos(\omega t) + \cos(3\omega t)\right) \\ &= \frac{a_2 A^2}{2} + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t) + \frac{a_3 A^3}{4}\cos(3\omega t) \end{aligned} \tag{2.61}$$

The small signal gain of a circuit is usually obtained by ignoring harmonics. However, as the input signal amplitude increases the gain of the circuit approaches zero for sufficiently high input levels, since the output is a compressive or saturating function of the input in most circuits. In RF circuits, "1-dB compression point" is a measure of this effect and defined as the input signal level at which small signal gain drops 1dB below its nominal value as seen in Figure 2.10. Since the input signals that exceed the compression point are usually clipped or saturated at the output, the dynamic range of the LNA is limited by the compression point.

The multiplication of the input signal with its harmonics is another issue that may cause signal distortion. This mixing (multiplication) produces output terms known as intermodulation products (IMP) that are not harmonics of the input frequency. In order to explain how a nonlinear system with input-output relation seen in equation (2.60), leads to intermodulation, assume the input consists of two close signals:

$$x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \tag{2.62}$$

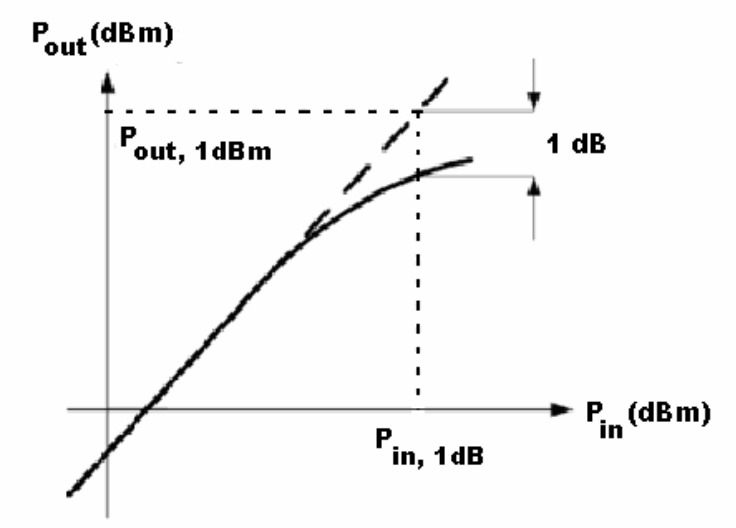


Figure 2.10 : 1-dB compression point [18].

Thus, the output of the system will be as follows:

$$\begin{aligned} y(t) = {} & \alpha_1 \left(A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \right) + \alpha_2 \left(A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \right)^2 \\ & + \alpha_3 \left(A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t) \right)^3 \end{aligned} \tag{2.63}$$

By arranging equation (2.63), the following intermodulation products can be obtained.

$$\omega = 2\omega_1 \pm \omega_2 \ : \qquad \alpha_2 A_1 A_2 \cos(\omega_1 + \omega_2) t + \alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2) t \tag{2.64}$$

$$\omega = 2\omega_1 \pm \omega_2 : \qquad \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 + \omega_2) t + \frac{3\alpha_3 A_1^2 A_2}{4} \cos(2\omega_1 - \omega_2) t \tag{2.65}$$

$$\omega = 2\omega_1 \pm \omega_2 : \qquad \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_2 + \omega_1) t + \frac{3\alpha_3 A_2^2 A_1}{4} \cos(2\omega_2 - \omega_1) t \tag{2.66}$$

where fundamental components are

$$\omega = \omega_1, \omega_2 \quad : \quad \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2\right)\cos(\omega_1 t) + \left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2\right)\cos(\omega_2 t) \tag{2.67}$$

The third-order intermodulation products are at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ and when ω_1 and ω_2 are close to each other, these products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ occur in the vicinity of the ω_1 and ω_2 as seen in Figure 2.11.

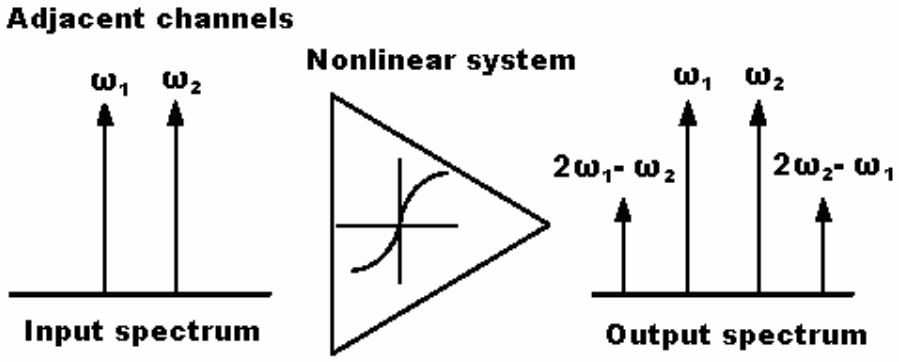


Figure 2.11 : Signal spectrum of a nonlinear system.

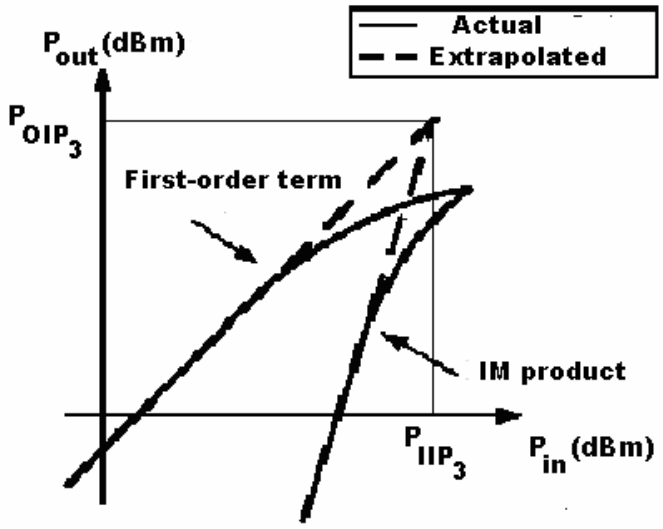


Figure 2.12 : Graphical interpretation of IIP_3 [18].

The third intercept point (IP_3) is a performance metric which has been defined to characterize corruption of signals due to third-order intermodulation product of two close interferes and measured by two tone test in which amplitudes of interferers are chosen equal [3]. As seen in Figure 2.12, as the amplitude of the input signals increase, first-order terms do not grow as fast as the third-order intermodulation products since first-order terms increase linearly with the amplitude (A) while intermodulation products increase proportional to A^3. The input level for which fundamental terms and IMP at the output have the same amplitude is called third-order input intercept point (IIP_3) which can be expressed as:

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.68}$$

2.4 Output Matching

Impedance matching at the input is always required, whereas it is only necessary at the output when the LNA drives an image filter. Since in integrated receivers, the image filter is driven by the antenna, the LNA can be directly connected to the mixer; thus output matching is not required in this case [17].

2.5 Stability

In addition to the parameters introduced in the previous sections, stability is an important concern in LNA design. Therefore, in this section, stability (tendency for oscillation) of low noise amplifiers is examined using scattering parameters (S-parameters) as design tools.

LNA may become unstable for certain combinations of source and load impedances due to feedback paths from the output to the input. Stern stability factor is a constant that is used to characterize the stability of circuits and defined as [3]:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \quad \textbf{(2.69)}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. When K is greater than unity and Δ is smaller than unity, then the circuit is unconditionally stable for any combination of source and load impedances.

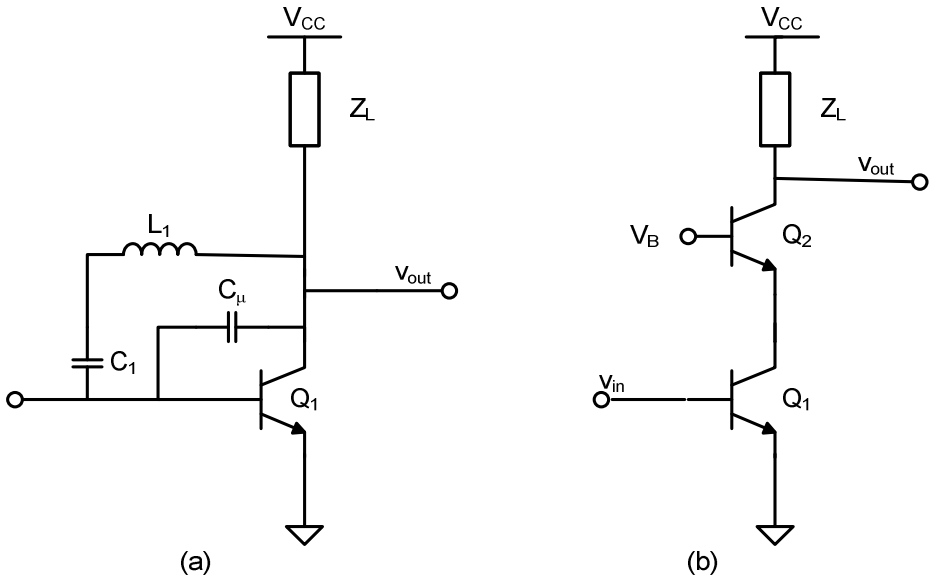


Figure 2.13 : Stabilization by (a) neutralization (b) cascoding.

As seen from equation (2.69), stability improves when S_{12} decreases due to increase in the reverse isolation of the circuit. In traditional RF design this can be achieved by neutralizing the input-output capacitive path as shown in Figure 2.13 (a) where L_1 and C_μ resonate at the desired frequency. However, in IC design the feedback is suppressed through the use of cascode topology as shown in Figure 2.13 (b) at the cost of slight increase in noise figure, since the parasitic capacitances of the floating inductor L_1 and coupling capacitor C_1 load the input and output nodes of the circuit [3].

Since scattering parameters of the circuit must be calculated or measured for a wide range to ensure K remains greater than "1" at all frequencies, using K for characterizing stability sometimes becomes difficult.

On the other hand, since LNA is an amplifier, it may also become unstable due to ac ground and supply loops resulting from the bond wire inductance. For the frequencies above 1GHz, a few nanohenries of inductance may cause considerable coupling between two stages through the ground node that result in oscillation [3].

3. INDUCTIVELY-DEGENERATED SIGE HBT LNA DESIGN AT 5.8 GHZ

As discussed in Chapter 2, the inductively-degenerated LNA architecture satisfies simultaneous noise and input matching. In addition, inductively-degenerated LNA consumes less power when compared to other architectures. Therefore, in this section to realize 5.8GHz LNA the relations given in the preceding section will be used.

3.1 Inductively-Degenerated SiGe HBT LNA with RLC Tank

As the first step, the inductively-degenerated cascode LNA is designed by using the design procedure given in Chapter 2, while RLC tank is used as load shown in Figure 3.1. The design parameters of inductively-degenerated SiGe HBT LNA are the emitter length of the input transistor, biasing current and emitter degeneration inductance L_e. The smallest emitter width of the technology is always used to reduce parasitic base resistance and so the noise figure. By appropriately choosing these parameters, the requirements of low power consumption, low noise figure, and simultaneous noise and input matching at the input should be satisfied.

In order to design low noise matched input transistor, the first step is finding the optimal noise current density. It is determined based on the fact that the bipolar transistor shows an optimum noise current density about ten times smaller than their peak f_T current density. Since the emitter length does not affect the minimum noise figure and the optimum noise current density, emitter length of the input transistor is adjusted to equalize the R_{opt} to the real part of Z_s (50 Ω) at the determined noise current density and desired frequency of 5.8 GHz. Under these conditions transistor Q1 is chosen with emitter geometry of 0.21x 6.72x2μm^2 (two of 0.21x 6.72 shunted together) and biased at 3.2 mA.

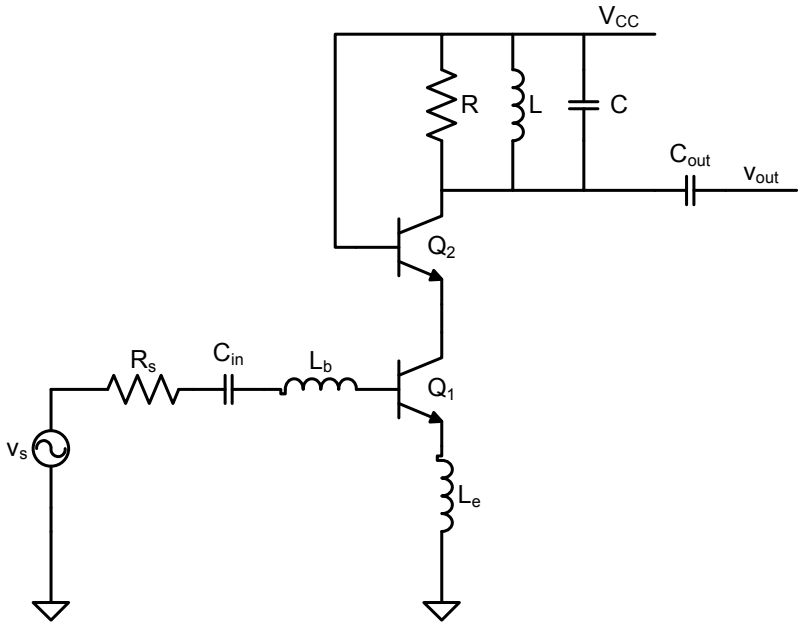


Figure 3.1 : Schematic of inductively-degenerated SiGe HBT LNA with RLC tank.

The emitter inductor L_e, is added to match the real part of the input impedance to Z_s (50 Ω) and its value can be calculated from equation (3.1). Since the transition frequencies of the transistors are about 120 GHz at the determined bias current in the used process which is IHP 0.25 µm BiCMOS process, the emitter inductor L_e values obtained are very small such as L_e = 70 pH in our design.

$$L_e \cong \frac{Z_s}{\omega_T} \tag{3.1}$$

When the inductance is lossless, it does not affect the value of the optimum source resistance R_{opt} whereas it shifts the optimum source reactance by $-\omega L_e$ as seen from equation (2.36). Finally, in order to cancel the reactance caused by the input capacitance and transform the optimum noise reactance X_{opt} to 0, the base inductor L_b is added to the input matching network. The value of the base inductor is obtained as L_b = 2.8nH based on equation (3.2).

$$L_b = \frac{1}{\omega^2 C_{in}} - L_e \tag{3.2}$$

Under matching conditions, noise figure of the LNA shown in Figure 3.1 is given in equation (3.3), where capacitors and inductors are assumed lossless.

$$F \cong 1 + \frac{r_b + r_e}{R_s} + \frac{1}{2\beta}.g_m.R_s + \frac{1}{2\beta.g_m.R_s}.\left(\frac{\omega_T}{\omega}\right)^2 + \frac{1}{2}.g_m.R_s\left(\frac{\omega}{\omega_T}\right)^2 + \frac{4.R_s}{R}.\left(\frac{\omega}{\omega_T}\right)^2 \quad \textbf{(3.3)}$$

The cascode stage has relatively small impact on the overall noise figure, therefore the size and biasing of the cascode stage (common-base stage) is optimized as base voltage V_B = 2.5 V and emitter geometry of 0.21x6.72x2 μm^2 (two of 0.21x6.72 shunted together) by considering the linearity and gain of the LNA.

The values of DC blocking capacitors C_{in} and C_{out} shown in Figure 3.1 are determined as C_{in} = C_{out} =5 pF which have negligible resistance at operating frequency f = 5.8 GHz, hence they have no effect on input and output matching conditions.

There is an RLC tank at the output of the LNA as seen from Figure 3.1. The values of the tank parameters are determined as R = 50 Ω, L = 1.8 nH and C = 280 fF to achieve 50 Ω at the output at desired frequency f = 5.8 GHz.

The designed LNA shown in Figure 3.1 is simulated with IHP 0.25 µm SiGe BiCMOS process parameters using Cadence Spectre-RF simulator. With a total power consumption of 8 mW from a 2.5 V supply (3.2 mA biasing current), a voltage gain (S_{21}) of 14.82 dB is achieved at the frequency of 5.8 GHz, while maintaining good matching at the input (S_{11}) and at the output (S_{22}) of -32.38 dB and -35.46 dB respectively. The reverse isolation (S_{12}) of the LNA is -67.6 dB. The noise figure of the designed LNA is 2.291 dB when the minimum noise figure is 1.721 dB at 5.8 GHz.

At 5.8 GHz, the 1dB-compression point for the output power is –13.67 dBm. Input referred third-order intercept point (IIP_3) simulations were performed by inserting two frequencies at 5.8 and 5.9 GHz and the IIP_3 was obtained as –11.14 dBm. These are the simulation results that exhibit the linearity performance of the designed LNA.

Additionally, the output voltage swing of the designed LNA is 13 mV where total harmonic distortion of the output signal is 1%.

3.2 Inductively-Degenerated SiGe HBT LNA with C_{ex} and RLC Tank

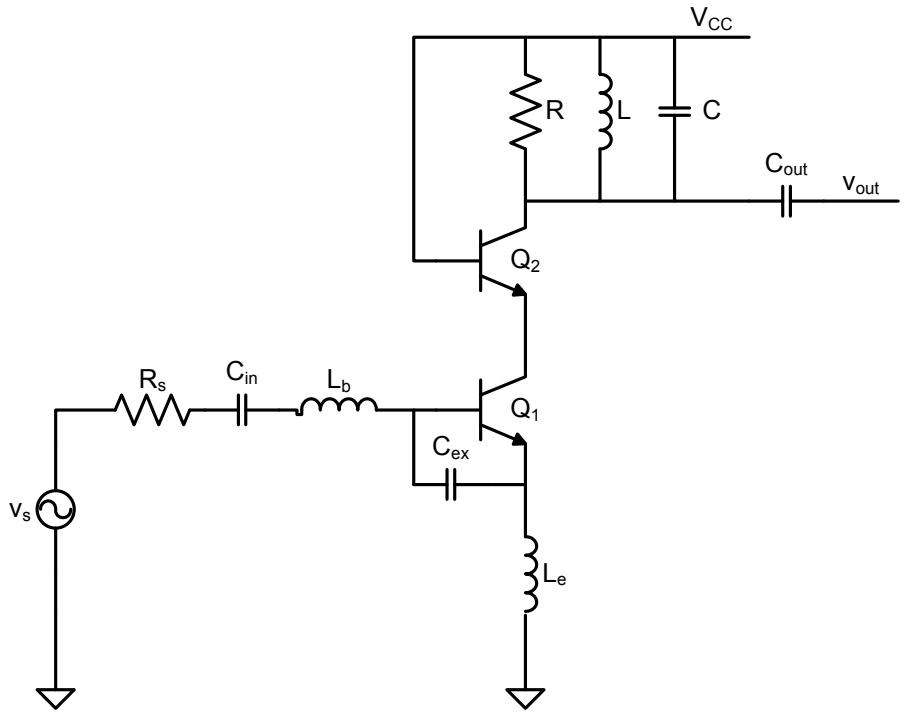


Figure 3.2 : Schematic of inductively-degenerated SiGe HBT LNA with C_{ex} and RLC tank.

In order to obtain further improve in noise figure of the LNA, noise contributions due to parasitic base and emitter resistances (r_b and r_x) and base current (I_B) must be reduced. As seen in Figure 3.2, placing an external capacitor (C_{ex}) between base and emitter terminals of the input transistor provides efficient filtering on the input mesh noise components (r_b, r_e and I_B) [16].

In this matching network, values of emitter and base inductances can be calculated from the equations below:

$$K = \frac{C_{in}}{C_{in} + C_{ex}} \tag{3.4}$$

$$L_e \cong \frac{Z_s}{K.\omega_T} \tag{3.5}$$

$$L_b \cong \frac{K}{C_{in}.\omega_o^2} - L_e \tag{3.6}$$

Noise figure equation of the LNA shown in Figure 3.2, under matching conditions when loaded with RLC tank and capacitors and inductances are assumed lossless again can be written as follows:

$$\begin{aligned} F \approx 1 + \frac{r_b + r_e}{R_s}.\left\{ K^2 + \left[g_m.R_s.\left(\frac{1}{K} - 1 \right).\left(\frac{\omega}{\omega_T} \right) \right]^2 \right\} \\ + \frac{g_m.R_s}{2}.\left[\frac{1}{\beta} + \left(\frac{\omega_o}{K.\omega_T} \right)^2 \right] + \frac{1}{2.\beta.g_m.R_s}.\left(\frac{K.\omega_T}{\omega} \right)^2 \\ + \frac{4R_s}{R}.\left(\frac{\omega}{K.\omega_T} \right)^2 \end{aligned} \tag{3.7}$$

As seen from the equation (3.7), the matching network with external base-emitter capacitance, filters out the white noise components caused by the collector current I_C and output resistance R, as matching network composed of only L_e and L_b does. Besides, it reduces the noise contributions coming from the input mesh (r_b, r_e and I_B). Moreover, the frequency dependent contributions due to I_C and R are increased; but since modern RF processes has high transition frequencies, frequency dependent terms coming from the output mesh are usually very small [17].

Since equation (3.7) includes terms proportional to the parameter K and inversely proportional to the K, an optimum value for K can be found to minimize the noise figure. Parameter K causes degradation in the frequency capability of the input transistor so tradeoff between the noise figure and the frequency capability. This tradeoff may be eliminated in a process which has higher transition frequency than the operating frequency.

The optimum noise resistance and minimum noise figure is not directly affected from the external base- emitter capacitance C_{ex}, therefore the determined size and biasing of the input transistor for the previous design are not changed. On the other hand the values of RLC tank components also are not changed, since output matching is not affected by the input matching conditions. However, values of base and emitter inductances change with the value of C_{ex} or parameter K. Since the value of the parameter K is lower than unity value of emitter inductor which satisfies the matching conditions is higher with respect to previous design as seen in equation (3.5). Finally, the sum of the L_b and L_e is reduced due to the parameter K less than one according to the equation (3.6).

By considering the conditions above, the values of input matching components are determined as $L_e = 0.25$ nH, $L_b = 1.7$ nH and $C_{ex} = 230$ fF.

The designed LNA shown in Figure 3.2 has voltage gain (S_{21}) of 8.712 dB at the frequency of 5.8 GHz while consuming 8 mW power from a 2.5 V supply (3.2 mA bias current). At 5.8GHz, the designed LNA has 2.057 dB noise figure when the minimum noise figure is 2.029 dB with input return loss (S_{11}) of -31.76 dB and output return loss (S_{22}) of -37.99 dB which denotes good input and output matching. The reverse isolation (S_{12}) of the LNA is -71.58 dB.

The 1dB-compression point for the output power is –12.018 dBm at 5.8 GHz and input referred third-order intercept point (IIP_3) is obtained as –8.845 dBm by inserting two frequencies at 5.8 and 5.9 GHz. From the transient response of the LNA, the output voltage swing is obtained as 11 mV where total harmonic distortion of the output signal is 1%.

When these two designs are compared, it can be seen that noise figure is improved about 0.3 dB with the additional capacitor C_{ex}. The value of L_e is increased and becomes realizable with on-chip spiral inductors. Moreover L_b is decreased as estimated based on equation (3.6) which is important for noise figure since the inductors are not lossless as assumed while deriving noise figure expressions. However, voltage gain of the LNA is reduced approximately 6 dB due to the reduction of the frequency capability of the input transistor. Finally, there is little

increase in minimum noise figure as a result of decrease in transition frequency of the input transistor caused by the external base-emitter capacitor.

3.3 Inductively-Degenerated SiGe HBT LNA with C_{ex} and L-tapped Output Matching

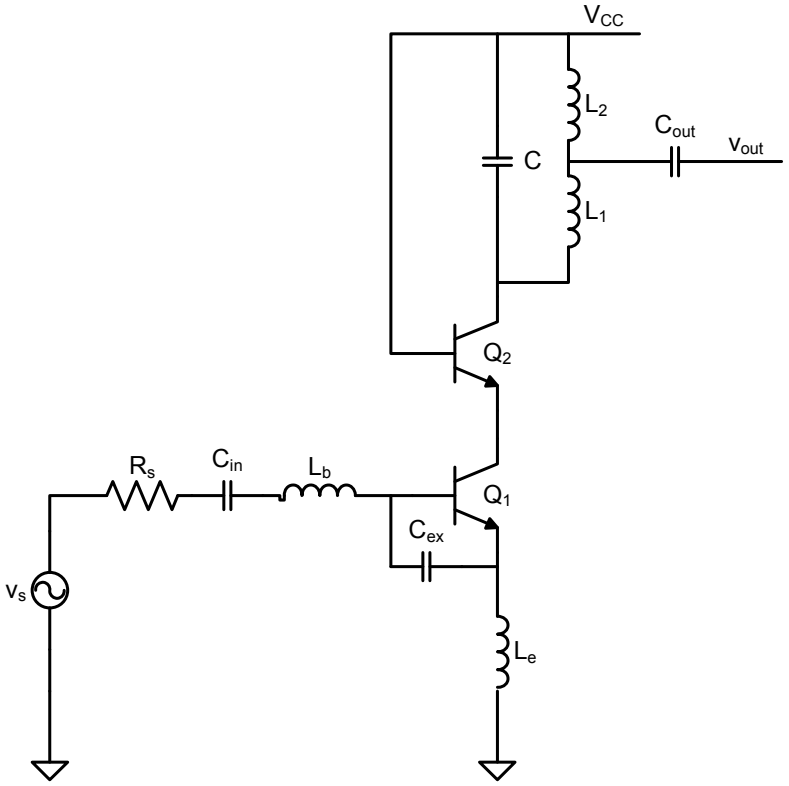


Figure 3.3 : Schematic of inductively-degenerated SiGe HBT LNA with C_{ex} and L-tapped output matching.

In order to maximize the power transferred to the load and the linear output power swing, a tapped-inductor output matching network is proposed instead of RLC tank as shown in Figure 3.3. The values of output matching components are determined as C = 135 fF, L_1 = 2.8 nH and L_2 = 0.94 nH so as to obtain a 50 Ω output match by using equations (3.8) - (3.11) in [12].

$$Q = \omega_o R_{in} C \qquad \textbf{(3.8)}$$

$$Q_2 = \sqrt{\frac{R_2}{R_{in}}\left(Q^2+1\right)-1} \tag{3.9}$$

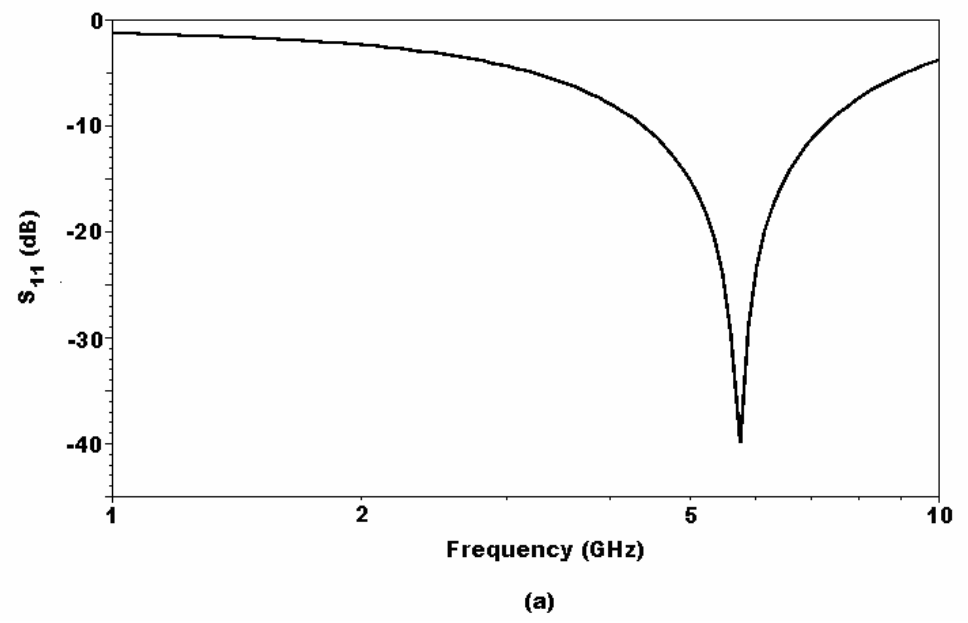
$$L_2 = \frac{R_2}{\omega_o Q_2} \tag{3.10}$$

$$L_1 = L_2 \frac{\left[QQ_2 - Q_2^2\right]}{Q_2^2+1} \tag{3.11}$$

where R_{in} is the resistance seen from the collector terminal of the output transistor, R_2 is 50 Ω, Q and Q_2 denote the quality factor of the output matching network and the R_2–L_2 network, respectively.

Since the output matching network does not have considerable impact on the input matching conditions, neither the values of passive components of the input matching network nor size and biasing of the transistors are changed.

Simulated scattering parameters of the proposed LNA are shown in Figure 3.4 - Figure 3.7. Total power consumption of the proposed LNA is 8 mW from a 2.5 V supply (3.2 mA bias current) as previously designed LNAs.



(a)

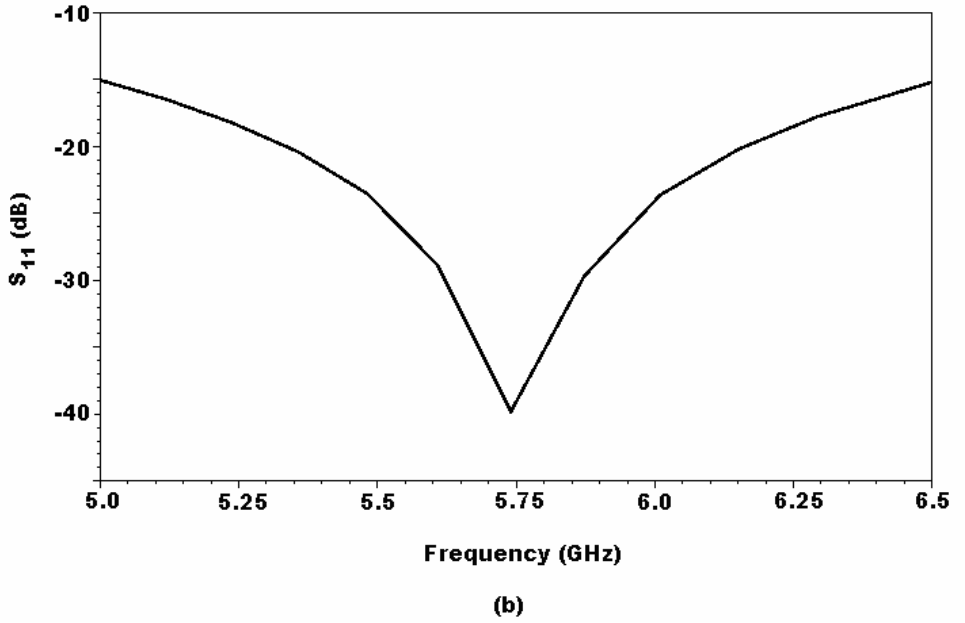
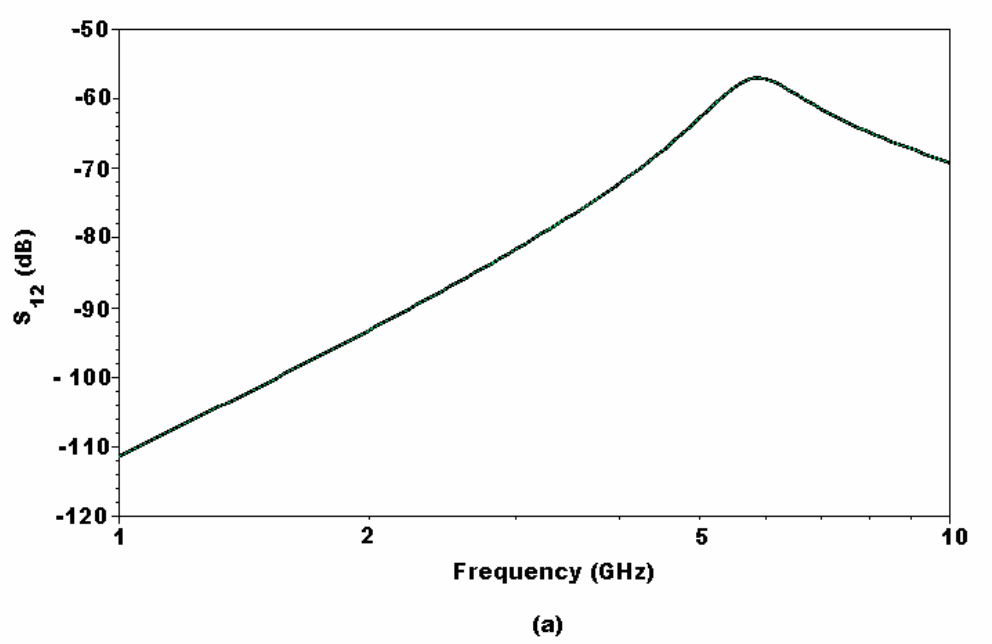


Figure 3.4 : (a) Input return loss of the proposed SiGe HBT LNA (S_{11}) between 1 GHz - 10GHz. (b) The same graphic (S_{11}) between 5 GHz - 6.5 GHz.



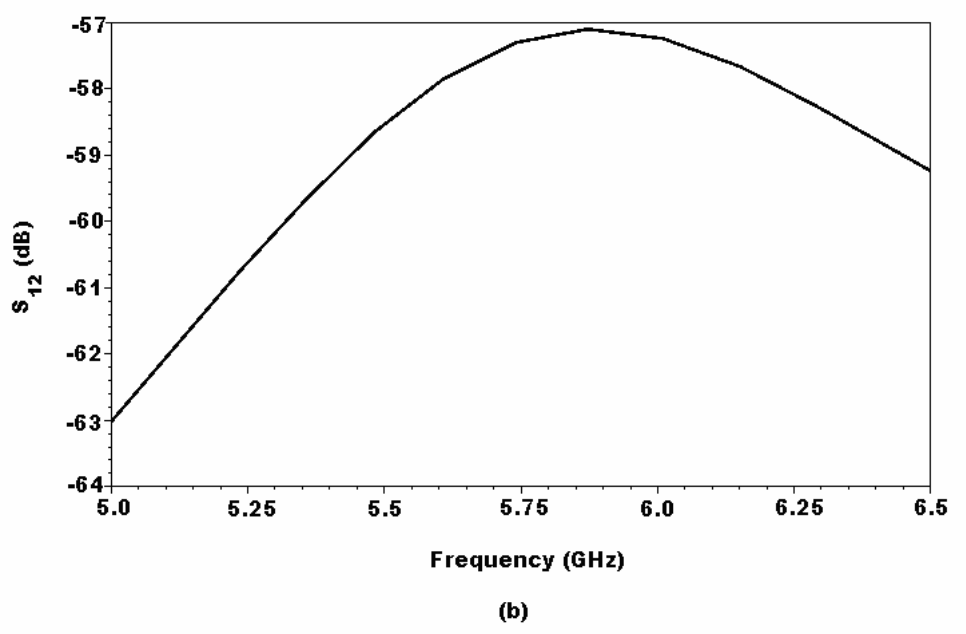
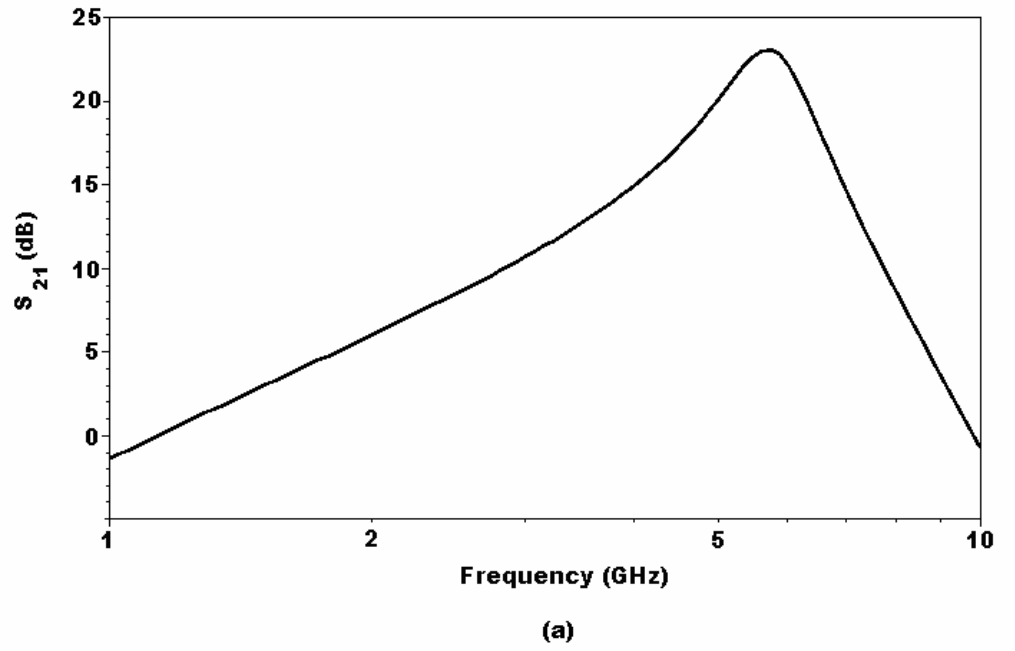


Figure 3.5 : (a) Reverse isolation between input and output terminals of the proposed SiGe HBT LNA (S_{12}) between 1 GHz - 10GHz. (b) The same graphic (S_{12}) between 5 GHz - 6.5 GHz.

Voltage gain (S_{21}) of 22.98 dB is achieved at the frequency of 5.8 GHz, while maintaining good matching at the input (S_{11}) and at the output (S_{22}) of -35.48 dB and -12.05 dB respectively. The reverse isolation (S_{12}) of the LNA is less than -57 dB.



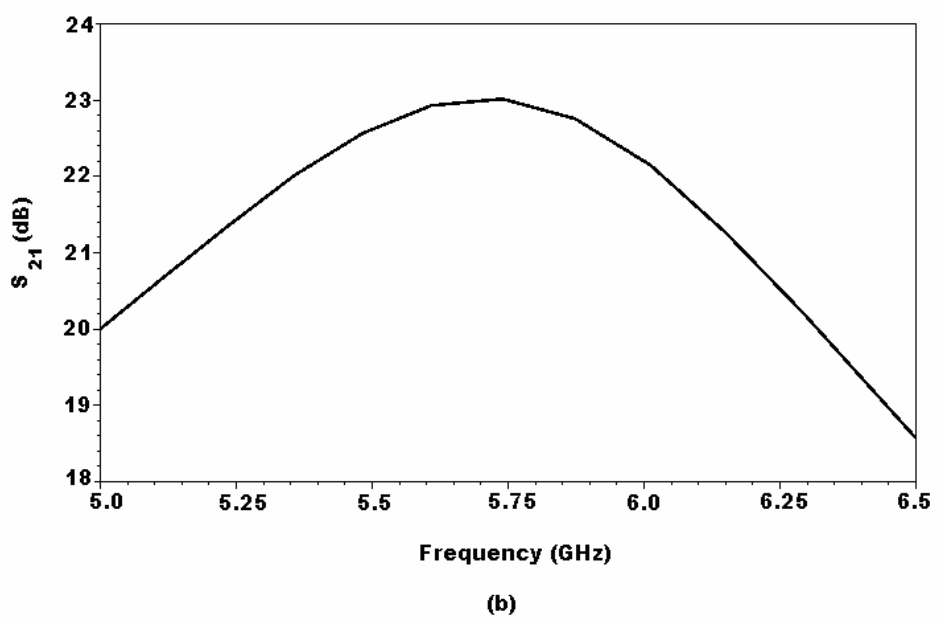
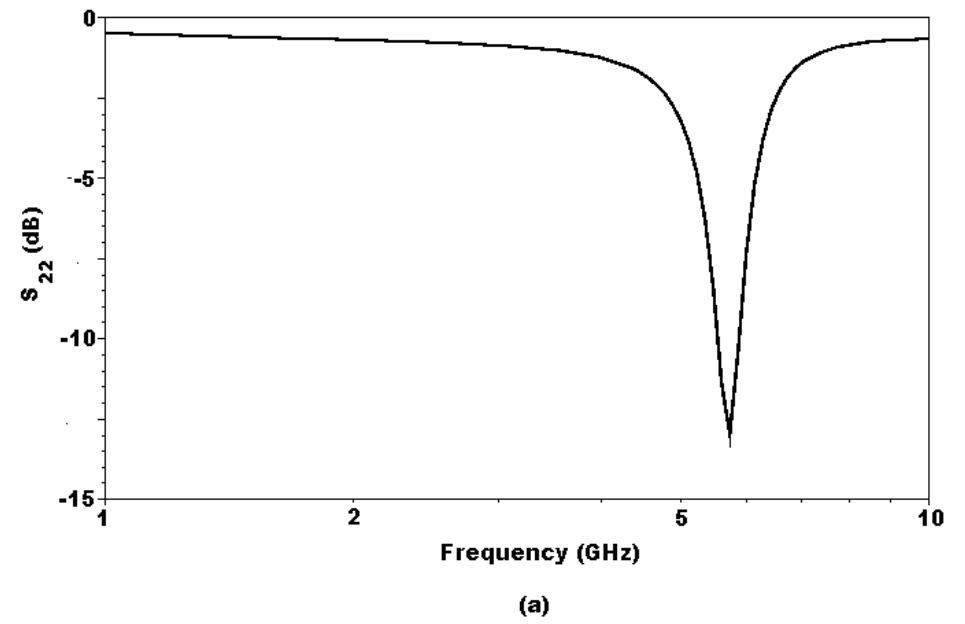


Figure 3.6 : (a) Voltage gain of the proposed SiGe HBT LNA (S_{21}) between 1 GHz - 10GHz. (b) The same graphic (S_{21}) between 5 GHz - 6.5 GHz.



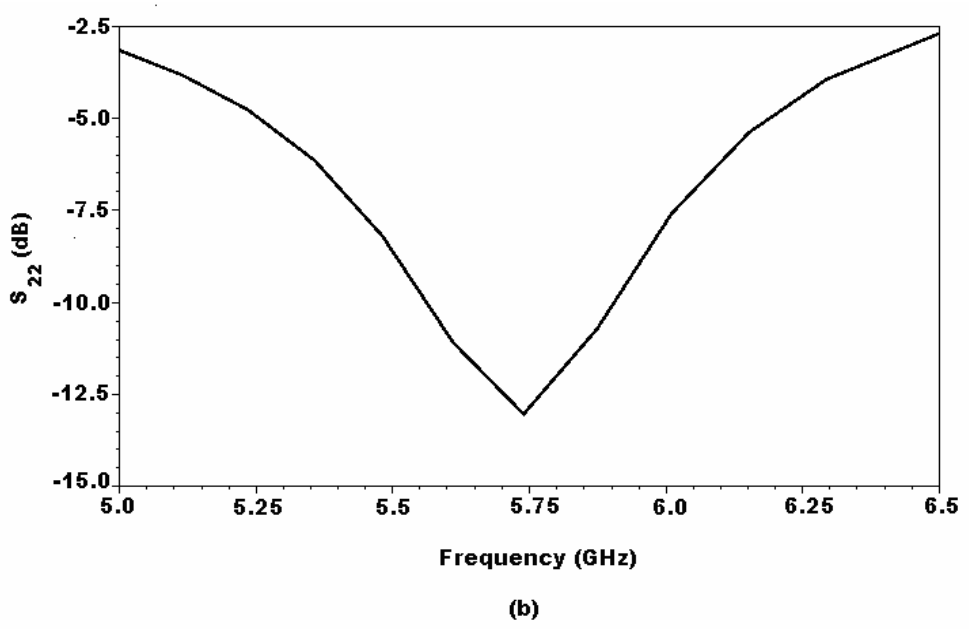


Figure 3.7 : (a) Output return loss of the proposed SiGe HBT LNA (S_{22}) between 1 GHz - 10GHz. (b) The same graphic (S_{22}) between 5 GHz - 6.5 GHz.

The proposed LNA has noise figure (NF) of 1.678 dB where minimum noise figure is 1.644 dB as shown in Figure 3.8. The difference between 50 Ω and minimum noise figure is only 0.03 dB at 5.8 GHz indicating close to optimum noise match due to the appropriately chosen transistor size and biasing.

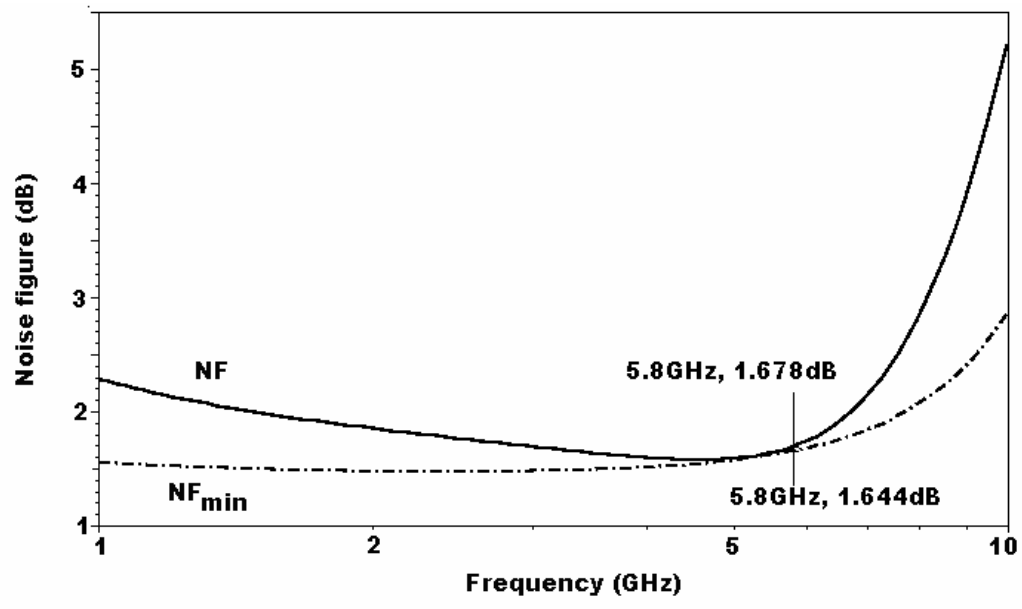


Figure 3.8 : Noise figure of the proposed SiGe HBT LNA.

Simulation results that exhibit the linearity performance of the proposed LNA are shown in Figure 3.9 - Figure 3.10. Simulated 1 dB compression point at 5.8 GHz is -8.798 dBm. Input referred third order intercept point (IIP3) simulations are performed by inserting two frequencies at 5.8 and 5.9 GHz and IIP_3 is obtained as -13.332 dBm. In Figure 3.11, transient response of the LNA is shown. The proposed LNA has output voltage swing of 290 mV where total harmonic distortion of the output signal is only 1%.

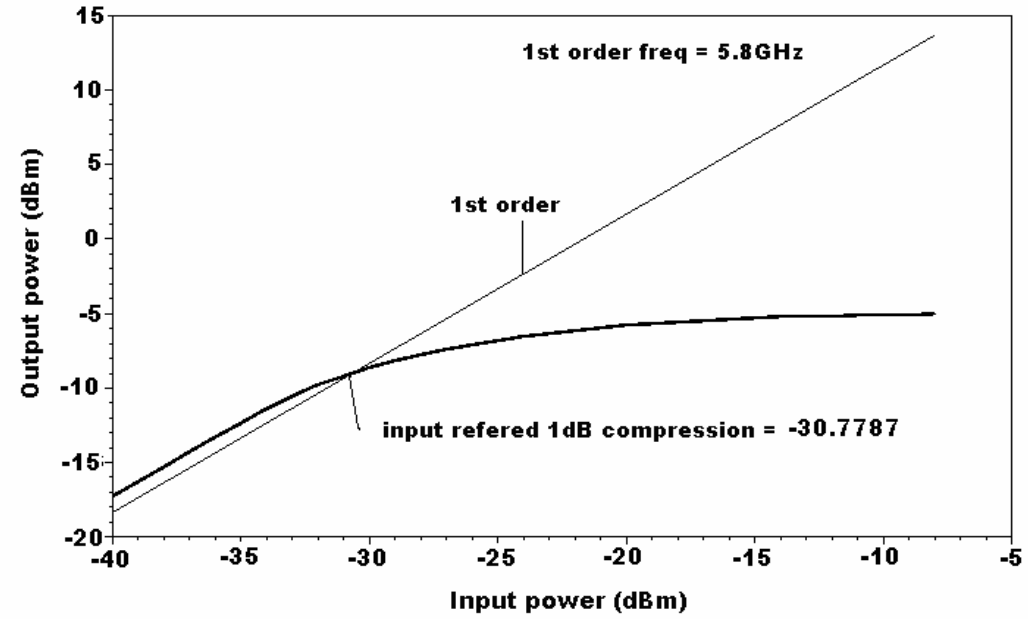


Figure 3.9 : 1-dB compression point of the proposed SiGe HBT LNA (P_{1dB}).

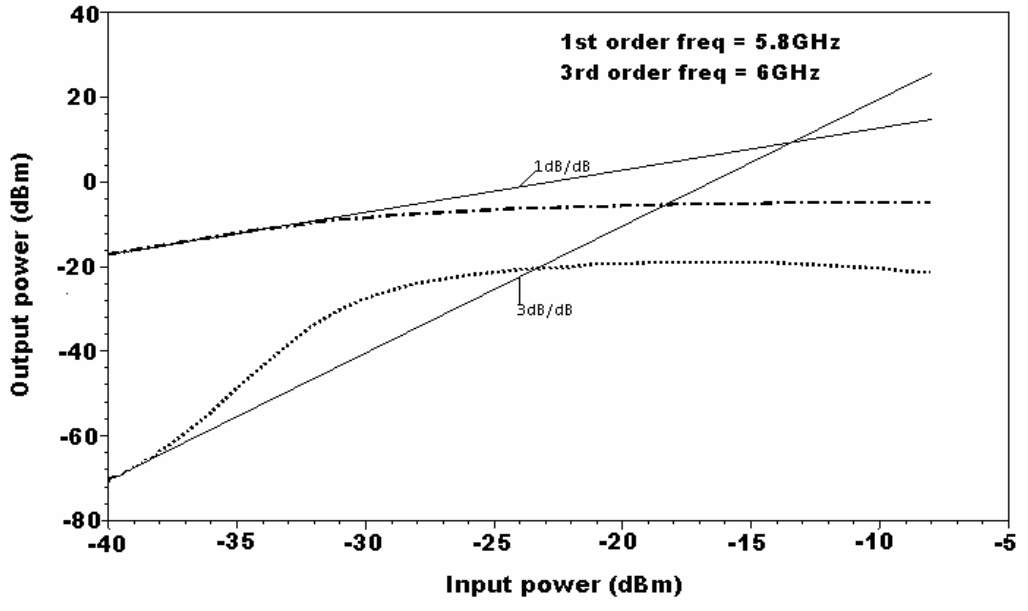


Figure 3.10 : Third-order intercept point of the proposed SiGe HBT LNA (IIP_3).

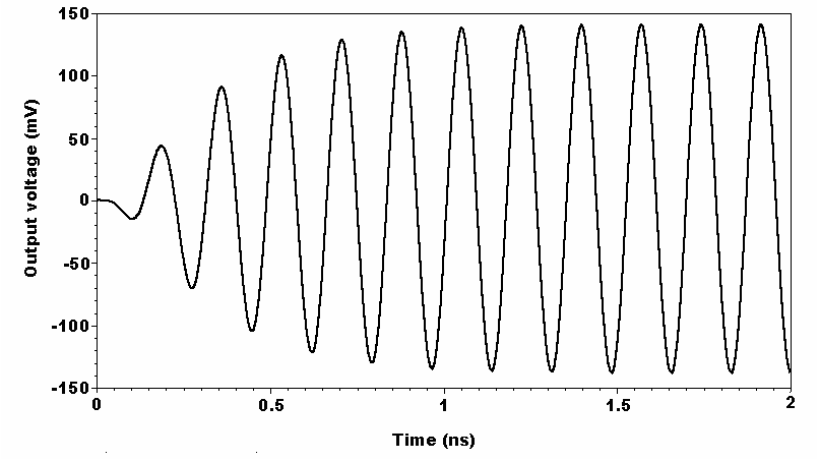


Figure 3.11 : Output signal of the proposed SiGe HBT with 1% THD.

Voltage gains and noise figures of these three LNA designs are shown in Figure 3.12 and 3.13, respectively. Voltage gain of the inductively-degenerated LNA with external capacitor C_{ex} is lower than that of which without C_{ex}, since C_{ex} cause degradation in frequency capability of input transistor. However, noise figure is improved with the addition of C_{ex} due to the efficient filtering on input noise contributions. On the other hand, these figures demonstrates that, L-tapped output matching not only maximize the linear output power but also reduce the noise figure, since output matching network does not includes any real resistor. Finally, bandwidth of the gain is narrower with respect to RLC tank load.

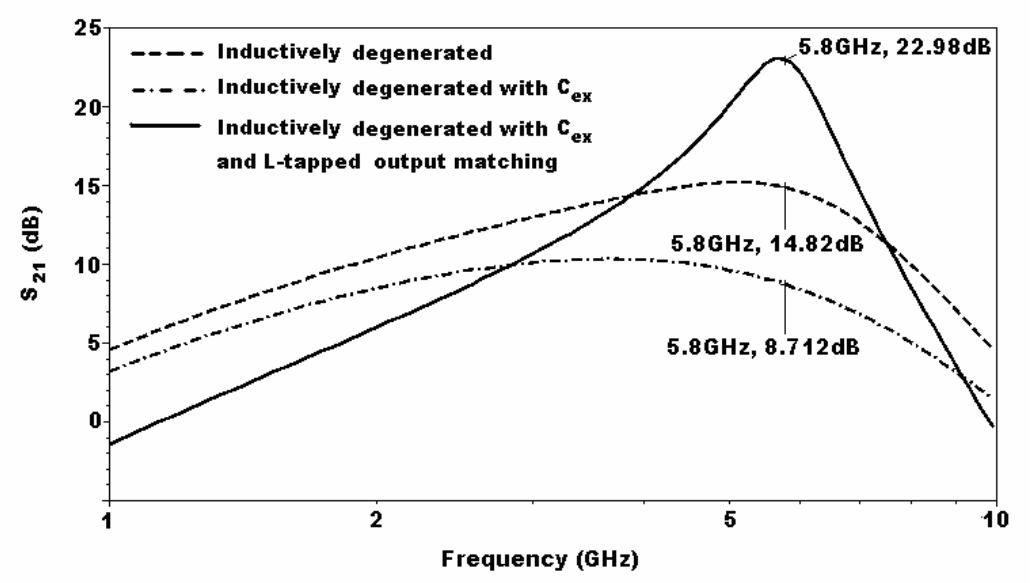


Figure 3.12 : Comparison of voltage gains of designed SiGe HBT LNAs.

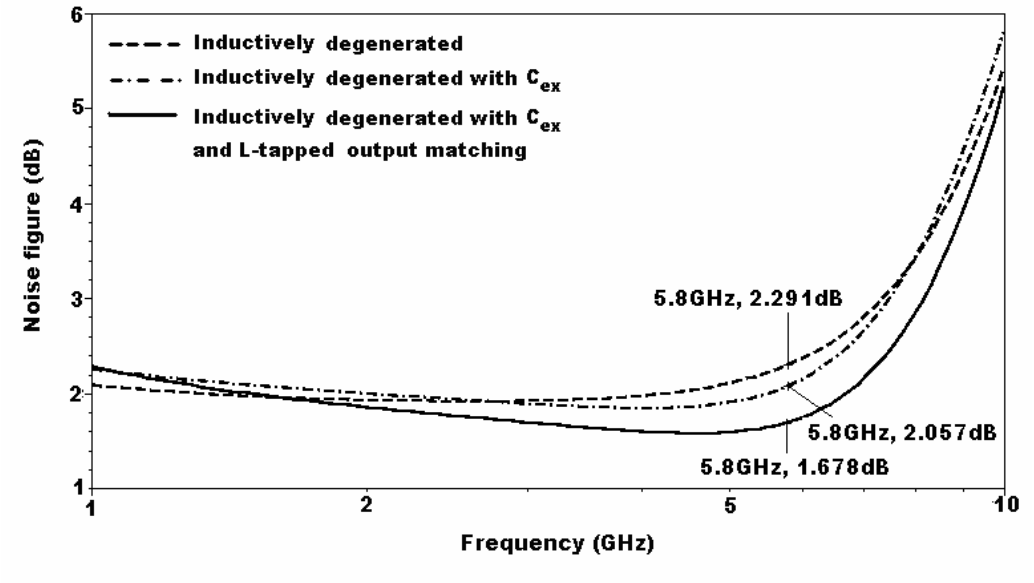


Figure 3.13 : Comparison of noise figures of designed SiGe HBT LNAs.

Performance summaries of the three different SiGe HBT LNA configurations designed in this section are given in Table 3.1. These LNAs have the same power consumption through the same supply voltage and same current. Additionally, the transistor sizes are same in each design; however, the input and output matching circuits are different.

Table 3.1 : Performance summaries of designed SiGe HBT LNAs.

at 5.8 GHz	**Performance Parameters**					
	NF (dB)	**S_{21} (dB)**	**S_{11} (dB)**	**S_{22} (dB)**	**P_{1dB} (dBm)**	**IIP_3 (dBm)**
Inductively-deg. with RLC tank	2.291	14.74	-32.38	-35.46	-13.67	-11.14
Inductively-deg. with C_{ex} and RLC tank	2.057	8.712	-31.76	-37.99	-12.02	-8.845
Inductively-deg. with C_{ex} and L-tapped output matching	1.678	22.98	-35.48	-12.05	-8.798	-13.33

Performance comparison with other LNAs in literature, operating at 5.8 GHz, is shown in Table 3.2. The noise figure, gain and input matching performance of the proposed LNA is better than the other LNAs, which demonstrates simultaneous noise and input matching can be achieved with comparable power consumption.

Table 3.2 : Comparison of SiGe HBT LNA performances.

at 5.8 GHz	**Various LNA Configurations**			
	This Work	***[6]***	***[7]***	***[8]***
Technology	SiGe HBT	SiGe HBT	SiGe BJT	SiGe HBT
V_{CC} (V)	2.5	1	1	1.5
P_d (mW)	8	13	6.6	1.5
NF (dB)	1.678	2.1	4	3.07
S_{21} (dB)	22.98	13	11.5	16.07
S_{11} (dB)	-35.48	-6	-9	-18.01
S_{22} (dB)	-12.05	-4	-13.7	-15.23
P_{1dB} (dBm)	-8.798	-21	-19	-6.54
IIP_3 (dBm)	-13.33	-10.5	n. a.	n. a.

3.4 Design Procedure for SNIM SiGe HBT LNA

Design procedure for SNIM SiGe HBT LNA that is applied in this chapter can be summarized as follows:

First design step is determining the size and biasing of the input transistor so that input transistor becomes noise matched. Since bipolar transistors show an optimum noise current density ten times smaller than their peak f_T current density, the optimal noise current density must be determined. The minimum noise figure and optimum noise current density is practically independent of the emitter length of the input transistor; therefore, emitter length of the device is chosen so as to make R_{opt} equal to the real part of the source impedance Z_s.

Second step is determining the value of emitter degeneration inductor L_e by using equation (3.1) which is required to match the real part of the input impedance to the real part of the source impedance Z_s. Values of the noise parameters R_{opt}, F_{min} and R_n are not changed by the emitter inductor while the value of the optimum noise reactance X_{opt} is reduced by ωL_e.

Last step for input and noise matching is adding base inductance L_b which cancels out the reactance due to the input capacitance of the device C_{in} and transforms the optimum noise reactance of the amplifier to 0 Ω. Value of L_b can be determined by using equation (3.2). After these steps simultaneous input and noise matching is achieved.

In order to further improve the noise figure of the LNA, an external capacitor (C_{ex}) can be placed between base and emitter terminals of the input transistor which provides efficient filtering on the input mesh noise components (r_b, r_e and I_B). In this case design parameters L_e and L_b can be calculated from the equations (3.4)-(3.6). Since the value of the parameter K is lower than unity, the emitter inductor value which satisfies the matching conditions is higher with respect to that of without C_{ex}. Besides, the sum of the L_b and L_e is reduced due to the parameter K less than one according to equation (3.6). On the other hand parameter K causes degradation in the frequency capability of the input transistor so a tradeoff between the noise figure and the frequency capability exists.

After values of the input elements are determined, appropriate matching network is designed for output of the LNA that maximizes the power transferred to the load and linear output power swing.

4. INDUCTIVELY-DEGENERATED CMOS LNA DESIGN AT 5.8 GHZ

The gate-source voltage (or overdrive voltage) of the input transistor V_{gs}, the width of the input transistor W, and the source degeneration inductance L_s are the design parameters of the inductively-degenerated CMOS LNA. Therefore, the requirements of low power consumption, low noise figure, and simultaneous noise and input matching at the input port should be satisfied by choosing these parameters appropriately.

4.1 Inductively-Degenerated CMOS LNA with RLC Tank

As the first step, the inductively-degenerated cascode CMOS LNA is designed by using the design procedure given in Chapter 2, while RLC tank is used as load shown in Figure 4.1. However, in order to make a comparison between the SiGe HBT LNA and the CMOS LNA, power consumptions are chosen as equal, therefore the bias current (or drain current of the input transistor) is fixed to I_D = 6.67 mA since the supply voltage of the used CMOS process is V_{DD} = 1.2 V.

To achieve $\mathrm{Re}\{Z_{opt}^{i}\} = \mathrm{Re}\{Z_{s}^{i}\}$ as indicated in equation (2.55) for noise minimization under a given power consumption constraint (or fixed biasing current), optimum size and V_{gs} voltage of the input transistor must be found. While determining V_{gs} and W of the input transistor, contributions of drain and induced gate noise given in equation (2.59) should be considered. Since source inductor L_s not only produces real part to the input impedance but also shifts the optimum noise reactance by $-\omega L_s$; matching of the real part of the input impedance to Z_s (50 Ω) and canceling of the imaginary part of the optimum noise impedance X_{opt} is provided by the source inductor. The value of the source inductor can be determined by using the following equation.

$$L_s \approx \frac{\alpha\sqrt{\frac{\delta}{5\gamma\left(1-|c|^2\right)}}}{\omega\omega_T C_{gs}} \qquad \textbf{(4.1)}$$

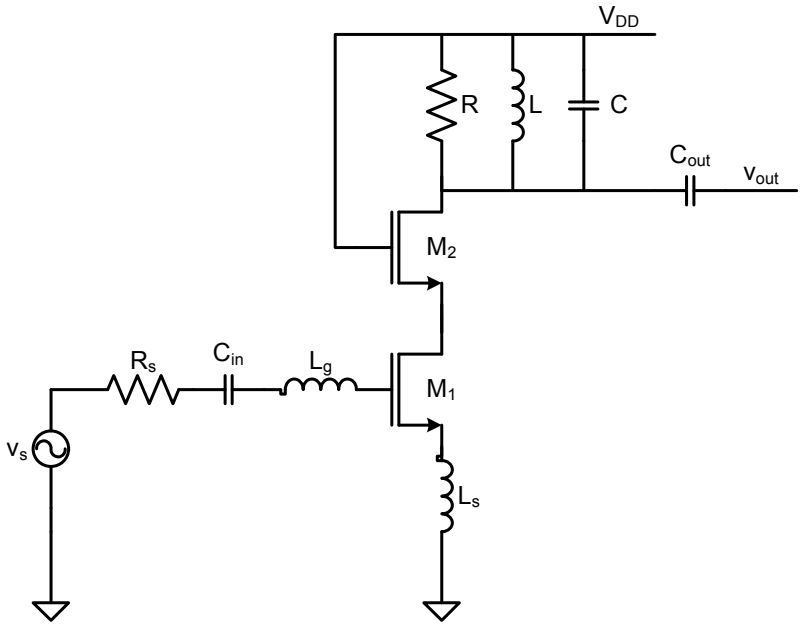


Figure 4.1 : Schematic of the inductively-degenerated CMOS LNA.

By choosing the gate width of the input transistor M1 as W_1 = 224 µm (two of 112 µm with 16 finger shunted together) and gate length 0.12 µm with V_{gs} = 0.46 mV and L_s = 0.24 nH under 6.67 mA biasing current, conditions given in equations (2.55) - (2.57) are satisfied. Under these conditions transition frequency of the input transistor is about 60 GHz. Finally, the last condition given in equation (2.58) to achieve noise and input matching simultaneously is satisfied by adding gate inductor L_g to the input matching network as seen in Figure 4.1. The value of the gate inductor is determined as L_g = 2.6 nH through the equation (4.2).

$$L_g \cong \frac{1}{\omega^2 C_{gs}} - L_s \qquad \textbf{(4.2)}$$

The cascode stage has relatively small impact on the overall noise figure. The bias of the cascode stage is tightly related to its size; therefore the width of the cascode

transistor can be increased until the bias of the cascode stage approaches to the threshold voltage and can be decreased until the input transistor reaches to triode region. Noise contribution of the cascode stage increases as the width of the cascode transistor (W_2) increases. However, the required L_s value for real part input matching is reduced due to the Miller effect since capacitance between the M1 and M2 increases as W_2 becomes larger. On the other hand, bias and width of the cascode stage influences the linearity and gain of the LNA. By taking these effects into consideration width and biasing of the cascode stage (common-base stage) is optimized as gate voltage V_B = 1.2 V and W_2 = 224 µm (two of 112 µm with 16 finger shunted together).

C_{in} and C_{out} are DC blocking capacitors as shown in Figure 4.1 and their values are determined as C_{in} = C_{out} = 5 pF so that they have no effect on input and output matching conditions since they have negligible resistance at operating frequency f = 5.8 GHz.

There is an RLC tank at the output of the LNA as seen from Figure 4.1. The values of tank parameters are determined as R = 50 Ω, L = 1 nH and C = 400 fF to achieve 50 Ω at the output at desired frequency f = 5.8 GHz.

The designed LNA shown in Figure 4.1 is simulated with UMC 0.13 µm CMOS process parameters using Cadence Spectre-RF simulator. With a total power consumption of 8 mW from a 1.2 V supply (6.67 mA biasing current), a voltage gain (S_{21}) of 8.21 dB is achieved at the frequency of 5.8 GHz, while maintaining good matching at the input (S_{11}) and at the output (S_{22}) of -37.41 dB and -20.52 dB respectively. The reverse isolation (S_{12}) of the LNA is -40.66 dB. The noise figure of the designed LNA is 1.677 dB when the minimum noise figure is 1.519 dB at 5.8 GHz.

At 5.8 GHz, the 1-dB compression point for the output power is 1.24 dBm. Input referred third-order intercept point (IIP_3) simulations were performed by inserting two frequencies at 5.8 and 5.9 GHz and the IIP_3 was obtained as –9.84 dBm. These are the simulation results that exhibit the linearity performance of the designed LNA. Additionally, the output voltage swing of the designed LNA is 40 mV where total harmonic distortion of the output signal is 1%.

In the above LNA design technique simultaneous noise and input matching is achieved by satisfying equations (2.55) – (2.57) with the addition of degeneration source inductor L_s. However, if there is a power constraint (low power) then the input transistor size must be low that leads to high value of optimum noise resistance due to smaller values of gate-source capacitance C_{gs} as seen from equation (2.33). For the given bias or ω_T (under the low consumption constraint), from equation (2.54) L_s has to be very large in order to provide real part input matching as seen from the equation (2.57). For values of L_s larger than some value, equation (2.53) becomes invalid since with large L_s the transconductance of the input stage degrades significantly thus; the feedback through C_{gd} can not be neglected. Therefore, minimum achievable noise figure increases considerably [27]. As a result, this technique is not applicable for transistor sizes and bias levels in other words for power dissipation levels that optimum noise resistance R_{opt} becomes greater than real part of the input impedance $\mathrm{Re}\{Z_{in}\}$. An optimum transistor size can be found which provides a minimum noise figure while satisfying input matching for small amount of power consumption where the above design technique is not applicable, yet the achievable minimum noise figure of the design will be higher than F_{min} of the common source stage [27].

4.2 Inductively-Degenerated CMOS LNA with C_{ex} and RLC Tank

The LNA in Figure 4.2 has one additional capacitor C_{ex} between gate and source terminals of the input transistor when compared to the LNA in Figure 4.1. This additional capacitor C_{ex} provides noise matching with smaller values of L_s as seen from the equation below:

$$L_s \approx \frac{\alpha \sqrt{\frac{\delta}{5\gamma\left(1-|c|^2\right)}}}{\omega\omega_T\left(C_{gs}+C_{ex}\right)} \qquad \textbf{(4.3)}$$

On the other hand the imaginary part of the input matching can be achieved with smaller values of L_g as seen from equation (4.4) in this architecture which is important since inductances are not lossless as assumed in noise analysis and

contribute noise to the system. However, the additional C_{ex} causes gain reduction due to the degradation of effective transition frequency of the input transistor.

$$L_g \cong \frac{1}{\omega^2 \left(C_{gs} + C_{ex} \right)} - L_s \tag{4.4}$$

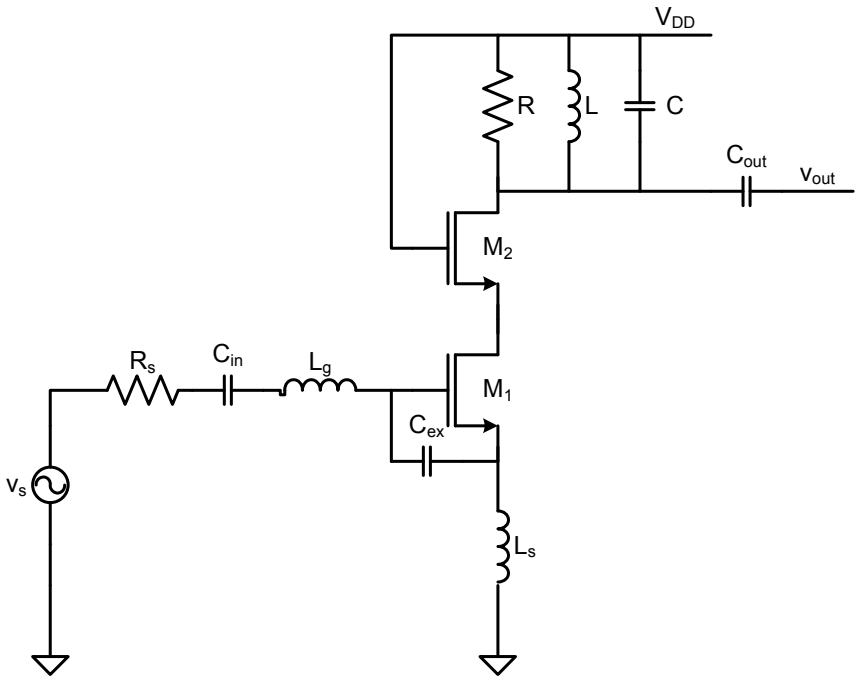


Figure 4.2 : Schematic of the inductively-degenerated CMOS LNA with C_{ex} and RLC tank.

Since the power consumption is fixed to 8 mW as mentioned before, biasing current is still 6.67 mA for this LNA design. Under these conditions gate width of the input transistor M1 is determined as W_1 = 224 µm (two of 112 µm with 16 fingers shunted together) with gate length 0.12 µm where gate source voltage V_{gs} = 0.46 mV. Source degeneration inductor is chosen as L_s = 0.13 nH and external capacitor C_{ex} = 104 fF in order to satisfy equation (2.55) - (2.56). Finally, to provide imaginary part of the impedance matching, the value of the gate inductor is determined as L_g = 1.9 nH from equation (4.4). The values of the RLC tank components are not changed since they are not affected by input matching conditions.

The designed LNA shown in Figure 4.2 has voltage gain (S_{21}) of 7.97 dB at the frequency of 5.8 GHz while consuming 8 mW power from a 1.2 V supply (6.67 mA bias current). At 5.8 GHz, the designed LNA has noise figure 1.607 dB when the minimum noise figure is 1.599 dB with input return loss (S_{11}) of -11.33 dB and output return loss (S_{22}) of -20.81 dB which denotes good input and output matching. The reverse isolation (S_{12}) of the LNA is -42.34 dB.

The 1-dB compression point for the output power is 1.442 dBm at 5.8 GHz and input referred third-order intercept point (IIP_3) is obtained as –9.66 dBm by inserting two frequencies at 5.8 and 5.9 GHz. From the transient response of the LNA, the output voltage swing is obtained as 32 mV where total harmonic distortion of the output signal is 1%.

If these two designs are compared, following remarks can be presented. The value of L_s is decreased to satisfy noise matching conditions where the bias and size of the input transistor is not changed. Under these conditions, small improvement in the noise performance of the LNA is observed that may be due to reduction in the value of the gate inductor which is not lossless as assumed. However, the real part of the input matching is not provided perfectly as seen from the value of the input return loss of the LNA (S_{11}). As a result, it can be said that additional C_{ex} removes noise match from the input match if there is no low power constraint as in this case. On the other hand, such small values of inductors (approximately smaller than 0.2 nH) can not be realized with on-chip spiral inductors. Additionally there is small decrease in the gain of the LNA caused by degradation in the effective transition frequency as expected. Therefore there is no need to the additional C_{ex} capacitance under this power consumption limit in this process.

4.3 Inductively-Degenerated CMOS LNA with L-tapped Output Matching

The last step is designing output matching network instead of RLC tank used in previous designs to maximize the power transferred to the load and the linear output power swing. Therefore a tapped-inductor output matching network is proposed shown in Figure 4.3 as in the case of SiGe HBT LNA. The values of output matching

components are determined as C = 135 fF, L_1 = 1.1 nH and L_2 = 0.9 nH so as to obtain a 50 Ω output matching by using equations (3.8) - (3.11).

In the proposed LNA shown in Figure 4.3, size and biasing of the transistors are not changed, while there are small changes in the values of passive components of the input matching network since input and output of the LNA are not isolated exactly. The values of passive components are determined as L_s = 0.28 nH and L_g = 2.35 nH.

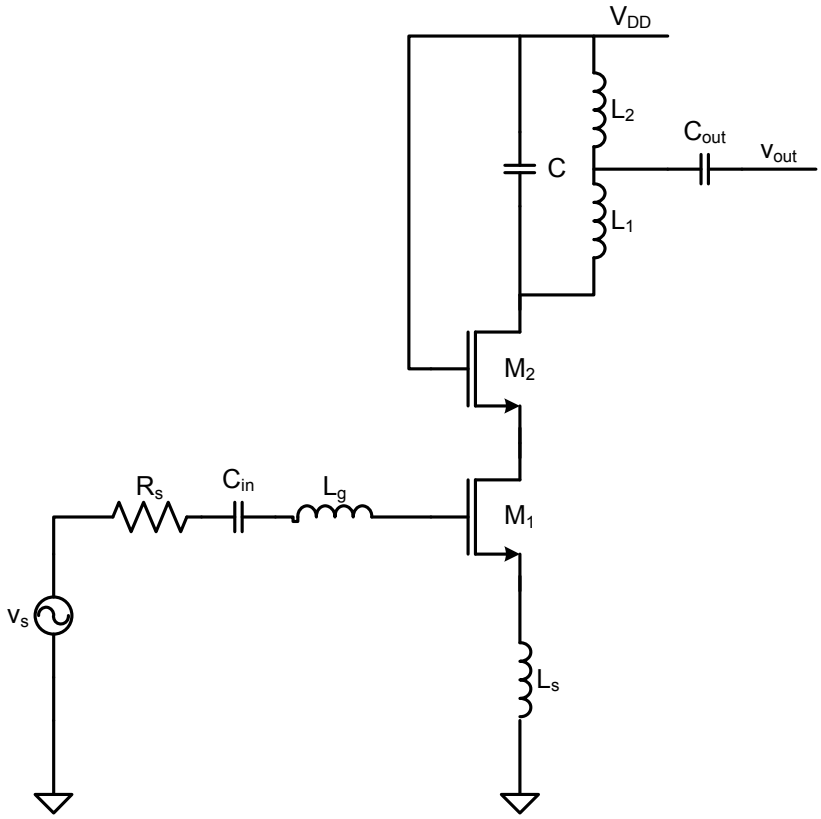
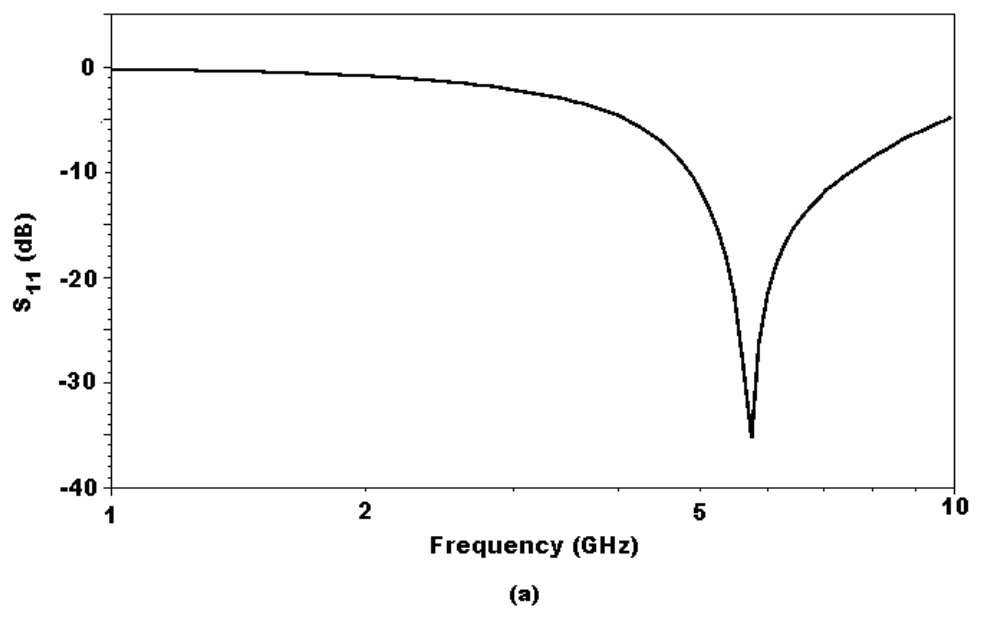


Figure 4.3 : Schematic of inductively-degenerated CMOS LNA with L-tapped output matching.

Simulated scattering parameters of the proposed LNA are shown in Figure 4.4 - Figure 4.7. Total power consumption of the proposed LNA is 8 mW from a 1.2 V supply (6.67 mA bias current) as the previously designed LNAs.



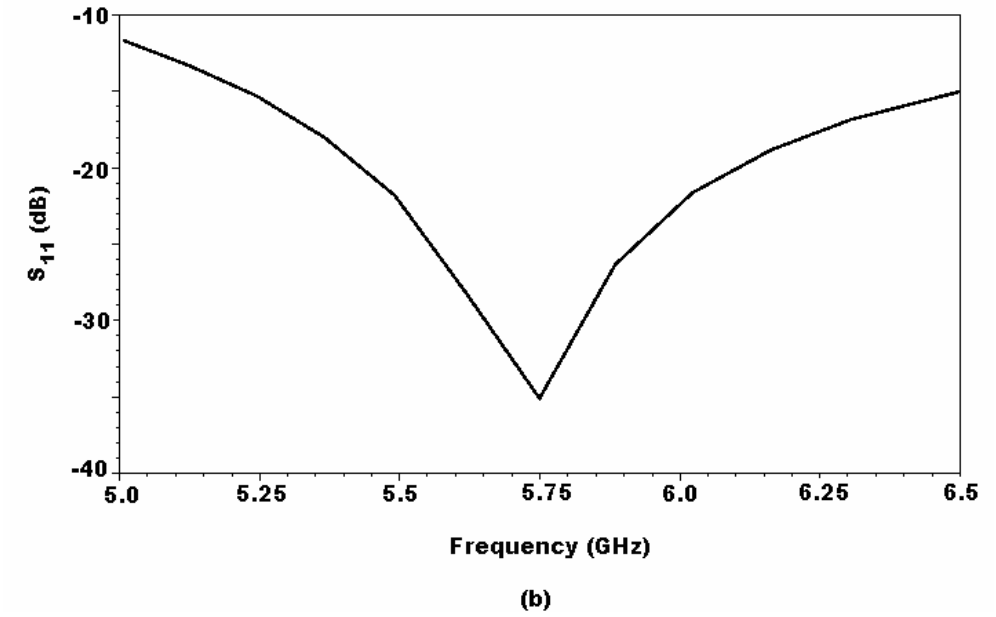
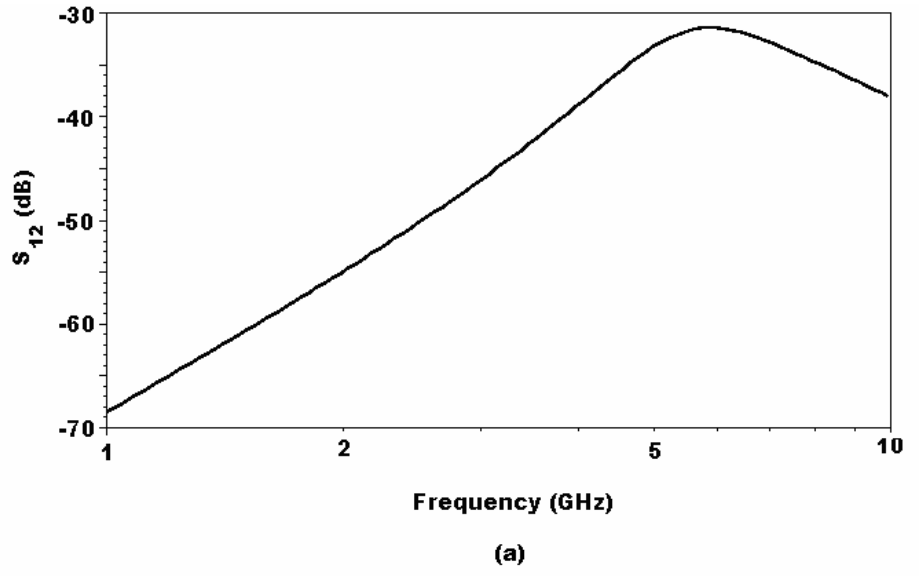


Figure 4.4 : (a) Input return loss of the proposed CMOS LNA (S_{11}) between 1 GHz - 10 GHz. (b) The same graphic (S_{11}) between 5 GHz - 6.5 GHz.



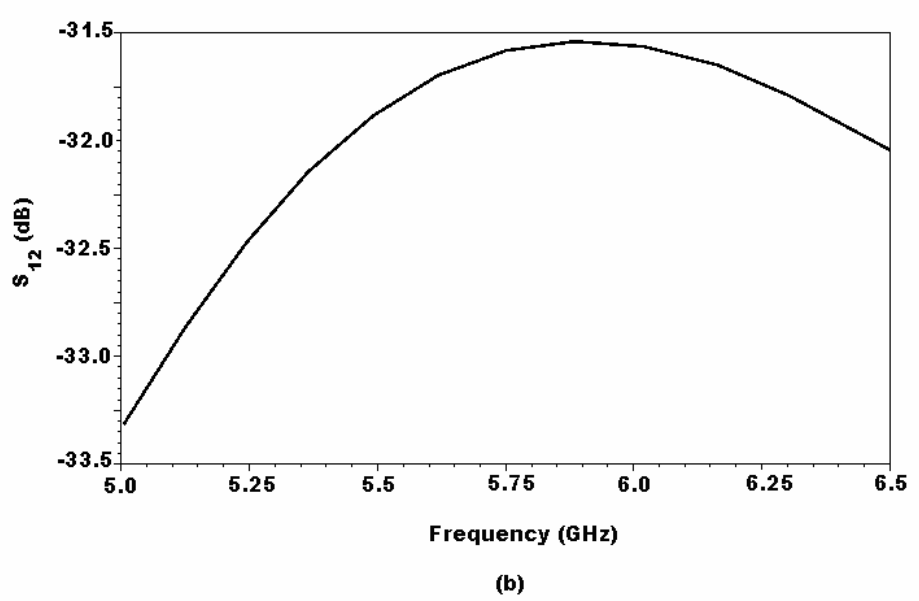
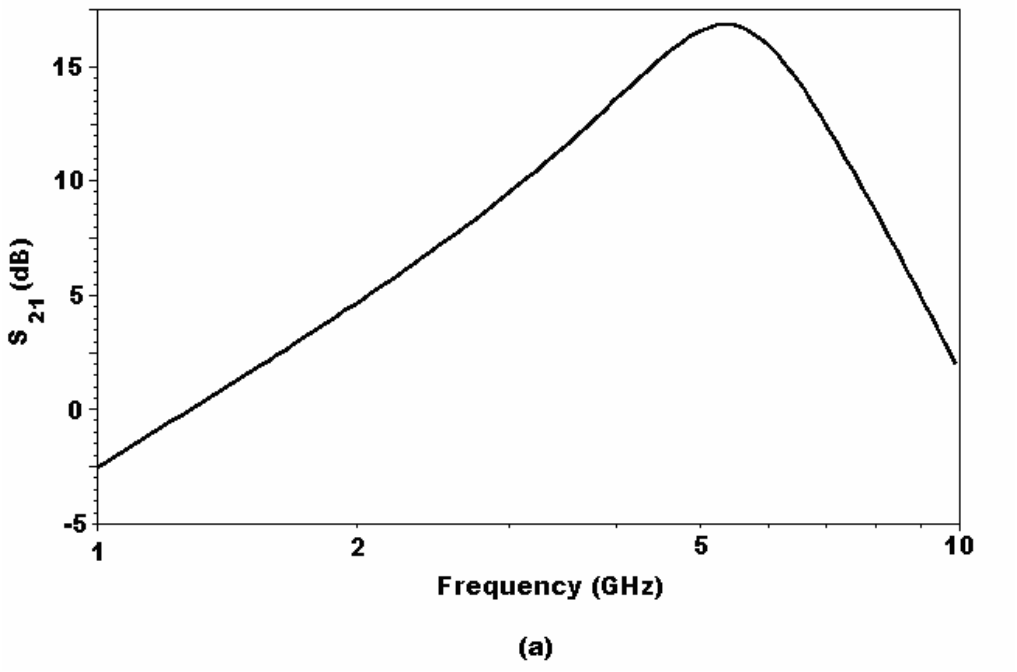


Figure 4.5 : (a) Reverse isolation between input and output terminals of the proposed CMOS LNA (S_{12}) between 1 GHz -10 GHz. (b) The same graphic (S_{12}) between 5 GHz - 6.5 GHz.

Voltage gain (S_{21}) of 16.47 dB is achieved at the frequency of 5.8 GHz, while maintaining good matching at the input (S_{11}) and at the output (S_{22}) of -32.17 dB and -16.71 dB respectively. The reverse isolation (S_{12}) of the LNA is less than -30 dB.



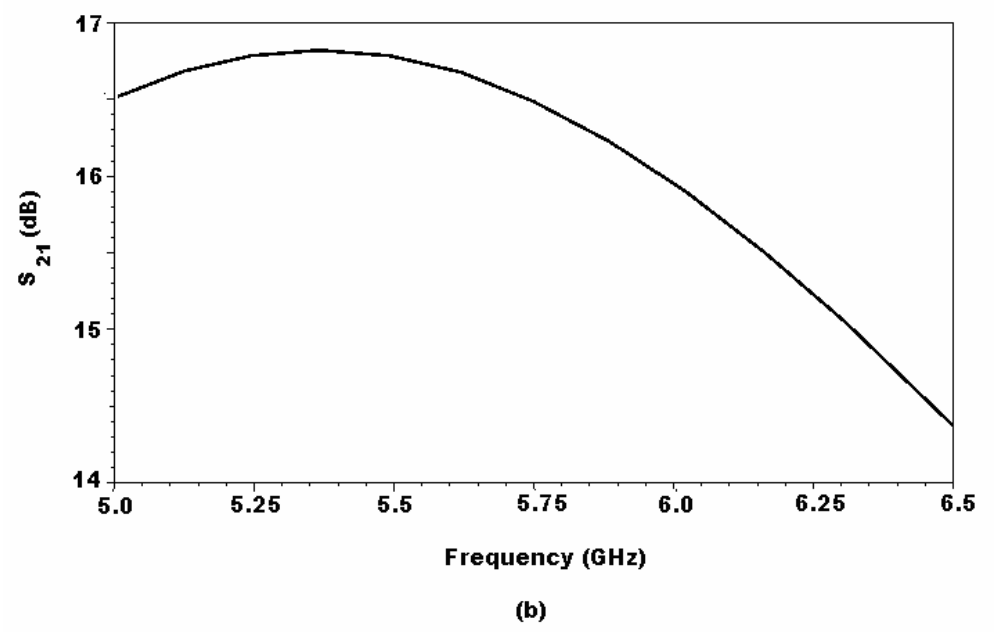


Figure 4.6 : (a) Voltage gain of the proposed CMOS LNA (S_{21}) between 1 GHz -10 GHz. (b) The same graphic (S_{21}) between 5 GHz - 6.5 GHz.

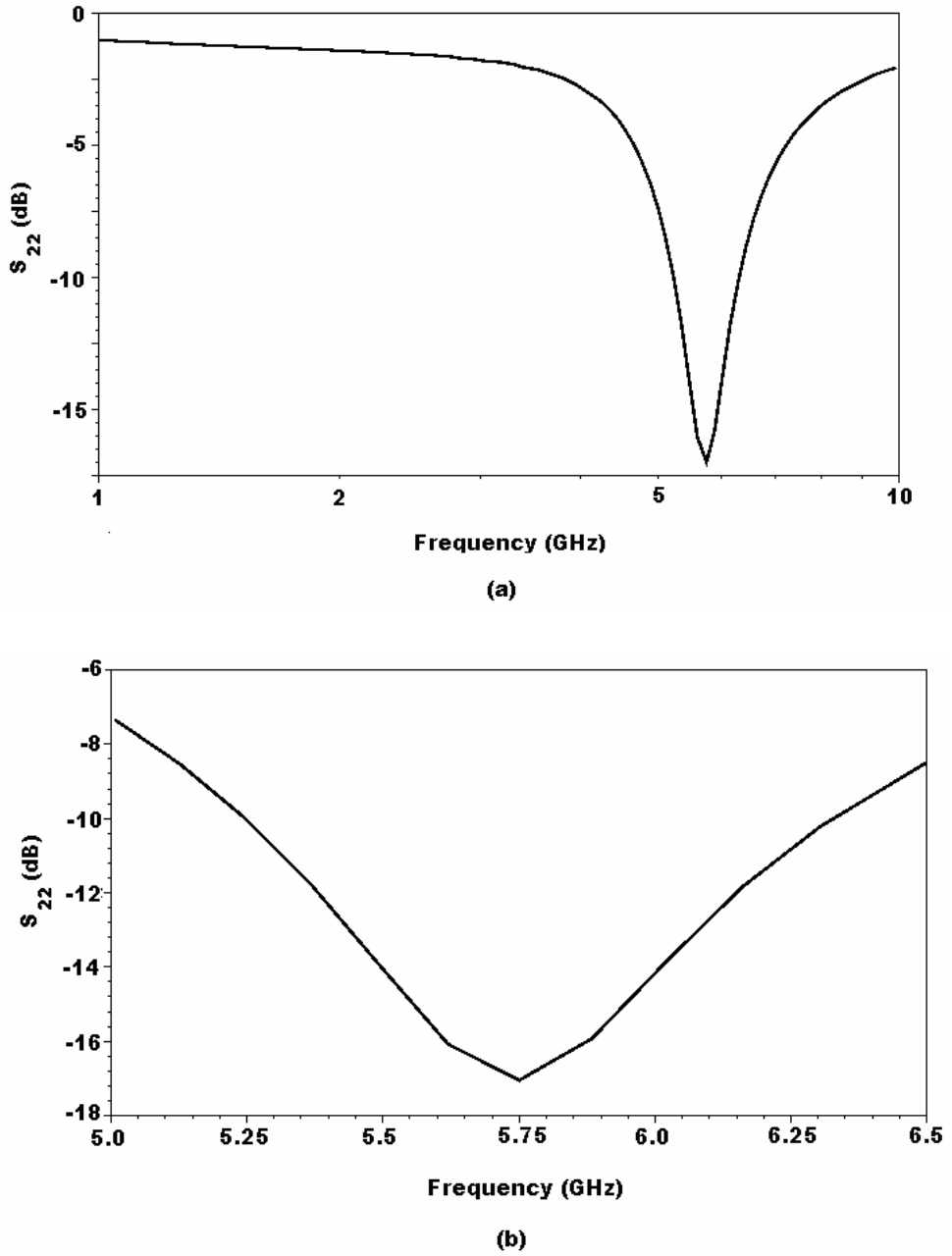


Figure 4.7 : (a) Output return loss of the proposed CMOS LNA (S_{22}) between 1 GHz -10 GHz. (b) The same graphic (S_{22}) between 5 GHz - 6.5 GHz.

The proposed LNA has noise figure (NF) of 1.226 dB where minimum noise figure is 1.022 dB as shown in Figure 3.8. The difference between 50 Ω and minimum noise figure is 0.2 dB at 5.8 GHz. The reason for not achieving minimum noise figure may be the fixed biasing current or the noise contribution of passive components which are not lossless as assumed during the analysis.

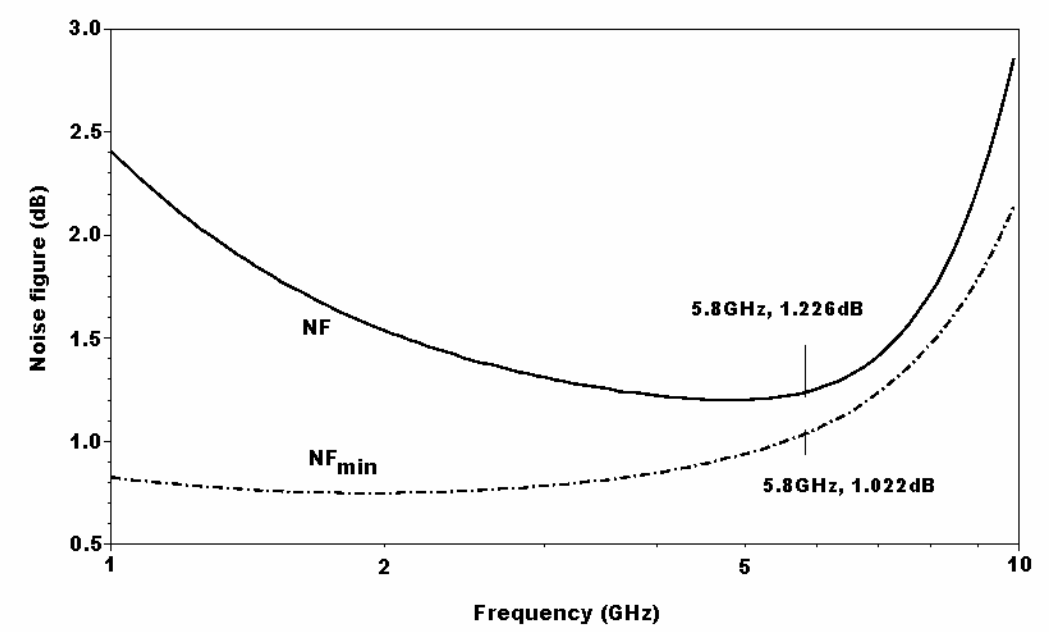


Figure 4.8 : Noise figure of the proposed CMOS LNA.

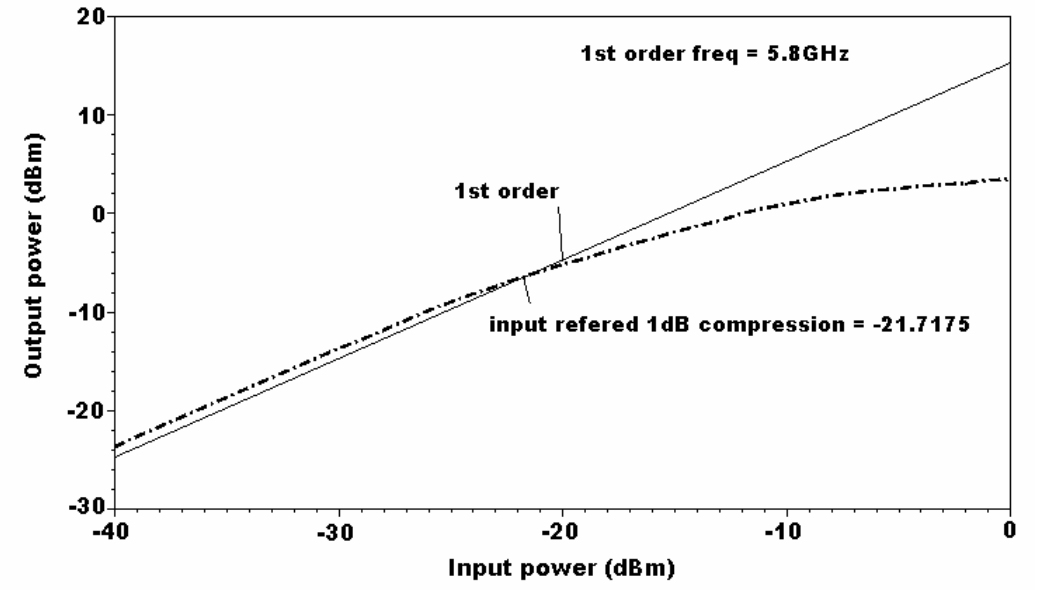


Figure 4.9 : 1-dB compression point of the proposed CMOS LNA (P_{1dB}).

Simulation results that exhibit the linearity performance of the proposed LNA are shown in Figure 4.9 - Figure 4.10. Simulated 1-dB compression point at 5.8 GHz is -6.25 dBm. Input referred third order intercept point (IIP_3) simulations are performed by inserting two frequencies at 5.8 and 5.9 GHz and IIP_3 is obtained as -11.98 dBm. In Figure 4.11, the transient response of the LNA is shown. The proposed LNA has

output voltage swing of 245 mV where total harmonic distortion of the output signal is only 1%.

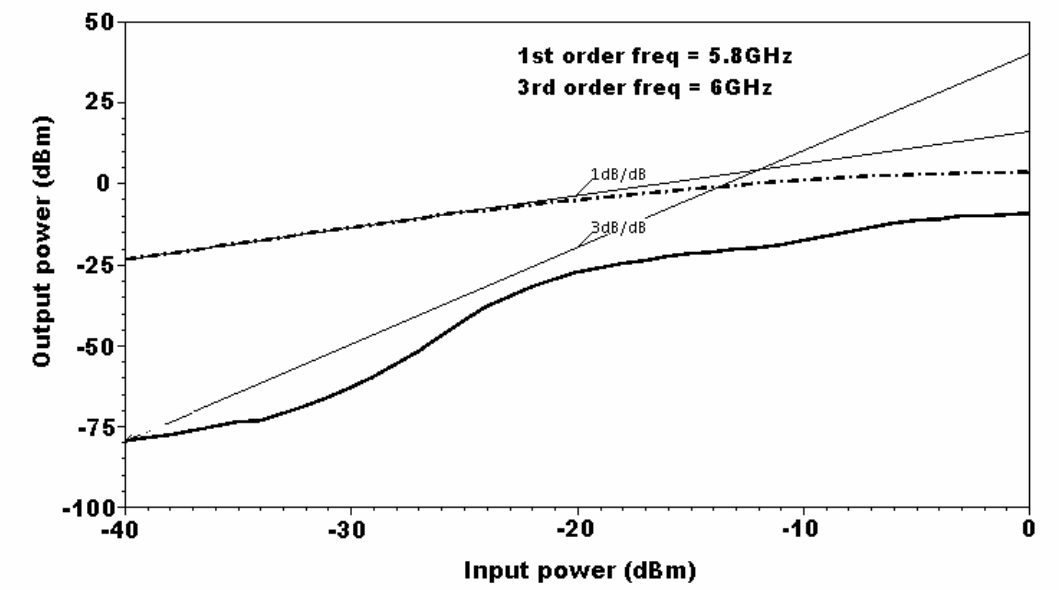


Figure 4.10 : Third-order intercept point of the proposed CMOS LNA (IIP_3).

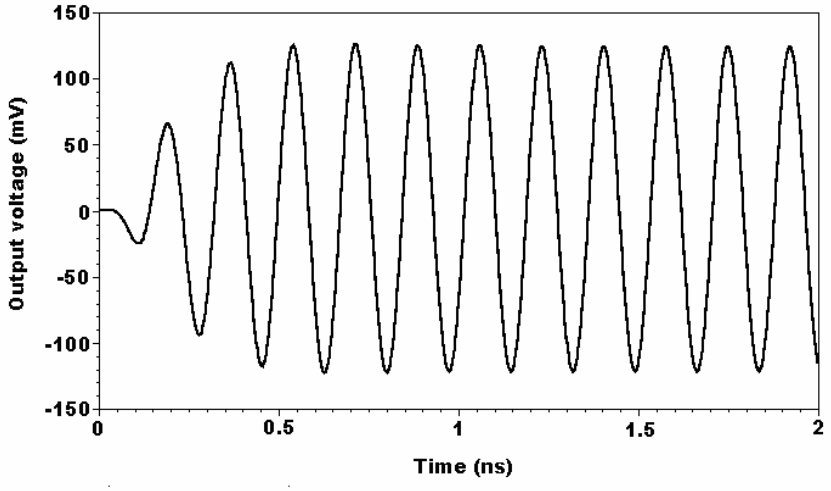


Figure 4.11 : Output signal of the proposed CMOS LNA with 1% THD.

Voltage gains and noise figures of these three LNA designs are shown in Figure 4.12 and 4.13, respectively. There is little decrease in the voltage gain of the inductively-degenerated LNA with external capacitor C_{ex} with respect to inductively-degenerated LNA without C_{ex}, since C_{ex} causes degradation in efficient transition frequency of input transistor. The small improvement in the noise figure with external C_{ex}

capacitance as shown in Figure 4.12 is provided at the cost of significant decrease in input matching. The proposed LNA with L-tapped output matching has the advantage of larger linear output power and considerable improve in the noise figure with respect to designs shown in Figure 4.1 and Figure 4.2, since output matching network does not include any real resistor. Finally, bandwidth of the voltage gain of the LNA is narrower than that of RLC tank load.

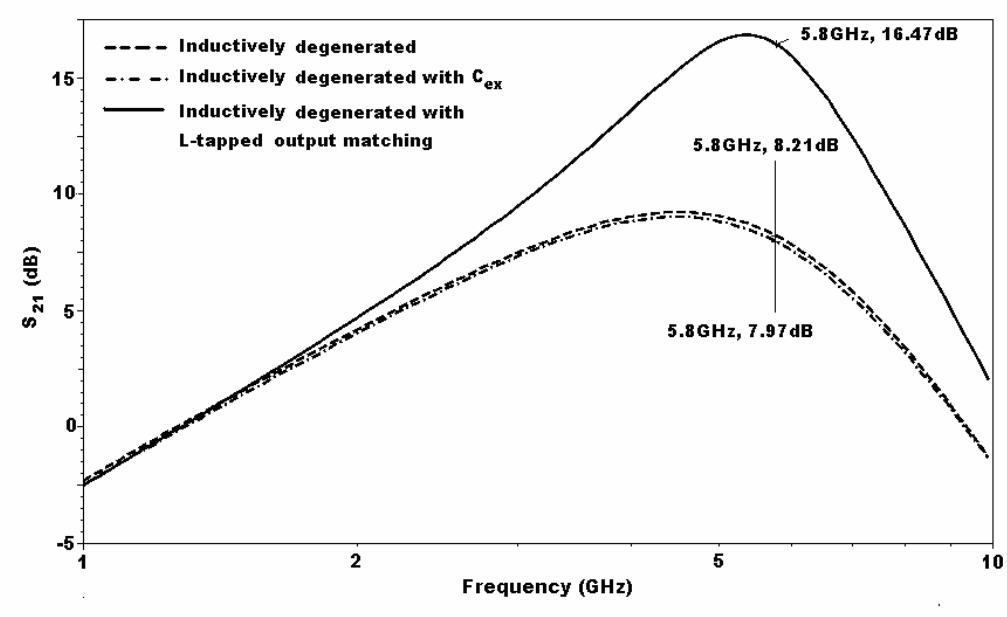


Figure 4.12 : Comparison of voltage gains designed CMOS LNAs.

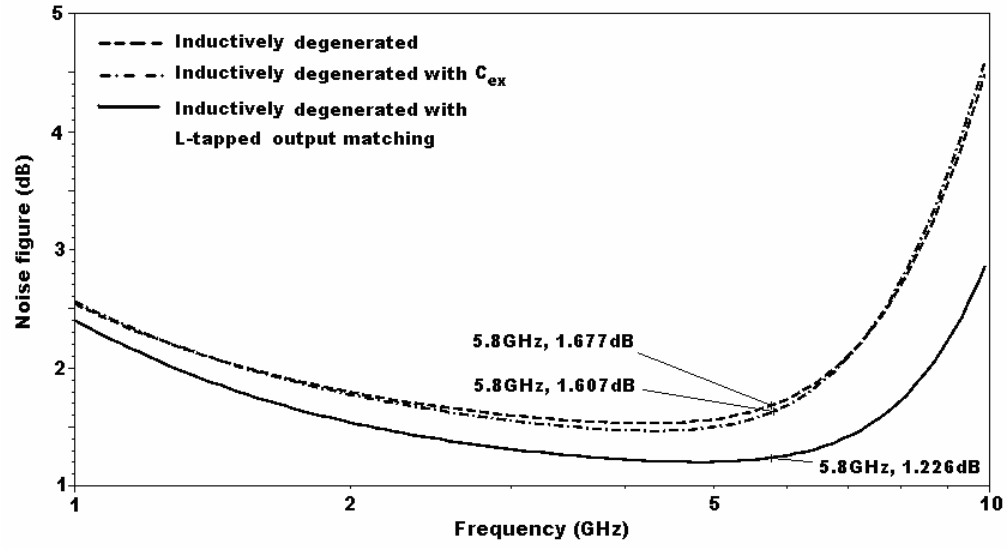


Figure 4.13 : Comparison of noise figures of designed CMOS LNAs.

Table 4.1 : Performance summaries of designed CMOS LNAs

at 5.8 GHz	Performance Parameters					
	NF (dB)	**S_{21} (dB)**	**S_{11} (dB)**	**S_{22} (dB)**	**P_{1dB} (dBm)**	**IIP_3 (dBm)**
Inductively-deg. with RLC tank	1.677	8.21	-37.41	-20.52	1.24	-9.84
Inductively-deg. with C_{ex} and RLC tank	1.607	7.97	-11.33	-20.81	1.442	-9.66
Inductively-deg. with L-tapped output matching	1.226	16.47	-32.17	-16.71	-6.25	-11.98

In Table 4.1, performance summaries of the three different CMOS LNA configurations designed in this section are presented. These LNAs have the same power consumption through the same supply voltage and same current. Additionally, the transistor sizes are same in each design; however, the input and output matching circuits are different.

Table 4.1 : Comparison of CMOS LNA performances.

at 5.8 GHz	Various LNA Configurations			
	This Work	***[6]***	***[7]***	***[8]***
Technology	0.13µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS
V_{CC} (V)	1.2	1.8	1.8	1
P_d (mW)	8	21.6	4.5	4.5
NF (dB)	1.226	1.8	1.4	2.463
S_{21} (dB)	16.47	14.1	16.7	11.57
S_{11} (dB)	-32.17	-21	-23	-15.35
S_{22} (dB)	-16.71	-11	-25	-16.26
P_{1dB} (dBm)	-6.25	-11.9	-15.6	n. a.
IIP_3 (dBm)	-11.98	4.2	-2.6	-5.47

Performance comparison with other CMOS LNAs in literature, operating at 5.8 GHz, is shown in Table 4.2. The noise figure, gain and input matching performance of the proposed LNA is better than the other LNAs, which demonstrates simultaneous noise and input matching can be achieved with comparable power consumption.

4.4 Design Procedure for SNIM CMOS LNA

Design procedure for SNIM CMOS LNA that is applied in this chapter can be summarized as follows:

First design step is determining the size and biasing of the input transistor so that input transistor becomes noise matched. The channel length of the input transistor must be chosen as small as possible in the given technology since it yields better noise figure. Channel width of the input transistor (W) is chosen so as to real part of the optimum noise impedance (R_{opt}) match to real part of the source impedance Z_s at the given power constraint and biasing conditions.

Second step is determining the value of degeneration inductance L_s which provides real part to the input impedance and shifts the value of X_{opt} by ωL_s. The value of L_s is determined so that imaginary part of the optimum noise impedance (X_{opt}) matches to imaginary part of the source impedance Z_s at desired frequency.

As third step gate-source voltage of the input transistor (V_{gs}) is determined so as to equalize real parts of the input impedance and source impedance for the selected values of W and L_s.

Finally, the value of the series gate inductance L_g is adjusted to cancel the imaginary part of the input impedance. This design procedure provides obtaining LNA with noise figure approximately equal to the F_{min} of the common-source transistor with nearly perfect input matching.

If there is a low power constraint, then the input transistor size must be low that leads to high value of optimum noise resistance due to small values of gate-source capacitance C_{gs} as seen from equation (2.33). For the given bias or ω_T (under the low consumption constraint L_s has to be very large in order to provide real part input matching as seen from equations (2.54) and (2.57). For values of L_s larger than a

certain value, equation (2.53) becomes invalid since with large L_s the transconductance of the input stage degrades significantly thus; the feedback through C_{gd} can not be neglected. Therefore, minimum achievable noise figure increases considerably. As a result, input matching network need external capacitance between gate and source terminals. In this case values of the design variables L_s and L_g can be calculated by using equations (4.3) and (4.4).

After values of the input elements are determined, appropriate matching network is designed for output of the LNA that maximizes the power transferred to the load and linear output power swing.

5. LAYOUT CONSIDERATIONS AND POST-LAYOUT SIMULATION RESULTS

This chapter includes layout issues and post layout simulation results of the proposed SiGe HBT LNA. The layout of the proposed CMOS LNA could not be drawn due to lack of the technology file of the UMC 0.13µm process that is required for the tool SPIRAL to synthesize degeneration inductor.

The circuit of the proposed SiGe HBT LNA is laid out in IHP 0.25µm BiCMOS process which has 4 metal layers using the Cadence Virtuoso layout tool. In order to minimize the noise and losses due to the parasitic elements layout of high frequency circuits must be drawn by reducing the effect of these parasitics wherever possible. On the other hand the maximum current densities must be taken into consideration that metal layers can carry for the lifetime of the circuit. For these purposes, wide interconnects and a large number of vias are used all over the chip to reduce the parasitic resistances and improve the gain and noise figure. While verifying input transistor Q1, two transistors are shunted together where each is consist of eight transistors with 0.21x0.84 μm^2 emitter area to reduce the base resistance, since base resistance has an important role on the noise figure of the LNA. Cascode transistor Q2 is implemented in the same way. Moreover inductances are placed away from each other and other circuit elements to prevent coupling and crosstalk. Finally top metal layer which has minimum sheet resistance is used in RF signal paths to prevent reduction in linearity (P_{1dB} and IIP3 values) of the circuit.

All the inductances used in the circuit are on-chip inductances. L1, L2 and L_b are present in the library of the used process. Some important RF parameters for these inductances are given in Table 5.1 where R_{SO} metal series resistance of coil (for low frequencies) and M2+M3+M4 represents that metal layers are shunted.

Table 5.1 : Important RF parameters for inductances

Inductor	**L (nH)**	**Metal Layers**	**R_{SO} (Ω)**	**Q (5.8 GHz)**
L1	2.8	M2+M3+M4	3.55 ± 0.22	11.25 ± 0.5
L_b	1.7	M2+M3+M4	1.65 ± 0.1	12.93 ± 0.5
L2	0.94	M2+M3+M4	0.95 ± 0.05	4.73 ± 0.4

The value of inductor L_e which is used for emitter degeneration is really small (L_e = 0.25 nH) and there is not any inductance smaller than 0.94 nH in the library of used process. Therefore, by using SPIRAL tool an emitter degeneration inductance is synthesized with the quality factor of approximately 7 in desired frequency band.

Layout of the proposed SiGe HBT LNA is shown in Figure 5.1. In this figure capacitances that are placed to prevent couplings are not shown. Moreover value of the external base-emitter capacitance C_{ex} is 10 fF smaller than that of in the schematic because of the parasitic capacitances. Also the value of the capacitance that is used in the L-tapped output matching circuit is 105 fF, 30 fF smaller than that of schematic due to the same reason as in the C_{ex} case. There is not any difference between the other element values of the circuit when layout compared to schematic.

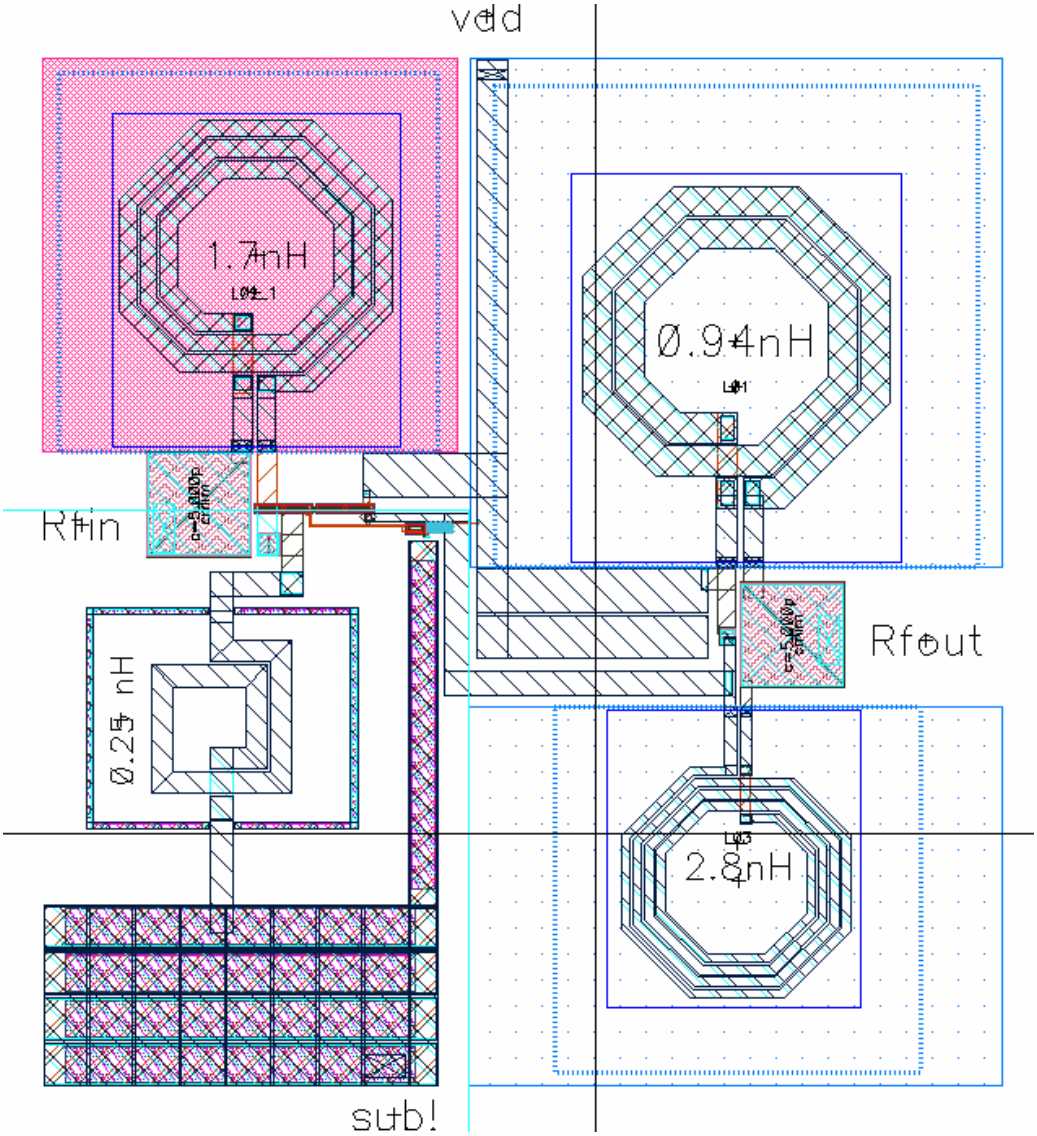
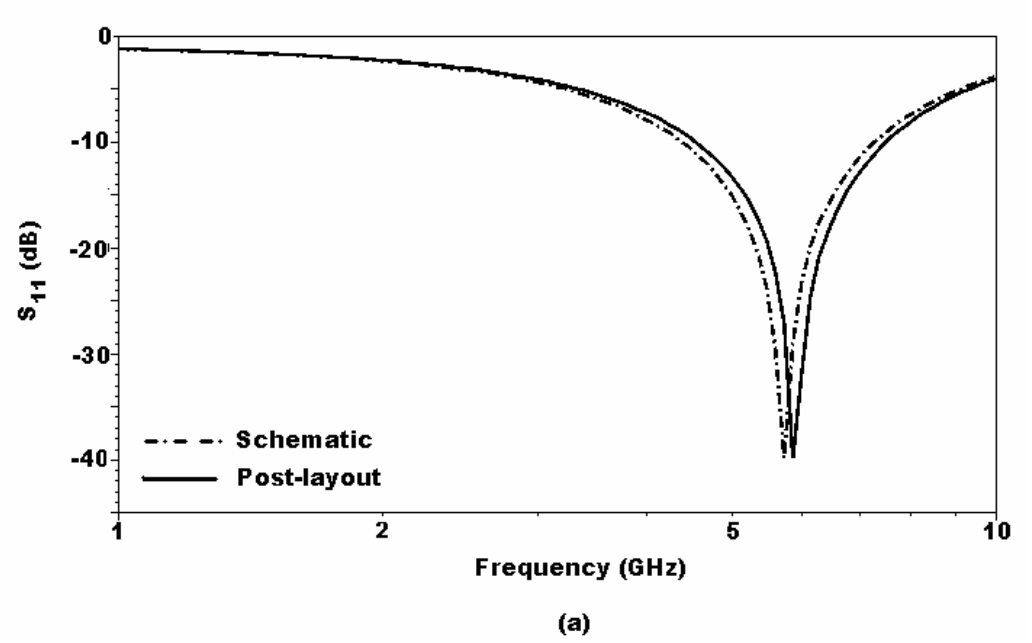


Figure 5.1 : Layout of the proposed SiGe HBT LNA.

Post-layout and schematic simulation results of scattering parameters of the proposed LNA are shown in Figure 5.2 - Figure 5.6. Voltage gain (S_{21}) of 22.94 dB is achieved at the frequency of 5.8 GHz, while maintaining good matching at the input (S_{11}) and at the output (S_{22}) of -31.5 dB and -10.34 dB respectively. The reverse isolation (S_{12}) of the LNA is less than -53 dB.



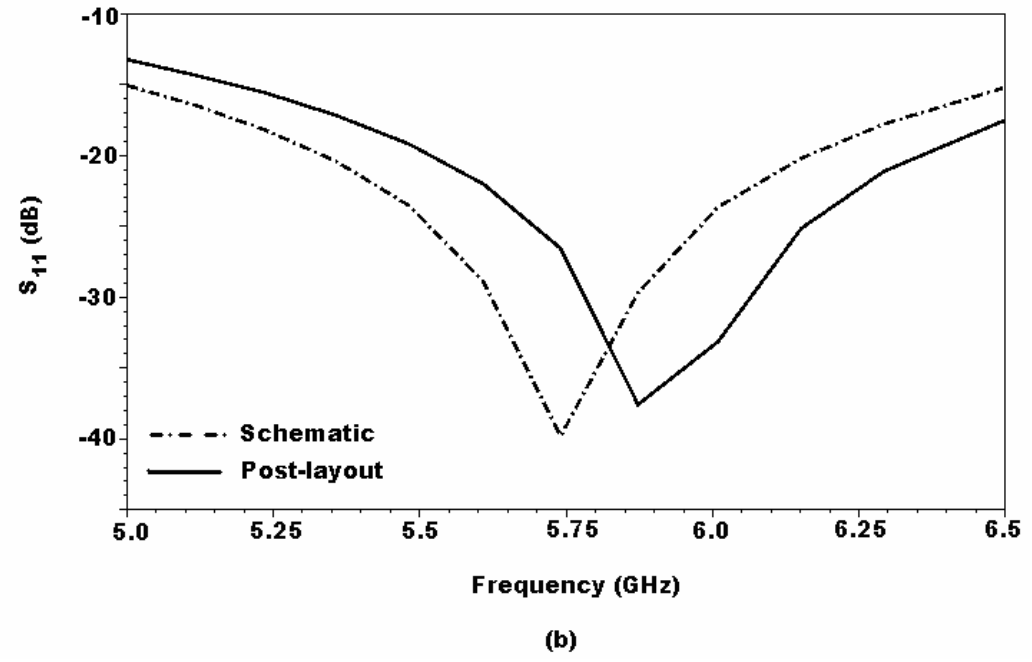
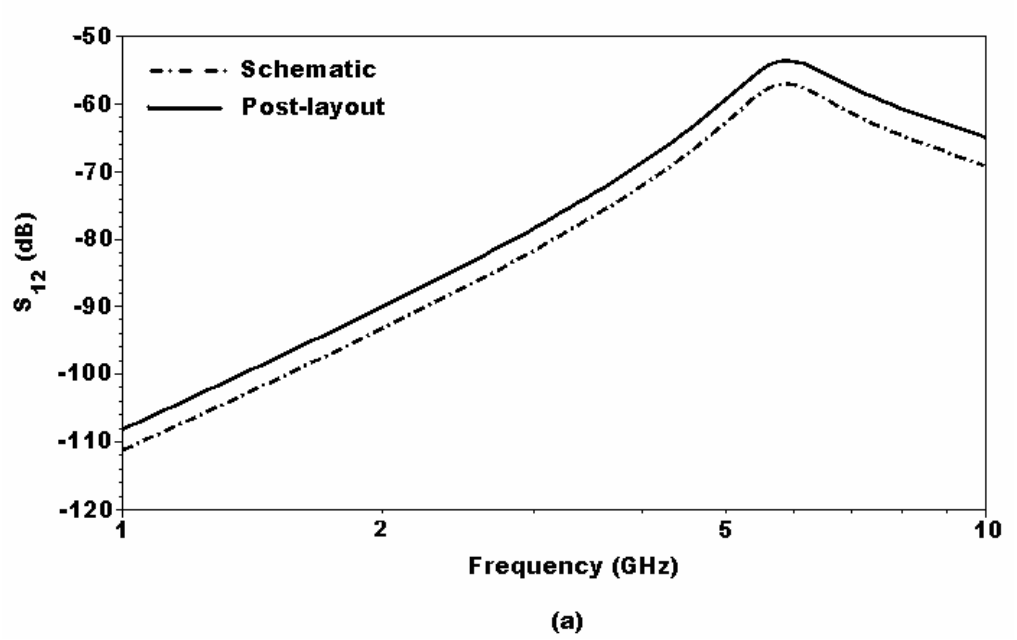


Figure 5.2 : (a) Input return loss of the proposed HBT SiGe LNA (S_{11}) between 1 GHz -10 GHz. (b) The same graphic (S_{11}) between 5 GHz - 6.5 GHz (post-layout).



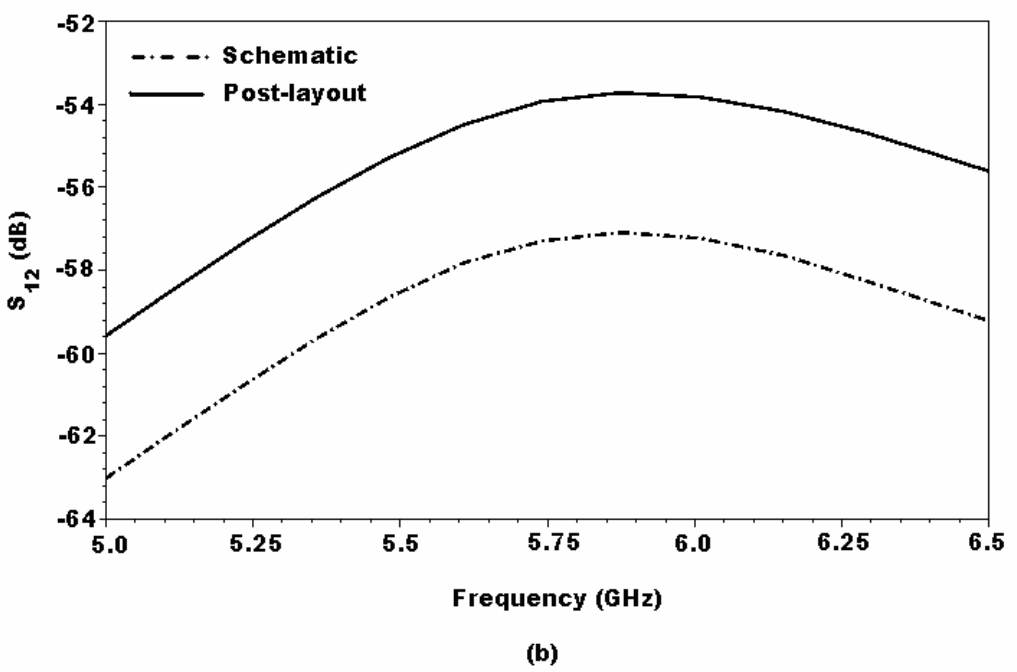
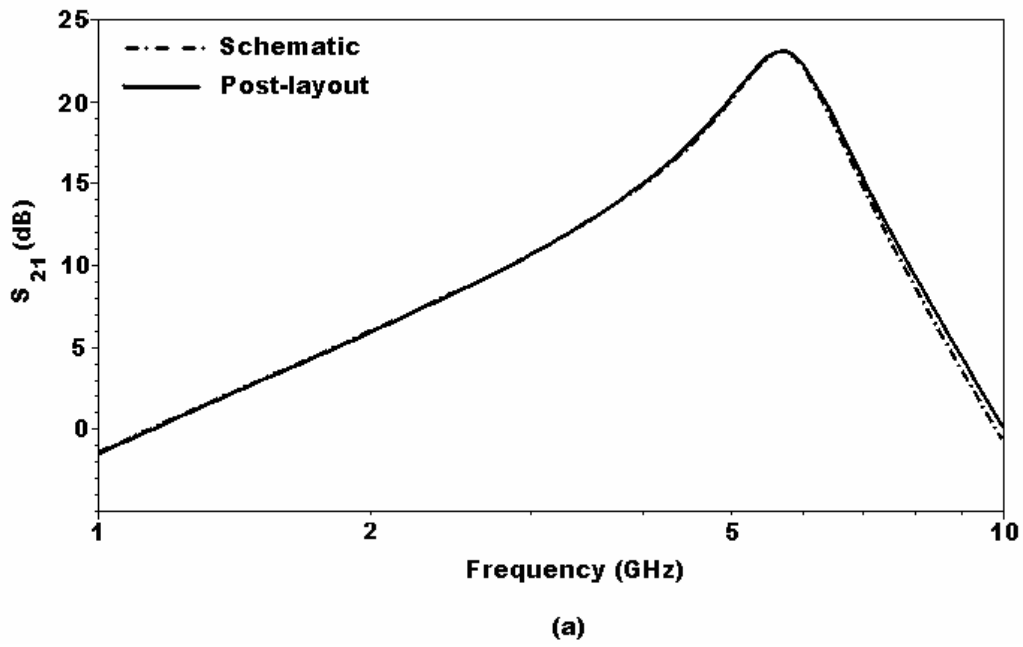


Figure 5.3 : (a) Reverse isolation between input and output terminals of the proposed HBT SiGe LNA (S_{12}) between 1 GHz -10 GHz. (b) The same graphic (S_{12}) between 5 GHz - 6.5 GHz (post-layout).



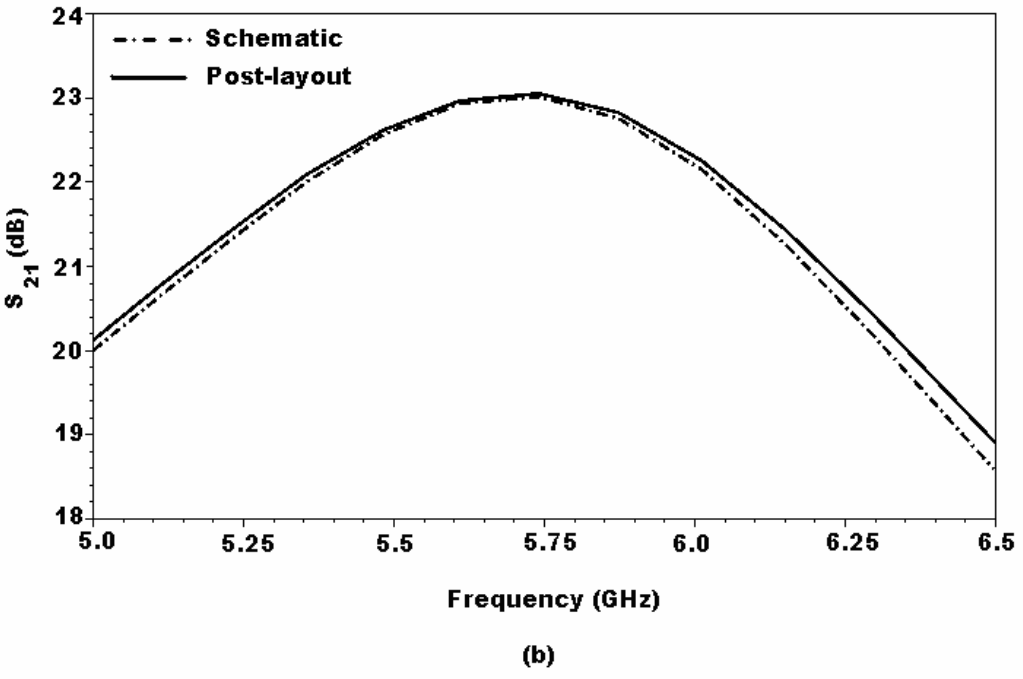
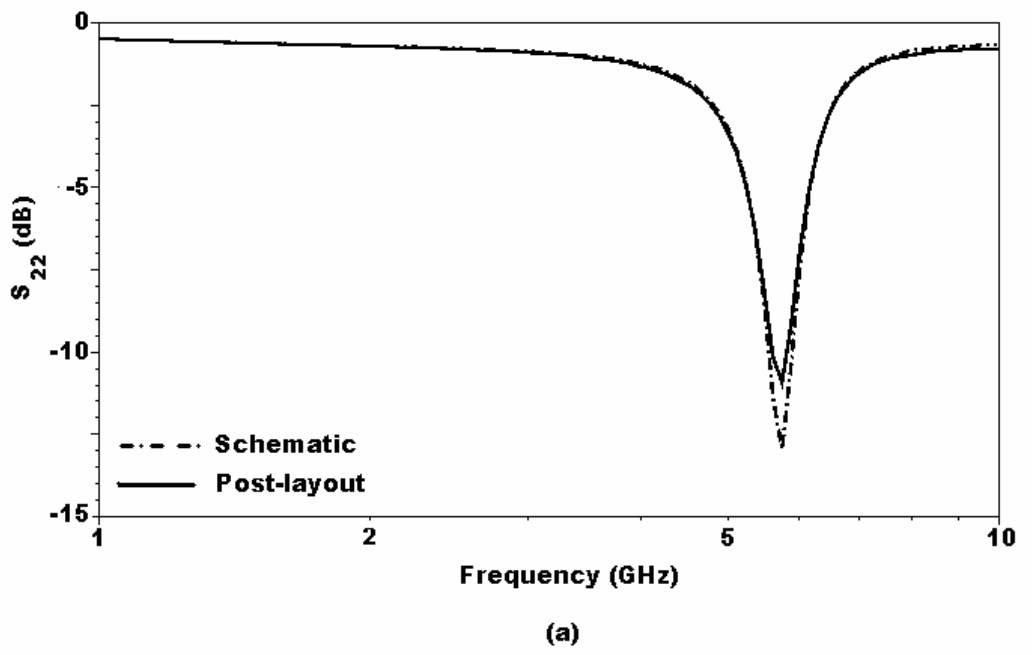


Figure 5.4 : (a) Voltage gain of the proposed SiGe HBT LNA (S_{21}) between 1 GHz - 10 GHz. (b) The same graphic (S_{21}) between 5 GHz - 6.5 GHz (post-layout).



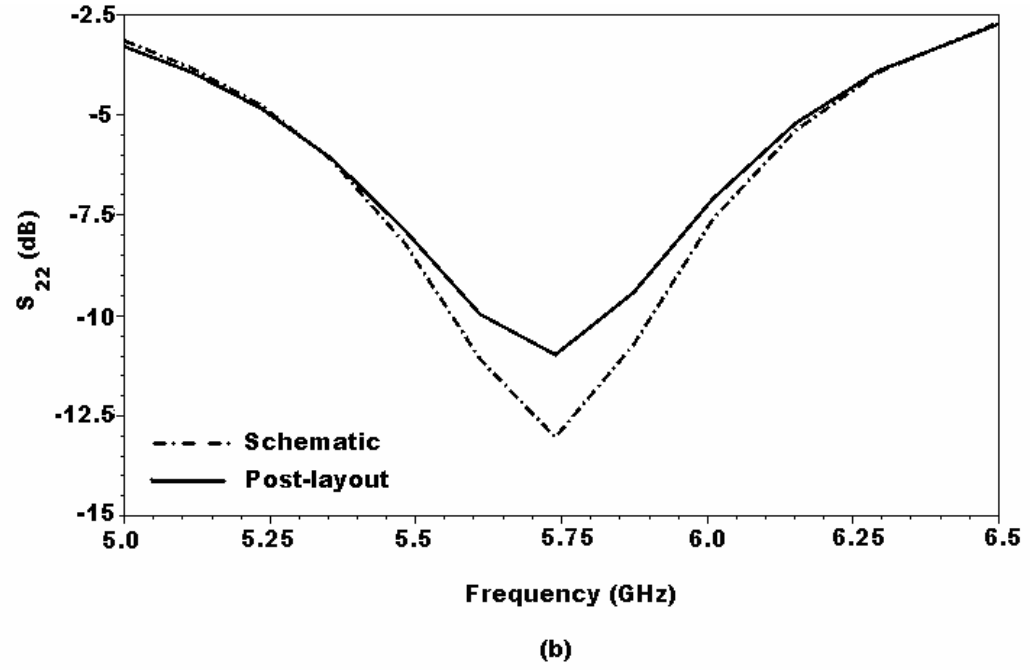


Figure 5.5 : (a) Output return loss of the proposed SiGe HBT LNA (S_{22}) between 1 GHz - 10GHz. (b) The same graphic (S_{22}) between 5 GHz - 6.5 GHz (post-layout).

The noise figure (NF) of LNA after the post layout simulations is 1.684 dB where minimum noise figure is 1.66 dB as shown in Figure 3.8. The difference between 50 Ω and minimum noise figure is only 0.02 dB at 5.8 GHz.

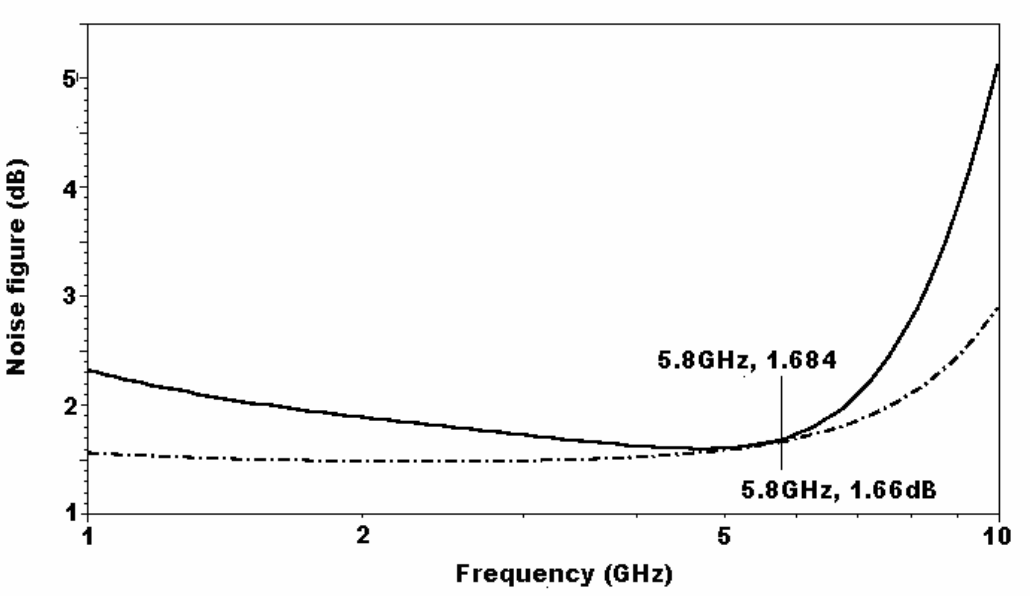


Figure 5.6 : Noise figure of the proposed SiGe HBT LNA.

The 1-dB compression point for the output power is -9.008 dBm at 5.8 GHz and input referred third-order intercept point (IIP_3) is obtained as –13.883 dBm by inserting two frequencies at 5.8 and 5.9 GHz as seen from Figure 5.7 – Figure 5.8. From the transient response of the LNA, the output voltage swing is obtained as 285 mV where total harmonic distortion of the output signal is 1%.

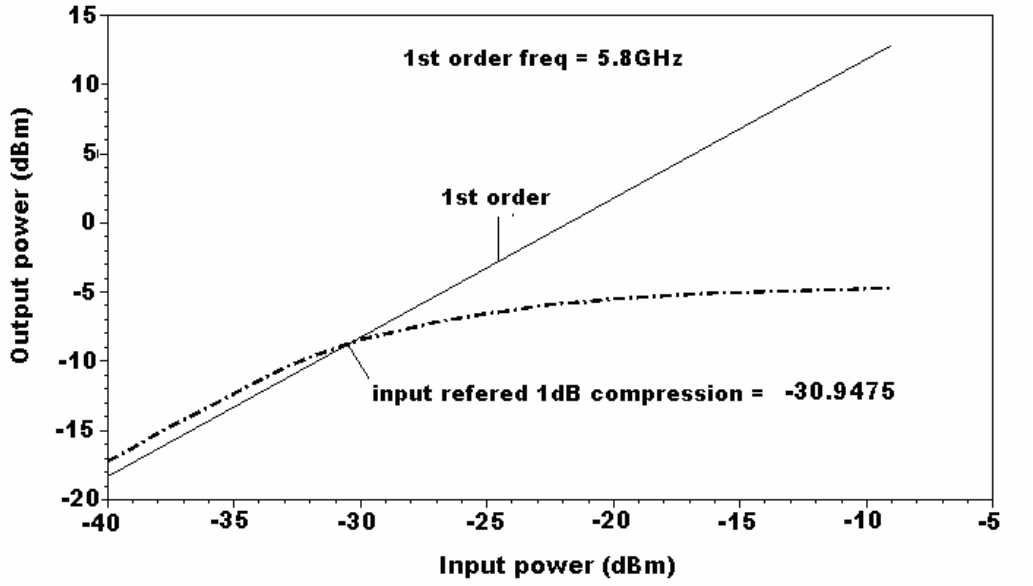


Figure 5.7 : 1-dB compression point of the proposed SiGe HBT LNA (P_{1dB}) (post-layout).

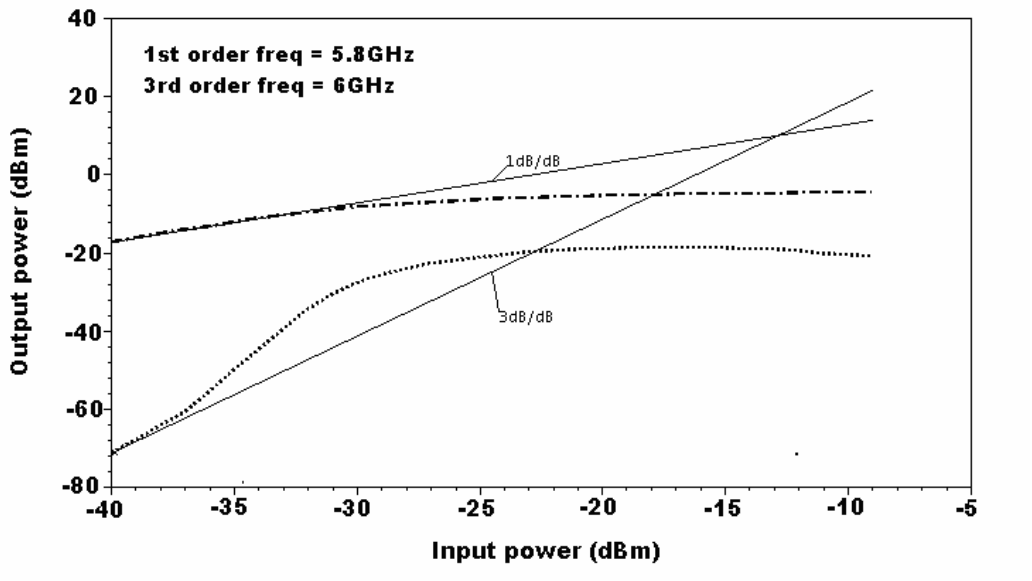


Figure 5.8 : Third-order intercept point of the proposed SiGe HBT LNA (IIP_3) (post-layout).

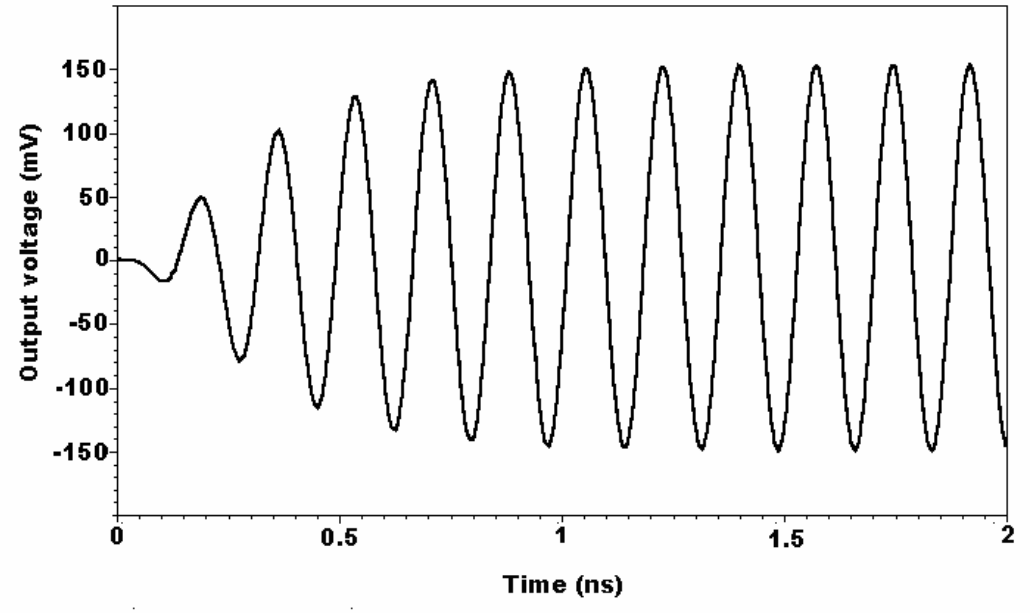


Figure 5.9 : Output signal of the proposed SiGe HBT LNA with 1% THD (post-layout).

CONCLUSION

The aim of this thesis is to review the theory and analysis of LNA circuits and to complete the designs of CMOS and SiGe HBT LNAs with minimum noise figure for IEEE 802.11a WLAN applications. Important design considerations of an LNA are noise figure, input impedance matching gain, power consumption and linearity. The inductively-degenerated architecture provides the possibility of achieving noise and input matching simultaneously in narrow band applications. On the other hand, cascode amplifiers are known as the best structure for a good tradeoff between low noise, high gain and stability. Therefore, this thesis is focused on LNAs based on the inductively-degenerated cascode topology.

At first, brief noise and matching performances of inductively-degenerated architecture are explored for SiGe HBT and CMOS devices. In order to improve the noise performances of the LNAs, the input matching networks are modified with an external base-emitter (or gate-source) capacitance. The impact of this capacitance is observed by comparing the designs with and without this capacitor for each process, SiGe HBT and CMOS. It has been shown that the external base-emitter (or gate-source) capacitance is required for the SiGe HBT LNA, however not required for the CMOS LNA under the given power consumption constraint.

Secondly, tapped-inductor matching is preferred as the output matching network to maximize the linear output power. Simulation results show that this output matching not only maximizes the linear output power but also improves the noise performance of the circuit since it does not include any real noisy resistor.

Finally, by using Spectre-RF simulator, two LNAs were designed and simulated by using the procedure introduced above. Two of the LNAs one of which is SiGe HBT and the other is CMOS operate at 5.8 GHz, since they are intended for IEEE 802.11a WLAN applications.

The further study includes implementing the final version of the designed SiGe HBT LNA if any financial support is found. The study will end with measuring the performances of the LNAs to verify simulation results.

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BIOGRAPHY

Pınar Başak BAŞYURT was born in Kırıkkale, TURKEY in 1983. She graduated from İzmir Fen Lisesi in 2000. In 2005, she received B.Sc. degree in Electronics and Communication Engineering from Istanbul Technical University where she started to pursue M.Sc. degree in the same year. She has been working as a research and teaching assistant at the Electronics and Communication Engineering Department of Istanbul Technical University since December 2005. Her research interests cover high frequency analog design.