

126973

QUADRATURE SIGNAL GENERATION IN 5-6GHz  
RANGE USING SiGe BiCMOS PROCESS

M.S. Thesis by  
Pinar TAŞCI, B.S.

504991071

**T.C. YÜKSEKÖĞRETİM KURULU  
DOKÜMANTASYON MERKEZİ**

Date of submission : 2 January 2002

Date of defence examination: 18 January 2002

Supervisor (Chairman): Assoc. Prof. Dr. Ali TOKER

Members of the Examining Committee Assoc. Prof. Sadri ÖZCAN

Assoc. Prof. Coşkun SÖNMEZ

**T.C. YÜKSEKÖĞRETİM KURULU  
DOKÜMANTASYON MERKEZİ**

JANUARY 2002

126973

**5-6GHz ARALIĞINDA, SiGe BiCMOS PROSES  
KULLANILARAK 90° FAZ FARKLI İŞARET ÜRETİMİ**

**YÜKSEK LİSANS TEZİ  
Müh. Pınar TAŞCI  
504991071**

**Tezin Enstitüye Verildiği Tarih : 2 Ocak 2002  
Tezin Savunulduğu Tarih : 18 Ocak 2002**

**Tez Danışmanı : Doç.Dr. Ali TOKER  
Diğer Jüri Üyeleri Doç.Dr. Sadri ÖZCAN  
Doç.Dr. Çoşkun SÖNMEZ**

**OCAK 2002**

## ACKNOWLEDGEMENT

I would like to thank to my supervisor Assoc. Prof. Dr. Ali TOKER, who have helped me from the beginning of my education in the university and supported me both for my B.Sc. and M.Sc. thesis.

I find it necessary to thank to my manager to Ibrahim Kurhan from Alcatel who supported me to continue to my education during two years of my work life and taught me a lot about RF design. I would like to thank to my project leader Jan Craninckx from Alcatel Microelectronics, who shared his knowledge on IC design with me and helped me to design the subject of my thesis.

I am very thankful to Ared Pontioglu from Alcatel, who supported me with all of my studies in and out of Alcatel with his great patience and who helped for the pictures of my thesis.

Ercan Altuntaş, helped me on the correction of the format of my thesis and solved many of my problems at work during my simulations. I am very grateful to him. I also would like to thank to my colleagues; Hüseyin Balcı, Feyzullah Yayıl.

I would like to thank to Alper Duruk, Veronique Bessodes, Isıl Öztelcan, Mariah Carey, Bruno Clairc, Florent Duarte who shared their friendships with me. I am very thankful to my grandfather Bayram Kaya, who supported me all my education life.

I feel obliged to dedicate my thesis to my mother, Nigar Taşcı, who encouraged and supported me while I was taking my steps at each stage of my life upon today.

I worked very hard during two years with job and with the studies of my thesis. I hope this thesis will be helpful to all the people who make research on this subject.

January, 2002

Pınar Taşcı

## CONTENTS

|                                          | <b><u>Page No</u></b> |
|------------------------------------------|-----------------------|
| <b>ACKNOWLEDGEMENT</b>                   | <b>iii</b>            |
| <b>ABBREVIATIONS</b>                     | <b>viii</b>           |
| <b>LIST OF TABLES</b>                    | <b>viii</b>           |
| <b>LIST OF FIGURES</b>                   | <b>ix</b>             |
| <b>LIST OF SYMBOLS</b>                   | <b>xivv</b>           |
| <b>ÖZET</b>                              | <b>xv</b>             |
| <b>SUMMARY</b>                           | <b>xvii</b>           |
| <br>                                     |                       |
| <b>1. INTRODUCTION</b>                   | <b>1</b>              |
| <br>                                     |                       |
| <b>2. BASICS IN RF SIGNAL GENERATION</b> | <b>6</b>              |
| 2.1 General Considerations               | 6                     |
| 2.2 Definition of Oscillation            | 7                     |
| 2.3 Oscillator Types                     | 9                     |
| 2.3.1 Wien-Bridge Oscillator             | 9                     |
| 2.3.2 Basic LC Oscillator Topologies     | 11                    |
| 2.3.2.1 Colpitts Oscillator              | 12                    |
| 2.3.2.2 Hartley Oscillator               | 14                    |
| 2.3.3 Crystal Oscillators                | 15                    |
| 2.3.3.1 Basics of Crystal Oscillators    | 15                    |
| 2.3.4 Relaxation oscillators             | 20                    |
| 2.3.5 Ring Oscillators                   | 22                    |
| 2.3.6 Other LC oscillators               | 24                    |
| <br>                                     |                       |
| <b>3. BASICS OF VCO DESIGN</b>           | <b>32</b>             |
| 3.1 Voltage Controlled Oscillators       | 32                    |
| 3.2 Basic VCO Terms                      | 33                    |
| 3.3 Phase Noise                          | 35                    |
| 3.3.1 General Considerations             | 35                    |
| 3.3.2 LC Oscillator Phase Noise          | 40                    |
| 3.3.3 Ring Oscillator Phase Noise        | 43                    |
| 3.4 Varactors                            | 46                    |
| 3.4.1 Varactor Diodes                    | 47                    |
| 3.4.2 MOS Varactors                      | 50                    |
| 3.4.3 Inversion-Mode MOS varactor        | 52                    |
| 3.4.4 Accumulation mode MOS varactor     | 53                    |

|           |                                                                   |            |
|-----------|-------------------------------------------------------------------|------------|
| 3.4.5     | Gated MOS varactor                                                | 56         |
| 3.5       | Inductors                                                         | 58         |
| 3.5.1     | Active inductors                                                  | 58         |
| 3.5.2     | Bondwire Inductors                                                | 59         |
| 3.5.3     | Spiral Inductors                                                  | 63         |
| <b>4.</b> | <b>REVIEW OF THE ON CHIP RF VCO CIRCUITS</b>                      | <b>70</b>  |
| 4.1       | RF VCOs                                                           | 70         |
| 4.1.1     | LC VCOs                                                           | 70         |
| 4.1.1.1   | Negative- $G_m$ LC VCOs                                           | 70         |
| 4.1.1.2   | Source-Coupled LC VCO                                             | 81         |
| 4.1.1.3   | Clapp Configuration VCO                                           | 82         |
| 4.1.1.4   | Comparison of the LC VCOs                                         | 83         |
| 4.1.2     | Ring Oscillators                                                  | 85         |
| 4.1.2.1   | Tuning of the Ring VCOs                                           | 85         |
| 4.1.2.2   | Examples of Ring VCOs                                             | 89         |
| 4.1.2.3   | Comparison of the ring oscillators                                | 93         |
| 4.2       | Quadrature Signal Generation                                      | 94         |
| 4.2.1     | RC-CR Network                                                     | 94         |
| 4.2.2     | Frequency Division                                                | 97         |
| 4.2.3     | Two Cross-Coupled VCO                                             | 98         |
| 4.2.4     | Quadrature Ring Oscillator                                        | 101        |
| 4.2.5     | Comparison of the Quadrature Generation Methods                   | 103        |
| <b>5.</b> | <b>DESIGN OF QUADRATURE LC AND RING VCOS FOR HIPERLAN2 SYSTEM</b> | <b>104</b> |
| 5.1       | LC oscillator with Quadrature Outputs                             | 104        |
| 5.1.1     | General Information                                               | 104        |
| 5.1.2     | Circuit Description                                               | 106        |
| 5.1.2.1   | Tuning of the Oscillator                                          | 106        |
| 5.1.2.2   | On Chip Inductance                                                | 107        |
| 5.1.2.3   | Buffer circuit                                                    | 110        |
| 5.1.2.4   | Biasing circuit                                                   | 111        |
| 5.1.3     | Discrete realization of quadrature LC oscillator                  | 111        |
| 5.1.4     | Simulation Results of the IC quadrature LC oscillator             | 113        |
| 5.1.4.1   | Typical Results                                                   | 115        |
| 5.1.4.2   | Characterization Simulations of the Quadrature LC VCO             | 118        |
| 5.1.4.3   | Monte Carlo Results                                               | 119        |
| 5.1.4.4   | Phase Noise Simulation                                            | 121        |
| 5.1.5     | Layout                                                            | 122        |
| 5.2       | Ring Oscillator with Quadrature Outputs                           | 125        |

|           |                                                         |            |
|-----------|---------------------------------------------------------|------------|
| 5.2.1     | General Information                                     | 125        |
| 5.2.2     | Circuit Description                                     | 125        |
| 5.2.2.1   | Tuning of the oscillator                                | 126        |
| 5.2.2.2   | Buffer circuit                                          | 131        |
| 5.2.3     | Simulation Results                                      | 132        |
| 5.2.3.1   | Typical results                                         | 133        |
| 5.2.3.2   | Characterization simulations of the quadrature ring VCO | 136        |
| 5.2.3.3   | Monte Carlo Simulations                                 | 137        |
| 5.2.3.4   | Phase Noise Simulations                                 | 138        |
| 5.3       | Comparison of the LC and ring VCOs                      | 140        |
| <b>6.</b> | <b>CONCLUSION</b>                                       | <b>142</b> |
|           | <b>REFERENCES</b>                                       | <b>148</b> |
| <b>A</b>  | <b>APPENDIX A</b>                                       | <b>158</b> |
| A.1       | Quality factor Q                                        | 158        |
| A.2       | Basic Properties of RLC Circuits                        | 159        |
| <b>B</b>  | <b>APPENDIX B</b>                                       | <b>163</b> |
| B.1       | Phase noise calculation of HP-ADS                       | 163        |
| <b>C</b>  | <b>APPENDIX C</b>                                       | <b>166</b> |
|           | <b>AUTOBIOGRAPHY</b>                                    | <b>179</b> |

## ABBREVIATIONS

|                 |                                               |
|-----------------|-----------------------------------------------|
| <b>ALC</b>      | : Automatic Level Control                     |
| <b>FET</b>      | : Field Effect Transistor                     |
| <b>Q</b>        | : Quality Factor                              |
| <b>MOS</b>      | : Metal-Oxide Semiconductor                   |
| <b>CMOS</b>     | : Complementary Metal-Oxide Semiconductor     |
| <b>NMOS</b>     | : n-Channel Metal-Oxide Semiconductor         |
| <b>PMOS</b>     | : p-Channel Metal-Oxide Semiconductor         |
| <b>BJT</b>      | : Bipolar Junction Transistor                 |
| <b>IC</b>       | : Integrated Circuit                          |
| <b>PLL</b>      | : Phase Locked Loop                           |
| <b>RF</b>       | : Radio Frequency                             |
| <b>VCO</b>      | : Voltage Controlled Oscillator               |
| <b>LO</b>       | : Local Oscillator                            |
| <b>LTI</b>      | : Linear Time Variant                         |
| <b>LTV</b>      | : Linear Time Varying                         |
| <b>GMD</b>      | : Geometric Mean Distance                     |
| <b>AMD</b>      | : Arithmetic Mean Distance                    |
| <b>Si</b>       | : Silicon                                     |
| <b>VXO</b>      | : Variable-Frequency Crystal Oscillators      |
| <b>VFO</b>      | : Variable-Frequency Oscillators              |
| <b>DECT</b>     | : Digital European Cordless Telephones        |
| <b>LAN</b>      | : Local Area Network                          |
| <b>BiCMOS</b>   | : Bipolar CMOS                                |
| <b>SiGe</b>     | : Silicon Germanium                           |
| <b>HIPERLAN</b> | : High Performance Local Area Network         |
| <b>WLAN</b>     | : Wireless Local Area Network                 |
| <b>PSS</b>      | : Periodic Steady State                       |
| <b>HP-ADS</b>   | : Hewlett Packard Advanced Design System      |
| <b>IO</b>       | : Input Output                                |
| <b>GND</b>      | : Ground                                      |
| <b>GSSG</b>     | : Ground-Signal-Signal-Ground                 |
| <b>SST</b>      | : Steady State Transient                      |
| <b>GaAs</b>     | : Gallium Arsenic                             |
| <b>QPSK</b>     | : Quadrature Phase Shift Keying               |
| <b>GMSK</b>     | : Gaussian Phase Shift Keying                 |
| <b>OFDM</b>     | : Orthogonal Frequency-Division Multiplexing. |

## LIST OF TABLES

|                   | <u>Page No</u>                                                                                        |
|-------------------|-------------------------------------------------------------------------------------------------------|
| <b>Table 4.1</b>  | Frequency behaviors of the VCOs proposed in [60]..... 77                                              |
| <b>Table 4.2</b>  | Phase noise Behaviour of the VCOs proposed in [60]..... 77                                            |
| <b>Table 4.3</b>  | Selected Phase Noise data points[80]..... 81                                                          |
| <b>Table 4.4</b>  | Figure of merit and tuning range by VCO type, with a comparison to other published VCOs [80] ..... 81 |
| <b>Table 4.5</b>  | Comparison of negative- $G_m$ LC VCOs ..... 83                                                        |
| <b>Table 4.6</b>  | Comparison of the ring VCOs..... 94                                                                   |
| <b>Table 5.1</b>  | Dimension of the transistors in Planar LC oscillator ..... 106                                        |
| <b>Table 5.2</b>  | Device dimensions of MOS varactor circuit ..... 107                                                   |
| <b>Table 5.3</b>  | Optimal coil parameters ..... 108                                                                     |
| <b>Table 5.4</b>  | Device values in the Nine-Element Model of the spiral ..... 109                                       |
| <b>Table 5.5</b>  | Dimensions of the buffer circuit..... 110                                                             |
| <b>Table 5.6</b>  | Device dimensions of the biasing circuits..... 111                                                    |
| <b>Table 5.7</b>  | Typical stimuli values for LC oscillator..... 115                                                     |
| <b>Table 5.8</b>  | Typical Simulation Results of LC oscillator (Eldo)..... 118                                           |
| <b>Table 5.9</b>  | Characterization Results of LC oscillator ..... 119                                                   |
| <b>Table 5.10</b> | Deviation value for the MOS transistors..... 121                                                      |
| <b>Table 5.11</b> | Dimension of the transistors in delay cell ..... 126                                                  |
| <b>Table 5.12</b> | Dimensions of the devices in NMOS bias circuit ..... 127                                              |
| <b>Table 5.13</b> | Dimensions of the devices of the op-amp circuit for NMOS biasing circuit..... 128                     |
| <b>Table 5.14</b> | Dimensions of the devices of the PMOS bias circuit..... 129                                           |
| <b>Table 5.15</b> | Dimensions of the devices in the op-amp circuit of PMOS bias circuit..... 130                         |
| <b>Table 5.16</b> | Dimensions of the devices in buffer circuit..... 131                                                  |
| <b>Table 5.17</b> | Typical stimuli value for ring oscillator ..... 133                                                   |
| <b>Table 5.18</b> | Ring Oscillator Typical condition results..... 136                                                    |
| <b>Table 5.19</b> | Characterization results of ring oscillator ..... 136                                                 |
| <b>Table 5.20</b> | Deviation of NPN transistors in the delay cell. .... 137                                              |
| <b>Table 5.21</b> | Deviation of MOS transistors..... 138                                                                 |
| <b>Table 5.22</b> | Monte Carlo simulation phase mismatch results..... 138                                                |
| <b>Table 5.23</b> | Characterization results of the oscillators ..... 141                                                 |
| <b>Table 5.24</b> | Phase Difference Error with Monte Carlo simulations ..... 141                                         |

## LIST OF FIGURES

|                                                                                                                                                    | <u>Page No</u> |
|----------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| <b>Figure 2.1</b> : Unity feedback oscillatory system [21].....                                                                                    | 7              |
| <b>Figure 2.2</b> : Feedback system with frequency selective network [34] .....                                                                    | 8              |
| <b>Figure 2.3</b> : Automatic level control system [21].....                                                                                       | 9              |
| <b>Figure 2.4</b> : Wien Bridge oscillator [34].....                                                                                               | 10             |
| <b>Figure 2.5</b> : (a) Feedback from collector to emitter (b) Insertion of an impedance transformer. [21] .....                                   | 11             |
| <b>Figure 2.6</b> : Use of an explicit transformer [21] .....                                                                                      | 12             |
| <b>Figure 2.7</b> : Colpitts oscillator [21].....                                                                                                  | 12             |
| <b>Figure 2.8</b> : Colpitts oscillator with MOS transistor [35].....                                                                              | 14             |
| <b>Figure 2.9</b> : Hartley oscillator [21] .....                                                                                                  | 14             |
| <b>Figure 2.10</b> : (a) Crystal resonator symbol (b) Equivalent circuit of a crystal resonator.[34] .....                                         | 15             |
| <b>Figure 2.11</b> : Crystal reactance versus frequency .....                                                                                      | 17             |
| <b>Figure 2.12</b> : Colpitts crystal oscillator operating in parallel resonant configuration [37].....                                            | 18             |
| <b>Figure 2.13</b> : Colpitts crystal oscillator operating in series resonant configuration [37].....                                              | 18             |
| <b>Figure 2.14</b> : (a) Pierce oscillator realization for fundamental crystals, (b) Colpitts oscillator realization for fundamental crystals..... | 19             |
| <b>Figure 2.15</b> : Emitter coupled multivibrator [42] .....                                                                                      | 20             |
| <b>Figure 2.16</b> : A simplified circuit of CMOS relaxation oscillator [8] .....                                                                  | 21             |
| <b>Figure 2.17</b> : Three stage ring oscillator using CMOS inverters [35]. .....                                                                  | 22             |
| <b>Figure 2.18</b> : Five stage ring oscillator using CMOS inverters. ....                                                                         | 22             |
| <b>Figure 2.19</b> : Four-stage ring oscillator with quadrature outputs [42].....                                                                  | 23             |
| <b>Figure 2.20</b> : Tuned gain stage [35].....                                                                                                    | 24             |
| <b>Figure 2.21</b> : Two tuned stages in a feedback loop [35].....                                                                                 | 25             |
| <b>Figure 2.22</b> : Redraw of the oscillator in Fig. 2.21 [35]. ....                                                                              | 25             |
| <b>Figure 2.23</b> : Addition of tail current to lower the supply sensitivity [35].....                                                            | 25             |
| <b>Figure 2.24</b> : One port view of oscillators [21] .....                                                                                       | 26             |
| <b>Figure 2.25</b> : (a) LC resonator (b) Equivalent circuit of (a) .....                                                                          | 27             |
| <b>Figure 2.26</b> : Source follower with positive feedback to create negative input impedance [35].....                                           | 28             |
| <b>Figure 2.27</b> : Oscillator using negative input resistance of a source follower with positive feedback.....                                   | 28             |
| <b>Figure 2.28</b> : Redrawing of the topology in Fig. 2.27[35].....                                                                               | 29             |
| <b>Figure 2.29</b> : Differential version of the topology in Fig.2.28 [35].....                                                                    | 29             |
| <b>Figure 2.30</b> : Equivalent circuit of Fig. 2.29 [35] .....                                                                                    | 30             |
| <b>Figure 2.31</b> : (a) Colpitts oscillator with active buffer in the feedback loop (b) implementation of buffer with emitter follower [21] ..... | 31             |
| <b>Figure 2.32</b> : Differential implementation of Fig. 2.31(b).....                                                                              | 31             |
| <b>Figure 2.33</b> : Differential implementation of Fig. 2.31(b) with MOS transistors [21] .....                                                   | 31             |

|                    |                                                                                                                                                                                                   |    |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| <b>Figure 3.1</b>  | : Definition of VCO [35].....                                                                                                                                                                     | 33 |
| <b>Figure 3.2</b>  | : Nonlinear VCO characteristic[35] .....                                                                                                                                                          | 34 |
| <b>Figure 3.3</b>  | : Output spectrum of the ideal and the actual oscillators [21].....                                                                                                                               | 36 |
| <b>Figure 3.4</b>  | : Power spectrum of oscillator [44] .....                                                                                                                                                         | 37 |
| <b>Figure 3.5</b>  | : Phase fluctuation power spectral density [44].....                                                                                                                                              | 38 |
| <b>Figure 3.6</b>  | : Generic transceiver front end [6] .....                                                                                                                                                         | 38 |
| <b>Figure 3.7</b>  | : (a) Downconversion by an ideal oscillator (b) reciprocal mixing....                                                                                                                             | 39 |
| <b>Figure 3.8</b>  | : Effect of the phase noise in transmitters .....                                                                                                                                                 | 39 |
| <b>Figure 3.9</b>  | : A definition of Q [ 21] .....                                                                                                                                                                   | 40 |
| <b>Figure 3.10</b> | : Definition of Q based on open-loop phase slope[21].....                                                                                                                                         | 41 |
| <b>Figure 3.11</b> | : General circuit diagram for an LC tune oscillator [11 ].....                                                                                                                                    | 42 |
| <b>Figure 3.12</b> | : Linearized of CMOS VCO [6].....                                                                                                                                                                 | 44 |
| <b>Figure 3.13</b> | : LC oscillator using varactor diodes.....                                                                                                                                                        | 47 |
| <b>Figure 3.14</b> | : Diodes realized in CMOS technology [35].....                                                                                                                                                    | 48 |
| <b>Figure 3.15</b> | : Circuit model of the varactor diode shown in Figure 3.14b .....                                                                                                                                 | 48 |
| <b>Figure 3.16</b> | : Tuning characteristic of the VCO with diode varactor [58].....                                                                                                                                  | 49 |
| <b>Figure 3.17</b> | : Capacitance curve of the p-n junction varactor [59].....                                                                                                                                        | 50 |
| <b>Figure 3.18</b> | : Tuning characteristic for the pMOS varactor with $B \equiv D \equiv S$ [60].....                                                                                                                | 51 |
| <b>Figure 3.19</b> | : Simulated capacitance curve of the pMOS varactor [59] .....                                                                                                                                     | 52 |
| <b>Figure 3.20</b> | : Tuning characteristics for the inversion-mode MOS varactor [60] .                                                                                                                               | 52 |
| <b>Figure 3.21</b> | : Accumulation-mode MOS varactor [60] .....                                                                                                                                                       | 53 |
| <b>Figure 3.22</b> | : Tuning characteristic for the accumulation mode varactor [60] .....                                                                                                                             | 54 |
| <b>Figure 3.23</b> | : Measured Q factor of accumulation MOS varactors presented in [62] .....                                                                                                                         | 54 |
| <b>Figure 3.24</b> | : Minimum current consumption for the diode varactor VCO, I-MOS varactor VCO, and A-MOS varactor VCO [60].....                                                                                    | 55 |
| <b>Figure 3.25</b> | : Polysilicon oxide silicon varactor: cross section [63].....                                                                                                                                     | 56 |
| <b>Figure 3.26</b> | : Measured capacitance and quality factor at 1800MHz [63]. .....                                                                                                                                  | 56 |
| <b>Figure 3.27</b> | : Cross-section of the P-type (N-body) gated varactor. $V_d$ and $V_g$ are the bias voltage applied to the “Drain” and “Gate” respectively[65]. .....                                             | 57 |
| <b>Figure 3.28</b> | : The C-V characteristic of the gated varactors versus gate voltage $V_g$ at various $V_d$ - $C_{ox}$ is the gate oxide capacitance and $C_{j0}$ is the zero-bias junction capacitance [65]...... | 58 |
| <b>Figure 3.29</b> | : A gyrator based active inductor circuit diagram [11] .....                                                                                                                                      | 59 |
| <b>Figure 3.30</b> | : Differential bondwire inductor [36] .....                                                                                                                                                       | 60 |
| <b>Figure 3.31</b> | : Parasitic elements of the bonding pad[36] .....                                                                                                                                                 | 61 |
| <b>Figure 3.32</b> | : Low-voltage enhanced LC-tank circuit.....                                                                                                                                                       | 62 |
| <b>Figure 3.33</b> | : Low-voltage enhanced LC-tank bondwire implementation[11] .....                                                                                                                                  | 62 |
| <b>Figure 3.34</b> | : Spiral inductor layout (a) Square (b) Octagonal .....                                                                                                                                           | 63 |
| <b>Figure 3.35</b> | : Equivalent circuit of a spiral inductor [36] .....                                                                                                                                              | 65 |
| <b>Figure 3.36</b> | : Layout of eight-turn square spiral [72] .....                                                                                                                                                   | 66 |
| <b>Figure 3.37</b> | : Layout of polygon spiral inductor [72] .....                                                                                                                                                    | 66 |
| <b>Figure 3.38</b> | : Lumped-element model with values representing the 1.45nH inductor [73].....                                                                                                                     | 67 |
| <b>Figure 3.39</b> | : Comparison of the measured and simulated characteristic of the 1.45nH inductor in Fig.3.38 [73].....                                                                                            | 67 |
| <b>Figure 3.40</b> | : Spiral inductor coil shape (a) standard octagonal (b) symmetrical [13] .....                                                                                                                    | 68 |

|                    |                                                                                                                                                                             |     |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| <b>Figure 3.41</b> | : (a) Equivalent circuit model for symmetrical octagonal coil; (b) Model of a single segment [36].....                                                                      | 69  |
| <b>Figure 4.1</b>  | : Simple Diagram of the VCO [11] .....                                                                                                                                      | 71  |
| <b>Figure 4.2</b>  | : Oscillator Circuit Schematic presented in [12] .....                                                                                                                      | 72  |
| <b>Figure 4.3</b>  | : Simplified schematic of VCO presented in [76] .....                                                                                                                       | 73  |
| <b>Figure 4.4</b>  | : Simplified VCO schematic presented in [78] .....                                                                                                                          | 75  |
| <b>Figure 4.5</b>  | : Schematic of the VCO presented in [60]. .....                                                                                                                             | 76  |
| <b>Figure 4.6</b>  | : Tuning characteristics of the diode varactor VCO, I-MOS varactor VCO, and A-MOS varactor VCO [60].....                                                                    | 77  |
| <b>Figure 4.7</b>  | : Circuit diagram of the 2GHz VCO. Gate voltage of the gated varactor is applied to the node $V_{ctrl}$ . [65].....                                                         | 78  |
| <b>Figure 4.8</b>  | : Frequency tuning characteristic of the VCO. The dotted line shows the resultant tuning curve when $V_{ctrl}$ and $V_{tune}$ are tied form a single tuning node [65] ..... | 79  |
| <b>Figure 4.9</b>  | : Planar LC oscillator circuit schematic [13].....                                                                                                                          | 80  |
| <b>Figure 4.10</b> | : VCO schematic presented in [80] .....                                                                                                                                     | 81  |
| <b>Figure 4.11</b> | : Simplified VCO schematic [83].....                                                                                                                                        | 82  |
| <b>Figure 4.12</b> | : Simplified VCO schematic [].....                                                                                                                                          | 83  |
| <b>Figure 4.13</b> | : Differential pair presented in [35].....                                                                                                                                  | 86  |
| <b>Figure 4.14</b> | : (a) Simple feedback defining $V_P$ (b) Differeantial stage with biasing[35].....                                                                                          | 86  |
| <b>Figure 4.15</b> | : (a) Differantial stage with variable negative resistance load, (b) Half circuit equivalent [35].....                                                                      | 87  |
| <b>Figure 4.16</b> | : Variable-frequency NMOS ring oscillator with voltage-controllable delay between stages presented in [10].....                                                             | 88  |
| <b>Figure 4.17</b> | : Dual ring oscillator with voltage-controllable mixing in feedback path presented in [10].....                                                                             | 88  |
| <b>Figure 4.18</b> | : CMOS Prototype of dual ring oscillator presented in [10] .....                                                                                                            | 89  |
| <b>Figure 4.19</b> | : Differential delay cell presented in [90].....                                                                                                                            | 89  |
| <b>Figure 4.20</b> | : Ring oscillator presented in [91] .....                                                                                                                                   | 90  |
| <b>Figure 4.21</b> | : (a) Delay Cell (b) Bias Circuitry presented in [91].....                                                                                                                  | 91  |
| <b>Figure 4.22</b> | : Differential delay cell presented in [92].....                                                                                                                            | 92  |
| <b>Figure 4.23</b> | : Four-input differentail delay cell presented in [92] .....                                                                                                                | 92  |
| <b>Figure 4.24</b> | : Ring oscillator structure with dual-delay paths presented in [92]....                                                                                                     | 92  |
| <b>Figure 4.25</b> | : (a) Ring oscillator (b) Delay cell presented in [94].....                                                                                                                 | 93  |
| <b>Figure 4.26</b> | : Quadrature network using RC-CR network[21] .....                                                                                                                          | 95  |
| <b>Figure 4.27</b> | : The two-stage sequence asymmetric polyphase filter used as quadrature generator[24] .....                                                                                 | 96  |
| <b>Figure 4.28</b> | : Local Oscillator quadrature generator[22] .....                                                                                                                           | 96  |
| <b>Figure 4.29</b> | : Low-Pass filter and phase shift network[23].....                                                                                                                          | 97  |
| <b>Figure 4.30</b> | : Polyphase Filter presented in [25].....                                                                                                                                   | 97  |
| <b>Figure 4.31</b> | : Frequency dividers as a quadrature generator.....                                                                                                                         | 98  |
| <b>Figure 4.32</b> | : Synchronizing two independent oscillators. ....                                                                                                                           | 98  |
| <b>Figure 4.33</b> | : LC Oscillator presented in [27].....                                                                                                                                      | 99  |
| <b>Figure 4.34</b> | : Oscillators Synchronized in Quadrature [27].....                                                                                                                          | 99  |
| <b>Figure 4.35</b> | : VCO circuit presented in [96] .....                                                                                                                                       | 100 |
| <b>Figure 4.36</b> | : VCO circuit presented in [97] .....                                                                                                                                       | 101 |
| <b>Figure 4.37</b> | : Differantial 4-stage ring oscillator .....                                                                                                                                | 101 |
| <b>Figure 4.38</b> | : Circuit level description of one transmitter channel[98].....                                                                                                             | 102 |
| <b>Figure 4.39</b> | : Two stage ring oscillator with composite load presented in [26] ..                                                                                                        | 102 |

|                    |                                                                                               |     |
|--------------------|-----------------------------------------------------------------------------------------------|-----|
| <b>Figure 5.1</b>  | : Injection locking of two oscillators.....                                                   | 104 |
| <b>Figure 5.2</b>  | : Schematic of the LC oscillator .....                                                        | 105 |
| <b>Figure 5.3</b>  | : MOS Varactor .....                                                                          | 107 |
| <b>Figure 5.4</b>  | : Digital Tuning Circuit.....                                                                 | 107 |
| <b>Figure 5.5</b>  | : Nine-Element Model of the spiral inductor .....                                             | 109 |
| <b>Figure 5.6</b>  | : Layout of the symmetrical inductor .....                                                    | 109 |
| <b>Figure 5.7</b>  | : Buffer circuit schematic .....                                                              | 110 |
| <b>Figure 5.8</b>  | : Biasing circuit .....                                                                       | 111 |
| <b>Figure 5.9</b>  | : Discrete quadrature LC oscillator circuit schematic .....                                   | 112 |
| <b>Figure 5.10</b> | : Simulation schematic of the LC oscillator .....                                             | 114 |
| <b>Figure 5.11</b> | : Quadrature Outputs of the oscillator .....                                                  | 116 |
| <b>Figure 5.12</b> | : Phase difference of outputs .....                                                           | 116 |
| <b>Figure 5.13</b> | : Amplitude Difference of Quadrature Outputs.....                                             | 117 |
| <b>Figure 5.14</b> | : Tuning Range of the LC Quadrature oscillator .....                                          | 118 |
| <b>Figure 5.15</b> | : Phase Noise Results (HP-ADS) .....                                                          | 122 |
| <b>Figure 5.16</b> | : Layout of the test chip of the quadrature LC oscillator .....                               | 123 |
| <b>Figure 5.17</b> | : Top level schematic of the quadrature ring oscillator .....                                 | 124 |
| <b>Figure 5.18</b> | : Differential delay Cell.....                                                                | 126 |
| <b>Figure 5.19</b> | : Bias Circuit.....                                                                           | 127 |
| <b>Figure 5.20</b> | : NMOS Bias Circuit.....                                                                      | 127 |
| <b>Figure 5.21</b> | : The schemataic of the op-amp used in the NMOS basing circuit....                            | 128 |
| <b>Figure 5.22</b> | : PMOS bias circuit .....                                                                     | 129 |
| <b>Figure 5.23</b> | : Op-amp circuit used in the PMOS biasing circuit .....                                       | 130 |
| <b>Figure 5.24</b> | : Bias circuit for NMOS biasing and PMOS biasing circuits.....                                | 131 |
| <b>Figure 5.25</b> | : Buffer circuit for ring oscillator .....                                                    | 131 |
| <b>Figure 5.26</b> | : Simulation schematic of the delay cell.....                                                 | 132 |
| <b>Figure 5.27</b> | : Transient response of the ring oscillator .....                                             | 134 |
| <b>Figure 5.28</b> | : SST Results of ring oscillator .....                                                        | 134 |
| <b>Figure 5.29</b> | : Amplitude difference of the outputs .....                                                   | 135 |
| <b>Figure 5.30</b> | : Tuning Range of ring oscillator .....                                                       | 135 |
| <b>Figure 5.31</b> | : Phase noise of Ring Oscillator with HP-ADS.....                                             | 139 |
| <b>Figure 5.32</b> | : Phase Noise results of eldorf.....                                                          | 139 |
| <b>Figure A.1</b>  | : LC tank circuit.....                                                                        | 158 |
| <b>Figure A.2</b>  | : Quality Factors for different tank circuits [36]. .....                                     | 159 |
| <b>Figure A.3</b>  | : LC tank (a) ideal (b) realistic .....                                                       | 160 |
| <b>Figure A.4</b>  | : Conversion of a series combination to parallel combination<br>(a) Series (b) parallel. .... | 160 |
| <b>Figure A.5</b>  | : Equivalent (a) series and (b) parallel RC circuits .....                                    | 161 |
| <b>Figure A.6</b>  | : Conversion of a tank to three parallel components [21] .....                                | 162 |
| <b>Figure B.1</b>  | : Phase noise results of an oscillator.....                                                   | 164 |
| <b>Figure B.2</b>  | : The method showing to find the valid results for phase noise of<br>an oscillator. ....      | 164 |
| <b>Figure C.1</b>  | : Top level schematic of the quadrature LC VCO test chip .....                                | 166 |
| <b>Figure C.2</b>  | : The block schematic of the quadrature LC VCO with bias and<br>buffer circuits .....         | 167 |
| <b>Figure C.3</b>  | : Block schematic of the two cross-coupled LC VCO .....                                       | 168 |
| <b>Figure C.4</b>  | : The schematic of one of the LC VCO of the quadrature LC VCO                                 | 169 |
| <b>Figure C.5</b>  | : Schematic of the buffers of the quadrature LC VCO.....                                      | 170 |
| <b>Figure C.6</b>  | : The schematic of the biasing circuit of the quadrature LC VCO...                            | 170 |

|                    |                                                                                                         |     |
|--------------------|---------------------------------------------------------------------------------------------------------|-----|
| <b>Figure C.7</b>  | : The schematic of the biasing circuit of the buffer of the quadrature LC VCO .....                     | 171 |
| <b>Figure C.8</b>  | : Top level block schematic of the quadrature ring VCO.....                                             | 172 |
| <b>Figure C.9</b>  | : Block schematic of the quadrature ring VCO with output capacitors.....                                | 173 |
| <b>Figure C.10</b> | : The block schematic of the quadrature ring VCO with biasing and buffer circuits .....                 | 174 |
| <b>Figure C.11</b> | : The schematic of one of the delay cell of quadrature ring VCO....                                     | 175 |
| <b>Figure C.12</b> | : The schematic of the one of the buffer circuit of the quadrature ring VCO .....                       | 176 |
| <b>Figure C.13</b> | : The schematic of the biasing of the PMOS and NMOS biasing circuits of the quadrature ring VCO.....    | 176 |
| <b>Figure C.14</b> | : The schematic of the NMOS biasing circuit of the quadrature ring VCO .....                            | 177 |
| <b>Figure C.15</b> | : The schematic of op-amp circuit used in the NMOS basing circuit of the quadrature ring VCO.....       | 177 |
| <b>Figure C.16</b> | : The schematic of the PMOS biasing circuit of the ring VCO.....                                        | 178 |
| <b>Figure C.17</b> | : The schematic of the op-amp circuit used in the PMOS biasing circuit of the quadrature ring VCO ..... | 178 |



## LIST OF SYMBOLS

|                     |                                       |
|---------------------|---------------------------------------|
| $\omega_0, f_{osc}$ | : Oscillation frequency               |
| $\beta$             | : Gain of a system                    |
| $g_m$               | : Transconductance                    |
| $\omega_R$          | : Resonance frequency                 |
| $V_D$               | : Diode voltage                       |
| $\tau_{inv}$        | : Delay of inverter                   |
| $V_{DD}$            | : Supply voltage                      |
| $K_{VCO}$           | : Gain of the VCO                     |
| $V_{cont}$          | : Control (tune) voltage.             |
| $f_m$               | : Offset frequency                    |
| $k$                 | : Boltzman's constant                 |
| $\Delta\omega$      | : Frequency offset from the carrier   |
| $\eta$              | : Proportionality constant            |
| $C_{var}$           | : Variable capacitor                  |
| $\phi_B$            | : Built-in potential of the junction, |
| $t_{ox}$            | : Oxide thickness,                    |
| $W$                 | : Width of the transistor             |
| $L$                 | : Length of the transistor            |
| $V_{FB}$            | : Flatband voltage                    |
| $V_T$               | : Threshold voltage                   |

## 5-6GHz ARALIĞINDA, SiGe BiCMOS PROSES KULLANILARAK 90° FAZ FARKLI İŞARET ÜRETİMİ

### ÖZET

Bu yüzyılın son on yılı, haberleşme endüstrisinde büyük bir büyüme görmüştür. İnsanlar telsiz haberleşme araçlarını kullanarak sürekli bağlantıda olmak istemektedirler. Büyüyen teknolojiyle, sistemlerin maliyeti de çok önemli hale gelmiştir ki RF tasarım ayırık tasarımdan tümleşik devre çözümlerine kaymıştır. Avrupa yüksek performanslı radyo yerel ağ (HIPERLAN) sistemi gibi 5GHz ISM bandı kullanılarak bilgi iletim hızlarının artırılmasında dünyaca yaygın bir ilgi vardır. Hatta HIPERLAN2 sistemi 54Mb/s' lara ulaşan çok yüksek iletim hızına sahiptir.

Bir haberleşme alıcı-vericisi değişik bloklar içerir fakat gerilim kontrollü osilatör (VCO), alıcı-vericinin kritik bir alt bloğudur. VCO'lar birçok yenilikler sunmasının yanında, kabul edilebilir faz gürültüsü ve ayar aralığı için, mikrodalga frekanslarında düşük güçlü aktif elemanlara ek olarak, yüksek kalitede düşük parazitik değerlere sahip pasif elemanlara ihtiyaç duyar. VCO'ların önemli karakteristikleri, çalışma frekansı, sıcaklıkla frekans kararlılığı, frekans karakteristiğine karşı gerilimin lineerliği, ayar aralığı, faz gürültüsü ve üretim maliyetini içerir.

QPSK, GMSK, OFDM gibi dijital modülasyonu kullanan alıcı-verici sistemlerinde, 90° faz farklı (quadrature) işaret üretimi çok kritik bir noktadır. HIPERLAN2 sistemi de dijital modülasyonu kullanan bu sistemlerden biridir. Bazı alıcı-vericilerde, tüm sistem performansı için, 90° faz farklı işaret hatası sınırı çok sıkıdır, diğer bir deyişle çok az hata kabul edilebilir. Bu da faz gürültüsü performansı ve ya güç tüketimi gibi kendi karakteristikleri ile birlikte VCO'nun, tasarımını çok güçleştirir. Bu tez 0.35µm SiGe (Silikon germanyum) BiCMOS prosesi ile HIPERLAN2 sisteminin 90° faz farklı lokal osilatörü (LO) işareti üretimi için tasarlanan iki değişik VCO tasarımını kapsar.

Temel bilgi olarak, genel osilasyon teorisi ve değişik tipte temel yüksek frekans osilatörleri sunulmuştur. Kristal osilatörler, temel LC osilatörler, Wien-Bridge osilatörü, Colpitts osilatörü, Hartley osilatörü, rölaksasyon osilatörler ve halka osilatörler, RF osilatörlerinin temelleri olduğundan 2. Bölümün konusu olmuşlardır.

Haberleşme kanal aralıklarının çok küçük olmasından dolayı, frekans sentezleyeceğinin çıkış işareti çok saf bir sinüs olmalıdır. Çevrim bant genişliğinden büyük olan ofset frekanslarında, faz gürültüsü esas olarak VCO tarafından belirlenir. Burada, osilatörlerdeki faz gürültüsünün temel teorisi sunulmuştur. Buradaki tasarımında kullanılan halka ve LC VCO'ların faz gürültü modelleri ve bu tür osilatörlerin değişik topolojilerdeki faz gürültüsü performansları tartışılmıştır. LC VCO tasarımında, devrenin faz gürültüsü ve ayar bölgesi performansı üzerinde özellikle etkili olan iki eleman vardır. Bunlar varaktör ve endüktanstır ve bunlar için bir literatür araştırılması yapılmıştır. Değişik tipte varaktörler verilmiş ve VCO'lar

üzerindeki performans etkileri karşılaştırılmıştır. Bunlar, diyot varaktörler, evirtim modlu MOS varaktör, akümülayon MOS varaktör ve geçirilmiş MOS varaktörlerdir. Akümülayon MOS varaktörlerin, şimdilerde diyot varaktörlerinin yerini aldığı görülmüştür. Çünkü, akümülayon MOS varaktörle tasarlanan VCO'ların, diyot varaktörle tasarlanmış VCO'lardan, daha az güç harcadığı, daha geniş ayar aralığının bulunduğu ve daha iyi bir faz gürültüsü performansı göstermektedir. Endüktanslar VCO'nun faz gürültüsü performansında çok etkilidir. Endüktansların değişik gerçekleştirilmesi olan, aktif endüktanslar, bağ telli ve spiral endüktanslar avantaj ve dezavantajlarıyla açıklanmıştır. Faz gürültüsü, varaktör ve endüktansla ilgili bu çalışmalar Bölüm 3'te sunulmuştur.

90'lar dan bugüne kadar sunulmuş olan değişik tipte VCO'lar Bölüm 4'te sunulmuştur. Bu çalışma LC ve halka osilatörler üzerine bir araştırmayı kapsar. LC VCO'lar okuyucunun karşılaştırması açısından, özellikle farklı varaktör, endüktans ve kuvvetlendirici devreleri kullananlardan seçilmiştir. LC VCO'lar üzerindeki çalışma daha çok negatif- $G_m$  osilatörleri üzerinedir. Halka osilatörler için değişik ayar metotları açıklanmıştır. Her iki osilatör çeşidi olan halka ve LC osilatörler, kendi kategorileri içinde faz gürültüsü performansı, ayar aralığı, güç tüketimi ve kapladıkları alan maliyeti açısından karşılaştırılmışlardır. Dört çeşit kuadratur LO işareti üretim yöntemleri de Bölüm 4'te sunulmuştur. Bunlar RC-CR ağı (polifaz filtre), frekans bölme, iki çapraz bağlı VCO ve 90° faz farklı halka osilatördür ve örneklerle açıklanmıştır. VCO ve RC-CR ağı kombinasyonu takip eden tampon veya sınırlandırıcılar kullanılan metot, çok güç tüketir, çok fazla kırmık alanı kaplar ve kuadratur işaret performansı serimdeki uygunsuz eşleşmeye çok bağlıdır. HIPERLAN2 gibi yüksek frekans uygulamalarında iki kat frekansta VCO tasarımı mümkün değildir. Bu nedenle, son iki metot olan, iki çapraz bağlı VCO ve 90° faz farklı halka VCO bizim tasarımıımız için mümkündür.

Bölüm 5'te, HIPERLAN2 projesi için 90° faz farklı LC ve halka osilatörü tasarımı sunulmuştur. Her iki VCO da 0.35µm SiGe BiCMOS prosesi kullanılarak tasarlanmıştır. Devrelerin çalışma prensipleri, tasarım şemaları ile birlikte açıklanmıştır. İlk tasarım birbirinin aynı iki çapraz bağlı LC VCO tasarımını içerir. Her iki VCO da diferansiyel çapraz bağlı PMOS ve NMOS transistorlar ve simetrik bir endüktans ile gerçekleşmiştir. Daha iyi bir ayar aralığı için, diyot varaktör yerine MOS varaktör tercih edilmiştir. Tipik, karakterizasyon ve Monte Carlo simülasyonları her iki VCO için de gerçekleşmiştir. İkinci tasarım, iki gecikme hücresiyle tasarlanan halka VCO'dur. Gecikme hücreleri diferansiyel BiCMOS çiftidir. Hem kuyruk akımı hem de gecikme hücrelerinin PMOS transistorlerinin geçit gerilimi, çıkış genlik salınımindaki değişimini azaltmak için aynı anda bir analog gerilim ile kontrol edilmektedir. Her iki VCO'nun sonuç ve performansları verilip karşılaştırılmıştır.

LC VCO'nun faz gürültüsü performansı halka VCO'dan daha iyidir. Halka osilatörün ayar aralığı LC VCO'dan daha iyidir. Kuadratur faz hatası her iki osilatörde de hemen hemen aynıdır. 5-6GHz aralığının kullanıldığı sistemlerde, faz gürültüsü performansının önemli ve sistem sınırlarının sıkı olduğu durumlarda, yüksek maliyetten ödün verilerek LC VCO seçilmelidir. Ve kırmığın alan maliyetinin önemli olduğu durumlarda ise, faz gürültüsünden feragat edilerek halka VCO seçilmelidir.

## QUADRATURE SIGNAL GENERATION IN 5-6 GHz RANGE USING SiGe BiCMOS PROCESS

### SUMMARY

The last decade of this century has seen an explosive growth in the communications industry. People want to be connected all the time using wireless communication devices. With the growing technology, the cost of the systems has also become very important that RF design is shifted from discrete design to IC solutions. There is worldwide interest in increasing data transmission rates by using the 5GHz ISM band like the European high-performance radio LAN (HIPERLAN) system where HIPERLAN2 has a very high transmission rate up to 54 Mb/s.

A communication transceiver consists of different blocks, but the VCO is a critical sub-block of the transceiver. They present many challenges to any technology since they require low parasitic high quality passive components for acceptable tuning range and phase noise levels, in addition to the need for low power active devices at microwave frequencies. Important characteristics of VCO's include frequency operation, frequency stability with temperature, linearity of the voltage to frequency characteristic, tuning range, phase noise and cost of fabrication.

Quadrature signal generation is a critical point of the transceiver systems, which use digital modulations such as QPSK, GMSK, OFDM etc. HIPERLAN2 system is one of them, which uses digital modulation. Some of the transceivers have very strict spec for the quadrature signal error for the overall system performance. This makes the design of the VCO more difficult together with its own characteristics like its phase noise performance or power consumption etc. This thesis covers the design of two different VCOs for quadrature LO signal generation for HIPERLAN2 system with 0.35 $\mu$ m SiGe BiCMOS process.

As a basic knowledge, the general theory of oscillation and different type of basic RF oscillators have been presented. Crystal oscillators, basic LC oscillators, Wien-Bridge oscillator, Colpitts oscillator, Hartley oscillator, relaxation oscillators and ring oscillators have been a subject of the 2<sup>nd</sup> Chapter as they are the basics of the RF oscillators.

Due to very small communication channel spacing, the output signal of the frequency synthesizer must be a very pure sinusoid. At frequency offsets larger than the loop bandwidth, the phase noise is mainly determined by the VCO. Here, the general theory of phase noise in oscillators has been presented. The phase noise models for ring and LC VCOs and phase noise performance of these kinds of oscillators have been discussed as these types of oscillators are used in this design. In the design of LC VCOs there are two devices which are especially effective on the phase noise and tuning range performance of the circuit. These are the varactors and inductors and a literature research has been done for them. Different types of varactors are given and their performance effects on the VCOs are compared. These varactors are diode varactor, inversion mode MOS varactor, accumulation MOS varactor and gated

MOS varactors. It is seen that nowadays the accumulation MOS varactor is taking the place of diode varactor because the LC VCOs designed with accumulation MOS varactor consumes less power, has a larger tuning range and a better phase noise performance than the ones designed with diode varactors. Inductors are very effective on the phase noise performance of the VCO. Different implementations of inductors; active inductors, bondwire and spiral inductors are explained with their advantages and disadvantages. All the research on phase noise, varactors and inductors have been presented in Chapter 3.

Different type of VCOs, designed from 90s until today has been presented in Chapter 4. The work covers a research on LC and ring VCOs with their operation principles. The LC VCOs are especially chosen from their different usage of varactor and inductors and amplifier circuits, so that the reader can compare them. The work for LC VCO is mostly on negative- $G_m$  oscillators. Different tuning methods has been explained for the ring VCOs. Both ring and LC VCOs are compared within their own category for their phase noise performance, tuning range, power consumption and cost of area. Different methods to generate quadrature LO signals have been also presented in Chapter 4. These are RC-CR network (polyphase filter), frequency division, two cross-coupled VCO and quadrature ring oscillator, are explained with examples. Using RC-CR network or polyphase filter after the VCO, following with buffers or limiters, consume too much power, costs big chip area and quadrature signal performance is very dependent to the mismatch in the layout. In applications of high frequency like HIPERLAN2 it is not possible to design a double frequency VCO. Therefore, the last two methods, two cross-coupled VCO and the quadrature ring oscillator are feasible for our design.

In Chapter 5, the design of the quadrature LC and quadrature ring VCO for HIPERLAN2 project has been presented. Both of the VCOs has been designed with 0.35 $\mu$ m SiGe BiCMOS process. The operating principles of the circuits have been explained with their design schematics. First design consists of two identical cross-coupled LC VCOs. Each VCO has been realized with coupled differential PMOS and NMOS transistors with a symmetrical coil. For a better tuning range MOS varactors have been preferred instead of diode varactors. The typical, characterization and Monte Carlo simulations have been performed for the VCOs. The second design is the quadrature ring oscillator with two delay cells. The delay cells are designed with a differential BiCMOS pair. Both the tail current and the gate voltage of the PMOS transistors of the delay cell are controlled with one tuning voltage in order to decrease the amplitude swing variation. The results and the performance of both VCOs have been given and compared.

The phase noise performance of the LC VCO is better than the ring VCO. The ring VCO has a better tuning range than LC VCO. The quadrature phase mismatch results are exactly the same. For other systems where the 5-6GHz range is used, if the phase noise performance is important and strict, the LC VCO should be preferred with high cost. And if chip area cost is important ring VCO should be preferred suffering from phase noise.

## 1. INTRODUCTION

Wireless technology came to existence when in 1901 Guglielmo Marconi successfully transmitted radio signals across Atlantic Ocean. Besides, after the invention of the transistors in 1948, there has been an explosive growth of telecommunication systems. Oscillators are fundamental building blocks used in radio equipment of all kinds. They are integral part of many electronic systems. Applications range from clock recovery generation in microprocessors to carrier synthesis in cellular telephones requiring vastly different oscillator topology and performance parameters [1].

The first stage in almost all-simple transmitters is an oscillator. In a similar manner, the various oscillators used in a superheterodyne communications receiver determine the frequency is tuned to. The simplest transmitter is a crystal-controlled oscillator. The popular crystal oscillators are Pierce, Colpitts, Clapp, harmonic and overtone crystal oscillators [2].

Variable-frequency crystal oscillators (VXO) are useful in place of conventional crystal oscillator when it is necessary to shift the crystal frequency in order to transmit signal at different frequencies. In these oscillators the operating frequency can be shifted slightly by means of trimmer capacitors [2,3].

Variable-frequency oscillators (VFO) are similar to VXOs but the essential difference is that greater frequency coverage is possible and no crystals are used. Therefore a VFO provides a necessary flexibility which is not possible with VXOs and crystal oscillators. A VFO permits greater effectiveness during low power work, especially if crowded band conditions prevail. Frequency stability is more difficult to realize when a VFO is used, to preference to a crystal oscillator. Improved performance is obtained if the VFO is mixed with crystal oscillators, which inherently have good stability [2]. The same configuration is used in the present day communication receivers and called a superheterodyne receiver. The real solution for solving the stability problem is the frequency synthesizer. Although there are many

types of frequency synthesizers, the phase lock loop (PLL) type is probably the most widely used approach in the communication receivers [4]. In modern wireless telecommunications systems, channels are placed very closely together for the efficient use of the frequency spectrum. The RF front end of a wireless transceiver should have the ability to detect a wanted signal while very large interfering signals are present in adjacent channels. In particular the characteristic of a local oscillator (LO) or frequency synthesizer is very important in designing such systems [5].

The PLL system includes a reference oscillator, phase detector, frequency divider and voltage controlled oscillator (VCO). The VCO is merely a VFO with usual mechanically tuned capacitor replaced with a varactor diode. A VCO is one of the key elements in a frequency synthesizer and the most critically determines the performance of a frequency synthesizer. They present many challenges to any technology since they require low parasitic high quality passive components for acceptable tuning range and phase noise levels, in addition to the need for low power active devices at microwave frequencies. Important characteristics of VCO's include frequency operation, frequency stability with temperature, linearity of the voltage to frequency characteristic, tuning range, phase noise [6] and cost of fabrication. High frequency VCOs have been realized as relaxation [7,8], ring oscillators [9,10] and LC oscillators. The design of monolithic LC VCOs within standards has been objective of several recent projects like DCS1800 (DECT cordless telephones)[11-14], GSM900 (European GSM cellular telephones) [15,16] and WLAN (Wireless LAN 2.4/5.8GHz) [17-20].

Modulation is an essential function in communication system. The systems that are using digital modulations like QPSK or GMSK generate both in-phase (I) and quadrature (Q) components of the signal. In receiver architectures like heterodyne receivers, homodyne receivers, image reject receivers and digital IF receivers, for frequency and phase modulated signals, the downconversion must provide quadrature outputs so as to avoid loss of information [21]. This is because the two sides of FM or QPSK spectra carry different information and must be separated into quadrature phases. In today's RF systems, homodyne or zero-IF or low-IF receivers are preferred mostly because they offer flexibility and low cost through high integration. As mentioned above in these transceivers, quadrature signals are needed

for modulation, and it is important to offer quadrature signal generation at minimal power consumption. There are different ways to produce quadrature signals. Traditionally I-Q outputs are generated either by using a RC-CR phase shifter. Different types of RC-CR phase shifters are used in [22-25]. When RC-CR networks are used the mismatches between resistors and capacitors cause phase and amplitude error for the quadrature outputs. The output buffers used after the phase shifter consume a lot of power [6] and the total design needs a lot of chip area. Another way to generate quadrature signals is the use of VCO at double frequency followed by master-slave flipflops. The VCO designed in double frequency will consume less power but the master-slave flip-flops have to be designed in double frequency, therefore they consume too much power depending on the technology. Third way is the use of ring oscillators with even number of delay cell [26]. Quadrature ring oscillators are preferred especially in clock recovery circuit. We can obtain a better tuning range when compared with LC VCOs. Also it has costless chip area. Another way is the use of two cross-coupled VCO [27]. This structure costs double VCO area. But if the VCO core is well designed it consumes less power than the output buffers or limiters, which are used with RC-CR network. The other advantage of this structure is that, it provides a very high voltage swing, which eases the design of the prescaler and mixer circuits connected to VCO [28].

As the need of VCOs grow, there is much work on the technologies to increase the performance of the circuits. SiGe heterojunction bipolar transistor (HBT) provides significant performance advantages in many mixed signal and microwave applications [29-31]. This technology is an attractive candidate in the emerging area of wireless communication since it has the potential to exceed the performance of conventional silicon technology to a level where it can cope with GaAs, yet provide the cost advantage and manufacturing volume capabilities of silicon. An industrial 0.35 $\mu\text{m}$  SiGe BiCMOS technology for 5GHz home digital networks have been recently presented [32] achieving transistors having  $f_T$  value of 80GHz. This extends the advantages of RF BiCMOS technology towards low-noise high speed and low power applications. Besides different technologies, there is an ever-decreasing line width of CMOS processing technology has gone from around 10 $\mu\text{m}$  in 1970, over 1 $\mu\text{m}$  in the late 1980s, to a present-day value of 0.13 $\mu\text{m}$  in mass production. This helps to reduce the power consumption, overall weight and the volume.

This work covers a research and design on RF oscillators and VCOs. The basics of VCO design like performance parameters, varactor and inductor design, phase noise calculation are given with examples. Different types of LC and ring oscillators, which have been designed in the last decades, are explained with their operation principle and the VCOs are compared with each other. The methods of quadrature signal generation for transceivers are discussed and the advantages and disadvantages of the methods are given. A feasibility of VCOs is done for HIPERLAN2 wireless system from the ETSI specs [33]. Then we present two quadrature VCOs, which are quadrature LC and ring VCOs. They are both designed to operate between 5-6GHz band for HIPERLAN2 wireless system satisfying the specs. 0.35 $\mu$ m SiGe BiCMOS process has been used. The quadrature LC VCO is designed with two cross-coupled planar LC oscillators. All the simulations to test the important performance parameters of the VCO are realized. The layout of the VCO is also performed. The quadrature ring VCO is designed with two delay cells. All the simulations are also performed for this VCO. A comparison between the two VCOs is given within the simulation results.

This thesis is organized in six chapters. In chapter 2, a brief description of oscillators and oscillation theory is given. Different types of RF oscillators are also discussed, including Wien-Bridge Oscillator, relaxation oscillators, crystal oscillators, Hartley oscillator, Colpitts oscillator, ring oscillators and LC oscillators. Chapter 3 begins with the definition of VCO and basic terms of VCO and continues with phase noise of the VCOs. The phase noise models for ring and LC VCOs and phase noise performance of these kinds of oscillators are discussed. In the design of LC VCOs there are two devices which are especially effective on the phase noise and tuning range performance of the circuit. These are the varactors and inductors. Different types of varactors, which are diode varactors, inversion mode MOS varactor, accumulation MOS varactor and gated MOS varactors are given and their performance effects on the VCOs are compared. Different implementations of inductors; active inductors, bondwire and spiral inductors are explained with their advantages and disadvantages. In the following chapter, Chapter 4, ring and LC VCOs, which are presented in last ten years, are given with their operating principle. Both ring and LC VCOs are compared within their own category. The LC VCOs are especially negative- $G_m$  type having the varactor and inductor types mentioned in

Chapter 3. Different tuning methods are explained for the ring VCOs. In the last section of the chapter four different methods of quadrature LO signal generation for the VCOs that are RC-CR network, frequency division, cross-coupled VCO and ring oscillator, are explained with examples. In Chapter 5, the design of the quadrature LC and quadrature ring VCO for HIPERLAN2 project is presented. The operating principles of the circuits are explained with their design schematics. The typical, characterization and Monte Carlo simulations are performed for the VCOs. The results and the performance of both VCOs are given and compared. Chapter 6 gives conclusion for each chapter and explain the future challenges for the designed VCOs.



## 2. BASICS IN RF SIGNAL GENERATION

This chapter gives an overview about oscillation system and oscillators. It begins with the definition and the criteria for oscillation. The basic oscillator types used in RF applications are given. These are Wien-Bridge oscillator, crystal oscillator, relaxation oscillator, ring oscillators, and basic LC oscillators. Oscillation principles of these circuits are explained with examples. Negative- $G_m$  oscillator topology is explained for LC oscillators.

### 2.1 General Considerations

In the design of electronic systems the need for signals having prescribed standard waveforms frequently arises. The most common is sinusoidal waveforms. Systems in which standard signals are required include: computer and control systems where clock pulses are needed for among the other things timing; communication systems where signals of a variety of waveforms are utilized as information carriers; test and measurement systems where signals, again of a variety of waveforms are employed for testing and characterizing electronic devices and circuits [34].

Oscillators are an integral part of many electronic systems. Applications range from clock generation in microprocessors to carrier synthesis in cellular telephones, requiring vastly different oscillator topologies and performance parameters.

There are two distinctly different approaches for the generation of sinusoids. The first approach employs a positive feedback loop consisting of an amplifier or a LC frequency selective network. The amplitude of generated sine waves is limited or set using a nonlinear mechanism, implemented either with a separate circuit or using nonlinearities of the amplifying device itself. In spite of this, these circuits, which generate sine waves utilizing resonance, phenomena are known as linear oscillators.

This is the second approach. In these circuits a sine wave is obtained by appropriately shaping a triangular form. Techniques have developed by which the

design of sinusoidal oscillators can be performed in two steps. The first step is a linear one and frequency-domain methods of feedback circuit analysis can be employed. Subsequently, a nonlinear mechanism for amplitude control can be provided.

## 2.2 Definition of Oscillation

An oscillator generates a periodic output usually in the form of voltage. As such the circuit has no input while sustaining the output indefinitely. The circuit must entail self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal.

Most RF oscillators can be viewed as feedback circuits. A simple linear feedback system is shown in Figure 2.1. The transfer function of the circuit is;

$$\frac{Y(s)}{X(s)} = \frac{A(s)}{1 - A(s)} \quad (2.1)$$

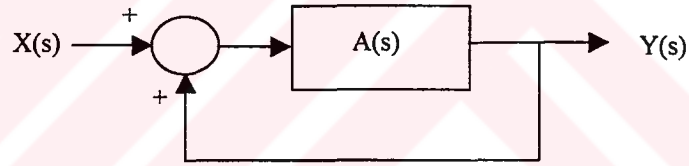


**Figure 2.1** Unity feedback oscillatory system [21]

For steady oscillation two conditions must be simultaneously met at the frequency  $\omega_0$ : The loop gain  $|A(j\omega_0)|$  must be equal to unity and the total phase shift around the loop  $\angle A(j\omega_0)$ , must be equal to zero. The above conditions imply that any feedback system can oscillate if this loop gain and phase shift, are chosen properly. Ring oscillators and phase shifters are example of this. But in most RF oscillators, a frequency selective network is included in the loop so as to stabilize the frequency. This is illustrated in Figure 2.2. The frequency-selective network is also called a resonator [34].

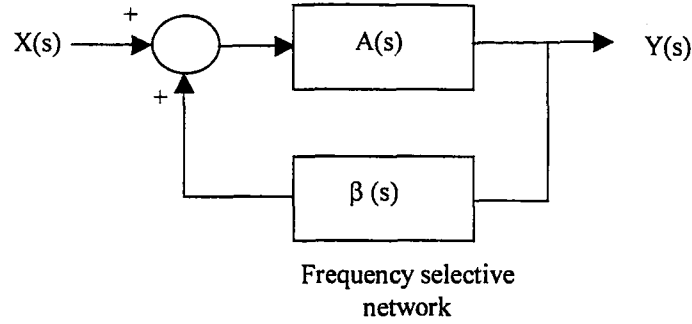


**Figure 2.2** Feedback system with frequency selective network [34]

We will now explain the oscillation criteria with this structure detailed. Although in an actual oscillator circuit, no input signal will be given, the input signal is put here to help to explain the principle better. The transfer function of the circuit;

$$\frac{Y(s)}{X(s)} = \frac{A(s)}{1 - A(s)\beta(s)} \quad (2.2)$$

If at a specific frequency  $f_0$  the loop gain  $A\beta$  is equal to unity, the gain will be infinite. That is, at this frequency the circuit will have finite output for zero input signals. Such a circuit is defined as oscillator. To provide sinusoidal oscillations of frequency  $\omega_0$ , the condition for the feedback loop of Figure 2.2 is

$$L(j\omega_0) \equiv A(j\omega_0)\beta(j\omega_0) = 1 \quad (2.3)$$

That means at  $\omega_0$ , the phase of the loop gain should be zero and the magnitude of the loop gain should be unity. This is known as the Barkhausen criteria. This oscillation criterion should be satisfied at one frequency only (that is  $\omega_0$ ), for the circuit to oscillate at one frequency; otherwise the resulting waveform will not be a simple sinusoid [34]. In some cases Barkhausen criteria is necessary but not sufficient. As an example, if the phase shift around the loop is equal to  $360^\circ$  at zero frequency and the loop gain is sufficient, the circuit latches up rather than oscillate.

The oscillation condition, the Barkhausen criterion that is discussed above guarantees sustained oscillations in a mathematical sense. But it is known that the parameters of a physical system can not be constant for any length of time. Suppose the conditions  $A\beta=1$  at  $\omega=\omega_0$  is satisfied; then temperature changes in the circuit and

$A\beta$  becomes slightly less than unity. So oscillation will cease in this case. Conversely if  $A\beta$  exceeds unity, oscillation will grow in amplitude. So we need a mechanism for forcing  $A\beta$  to remain equal to unity at the desired value of output amplitude. This mechanism is called automatic level control (ALC).

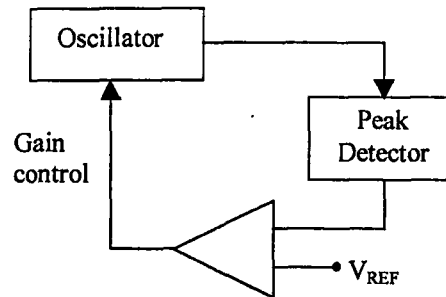


**Figure 2.3** Automatic level control system [21]

This technique is shown in Figure 2.3, which measures the amplitude by means of a peak detector and compares the result by a reference and adjusts the gain of the oscillator, by a negative feedback. Thus at the start up, the amplitude is small and the gain is high, and in the steady state, the amplitude is equal to  $V_{REF}$ . The use of ALC allows the oscillation to remain linear if  $V_{REF}$  is chosen properly providing a sinusoidal output with low distortion. But in RF application this technique doesn't have a wide usage because of the complexity of the circuit and the possibility of the additional noise.

## 2.3 Oscillator Types

In this section, we will explain different types of oscillators used in RF applications. These are Wien-Bridge oscillator, crystal oscillator, relaxation oscillator, ring oscillators, and LC oscillators. The basic operation principle of the oscillators is explained.

### 2.3.1 Wien-Bridge Oscillator

One of the simplest oscillator circuits is based on Wien-Bridge as shown in Figure 2.4. The active element in the circuit is an operational amplifier circuit connected in

the nonconverting configuration. It has a closed loop gain of  $(1 + R_2/R_1)$ . RC network is connected in the feedback path of this positive-gain amplifier [34].

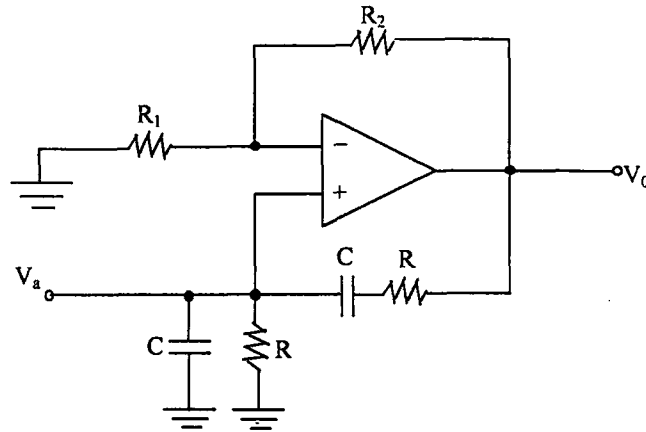


**Figure 2.4** Wien Bridge oscillator [34]

The loop gain can be written as

$$L(s) = \frac{1 + R_2/R_1}{3 + sCR + 1/sCR} \quad (2.4)$$

After converting the equation to  $j\omega$  domain,

$$L(j\omega) = \frac{1 + R_2/R_1}{3 + j(\omega CR - 1/\omega CR)} \quad (2.5)$$

When the phase will be zero, that is, the loop gain will be a real number at one frequency, and that is the oscillation frequency;

$$\omega_0 = 1/CR \quad (2.6)$$

At this frequency to obtain sustained oscillations, the magnitude of the loop gain has to be unity. This can be achieved according to equation (2.5) by selecting

$$R_2/R_1 = 2 \quad (2.7)$$

To ensure the oscillations will start,  $R_2/R_1$  has to be chosen slightly greater than 2. The amplitude of oscillation can be determined and stabilized by using a nonlinear control network.

### 2.3.2 Basic LC Oscillator Topologies

An LC oscillator can be realized with one bipolar transistor in the signal path, including a LC tank at the collector with the feedback signal applied to the base or emitter (the same idea applies to FET implementations as well). So the feedback model of Figure 2.1 is followed. The application is shown in Figure 2.5 having a tank circuit consisting of an inductor and a capacitor parallel. Since at resonance the impedance of the tank is real, the phase difference between its current and voltage is zero. Thus, to achieve a total phase equal to zero, the feedback signal must return to emitter of the transistor. This is the basic idea in a number of oscillator topologies. The same idea can be applied with FETs also [21].

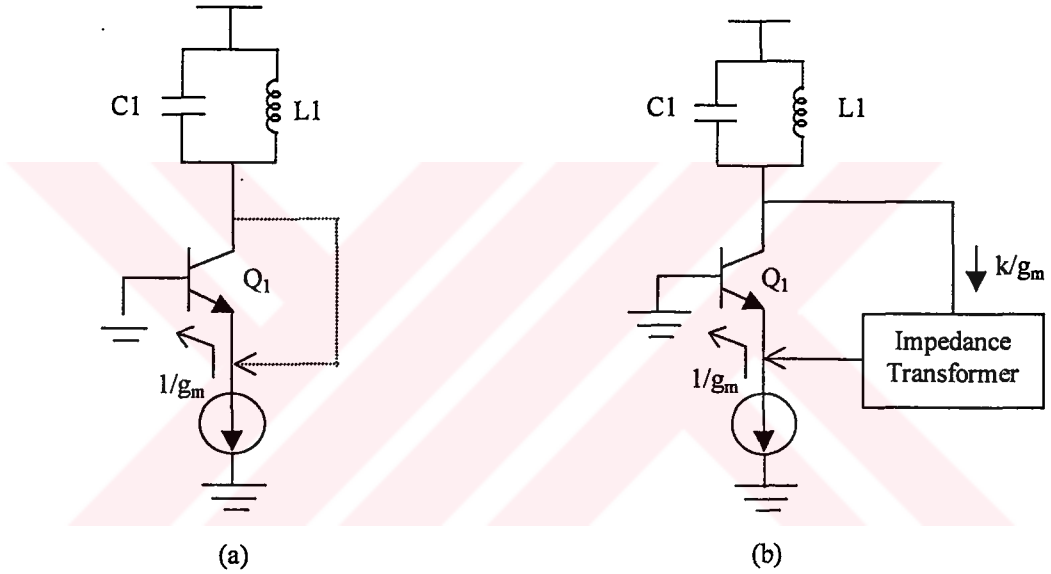


**Figure 2.5** (a) Feedback from collector to emitter (b) Insertion of an impedance transformer [21].

If the collector voltage is directly applied to the emitter, the resistive loading ( $1/g_m$ ) seen at the emitter terminal can reduce the Q of the tank. Consequently the loop gain drops below unity preventing oscillation. There are ways to solve this problem. An impedance transformer can transform the emitter impedance to a higher value before it appears parallel with the tank as shown in Figure 2.5b. Secondly a lossless step-down transformer having a turn ratio of  $n$  can be used to transformer the emitter impedance to  $n^2/g_m$  as shown in Figure 2.6.

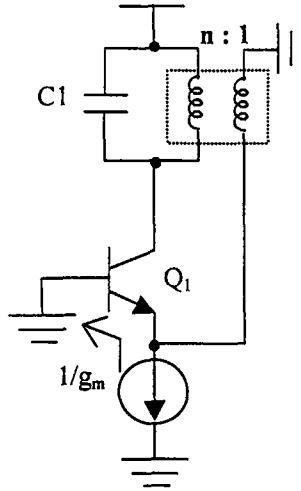


**Figure 2.6** Use of an explicit transformer [21].

A third method of passive impedance transformation can be achieved by using tanks with capacitive or inductive dividers. These circuits are called as Colpitts and Hartley oscillators. The definition of the quality factor  $Q$  and quality factor's for different tank circuits are given in Appendix A.

### 2.3.2.1 Colpitts Oscillator

The Colpitts oscillator and the equivalent circuit are shown in Figure 2.7. The equivalent parallel resistance in the tank is approximately equal to  $(1 + C_1 / C_2)^2 / g_m$ . So as discussed before the emitter impedance is transferred to a higher value.

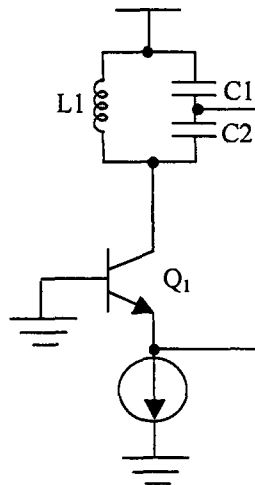


**Figure 2.7** Colpitts oscillator [21]

The resonance frequency is,

$$\omega_R = \frac{1}{\sqrt{L_1 \frac{C_1 C_2}{C_1 + C_2}}} \quad (2.8)$$

If large voltage swings wanted to be achieved, the value of the inductor has to be maximized. The reason is; the Q of the inductors is lower than that of capacitors, so that the equivalent parallel resistance of the tank can be written as

$$R_P = (L_1 \omega_R)^2 / R_S = \frac{L_1}{C_{eq} R_S} \quad (2.9)$$

where  $R_S$  models the loss of the inductor as a series resistor and  $C_{eq}$  is the equivalent capacitance of the tank.. In typical inductors,  $L_1$  and  $R_S$  scale proportionally, that means if  $L_1$  increases by the factor  $m$  then so does  $R_P$ . The impedance of the tank at resonance is equal to  $R_P$ , so the voltage swing for a given bias current also increases by the same factor.

If the inductor is off-chip, increasing its value also minimizes the effect of bond wire inductance, very important for high frequency applications over 1GHz. Maximizing the value of inductor has got two disadvantages. First the self-resonance frequency of the inductor decreases, approaching oscillation frequency of interest. Secondly, the tank capacitance becomes limited by device capacitances, so that making it difficult to vary the frequency by adding a variable capacitor to the oscillator.

Colpitts oscillator has two disadvantages. It provides only single-ended output. Secondly, the ratio of the capacitors tends to be large number, for the emitter impedance of the transistor to have negligible effects on the Q of the tank.

Colpitts oscillator can be designed with MOS transistors also as shown in Figure 2.8.

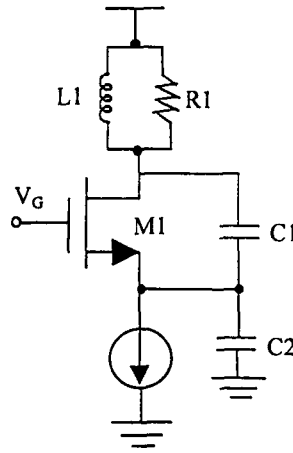


**Figure 2.8** Colpitts oscillator with MOS transistor [35]

### 2.3.2.2 Hartley Oscillator

Hartley oscillator has the same structure with Colpitts oscillator, but inductive dividers are used instead of capacitive dividers as shown in Figure 2.9. The resonance frequency is

$$\omega_R = \frac{1}{\sqrt{C_1 \frac{L_1 L_2}{L_1 + L_2}}} \quad (2.10)$$

All the properties and trade-off of the Hartley oscillator is same with Colpitts oscillator as mention in Section 2.3.2.1 But Hartley oscillator is less used than Colpitts oscillator, due to incorporating two inductors.

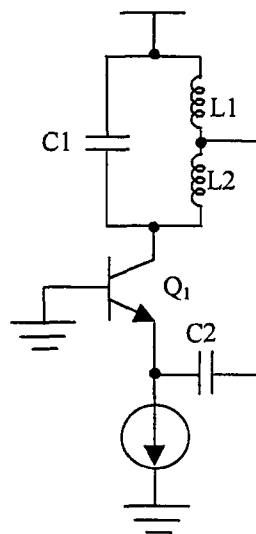


**Figure 2.9** Hartley oscillator [21]

### 2.3.3 Crystal Oscillators

Crystal oscillators play an important role in modern electronic circuits. The resonant frequency of a crystal is accurately defined and its quality factor is very high usually more than 10000. Whenever an application requires precise definition of oscillation frequency, low phase noise and low power, a crystal oscillator is the best candidate. And also because of these facilities of crystal oscillator it is the first choice for generating reference signals for frequency synthesizers.

#### 2.3.3.1 Basics of Crystal Oscillators

A piezoelectric crystal shows electromechanical-resonance characteristics that are very stable with time and temperature, and highly selective (having very high Q factors). So the oscillators based on the characteristic of a crystal, are the most stable ones. The circuit symbol of a crystal is shown in Figure 2.10a and its equivalent circuit model is shown in Figure 2.10b.

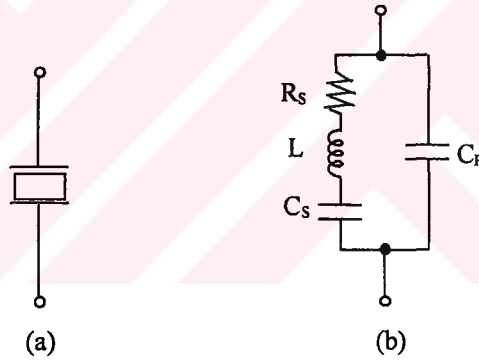


**Figure 2.10** (a) Crystal resonator symbol (b) Equivalent circuit of a crystal resonator [34].

The resonance properties are characterized by a large inductance  $L$ , (as high as hundreds of henries), a very small series capacitance  $C_s$  (as small as 100fF), a series resistance  $R_s$  representing a Q factor  $\omega_0 L/R_s$  that can be high as a few thousand, and a parallel capacitance  $C_p$  (a few picofarads). Capacitor  $C_p$  represents the electrostatic capacitance between the two parallel plates of the crystal. Note that  $C_p \gg C_s$ . Due to the high quality factor  $Q$ , the resistance  $R_s$  can be neglected and the crystal impedance can be expressed as [34]

$$Z(s) = 1 / \left[ sC_P + \frac{1}{sL + 1/sC_S} \right] \quad (2.11)$$

and can be written as

$$Z(s) = \frac{1}{sC_P} \frac{s^2 + (1/LC_S)}{s^2 + [(C_P + C_S)/LC_S C_P]} \quad (2.12)$$

From this equation, it can be seen that the crystal oscillator has two resonance frequencies. The series resonance at  $\omega_s$ ,

$$\omega_s = 1/\sqrt{LC_S} \quad (2.13)$$

At series resonance frequency the impedance becomes almost zero. This happens when the negative impedance of the capacitor  $C_S$  cancels the positive impedance of the inductor  $L$  [36]. The parallel resonance at  $\omega_p$ ,

$$\omega_p = 1/\sqrt{L \left( \frac{C_S C_P}{C_P + C_S} \right)} \quad (2.14)$$

For  $s=j\omega$ , equation (2.14) can be written as

$$Z(j\omega) = -j \frac{1}{\omega C_P} \left( \frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2} \right) \quad (2.15)$$

From equations (2.14) and (2.15) it seems  $\omega_p > \omega_s$  but because  $C_P \gg C_S$ , the two resonance frequencies are very close to each other. Expressing  $Z(j\omega) = jX(\omega)$ , the crystal reactance  $X(\omega)$  will have the shape shown in Figure 2.11. It shows that the crystal reactance is inductive over the very narrow frequency band between  $\omega_s$  and  $\omega_p$  [34].

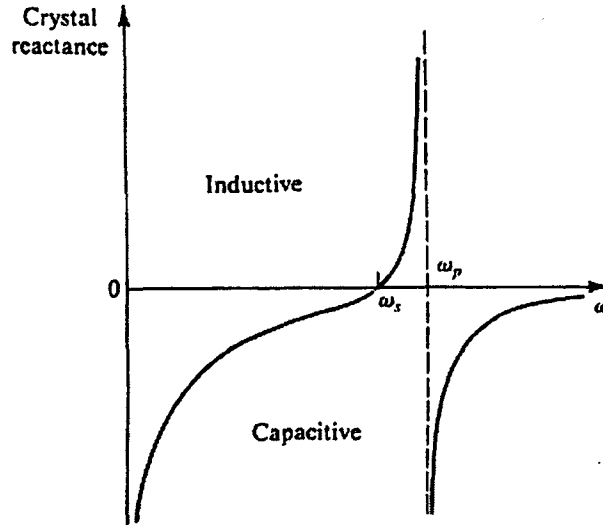


**Figure 2.11** Crystal reactance versus frequency

There are different configurations for crystal oscillators. Certain configurations give superior performance in one area at the expense of other area. So the choice of the circuit configuration is generally predicted by the required performance. Here, by making few simple modifications to the common Colpitts-Pierce-Butler configurations, some high performance crystal oscillators will be shown.

A parallel resonant oscillator is one in which the crystal and any load capacitance across the crystal operate at a pole. This can be somewhat confusing, though, since several components in series can function as a net capacitor or inductor at the frequency of operation. Thus, capacitor and inductor may be placed in series with crystal in a Colpitts oscillator, yet it will still be a parallel resonant oscillator [micro].

Note that we could take a Colpitts LC oscillator and place the crystal between the transistor emitter and capacitor junctions as shown in Figures 2.12 and 2.13. This oscillator would be considered series resonant since the crystal could be replaced with a small resistor. However, the LC split tank would still be operating at its high impedance or parallel resonant state. This illustrates the confusion that can be generated by the use of the term series or parallel resonant. The only reason to specify an oscillator as series or parallel resonant is so that one can specify the crystal properly. The proper crystal load designation is usually obvious from the circuit configuration [37].

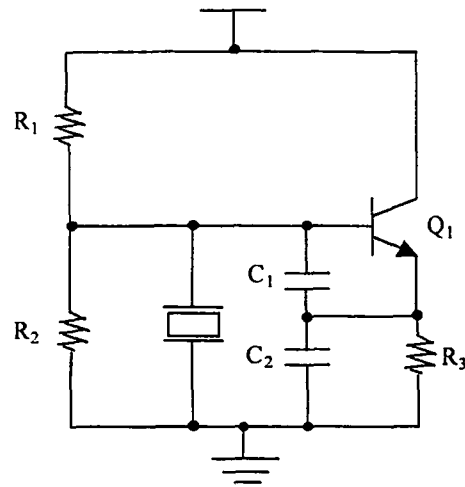


**Figure 2.12** Colpitts crystal oscillator operating in parallel resonant configuration [37].

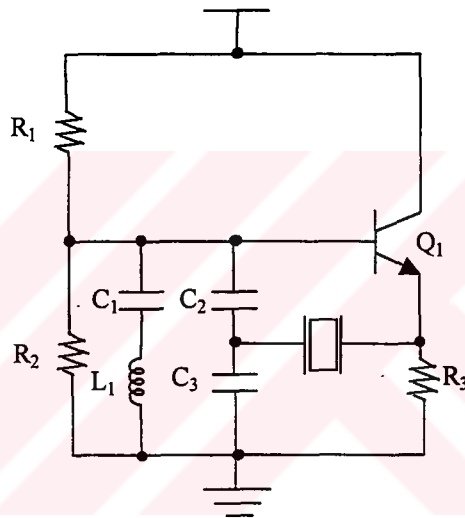


**Figure 2.13** Colpitts crystal oscillator operating in series resonant configuration [37]

The crystal appears inductive in parallel resonant configuration and resistive in the series resonant configuration, neglecting the small effect of the crystal  $C_p$ .

In Figure 2.14 Pierce and Colpitts crystal oscillators are shown in a different way with comparison. The principle difference between them is the choice of signal ground. If the emitter is grounded for the Pierce oscillator, the configuration reverts to the Colpitts oscillator. Note that in Figure 2.14, the biasing circuits are not illustrated for simplicity.

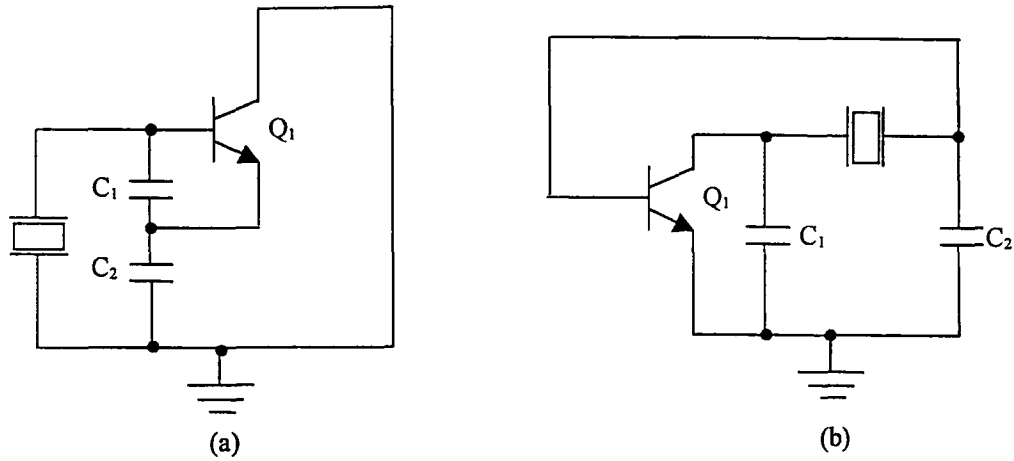


**Figure 2.14** (a) Pierce oscillator realization for fundamental crystals, (b) Colpitts oscillator realization for fundamental crystals.

Colpitts crystal oscillator works very well for good performance up to about 50MHz. Since there is no collector resistor in the typical Colpitts oscillator, the amplitude limiting is done generally by cut-off in the transistor. This method of limiting is preferable to saturation of the transistor.

The Pierce oscillator is also very capable of good performance, but the impedance at the collector may cause transistor saturation if the oscillator gain is too high. This oscillator can be used up to 50MHz. In recent years low power design of high frequency CMOS crystal oscillators with Pierce oscillator is achieved where the oscillation frequency is tuned digitally [38]. More examples for different configurations are explained in detail [37].

Pierce oscillator is the most common configuration to provide clock signal in digital ICs. It's crystal and load capacitors are connected between two pins of the IC. To minimize the number of external components, load capacitors and bias resistor may be integrated on chip. In Pierce oscillator both capacitors refer to ground, facilitating the use of MOS gate capacitance and thereby greatly reducing the chip area. Due to the limited numbers of pins on an IC package it is desirable to have the same function with a single pin and crystal referring to ground. So having at least one floating capacitor makes the chip area larger and IC expensive. A universal  $0.03\text{mm}^2$  one pin crystal oscillator also presented in that overcomes these problems in ICs [39].

Crystals suffer from frequency drift with temperature today high performance applications ask for much better frequency stabilities. This requires controlling circuitry for either temperature of the crystal or for the frequency itself. In recent years the systems are designed that uses digitally stored constants to tune the frequency of a crystal oscillator depending on the ambient temperature [40].

Many measurement systems like pressure temperature or detection and measurement of other physical or chemical quantities need specially designed sensitive crystals and resonators. Analog ALC Crystal oscillator for high temperature applications are used for these measurement applications [41].

In general the most common oscillation frequencies for crystal oscillator are of the order of 10MHz, but crystal using a harmonic overtone of the fundamental resonance frequency can achieve several hundred MHz. But unfortunately they are fixed-frequency circuits.

#### 2.3.4 Relaxation oscillators

Monolithic oscillators can be realized with relaxation oscillators, which are capable of high speeds. The basic circuit is the emitter-coupled multivibrator shown in Figure 2.15 [42,43].

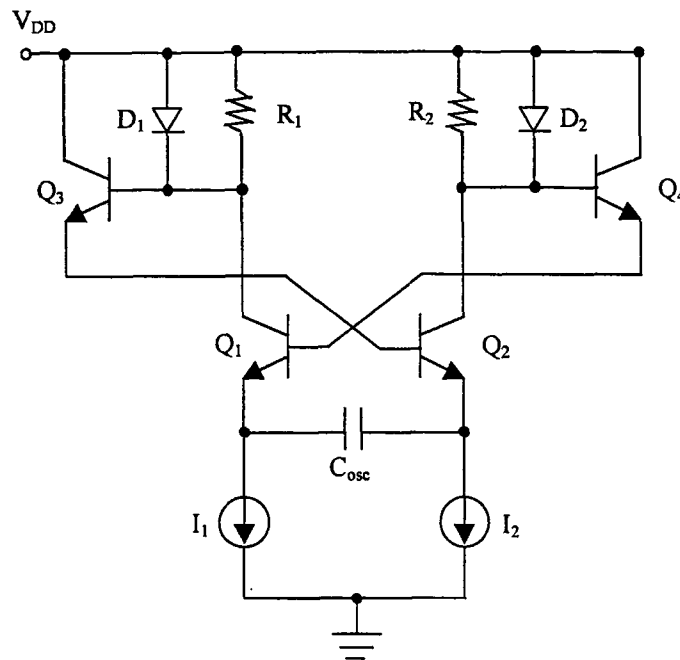


**Figure 2.15** Emitter coupled multivibrator [42]

They operate by alternately charging and discharging an energy storage element between two initially set threshold voltage levels. In this oscillator  $Q_1$  and  $Q_2$  alternately turn on and off. When one of these transistors is off, the node at its emitter slowly changes to a more negative voltage due to the current following from current source,  $I_1$ , connected to emitter out of capacitance  $C_{osc}$ , which is also connected to the emitter. The transistors  $Q_3$  and  $Q_4$  both operate as level shifting emitter followers and the diodes  $D_1$  and  $D_2$  define the voltage swings at the collectors of  $Q_1$  and  $Q_2$ . The oscillation frequency can be defined as [42]:

$$f_{osc} = \frac{I_1}{4V_D C_{osc}} \quad (2.16)$$

To control the oscillation frequency, the current sources used to discharge  $C_{osc}$ , are made proportional to a control voltage. It should be noted that this oscillator could be strongly temperature dependent due to the temperature dependence of  $V_D$ , which is the voltage drop across a forward biased diode. Making all currents proportional to absolute temperature can minimize this temperature dependence.

In Figure 2.16 a MOS relaxation oscillator is drawn. The analyses in [8] indicate that MOS relaxation circuits has potential advantage over classical bipolar circuits. Parasitic MOS oscillator structures allow greater circuit integration and lower power consumption. However the maximum oscillation frequency is related to the device speed and device sizing and therefore parasitic-only MOS oscillators can be optimized for speed through architecture and layout techniques.

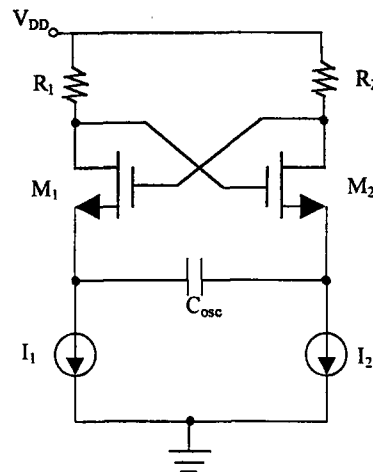


**Figure 2.16** A simplified circuit of CMOS relaxation oscillator [8]

Since the relaxation oscillators do not require any external component for oscillation, they are now becoming preferable in most high frequency fully integrated PLL circuits. The relaxation oscillator architectures must have some form of compensation, or use some special techniques to accommodate wide tuning range.

### 2.3.5 Ring Oscillators

Ring oscillator is a very important integrated oscillator configuration. Due to its simplicity and its ease in IC integration as it does not need passive elements, it is used in a lot of PLL frequency synthesizer and clock recovery designs.

A ring oscillator consists of number gain stages in a loop. There should be at least three gain stages, with less the oscillation conditions are not satisfied. In Figure 2.17, a three-stage ring oscillator is shown. According to the equations of loop gain and phase, to satisfy oscillation, each stage requires a low frequency gain of 2 and it oscillates at a frequency of  $\sqrt{3}\omega_0$  where  $\omega_0$  is the 3dB bandwidth of each stage [35].

A simple implementation of ring oscillators that does not require resistors is shown in Figure 2.17 where inverters are used. Here  $\omega_0$  is determined by small-signal output resistance and the capacitance of each inverter near the trip point whereas time delay of inverter results from large signal, nonlinear current drive and capacitances of each stage [35].

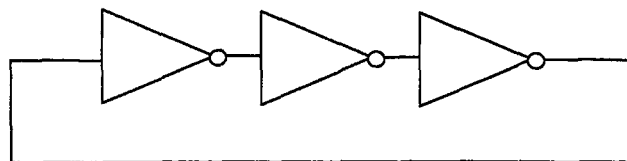


**Figure 2.17** Three stage ring oscillator using CMOS inverters [35].

A ring oscillator employing more than three stages are also feasible but there must be odd number of open loop inverting amplifiers in a feedback loop.

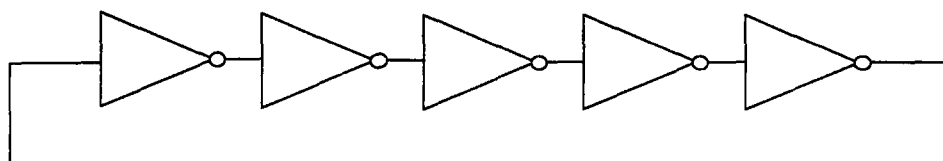


**Figure 2.18** Five stage ring oscillator using CMOS inverters.

A five-stage ring oscillator is shown in Figure 2.18. It is a form of negative feedback but because each inverter has 90 degrees phase shift at its unity-gain frequency, it is sure that loop gain will be greater than unity when the phase shift around the loop becomes greater than 180 degrees. As a result the circuit is unstable and oscillation occurs. Each half period, the signal will propagate around the loop with an inversion. For example assume the output of the first inverter changes to one. This change will propagate through all five inverters in a time  $T/2$  at which time the output of the first inverter will change to 0; after an additional time of  $T/2$ , the first inverter's output will change back to 1 and so on. Assuming each inverter has a delay of  $\tau_{inv}$  and that there are  $n$  inverters, then it can be written:

$$\frac{T}{2} = n\tau_{inv} \quad (2.17)$$

$$f_{osc} = \frac{1}{T} = \frac{1}{2n\tau_{inv}} \quad (2.18)$$

It is very important that in CMOS technology, ordinary CMOS inverters are not used because they have a gate threshold voltage proportional to power supply voltage. In most ring oscillators, fully differential inverters are used to obtain better power supply insensitivity. When this is done, an even number of the inverters can be used and the inversion required around the loop can be achieved by simply interchanging the outputs of the last inverter before feeding them back to the input as shown in Figure 2.19 [42]. This realization is very important advantage in that the outputs of the middle inverters will have a quadrature phase relationships as compared with last inverters. This type of ring oscillator is used in our design, which explained in Chapter 4 and Chapter 5. The delay cells or inverters used for the ring oscillators are also explained in Chapter 4.

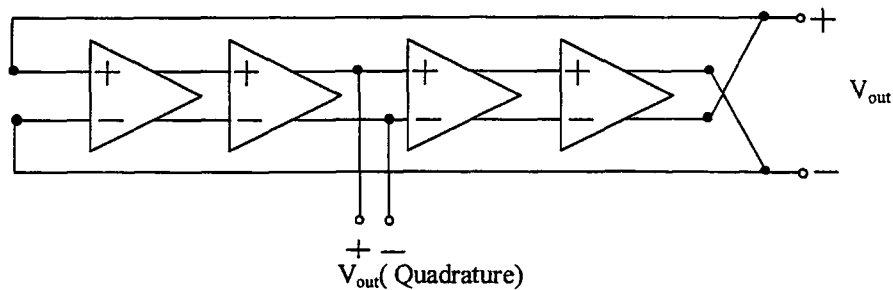


**Figure 2.19** Four-stage ring oscillator with quadrature outputs [42]

The number of stages in a ring oscillator is determined by various requirements, including speed, power dissipation, noise immunity etc. In most applications, three to five stages provide optimum performance (for differential implementations) [35].

### 2.3.6 Other LC oscillators

Both relaxation oscillator and ring oscillator are capable of an operating frequency in the GHz range when implemented in an advanced submicron CMOS technology, and they require no external passive components. But their phase noise behavior is generally not good enough to be applicable in a wireless system. Lowering the phase noise to an acceptable level requires too much power. The only other monolithic oscillator type is the one based on the resonance of an inductor and capacitor connected in a loop, the LC oscillator. Therefore LC oscillators seem to be more suitable for wireless applications. In Section 2.3.2, we have mentioned about basic LC topologies, but these are not used in the wireless systems. The ones that are explained in this section and in Chapter 4 are the common ones.

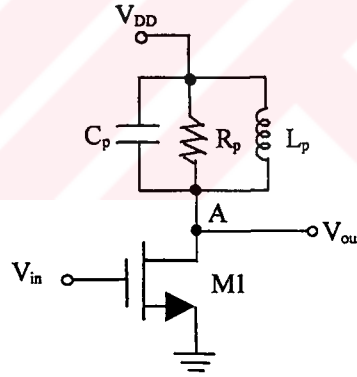


**Figure 2.20** Tuned gain stage [35]

Consider a tuned gain stage showed in Figure 2.20, placing the two stages of it in cascade as depicted in Figure 2.21, the core of many LC oscillators is achieved. If  $g_{m1}R_p g_{m2}R_p \geq 1$ , the loop oscillates.  $V_A$  and  $V_B$  are differential waveforms.

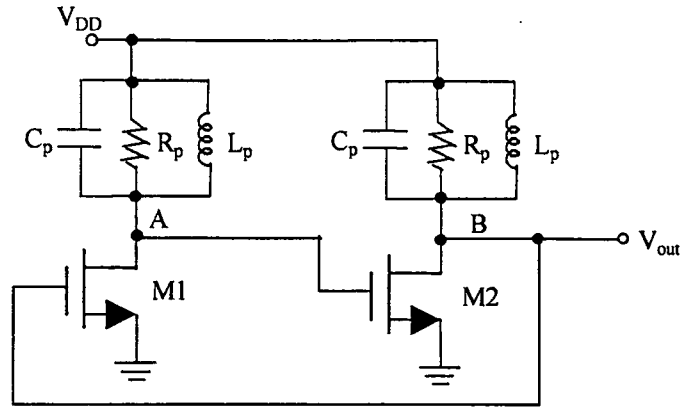


**Figure 2.21** Two tuned stages in a feedback loop [35]

This circuit can be drawn as in Figure 2.22. The drain currents of M1 and M2 and the output swing heavily depend on the supply voltage.

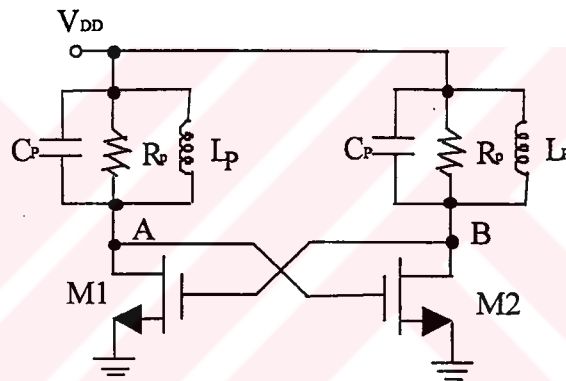


**Figure 2.22** Redraw of the oscillator in Fig. 2.21 [35].

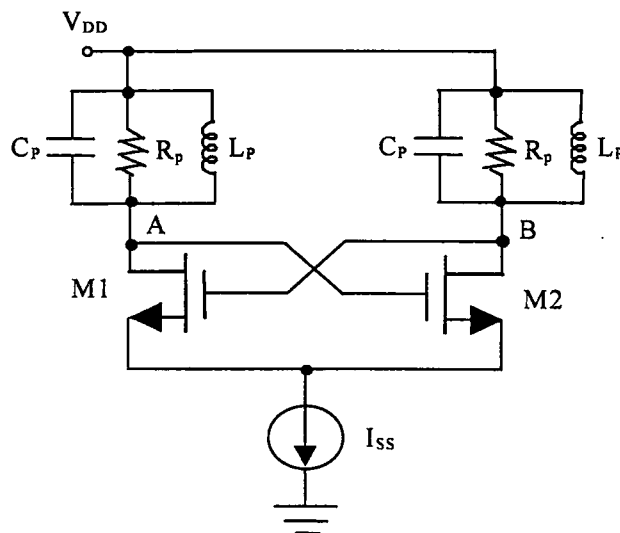


**Figure 2.23** Addition of tail current to lower the supply sensitivity [35]

Since the waveforms at nodes A and B are differential, the drawing in Figure 2.22 suggests that M1 and M2 can be converted to a differential pair as shown in Figure 2.23 where total bias current is defined by  $I_{SS}$ .

In the beginning of oscillation, if there is zero difference between  $V_A$  and  $V_B$  then  $V_A = V_B \approx V_{DD}$ . The two transistors share the tail current equally. If  $(g_{m1,2} R_P)^2 \geq 1$ , where  $R_P$  is the equivalent parallel resistance of the tank at resonance, then M1 and M2 continually amplify the noise components at the resonance frequency, allowing oscillation to grow. The drain currents of M1 and M2 vary according to instantaneous value of  $V_A - V_B$ . The oscillation amplitude grows until the loop gain drops at the peaks. This oscillator is constructed fully differential form. The supply sensitivity of the circuit is nonzero with perfect symmetry. This is because the drain junction capacitances of M1 and M2 vary with the supply voltage [35].

As explained above, oscillators utilized in RF applications often fall in the feedback category but where applicable, the one port model can give additional insight into their operation with the concept of negative resistance. One port model treats the oscillator as two one-port networks, are connected to each other as shown in Figure 2.24.

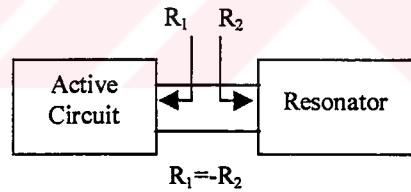


**Figure 2.24** One port view of oscillators [21]

Suppose the resonator is a simple tank shown in Figure 2.25a along with parasitic resistances. As mentioned in Appendix A for a narrow band of frequencies, the circuit can be converted to parallel combination shown in Figure 2.25b [21].

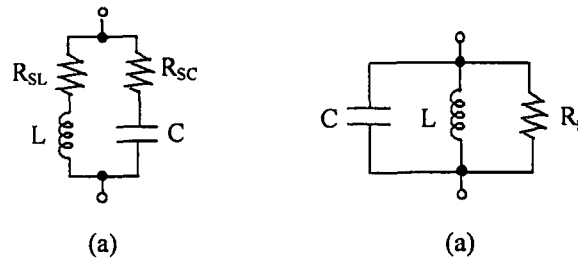


**Figure 2.25** (a) LC resonator (b) Equivalent circuit of (a)

The tank itself doesn't oscillate indefinitely because some of the stored energy is dissipated in  $R_p$  every cycle. The idea in one port model is that active network generates an impedance equal to  $-R_p$  so that the equivalent parallel resistance seen by the intrinsic, lossless resonator is infinite. So  $R_p \parallel (-R_p) = \infty$ , the tank oscillates indefinitely. The active circuit replenishes the energy lost in  $R_p$  in every cycle [21].

We should find the circuit, which provides negative resistance. The feedback multiplies or divides the input and output impedances of circuits by a factor equal to one plus the loop gain. If the loop gain is sufficient negative (the feedback is sufficiently positive) a negative resistance is achieved. We can apply a positive feedback around a source follower as shown in Figure 2.26, where the feedback is implemented by a common gate stage and the current source  $I_b$  is added to provide the bias current of M2 [35].

If  $g_{m1} = g_{m2} = g_m$ ,

$$R_{in} = \frac{-2}{g_m} \quad (2.19)$$

Negative resistance indicates that if the applied voltage increases, the current drawn by the circuit decreases. The oscillator using negative input resistance of a source follower with positive feedback is shown in Figure 2.27.

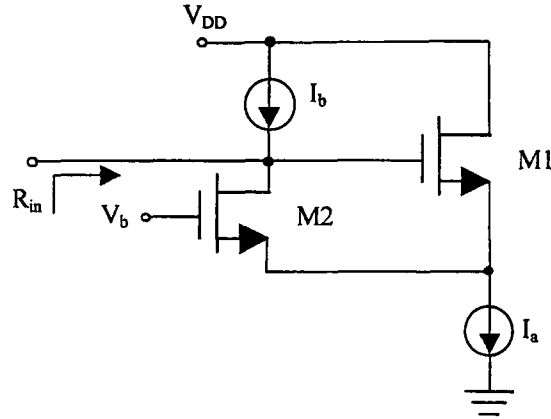


**Figure 2.26** Source follower with positive feedback to create negative input impedance [35].

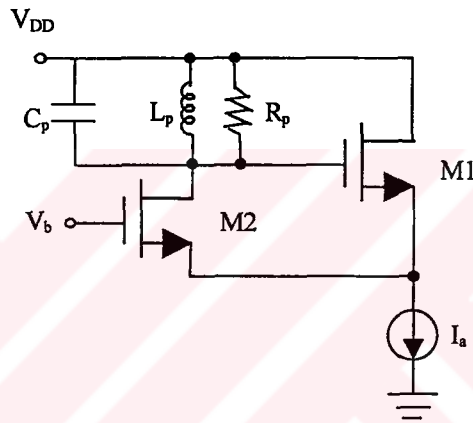


**Figure 2.27** Oscillator using negative input resistance of a source follower with positive feedback.

Here  $R_p$  denotes the equivalent parallel resistance of the tank and for oscillation build-up  $R_p - 2/g_m \geq 0$ . The inductor provides the bias current of M2. If the small signal resistance presented by M1 and M2 to the tank is less negative than  $-R_p$ , then the circuit experiences large swings such that each transistor is nearly off for the part of the period, thereby yielding an average resistance of  $-R_p$ . This circuit can be drawn as in Figure 2.28. If the drain current of M1 flows through a tank and the resulting voltage is applied to the gate of M2, then the circuit topology as shown in Figure 2.29 is obtained. So we arrive to the same topology in Figure 2.23.

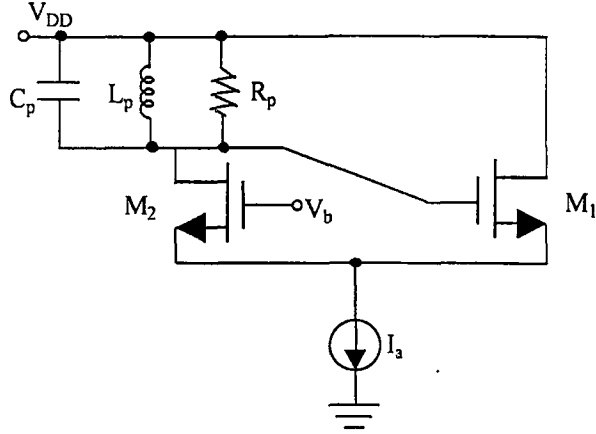


**Figure 2.28** Redrawing of the topology in Fig. 2.27[35].

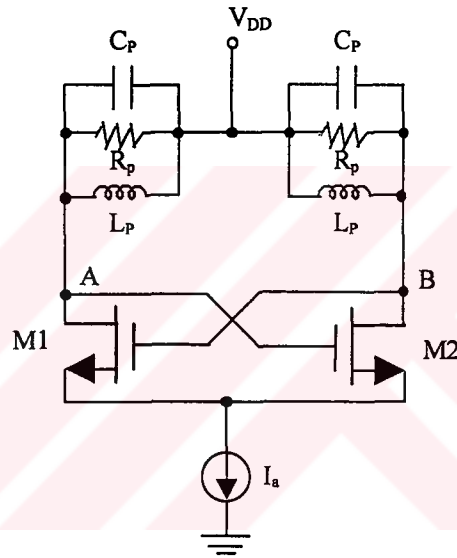


**Figure 2.29** Differential version of the topology in Fig. 2.28 [35]

There are two tank circuits here, if we merge these two tanks into one as shown in Figure 2.30, it is known that the cross-coupled pair must provide a negative resistance of  $-R_p$  between nodes A and B to enable oscillation. This resistance is equal to  $-2/g_m$  and it is necessary that  $R_p \geq 1/g_m$ . The circuit can be viewed as either feedback system or a negative resistance in parallel with a lossy tank. This topology is called a “negative- $G_m$  oscillator”.

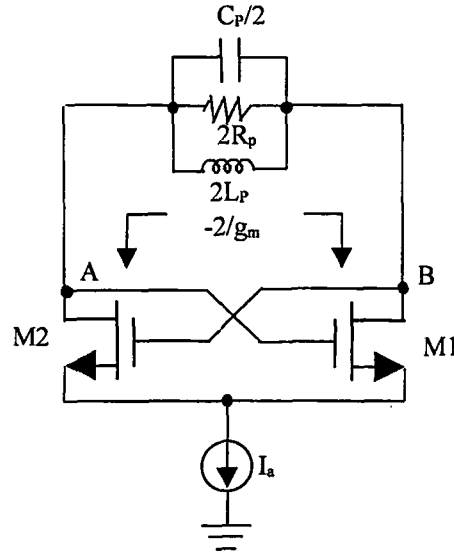


**Figure 2.30** Equivalent circuit of Fig. 2.29 [35]

This topology can be explained with Colpitts and Hartley oscillators. In Colpitts and Hartley oscillators the impedance transformed by means of passive networks. Consider the oscillator shown where active buffer,  $B_1$  is used between the collector and the emitter, presenting a relatively high impedance to the tank. As shown in Figure 2.31a the buffer can be implemented as an emitter follower Figure 2.31b. The circuit can also incorporate two inductors to operate differentially. However if the inductors are off-chip bondwire parasitics make it difficult to achieve a small phase mismatch between the two tanks.

The differential implementation of Figure 2.31b is shown in Figure 2.32. The impedance seen at the collector of  $Q_1$  and  $Q_2$  can be calculated. As calculated before with positive feedback  $R_m = -2/g_m$ . If  $|R_m|$  is less than or equal to equivalent parallel resistance of the tank, the circuit oscillates (negative  $G_m$  oscillator). A capacitive divider can be inserted in the feedback path in order to avoid heavily saturation of  $Q_1$  and  $Q_2$ . (Especially when the collector voltage of transistors exceed 400mV). This divider also allows greater voltage swings and higher common mode level at nodes A and B than the bases of  $Q_1$  and  $Q_2$  [21].

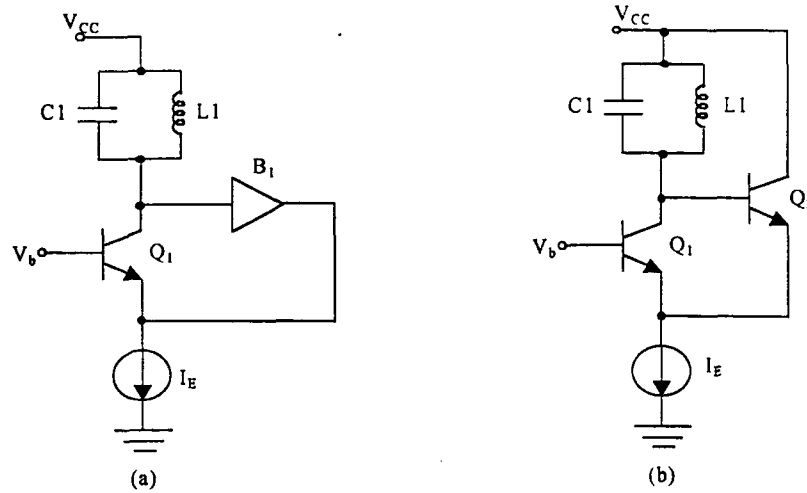


**Figure 2.31** (a) Colpitts oscillator with active buffer in the feedback loop (b) implementation of buffer with emitter follower [21].

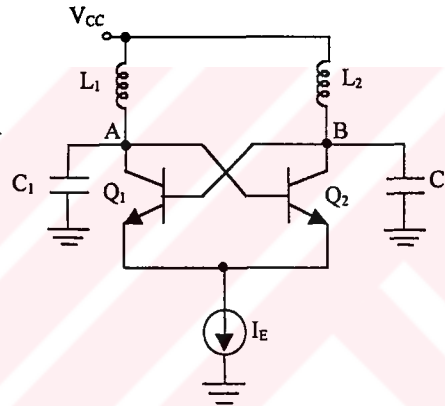


**Figure 2.32** Differential implementation of Fig. 2.31(b)

The same type of LC oscillator can be designed with MOS transistors as shown in Figure 2.33. Other type of LC oscillators is explained in Chapter 4 serving as VCOs.

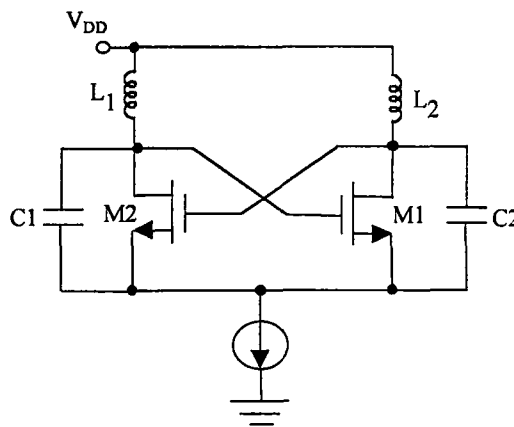


**Figure 2.33** Differential implementation of Fig. 2.31(b) with MOS transistors [21]

### 3. BASICS OF VCO DESIGN

In the previous chapter, we mentioned about the oscillation theory and some RF oscillators basically. In wireless systems, as there is an operating frequency band spec, we need oscillators that are controlled by voltage to oscillate at different frequencies. In this chapter, we start with the definition of the VCO and the basic VCO terms where we meet frequently in the books, journals or catalogues. The phase noise of the RF system is mainly determined by the phase noise of the VCO, therefore phase noise models of LC and ring oscillators are given. The key elements in a VCO are inductors and varactors. Varactors are important for their effect on the tuning range performance and inductors are important for the phase noise performance. In the last sections of this chapter different types of varactor and inductor implementations are explained with examples.

#### 3.1 Voltage Controlled Oscillators

If the output frequency of an oscillator can be varied by a voltage, then the circuit is called VCO. So an ideal VCO is circuit whose output frequency is a linear function of its control voltage. Equation (3.1) explains the mathematical model of VCO

$$\omega_{\text{out}} = \omega_{\text{FR}} + K_{\text{VCO}} V_{\text{cont}} \quad (3.1)$$

In the equation  $\omega_{\text{FR}}$  is the free running frequency meaning that the output frequency when  $V_{\text{cont}}=0$ ,  $K_{\text{VCO}}$  is the gain of the VCO (expressed in rad/s/V). The equation shows that for a practical change of  $V_{\text{cont}}$  creates a change around  $\omega_{\text{FR}}$ . The definition of VCO is showed in Figure 3.1.

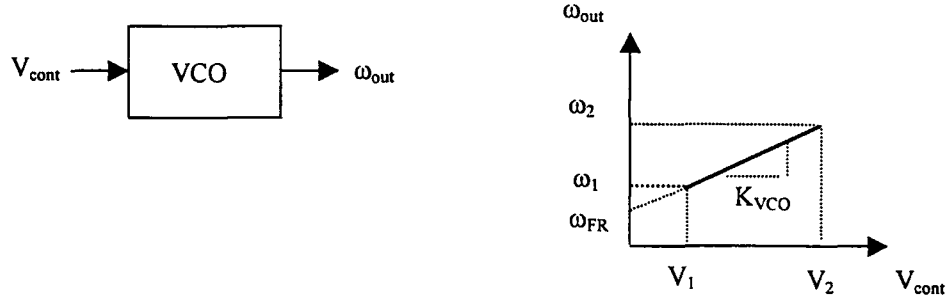


**Figure 3.1** Definition of VCO [35]

$\omega_1$ - $\omega_2$  is the tuning range of the oscillator. The method of tuning the oscillator depends on the type of oscillator. For this work we will discuss about ring and LC VCOs. The tuning method of these VCOs is going to be discussed in Chapter 4 in detailed. Before going further about VCOs we should know all the terms used for VCOs.

### 3.2 Basic VCO Terms

The VCOs have important performance parameters like centre frequency, tuning range, tuning linearity, phase noise, output amplitude, power dissipation etc. You can find these parameters in the catalogue of a VCO, or in system specs.

**Centre frequency:** It is the midrange frequency of the VCO's achievable frequency range.

**Tuning range:** It is the frequency range that the VCO can achieve or the difference between the achievable maximum and minimum frequency of the VCO. The tuning range of a VCO is the necessary frequency range for the application. The variation of the center frequency of the VCO with process and temperature also determines the tuning range. Some applications incorporate clock frequencies that must vary by one to two orders of magnitude depending on the mode of operation, demanding a proportionally wide tuning range.

An important concern in the design of VCOs is the variation of the output phase and frequency as a result of noise on the control line. For a given noise amplitude, the noise in the output frequency is proportional to  $K_{VCO}$  because

$\omega_{\text{out}} = \omega_{\text{FR}} + K_{\text{VCO}} V_{\text{cont}}$ . Thus, to minimize this effect of noise in  $V_{\text{cont}}$ , VCO gain must be minimized, which is a constraint in direct conflict with the required tuning range. In fact, if, as shown in Figure 3.1, the allowable range of  $V_{\text{cont}}$  is from  $V_1$  to  $V_2$  and the tuning range must span at least  $\omega_1$  to  $\omega_2$ , then  $K_{\text{VCO}}$  must satisfy the following requirement [35]:

$$K_{\text{VCO}} \geq \frac{\omega_2 - \omega_1}{V_2 - V_1} \quad (3.2)$$

**Tuning Linearity:** The deviation of the frequency versus tuning voltage characteristic from a best-fit straight line. The tuning characteristics of the VCOs exhibit nonlinearity because  $K_{\text{VCO}}$  is not constant. This nonlinearity degrades the settling behaviour of the PLL. Therefore it is desirable to minimize the variation of  $K_{\text{VCO}}$  across tuning range. As shown in Figure 3.2, actual oscillator characteristics typically exhibit a high gain region in the middle of the range and a low gain at the two extremes. Compared to a linear characteristic (the gray line), the actual behaviour displays a maximum gain greater than that predicted by the Equation (3.2), implying that, for a given tuning range, nonlinearity inevitably leads to higher sensitivity for some region of the characteristic.

**Tuning Performance:** In some books or journals, the tuning performance of the VCO is also called tuning sensitivity, that enumerates how much a VCO's frequency changes per unit of tuning-voltage change. This is typically expressed in megahertz per volt (MHz/V).

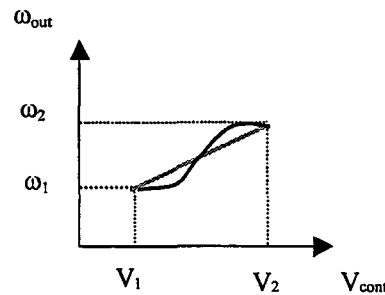


**Figure 3.2** Nonlinear VCO characteristic[35]

**Tuning Speed:** This is the time required for the output frequency to settle to within 90 percent of its final value on the application of a tuning-voltage step.

**Output Amplitude:** It is desirable to achieve large output oscillation amplitude, thus making the waveform less sensitive to noise. The amplitude trades with power dissipation, supply voltage, and even the tuning range. Also the amplitude may vary across the tuning range which is an undesirable effect.

**Power Dissipation:** As with other analog circuits, oscillators suffer from trade-offs between speed, power dissipation, and noise. Typical oscillator drain 1 to 10mW of power.

**Output Signal Purity:** Even with a constant control voltage, output waveform of a VCO is not perfectly periodic. The electronic noise of the devices in the oscillator and supply noise lead to noise in the output phase and frequency. These effects are quantified by “jitter” and “phase noise” and determined by the requirements of the application.

**Frequency pushing:** The changing of output frequency corresponding to a given change in the supply voltage at a fixed tuning voltage. So it is the dependency of the center frequency on the power supply voltage (in [MHz/V]).

The other important VCO terms like phase noise, varactors and inductors are going to be explained in detailed in the next sections of this chapter.

### 3.3 Phase Noise

Phase noise is a very important performance parameter of RF systems. First the definition and the effect of the phase noise is explained. Following that, the phase noise models for LC and ring oscillators are discussed.

#### 3.3.1 General Considerations

Oscillators, as other analog circuits, are susceptible to noise. Noise injected into an oscillator by its constituent devices or by external means may influence both the frequency and the amplitude of the output signal. In most cases, the disturbance in

the amplitude is negligible or unimportant and only the random deviation of frequency is considered.

In RF applications, phase noise usually characterized in the frequency domain. For an ideal oscillator operating at frequency  $\omega_0$ , the output can be expressed as  $V_{\text{out}}(t) = A\cos(\omega_0 t + \theta)$ , where  $A$  is the amplitude and  $\theta$  is a fixed phase reference. Therefore the spectrum assumes the shape of a Dirac impulse. In a practical oscillator, however, the output is more generally given by:

$$V_{\text{out}}(t) = A(t)\cos(\omega_0 t + \theta(t)) \quad (3.3)$$

where  $A(t)$  and  $\theta(t)$  are now functions of time.  $\theta(t)$  is a small random excess phase representing variations in the period. The function  $\theta(t)$  is called “phase noise”. The spectrum of the actual oscillator will have sidebands close to the oscillation frequency. The output spectrum of an ideal and actual oscillator is shown in Figure 3.3

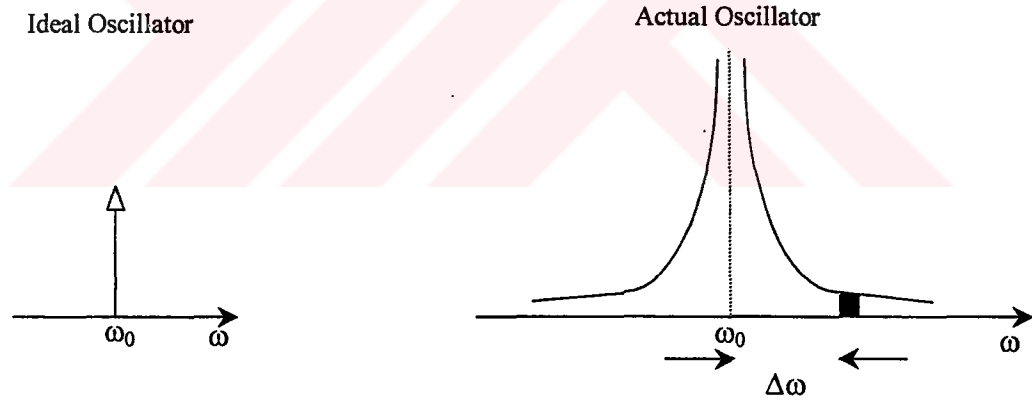


**Figure 3.3** Output spectrum of the ideal and the actual oscillators [21]

To quantify this phase noise, we consider a unit bandwidth of an offset  $\Delta\omega$  from the carrier, calculate the noise power in the band, and divide this result by the carrier power. This is the single sided spectral noise density in units of deciBell carrier per Hertz [dBc/Hz]:

$$L\{\Delta\omega\} = 10 \log \left( \frac{\text{noise power in a 1 - Hz badwidth at frequency } \omega_0 + \Delta\omega}{\text{carrier power}} \right) \quad (3.4)$$

Another plot of an oscillator signal with phase noise is given in Figure 3.4. This spectrum is the power spectrum of an oscillator with a noisy phase angle. Therefore it is the power spectrum of the  $V_{out}(t)$  given in Equation (3.3).

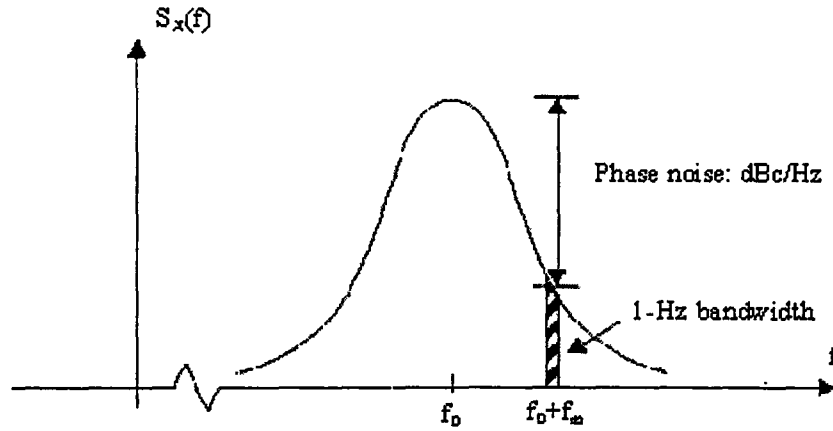


**Figure 3.4** Power spectrum of oscillator [44]

The frequency,  $f_m$  is the offset frequency from the center. As mentioned above phase noise is usually specified in dBc/Hz at a given offset, where dBc refers to the level in dB relative to the carrier. Therefore, the phase noise of an oscillator at a given offset is found from the ratio of the power in a 1-Hz bandwidth at the offset frequency, to the total power of the carrier. In Figure 3.4, this would be the ratio of the area of the rectangle with 1-Hz bandwidth at offset  $f_m$  to the total area under the power spectrum curve.

The spectrum of the phase fluctuations themselves can also be shown, as in Figure 3.5 which is shown on a log-log scale, with phase noise sidebands that fall as  $1/f_m^2$ , or 20dB/decade. In practice, as described in [45] and [46], there are regions in the sidebands where the phase can fall as  $1/f^3$ ,  $1/f^2$  depending on the noise process involved. The  $1/f^2$  region is referred to as the “white frequency” variation region, since it is due to white, or uncorrelated, fluctuations in the period of the oscillator. The behaviour in this region is dominated by the thermal noise in the devices of the oscillator circuit. For low enough offset frequencies the flicker noise of devices generally comes into play and the spectrum in this region falls as  $1/f^3$ .

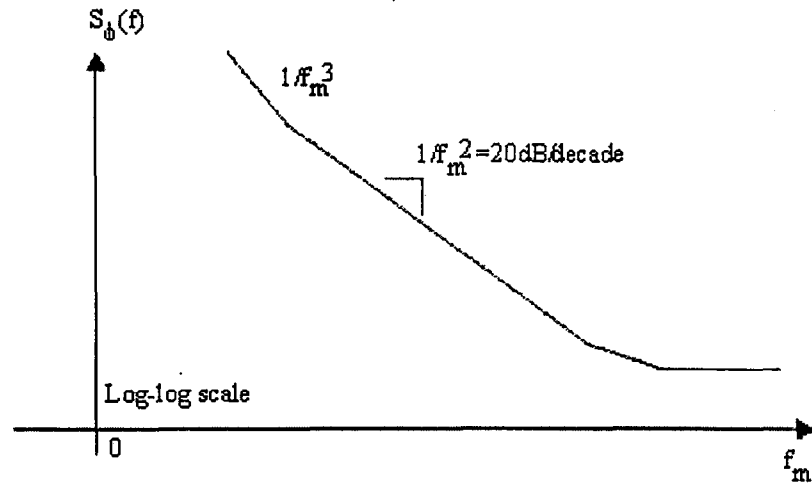


**Figure 3.5** Phase fluctuation power spectral density [44]

To understand the importance of phase noise in RF systems, consider a generic transceiver as shown in Figure 3.6, where a local oscillator provides the carrier signal for both the receive and transmit paths. If the LO output contains phase noise, both upconverted and down converted signals are corrupted. This is shown in Figure 3.7 and in Figure 3.8 [6,21].

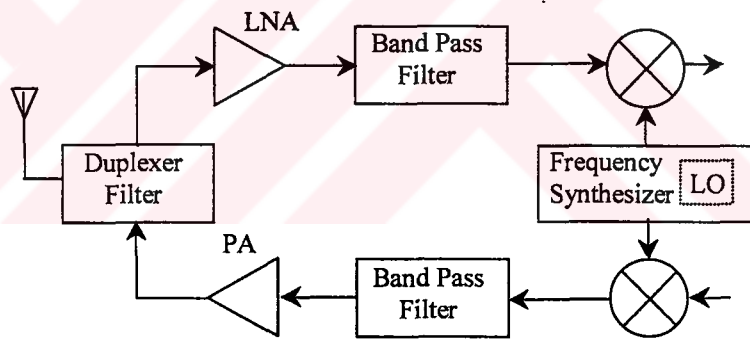


**Figure 3.6** Generic transceiver front end [6]

The ideal case is shown in Figure 3.7a. We note that the signal of interest is convolved with an impulse and thus related to a lower (and a higher) frequency with no change in its shape. In reality, however, the wanted signal may be accompanied by a large interfere in an adjacent channel, and the local oscillator exhibits finite phase noise as shown in Figure 3.7b. When two signals are mixed with the LO output, the downconverted band consists of two overlapping spectra, with the wanted signal suffering from significant noise due to the tail of the interferer. This effect is called “reciprocal mixing”[21].

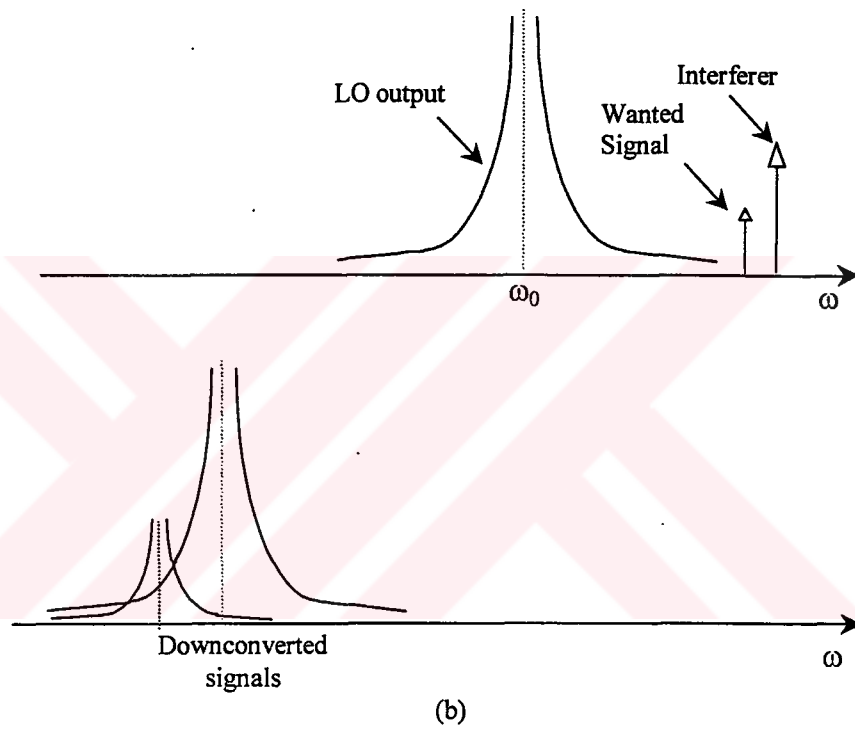
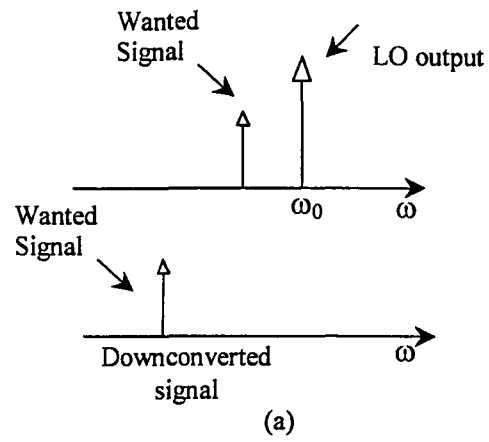


**Figure 3.7** (a) Downconversion by an ideal oscillator (b) reciprocal mixing

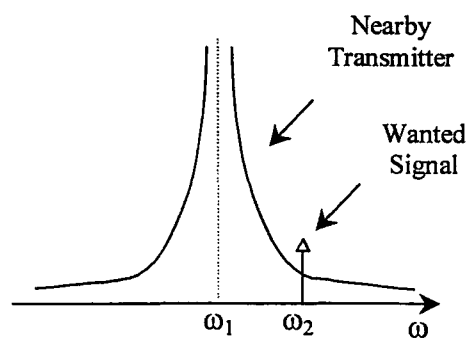


**Figure 3.8** Effect of the phase noise in transmitters

The effect of the phase noise, on the transmit path is slightly different which is shown in Figure 3.8. Suppose a noiseless receiver is to detect a weak signal at  $\omega_2$  while a powerful nearby transmitter generates a signal at  $\omega_1$  with substantial phase noise tail of the transmitter. [6, 21]

Phase noise is a big search subject for researchers. Each researcher proposes new phase noise models for different type of oscillators. In the sections below we will discuss the phase noise of LC oscillators and ring oscillators.

### 3.3.2 LC Oscillator Phase Noise

The phase of definition given with the Equation (3.4), is a general one for all oscillators. In this section we will discuss about the phase noise models and equations specialized for LC oscillator. But first we will discuss about the definitions of Q.

The phase noise of LC oscillators usually depend on their Q. We expect that the higher the Q of the tank, the sharper resonance and the lower phase noise skirts. It is better to examine the three definitions of Q within the context of oscillator before we go deep in phase noise in LC oscillators. We will discuss about three definitions of Q. For an RLC circuit, Q is defined as the ratio of the center frequency and the two sided  $-3\text{dB}$  bandwidth as shown in Figure 3.9 [6].

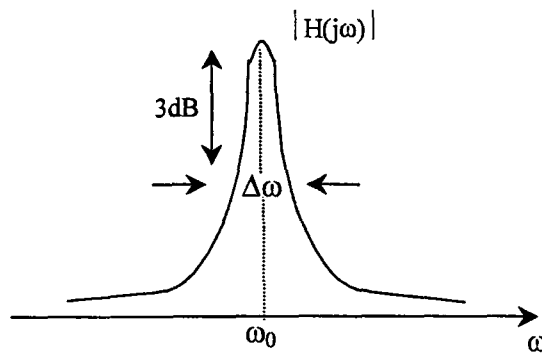


**Figure 3.9** A definition of Q [21]

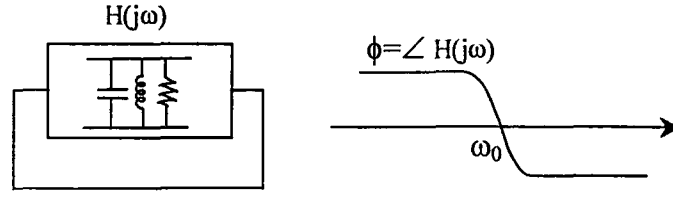


**Figure 3.10** Definition of  $Q$  based on open-loop phase slope [21]

However if the inductor is removed, this definition cannot be applied. A more general definition is:  $2\pi$  times the ratio of the stored energy and the dissipated energy per cycle, and can be measured by a step input and observing the decay of oscillations at the output. Again if the circuit has no oscillatory behaviour (e.g. contains no inductors), it is difficult to define the energy dissipated per cycle. As shown in Figure 3.10, in a third definition, the circuit is considered as a feedback system and the phase of the open-loop transfer function,  $\phi(\omega)$ , is examined at resonance. The  $Q$  is defined as

$$Q = \frac{\omega_0}{2} \left| \frac{d\phi}{d\omega} \right| \quad (3.5)$$

The open-loop  $Q$  is a measure of how much the closed-loop system opposes variations in the frequency of oscillation.

There is a wide body of work on phase noise in LC-tuned oscillators, including Leeson [47], Underhill [48], and others [49]. These analyses use a linear circuit model for the oscillator feedback circuit. Analysis is then carried out in the frequency domain to determine phase noise sidebands directly. Experimental results have been matched well with theory, showing among other things, that phase noise improves with the quality factor ( $Q$ ) of the resonance squared.

The Leeson-Cutler phase noise model is based on a linear time variant (LTV) assumption for tuned LC tanks [73]. It predicts the following behaviour for phase noise as follows:

$$L\{\Delta\omega\} = 10 \log \left\{ \frac{2FkT}{P_s} \left[ 1 + \left( \frac{\omega_0}{2Q_L \Delta\omega} \right)^2 \right] \left( 1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|} \right) \right\} \quad (3.6)$$

where  $F$  is an empirical parameter (often called the “device excess noise number”),  $k$  is Boltzman’s constant,  $T$  is the absolute temperature,  $P_s$  is the average power dissipated in the resistive part of the tank,  $\omega_0$  is the oscillation frequency,  $Q_L$  is the effective quality factor of the tank with all the loadings in place (also known as loaded  $Q$ ),  $\Delta\omega$  is the offset from the carrier and  $\Delta\omega_{1/f^3}$  is the frequency of the corner between  $1/f^3$  and  $1/f^2$  regions which is shown in power spectrum of the oscillator in Figure 3.4. This model suggests that increasing  $Q$  and signal amplitude are ways to reduce phase noise. But for the factor  $F$ , without knowing precisely what it depends on, it is difficult to identify specific ways to reduce it. The same problem exists with  $\Delta\omega_{1/f^3}$  as well [50].

Another model for LC tuned oscillators use the LTI approach and there is an embedded assumption of no amplitude limiting, contrary to most practical cases. The general circuit diagram of an LC-tuned oscillator is shown in Figure 3.11.

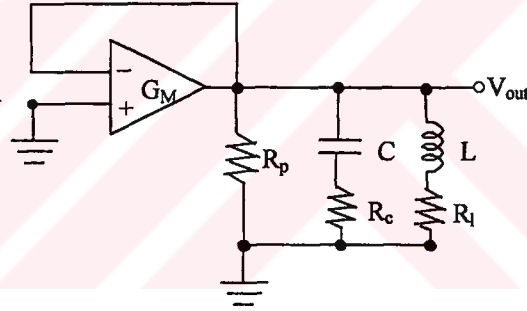


**Figure 3.11** General circuit diagram for an LC tune oscillator [11]

All parasitic resistances are included. The transconductance  $G_M$  implements a negative resistance to compensate for the losses in  $R_p$ ,  $R_l$ , and  $R_C$ . This model [51] predicts:

$$L\{\Delta\omega\} = 10\log \frac{kTR_{\text{eff}} \left[1 + A\right] \left(\frac{\omega_0}{\Delta\omega}\right)^2}{P_{\text{signal}}} \quad (3.7)$$

Here,  $R_{\text{eff}}$  is the total equivalent series resistance of the LC tank, given by

$$R_{\text{eff}} = R_l + R_C + \frac{1}{R_p (C\omega_0)^2} \quad (3.8)$$

$\omega_0$  is the oscillation frequency,  $\Delta\omega$  is the frequency offset from the carrier,  $P_{\text{signal}}$  is the power of the carrier signal.  $A$  is an empirical fitting parameter, also called the excess noise factor of the amplifier circuit of the oscillator [12]. This amplifier circuit is the negative- $G_m$  oscillator type that has NMOS amplifying transistors as shown in Figure 2.33. The examples of the different VCO designs where this model is used to calculate the phase noise are [11,12]. In these journals we can see that the measured phase noise values agree very well with the theoretical values. In the given equation (3.7), it shows that the inductors with a very low series resistance are required for low-phase-noise oscillators.

The calculations above are for the oscillators with a passive inductor. The oscillators employing active inductors have larger phase noise because of the noise generated by the active elements of the inductor. The same model predicts the phase noise with active inductor with the following equation

$$L\{\Delta\omega\} = 10 \log \frac{kTR_{\text{eff}} [1 + A + 2Q] \left( \frac{\omega_0}{\Delta\omega} \right)^2}{P_{\text{signal}}} \quad (3.9)$$

where  $Q=1/R_{\text{eff}}(\omega_0 C)$ . Compared to the phase noise equations for a passive inductor (Equation (3.7)), the factor  $[1+A]$  is now expanded with a term  $2Q$ . Since mostly  $Q$ -factors are large as possible are used, the last term will be dominant achieving a phase noise larger than passive inductor-implementations.

Another model is a linear, time varying (LTV) phase-noise theory, which is explained in [50]. There are two LC oscillator examples with comparison of theoretical and measured phase noise. Different studies on LC oscillator phase noise can be found in [52-54].

### 3.3.3 Ring Oscillator Phase Noise

The analysis of noise in ring oscillators is done with results for both time domain and frequency domain approaches. In this analysis, timing jitter is derived directly in the time domain, and a link is made back to the frequency domain to determine phase noise sidebands which result from device thermal noise in the inverter delay cells

which make up the ring. This translation will be shown to map well to the  $1/f^2$  region of the phase noise sidebands described in Section 3.3.1.

In addition to the time domain approach, phase noise in ring oscillators has also been investigated directly in the frequency domain. In the limit that a ring is oscillating at a high enough frequency that delay stages do not have a chance to fully switch, then a feedback model can be applied. It has been suggested that a ring oscillator is a feedback oscillator with an effective  $Q$  of one. A more detailed analysis, carried out by Razavi [6], defines  $Q$  in terms of the derivative of the phase angle function in a linearized version of the ring oscillator loop. Typical  $Q$ 's in this analysis are in the range of 1.3 to 1.4. In this work a three-stage ring oscillator VCO is used. To calculate phase noise, the signal path of the VCO is modelled with a linearized circuit as shown in Figure 3.12.

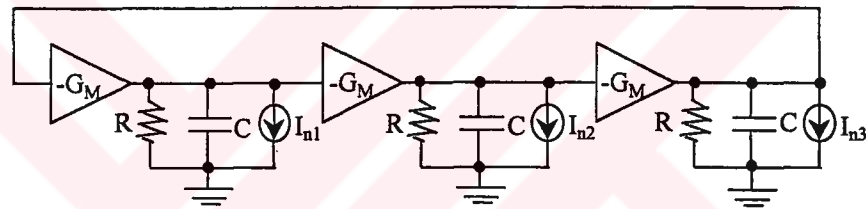


**Figure 3.12** Linearized of CMOS VCO [6]

$R$  and  $C$  represent the output resistance and load capacitance of each stage respectively. In this work, additive noise, high frequency multiplicative noise, low-frequency multiplicative noise, cyclostationary noise sources are calculated [6]. The choice of the number of the stages is also discussed. For the cases of interest in RF applications, a comparison is done with three-stage and four-stage ring oscillator. It is considered that both of them are designed to operate at the same frequency. Three observations are made during the simulations: 1) If four stage oscillator is to operate at the same speed as the three-stage VCO, the value of the  $R$  in the former must be approximately 60% of that the latter. 2) The  $Q$ 's of the two VCO's are roughly equal. 3) The total additive thermal noise of the two VCO's is about the same, because four-stage topology has more sources of noise, but with lower magnitudes.

As a conclusion, first, the phase noise depends on not only the  $Q$ , but also the number and the magnitude of sources of noise in the circuit. Secondly, four-stage

VCO's have no significant advantage over three stage VCO's, except for providing quadrature outputs.

Another study of ring oscillators is done for different type ring oscillators [14,50]. These are single-ended CMOS, differential CMOS and bipolar ring oscillators.

Starting with a single-ended CMOS ring oscillator with inverter delay cells which have equal-length NMOS and PMOS transistors. Assuming  $V_{TN} = |V_{TP}|$  and the thermal noise sources of different devices are uncorrelated and using  $N$  delay cells, the phase noise is modeled with the following formula

$$L\{\Delta f\} \approx \frac{8}{3\eta} \frac{kT}{P} \frac{V_{DD}}{V_{char}} \frac{f_0^2}{\Delta f^2} \quad (3.10)$$

where  $\eta$  is proportionality constant, which is typically close to one.  $V_{char}$  is the characteristic voltage of the device.  $P$  is the total power dissipation. From the equation, minimum phase noise is inversely proportional to the power dissipation and grows quadratically with the oscillator frequency. For a single-ended CMOS ring oscillator, phase noise is not dependent on the number of the stages.

For a differential CMOS ring oscillator with a resistive load, a differential pair is used for the delay cell and only the noise of the differential transistors and the load are taken into account. The expression for the phase noise of the differential MOS ring oscillator is

$$L_{min}\{\Delta f\} = \frac{8}{3\eta} N \frac{kT}{P} \left( \frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{tail}} \right) \frac{f_0^2}{\Delta f^2} \quad (3.11)$$

where  $N$  is the number of the stages and  $I_{tail}$  is the tail bias current of the differential pair. Note that in contrast with the single-ended ring oscillator, a differential oscillator does exhibit a phase noise dependency on the number of the stages, with the phase noise degrading as the number of the stages increases for a given frequency and power dissipation. For bipolar differential ring oscillator the same Equation (3.11) is used with the appropriate choice of  $V_{char}$ . In this study [55], many different ring oscillators are tested having different dimensions of transistors or different

number of stages. The measured results quite agree with the theoretical results. Other general theories and some examples on ring oscillators can be found in [56,57].

LC oscillators generally have better phase noise compared to ring oscillators for two reasons. First, a ring oscillator stores a certain amount of energy in the capacitors during every cycle and dissipates all the stored energy during the same cycle, while an LC resonator dissipates only  $2\pi/Q$  of the total energy during one cycle. Thus, for a given power dissipation in steady state, a ring oscillator suffers from a smaller maximum charge swing. Second, in a ring oscillator, the device noise is maximum during the transitions, which is the time where the sensitivity is largest. For ring-oscillator VCOs, however, there is freedom for the designer to change the current per stage,  $I_{SS}$ , over several orders of magnitude, allowing for a range of possible phase noise performance levels. Since device sizes are scaled with the current, this implies an increase in area as well. In some applications there are other reasons to increase the size and power consumption of the ring as well. In a PLL for instance, it makes sense that the VCO power budget is at least as high as for the other components of the system. Also, for applications where the VCO is called upon to drive mixers or sampling circuits with reasonably high capacitive loads, a larger VCO is favoured.

### 3.4 Varactors

The oscillation frequency of LC topologies is equal to  $f_{osc} = 1/(2\pi\sqrt{LC})$ , that only the inductor and capacitor values can be varied to tune the frequency. Other parameters such as biasing currents and transistor transconductances affect  $f_{osc}$  negligibly. Since it is difficult to vary the value of monolithic inductors, we simply change the tank capacitance to tune the oscillator. Voltage dependent capacitors are called “varactors”.

Varactors are an active research area for LC oscillator designers. The performance of the varactors effect very much on the phase noise and the tuning range of the oscillator. Varactor diodes, MOS varactors, inversion-mode, accumulation-mode MOS capacitors and gated MOS varactors are types of varactors.

### 3.4.1 Varactor Diodes

A reverse-biased pn junction can serve as a varactor. The voltage dependence is expressed as

$$C_{\text{var}} = \frac{C_0}{\left(1 + \frac{V_R}{\phi_B}\right)^m} \quad (3.12)$$

where  $C_0$  is the zero-bias voltage value,  $V_R$  is the reverse-bias voltage,  $\phi_B$  is the built-in potential of the junction, and  $m$  is a value typically between 0.3 and 0.4. This equation reveals an important drawback of LC oscillators: at low supply voltages,  $V_R$  has a very limited range, yielding a small range for  $C_{\text{var}}$  and hence for  $f_{\text{osc}}$ . To maximize the tuning range of the oscillator, constant capacitances in the tank must be minimized [35].

Remember the cross-coupled LC oscillator, which is explained in Section 2.3.6. The LC oscillator with varactor diodes is shown in Figure 3.13. To avoid forward biasing D1 and D2,  $V_{\text{cont}}$  must not exceed  $V_X$  or  $V_Y$  by more than a few hundred millivolts. Since the swings at X and Y are typically large, the capacitance of D1 and D2 varied with time. Nonetheless, the average value of the capacitance is still a function of  $V_{\text{cont}}$ , providing the tuning range [35].

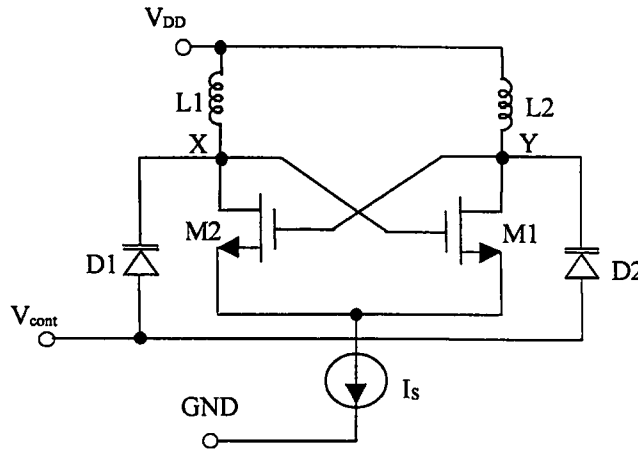


**Figure 3.13** LC oscillator using varactor diodes

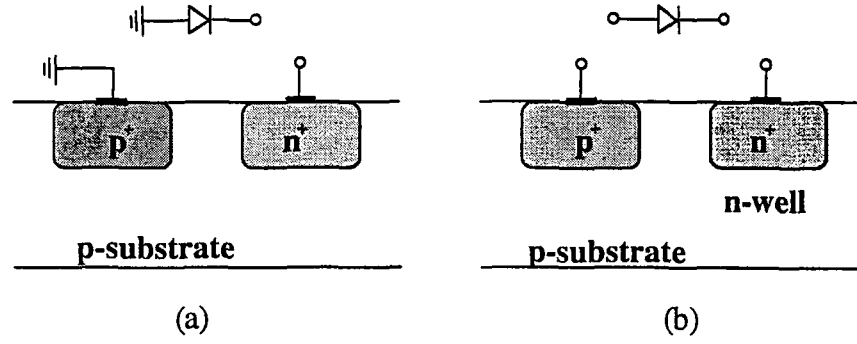


**Figure 3.14** Diodes realized in CMOS technology [35]

Varactor diodes can be realized in different technologies. Two varactor diodes realized in CMOS technology are shown in Figure 3.14. In Figure 3.14a, the anode is inevitably grounded whereas in Figure 3.14b, both terminals are floating. For the oscillator shown in Figure 3.13, only the floating diode can be used as the anode of the diode is connected to  $V_{\text{cont}}$  and the cathode is connected to node X or Y. But this structure suffers from a number of drawbacks. First n-well material has a high resistivity, creating a resistance in series with reverse-biased diode and lowering the quality factor of the capacitance. Second, the n-well displays substantial capacitance to the substrate, contributing a constant capacitance to the tank and limiting the tuning range. The diode is therefore represented as shown in Figure 3.15, where  $C_n$  represents the (voltage dependent) capacitance between the n-well and the substrate.

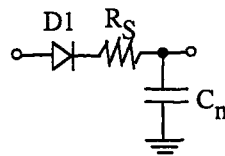


**Figure 3.15** Circuit model of the varactor diode shown in Figure 3.14b

In order to decrease the series resistance of the floating diode structure, the  $p^+$  region can be surrounded by an  $n^+$  ring so that the displacement current flowing through the junction capacitance sees a low resistance in all four directions.

There are different applications with varactor diodes for LC oscillators. Tunable junction capacitors is made as a  $p^+$  active area in an n-well [12,13,36]. Its capacitance can be tuned with the control voltage  $V_C$ , which controls the bias voltage of the n-well. Since this n-well is a common-mode node for D1 and D2, its parasitic

capacitance to substrate is not important. The performance of this diode type is explained in chapter 4 with its VCO design.

Another varactor diode type with CMOS technology is used for a symmetric implementation commonly used in the design of CMOS VCOs, which is explained in Chapter 4. In an N-tub CMOS process, the diodes are made of a  $p^+n\bar{n}^+$  lateral diffusion sequence where  $n^-$  is the doping level of the N-tub. Since N-tub has a high resistivity (about  $1K\Omega/\square$ ), the parasitic resistance introduced by the varactor diode is not negligible and may have severely affect the varactor's Q value [58]. The tuning characteristic of the VCO with diode varactor is shown in Figure 3.16.

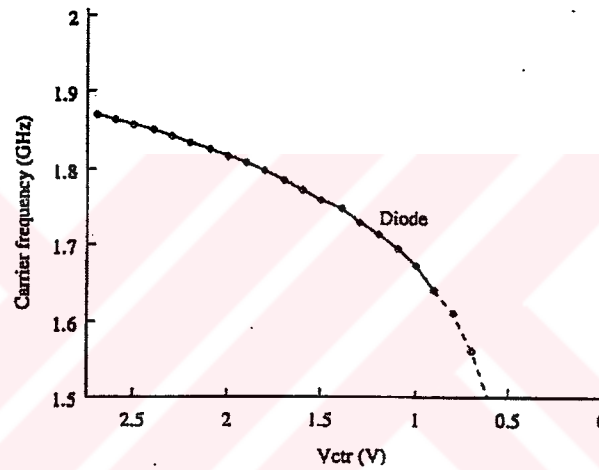


**Figure 3.16** Tuning characteristic of the VCO with diode varactor [58]

The varactor diodes can also be realized with bipolar IC technology. In a bipolar technology, a p-n junction type varactor is readily available, for example, by connecting the emitter to the base of the transistor and using the collector-base junction reverse biased. Alternatively the base-emitter junction can be used. Generally, the collector-base junction has a higher breakdown voltage than the base-emitter junction breakdown voltage. Figure 3.17 shows simulated capacitance curve of 20 NPN's in parallel with base and emitter short-emitter short-circuited [59]. The simulated capacitance ratio is 1.9 with reverse bias voltage  $V_{tune}$  varying from 0 to 5V.

More examples on varactor diodes will be given in next sections with MOS varactors.

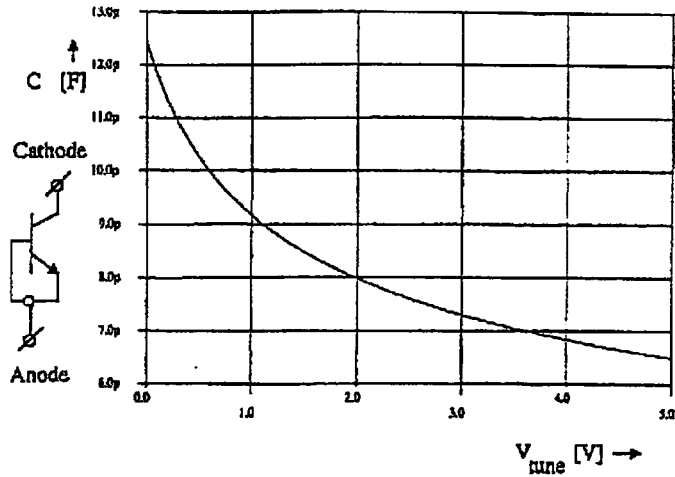


**Figure 3.17** Capacitance curve of the p-n junction varactor [59]

### 3.4.2 MOS Varactors

In any CMOS process, there is readily available capacitance tunable by voltage, which is the MOS transistor itself. It is well known that a MOS transistor with drain, source and bulk (D, S, B) connected together realizes an MOS capacitor with capacitance value dependent on the voltage  $V_{BG}$  between B (bulk) and G (gate). In the case of a pMOS capacitor, an inversion channel with mobile holes builds up for  $V_{BG} > |V_T|$ , where  $|V_T|$  is the threshold voltage of the transistor. The condition  $V_{BG} \gg |V_T|$  guarantees that the MOS capacitor works in the strong inversion, the region where the MOS device shows a transistor behaviour. On the other hand, for some voltage  $V_G > V_B$ , the MOS device enters the accumulation region, where the voltage at the interface between gate oxide and semiconductor is positive and high enough to allow electrons to move freely. Thus, in both strong inversion and accumulation region the value of the MOS capacitance  $C_{mos}$  is equal to  $C_{ox} = \epsilon_{ox} S / t_{ox}$ , where  $S$  and  $t_{ox}$  are the transistors channel area and the oxide thickness, respectively [60].

Three more regions can be distinguished for intermediate values of  $V_{BG}$ : moderate inversion, weak inversion and depletion. In these regions there are few or very few mobile charge carriers at the gate oxide interface, which causes a decreases of the capacitance  $C_{mos}$  of the MOS device.  $C_{mos}$  now can be modelled as  $C_{ox}$  in series with parallel of capacitances  $C_b$  and  $C_i$ .  $C_b$  accounts for the modulation of the depletion region below oxide, while  $C_i$  is related to the variation of the number of the holes at

the gate oxide interface. If  $C_b$  ( $C_i$ ) dominates, the MOS device is working in depletion (moderate inversion) region; if neither capacitance dominates, the MOS device is working in the weak inversion region. The behaviour of  $C_{mos}$  versus  $V_{BG}$  is reproduced qualitatively as shown in Figure 3.18 [60].

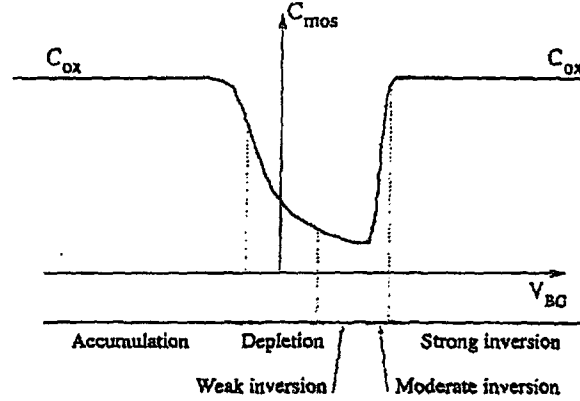


**Figure 3.18** Tuning characteristic for the pMOS varactor with  $B=D=S$  [60].

It should be noted that this figure shows  $C_{mos}$ - $V_{BG}$  characteristic for a very small  $v_{bg}$  signal superimposed on bias voltage  $V_{BG}$ . If the signal  $v_{bg}$  is large, as it happens in the VCO circuits, then the instantaneous value of the  $C_{mos}$  still varies with  $V_{BG}$  [60]. In Figure 3.19, a simulated capacitance curve of the pMOS varactor is shown [59]. The simulated device has a W/L of  $200\mu\text{m}/1.2\mu\text{m}$  and is built up with 20 devices in parallel. Hence the total width of the varactor is  $4000\mu\text{m}$ . The bulk is connected to the drain and source contact and forms the varactor cathode. The gate terminal acts as an anode. The performance of the VCOs which uses MOS varactors is explained in Chapter 4 [58,59,61]. In early researches like [58], it is believed that diode varactor shows a better performance than the MOS varactor, but in the next sections we will see that with different type of MOS varactors have better performance than diode varactors.

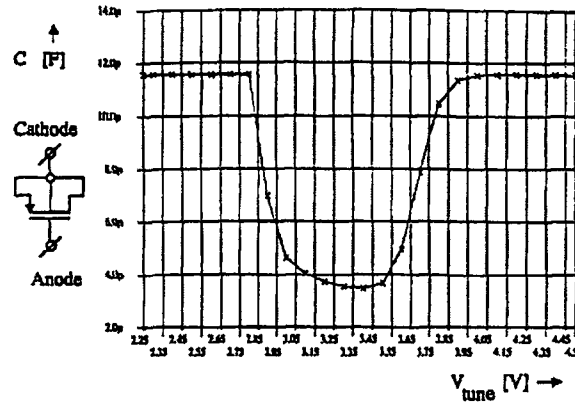


**Figure 3.19** Simulated capacitance curve of the pMOS varactor [59]

### 3.4.3 Inversion-Mode MOS varactor

In the section above, we have mentioned that when the signal at the transistor gate is large, then the instantaneous value of  $C_{mos}$  changes throughout the signal period. Although the average value of  $C_{mos}$  is still a function of  $V_{BG}$ , the tuning capability of the circuit is weakened by the nonmonotonicity of  $C_{mos}$ .

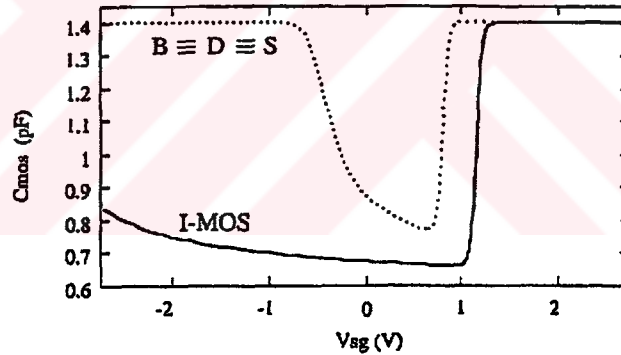


**Figure 3.20** Tuning characteristics for the inversion-mode MOS varactor [60].

One way to obtain an almost monotonic function for  $C_{mos}$  is by ensuring that the transistor does not enter the accumulation region for a very wide range of values of  $V_G$  [60]. This is accomplished by removing the connection between D-S and B, and connecting B to the highest dc-voltage available in the circuit (i.e., the power supply  $V_{DD}$ ). We call this topology as Inversion-mode MOS or I-MOS varactor. Figure 3.20 shows the comparison between the simulated  $C_{mos}$ - $V_{SG}$  characteristics of two equally sized pMOS capacitors designed in the CMOS process used in [60]. It is clear that the tuning range of the pMOS capacitor with  $V_B=V_{DD}$  is much wider than for the

pMOS capacitor with  $B \equiv D \equiv S$ , since the former capacitance is working in the strong, moderate or weak inversion region only and never enter the accumulation region. It should be noted that an equally large tuning range can be obtained with an nMOS capacitor floating D-S and grounded B, which is readily available in a p-substrate CMOS process. It is shown in [60] that I-MOS varactor VCO has less power consumption and than the diode varactor VCO has. The phase noise performance of the I-MOS VCO at high offset frequencies is lower than diode varactor VCO. The tuning performance of the I-MOS varactor VCO is nearly the same with the diode varactor, only the linear portion of the tuning characteristic of I-MOS is reduced compared to the diode varactor VCO [60].

#### 3.4.4 Accumulation mode MOS varactor

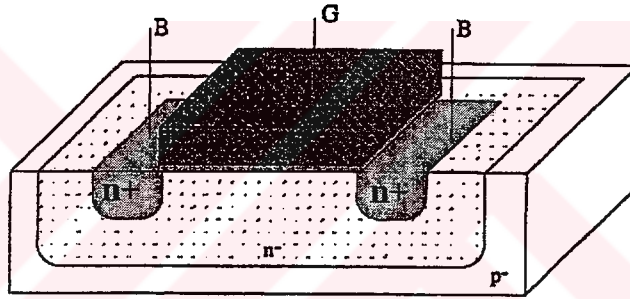


**Figure 3.21** Accumulation-mode MOS varactor [60]

Another attractive way is the use of pMOS device in the depletion and accumulation regions only [62]. This solution allows for implementation of a MOS capacitor with large tuning range ( $C_{mos}$  does not climb back to  $C_{ox}$  since there is no inversion regions), together with a lower parasitic resistance. To obtain an accumulation-mode MOS capacitor, we must make sure that the formation of the strong, moderate and weak inversion regions is inhibited, which requires the suppression of any injection holes in the MOS channel. This can be accomplished with the removal of the D-S diffusions ( $p^+$ doped) from the MOS device (since we are dealing with circuits working at high frequencies, we do not need to worry about thermal generation of the hole-electron pairs). At the same time, we can implement the bulk contacts ( $n^+$ ) in the place left by D-S, as shown in Figure 3.21, which minimizes the parasitic n-well resistance of the device. The tuning characteristic of the A-MOS capacitor is shown in Figure 3.22, compared with that of the pMOS capacitor with  $B \equiv D \equiv S$ .

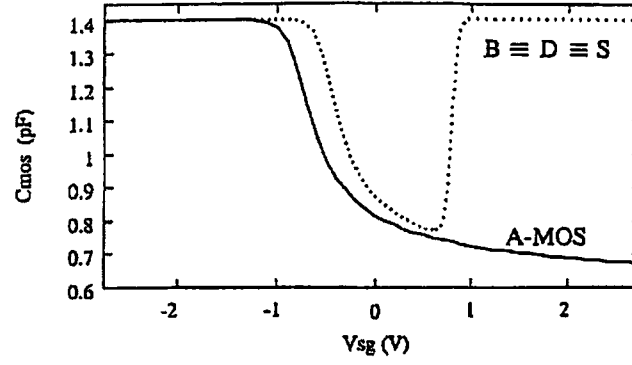


**Figure 3.22** Tuning characteristic for the accumulation mode varactor [60]

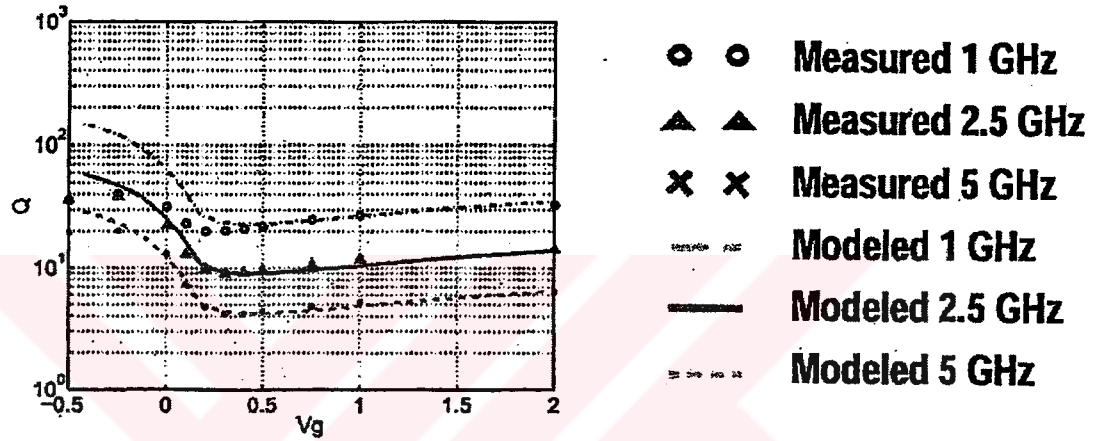


**Figure 3.23** Measured Q factor of accumulation MOS varactors presented in [62]

In the first study of accumulation MOS varactor in [62] the Q of the capacitance is modelled and measured for different frequencies as shown in Figure 3.23. Q reaches minimum at flatband voltage where changes in capacitance is large, so there is a trade-off between Q and capacitance tuning. The tuning range is calculated as

$$TR = \frac{2C_{ox}}{C_{ox} + 2C_{Si,min}} \quad (3.13)$$

where this value is 200% at the maximum limit.  $C_{Si,min}$  is the minimum semiconductor capacitance. As technology scales tuning range increases towards the limit.

In the study of [60] with different type of varactors, accumulation MOS varactor VCO has the minimum power consumption as shown in Figure 3.24. Phase noise of

the accumulation MOS (A-MOS) varactor VCO is better at high offset frequencies. The detailed results for these VCOs is given in Chapter 4.

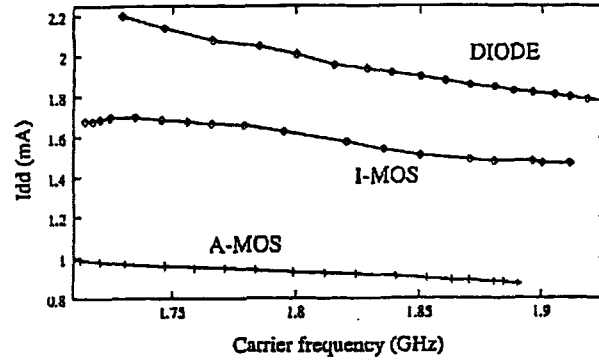


**Figure 3.24** Minimum current consumption for the diode varactor VCO, I-MOS varactor VCO, and A-MOS varactor VCO [60].

Another study for accumulation MOS varactors is based on a polysilicon-oxide-nwell structure. The varactor is realized in a standard CMOS process, by changing the surface population from the accumulation to depletion. With technology scaling, the oxide thickness is reduced and correspondingly the oxide capacitance is increased. Scaled technologies enable to realize polysilicon oxide semiconductor varactors with better quality factors because the parasitic resistance scales with channel length. In Figure 3.25 the cross-section of the device is shown. The polysilicon gate and the two  $n^+$  contacts inside the n-well are the controlling electrodes. By applying a positive voltage between the polysilicon and the n-well the surface is accumulated and the device capacitance equals the oxide capacitance. If the applied voltage is reverse, the surface layer is depleted and the device capacitance decreases. With technology scaling, the quality factor increases. The varactor is realized in  $0.35\mu\text{m}$  standard CMOS process. The change of the capacitor and the quality factor with the bias voltage at  $1800\text{MHz}$  is shown in Figure 3.26. The capacitance changes from about  $1.7\text{pF}$  (when the surface is depleted) to  $3.5\text{pF}$  (when it is accumulated). The quality factor changes from 17 (corresponding to the large capacitance, accumulation) to 33 (corresponding to the small capacitance). 30% tuning range is achieved for a variation of the tuning voltage of  $2\text{V}$  [63].

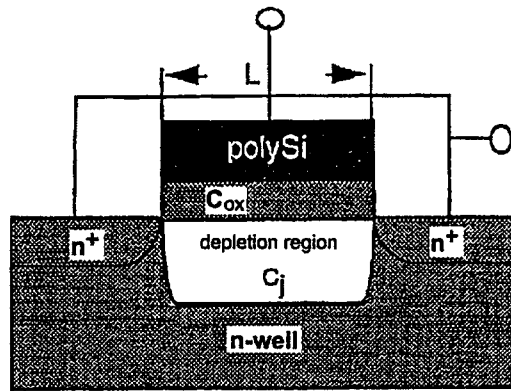


**Figure 3.25** Polysilicon oxide silicon varactor: cross section [63]

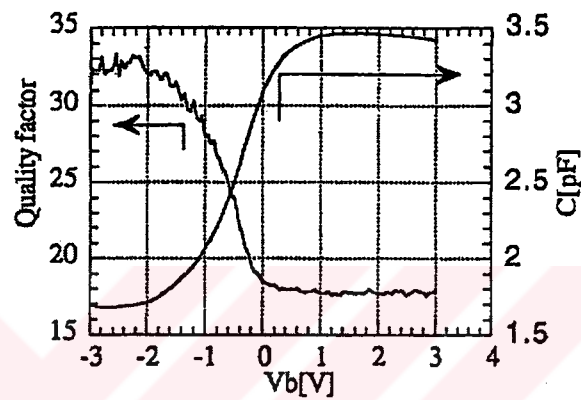


**Figure 3.26** Measured capacitance and quality factor at 1800MHz [63].

### 3.4.5 Gated MOS varactor

The accumulation-mode MOS varactor can theoretically achieve quite high quality factor. In [64] it is said that the maximum capacitance variation of the accumulation mode varactor is limited to the difference between  $C_{ox}$  and minimum depletion capacitance. And the sensitivity is limited by the classic capacitance-voltage (C-V) characteristics of the MOS device. The gated varactor achieves wider tuning range than the accumulation MOS varactor. The cross-sectional view of the varactor is shown in Figure 3.27 [65].

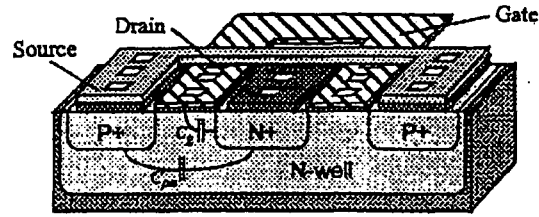


**Figure 3.27** Cross-section of the P-type (N-body) gated varactor.  $V_d$  and  $V_g$  are the bias voltage applied to the “Drain” and “Gate” respectively [65].

The structure of the varactor is similar to a p-channel MOS transistor with the drain replaces by an N+ region. This varactor is a three-terminal device rather than two-terminal devices as in conventional varactor. The gate capacitance  $C_g$  and the lateral junction capacitance  $C_{pn}$  make up the total capacitance. Varying the drain voltage and the gate voltage can vary the total capacitance measured at the drain. When the applied voltage  $V_g$  is far above the flatband voltage  $V_{FB}$ , the silicon surface of the n-region under the gate is accumulated with electrons provided by the n+ region and the capacitance  $C_g$  is at a maximum at drain voltage  $V_d=0V$ . The total capacitance ( $C_{max}$ ) is equal to the gate oxide capacitance plus the drain/source junction capacitance. The  $C_{max}$  of the gated varactor is larger than the  $C_{max}$  of the accumulation mode varactor, which is essentially the gate oxide capacitance. When the gate is grounded and a positive voltage is applied at the drain, an inversion layer is formed beneath the gate and the region under the channel is further depleted by the drain due to the subsurface DIBL effect. As a result, the depletion region can extend further than accumulation-mode varactor and hence achieving a minimum capacitance less than that of the accumulation-mode varactor.

A plot of capacitance value versus the biasing voltages of a gated varactor, which is implemented in 0.35 $\mu m$  CMOS technology, is shown in Figure 3.28 [65].

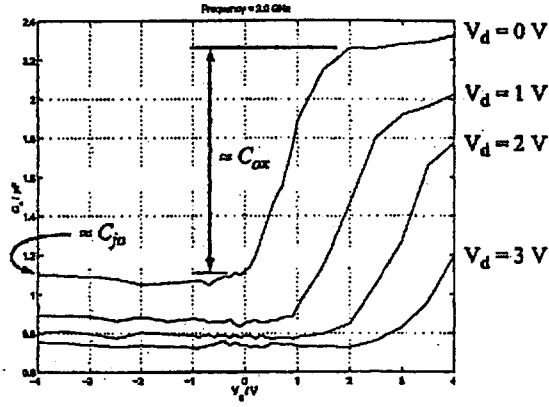


**Figure 3.28** The C-V characteristic of the gated varactors versus gate voltage  $V_g$  at various  $V_d$ .  $C_{ox}$  is the gate oxide capacitance and  $C_{j0}$  is the zero-bias junction capacitance [65].

The capacitance of the varactor increases from 0.8pF to 2.25pF as the gate/drain voltage varies 0V to 2V. The variation covers 90% of the tuning range. This allows the varactor to be used in low voltage VCO. Wide tuning range VCO can be achieved without increasing the power supply voltage. The maximum quality factor of the varactor is measured to be 22 at 2GHz.

### 3.5 Inductors

Integrated inductors are also a big research area like varactors, but unlike them, inductors are not readily available in a standard process. In this section we will discuss about active inductors and passive inductors like bondwires and different type of spiral inductors. We will mention about their quality factor value, which is a key design point for a low phase noise VCO. The total performance of the VCOs with different inductor types is explained in Chapter 4.

#### 3.5.1 Active inductors

An often-used way to integrate an inductor is to simulate one with active elements. These active elements can modify the impedance of a capacitor such that the input impedance of the circuit resembles that of an inductor. In general, a gyrator and a capacitor are required which is shown in Figure 3.29. The equivalent inductance can easily be calculated as [11]:

$$L_{eq} = \frac{C_L}{g_{mi}g_{mv}} \quad (3.14)$$

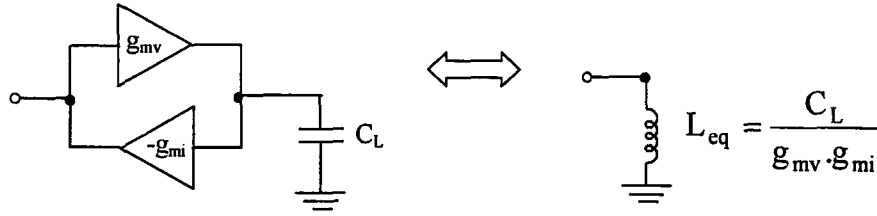


**Figure 3.29** A gyrator based active inductor circuit diagram [11]

Practical realizations of this structure can achieve very high speeds. A GaAs implementation [66] has proven to be able to operate up to the cut-off frequency of a single transistor. Therefore, submicron CMOS active inductors are possible at 1 or 2GHz. Apart from that, an active inductor has the advantage that it is tunable, which allows an easy realization of a tunable oscillator. The biggest problem associated with active inductors is their noise contribution to the circuit. The noise is generated by both transconductors in the gyrator. The phase noise model of the VCO with an active inductor is discussed in Section 3.3.2. The noise sources effect very badly to the phase noise of the VCO. Therefore, passive implementations of integrated passive inductors are necessary.

### 3.5.2 Bondwire Inductors

From phase noise calculations in the previous sections, clearly the best inductor for low-phase-noise oscillator is a passive inductor with a series resistance as low as possible. Since the bonding process is a standard step in the fabrication of ICs, bondwire inductors can be regarded as being a standard passive element of a silicon CMOS technology. Normally a bonding wire connects a pad of the IC to a pin package. A rule of thumb for the inductance associate with this connection is 1nH per mm length. So, the inductance values of several nH can be realized. In combination with 4pF capacitor, only 6nH is needed to create an LC tank oscillating at 1GHz. The series resistance of the bondwire is very low, so high quality factors can be accomplished. Also the parasitic capacitance to the substrate is limited to the capacitance of two bondpads, so the self-resonance frequency will be high [36].

A differential bondwire inductor is shown in Figure 3.30. Some first order formulas to calculate the inductance value, are [67]:

$$L = \frac{l}{5} \left[ \ln \left( \frac{2l}{r} \right) - 0.75 + \frac{r}{l} \right] \quad (3.15)$$

$$M = \frac{l}{5} \left[ \ln \left( \frac{l}{d} + \sqrt{1 + \left( \frac{l}{d} \right)^2} \right) - \sqrt{1 + \left( \frac{d}{l} \right)^2} + \frac{d}{l} \right] \quad (3.16)$$

where  $L$  is the self inductance in nH of one conductor,  $M$  is the mutual inductance in nH between the two conductors,  $l$  is the conductor length in mm,  $r$  is the radius of the cross section in mm and  $d$  is the distance between the two conductors in mm [36].

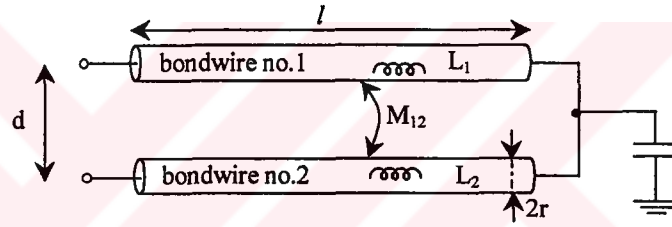


**Figure 3.30** Differential bondwire inductor [36]

Since we want to predict the inductance value as correctly as possible, the length of bondwires must be controlled accurately. This can be done using chip-to-chip bonds. Real bondwires, however, are never straight conductors, and the actual inductance value will differ from the one calculated with the equations (3.15) and (3.16). This is due to several uncertainties in the fabrication of bondwire inductors. These are explained in [11]. When the variation of bondwire parameters are calculated, it has been found that the final inductance value to be within 6% of the expected value [11]. This is very acceptable for LC-tuned oscillators, since there will always be a larger uncertainty on the requested capacitor value. For tunability, junction capacitors are required. The variation on their capacitance value is even worse, e.g., a MOS drain or source capacitance can vary  $\pm 20\%$ . This shows that the deviation in the oscillation frequency from the expected value will be mostly due to an incorrect capacitance value.

When the inductor is used differentially, the internal node will be a common mode node, and the parasitic effect of the bondpads and that end of the bondwire will not be important. So the only parasitic capacitance is the one from the two bondpads at the beginning of the bondwires. A bondpad can be modeled by a capacitor in series with the resistance of the substrate. This is shown in Figure 3.31.

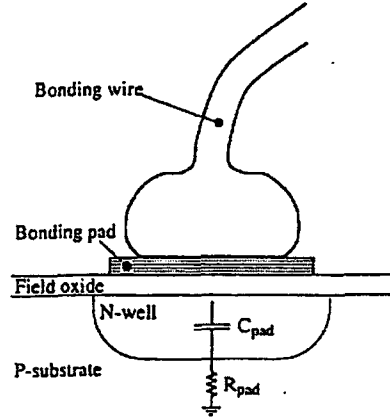


**Figure 3.31** Parasitic elements of the bonding pad[36]

Typical values for these parasitic are estimated to be 400fF for  $C_{pad}$  and  $20\Omega$  for  $R_{pad}$ . The series resistance will increase the losses in the LC-tank, but its effect can be small when a larger capacitor is placed in parallel with the bondpad. The parasitic capacitance determines the self-resonant frequency of the inductor. For a differential bondwire inductor as in Figure 3.30, the two-bondpad capacitors are placed in series, so the resulting parallel capacitance is typically 200fF. With an inductance value of e.g., 5nH, this yields a self-resonant frequency of 5GHz. However, at high frequencies, the skin effect becomes important.

An LC-tank is designed for 1.8GHz VCO. In Figure 3.32 it is shown that two inductors and two capacitors are used. The LC-tank is implemented using bondwire inductors as shown in Figure 3.33. Four bondwires (two per inductor) are used. Their placement next to each other causes them to interact, an effect that was accounted for by incorporating the appropriate mutual inductances in the simulations. Because of the interaction, the effect of the horizontal bends in the bondwires is not as severe as was calculated in Equations (3.15), (3.16). If one of the mutual inductances increases because of the smaller spacing, another will decrease [11].

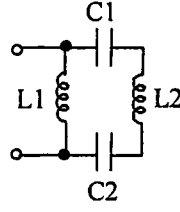


**Figure 3.32** Low-voltage enhanced LC-tank circuit

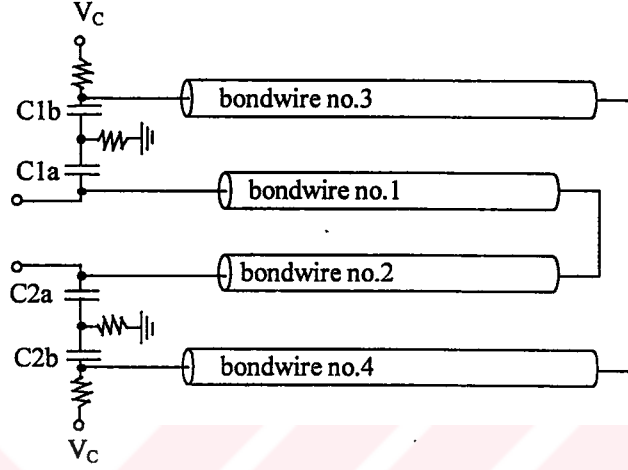


**Figure 3.33** Low-voltage enhanced LC-tank bondwire implementation [11]

The capacitors are realized as the series connection of two capacitors. The first one (C1a and C2a) is a Metal1/Metal2 capacitor and shifts the dc-voltage at the internal node to ground. The other capacitors (C1b and C2b) are varactor diodes, which are  $p^+/n$ -well junction capacitors. The advantage of this type of LC-tank is the branch of having only one inductor (L1). This makes it possible to develop a simple transconductor, since the tank's impedance at low frequencies is zero. The total performance of the VCO is given in chapter 4 with this LC-tank.

Bondwire inductor is also used in a 1.8GHz VCO design [60], which the design is especially done to test different type of varactors. Since the objective of the work is to make the behaviour of the VCO's sensitive to the respective varactor, it is necessary to design the VCO's in a way that guarantees that the parasitic resistance of the varactors dominate the performance of the VCO's. This condition rules out the use of monolithic spiral inductor in favour of on-chip bondwire inductors as they have higher Q value.

More examples on bondwire inductance are in the next section with spiral inductors.

### 3.5.3 Spiral Inductors

Spiral inductor is more normal type of integrated inductor than the bondwire inductor. For the designer, it is easier to use a spiral metal track laid out in the standard metal routing levels of the IC as an inductor. If the required specifications can be achieved with this technique, the cost will certainly be lower than a design using bonding wire inductors. The die area can be reduced by an order of magnitude, and the variations in inductance value due to the non-uniform bonding are of course no longer present. Once the processing masks are made, the inductor geometry will always be the same, since the processing accuracy ( $<0.1\mu\text{m}$ ) is certainly negligible with respect to the size of the coil ( $\approx 100\mu\text{m}$ ).

Although the spiral inductor solution is smarter than the bonding-wire design, it has some major drawbacks. A lot of parasitics limit the quality of the inductors, which has led many designers to the use of special processing techniques to enhance their performance. To decrease the series resistance, multi-level and extra thick metallization are used. And to eliminate the self-resonance with parasitic capacitance to the substrate, this substrate is etched away underneath the inductor [36].

Spiral inductors consist of a rectangular spiral metal track on the silicon substrate, using one or more of the standard metal interconnection levels available as shown in Figure 3.34a. The basics for the inductance calculation of these spiral inductors were developed by Greenhouse [67]. If the technology allows 45-degree routing, an octagonal shape can be used as shown in Figure 3.34b.

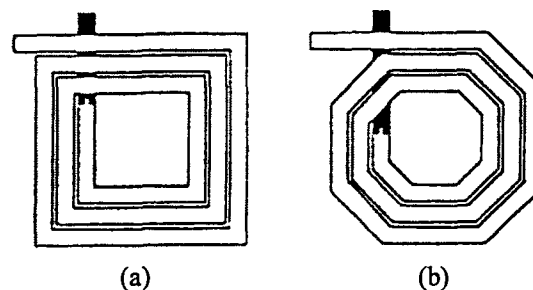


**Figure 3.34** Spiral inductor layout (a) Square (b) Octagonal

The series resistance of the metal tracks will limit the quality factor of the inductor. Typical values in a simple process are  $15\Omega$  for a  $10\text{nH}$  inductor [68].

One of the most recognized parasitics is the capacitance to the substrate. Together with the wanted inductance, this gives an LC resonance frequency above which the coil can no longer be used as an inductor. A typical value for the self-resonance frequency is 2.5GHz for a 10nH inductor [68]. This puts a limit on the maximal inductance value achievable at a certain frequency, as larger inductors require a larger area and thus also a larger capacitance and a smaller self-resonance frequency. Special processing technologies exist that create an air-gap underneath the inductor, or have very thick oxide under their top metal routing [69]. The resulting smaller parasitic capacitance allows higher operation frequencies.

Another solution for the self-resonance problem has been developed. By using selective etching techniques, the silicon substrate can be removed in a post-processing step from the underneath the inductor, either by etching from the top of the wafer or from the back of the wafer. This removes the capacitance to the substrate and shifts the self resonance frequency of a 100nH inductor from 0.8GHz to 3GHz[70]. But more important this technique also eliminates the resistive losses in the substrate. However, this requires extra non-standard processing steps.

A general reference for the calculations of the spiral inductors is [67]. A method to accurately calculate the inductance value that is based summing/subtracting the appropriate self and mutual inductance values of different segment of the coil. The basic formula for the exact self-inductance of a straight conductor is

$$L = \frac{l}{5} \left[ \ln \left( \frac{2l}{\text{GMD}} \right) - 1.25 + \frac{\text{AMD}}{l} + \frac{\mu_r}{4} T \right] \quad (3.17)$$

where  $L$  is the self inductance in nH,  $l$  is the conductor length in mm, GMD and AMD are the geometric and arithmetic mean distances, respectively of the conductor cross section in mm,  $\mu_r$  is the relative permeability of the conductor, and  $T$  is a frequency correcting parameter. The geometric mean distance (GMD) between two conductors is the distance between two infinitely thin imaginary filaments whose mutual inductance is equal to the mutual inductance between the two original conductors. By definition, self-inductance of a conductor is the sum of all the mutual inductances of all pairs of filaments of which it is composed. The arithmetic mean distance (AMD) is the average of all the distances between the points of one

conductor and the points of another. The further calculations are explained in [67]. Another type of model is given in [71] where some of the parameters are a functions of the geometry of the inductor.

The biggest problem of this first-order inductor model is the fact that it does not take into account all parasitics of the inductor when this one is used at high frequencies on a conductive silicon substrate.

As we have mentioned before spiral inductors suffer from three parasitic effects. First, parasitic capacitance to the substrate causes the inductor to self-resonate at a certain frequency. Second, the high frequency series resistance will differ from the calculated one due to the skin effect and other magnetic field effects. Third, the losses in the heavily doped substrate cause a large degradation in the overall quality factor reduce the inductance value.

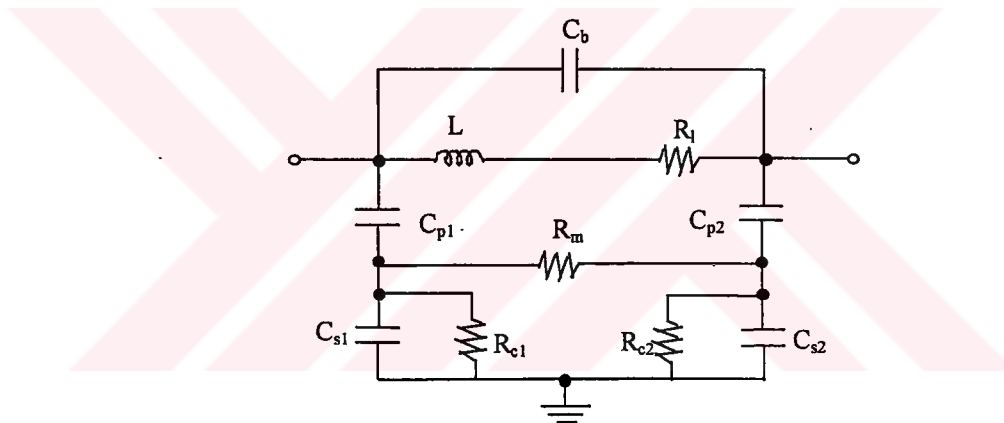


**Figure 3.35** Equivalent circuit of a spiral inductor [36]

Generally spiral inductors can be modelled as shown in Figure 3.35. The inductance  $L$ , the series resistance  $R_l$ , the parasitic capacitance  $C_p$ , and its associated resistance  $R_c$  are modeled as a function of the coil area, conductor width and spacing, area efficiency, frequency etc. In the frequency range up to 3GHz, the accuracy of the model is 10% for the inductance value and 40% for the series resistance. This model is used especially for low  $Q$  applications. In oscillator design however, high  $Q$  inductors are needed and a 30% accuracy in resistive losses is certainly unacceptable. So for VCO inductors, the optimum inductor must be chosen on a trial-and-error basis.

Many studies are made on spiral inductor for different technologies. In [72] the spiral inductors are categorized according to their shape. First one is the square spiral inductor which is shown in Figure 3.36 with a layout of eight-turn spiral. This is the most common type in Si RF ICs. Second is the polygon spiral inductor. Since polygon spirals with more than four sides have higher Q than square spirals (for the same area), it is advantageous to use these structures. The chip layout of a sample polygon spiral is shown in Figure 3.37. Third type is the multimetal spiral inductor, where metal layers placed in shunt metals to improve the low frequency Q of the spiral.

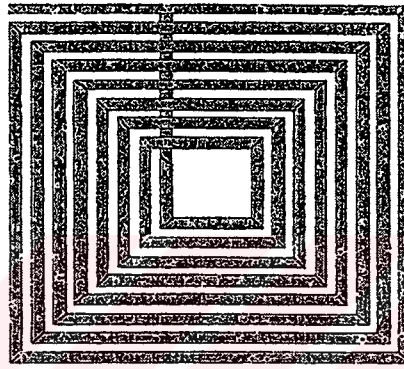


**Figure 3.36** Layout of eight-turn square spiral [72]

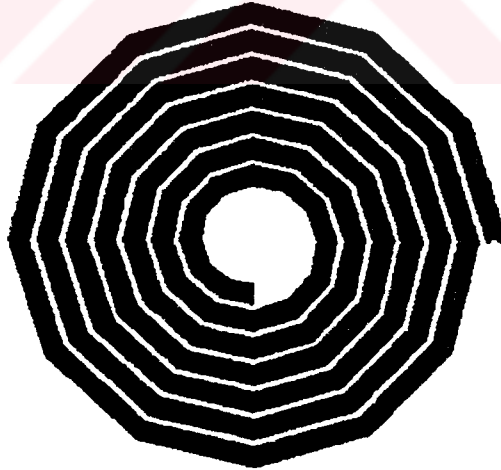


**Figure 3.37** Layout of polygon spiral inductor [72]

The spiral inductors are fabricated in SiGe bipolar process for high Q values in [73]. The lumped element model for the 1.45nH inductor is shown in Figure 3.38. L is the ideal inductance, a series resistance  $R_{cd} + R_{ac}$ , and a capacitance  $C_p$ , describes the spiral coil of the inductor. The effect of the lossy silicon substrate as a parasitic RF

signal path is represented by oxide capacitances  $C_{ox}$  and substrate resistances  $R_B$ . Figure 3.39 shows the measured and simulated characteristics of the 1.45nH inductor in comparison. The results show that the agreement between data and model is excellent in spite of the simplicity of the model [73]. Different methods for quality factor estimation can be found in [74].

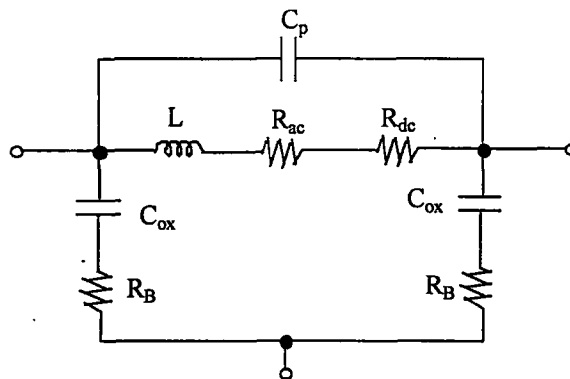


**Figure 3.38** Lumped-element model with values representing the 1.45nH inductor [73].

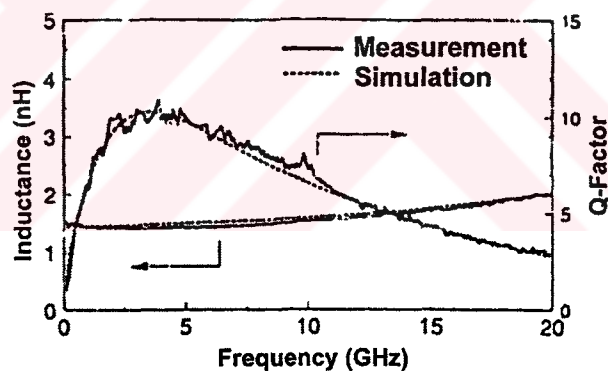


**Figure 3.39** Comparison of the measured and simulated characteristic of the 1.45nH inductor in Fig.3.38 [73].

A LC VCO has been designed with 0.7 $\mu$ m CMOS process with spiral inductor [12]. The technology is a standard double metal CMOS with heavily doped substrate without any extra processing step. The losses of the coil must be as low as possible for low noise and low power. The size of the inductance is also an important subject for the design. If the inductance is too small, then this will require a large capacitance to set the desired frequency and hence large power consumption will result. The inductance value can not be higher either than the required capacitance value will be almost achieved with parasitics of the coil and the amplifying transistors alone. This leaves no room for an extra tunable junction capacitance, so the tuning range will be

small. In this design, an octagonal shape of coil is used. The size of the octagon is chosen such that the average radius is  $85\mu\text{m}$ . Two coils are used in series. The calculated inductance value is  $3.2\text{nH}$  and the  $Q$  is  $5.7$ . The overall performance of the VCO is given in Chapter 4.

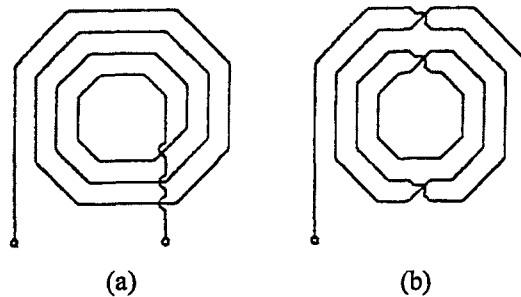


**Figure 3.40** Spiral inductor coil shape (a) standard octagonal (b) symmetrical [13]

Another  $1.8\text{GHz}$  VCO is designed on lowly doped substrate  $0.4\mu\text{m}$  CMOS process [13]. It is said that the optimum VCO design should include only one coil in the inductor. The developed coil shape is shown in Figure 3.40. Instead of drawing a normal spiral track, and then making the connection to the inner turn in a different metalization level, the metal track now moves outside again every half turn, until the centre is reached and then moves outside again every half turn. Both metal1 and metal 2 routing levels are used, except for the cross sections, which use of course only one metal level for each direction. The number of cross sections is equal for both shapes, so this new shape has no effect on the DC resistance. This coil is completely symmetrical and can thus be used as a differential floating inductor. A disadvantage of this coil is the fact that no common mode point is the innermost turn and is difficult to reach from outside, because both metalization levels are already used. One aspect of the symmetrical coil shape is the fringing capacitance between the segments. In a standard spiral coil with a certain number of turns, the voltage between the outer track and the one next to that is not so big. So the voltage swing across the fringing capacitance is limited, and it will have a little effect on the total parasitic capacitance of the coil. But in symmetrical coil almost the complete voltage swing stands across these adjacent segments. The fringing capacitance will therefore become more important and its effect must be incorporated in the simulations. Since the lumped equivalent circuit model of Figure 3.35, is no longer sufficient, a more accurate model is shown in Figure 3.41. The coil split up in segments that each

represents one half turn. Those segments are modeled as seven-terminal devices as shown in Figure 3.41b. The first two terminals are the normal ones, i.e. both ends of the useful inductor, and are indicated with a round shape. The inductance value  $L$  is split up in four parts, the series resistance  $R_l$ , in three parts. At the two intermediate nodes that appear in this way the parasitic capacitance are connected. There is of course the capacitance to the substrate  $C_p$ , and its associated resistance  $R_c$ . they are connected to the third terminal of the segment, i.e. the substrate connection. The four other terminals are used to connect the fringing capacitance  $C_f$  to the adjacent segments and are indicated with the square shape. The calculated inductance value of the coil is 2.8nH and the quality factor is 8.6. [36]

The overall performance of the VCO is given in Chapter 4. The symmetrical coil is also used in our design of the quadrature LC VCO as explained in Chapter 5.

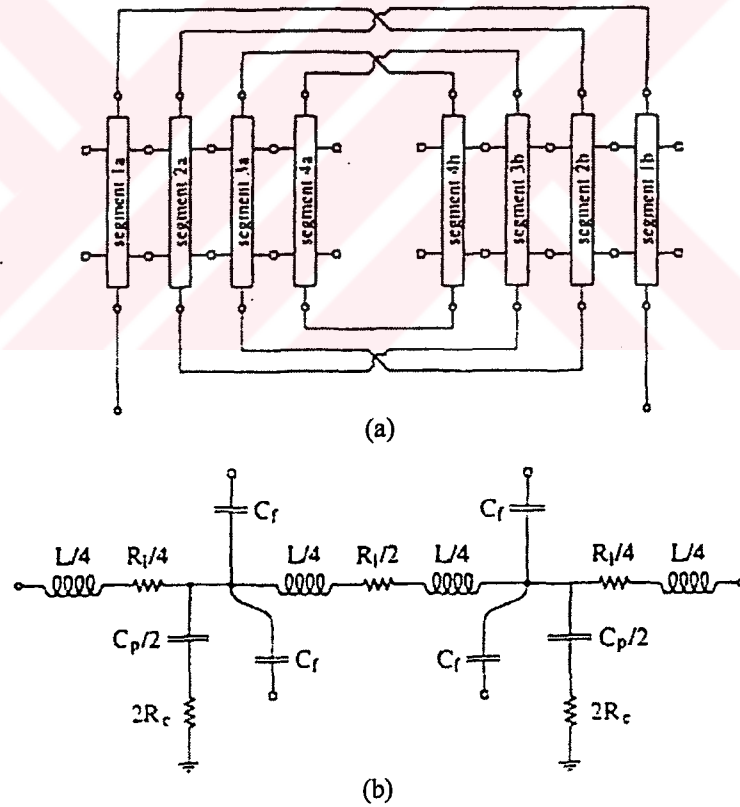


**Figure 3.41** (a) Equivalent circuit model for symmetrical octagonal coil; (b) Model of a single segment [36].

## **4. REVIEW OF THE ON CHIP RF VCO CIRCUITS**

This chapter covers the design of LC, ring VCOs and method of quadrature signal generation. In chapter 2, different types of RF oscillator are given. But in this Chapter we will mention about LC and ring VCO because in last years there is a big search area for these VCOs as the modern telecommunication systems rise. And to build a low-power, low-phase noise VCOs, is a major importance.

Different LC topologies are discussed which are designed with different type of varactors and inductors. In Chapter 2, the performance of the different varactors and inductors are given but in chapter we will see the effect of these devices to the overall performance of the LC VCO. Following the LC VCOs, different types of ring VCOs are given. The quadrature signal generation of RF VCOs is explained with four different methods and these methods are compared with each other.

### **4.1 RF VCOs**

In this part we will discuss about LC and ring VCO topologies from 90's until today.

#### **4.1.1 LC VCOs**

There are many types of LC VCOs, but here we categorize them into three parts like negative- $G_m$  LC VCOs, source-coupled LC VCO and Clapp configuration VCO. More examples are given for negative- $G_m$  VCO, as it is more preferred. A comparison of the VCOs is also give at the end of the section.

##### **4.1.1.1 Negative- $G_m$ LC VCOs**

The definition of negative- $G_m$  oscillator is first given in Section 2.3.6. In this section, different negative- $G_m$  oscillators are given, with different inductor and varactor types. Their performances are compared with each other.

VCO (1): The first example circuit of the negative- $G_m$  oscillator is shown in Figure 4.1. This VCO have been designed for low power and low phase noise applications using on-chip inductors for 1.8GHz standard with 0.7 $\mu$ m CMOS process [11]. The enhanced LC tank is implemented using bondwire inductors, which is explained in Chapter 3, satisfying noise reduction.

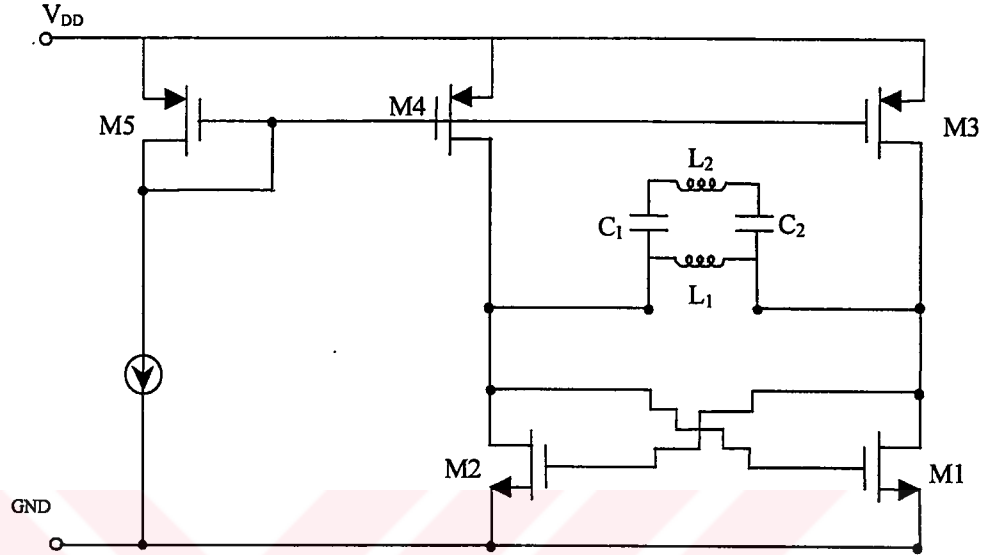


**Figure 4.1** Simple Diagram of the VCO [11]

The schematic of the VCO is given with the biasing part. Here the PMOS transistors are current sources so the amplification is done with two NMOS transistors. The biasing points of NMOS transistors are very important for the oscillation amplitude and phase noise performance of the circuit. So the gate voltages of the NMOS transistors are chosen as half of the power supply.

The measured center frequency of the VCO is 1.76GHz. The phase noise at 200kHz-carrier frequency is -115dBc/Hz. When the tuning voltage is changed from 0 to 10 V, the oscillation frequency changes from 1.68GHz to 1.8GHz. The tuning range is 4.5% for tuning up to 3V and almost 7% for tuning voltages up to 10V.

VCO (2): In academic research, we can see different type of VCOs for different frequencies, some of these researches depend on the industrial system specs like GSM, DCS-1800. An improved version of the first VCO has been designed by using the same amplifier circuit topology in Figure 4.1. In this design integrated planar inductors are used in LC tank instead of bondwire topology [12]. The main goal of

this design is especially to prove the feasibility of planar inductors in standard CMOS design. The simplified schematic of the VCO is shown in Figure 4.2. This type of inductor is already explained in Chapter 3. Two of the hollow inductors are used in series in differential configuration. The capacitor of the LC tank is formed by the inductor's parasitic capacitance to the substrate, the drain-bulk, gate-drain and gate-source capacitances of the NMOS transistors and a tunable capacitor. The tunable capacitor is a p+/n-well diode varactor, which is explained in Chapter 3. The biasing point and the dimension of the transistors are chosen in order to satisfy the total capacitance on each node to obtain the oscillation frequency 1.8GHz. For this target the inductance value should be 3.2nH and total node capacitance should be 2.4pF. In theory, the phase noise at 600kHz offset frequency is calculated -115.6dBc/Hz.

The measured free running oscillation frequency of the chip is 1.81GHz. The phase noise at 600kHz offset frequency is found -116dBc/Hz, which is the same with theoretical value. The tuning voltage changes between 0.5V and 3V. The tuning range is %14 [12].

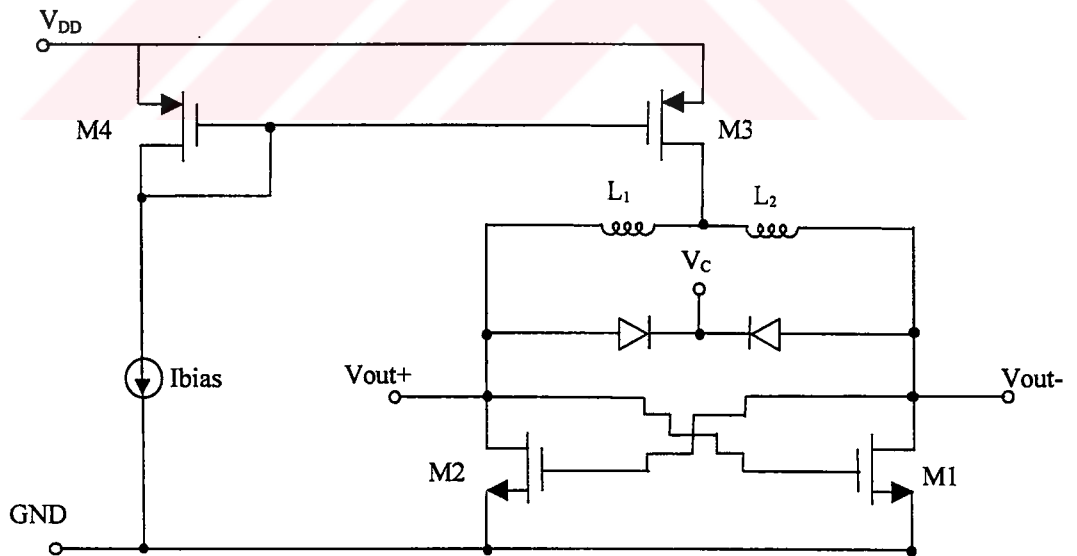


**Figure 4.2** Oscillator Circuit Schematic presented in [12]

It is also claimed that although only two layered CMOS technology is used, which is the worst technology to design a VCO, the results are satisfying [12].

VCO (3): Another 5GHz CMOS VCO is designed also for wireless applications using the same circuit schematic in Figure 4.2. The centre frequency is measure 4.7GHz. For a 0.7V – 2.7V tune voltage range a 200MHz or %4.3 tuning range is available. The phase noise at 100kHz offset frequency is –90dBc/Hz and for 1MHz offset frequency it is –110dBc/Hz [75].

VCO (4): As 1GHz is very near to GSM system operating frequency, many research designs are made around this frequency with negative- $G_m$  topology. The simplified schematic of the 1.24GHZ monolithic CMOS VCO is shown in Figure 4.3 [76]. Actually it is not so different from the second design in Figure 4.2. Instead of using NMOS transistors in the cross-coupled pair, here PMOS transistors are used. The benefit is that the flicker noise of PMOS transistors is lower than NMOS transistors with same width. The inductors for the LC tank are implemented using a spiral inductor. The varactor diodes are implemented using p+ to n-well junction diodes. The centre frequency of the VCO is measured as 1.28GHz. The phase noise at 10kHz offset frequency is –88dBc/Hz, at 600kHz offset frequency –125dBc/Hz and at 3MHz offset frequency –137dBc/Hz. The tuning range is 130MHz.

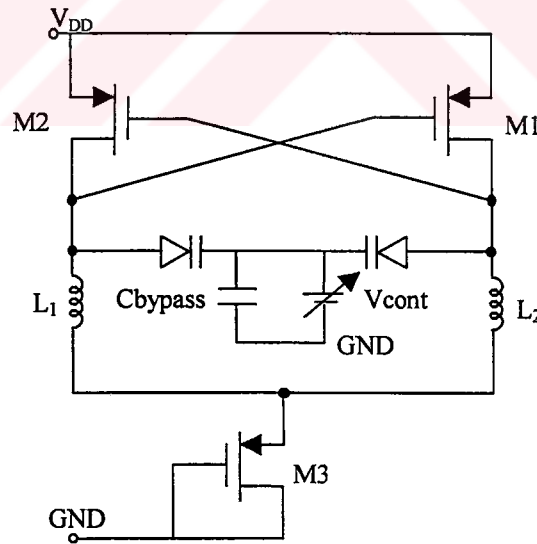


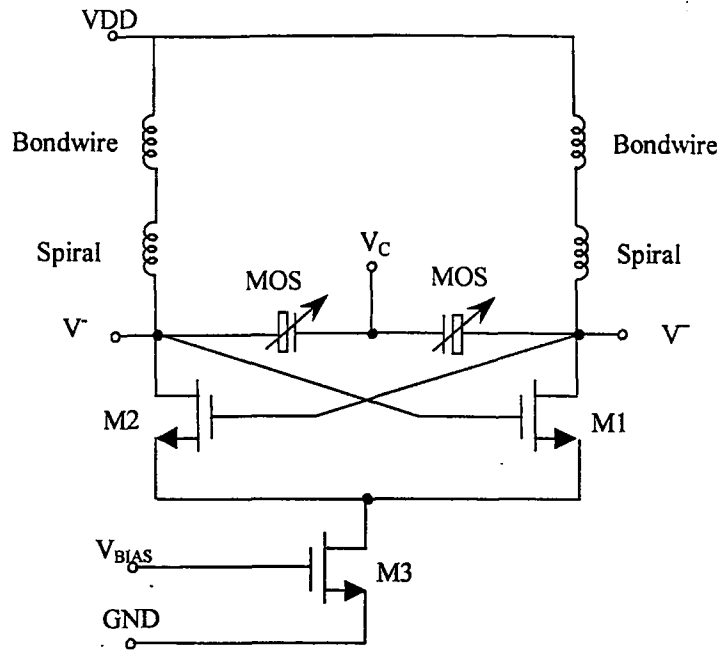
**Figure 4.3** Simplified schematic of VCO presented in [76]

VCO (5): By using the same VCO schematic with the fourth one, but with a different implementation of inductors a better phase noise and power consumption is achieved [77]. This time inductors are implemented using a series combination of spiral inductors, four bond wires and two package leads in order to increase Q. The centre

frequency is 1.09GHz. The circuit consumes 12.7mW of power at  $V_{DD}=3V$  when the fourth one [76] consumes 66mW. The measured phase noise at 10kHz is  $-92\text{dBc/Hz}$  and at 100kHz offset it is  $-112\text{dBc/Hz}$ . The tuning range is 103.7MHz.

VCO (6): A 1.3GHz low phase noise CMOS LC VCO is designed [78] by using spiral inductor and bondwire at the same time. The simplified VCO schematic is shown in Figure 4.4. The designer mentions that using only bondwire inductors like in the first VCO [11] have some disadvantages. First, when the optimum inductance value is high, it is not possible to use the standard bonding length so this leads to use die to die bonding. This method has not been accepted yet in a production environment. Second, the bondwire inductors have large spread ( $\pm 20\%$ ), it is practically impossible to tune out the variations of the components with a standard p-n varactor, due to its limited tuning range. Spiral inductors, instead, feature less spreads ( $\pm 5\%$ ) making the tuning of the tank variations more feasible. But as they are produced in standard CMOS process, you can't get high Q values. In this VCO a series combination of bondwire inductor and spiral inductor is made. With this combination, the spread of the tank is smaller when compared with pure bondwire inductor and also the optimum inductor value with a standard die to frame lead bonding. And the quality factor of the combination will be greater than that of the spiral.

In the LC tank, the accumulation mode MOS varactor is used. The VCO is realized in a  $0.35\mu\text{m}$  CMOS technology. The center frequency of the VCO is 1.3GHz. The tuning range is 28%. The phase noise at 600kHz offset frequency is measured  $-119\text{dBc/Hz}$ .



VCO (7): In the previous design the inductor is realized with both spiral and bondwire inductors. By using the same type of VCO circuit design like, only with spiral inductors a 5GHz CMOS VCO has been designed [18]. This frequency level satisfies the specs of Wireless LAN systems. The tuning is done with the accumulation mode MOS capacitors. The inductors are 2.26nH each. With a 1.5V control voltage variation more than 500MHz of VCO tuning range is achieved. The phase noise at 1MHz offset frequency is  $-101\text{dBc/Hz}$ .

VCO (8): In Chapter 3, we mentioned about different type of varactors. Some designers use negative-Gm oscillator topology to test the performance of different varactors on VCOs.

A 1.8GHz VCO has been designed to compare the performance of the diode varactor VCO and MOS varactor VCO. The basic VCO schematic is shown Figure 4.5. [58,60]. The diode varactors are made of a  $p^+n\bar{n}^+$  lateral diffusion sequence as explained in Section 3.4.1. The MOS varactor is a standard one. In the measurement results, the MOS varactor VCO displays a higher tuning range than the diode varactor VCO, however the phase noise level of the diode varactor VCO is the lowest one. For the overall performance of the circuit, the writer says that diode varactor VCO has a better performance. But in the examples below, we will see that

the VCOs with other types of MOS varactors show better performance than diode varactor VCOs.

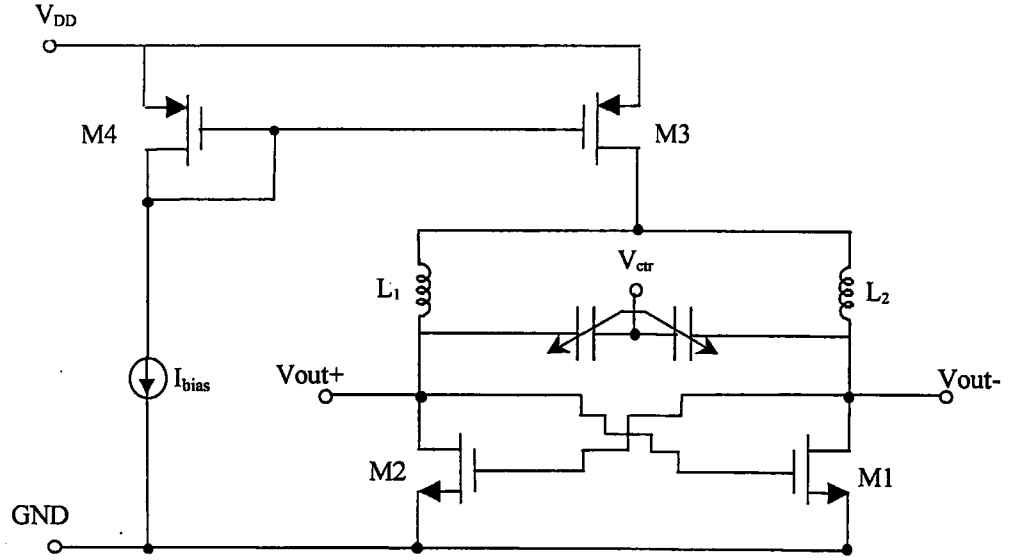


**Figure 4.5** Schematic of the VCO presented in [60].

VCO (9): As mentioned in the 8<sup>th</sup> example circuit, there are different MOS varactor types. Another 1.8GHz VCO has been designed to test different type of varactors. The basic VCO schematic is also shown Figure 4.5 [60]. In design it is mentioned that the previous design of VCOs studies like [13] for DCS-1800 system shows that the poor quality factor  $Q$  of the reverse biased diode varactor used to tune the VCO prevents compliance with the phase noise specifications over the whole tuning range. In the design of the VCO bondwire inductors and three different varactors are used. These are diode varactor, inversion-mode varactor (I-MOS) and accumulation mode varactor (A-MOS).

The tuning characteristics of the VCOs are given in Figure 4.6 and the results are summarized in Table 4.1. The center frequency and the tuning range is same for all VCOs but the linear portion of the tuning characteristics of both MOS varactor VCO's is reduced.

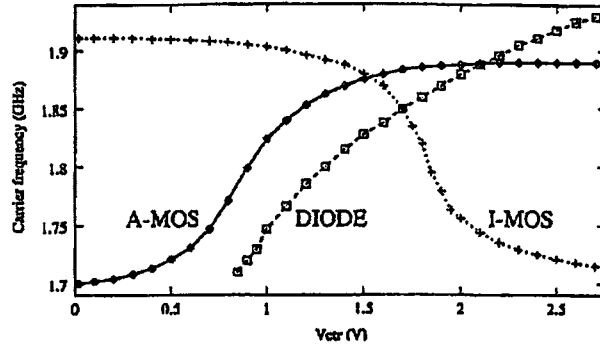


**Figure 4.6** Tuning characteristics of the diode varactor VCO, I-MOS varactor VCO, and A-MOS varactor VCO [60].

**Table 4.1** Frequency behaviors of the VCOs proposed in [60]

| Varactor | $f_L$ - $f_H$<br>(GHz) | $f_c$<br>(GHz) | Tuning<br>Range |
|----------|------------------------|----------------|-----------------|
| Diode    | 1.73-1.93              | 1.83           | 10.9%           |
| I-MOS    | 1.71-1.91              | 1.81           | 11.0%           |
| A-MOS    | 1.70-1.89              | 1.80           | 10.6%           |

**Table 4.2** Phase noise Behaviour of the VCOs proposed in [60]

| Varactor | $I_{dd}$<br>(mA) | Phase noise<br>@ 100kHz,600kHz,3MHz<br>offset from the carrier(dBc/Hz) |
|----------|------------------|------------------------------------------------------------------------|
| Diode    | 4.5              | -100,-116,-130                                                         |
| I-MOS    | 3.8              | -100,-117,-132                                                         |
| A-MOS    | 2.7              | -101,-121,-137                                                         |

The current consumption for the A-MOS VCO is less than half of the current consumption of the diode VCO. The phase noise results of the VCOs are shown in Table 4.2. At high offset frequencies MOS varactor VCOs show better performance than diode varactor. For overall results A-MOS has the best performance of all [60,79].

VCO (10): With the same circuit design like in Figure 4.5, a 2.4GHz monolithic VCO has been designed. The VCO is based on spiral inductance and pMOS varactors implemented in standard 0.8 $\mu$ m CMOS process. The VCO operates between 2.2GHz and 2.55GHz, corresponding to a 15% tuning range. The phase noise of the VCO is -118dBc/Hz at 1MHz offset frequency [61].

VCO (11): As mentioned in Chapter 3, the gated MOS varactor is a new type of varactor, which is still under research. A 2GHz VCO has been designed with gated

MOS varactor [64,65]. The circuit design is shown in Figure 4.7. In the VCO, the gate of the varactors is controlled via  $V_{ctrl}$ , and the drain of the varactors maintains a positive voltage by  $V_{tune}$  through the biasing circuit. As the control voltage ( $V_{tune}$ ) increases, both potentials, across the drain/source and drain/gate reduce. Reducing the voltage across the drain/source, the depletion region underneath the channel shrinks, and hence the total capacitance. Reducing the voltage across the drain/gate, device is driven from inversion mode to depletion mode and the total capacitance is increased. The resulting tuning characteristic is shown in Figure 4.9. The gated varactor achieves a wide tuning range of 53% at 1.5pF. The VCO achieves a tuning range of 320MHz.

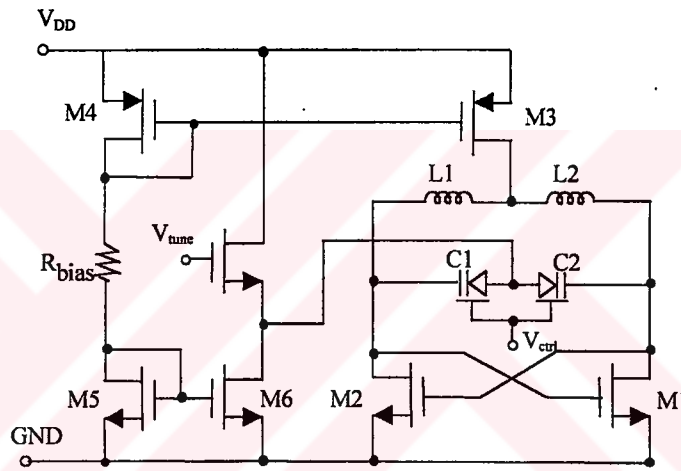


**Figure 4.7** Circuit diagram of the 2GHz VCO. Gate voltage of the gated varactor is applied to the node  $V_{ctrl}$  [65].

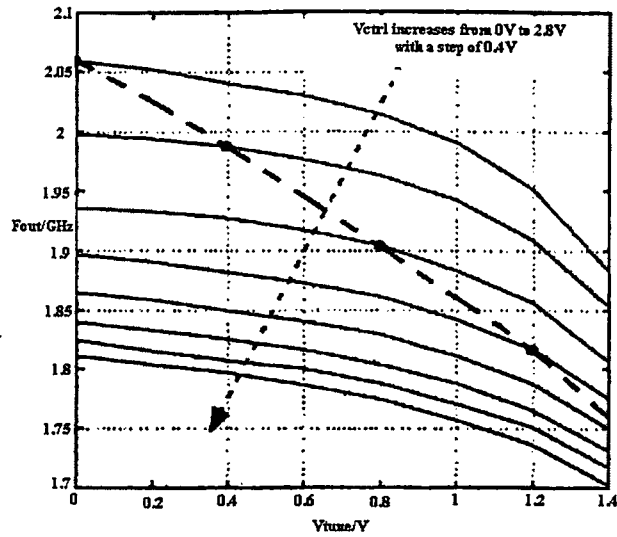


**Figure 4.8** Frequency tuning characteristic of the VCO. The dotted line shows the resultant tuning curve when  $V_{ctrl}$  and  $V_{tune}$  are tied form a single tuning node [65].

VCO (12): A VCO has been designed for DCS-1800 system with a new type of inductor and amplifier circuit [13]. Up to now, we have given circuit examples of negative- $G_m$  oscillators designed with NMOS-only cross-coupled pair or PMOS-only cross-coupled pair. But in this design both of them are used.

The planar LC oscillator schematic is shown in Figure 4.9. One coil inductor is used. This is very important for an optimum VCO design. The negative resistance is formed by the double cross connection of NMOS (M1-M2) and a PMOS (M4-M5) differential pair in positive feedback [13]. We know that generally NMOS-only cross-coupled pair is used with two coils in series. But in this circuit the advantage is, that there is no need for a connection to the common-mode point of the inductor, which would be a problem for the symmetrical coil shape. The oscillation amplitude of this structure is approximately a factor of two larger than that of the NMOS-only structure [28] A drawback of this configuration is the larger parasitic capacitances of the PMOS transistors with respect to an NMOS-only implementation. This results in a slightly available tuning range as the fixed part of the tank capacitance has increased. The frequency tuning is done with standard available P+/N well junction capacitances.

The measured free running oscillation frequency is 1.99GHz. The phase noise at 200kHz-oscillation frequency is  $-113\text{dBc/Hz}$  and the extrapolated value for 600kHz is  $-122.5\text{dBc/Hz}$ . The tuning range is from 1.62GHz to 1.99GHz, which is %20.

**Figure 4.9** Planar LC oscillator circuit schematic [13]

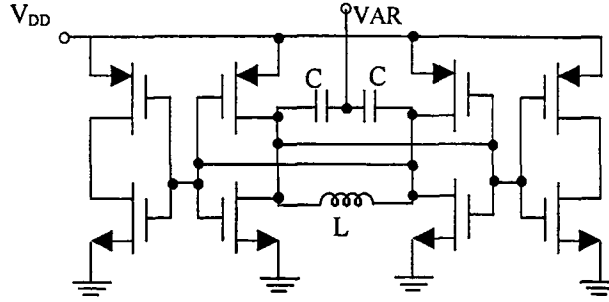


**Figure 4.10** VCO schematic presented in [80]

**Table 4.3** Selected Phase Noise data points[80]

| VCO          | 10kHz | 100kHz | 1MHz   |
|--------------|-------|--------|--------|
| Inversion    | -69.8 | -95.7  | -119.6 |
| Accumulation | -63.2 | -96.0  | -119.7 |
| Gated        | -58.9 | -92.0  | -116.7 |

In Table 4.4 a comparison of the tuning range of some published VCOs are shown.

**Table 4.4** Figure of merit and tuning range by VCO type, with a comparison to other published VCOs [80]

| VCO          | $F_{meas}$<br>(GHz) | @100<br>kHz | @1<br>MHz | Tuning<br>(%) |
|--------------|---------------------|-------------|-----------|---------------|
| Inversion    | 5.922               | -187.0      | -190.9    | 14.5          |
| Accumulation | 5.67                | -187.3      | -191.0    | 14.9          |
| Gated        | 7.342               | -183.3      | -188.0    | 25.6          |
| [75]         | 4.7                 | -173.1      | -173.1    | 4.3           |
| [81]         | 5.05                | -180.3      | -180.3    | 12.3          |
| [82]         | 9.98                | -182.2      | -187.2    | 2.8           |

#### 4.1.1.2 Source-Coupled LC VCO

This type VCO is shown in Figure 4.12, which is designed for 4GHz application [83]. As this circuit does not require bonding wires as inductive elements it is a fully monolithic one. A source-coupled NMOS differential pair M1-M2 combined with the current source M3 forms the negative-resistance cell through positive feedback. The positive feedback is obtained by connecting the gate of M2 to drain of M1. This node also defines the resonator port where an integrated LC circuit can be connected. The inductor is a four-turn spiral inductor. The base-collector junctions of Q1, Q2 and Q3 are employed as a varactor diode. The technology used is 0.5 $\mu$ m BiCMOS process. The VCO achieves %9 tuning range for a control voltage variation of 0-3V.

The VCO gain is about 85MHz/V at 4.1GHz. The measured phase noise is –106dBc/Hz at 1MHz and –85dBc/Hz at 100kHz offset frequency.

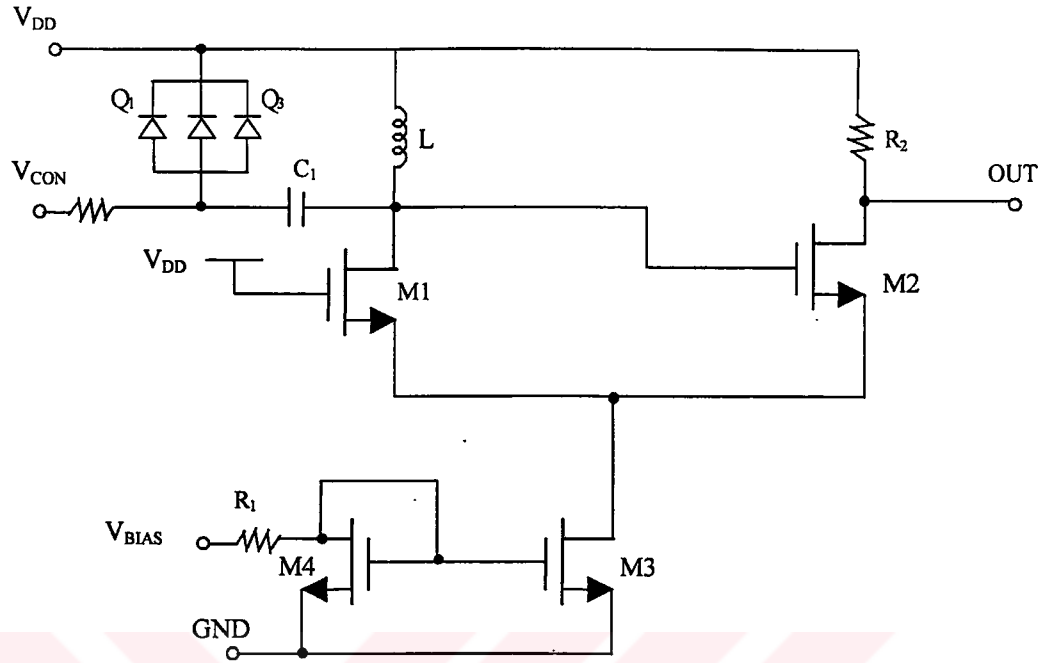


Figure 4.11 Simplified VCO schematic [83]

#### 4.1.1.3 Clapp Configuration VCO

As the new technologies are developed, to produce transistors having high  $f_T$  becomes possible for high frequency systems. An 11GHz 3V fully monolithic VCO is designed in SiGe technology [73]. The simplified schematic of the VCO is shown in Figure 4.12. The goal of this SiGe design is low power dissipation and low voltage operation with acceptable phase noise.

The VCO is based on a modified Clapp configuration. A bipolar device Q1 combined with current source Q2 and capacitor C1 defines the negative-resistance cell for this configuration. The custom-designed varactor diode is based on the extrinsic-base and collector junction. The VCO tuning range is from 10.5GHz to 11GHz and the average VCO gain is 170MHz/V for a tuning range 4.7%. At 1MHz offset frequency the phase noise is between –98dBc/Hz and –106dBc/Hz.

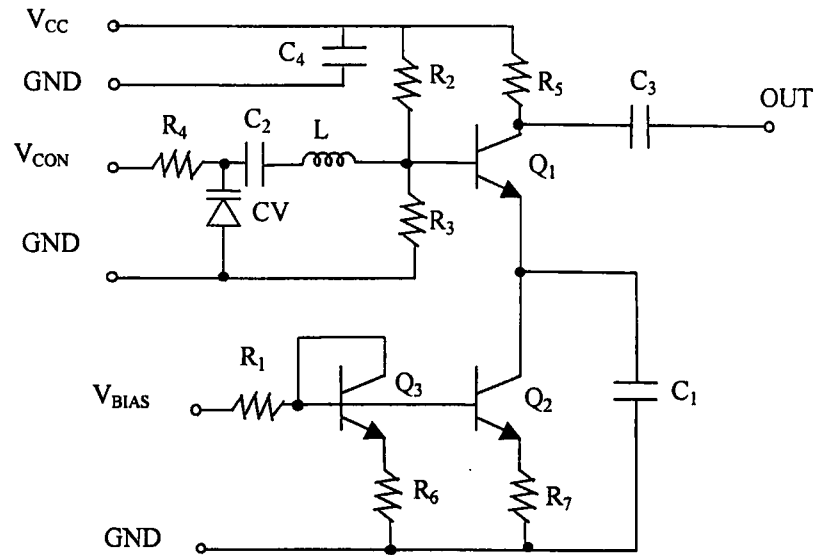


**Figure 4.12** Simplified VCO schematic [73]

#### 4.1.1.4 Comparison of the LC VCOs

In the section above we have discussed about different type of LC VCOs with different circuit topologies. In Table 4.5, the performance results of some of the negative- $G_m$  VCOs are given.

**Table 4.5** Comparison of negative- $G_m$  LC VCOs

| Negative- $G_m$ VCOs | Technology        | Freq. | Tuning Range | Phase Noise |
|----------------------|-------------------|-------|--------------|-------------|
|                      | [-]               | [GHz] | [%]          | [dBc/Hz]    |
| 1                    | 0.7 $\mu$ m CMOS  | 1.76  | 4.5          | -115 @ 200k |
| 2                    | 0.7 $\mu$ m CMOS  | 1.81  | 14           | -116 @ 600k |
| 3                    | 0.35 $\mu$ m CMOS | 4.7   | 4.3          | -110 @ 1M   |
| 4                    | 0.8 $\mu$ m CMOS  | 1.24  | 10.4         | -125 @ 600k |
| 5                    | 0.8 $\mu$ m CMOS  | 1.1   | 11.4         | -126 @ 600k |
| 6                    | 0.35 $\mu$ m CMOS | 1.3   | 28           | -119 @ 600k |
| 7                    | 0.24 $\mu$ m CMOS | 5     | 10           | -101 @ 1M   |
| 10                   | 0.8 $\mu$ m CMOS  | 2.4   | 15           | -118 @ 1M   |
| 12                   | 0.4 $\mu$ m CMOS  | 1.8   | 20           | -119 @ 600k |

Low phase noise, high tuning range, low power consumption are the targets of a designer for VCOs. The technology used for the design and the oscillation frequency of the VCO are effective on the circuit performance. The first and the second VCO are designed with the same technology for DCS-1800 systems. As explained before the first one is designed with bondwire inductors and the second one is designed with

spiral inductors. The first one achieves a better phase noise than the second one because you can't get high Q values with spiral inductors. So the VCOs designed with bondwire inductor have better phase noise performance. But because the bondwire inductors have too much process variation, the first VCO has a tuning range performance worse than the second VCO has. Actually due to the bonding method used in the first VCO is not a way accepted in the production environment. The VCO (12) is also design for DCS-1800 system but with 0.4 $\mu$ m CMOS technology. When compared with the VCO (2), both phase noise and the tuning range performance of the VCO is increased due to the optimum symmetrical coil design and new amplifier circuit design. The VCO (4) is designed with PMOS transistors instead of NMOS transistors. As PMOS transistors have lower flicker noise, the VCO (4) has a better phase noise performance compared with VCO (2) at the same offset frequency. VCO (5) uses the same topology but with both bondwire and spiral inductors. Therefore this combination makes the tuning range and phase noise performance better than VCO (4). VCO (6) has the best tuning range performance of all shown in Table 4.5 The reason is the usage of accumulation MOS varactors. Also the usage of both spiral and bondwire inductors as a series combination has increased the phase noise compared with VCO (2). VCO (10) is a typical negative- $G_m$  VCO designed with simple MOS varactor, so the tuning range performance is over the average. The phase noise performance of VCO (10) is below the average when compared with VCO (1), VCO (2), VCO (4), and VCO (5). As the oscillation frequency increases it is difficult to achieve good circuit performance. VCO (3) and VCO (7) are examples of 5GHz VCO for wireless systems. VCO (7) has a better tuning range than VCO (3) due to the usage of accumulation MOS varactors.

The other VCOs, which are not given in Table 4.5, are designed especially to compare different types of varactors. The comparison of them is already given in their own section. The source-coupled VCO and Clapp configuration VCO has worse tuning range performance compared with the negative- $G_m$  oscillators.

More examples of VCO circuits designed for different systems are presented in [15,19,20,83 – 85, 87 – 89].

### 4.1.2 Ring Oscillators

As mentioned before in Chapter 2 that the oscillation frequency of N stage ring oscillator equals to  $1/(2NT_D)$ . To control the frequency the delay of each stage  $T_D$ , can be adjusted in order to change the oscillation frequency. The types of ring VCO depends on different things like, the differential cell design, bias control circuit design and the number of the delay cells used. In this section we give different types of ring VCOs, explain the circuit topology and give the resulting performance of the circuits.

#### 4.1.2.1 Tuning of the Ring VCOs

This section explains the tuning method of the ring VCOs by giving examples. More circuit examples are given in the next section.

In Figure 4.13, an example of differential pair circuit as the delay circuit is shown. Here the PMOS transistors operate in triode region as they act as a variable resistor controlled by  $V_{cont}$ . As  $V_{cont}$  becomes more positive on-resistance of M3 and M4 increases, so the time constant at the output increases and the oscillation frequency decreases.

But this differential pair has a drawback, as the output swing of the circuit varies considerably across the tuning range. The reason is that the stage provides a differential output swing of  $2I_{SS}R_{on3,4}$ . So when the  $V_{cont}$  changes, only  $R_{on3,4}$  is effected, resulting a variation [35].

In order to minimize the swing variation, the tail current can be adjusted by  $V_{cont}$  so that when  $V_{cont}$  becomes more positive,  $I_{SS}$  decreases. The topology, that serves to maintain  $I_{SS}R_{on3,4}$  relatively constant, is shown in Figure 4.14.

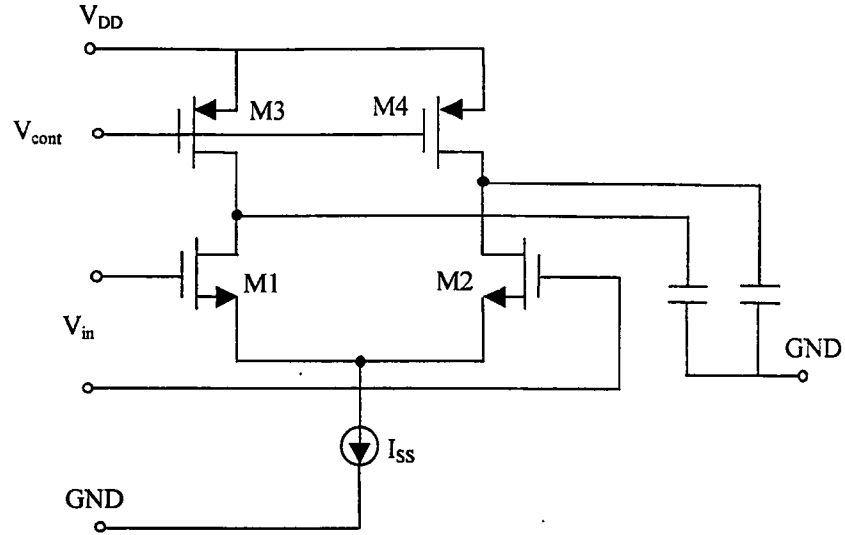


**Figure 4.13** Differential pair presented in [35]

The feedback circuit in Figure 4.14(a) serves for all stages of the ring oscillator, defining the oscillation amplitude. M5 operates in deep triode region and amplifier A<sub>1</sub> applies negative feedback to the gate of M5. If the loop gain is sufficiently large, the differential input voltage of A<sub>1</sub> must be small, giving  $V_P \approx V_{REF}$  and  $|V_{DS5}| \approx V_{DD} - V_{REF}$ . The feedback ensures a relatively constant drain-source voltage even  $I_1$  varies. In Figure 4.14(b) the differential delay cell is shown with the feedback circuit. By controlling the  $I_S$  current also  $I_{SS}$ , the oscillation frequency can be varied satisfying a stable oscillation amplitude with the feedback circuit [35].

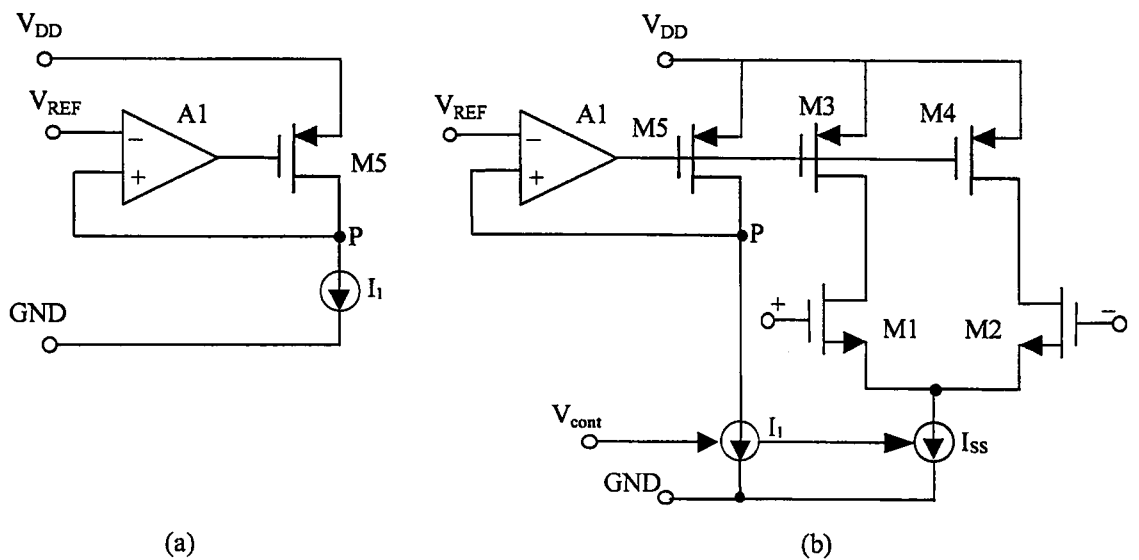


**Figure 4.14** (a) Simple feedback defining  $V_P$  (b) Differeantial stage with biasing [35].

Another technique to tune the ring oscillators is shown in Figure 4.15. As mentioned in Chapter 2, the cross-coupled transistor pair exhibits resistance of  $-2/g_m$ , which can be controlled by the bias current. The equivalent half circuit of the differential pair is shown in Figure 4.15(b). As  $I_1$  increases the small signal differential resistance  $-2/g_{m3,4}$  becomes less negative, then the equivalent resistance of the half circuit is  $R_p \parallel (-1/g_{m3,4}) = R_p / (1 - g_{m3,4} R_p)$  increases, thereby lowering the oscillation frequency. As  $I_1$  varies, the currents flowing from  $R_1$  and  $R_2$  are steered by M3 and M4, this causes the output voltage swing not be constant across the tuning range. Further methods to minimize these effects are explained in [35]

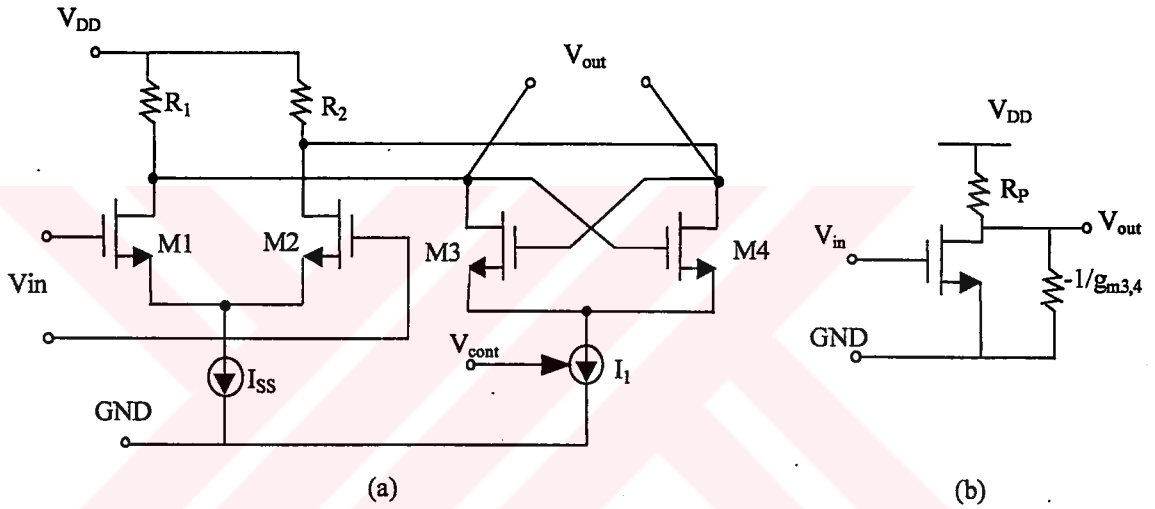


**Figure 4.15** (a) Differential stage with variable negative resistance load, (b) Half circuit equivalent [35].

In Figure 4.16 a variable-frequency NMOS ring oscillator is shown. Inserting a FET in series with every inverter varies the delay per stage. The FET acts like voltage controlled resistor and varies the RC time constant driving each stage where C is the input capacitance of the inverter. The drawback of this circuit is that by adding the FETs, we increase delay, so it becomes difficult to obtain the maximum possible oscillation frequency, as it requires the fewest number of inverters. And if the number of inverters is reduced, insufficient loop gain may exist, prohibiting the oscillation [10].

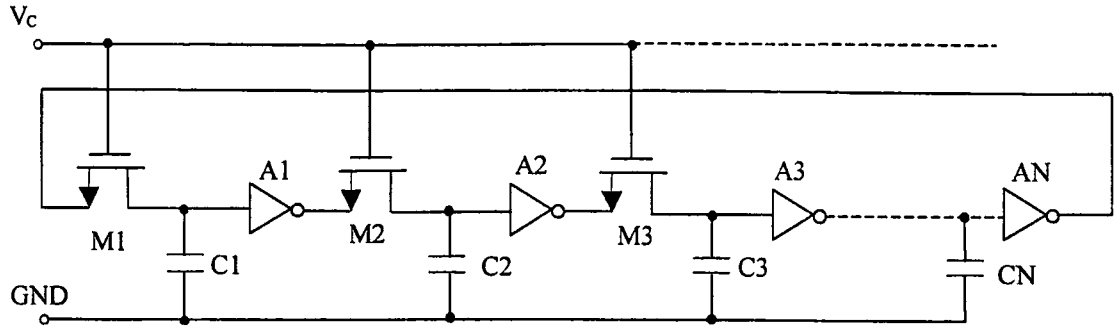


**Figure 4.16** Variable-frequency NMOS ring oscillator with voltage-controllable delay between stages presented in [10].

Another way to control the frequency is shown in Figure 4.17. The structure consists of an odd ( $m$ ) and ( $n$ ) even number of inverters. The FETs act as a voltage controlled a potentiometer. Depending on the biasing of points M1 and M2, different oscillation frequencies can be achieved.

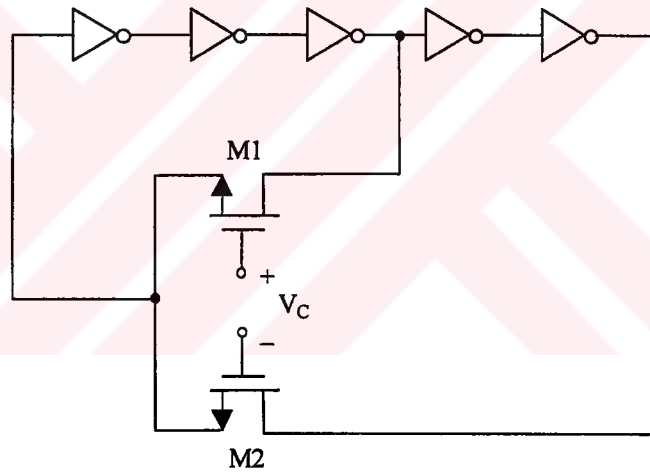


**Figure 4.17** Dual ring oscillator with voltage-controllable mixing in feedback path presented in [10].

The same structure, with CMOS implementation is designed with inner ring of five stages, and an outer ring of nine stages. The schematic is shown in Figure 4.18. The oscillation frequency could be varied over a range greater than 100MHz by changing the  $V_c$  from  $-2V$  to  $5V$ . The frequency can be varied from 275MHz to 325MHz.

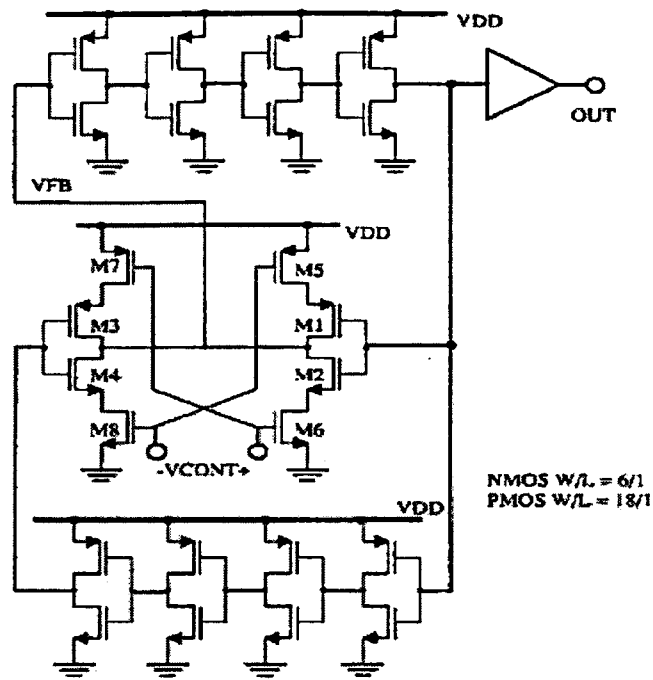


**Figure 4.18** CMOS Prototype of dual ring oscillator presented in [10]

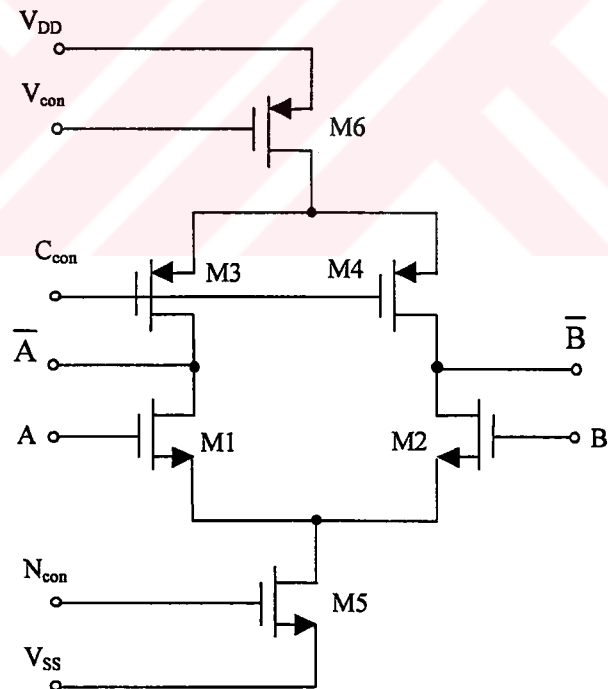


**Figure 4.19** Differential delay cell presented in [90]

#### 4.1.2.2 Examples of Ring VCOs

VCO (14): The first example is a 1GHz VCO designed for mobile communication application [90]. The VCO is composed of three-stage ring oscillator where each

stage is voltage controlled differentially delay element as shown in Figure 4.19. The delay cell consists of a NMOS source-coupled pair with PMOS loads. The control voltage of the circuit  $V_{con}$  is applied at the gate PMOS transistor M6. The gate input  $N_{con}$  of NMOS transistor M5 is controlled by a biasing circuitry. So there is separate ways to control the output voltage of the delay cell.

The tuning range of the VCO is between 600MHz and 1000MHz. The voltage gain is 290MHz/V at the center frequency of 800MHz. The phase noise is  $-80\text{dBc/Hz}$  at 100kHz offset frequency and  $-100\text{dBc/Hz}$  at 1MHz offset frequency.

VCO (15): A 1.3GHz to 1.8GHz CMOS VCO is designed for wireless communications [91]. The designed oscillator is a three staged one as shown in Figure 4.20. This three stage VCO is employed for power minimization and frequency optimization. The similar method showed in Figure 4.14 is used. The delay cell and the bias control cell are shown in Figure 4.21. Here the active amplifier keeps the drain voltages of load transistors to be constant for different input current  $I_{in}$ . The transistor M6 is used to limit the oscillation amplitude.

The VCO can operate from 1.3 to 1.8GHz with a gain of 970MHz/mA. The peak to peak value of the output amplitude is between 1.43 and 1.53V.

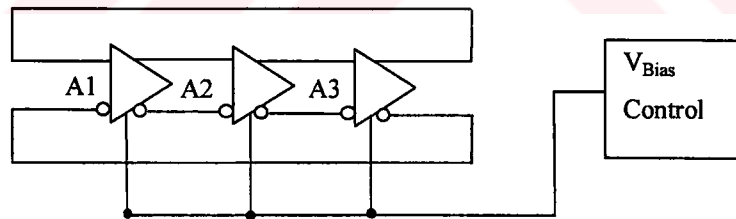


**Figure 4.20** Ring oscillator presented in [91]

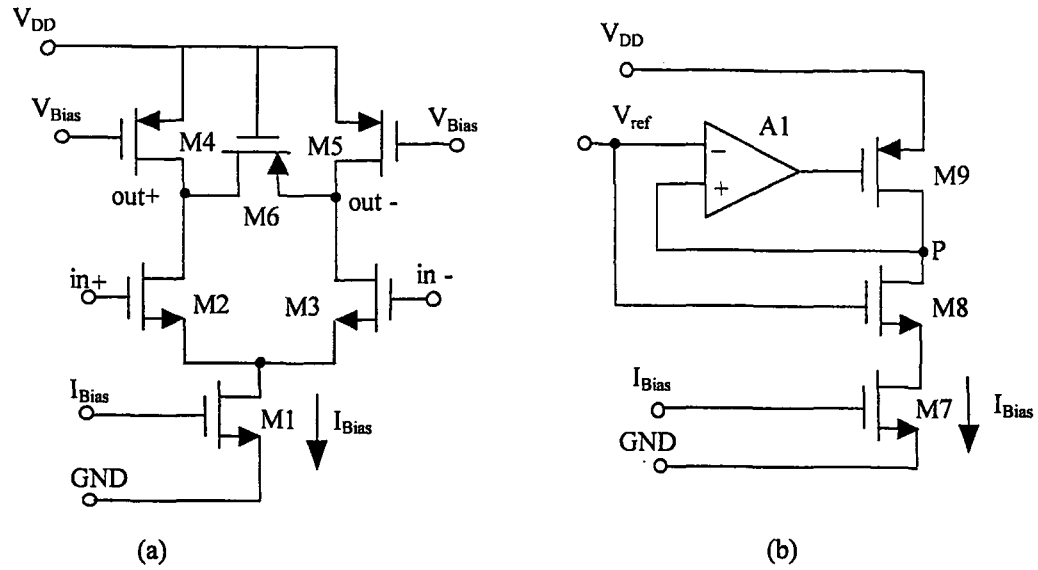


**Figure 4.21** (a) Delay Cell (b) Bias Circuitry presented in [91]

VCO (16): A 900MHz VCO is designed for low noise applications [92]. The delay cell is shown in Figure 4.22. A pair of PMOS load transistors, M3 and M4, are added to the delay cell to constitute a CMOS latch. The cross-coupled NMOS transistors, M5 and M6, control the maximum gate voltage of the PMOS load transistors and limit the strength of the added latch. When  $V_{cont}$  is low, the strength of the latch becomes weak, and the output current of the PMOS load increases. Therefore, the state of the latch is changed easily, and the delay time is reduced. In conventional ring oscillators, the oscillation frequency is decided by the delay time of one delay element and the number of the delay stages. The delay time can not be smaller than that of a single inverter. So the maximum oscillation frequency of the VCO is limited by the delay time of the basic inverter cell. To solve this problem, a negative skewed delay scheme has been reported [93].

The dual-delay scheme is used to implement the VCO [92]. The dual-delay scheme means that both the negative skewed delay paths and normal delay paths exist in the same ring oscillator. As the negative skewed delay paths decrease the unit delay time of the ring oscillator below the single inverter delay time, higher oscillation frequency is obtained. Since the normal delay paths also exist, the frequency range of the VCO can be wider than that of an oscillator with only skewed delay paths. This type of delay cell is shown in Figure 4.23.

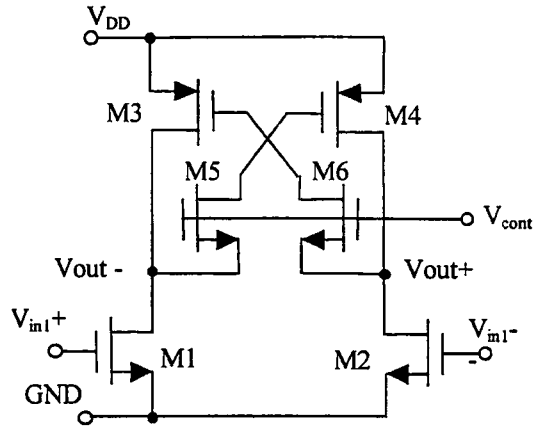


**Figure 4.22** Differential delay cell presented in [92]

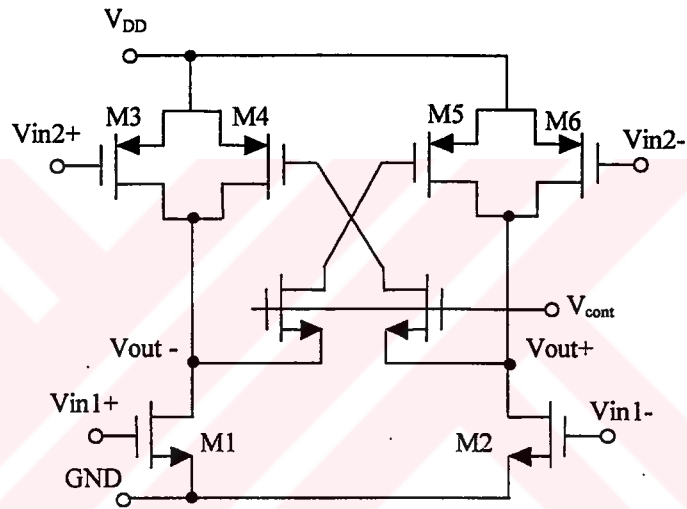


**Figure 4.23** Four-input differentail delay cell presented in [92]

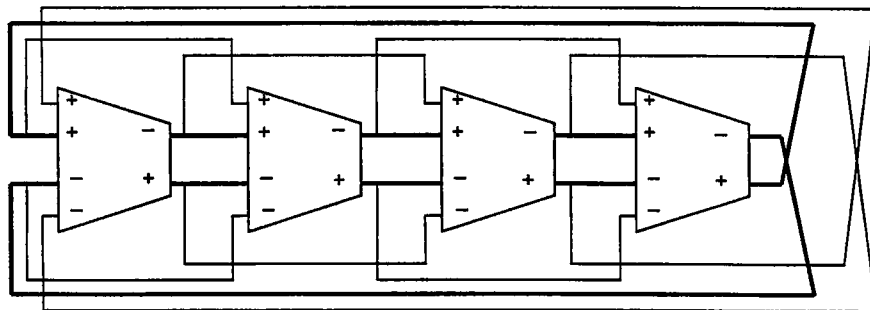


**Figure 4.24** Ring oscillator structure with dual-delay paths presented in [92]

A pair of PMOS transistors is added to the PMOS loads of the delay cell and is used to take the negative skewed signals. Negative skewed signal is connected to the PMOS input delay cell, and the normal signal is connected to the NMOS input of the delay cell. The ring oscillator structure with dual-delay paths is shown in Figure

4.24. The resulting phase noise of this ring oscillator is measured  $-101\text{dBc/Hz}$  at  $600\text{kHz}$  offset frequency and  $-117\text{dBc/Hz}$  at  $600\text{kHz}$  offset frequency. The frequency range is from  $750\text{MHz}$  to  $1.2\text{GHz}$ , so %50 of tuning range.

VCO (17): A ring oscillator is designed for CMOS Dual-Loop Frequency Synthesizer for GSM applications [94]. The ring oscillator and its delay cell schematic are shown in Figure 4.25. The delay cell consists of NMOS transistors  $M_{n1}$  as input transconductors, cross-coupled PMOS transistors  $M_{p1}$  for maintaining oscillation, diode connected PMOS transistors  $M_{p2}$  and a bias transistors  $M_{b1}$  for frequency tuning. The source nodes of transistors  $M_{p1}$  are connected to supply to maximize its output amplitude. The measured operating frequency is between  $324\text{MHz}$  and  $642\text{MHz}$ . The phase noise is between  $-111\text{dBc/Hz}$  and  $-108\text{dBc/Hz}$  at  $600\text{kHz}$  offset frequency.

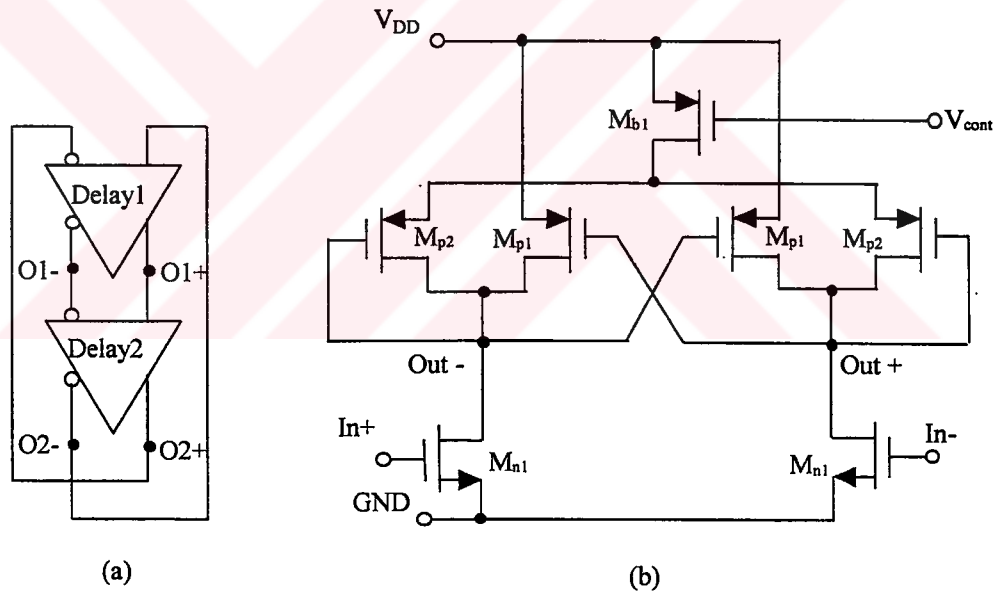


**Figure 4.25** (a) Ring oscillator (b) Delay cell presented in [94]

#### 4.1.2.3 Comparison of the ring oscillators

In section 4.2.2.2, four different ring VCOs are given. The performance of the ring VCOs are given in Table 4.6.

**Table 4.6** Comparison of the ring VCOs

| Ring VCOs | Technology | Freq. | Tuning Range | Phase Noise |
|-----------|------------|-------|--------------|-------------|
|           | [-]        | [MHz] | [%]          | [dBc/Hz]    |
| 14        | 0.8μm CMOS | 800   | 25           | -80 @ 100k  |
| 16        | 0.6μm CMOS | 900   | 50           | -101 @ 100k |
| 17        | 0.5μm CMOS | 483   | 32           | -108 @ 600k |

A fully switching of the differential delay cell is used for VCO (2) to reduce the phase noise of the ring VCO and the dual path technique is used to increase the tuning range. Therefore VCO (2) has a better tuning range and phase noise performance than the VCO (1) has. Actually VCO (2) has the best performance of all. VCO (2) also has a better phase noise and tuning range performance than VCO (3). The type of the differential delay cell used in VCO (3), makes it have a better performance than VCO (1).

## 4.2 Quadrature Signal Generation

In some transceiver systems depending on the modulation type, quadrature LO signals are needed. There are four ways to generate quadrature signal.

### 4.2.1 RC-CR Network

In this method, quadrature generation is obtained with the combination of VCO, RC-CR network (or polyphase filters) and buffers or limiters.

The simple quadrature technique is to shift the signal by  $\pm 45^\circ$  using a RC-CR network as shown in Figure 4.26. Suppose  $V_{in}(t) = A_1 \cos \omega t$  then,

$$V_{out1}(t) = \frac{A_1}{\sqrt{R^2 C^2 \omega^2 + 1}} \cos[\omega t - \tan^{-1}(RC\omega)] \quad (4.1)$$

$$V_{out2}(t) = \frac{A_1 RC\omega}{\sqrt{R^2 C^2 \omega^2 + 1}} \cos\left[\omega t - \tan^{-1}(RC\omega) + \frac{\pi}{2}\right] \quad (4.2)$$

The phase shift of  $V_{out1}(t)$  and  $V_{out2}(t)$  are equal to  $\pi/2 - \tan^{-1}(RC\omega)$  and  $-\tan^{-1}(RC\omega)$  respectively. So  $V_{out1}(t)$  and  $V_{out2}(t)$  have  $90^\circ$  degrees phase difference at all frequencies. But the output amplitudes are equal only at  $\omega = 1/(RC)$ .

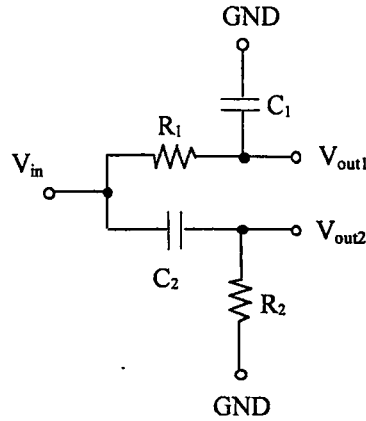


**Figure 4.26** Quadrature network using RC-CR network [21]

If the absolute value of  $RC$  varies with temperature and process, so does the frequency at which equal-amplitude quadrature signals exits. So we need limiters to equalize the amplitude. But in gigahertz circuits, amplitude limiting becomes difficult. The mismatches between resistors and capacitors cause phase error. Also mismatches between load capacitance also contribute to phase error.

To minimize the attenuation caused by the load capacitance, the value of  $C$  is chosen like  $C \approx 5C_L$ . If buffers are used after the filter, they consume too much power.

In a fully integrated 900MHz CMOS Double quadrature modulator, a two stage sequence asymmetric polyphase filter is designed [24]. The schematic is shown in Figure 4.27. Two-stage structure is preferred, because the conventional RC-CR network does not have good broadband amplitude matching. By applying only an I-signal, a quadrature signal can be generated. Passband range is designed from 600MHz to 1.2GHz. The signals at 900MHz are always in quadrature, independent of process variation. The phase error is  $< 0.3^\circ$ .

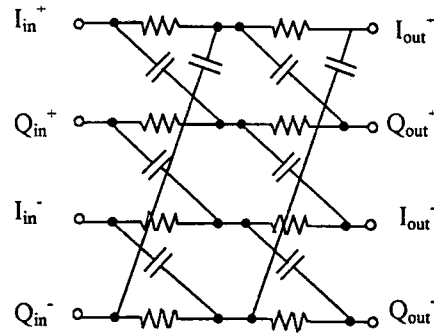


**Figure 4.27** The two-stage sequence asymmetric polyphase filter used as quadrature generator[24].

Another polyphase filter is designed for 1.9GHz mobile radio telephone application [22]. In Figure 4.28, the local oscillator quadrature generator is shown. The error is found less than  $0.5^\circ$  degrees.

A LO phase shift network is designed for a direct conversion receiver for 900MHz spread-spectrum digital cordless telephone [23]. The LO phase shift circuit consists of an integrated low pass filter, buffer and differential R-C phase shift network. The full schematic is depicted in Figure 4.29.

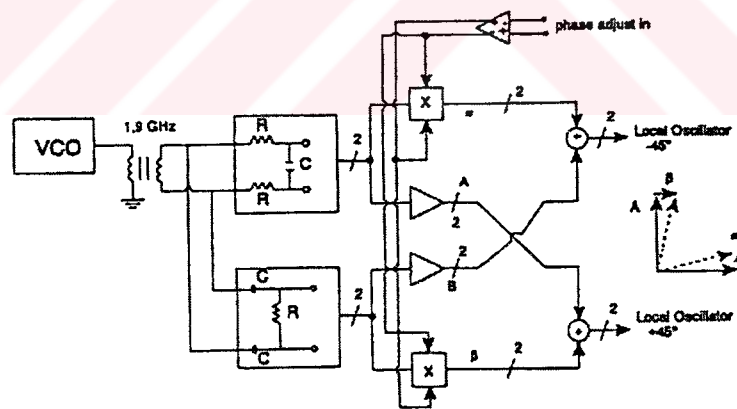


**Figure 4.28** Local Oscillator quadrature generator[22]

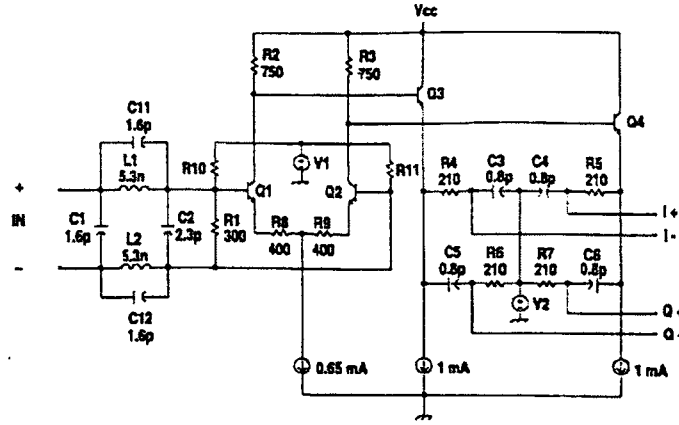


**Figure 4.29** Low-Pass filter and phase shift network [23]

The phase shift network consisting of R4-R7 and C3-C6 forms a differential version of conventional RC-CR network. In the measurements it is found that the phase error increases with the frequency. But between 300MHz and 2GHz the phase error is at most  $1^\circ$  degree. Because of the process variations, the only frequency that the amplitudes are matches is 915MHz. Amplitude mismatch is up to %30.

In Figure 4.30, it is shown how differential quadrature phases are generated from a differential input. More about polyphase filters are explained in [25]

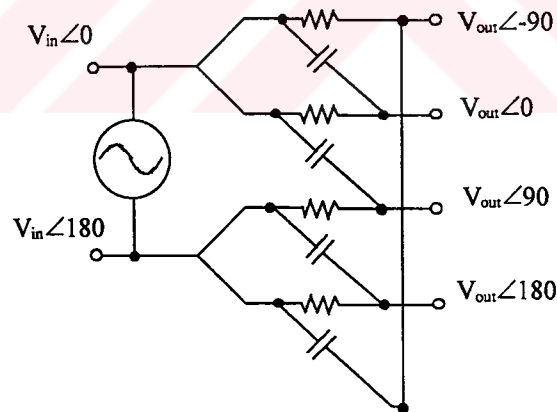


**Figure 4.30** Polyphase Filter presented in [25]

#### 4.2.2 Frequency Division

Another way to generate quadrature periodic signals with frequency  $\omega_1$ , is to use master-slave flip-flops to divide a signal at  $2\omega_1$  by factor two, as shown in Figure 4.31. So the VCO should be designed in double frequency.

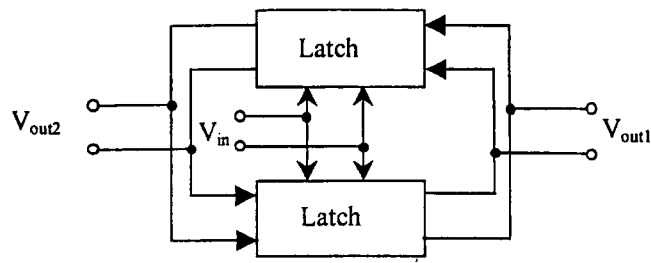


**Figure 4.31** Frequency dividers as a quadrature generator

If the input voltage  $V_{in}$  has a 50% of duty cycle, then  $V_{out1}$  and  $V_{out2}$  are out of phase. The VCO designed in double frequency will consume less power, as a higher  $Q$  for integrated tanks at higher frequencies are achievable. And the coil area is smaller with double frequency. The master-slave flip-flops have to be designed in double frequency, therefore they consume too much power depending on the technology. But as the technology develops, this method can be used. A disadvantage could be that the phase imbalance resulting from the deviation of the input duty cycle from 50% [21].

### 4.2.3 Two Cross-Coupled VCO

In this method two oscillators are cross-coupled to each other. The oscillators don't need to be identical, only have frequencies that are close. Then they synchronize to exactly the same frequency. The basic shape of the system is shown in Figure 4.32. The coupling signal from Oscillator A forces Oscillator B to operate exactly the same frequency as A. This type of connection is called "injection locking"[27].



**Figure 4.32** Synchronizing two independent oscillators.

The basic circuit building block, shown in Figure 4.33, is the MOSFET LC oscillator consisting of a cross-coupled pair of FETs (M1, M2), having the same structure with LC oscillator shown in Figure 4.4. Two such identical oscillators, labeled A and B in Figure 4.34, are coupled by FETs (M3, M4) of the same size as the main FETs (M1, M2) such that there is direct coupling in one direction, and cross-coupling in the other.

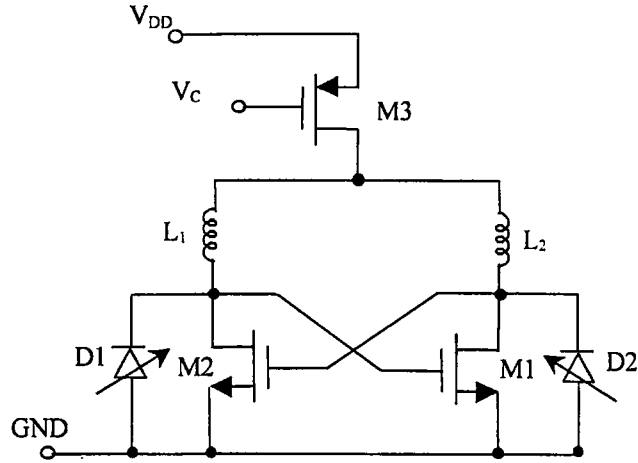


**Figure 4.33** LC Oscillator presented in [27]

Suppose now that the two oscillations synchronize in-phase. Then the cross-coupled path from Oscillator B to A absorbs the negative-resistance current produced by M1A, M2A and Oscillator A ceases. The inductors in Oscillator A pull up both drain nodes to  $V_{DD}$ , and through the cross-coupled FETs, this shuts off Oscillator B. The same process applies in reverse if the two oscillations are anti-phase. Therefore the oscillations only co-exist when they synchronize in quadrature. Then they acquire combination of  $0^\circ$  at M2A,  $180^\circ$  at M1A,  $90^\circ$  at M2B, and  $270^\circ$  at M1B.

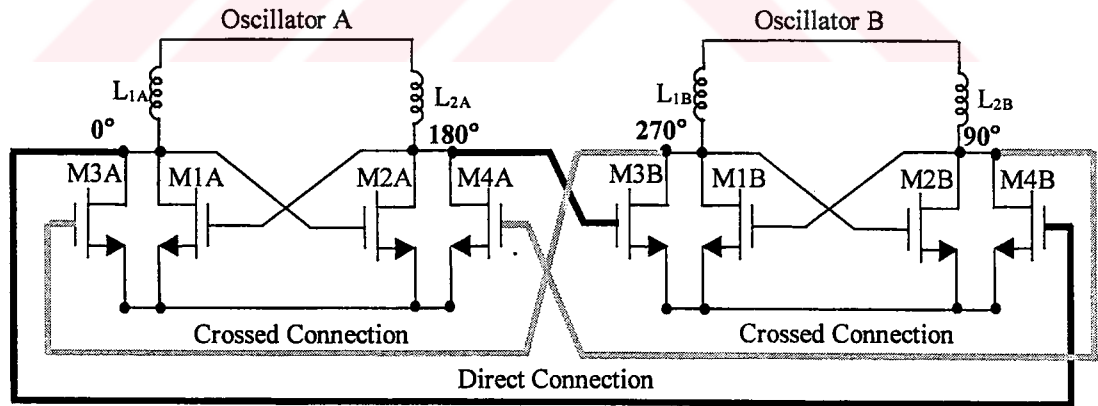


**Figure 4.34** Oscillators Synchronized in Quadrature [27]

When compared with other methods, this structure costs double VCO area. But if the VCO core is well designed it consumes less power than the output buffers or limiters which are used with RC-CR network. The other advantage of this structure is that, it provides a very high voltage swing, which eases the design of the prescaler and mixer circuits connected to VCO. The layout of the circuit plays a big role for the mismatches of the VCO.

This quadrature VCO has been realized. The measured tuning range is between 860-958MHz. The phase noise at 100kHz offset frequency is measured,  $-96\text{dBc/Hz}$ . The measure phase mismatch is less then 1 degrees [27].

A similar 900MHz VCO is designed with improved amplitude and phase matchings. Amplitude control, quadrature phase control and different layout techniques are proposed. The phase noise is measured  $-105\text{dBc/Hz}$  at 100kHz offset frequency. The tuning range is 100MHz [95].

A 1.8GHz CMOS Quadrature VCO is designed with a new oscillator, which satisfies better tuning range. The oscillators are identical and one of them is shown in Figure 4.35.

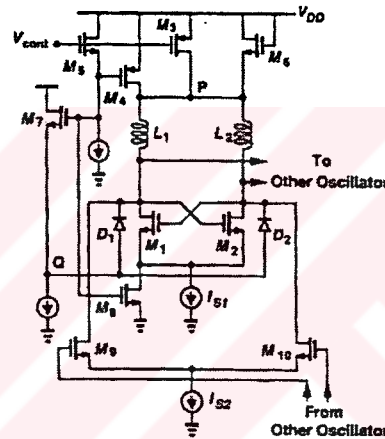


**Figure 4.35** VCO circuit presented in [96]

In this circuit, M3-M5 provide a resistance from P to  $V_{DD}$  that varies smoothly with  $V_{cont}$ . The voltage is clamped by M6 to about 1.2V (Supply voltage=3.3V). To increase the tuning range, the anode voltage of the diodes can be varied in the opposite direction with respect to their cathode voltage. M9 and M10 are used to sense the output of the other oscillator in the quadrature circuit. The tuning range of the VCO is measured 120MHz. The phase noise at 500kHz offset frequency is  $-100\text{dBc/Hz}$  [96].

A similar LC quadrature VCO is designed for a 2.6GHz/5.2GHz Frequency Synthesizer. One of the VCO is shown in Figure 4.36. The use of transistor M6 is for sensing 5.2GHz signal at node A. This structure ensures the common gate stage

carries a constant bias current across the full tuning range. The connection of the two VCOs is done with the same method, which is shown in Figure 4.34. Phase noise measured at 10MHz offset frequency is  $-110\text{dBc/Hz}$  for 2.6GHz operation frequency [97].

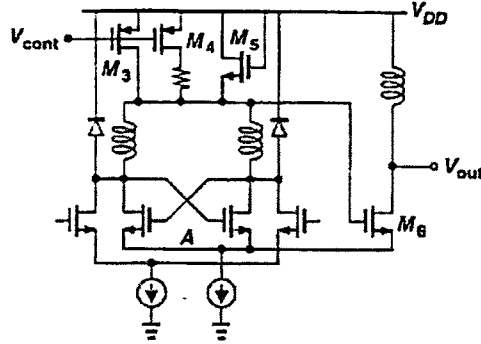


**Figure 4.36** VCO circuit presented in [97]

#### 4.2.4 Quadrature Ring Oscillator

In a ring chain, if even numbers of delay cells are used, quadrature phase relationships are obtained between the outputs. A 4-stage ring oscillator is shown in Figure 4.37.

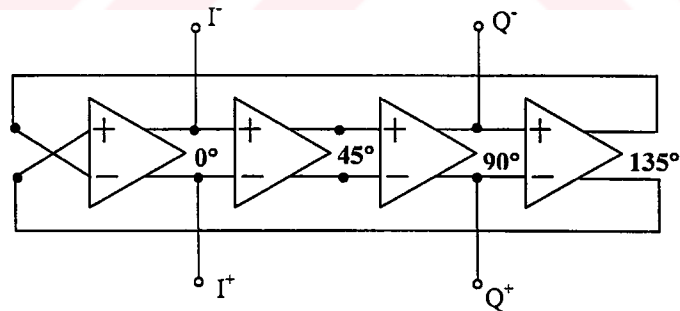


**Figure 4.37** Differential 4-stage ring oscillator

With this type of quadrature VCO, we can obtain a better tuning range when compared with LC VCOs. Also it will cost less chip area. The phase mismatch, which is caused by layout of the circuit, is better, as the matching of inverters is easier than that of coils. The only disadvantage is that the ring VCO has a poor phase noise. If the system doesn't need a good phase noise spec, for all properties

quadrature ring VCO is the best choice. Quadrature ring oscillators are preferred especially in clock recovery circuit.

This type of quadrature generation is used in a CMOS Dual channel transmitter for Cable applications. The figure of the total transmitter is shown in Figure 4.38. The tuning range is between 55MHz and 1.2GHz [98].

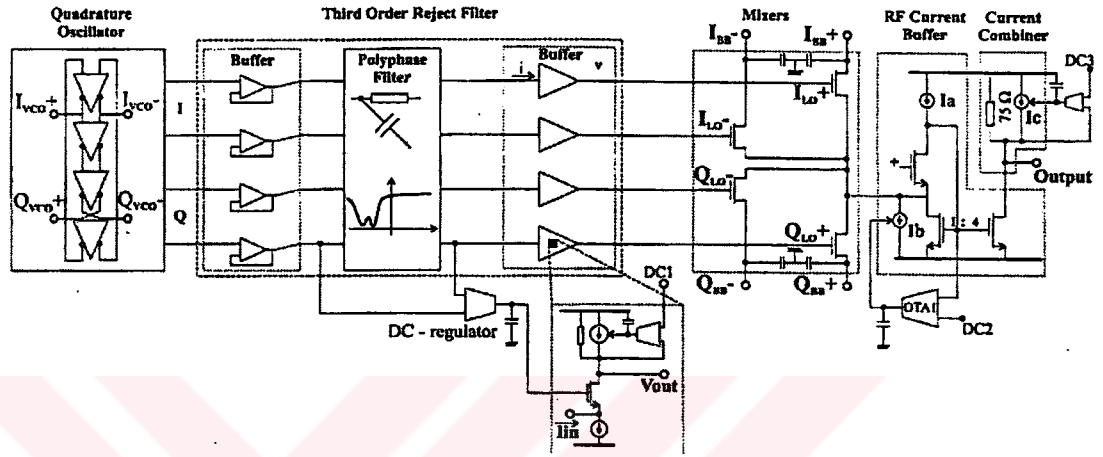


**Figure 4.38** Circuit level description of one transmitter channel [98]

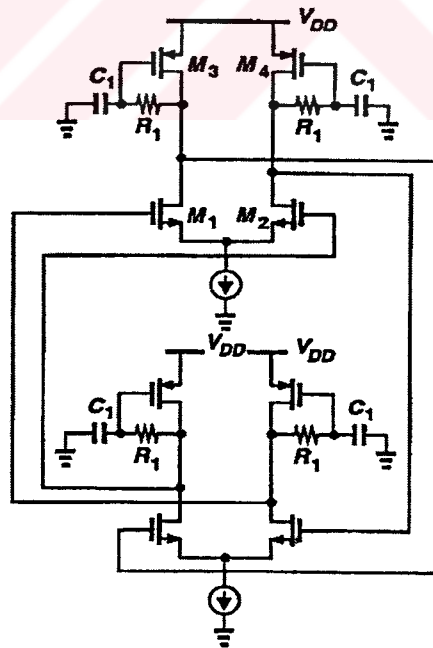


**Figure 4.39** Two stage ring oscillator with composite load presented in [26]

A 2-stage ring oscillator is designed for CMOS clock recovery circuit for 2.5-Gb/s NRZ Data [26]. The design is done with 0.4 $\mu$ m CMOS technology. But using this

technology, with four-stage ring oscillator, the oscillation frequency does not exceed 1.8GHz. To achieve 2.5GHz-operation frequency, two-stage topology is necessary. The two-stage ring oscillator is shown in Figure 4.39. The measure phase noise of the oscillator is  $-80\text{dBc/Hz}$  at 5MHz offset frequency.

#### 4.2.5 Comparison of the Quadrature Generation Methods

The RC-CR network, which is especially followed by limiters or buffers, consumes too much power. The mismatch between resistors and capacitors cause phase and amplitude error. Therefore the filter layout needs good matching. This kind of circuit also consumes a lot of chip area.

The second method, frequency division, has smaller area than the RC-RC network and cross-coupled VCO. The LC VCO designed at double frequency does not consume too much power, but the master-slave flipflops consume too much power in today's technology. Mismatches in the signal path through the latches contribute to phase error. If the power consumption is not so important and if you want a low cost design or small area, this method can be preferred.

Third method, cross-coupled VCO, costs double VCO area. This option consumes less power than the buffers or limiters of the RC-CR network and master-slave flipflops designed for the frequency division method. This method also provides high voltage swing. For the phase mismatch of the outputs, layout of the two VCO should match well. The quadrature mismatch is less than five degrees [28].

Fourth method, quadrature ring oscillator, costs less chip area than cross-coupled VCO method. As it is a ring oscillator, the phase noise performance of the VCO will be worse than the options use LC VCOs. But the tuning range performance will be better. The matching of the delay cells is important for the quadrature phase mismatch.

More examples for quadrature oscillators are presented in [99,100].

## 5. DESIGN OF QUADRATURE LC AND RING VCOS FOR HIPERLAN2 SYSTEM

This chapter describes two different RF oscillators with quadrature outputs designed for HIPERLAN system, which has a frequency band of 5GHz-6GHz. Circuits are designed in 0.35 $\mu$ m BICMOS SiGe technology. First both of the circuits are explained and their simulation results are given then the circuit performances of the LC and ring quadrature VCOs are compared.

### 5.1 LC oscillator with Quadrature Outputs

#### 5.1.1 General Information

The circuit is designed for the test-chips of HIPERLAN project. Because this is a test chip, the biasing currents are given from the pads. The outputs are buffered for the test measurement system. As explained in section 4.4.3, the “injection locking” method is used to generate quadrature outputs. The connection of the oscillators is shown in Figure 5.1.

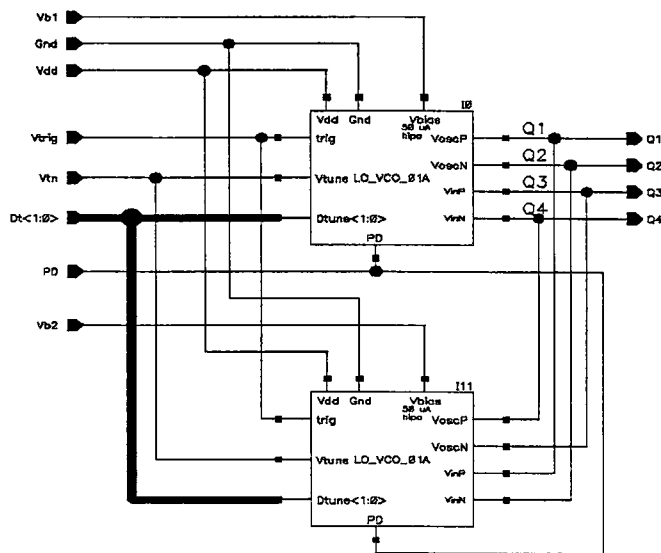


Figure 5.1 Injection locking of two oscillators



### 5.1.2 Circuit Description

The quadrature VCO is designed with cross-coupled VCO method as explained in Section 4.4.3. The two LC oscillators are identical. One of the LC oscillators is shown in Figure 5.2. This is a planar LC oscillator, which is explained in Section 4.2.1, with Figure 4.7. The only difference is that, MOS varactors are used for tuning, instead of junction capacitances (varactor diodes). The transistors M7 and M8, with the same size of M1 and M2, are used to couple the two oscillators for quadrature oscillation. The dimensions of the transistors are shown in Table 5.1

**Table 5.1** Dimension of the transistors in Planar LC oscillator

| Device Name | Aspect Ratio( $\mu\text{m}/\mu\text{m}$ ) |
|-------------|-------------------------------------------|
| M1,M2,M7,M8 | 70/0.35                                   |
| M3,M4       | 210/0.35                                  |
| M5          | 1000/0.7                                  |
| M6          | 20/0.7                                    |
| M9          | 2/0.35                                    |
| M10         | 16/2                                      |
| M11,M12     | 75/1                                      |

The gate lengths of the cross-coupled PMOS and NMOS transistors are chosen as the minimum value that technology satisfy, so that they work fast. The width of transistor M5 is chosen  $1000\mu\text{m}$  to drive nearly 5mA of current.

With an inductance value of  $0.8\text{nH}$ , the total capacitance on each node of oscillation must be between  $0.87\text{pF}$  and  $1.26\text{pF}$  to achieve an oscillation between 5-6GHz. The total capacitance of the LC-tank is formed by inductor's parasitic capacitance to the substrate, the gate-drain and gate-source capacitance of the NMOS and PMOS transistors, and the tuning capacitors from the MOS varactors.

#### 5.1.2.1 Tuning of the Oscillator

The frequency tuning of the oscillator is done with analog tuning and digital tuning. In both, MOS varactor circuits are used. The frequency band of the oscillator is between 5-6GHz. This band is divided into four frequency ranges. The digital tuning is used to switch from one frequency range to another inside the frequency band. Analog tuning is used for the tuning inside one of these ranges. Digital tuning is

obtained with 2-bit control. Analog tuning voltage is between 0.7V and 2.3V. The MOS varactor is shown in Figure 5.3. This type of MOS varactor is explained in Chapter 3. Digital tuning circuit is shown in Figure 5.4. This circuit consists of two MOS varactors connected in parallel. The MOS transistor dimensions of the digital tuning circuit are shown in Table 5.2. The dimensions of the transistors in the analog tuning circuit is already given in Table 5.1

**Table 5.2** Device dimensions of MOS varactor circuit

| Device Name     | Aspect Ratio( $\mu\text{m}/\mu\text{m}$ ) |
|-----------------|-------------------------------------------|
| M1A,M1B,M2A,M2B | 40/1                                      |

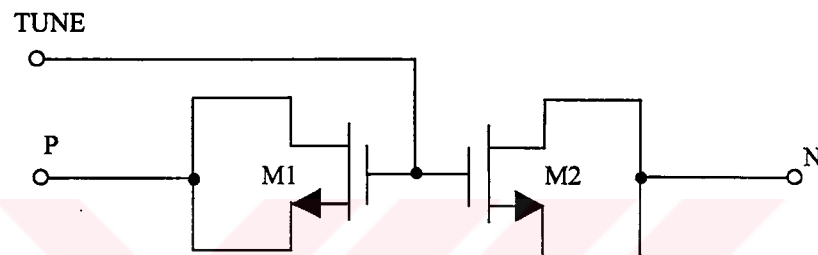


**Figure 5.3** MOS Varactor

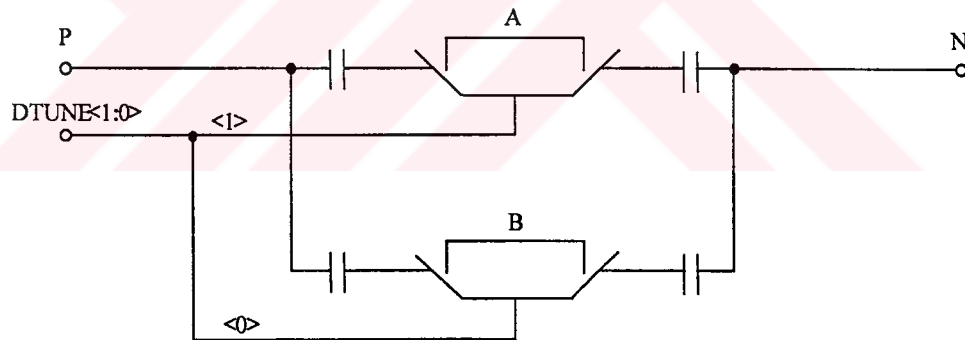


**Figure 5.4** Digital Tuning Circuit

### 5.1.2.2 On Chip Inductance

The inductance is a symmetrical one. Both Metal 2 and Metal 3 routing levels are used except for the cross sections, which use only one metal level for each direction. This coil is completely symmetrical and can be used as a differential floating inductor [13].

As mentioned in circuit description, the inductance value is chosen 0.8nH. The design of the inductor is a critical subject. It is directly related to layout design. In this design the coil is a symmetrical one. To reach the value of the inductor, a program which makes calculations, optimizations, is used. The program is called Spiral [101].

In this program, as input, you can either give the value of the inductor with some shape parameters or all shape parameters without the value. When you give the value of the inductor with some parameters, it draws the inductor how it wants because of the missing parameters. So it better to give all the shape parameters as input. The coil parameters are given in Table 5.3. The radius of the first inside turn, the width of the metal, the spacing between the metals and the number of the turns are the shape parameters given as input. The frequency range is also given as input for the calculation of the Q value. Depending on the user's specs, optimization can be done for Q or depending on some other parameter. For this design, the optimization is done for the value of the Q. In the given frequency range (5-6GHz) the maximum Q is found with optimization. Then with this value the shape parameters are once more modified. The results in Table 5.3 are the ones after optimization.

**Table 5.3** Optimal coil parameters

|                  |    |      |                   |
|------------------|----|------|-------------------|
| Radius           | r  | 40   | [ $\mu\text{m}$ ] |
| Width            | w  | 20   | [ $\mu\text{m}$ ] |
| Spacing          | Sp | 2    | [ $\mu\text{m}$ ] |
| No. of turns     | N  | 2    | -                 |
| Frequency        | F  | 5.5  | [GHz]             |
| Inductance       | L  | 0.8  | [nH]              |
| Total resistance | R  | 1.44 | [ $\Omega$ ]      |
| Quality Factor   | Q  | 10   | [-]               |

Up to now, the obtained values is especially for layout. But we also need a model of the inductor to use for the simulation. The program SPIRAL also creates a nine-element model for the inductor with the given parameters in Table 5.4. The model is shown in Figure 5.5

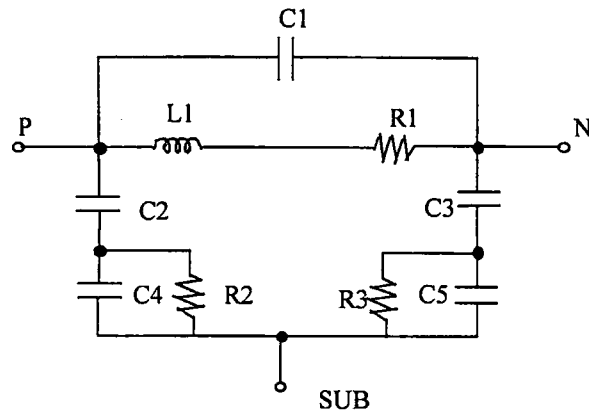


**Figure 5.5** Nine-Element Model of the spiral inductor

The values of the elements in the model are shown in Table 5.4.

**Table 5.4** Device values in the Nine-Element Model of the spiral

| Element    | Value            |
|------------|------------------|
| $C_1$      | 34.232fF         |
| $C_2, C_3$ | 159.885fF        |
| $C_4, C_5$ | 5.96969fF        |
| $R_1$      | 2,31407 $\Omega$ |
| $R_2, R_3$ | 2.1924K $\Omega$ |
| $L_1$      | 783.821pH        |

The layout of the spiral is shown in Figure 5.6.

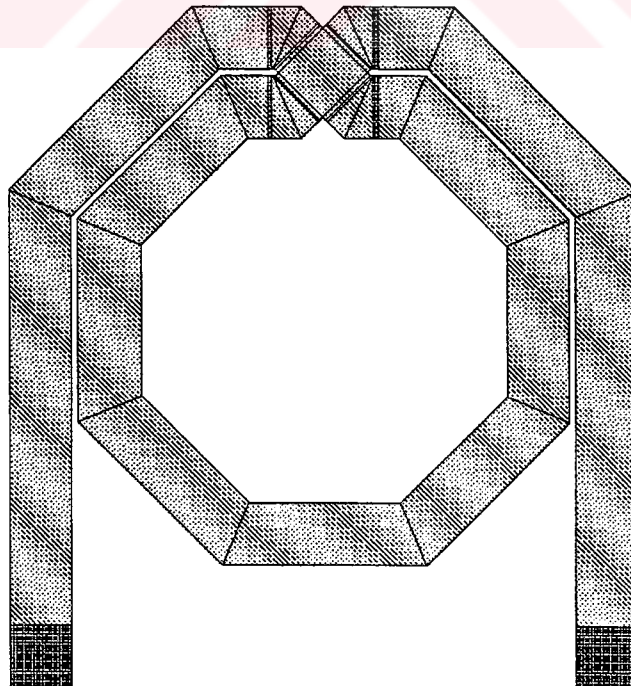


**Figure 5.6** Layout of the symmetrical inductor

### 5.1.2.3 Buffer circuit

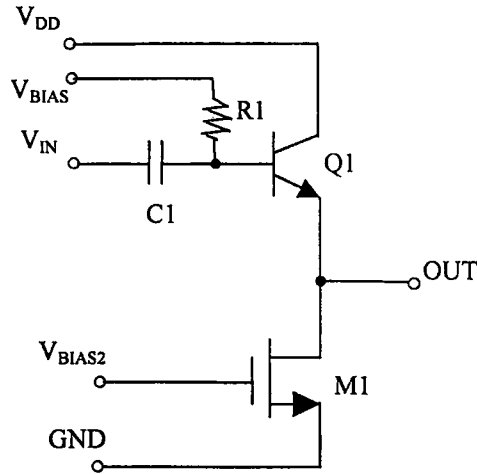


**Figure 5.7** Buffer circuit schematic

The outputs of the oscillator are buffered for the test chip. They are designed to drive  $50\Omega$  of load resistance. This load is the input impedance of the spectrum analyzer. As shown in Figure 5.7, the buffer circuit is a simple emitter follower.

The biasing of the MOS transistor comes from a simple current mirror, which is explained in the next section. The biasing of the NPN transistor is obtained from a voltage source over a resistor. The biasing voltage is given from the pads of the test chip. By this way, it is easy to control every transistor of the circuit from outside.  $V_{BIAS}$  voltage is 2.4V. C1 is used for DC coupling. The current flowing through each MOS transistor is 6mA. The dimensions of the devices are shown in Table 5.5. The BJT transistors used in this technology have six different emitter area choices. These are N1, N2, N4, N8, N16 and N32. Here N16 is used because the value of the current is large. It is better to use one with a big emitter area.

**Table 5.5** Dimensions of the buffer circuit

| Devices | Dimensions                                    |
|---------|-----------------------------------------------|
| R1      | $2K\Omega$                                    |
| C1      | 100fF                                         |
| M1      | $4\mu\text{m}/0.35\mu\text{m}$ (Aspect ratio) |
| Q1      | N16                                           |

The buffers lower the amplitude of the oscillation because the gain of the buffers is smaller than one. At these high frequencies it is not possible to design an ideal

emitter follower. Normally the oscillator achieves high amplitudes, but for the test chip it is better to have low values for easier measurements.

#### 5.1.2.4 Biasing circuit

Two biasing circuits are used for the test chip. One is for the oscillators the other is for the buffers. The circuit design of both is the same only the dimensions of transistors are different. The bias circuit is shown in Figure 5.8. This is a simple current mirror circuit with power down mechanism. The biasing current is given directly from the pads to the  $I_B$  input. For the biasing of oscillators, the output of the bias circuit is connected to the  $V_{BIAS}$  input of oscillator. The current flowing from  $I_B$  input is  $50\mu A$  for the oscillator biasing.

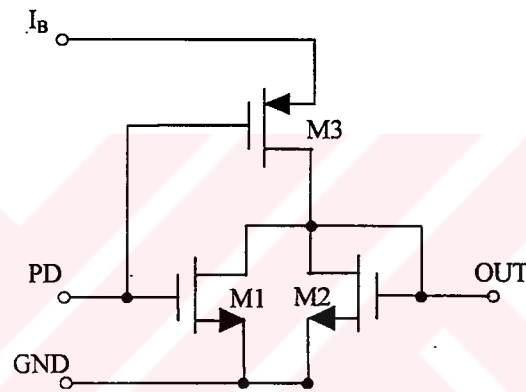


Figure 5.8 Biasing circuit

For biasing the buffers, the output of the circuit is connected to the  $V_B$  input of the buffers. The current flowing from the  $I_B$  input is  $100\mu A$  for buffer biasing. The device dimensions are shown in Table 5.6.

Table 5.6 Device dimensions of the biasing circuits

| Device Name | Aspect Ratio( $\mu m/\mu m$ ) |                        |
|-------------|-------------------------------|------------------------|
|             | Oscillator biasing circuit    | Buffer biasing circuit |
| M1          | 2/0.32                        | 4/0.5                  |
| M2          | 8/2                           | 4/1                    |
| M3          | 10/0.35                       | 10/0.35                |

#### 5.1.3 Discrete realization of quadrature LC oscillator

Before designing the IC quadrature LC oscillator, the same oscillator is realized with discrete components to verify the theoretical predictions, which are explained in

Chapter 4. The discrete design of the LC oscillator is designed to oscillate at 5MHz. The aim of this design is to see the quadrature phase difference of the outputs. The test is very helpful to understand the behaviour of the quadrature oscillator. The setup for the test circuit schematic is shown in Figure 5.9.

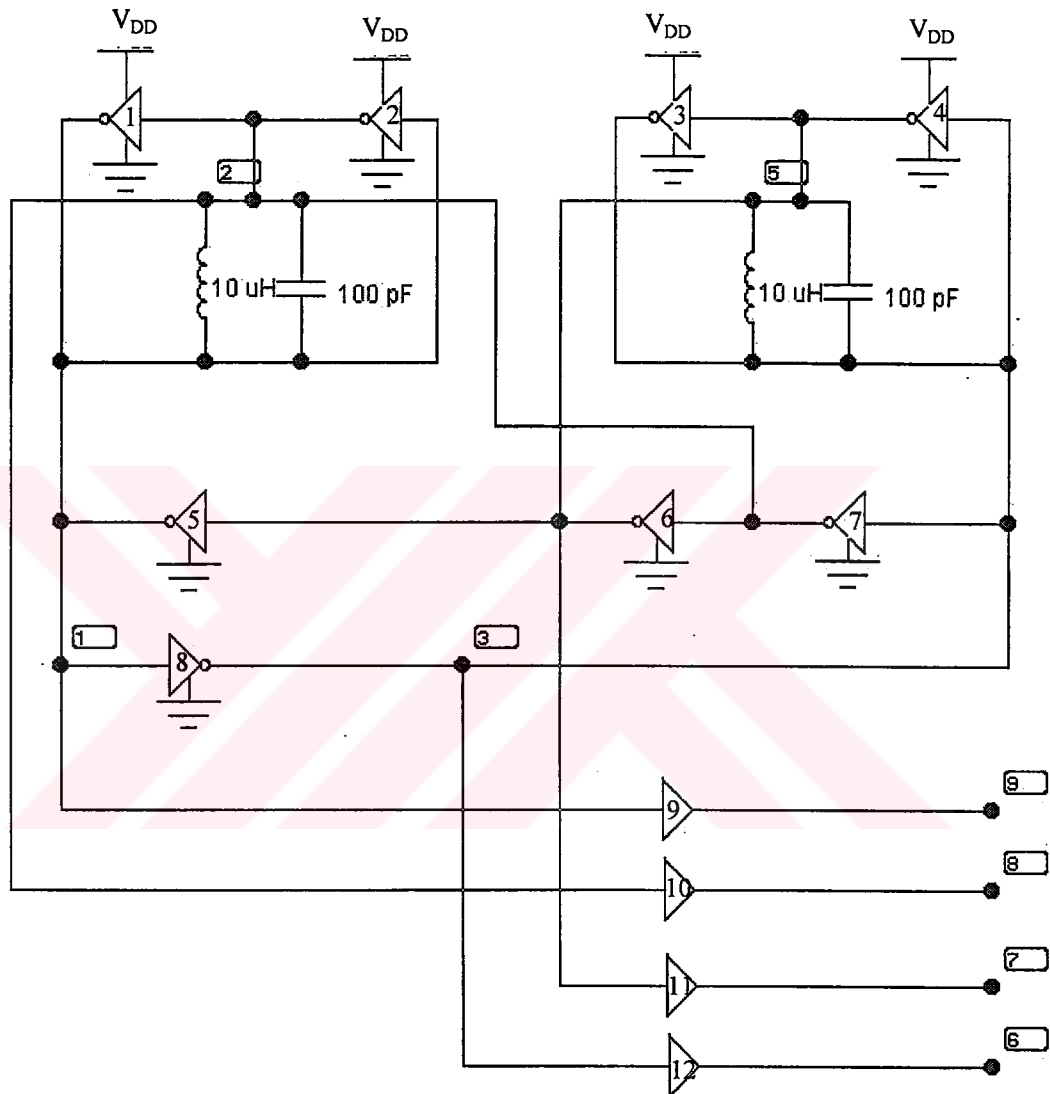


**Figure 5.9** Discrete quadrature LC oscillator circuit schematic

This schematic consists of two LC oscillators connected with injection locking method as explained in section 4.4.3. Each oscillator schematic is another type of draw of the amplifier part of the quadrature LC oscillator in Figure 5.2. so this discrete design is totally same with its IC design as shown in Figure 5.1.

The inverters (1-8) in the circuit, are unbuffered HEF4049UB inverter gates. The devices (9-12) are emitter follower type buffers, which are added to the circuit to

drive  $50\Omega$  load. This is the input of the spectrum analyzer. Inverters (1-4) resemble the cross-coupled NMOS and PMOS transistors of the oscillators and inverters (4-8) resemble the NMOS transistors, which couples the two LC oscillators for quadrature oscillation.

The circuit is designed to oscillate around 5MHz. Therefore the tank circuit elements are chosen as  $L=10\mu\text{H}$  and  $C=100\text{pF}$ . The two identical LC VCO oscillate around 5MHz and the initial frequency difference of them is as low as 10kHz.

The supply voltage  $V_{DD}$  used for this design is 5V. With typical conditions the oscillation frequency of the quadrature oscillator is 4.8826MHz. The phase difference between the outputs is measured from the oscilloscope which is  $\pm 5$  degrees. When one of the oscillators is removed from the quadrature circuit, one oscillator oscillates at 4.708MHz. We can see that the oscillation frequency does not change very much. From the measurements it has been seen that the quadrature LC VCO starts to oscillate very easily, and its frequency did not change after every start-up under certain conditions. As a conclusion the quadrature oscillator works properly with injection locking method.

#### **5.1.4 Simulation Results of the IC quadrature LC oscillator**

After the design of the blocks, the effects of the layout should be included to the circuits for realistic simulation results. These effects can be listed as, the parasitics which come from the layout, some device model parasitics which are not well modeled in the device models of the technology.

The most important parasitics comes from the planar LC circuit. The circuit schematic prepared for simulation is shown in Figure 5.10. These parasitic capacitances are between two metals from the layout, which are called as fringing capacitors. The values of the capacitors are estimated for this design from the previous experiences. The parasitics mostly come from the two outputs of the oscillator.



which connects the gates and they are also the outputs. Therefore between these metals there is the fringing capacitance. The same effect comes from the cross-coupled PMOS transistors.

C5 and C6 are fringing the capacitors, from the metal used for  $V_{cont}$ , to each of the outputs. C0 and C1 are fringing capacitors from VDD to the outputs. C3 and C4 are the fringing capacitors from outputs to the GND.

For the simulation, we have to trigger the oscillators to start oscillation. The MOS transistor M40 is connected parallel with one of the coupling transistors for triggering. The trigger signal is applied to the gate of the transistor. Transistor M38 is added to the circuit as dummy transistor to give the same effect as M40. All of the simulation schematics of this design are given in Appendix C.

#### 5.1.4.1 Typical Results

Three different design environments are used which are Analog Artist, Made and HP advanced design system HP-ADS. The Periodic Steady State (PSS) and transient simulations are done with Spectre RF. The characterization simulations and Monte Carlo simulations are done with eldorf. Phase noise simulation is done with HP-ADS. In Table 5.7, some stimuli values of the circuit are given for typical conditions.

**Table 5.7** Typical stimuli values for LC oscillator

|                      | Typical Values |
|----------------------|----------------|
| Temperature          | 27 degrees     |
| Analog Tune (Vtune)  | 700mV          |
| Digital Tune (Dtune) | 00             |
| Supply Voltage       | 3.3V           |
| Device Models        | Typical        |

With the given typical conditions transient and PSS simulations are done. In Figure 5.11 the transient response of circuit is shown. The circuit achieves the quadrature outputs.

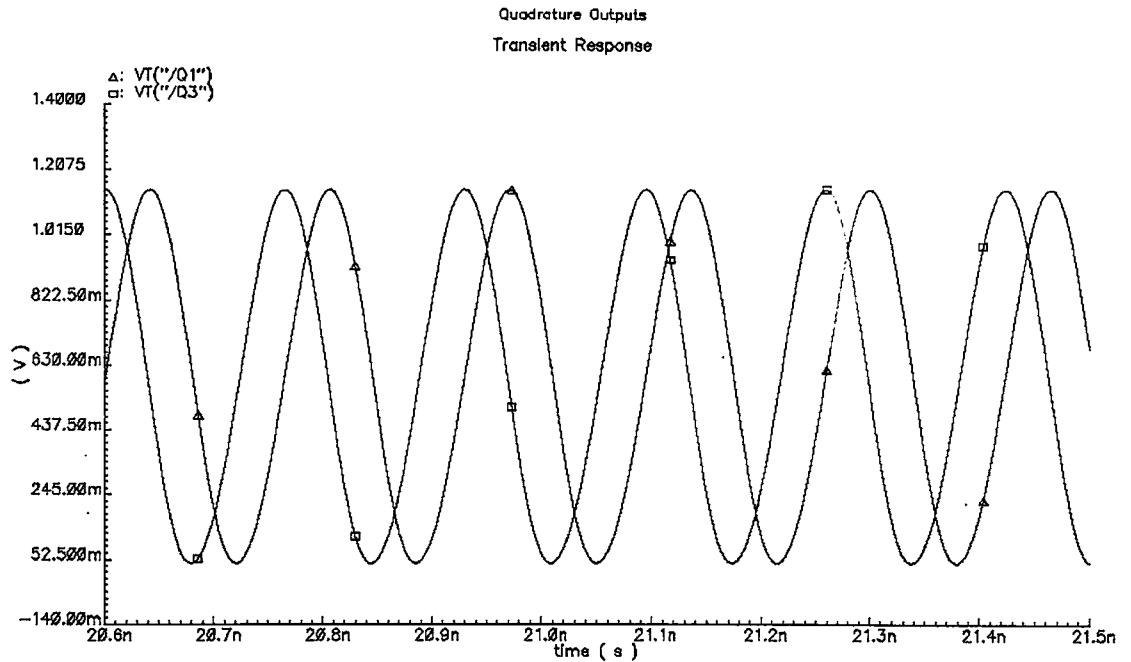


**Figure 5.11** Quadrature Outputs of the oscillator

Also to see the 90 degrees difference between the outputs, PSS analysis is done. The result is shown in Figure 5.12. At 6GHz where the circuit oscillates, there is -90 degrees difference between two outputs.

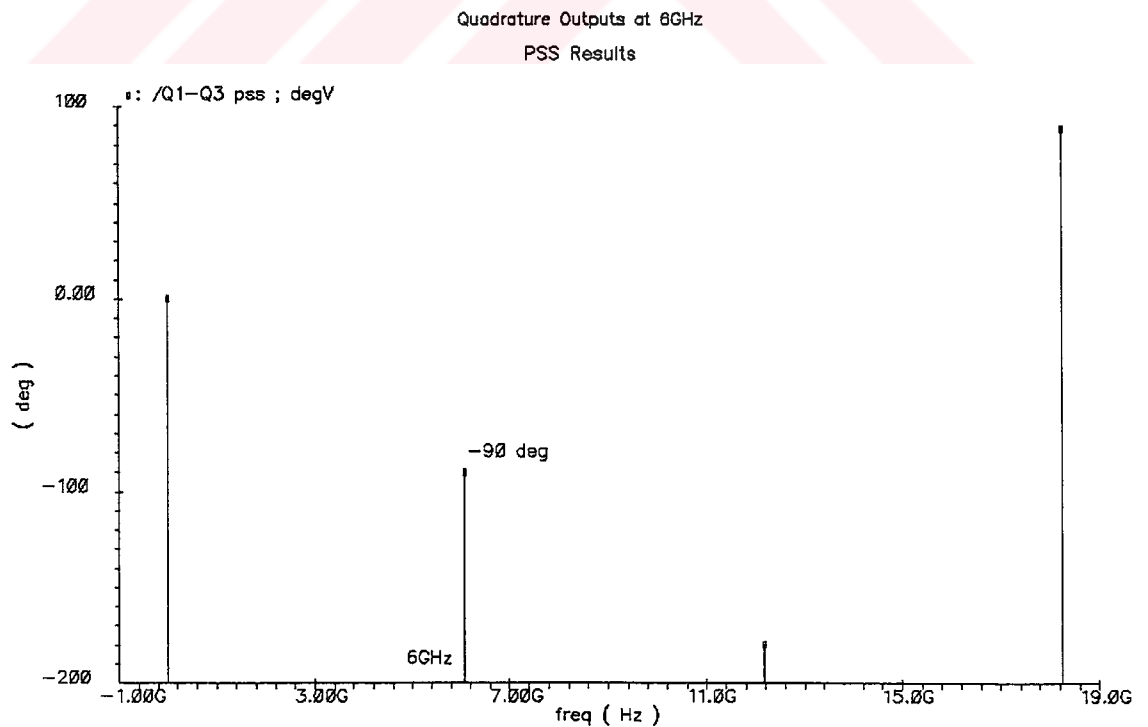


**Figure 5.12** Phase difference of outputs

In this circuit, there is no amplitude difference between quadrature outputs. The amplitude difference is shown in Figure 5.13.

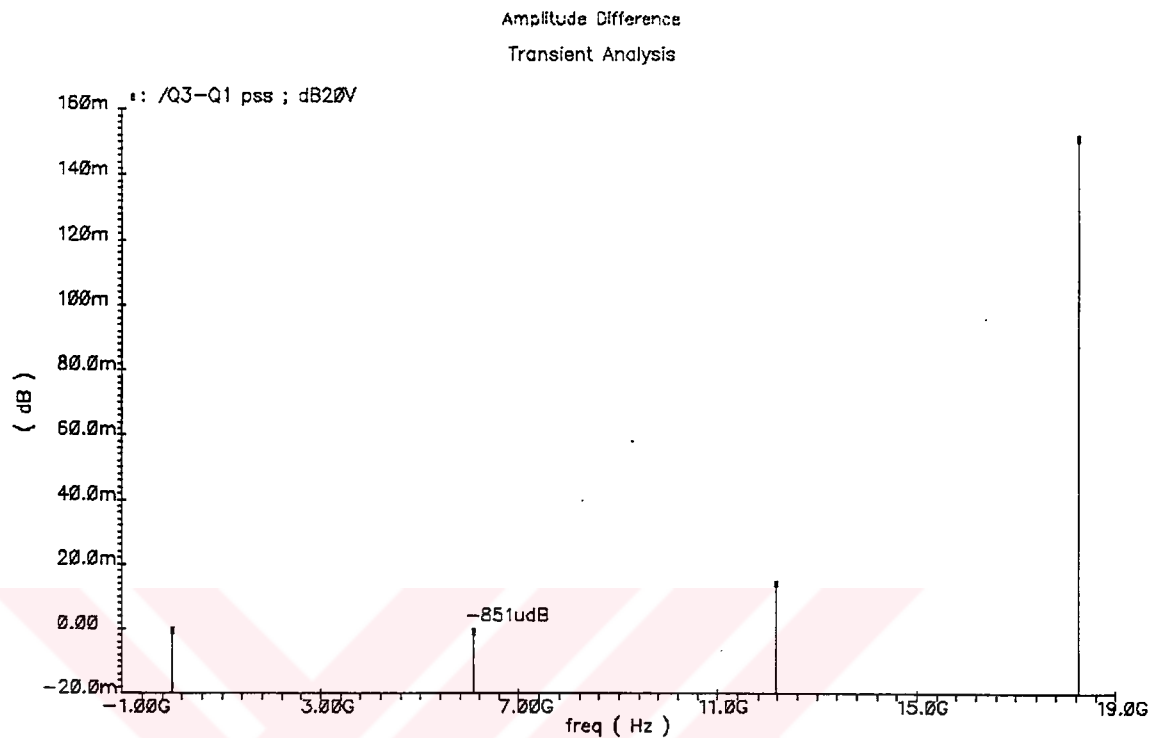


**Figure 5.13** Amplitude Difference of Quadrature Outputs.

The tuning range of the oscillator is shown in Figure 5.14 where the analog tuning voltage is changed between 0.7V and 2.3V and the digital tuning has four different levels which are 00,01,10 and 11. The four-frequency range is easily seen from the results as explained in the section 5.1.2.1

The simulation results given above are done with Spectre. But the total simulations of the circuit are done with Eldo RF, because the corner device models for this technology are only available for the simulator Eldo. The total simulation results are shown in Table 5.8. Here there are differences between the simulation results with Spectre (shown in figures above) due to the calculation of device parameters of each of the simulators.

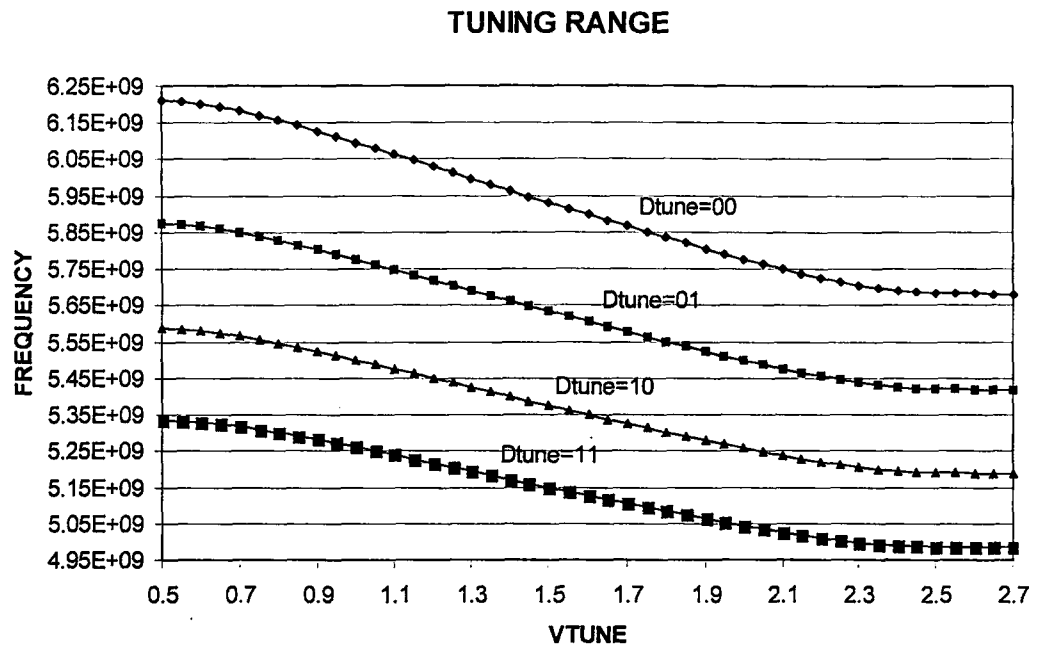


**Figure 5.14** Tuning Range of the LC Quadrature oscillator

**Table 5.8** Typical Simulation Results of LC oscillator (Eldo)

|                                 | TUNING       |              |
|---------------------------------|--------------|--------------|
|                                 | 1 (Dtune:11) | 2 (Dtune:00) |
| FREQUENCY(GHz)                  | 4.917        | 6.126        |
| AMPLITUDE(V <sub>pp</sub> diff) | 0.374        | 0.55         |
| PHASE DIFF.(degrees)            | 90           | 90           |
| AMP. DIFF.                      | 0            | 0            |
| TUNING RANGE                    | 1209MHz      |              |

The circuit oscillates between 5.917GHz and 6.126GHz at typical conditions, having a tuning range of 1209MHz. The amplitude difference between the outputs is negligible. The phase difference between the output is 90 degrees, achieving quadrature outputs. The amplitude of the oscillator is calculated as peak to peak value of the differential outputs. The real performance of the circuit is determined after the characterization simulations.

#### 5.1.4.2 Characterization Simulations of the Quadrature LC VCO

Characterization simulation is the simulation, which is done to see the effects of process variation, temperature variation and supply variation on the circuit performance. The design specs of the circuit should be satisfied in all kind of

conditions. In the characterization simulations, the best and the worst value of the parameters are used. For example in our design, the supply differs from 3V to 3.6V and the temperature can change from  $-10^{\circ}$  to  $70^{\circ}$  degrees. In the simulations, the maximum and the minimum value of the stimulus, which are called corner values, are used. Slow and fast models are used for devices like MOS transistors, BJT transistors, resistors and capacitors. For this design totally 128 different simulations run for all characterization. But in each all devices of the same type is effected at the same time, in the same way. For example, if in one of the simulation, fast model runs for PMOS transistor, all PMOS transistors have the fast model. So we can examine the deviations with only one way at the same time. The results, which are shown in Table 5.9, are the ones reported for the worst case.

**Table 5.9** Characterization Results of LC oscillator

|                                 | MIN     | MAX    |
|---------------------------------|---------|--------|
| FREQUENCY(GHz)                  | 5.008   | 5.969  |
| AMPLITUDE(V <sub>pp</sub> diff) | 0.2     | 0.72   |
| PHASE DIFF.(deg)                | 90      | 90.125 |
| AMP. DIFF.(Volt)                | -0.0401 | 0.0673 |
| TUNING RANGE                    | 961MHz  |        |

In characterization simulations, the results that are the worst of all, determines the performance of the circuit. The tuning range of the oscillator is lower now when compared with typical results. The maximum phase difference is  $90.125^{\circ}$  degrees. This value is also inside our design spec. The amplitude difference results are peak to peak and differential voltage values. Normally the LC oscillator can achieve bigger oscillation amplitudes but the buffers decrease the amplitudes. But this is better for measurements of the test chip. We know that the oscillation amplitude of the amplifier structure of this LC VCO is approximately a factor of two larger than that of the nMOS-only structure due to the pMOS pair [102,103]. The amplitude difference between two quadrature outputs is very small which is 0.0673V maximum.

#### 5.1.4.3 Monte Carlo Results

As mentioned before, characterization simulations calculate only one way of deviation at the same time. But we also need to see the deviations of different ways

for the same type of devices. Beyond the process variations, there can be mismatches of the devices due to the layout. For example, when you draw two MOS transistors with same dimension, but far away from each other, it is possible that they will not be identical. This is because of the process. This type of analysis can be done with Monte Carlo simulation.

In this simulation, you give some deviations to some parameters of the devices. This can be done to some of the devices in the design while the others can stay with typical models. So we are able to apply the simulation for our critical devices. In this design the Monte Carlo simulations are done for NMOS transistors and PMOS transistors. The transistors are chosen according to their effect in the circuit.

For this design the effective transistors are the one in planar LC oscillator circuit. The PMOS current source transistor M5, double cross connected NMOS transistors M1 and M2, double cross connected PMOS transistors M3 and M4 and varactor transistors M11 and M12 are most effective ones for the oscillation frequency, phase and amplitude. For these transistors, their current matching is simulated. The current matching can be divided into two subjects, the mismatch of  $\beta$  and mismatch  $V_T$ . These two parameters of the MOS transistor are changed with the amount of deviation. Both of the deviations are calculated with the formula given in Equation 5.1

$$\sigma^2 = \frac{A^2}{WL} + B^2 \quad (5.1)$$

A and B are the parameters given from the technology which are different for a PMOS and NMOS transistor. The deviation is inversely proportional with the area of the transistor. When the area is greater, the mismatch errors are smaller. The  $\beta$  deviation is calculated as a percentage value. The  $V_T$  deviation is calculated in mVolts. According to our technology and to the area of the transistors, the calculated deviations of the transistors,  $\beta$  and  $V_T$  deviation values are given below in Table 5.10.

**Table 5.10** Deviation value for the MOS transistors

| Device Name   | Deviation            |                     |
|---------------|----------------------|---------------------|
|               | $\beta$ Deviation(%) | $V_T$ Deviation(mV) |
| PMOS M5       | 0.33                 | 0.33                |
| PMOS M3, M4   | 0.46                 | 1.19                |
| NMOS M1, M2   | 0.46                 | 1.93                |
| NMOS M11, M12 | 0.4                  | 1.61                |

For the simulation, all other devices have typical models and the stimuli values of the circuit, like supply voltage, temperature, tuning voltage are in typical values. Totally 250 runs are made. This number of simulation is enough to make a statistic.

The results of the total simulation are given below.

|                                             |            |
|---------------------------------------------|------------|
| Phase Difference (max)                      | : 90.19°   |
| Phase Difference Error (Standard deviation) | : 0.07°    |
| Amplitude Difference (max)                  | : 0.027 dB |
| Amplitude Difference (Standard deviation)   | : 0.007 dB |
| Frequency Difference (max)                  | : 2 MHz    |

The phase difference between two outputs is maximum 90.19° and the standard deviation of the phase difference error is 0.07° degrees. The maximum amplitude difference between two quadrature outputs is 0.027dB and the standard deviation is 0.007dB, which is negligible. The maximum deviation from the typical oscillation frequency is 2MHz. The oscillation frequency and the amplitude difference are not so much effected by the mismatch of transistors. Phase difference is the one mostly effected from the process variations.

#### **5.1.4.4 Phase Noise Simulation**

The phase noise simulation is done separately with simulator HP-ADS. Therefore the phase noise results couldn't be examined with characterization and Monte Carlo simulations. The phase noise calculation of HP-ADS simulator is explained in Appendix B.

The most effective devices to phase noise are the double crossed NMOS and PMOS transistors. The phase noise result is shown in Figure 5.15. At 10MHz offset frequency, the phase noise is nearly -123dBc/Hz. This phase noise calculation is also done with eldorf. With that simulator at the same offset frequency the phase noise is

-114dBc/Hz. The difference of the result between two simulators arrive from the device models and simulation methods.

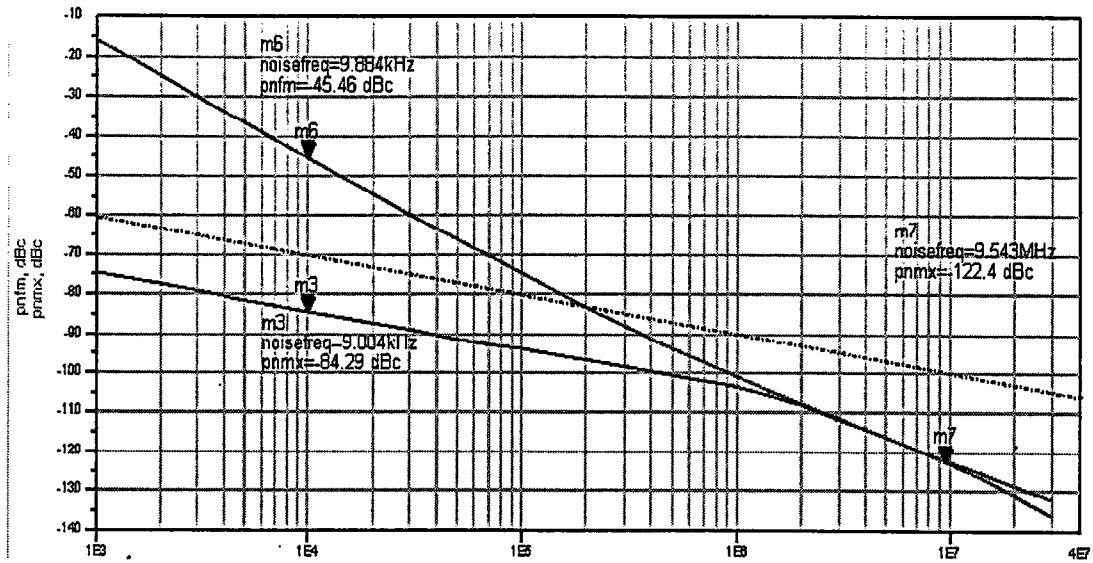


Figure 5.15 Phase Noise Results (HP-ADS)

### 5.1.5 Layout

After the simulations, the schematics are prepared once more for the layout. All the MOS transistors, which are directly connected to the PAD, are chosen from IO MOS transistors. They are also MOS transistors but they have larger drain area than the normal MOS transistors. The length of the drain is determined by the technology. These transistors are stronger than the others are, and they can drive more current. Therefore they are used for protection.

For ESD protection, both metals of the capacitors are connected to ground via diodes. Each of the simple current mirrors is filtered for high frequency signals.

Decoupling capacitors are used for VDD and GND. All the schematics of the design for simulations and layout are shown in Appendix C. In Figure 5.16, the layout of the test chip is shown. The symmetry in the layout is very important for proper operation. The RF outputs are measured with GSSG (Ground-signal-signal-ground) pad configuration. These four pads have to be 150μm far away from each other from their middle point for the measurement by the probe station. Three metal layers are used for the circuit layout, metal four is used to connect the positive and negative connections of the pads.

The VDD and GND connections are done also with symmetrical metals from different parts of the chip. The metals, which carry the RF signals, are shielded from each other to prevent coupling of the signals. The total chip area is  $1300\mu\text{m} \times 1300\mu\text{m}$ .

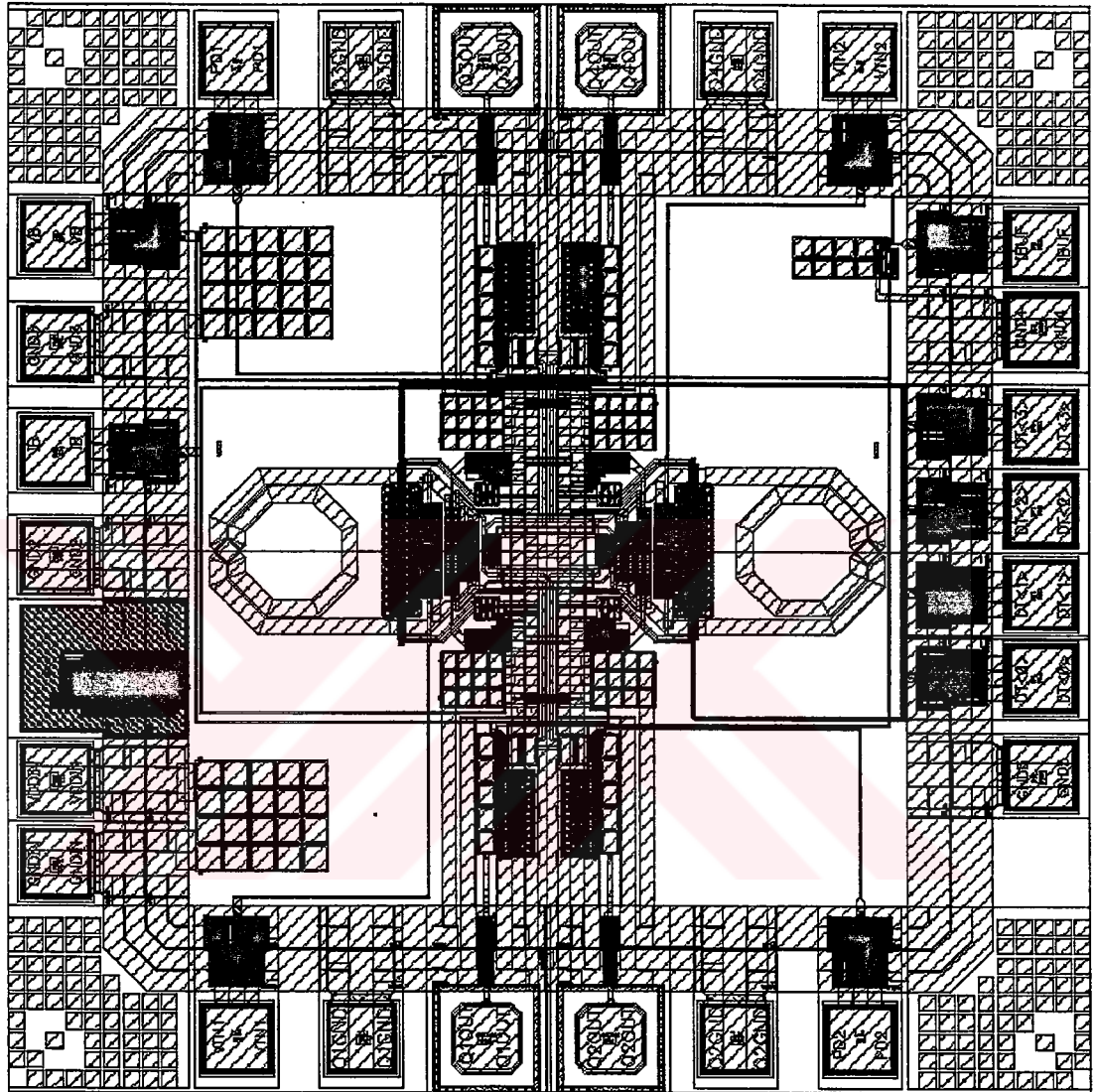


**Figure 5.16** Layout of the test chip of the quadrature LC oscillator



## 5.2 Ring Oscillator with Quadrature Outputs

### 5.2.1 General Information

Quadrature ring oscillator circuit is also designed for HIPERLAN project as a test chip. As mentioned before, even numbers of delay cells are used to provide quadrature outputs. Here two delay cells are used. The oscillator is buffered again for the test measurements. The top-level schematic is shown in Figure 5.17.

### 5.2.2 Circuit Description

The quadrature ring oscillator is designed with the method as explained in Section 4.3.4 which uses even number of delay cells to have quadrature outputs. In this design two delay cells are used to achieve quadrature signals. The frequency control is done with both controlling tail current and gate voltage of the PMOS transistors in the delay cell to minimize the swing variation. This type of ring VCO is explained Section 4.2.2 in Figure 4.9. The delay cell is designed with a differential BiCMOS pair as shown in Figure 5.18. This is a typical differential pair with BJT buffers. In typical conditions, same amount of current flows from M3, M4 and M5, which is nearly 1.2mA. The PMOS transistors operate in triode region, each acting as a variable resistor controlled by the analog tuning voltage indirectly helping to change the oscillation frequency. The dimensions of the transistors in this delay cell are shown in Table 5.11.

The dimensions of the MOS transistors are a big concern. There is trade-off between the oscillation frequency and mismatch of the circuit. Both of them depend on the dimensions PMOS transistors. First, as it will be explained in next sections, in Monte Carlo simulations it is seen that PMOS transistors in the delay cell M1 and M2 are the most effective ones on the mismatch results of the circuit. Secondly, these transistors are very effective on the oscillation frequency as they act as variable resistor. The oscillation frequency is very sensitive to the width of the transistors. Proper dimension should be chosen which satisfies the exact oscillation frequency with minimum phase mismatch. For NMOS transistors, only M5 is effective on mismatch. Therefore, the dimensions of M5 are chosen as its area to be bigger but having same W/L ratio with M3 and M4, as they drive the same current. As

explained in Equation 5.1, the area of the transistor is effective on the mismatch, but we also know that for layout mismatches when the channel length of the transistor is bigger, it is better for the mismatch. Hence, the length of the transistor M5 is chosen  $3\mu\text{m}$ .

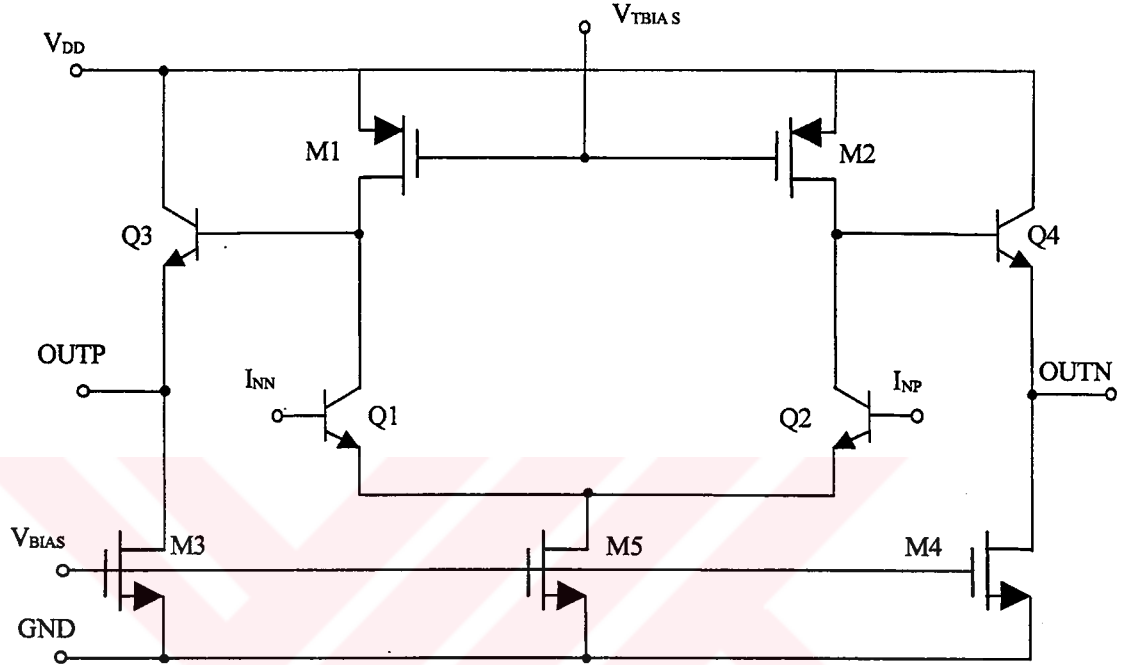


**Figure 5.18** Differential delay Cell

**Table 5.11** Dimension of the transistors in delay cell

| Device Name | Dimension                             |
|-------------|---------------------------------------|
| M1, M2      | 48/0.45 ( $\mu\text{m}/\mu\text{m}$ ) |
| M3,M4       | 83.6/2 ( $\mu\text{m}/\mu\text{m}$ )  |
| M5          | 125.4/3 ( $\mu\text{m}/\mu\text{m}$ ) |
| Q1,Q2,Q3,Q4 | NH8                                   |

### 5.2.2.1 Tuning of the oscillator

An analog voltage is used to tune the oscillator. The simple diagram of the tuning system is shown in Figure 5.19. The circuit can be divided into two parts as NMOS biasing and PMOS biasing. The first part, which is called NMOS biasing, supplies bias gate voltage for NMOS transistors in the delay cell. Therefore they tune the tail current of the delay cell. The second part, which is called PMOS biasing, supplies bias gate voltage for the PMOS transistors in the delay cell. This voltage tunes the PMOS transistors to change the oscillation frequency.

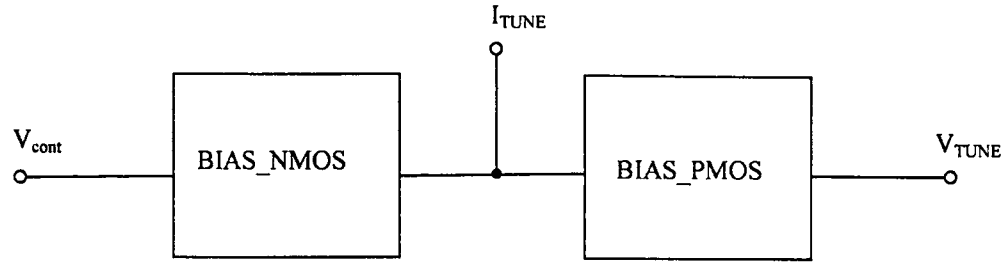


**Figure 5.19** Bias Circuit

The NMOS biasing part is shown in Figure 5.20. The input voltage  $V_N$  is the tuning voltage, which is between 0.4V and 1.6V. In this circuit the tuning voltage is converted to current over a resistor with a simple feedback circuit. Then the simple PMOS current mirror mirrors this current which is proportional to the tune voltage. The transistor M4 will mirror the tuning current. The OUT pin is connected to the gate of NMOS transistors in the delay cell, also to the NMOS transistors in the next PMOS biasing cell. The dimensions of the devices are given in Table 5.12

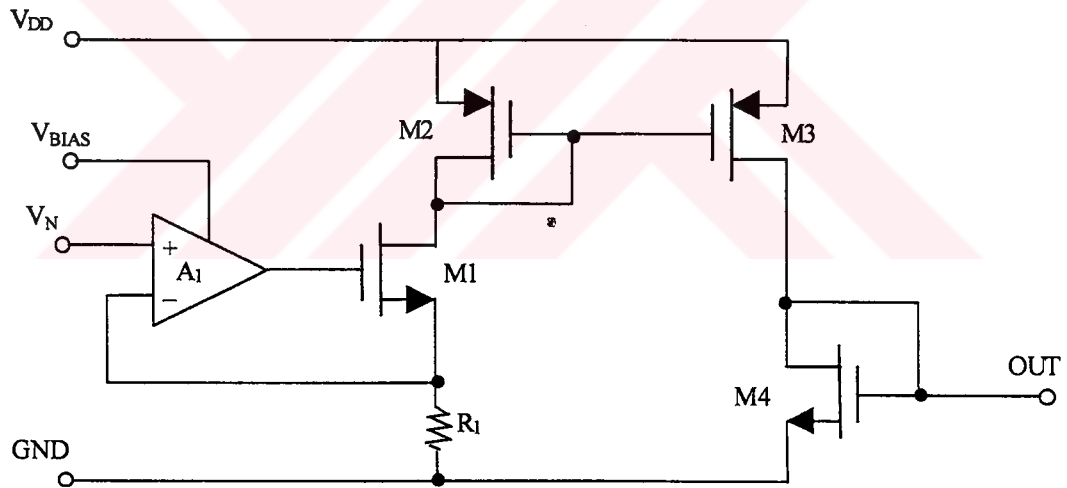


**Figure 5.20** NMOS Bias Circuit

**Table 5.12** Dimensions of the devices in NMOS bias circuit

| Devices | Dimensions and Values                                |
|---------|------------------------------------------------------|
| R1      | 3.2K $\Omega$                                        |
| M1      | 100 $\mu\text{m}$ /0.65 $\mu\text{m}$ (Aspect ratio) |
| M2, M3  | 140 $\mu\text{m}$ /1 $\mu\text{m}$ (Aspect ratio)    |
| M4      | 20.9 $\mu\text{m}$ /2 $\mu\text{m}$ (Aspect ratio)   |

The op-amp circuit  $A_1$ , used in the NMOS biasing circuit is shown in Figure 5.21.

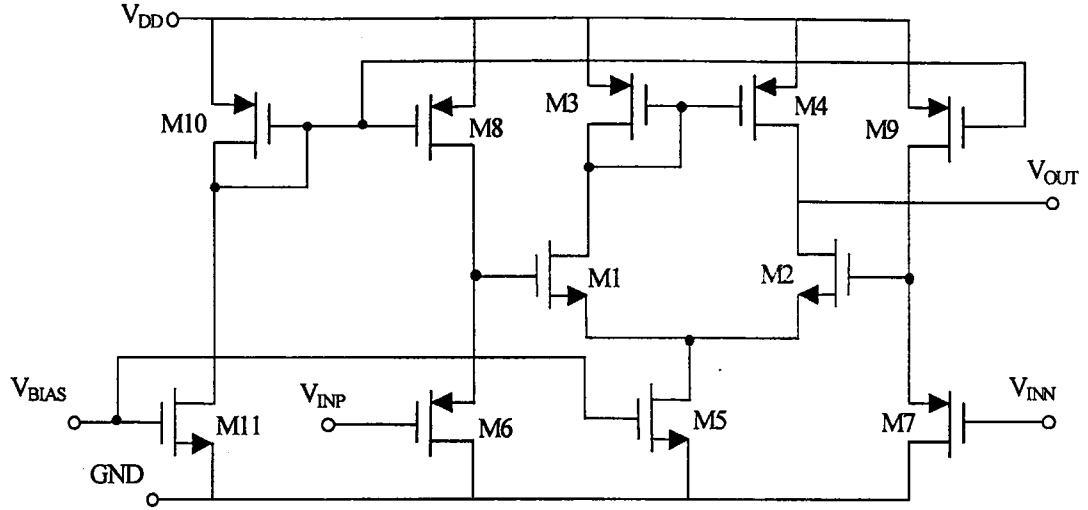


**Figure 5.21** The schemataic of the op-amp used in the NMOS basing circuit

The design of this op-amp circuit is also critical because the input voltage range is between 0.4V and 1.6V. The op-amp is a simple differential pair with PMOS level shifters. The use of level shifters is a must as 0.4V input voltage is not enough to drive transistors M2 (or M1) and M5 with only differential pair. The dimensions of the transistor are given in Table 5.13. All of the dimensions are optimized very carefully. The circuit should work properly within all characterization conditions, satisfying the minimum input offset voltage error. All of the transistors should stay in saturation region for proper work and stability.

**Table 5.13** Dimensions of the devices of the op-amp circuit for NMOS biasing circuit.

| Device Name | Aspect Ratio( $\mu\text{m}/\mu\text{m}$ ) |
|-------------|-------------------------------------------|
| M1, M2      | 60/1                                      |
| M3,M4       | 20/0.5                                    |
| M5          | 30/1                                      |
| M6, M7      | 75/0.45                                   |
| M8, M9, M10 | 15/0.5                                    |
| M11         | 10/1                                      |

The PMOS biasing circuit is shown in Figure 5.22. This circuit is the second part of the tuning system, which obtains the control voltage for the PMOS transistors in the delay cell. The input voltage of the circuit  $V_{IN}$ , is supplied by the NMOS biasing circuit, which changes with the control voltage. The resistor dividers are used to fix the  $V_{DS}$  voltage of the PMOS transistor to guarantee that it stays in triode region. Therefore the dividers also satisfy a stable oscillation frequency region. The gate

voltage of M1 changes with the supply voltage and the tuning voltage. The output of the circuit is connected to the gate voltage PMOS transistors in the delay cell.

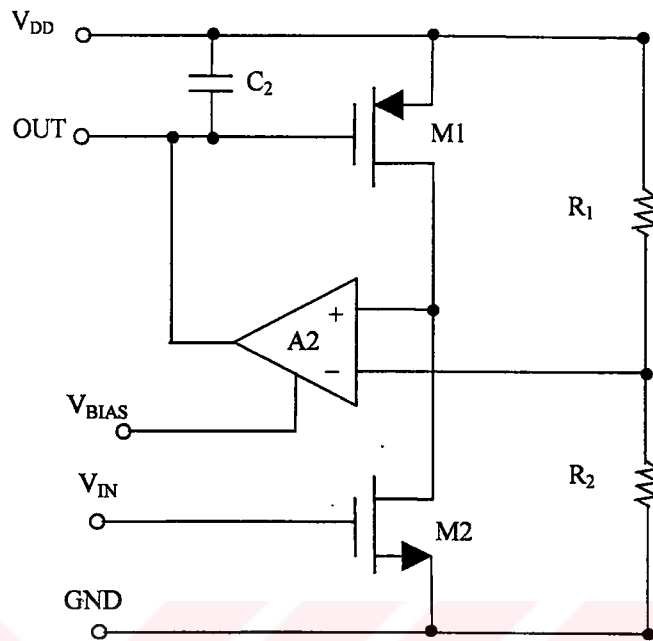


**Figure 5.22** PMOS bias circuit

The device dimensions and values are given in Table 5.14.

**Table 5.14** Dimensions of the devices of the PMOS bias circuit

| Devices | Dimensions                                          |
|---------|-----------------------------------------------------|
| R1      | 750 $\Omega$                                        |
| R2      | 9250 $\Omega$                                       |
| C1      | 1pF                                                 |
| M1      | 24 $\mu\text{m}$ /0.45 $\mu\text{m}$ (Aspect ratio) |
| M2      | 20.9/2                                              |

The op-amp circuit (A<sub>2</sub>) used in PMOS biasing circuit is shown in Figure 5.23.

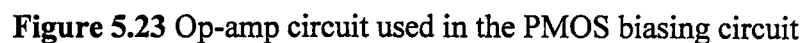


**Table 5.15** Dimensions of the devices in the op-amp circuit of PMOS bias circuit.

The biasing of the transistors in PMOS and NMOS biasing circuits are obtained by three diode-connected NMOS transistors as shown in Figure 5.24. The output pin of the circuit is connected to gate of transistors M11 in NMOS biasing cell, M5, M6, M7 in PMOS biasing cell. The aspect ratio of the transistors is  $4\mu\text{m}/1\mu\text{m}$ .

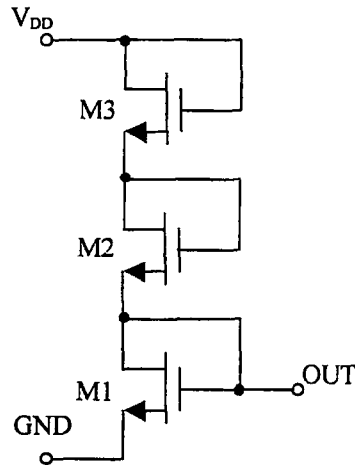


**Figure 5.24** Bias circuit for NMOS biasing and PMOS biasing circuits

### 5.2.2.2 Buffer circuit

The buffer circuit is shown in Figure 5.25. It is very similar with the emitter follower used in LC oscillator circuit. Biasing of the transistor is satisfied by the NMOS biasing circuit. So the current of the buffer changes with the tuning voltage. The input of the BJT transistor is directly connected to the output of the delay cell. The dimensions of the devices are shown in Table 5.16.

**Table 5.16** Dimensions of the devices in buffer circuit

| Devices | Dimensions                                         |
|---------|----------------------------------------------------|
| M1      | 83.6 $\mu\text{m}$ /2 $\mu\text{m}$ (Aspect ratio) |
| Q1      | NH4                                                |

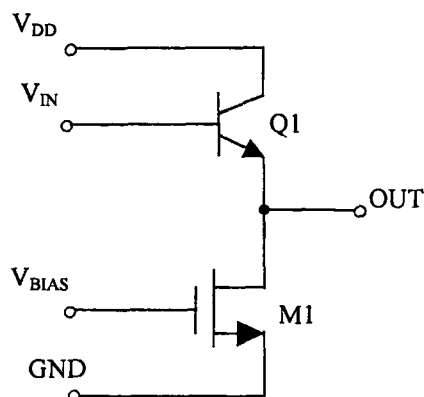


**Figure 5.25** Buffer circuit for ring oscillator

### 5.2.3 Simulation Results

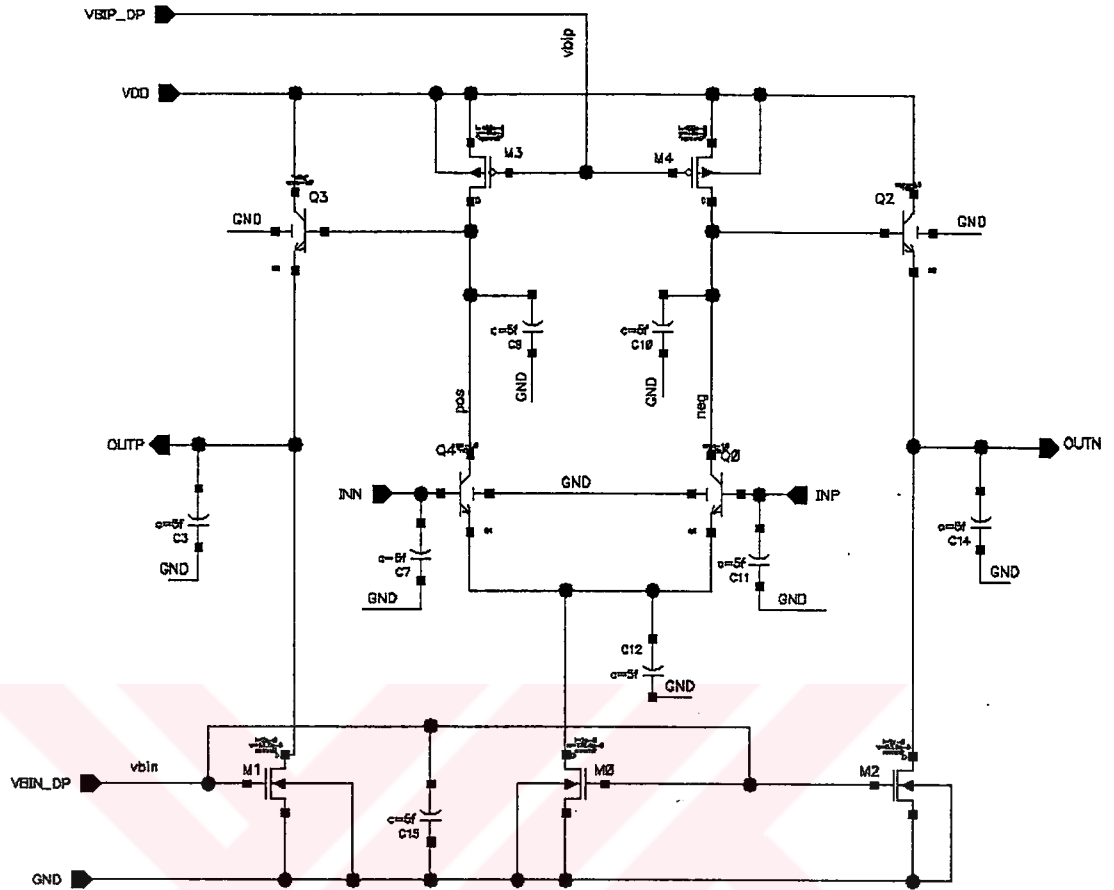


**Figure 5.26** Simulation schematic of the delay cell

As we have mentioned in the simulation results section of the LC oscillator, the quadrature ring VCO circuit is also prepared for the simulations. To symbolize the layout effects, for critical nodes of the circuit, 5fF of capacitance are connected from the nodes to GND. As an example the schematic of the delay cell with parasitics is shown in Figure 5.26.

In the MOS transistor models, there are some optional parameters that change the default property of the transistor. One of the optional parameter is GEO parameter. This is a switch parameter, which determines the layout of the device. The default value of this parameter is GEO= 0, which indicates that the drain and the source of the device are not shared by the other devices. In our design all the MOS transistor's GEO parameter is GEO=1, which indicates the drain is shared with another device. This is used to decrease the parasitic capacitance of the MOS transistor. The change

in the value of capacitance of the transistor will change the oscillation frequency. Therefore changing the GEO parameter of the MOS transistors in the delay cell is most effective. The parameter change of the MOS transistors in the biasing cells doesn't make a difference in the results. But not to loose the integrity in the design, all the MOS transistor's GEO parameter has been changed to GEO=1.

For the simulations a trigger pulse is connected between the outputs of the first delay cell. All of the circuit schematics of the simulations are given in Appendix C.

### 5.2.3.1 Typical results

Two different design environments are used which are Made and HP-ADS. Transient simulations and Steady State (SST) analyses are done with eldorf. The characterization simulations and Monte Carlo simulations are done with eldorf also. Phase noise simulation is done with HP-ADS.

In Table 5.17, some stimuli values of the circuit are given for typical conditions.

**Table 5.17** Typical stimuli value for ring oscillator

|                     | Typical Values |
|---------------------|----------------|
| Temperature         | 27 deg.        |
| Analog Tune (Vtune) | 900mV          |
| Supply Voltage      | 3.3V           |
| Device Models       | Typical        |

With given typical conditions transient simulation is realized. In Figure 5.27 the transient response of the outputs is shown.

The oscillator achieves quadrature outputs. We can see this result ones more from the SST analysis as shown in Figure 5.28. At oscillation frequency, 6GHz, there is 90 degrees difference between two ouputs. This proves the quadrature outputs.

The amplitude difference between two quadrature outputs are shown in Figure 5.29. the difference at 6GHz is negligble enough which is 0.0583dB.

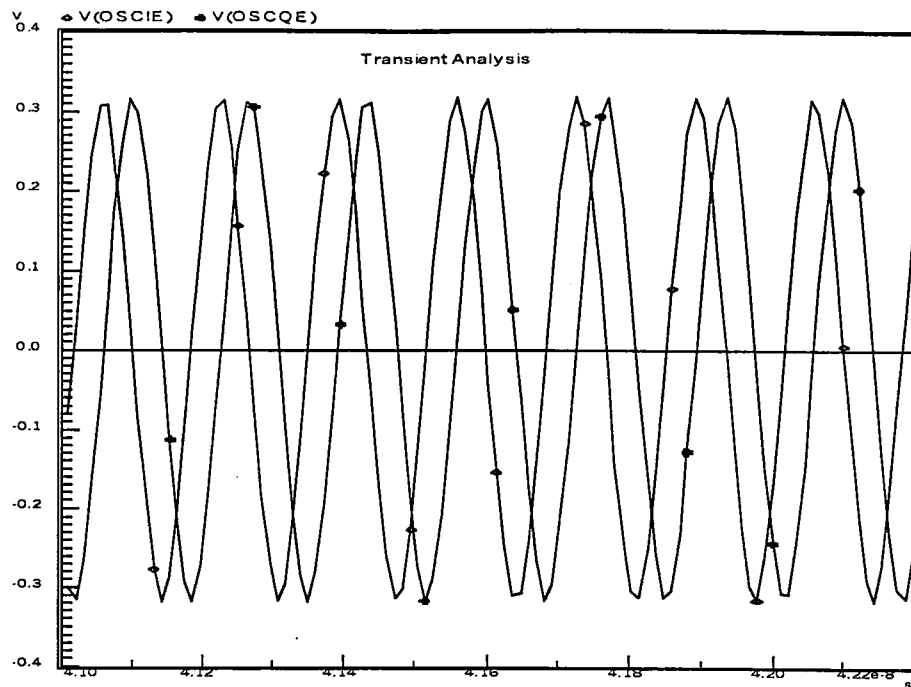


Figure 5.27 Transient response of the ring oscillator

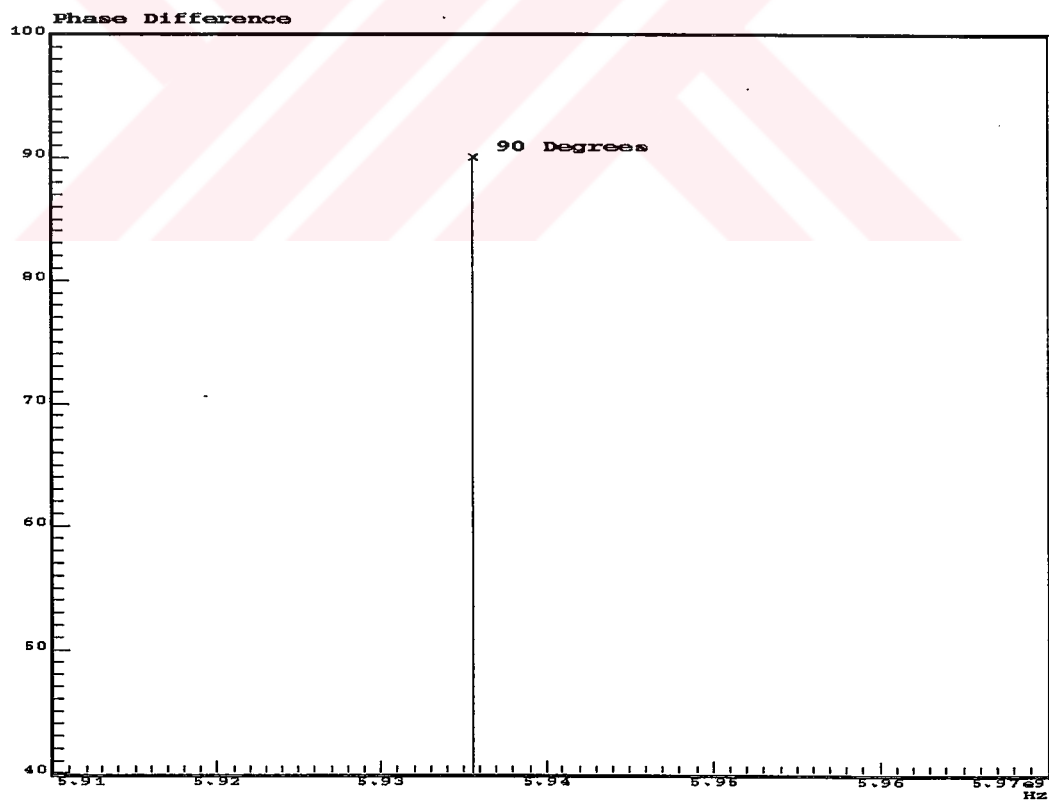


Figure 5.28 SST Results of ring oscillator

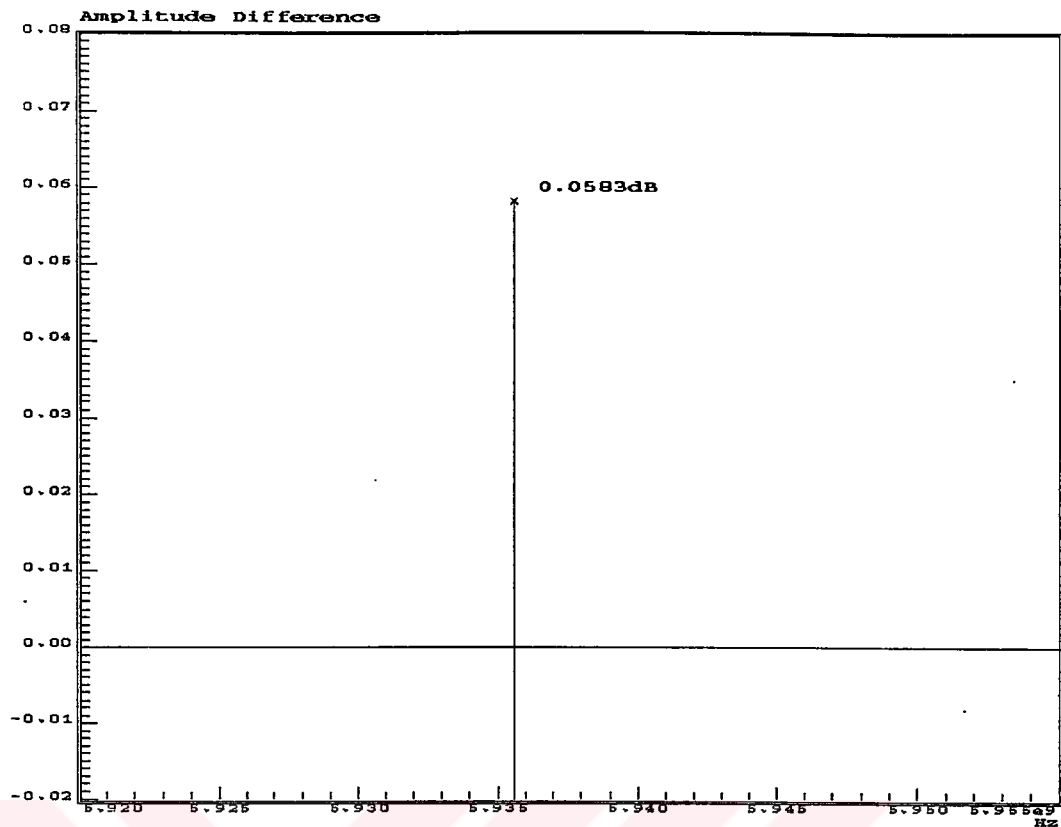


**Figure 5.29** Amplitude difference of the outputs

The tuning range of the oscillator is shown in Figure 5.30. The tuning voltage is changed between 0.4V and 1.6V. Within this range the oscillation frequency changes from 2.81GHz to 7.55GHz.

### TUNING RANGE

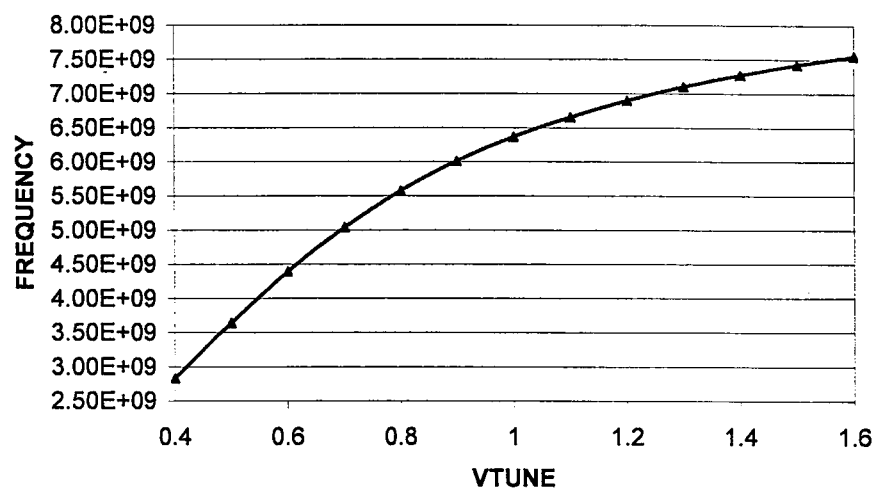


**Figure 5.30** Tuning Range of ring oscillator

The tuning range of the oscillator is 4.74GHz. The peak to peak differential voltage value of the outputs is between 0.670V and 0.799V. The maximum amplitude difference between two quadrature outputs is 30mV.

The typical results of the circuit are summarized in Table 5.18.

**Table 5.18** Ring Oscillator Typical condition results

|                                 | TUNING  |       |
|---------------------------------|---------|-------|
|                                 | 0.4V    | 1.6V  |
| FREQUENCY(GHz)                  | 2.81    | 7.55  |
| AMPLITUDE(V <sub>pp</sub> diff) | 0,670   | 0,799 |
| PHASE DIFF.(degrees)            | 90      | 90    |
| AMP. DIFF.(mV)                  | 1       | 30    |
| TUNING RANGE                    | 4.74GHz |       |

#### 5.2.3.2 Characterization simulations of the quadrature ring VCO

The characterization simulation for quadrature ring oscillator is also very important as it gives the performance results of the circuit. The general characterization conditions for our design are already explained in section 5.1.3.2. In addition to these, this time we have BJT transistors with its fast and slow models. This increases the number of simulations, which makes 256 simulations totally. The results of the simulations are given below in Table 5.19.

**Table 5.19** Characterization results of ring oscillator

|                                  | MIN      | MAX   |
|----------------------------------|----------|-------|
| FREQUENCY(GHz)                   | 4.83     | 6.0   |
| AMPLITUDE (V <sub>pp</sub> diff) | 526mV    | 1.15V |
| PHASE DIFF.(degrees)             | 90.004   | 90.13 |
| AMP. DIFF.                       | 4mV(max) |       |
| TUNING RANGE                     | 1120MHz  |       |

These are the worst results of the characterization simulations, which gives the real performance of the circuit. The tuning range of the oscillator is decreased, when compared with the typical results, which is 1120MHz. The amplitude of the outputs changes with different conditions of the circuit. The amplitude difference value is checked within the tuning range area, which is between 4.83GHz and 6GHz and found as 4mV. The phase difference of the outputs is maximum 90.13 degrees, which is very normal.

### 5.2.3.3 Monte Carlo Simulations

In the quadrature ring VCO, Monte Carlo simulations are only done in order to see the phase difference of the oscillator. We know that the devices in the delay cell are most effective ones for the phase mismatch of the circuit. This time we have also BJT transistors. For MOS transistors the same method is used to calculate the deviations as explained in Equation (5.1). The mismatch of NPN BJT transistors will be calculated with the  $I_S$  and  $\beta$  parameter deviation.  $I_S$  is for collector current matching,  $\beta$  is for current gain matching. Both of the deviations can be calculated from the given equation.

$$\sigma = \frac{A}{\sqrt{B}} \quad (5.2)$$

In the equation, A is the parameter given from the technology depending on the type of the NPN transistor. The unit of this parameter is [% $\mu\text{m}$ ]. The parameter B is the effective emitter area of the BJT. This area also changes with the type of the BJT.

The NPN transistors in the delay cell are all same type, which is called NH8 in our technology. The deviation is calculated with the formula in equation 5.2. The deviations of the NPN transistor are shown in Table 5.20.

**Table 5.20** Deviation of NPN transistors in the delay cell.

|                | Deviation            |                    |
|----------------|----------------------|--------------------|
| Device Name    | $\beta$ Deviation(%) | $I_S$ Deviation(%) |
| Q1, Q2, Q3, Q4 | 0.65                 | 5.25               |

The PMOS transistors M1 and M2 in the delay cell and the PMOS transistor M1 in the PMOS biasing cell are very effective on the mismatch. For NMOS transistors, current source transistor M5 in the delay cell is an effective one. The current sources of the buffers in the delay cell M3 and M7 are also included to the Monte Carlo simulations.

The deviations calculated for the MOS transistors are given in Table 5.21. We know that the deviations are inversely proportional to the area of the transistor. The results given in table are obtained after many optimization simulations. The optimum dimensions are already given in the circuit description section.

**Table 5.21** Deviation of MOS transistors

| Device Name              | Deviation            |                     |
|--------------------------|----------------------|---------------------|
|                          | $\beta$ Deviation(%) | $V_T$ Deviation(mV) |
| PMOS M1(PMOS bias cell)  | 0.7                  | 2.3                 |
| PMOS M1,M2 (delay cell)  | 0.54                 | 1.63                |
| NMOS M3, M4 (delay cell) | 0.27                 | 0.88                |
| NMOS M5 (delay cell)     | 0.22                 | 0.44                |

On the list given above, for the mismatch of  $V_T$ ,  $V_{TH0}$  parameter and for the mismatch of  $\beta$ ,  $WMLT$  parameter is used for MOS transistors.

As mentioned in the results of Monte Carlo simulations in LC oscillator, all other parameters of the circuit are in typical conditions. The results of the simulations are given below in Table 5.22.

**Table 5.22** Monte Carlo simulation phase mismatch results

| Mismatch Types     | Standard Phase Deviation |
|--------------------|--------------------------|
| Only PMOS mismatch | 0,14 degrees             |
| Only NMOS mismatch | 0,06 degrees             |
| Only NPN mismatch  | 0,05 degrees             |
| Total mismatch     | 0,15 degrees             |

The simulations are done separately for each type of device to see which one is causing the most mismatches. PMOS transistors are the ones causing phase mismatch, but these results are the last values after the optimization. The total phase mismatch is 0.15 degrees.

#### 5.2.3.4 Phase Noise Simulations

The phase noise simulations are realized with HP-ADS and eldorf. The phase noise simulations is done only for typical conditions. The result of HP-ADS [104] is given in Figure 5.31. At 10MHz offset frequency, the phase noise is -97dBc/Hz at 10MHz.

In eldorf results of phase noise is shown in Figure 5.32 and is found -105dBc/HZ at 10MHz offset frequency. The difference in the results is because of the device model differences between two simulators. The phase noise of the ring oscillator is an expected one as it suffers from the Q. We know that we can't achieve better phase noise results as in LC oscillators.

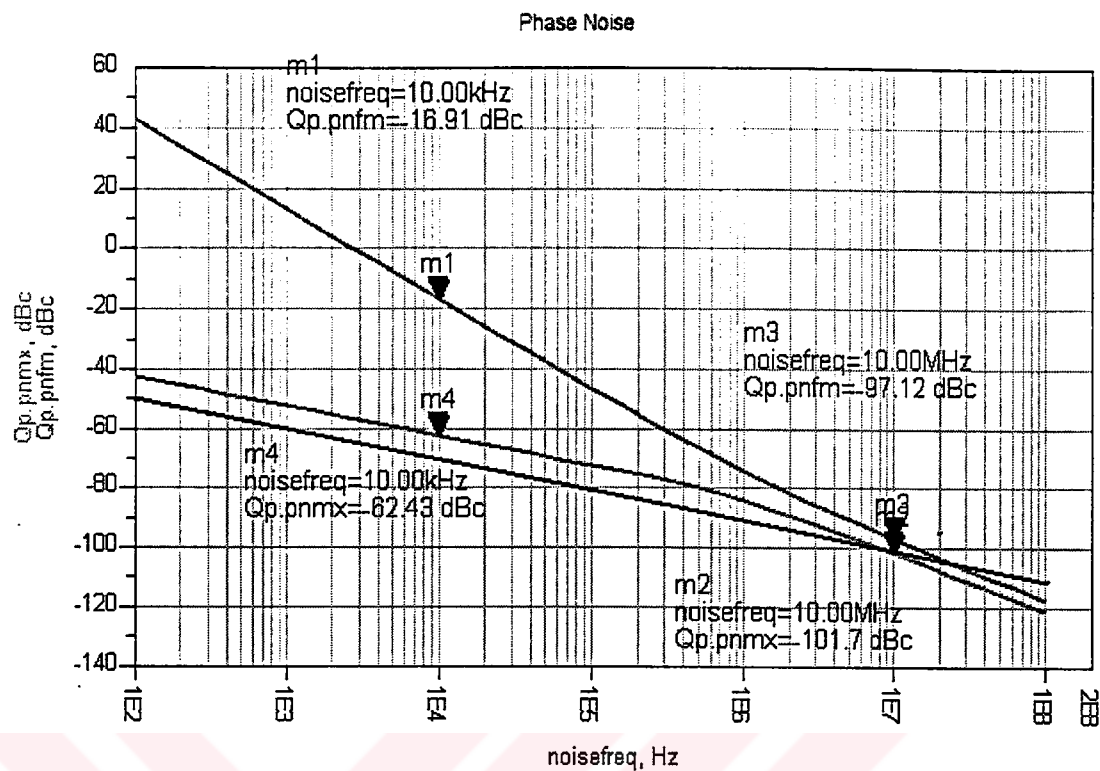


Figure 5.31 Phase noise of Ring Oscillator with HP-ADS

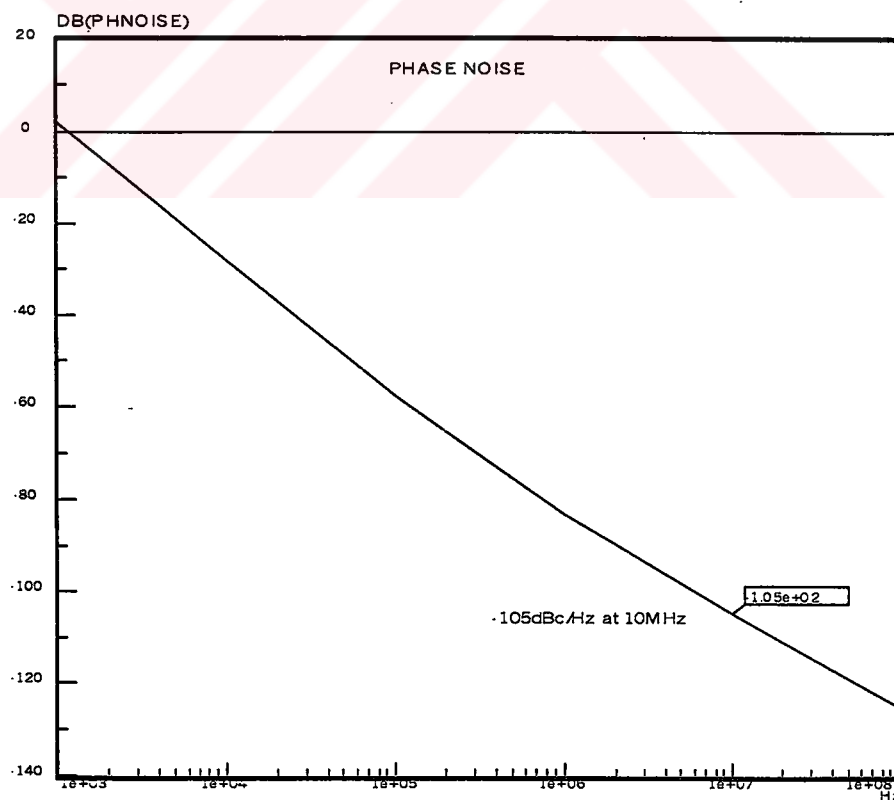


Figure 5.32 Phase Noise results of eldorf

### 5.3 Comparison of the LC and ring VCOs

In the sections above we have discussed about the quadrature LC and Ring oscillators. The performance of both of the circuits is summarized in Table 5.23. As mentioned before the performance of the circuit is obtained by the characterization simulation results of the circuit. Hence the results in Table 5.23 are comparable characterization results for both of the oscillators. In the comparison of the circuits, we should consider the performance of the produced chip with layout effects.

The tuning range is one of the important design spec for a VCO. The tuning range of the ring oscillator is 159MHz wider than the LC oscillator. There is not too much difference but the method of gaining this range is also important. Only an analog voltage tunes the ring oscillator, but for the LC oscillator we use a digital tuning and an analog tuning circuit together. In Monte Carlo analysis, it is seen that the mismatch of the devices doesn't effect the performance too much for both of the oscillators. But for the LC oscillator the effects of the inductors should be considered. There would be a mismatch between the inductors, so the tuning range value for the LC oscillator can change. The mismatch of the inductors is drawback of the LC oscillator. But both of the oscillators satisfy the 5-6GHz-frequency range of HIPERLAN.

The phase difference results are very satisfying for both of the circuits. In Table 5.24 the Monte Carlo results are given for phase difference, here the ring oscillator has more mismatches than the LC oscillator. But we have to remember that the mismatch of the inductors is not simulated. We know from some the measured chips that [28], the mismatch of the LC oscillator cause up to 5 degrees of mismatch between the quadrature outputs. For the oscillation amplitudes, the difference between the maximum and the minimum value of the ring oscillator is bigger than that of the LC oscillator. That means the oscillation amplitude of the ring oscillator changes more with the mismatch. And the results are differential and peak to peak amplitude values. For example the minimum amplitude value for the ring oscillator is 0.526V. The peak value of one the output of the oscillator makes 131.5mV. This low value makes the design of the mixer more difficult. But the LC oscillator can achieve bigger oscillation amplitudes.

The phase noise performances of the oscillators are incredibly comparable. This difference is already explained in Chapter 3 that the LC oscillators always have better phase noise. The LC oscillator achieves  $-123\text{dBc/Hz}$  while the ring oscillator achieves only  $-97\text{dBc/Hz}$  at  $10\text{MHz}$  offset frequency. Again the phase noise result of the LC oscillator will be depended on the production of the inductors, which is effective on the value of the  $Q$  of the inductor.

**Table 5.23** Characterization results of the oscillators

|                             | LC oscillator | Ring oscillator |
|-----------------------------|---------------|-----------------|
| Tuning Range                | 961MHz        | 1120MHz         |
| Phase Difference (Degrees)  | 90.125        | 90.13           |
| Amplitude(max V)            | 0.72          | 1.15            |
| Amplitude(min V)            | 0.2           | 0.526           |
| Amplitude Difference(max V) | 0.0673        | 0.004           |
| Phase Noise(10MHz offset)   | -123dBc/Hz    | -97dBc/Hz       |

**Table 5.24** Phase Difference Error with Monte Carlo simulations

|                                                       | LC oscillator | Ring oscillator |
|-------------------------------------------------------|---------------|-----------------|
| Phase Difference Error<br>Standard deviation(Degrees) | 0.07          | 0,15            |

The phase noise of the ring oscillator satisfies the spec of the system but the value will make the design of the PLL more difficult, which has to improve the value of the phase noise.

When the chip area of the circuits are compared, the LC oscillator consumes more chip area than the ring oscillator. For all the performance results of the LC oscillator, the mismatch of the inductor is very effective. To achieve the exact oscillation frequency band of the system, the LC oscillator needs much iteration. We have this experience from the  $3.5\text{GHz}$  LC oscillator design for the DECT project [105].

## 6. CONCLUSION

The last decade of this century has seen an explosive growth in the communications industry. People want to be connected all the time using wireless communication devices. In addition, the demand for high bandwidth communication channels has exploded with the advent of the Internet. Thanks to the high density available on integrated circuits, sophisticated digital modulation schemes can be employed to maximize the capacity of these channels. This has changed the design of wireless and wireline transceivers.

The advances in the technology are also a determining factor in this evolution. The RF design is shifted from discrete design to IC solutions. With performance the cost of the chip is also very important. GaAs has a very good frequency performance but it is expensive. BiCMOS give the best results when bipolar transistors are used for high frequency blocks and MOS transistor for digital blocks. But the standard CMOS process is cheaper than the BiCMOS process. Besides SiGe BiCMOS process achieves bipolar transistors with high  $f_T$  values. Today a lot of research is done on the single chip CMOS or BiCMOS RF.

A communications transceiver consists of different blocks, but the VCO is a critical sub-block of the transceiver. This thesis covers the design of RF VCOs. Before going deeply with the design tips of the VCOs, the general theory of oscillation and different type of basic RF oscillators have been presented in Chapter 2. Crystal oscillators, basic LC oscillators, Wien-Bridge oscillator, Colpitts oscillator, Hartley oscillator, relaxation oscillators and ring oscillators have been a subject of this chapter as they are the basics of the RF oscillators.

Chapter 3 has presented the basics of VCO beginning with the definition of a VCO. Main requirements for the VCO are low phase noise, wide tuning range and low power consumption. Due to very small communication channel spacing, the output signal of the frequency synthesizer must be a very pure sinusoid. At frequency offsets larger than the loop bandwidth, the phase noise is mainly determined by the

VCO. The general theory of phase noise in oscillators has also been presented in Chapter 3. Calculation of phase noise LC and ring oscillators are given with different models and formulas. We can conclude that LC oscillators have a better phase noise performance than ring oscillators. For a single-ended CMOS ring oscillator, phase noise is not dependent on the number of the stages. A differential ring oscillator does exhibit a phase noise dependency on the number of the stages, with the phase noise degrading as the number of the stages increases for a given frequency and power dissipation. The phase noise performance of an LC oscillator is mostly determined by the quality factor of the inductor. Higher Q valued inductors bring a better phase noise performance to the VCO. Of course it is not possible to go beyond a certain phase noise level due to the limitations of the technology.

Varactors and inductors are also a subject of Chapter 3. Varactors are key element in the design of LC VCOs for overall performance. We know that LC oscillators do not have a wide tuning range like ring oscillators. Therefore to increase the tuning range of the LC VCOs, different types of varactors are studied. Gated MOS varactors give the best performance of tuning range over all other varactor types. But this is a very new type varactor so it is still under research and there are not so many designs with this type of varactor. If you look at the LC VCO designs in last three years, it is seen that accumulation MOS varactor is taking the place of diode varactor. The LC VCO designed with accumulation MOS varactor consumes less power, has a larger tuning range and a better phase noise performance than the ones designed with diode varactors. Inductors have been presented in three categories; active inductors, bondwire inductors and spiral inductor. Inductors are very effective on the phase noise performance of the VCO. Active inductors are not preferred because they are noisy. More research is on bondwire and spiral inductors. High quality inductors are not readily available in a standard silicon process. Both bondwire inductors and spiral inductors have advantages and disadvantages. Bondwire inductors has a low series resistor so that high quality factors can be achieved, but on the other hand, they have a spread of ( $\pm 20\%$ ), which makes the tuning of the tank limited. Spiral inductors suffer from the high Q values because of the standard CMOS process, but better tuning is feasible with a spread of ( $\pm 5\%$ ). Die to die bonding is not accepted yet in a production environment, therefore die to frame lead bonding can be used with a series combination with a spiral inductor which collects the advantages of

both bondwire and spiral inductor. Spiral inductors are used with different shapes like octagonal, polygon or symmetrical. Octagonal spiral inductor is the one mostly used but the performance of the symmetrical one seems better. The symmetrical inductor is one differential coil. The use of one differential coil instead of two single coils exploits the coupling factor to increase the inductance, leading to a higher L C ratio. Using one coil costs less chip area. But the research on the symmetrical inductors still goes on, especially for their lumped element modelling for the simulations.

Different type of VCOs, designed from 90s until today has been presented in Chapter 4. The work covers a research on LC and ring VCOs. The LC VCOs are especially chosen for their different usage of varactor and inductors and amplifier circuits, so that the reader can compare them. The work is mostly on negative- $G_m$  oscillators, which are more preferred. The LC VCO using a series combination of bondwire inductor and spiral inductor, and an accumulation MOS varactor has the best performance of tuning range and phase noise when compared with the VCOs with same type amplifier circuit. Of course the circuits which are designed with cross-coupled PMOS transistors have better phase noise performance. The tuning range performance of the gated MOS varactor VCOs are challenging. Different types of delay cells and tuning methods have been presented for ring VCOs. The ring VCO having a fully switching of the differential delay cell and dual-delay path technique achieves better tuning range and phase noise performance than the ones that are studied in our work.

Quadrature signal generation is a critic point of the systems, which use digital modulations such as QPSK, GMSK, OFDM etc. Different methods to generate quadrature LO signals have been presented in Chapter 4. Four different methods are discussed and compared with each other. Using RC-CR network or polyphase filter after the VCO, following with buffers or limiters consume too much power, costs big chip area and quadrature signal performance is very dependent to the mismatch in the layout. Therefore this method is not preferred. Frequency division method, costs smaller area than the RC-RC network and cross-coupled VCO method. But the master-slave flipflops, which have to be designed in double frequency, too much power in currently used CMOS technology. As the technology scales down, this

could change very rapidly. If the primary design concern is low cost and or small area, then this solution clearly must be preferred, as the VCO designed at double frequency features a smaller coil however, in applications of high frequency like HIPERLAN2 it is not possible to design a double frequency VCO. Third method is two cross-coupled VCO. This costs double VCO area but consumes less power than the first and second method. One of the advantages of this method is that it provides high voltage swing, which eases the design of prescaler and mixers. The quadrature mismatch is mostly less than 5 degrees in the previous designs. Fourth method is the quadrature ring oscillators designed with even number of delay cells. This method costs less chip area than the cross-coupled VCO method but as it is a ring oscillator, the phase noise performance of the VCO will be worse than the cross-coupled LC VCO method. The third and the fourth method can be chosen according to the design specs of the VCO. If there is no need for a good phase noise performance, the quadrature ring oscillator is a good choice as it also performs high tuning range. And if the system requires low phase noise, the cross-coupled LC VCO should be chosen.

The demand for wireless local area network (WLAN) systems, which can support data rates in excess of 20Mb/s with very low cost and low power consumption, is rapidly increasing. Most of these systems use the 2.4GHz ISM band, but there is worldwide interest in increasing data transmission rates by using the 5GHZ ISM band like the European high-performance radio LAN (HIPERLAN) system. HIPERLAN2 has a very high transmission rate up to 54 Mb/s. This is achieved by making use of a modularization method called Orthogonal Frequency Digital Multiplexing (OFDM). The HIPERLAN2 has been specifically developed to mainly have a wired infrastructure providing a short range wireless access to IP, ATM and UMTS networks. In Chapter 5, two different types of VCO have been presented, designed for in HIPERLAN2 system. Both of the VCOs generate quadrature signals, as OFDM modulation is used in this system. Both of the VCOs are designed with 0.35 $\mu$ m SiGe BiCMOS process.

First design consists of two identical cross-coupled LC VCOs. Each VCO is realized with coupled PMOS and NMOS transistors with a symmetrical coil. For a better tuning range MOS varactors are preferred instead of diode varactors, for both analog and digital tuning. Accumulation varactors could not have been used because this

type of varactor has not been modelled or tested by this technology. The VCO operates between 5.008 and 5.969GHz having a tuning range of 961MHz. The VCO achieves  $-125\text{dBc/Hz}$  of phase noise at 10MHz offset frequency. The quadrature phase mismatch is less than 0.125 degrees. The second design is the quadrature ring oscillator with two delay cells. The delay cells are designed with a differential BiCMOS pair. Both the tail current and the gate voltage of the PMOS transistors of the delay cell are controlled with one tuning voltage. The ring VCO operates between 4.83 and 6GHz, having a tuning range of 1120MHz. The phase noise of the ring VCO is  $-97\text{dBc/Hz}$  at 10MHz offset frequency. The quadrature mismatch is less than 0.13 degrees. The simulation results of LC and ring oscillator are comparable with each other. The phase noise performance of the LC VCO is better than the ring VCO. The ring VCO has a better tuning range than LC VCO. The quadrature phase mismatch results are exactly the same. Although we have done the Monte Carlo and all characterization simulations, the performance of the VCOs will be slightly different when they are really measured. There will be some mismatches due to the process variations and the results will not be the same with simulation results. We had studied that the quadrature LC VCOs have quadrature mismatch values up to 5 degrees. Therefore in reality the phase mismatch will be much greater than it is simulated, however with a very careful design, mismatch values up to 1 degrees can be achieved. The operation frequency can change because of the integration of the inductors. The operation frequency band can change because of the difficulties to integrate the inductor. It is possible that finding the correct frequency band can need some iteration. For the quadrature ring VCO, in the simulations it was seen that the oscillation frequency is very sensitive to the PMOS transistors in the delay cell. The operation frequency band can also change for this VCO in the measurement results. The LC VCO will cost more chip area than the ring VCO. The phase noise spec of the VCO in the HIPERLAN2 system is the  $-99\text{dBc/Hz}$  at 10MHz. The LC VCO achieves very well this spec, but the ring VCO achieves lower than the spec. We know that the PLL improve the phase noise, so the ring VCO can still be used in the system but the design of the PLL will be difficult than the design of the PLL of the LC VCO. Both of the VCOs seem feasible for HIPERLAN2 system but one should know that ring VCO has a higher phase noise but easy to implement and cost less chip area whereas the LC VCO has a lower phase noise, cost more chip area and not so easy to implement because of the inductors.

With the simulations results we have shown that quadrature LC VCO and quadrature ring VCO are feasible for HIPERLAN2 system. For other systems where the 5-6GHz range is used, if the phase noise performance is important and strict, the LC VCO should be preferred with high cost. And if chip area cost is important ring VCO should be preferred suffering from phase noise. The remaining challenge is to test both of the VCOs and see which one better and how the VCOs can be improved. It will be interesting to design the LC VCO tank with an accumulation MOS varactor to increase the tuning range of the LC VCO. For the ring VCO another feasibility can be done to improve the phase noise performance.



## REFERENCES

- [1] **Terman, F.**, 1955. Electronic and radio engineering, fourth edition, McGraw Hill Book Co., NY.
- [2] **The ARRL writers**, 1982. The ARRL handbook for radio amateur, American radio relay league Inc.
- [3] **Hayward, W.**, 1977. Solid state design for the radio amateur, American radio relay league Inc.
- [4] **Drentea, C.**, 1982. Radio communication receiver, Tab books Inc. Blue Ridge Summit, PA. USA.
- [5] **Clark, K.K and Hess, D.T**, 1971. Communication Circuits: Analysis and Design, Addison Wesley Reading, Mass.
- [6] **Razavi, B.**, March 1996. A study of phase noise in CMOS oscillators, *IEEE Journal of solid-state circuits*, **31**, 331-343.
- [7] **Wu, J.T.**, February 1990. A bipolar 1-GHz multi-decade monolithic variable-frequency oscillator, in *ISSCC Dig. Tech. Papers*, 106-107
- [8] **Thamsirainunt, M. and Kwasniewski, T. A.**, October 1997. CMOS VCOs for PLL frequency synthesis in GHz digital Mobile communications, *IEEE Journal of solid-state circuits*, **32**, 1511-1524
- [9] **Ware, K.M., Lee H.S. and Sodini, C.G.**, December 1989. A 200MHz CMOS phase-locked loop with dual phase detectors, *IEEE Journal of Solid-State Circuits*, **24**, 1560- 1568.
- [10] **Enam, S.K and Abidi, A.A.**, February 1990. A 300-MHz CMOS voltage-controlled ring oscillator, *IEEE Journal of solid-state circuits*, **25**, 321-315
- [11] **Craninckx, J. and Steyaert, M .S. J.**, December 1995. A 1.8GHz CMOS low-phase noise voltage-controlled oscillator with prescaler, *IEEE Journal of solid-state circuits*, **30**, 1474-1482.

- [12] **Craninckx, J. and Steyaert, M. S. J.**, May 1997. A 1.8GHz low-phase noise CMOS VCO using optimized hallow spiral inductors, *IEEE Journal of solid-state circuits*, **32**, 736-744.
- [13] **Craninckx, J. and Steyaert, M. S. J.**, December 1998. A fully integrated CMOS DCS-1800 frequency syntesizer, *IEEE Journal of solid-state circuits*, **33**, 2054-2065.
- [14] **Chen, W. and Wu, J.**, June 1999. A 2-V 1.8-GHz BJT phase-locked loop, *IEEE Journal of solid-state circuits*, **34**, 784-789
- [15] **Tham, J.L., Margarit, M.A., and Pregardier ,B.**, Hull C.D. and Carr F., March 1999. A 2.7-V 900-MHz/1.9-GHz dual-band transceiver IC for digital wireless communication, *IEEE Journal of solid-state circuits*, **34**, 286-291.
- [16] **Craninckx, J. Steyaert, M. and Miyakawa, H.**, 1997. A fully integrated spiral-LC CMOS VCO set with prescaler for GSM andDCS-1800 systems, in *Proc. Custom Integrated Circuits Conf.*, 1997, 403-393.
- [17] **Lam ,C. and Razavi, B.**, 1999. A 2.6-GHz/5.2-GHz CMOS Voltage-Controlled Oscillator," *Dig. International solid-state Circuits Conference, San Francisco*, February 15-17. 402-403.
- [18] **Rategh, H.R, Samavati, H. and Lee, T.H.**, May 2000. A CMOS frequency synthesizer with an injection-locked frequency divider for a 5-GHz wireless LAN receiver, *IEEE Journal of solid-state circuits*, **35**, 780-787.
- [19] **Meyer, R.G., Mack, W.D. and Hegaraats, J.J.E.**, December 1997. A 2.5-GHz BiCMOS transceiver for wireless LAN's, *IEEE Journal of solid-state circuits*, **32**, 2097-2104.
- [20] **Grau, G., Langmann U., Winkler, W., Winkler, W., Knoll D., Osten, J. and Pressel, K.**, September 2000. A current-folded up-conversion mixer and VCO with center-tapped inductor in a SiGe-HBT technology for 5-GHz wireless LAN applications, *IEEE Journal of solid-state circuits*, **35**, 1345-1352.
- [21] **Razavi, B.**, 1997. RF Microelectronics, Printice Hal PTR
- [22] **Sevenhans, J., Haspeslagh, D., Delarbre, A., Kiss, L., Chang, Z. and Kukielka ,J.F.** 1994. An analog radio front-end chip set for a 1.9GHz

mobile radio telephone application, *IEEE Journal of Solid-State Conf.* February 1997, 44- 45.

- [23] Hull ,C.D., Tham, J.L and Chu R.R., December 1996. A direct conversion receiver for 900MHz (ISM band) spread-spectrum digital cordless telephone, *IEEE Journal of Solid-State*, **31**, 1955-1963.
- [24] Crols, J. and Steyaert, M., 1995. A fully integrated 900MHz CMOS double quadrature downconverter, , *IEEE Journal of Solid-State Conf.*, February 1995, 136-137.
- [25] Behbahani, F., Kishigami, Y., Leete, J. and Abidi, A., June 2001. CMOS mixers and polyphase filters for large image rejection, , *IEEE Journal of Solid-State*, **36**, 873-887.
- [26] Razavi, B. and Anand, B.A., March 2001. A CMOS clock recovery circuit for 2.5-Gb/s NRZ Data, *IEEE Journal of Solid-State circuits*, **36**, 432-439.
- [27] Rafougaran, A., Rafougaran, M., Rael, J. and Abidi, A., 1996. A 900MHz CMOS LC-Oscillator with quadrature outputs, *Proc.IEEE Int. Solid-State Circuits Conf.*, Newyork,NY, p. 332.
- [28] Tiebout, M. July 2001. Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS, *IEEE Journal of solid-state circuits*, **36**, 1018-1024.
- [29] Harame, D.L., Gilbert, M., Malinowski, J. and Kebeb, T., 1994. A 200mm SiGe-HBT technology for wireless and mixed signal applications, in *tech.Dig. Int, Electron Devices Meeting*, 437-440
- [30] Schüppen, A., Dietrich, H.i Gerlach ,S., Hohnemann, H. andSchumacher, H., 1996. SiGe technology and components for mobile communication systems, in *Proc. Bipolar Circuitss and Technology Meeting*, 1996, 130-133.
- [31] Burghartz, J.N. Soyuer, M., Jenkins, K.A and Kies, M., September 1997. Integrated RF components in a SiGe bipolar technology, *IEEE Journal of solid-state circuits*, **32**, 1440-1445.
- [32] Chevalier, P., De Pestel, F., Ziad, H., fathoutdinov ,M., Ackaert, J., Coppens, P., Craninckx, J., Günçer, S., Ponitoglu, A., Taşci, P., Yayil, F., Ergun, B.S., Kurhan, I. And Gillon, R., 2001. BC035G: An industrial 0.35 $\mu$ m SiGe BiCMOS technology for 5GHz home

digital networks, 9th IEEE International Symposium on Electron Devices for Microwave and Optoelectronic Applications(EDMO), 15-16 November 2001, Vienna, Austria.

- [33] **DTS/BRAN-0023003**, 1999. Broadband radio access networks (BRAN) HIPRLAN type 2 technical specification, ETSI.
- [34] **Sedra, A.S and Smith, K.C.**,1991. Microelectronic circuits, Oxford University press, NewYork.
- [35] **Razavi, B.**,2001, design of analog CMOS integrated circuits, McGraw-Hill companies Inc. New York.
- [36] **Craninckx, J.**, 1997. Low-phase-noise fully integrated CMOS frequency synthesizers, Phd Thesis, Catholic University of Leuven, Belgium.
- [37] **Rohde, U.**, 1997. Microwave wireless synthesizers, John Wiley and Sons Inc.
- [38] **Huang, Q. and Basedau, P.**, December 1997. Design considerations for high frequency crystal oscillators digitally trimmable to sub-ppm accuracy, *IEEE transactions on very scale integration (VLSI) systems*, **5**, 408-416.
- [39] **Homberg, J.**, July 1999. A universal 0.03-mm<sup>2</sup> one-pin crystal oscillator in CMOS, *IEEE Journal of solid-state circuits*, **34**, 956-961.
- [40] **Achenbach, R., Raible, M., Hiller, F., Keller, M., Meier, K., Rudolph, H. and Sur-Brosch, R.**, October 2000. A digitally temperature-compensated crystal oscillator, *IEEE Journal of solid-state circuits*, **35**, 1502-1506.
- [41] **Bianchi, R.A., Karam, J.M. and Courtois, B.**, January 2000. Analog ALC crystal oscillators for high-temperature applications, *IEEE Journal of solid-state circuits*, **35**, 2-14.
- [42] **Johns, D. and Martin, K.**, 1997. Analog integrated circuit design, John Wiley and sons Inc. New York
- [43] **Abidi, A.A and Meyer, R.G.**, December 83. Noise in relaxation oscillators, *IEEE Journal of solid-state circuits*, **18**, 794-802
- [44] **Weigandt, T.C.**, 1998. Low-Phase-Noise, Low-Timing-Jitter Design Techniques for Delay Cell Based VCOs and Frequency Synthesizers, Doctor of Philosophy in Engineering-Electrical Engineering and Computer Sciences, University Of California, Berkeley.

- [45] **Robins, W. P.**, Phase noise in signal sources: (theory and applications), Peregrinuson behalf of the IEE, 1982.
- [46] **Underhill, M.J.**, August 1992. Fundamentals of Oscillator Performance, *Electronics & Communication Engineering Journal*, **4**, 175-183.
- [47] **Leeson, D.B.**, 1996. A Simple Model of Feedback Oscillator Noise Spectrum, *Proc. Of the IEEE*, **54**, 329-330
- [48] **Underhill, M.J.**, August 1992. Fundamentals of Oscillator Performance, *Electronics & Communication Engineering Journal*, **4**, 195-183
- [49] **Everhard, J.K.**, August 1986. Low-Noise Power-Efficient Oscillators: Theory and Design, *IEE Proceedings*, **133**, No. 4, 172-180.
- [50] **Lee, T. and Hajimiri, A.**, March 2000. Oscillator phase noise: A tutorial, *IEEE Journal of solid-state circuits*, **35**, 326-336.
- [51] **Craninckx, J. and Steyaert, M. S. J.**, December 1995. Low-noise voltage controlled oscillators using enhanced LC-tanks, *IEEE Trans. Circuits Syst. II*, **42**, 794-804.
- [52] **Kouznetsov, K.A and Meyer, R.G.**, August 2000. Phase noise in LC oscillators, *IEEE Journal of solid-state circuits*, **35**, 1244-1248
- [53] **Samori, C. Lacaita A.L., Zanchi, A. Levantino, S., and Cali, G.**, January 2000. Phase noise degradation at high oscillation amplitudes in LC-tuned VCO's, *IEEE Journal of solid-state circuits*, **35**, 96-99.
- [54] **Muer, B.D, Borremans, M., Steyaert, and Li Puma, G.**, July 2000. A 2-GHz Low-phase-noise integrated LC-VCO set with Flicker-noise upconversion minimization, *IEEE Journal of solid-state circuits*, **35**, 1034-1038.
- [55] **Hajimiri, A., Limotyrakis, S. and Lee, T.H.**, June 1999. Jitter and phase noise in ring oscillators, *IEEE Journal of solid-state circuits*, **34**, 790-804.
- [56] **Hajimari, A. and Lee, T.**, February 1998. A general theory of phase noise in electrical oscillator, *IEEE Journal of solid-state circuits*, **33**, 179-194
- [57] **Gierkink, S.L.J., Klumperink, E.A.M. and Hoogzaad, G.**, July 1999. Intrinsic 1/f device noise reduction and its effect on phase noise in CMOS ring oscillators, *IEEE Journal of solid-state circuits*, **34**, 1022-1025.

- [58] **Andreani, P.**, September 1998. A comparison between two 1.8GHz CMOS VCOs tuned by different varactors, in *Proc. ESSCIRC'98*, 380-383.
- [59] **Tang, J.D and Kasperkovitz, D.**, August 2000. A low-phase-noise reference oscillator with integrated pMOS varactor for digital satellite receivers, *IEEE Journal of solid-state circuits*, **35**, 1238-1243.
- [60] **Andreani, P. and Mattison, S.**, June 2000. On the use of MOS varactors in RF VCO's, *IEEE Journal of solid-state circuits*, **35**, 905-910.
- [61] **Andreani, P. and Mattisson, S.**, May/June 1999. A 2.4-GHz CMOS monolithic with an MOS varactor, in *Proc ISCAS'99*, vol.II, 557-560.
- [62] **Sorraphanth, T.**, 1998. Analysis and optimization of accumulation-mode varactor for RF ICs, in *Dig. Tech. Papers, Symp. VLSI circuits*, 1998, 32-33.
- [63] **Castello, R., Erratico, P., Manzini, P. and Svelto, F.**, June 1998. A  $\pm 30\%$  tuning range varactor compatible with future scaled technologies, in *Dig. Tech. Papers, symp. VLSI circuits*, 1998, 34-35
- [64] **Shen, K., Hui, F.P.S, Wong, W.M.Y and Chen, Z.**, February 2001. A three-terminal SOI gated varactor for RF applications, *IEEE transactions on electron devices*, **48**, 289-293.
- [65] **Wong, W., Hui, F., Chen, Z., Shen, K. and Lau, J.**, June 1999. Wide tuning range inversion-mode gated varactor and its application on a 2-GHz VCO, *Symp. VLSI Circuit Dig. Tech. Papers*, 53-54.
- [66] **Zhang, G.F. and Gautier, J.L.**, April 1993. Broad-band, lossless monolithic microwave active floating inductor, *IEEE Microwave and Guided Lett.*, **3**, 98-100.
- [67] **Greenhouse, H.M.**, June 1974. Design of planar rectangular microelectronic inductors, *IEEE Trans. Parts, Hybrids, Packag.*, PHP-10, 101-109.
- [68] **Nguyen, N.M. and Meyer, R.G.**, August 1990. Si IC-compatible inductors and LC passive filters, *IEEE Journal of solid-state circuits*, **25**, 1028-1031.
- [69] **Soyuer, M., Jenkins, K.A., Burghartz, J.N. and Hulvey, M.D.**, February 1996. A 3-V 4-GHz voltage-controlled oscillator with integrated resonator, in *ISSCC Dig. Tech. Papers*, San Fransisco, CA, 394-395.

- [70] **Chang, J.Y., Abidi, A.A. and Gaitan, M.**, May 1993. Large suspended inductors on silicon and their use in a  $2\mu\text{m}$  CMOS RF amplifier, *IEEE Electron Device letter*, **14**, 246-248.
- [71] **Lee ,T.H. and Wong, S.S.**, October 2000. CMOS RF integrated Circuits at 5GHz and beyond, *proceeding of the IEEE*, **88**, 1560-1571.
- [72] **Niknejad, A.M. and Meyer, R.G.**, October 1998. Analysis, design and optimization of spiral inductors and transformers for Si RF IC's, *IEEE Journal of solid-state circuits*, **33**, 1470-1481
- [73] **Soyuer, M., Burghartz, J.N., Ainspan, H.A., and Jenkins, K.A.**, September 1997. An 11-GHz 3-V SiGe Voltage-controlled oscillator with integrated resonator, controlled, *IEEE Journal of solid-state circuits*, **32**, 1451-1454.
- [74] **Kenneth, O.**, August 1998. Estimation methods for quality factors of inductors fabricated in silicon integrated circuit process technologies, *IEEE Journal of solid-state circuits*, **33**, 1249-1252
- [75] **Kinget, P.**, 1998. A 2.7V fully integrated  $0.35\mu\text{m}$  CMOS VCO for 5 GHz wireless applications, *Digest of the IEEE International Solid State Circuits Conference (ISSCC)*, San Fransisco, February 1998.
- [76] **Hung, C.M. and Kenneth, K.O.**, March 1999. A 1.24-Ghz monolithic CMOS VO with phase noise of  $-137\text{dBc/Hz}$  at a 3-MHz offset, *IEE microwave and guided wave letters*, **9**, 111-113.
- [77] **Hung, C.M and Kenneth, K.O.**, January 2000. A packaged 1.1GHz CMOS VCO with phase noise of  $-126\text{dBc/Hz}$  at a 600kHz offset, *IEEE Journal of solid-state circuits*, **35**, 100-103.
- [78] **Svelto, F., Deantoni, S. and Castello, R.**, March 2000. A 1.3GHz low-phase noise fully tunable CMOS LC VCO, *IEEE Journal of solid-state circuits*, **35**, 356-361.
- [79] **Andreani, P. and Mattison, S.**, May 2000. A 1.8GHz CMOS VCO tuned by an accumulation-mode MOS varactor, *in Proc ISCAS'00*, 315-318.
- [80] **Ainspan, H. and Plouchart, J.**, September 2000. A comparison of MOS varactors in fully-integrated CMOS LC VCO's at 5GHz and 7GHz, *in Proc. ESSCIRC'00*, 19-21 September.

- [81] **Plouchart, J.**, June 2000. A fully-monolithic SiGe differential voltage-controlled oscillator for 5GHz wireless applications, in *Proc. IEEE RFIC*.
- [82] **Wang, H.M.**, February 1999. A 9.8-GHz back-gate tuned VCO in 0.35 $\mu$ m CMOS, *IEEE ISSCC Dig. Tech. Papers*, 406-407.
- [83] **Nguyen, N.M and Meyer, R.G.**, March 1992. A 1.8-GHz monolithic LC voltage-controlled oscillator, *IEEE Journal of solid-state circuits*, **27**, 444-450.
- [84] **Kobayashi, K.W and Oki, A.K.**, July 1994. A novel heterojunction bipolar transistor VCO using an active tunable inductance, *IEEE microwave and guided wave letters*, **4**, 235-237.
- [85] **Baltus, P.G.M., Wegamens, A.G., Dekker, R., Hoogstraate, A. and Tombeur, A.**, December 1998. A 3.5-mW, 2.5-GHz diversity receiver and a 1.2-mW, 3.6-GHz VCO in silicon on Anything, *IEEE Journal of solid-state circuits*, **33**, 2074-2079.
- [86] **Chen, W. and Wu, J.**, September 1998. A 2-V 2-GHz BJT variable frequency oscillator, *IEEE Journal of solid-state circuits*, **33**, 1406-1410.
- [87] **Zannoth, M., Kolb, B., Fenk, J. and Weigel, R.**, December 1998. A fully integrated VCO at 2GHz, *IEEE Journal of solid-state circuits*, **33**, 1987-1991.
- [88] **Zannoth, M., Fenk, J., Springer, A. and Weigel, R.**, February 2000. A single-chip SI-Bipolar 1.6-GHz VCO with integrated-bias network, *IEEE transactions on microwave theory and techniques*, **48**, 203-205.
- [89] **Margarit, M.A., Tham, J.L., Meyer, R.G and Deen, M.J.**, June 1999. A low-noise, low-power VCO with automatic amplitude control for wireless applications, *IEEE Journal of solid-state circuits*, **34**, 761-771.
- [90] **Lee, S., Kim, B. and Lee, K.**, May 1997. A fully integrated low-noise 1-GHz frequency synthesizer design for mobile communication application, *IEEE Journal of solid-state circuits*, **32**, 760-765.
- [91] **Yan, S. and Luong, H.C.**, July 1998. A 3-V to 1.3-to-1.8GHz CMOS voltage controlled oscillator with 0.3-ps jitter, *IEEE transactions on circuits and systems-II: Analog and digital signal processing*, **45**, 876-880.
- [92] **Park, C. and Kim, B.**, May 1999. A low-noise, 900MHz VCO in 0.6 $\mu$ m CMOS, *IEEE Journal of solid-state circuits*, **34**, 586-590.

- [93] **Lee S.J, Kim B. and Lee K.**, February 1997. A novel high speed ring oscillator for multiphase clock generation using skewed delay scheme, *IEEE Journal of solid-state circuits*, **32**, 289-291.
- [94] **Yan, W.S. and Luong, H. C.**,2000. A 2-V 900-MHz monolithic CMOS dual-loop frequency synthesizer for GSM wireless receiver, in *Proc. ESSCIRC*, Sweden, 19-21 September 2000.
- [95] **Lo, C. and Luong, H.C.**, June 1999. 2-V 900MHz quadrature coupled LC oscillator with Improved amplitude and phase matchings, *IEEE International Symposium on circuits and systems*, Florida, USA, 589-592
- [96] **Razavi, B.**, February 1997. A 1.8GHz CMOS voltage controlled oscillator, *ISSCC Dig. Tech. Papers*, 388-389.
- [97] **Lam, C. and Razavi, B.**, May 2000. A 2.6-GHz/5.2-GHz frequency synthesizer in 0.4- $\mu$ m CMOS technology, *IEEE Journal of solid-state circuits*, **35**, 788-794
- [98] **Borremans, M., De Ranter, C. and Steyaert, M.**, 1999. A CMOS Dual Channel, 100MHz-1.1GHz Transmitter for Cable Applications, the extended version, *IEEE Journal of Solid-State Circuits Conference*, San Francisco February 15-17.
- [99] **ElSayed, A.M. and Elmasry, M.I.**, April 2001. Low-phase-noise LC quadrature VCO using coupled tank resonators in a ring structure, *IEEE Journal of solid-state circuits*, **36**, 701-705.
- [100] **Tang, J., Kasperkovitz, D. and Roermund, A.**, 2000. A 2.7 V, 8 GHz Monolithic I/Q RC Oscillator with Active Inductive Loads, in *Proc. ESSCIRC*, Sweden, 19-21 September 2000, pp. 304-307
- [101] **SPIRAL Users Reference Manual** (C) OEA INTERNATIONAL, Inc. 2000 Santa Clara.
- [102] **Hajimiri, A. and Lee T.**, May 1999. Design Issues in CMOS Differential LC oscillators, *IEEE Journal of solid-state circuits*, **34**, 717-724.
- [103] **Ham, D. and Hajimiri, A.**, June 2001. Concepts and methods in optimization of integrated LC VCOs, *IEEE Journal of solid-state circuits*, **36**, 896-909.
- [104] **HP-ADS**, 2000-2001. HP-ADS circuit simulation user manual, Agilent technologies 2000-2001

[105] **Craninckx J.** 2000. Personal talk.



## A APPENDIX A

In oscillator circuits, RC, LC and RLC circuits are frequently used. So it is useful to review, the properties of these circuits like the quality factor  $Q$ , and passive impedance transformation of RLC circuits.

### A.1 Quality factor $Q$

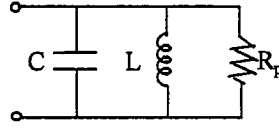


**Figure A.1** LC tank circuit.

The general definition of the quality factor is,

$$Q = 2\pi \frac{\text{Peak energy stored}}{\text{Energy loss per cycle}} \quad (\text{A.1})$$

This formula can be used for the well-known LC tank circuit with a parallel resistor as shown in Figure A.1. If a sinusoidal voltage  $V(t) = V_A \cdot \sin(\omega t)$  is applied to the circuit, at times  $t$  when the applied voltage reaches its maximum, voltage across  $C$  equals to  $V_0$  and the current through  $L$  equals zero. At that time the energy stored in the capacitor is at a maximum, and the energy in the inductor is zero. The peak energy stored is,

$$E_{\text{peak}} = \frac{CV_A^2}{2} \quad (\text{A.2})$$

The amount of energy, which is lost in the circuit through the resistor  $R_p$ , is,

$$E_{\text{loss}} = \int_0^{2\pi/\omega} \frac{[V_A \cdot \sin(\omega t)]^2}{R_p} dt = \frac{\pi \cdot V_A^2}{\omega \cdot R_p} \quad (\text{A.3})$$

According to the equation (A.3), the quality factor of the LC tank with parallel resistor is,

$$Q_{L,C,R_p} = 2\pi \frac{\frac{CV_A^2}{\pi V_A^2}}{\omega R_p} = R_p \omega C \quad (A.4)$$

This quality factor is frequency dependent. At the LC tank's resonance frequency  $\omega_0 = 1/\sqrt{LC}$ , resulting quality factor is equal to

$$Q_{L,C,R_p} = R_p \sqrt{\frac{C}{L}} \quad (A.5)$$

The quality factor values for several tank circuits are shown in Figure A.2 [36].

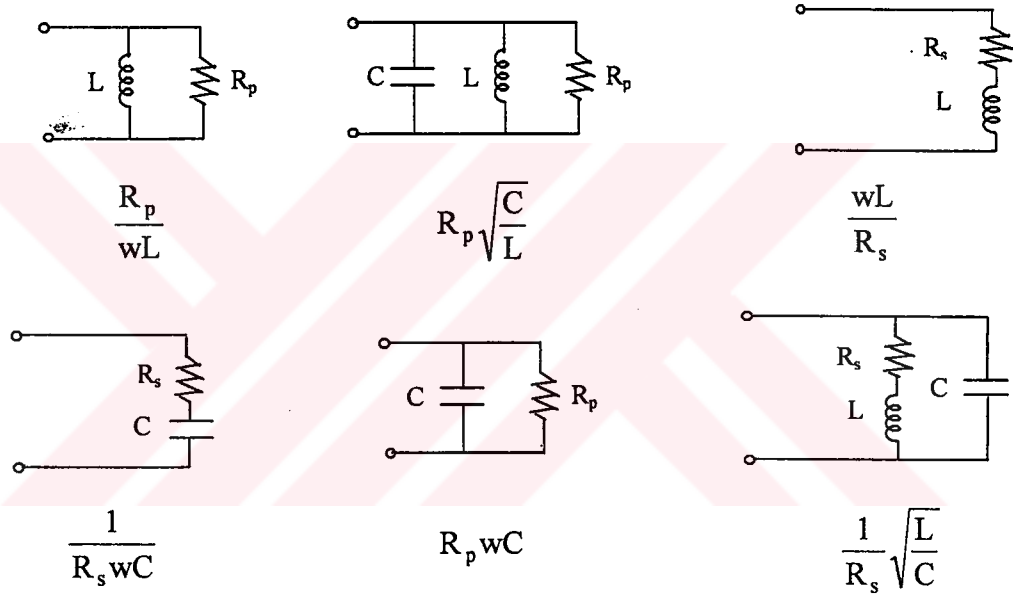


**Figure A.2** Quality Factors for different tank circuits [36].

## A.2 Basic Properties of RLC Circuits

As shown in Figure A.3a, a capacitor  $C_1$  is placed in parallel with an inductor  $L_1$  that resonates at a frequency  $\omega_{\text{res}} = 1/\sqrt{L_1 C_1}$ . At this frequency the impedance of the inductor is  $jL_1\omega_{\text{res}}$  and the impedance of the capacitor is equal to  $1/(jC_1\omega_{\text{res}})$  and these values are equal. And they form infinite impedance, so that the circuit has an infinite quality factor. But in practice, inductors (and capacitors) suffer from resistive components. The series resistance used in the inductor is modelled as shown in Figure A.3b. The  $Q$  of the inductor is defined as

$$Q = L_1 \omega / R_s \quad (A.6)$$

The equivalent impedance of the circuit is

$$Z_{eq}(s) = \frac{R_s + L_1 s}{1 + L_1 C_1 s^2 + R_s C_1 s} \quad (A.7)$$

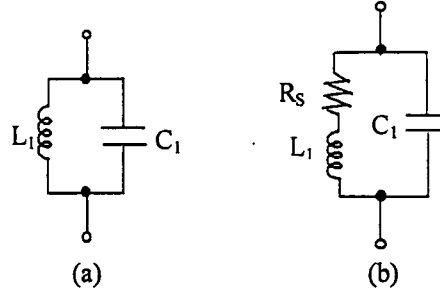


**Figure A.3** LC tank (a) ideal (b) realistic

$$|Z_{eq}(s = j\omega)|^2 = \frac{R_s^2 + L_1^2 \omega^2}{(1 - L_1 C_1 \omega^2)^2 + R_s^2 C_1^2 \omega^2} \quad (A.8)$$

That means the impedance does not go to infinity at any \$s=j\omega\$. And it can be said that the circuit has a finite Q. The circuit of Figure A.3b can be transformed to an equivalent topology, which is more easily analyzed and designed.

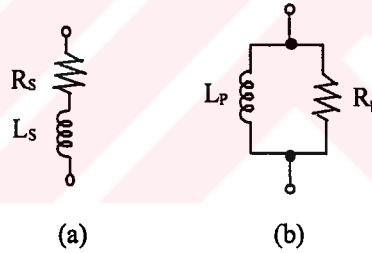


**Figure A.4** Conversion of a series combination to parallel combination (a) Series (b) parallel.

For a narrow frequency range, it is possible to convert the circuit to the parallel configuration, which is showed in Figure A.4b. And for the two impedances to be equal:

$$L_1 s + R_s = \frac{R_p L_p s}{R_p + L_p s} \quad (A.9)$$

If we rewrite the formula, considering only steady state response:

$$(L_1 R_p + L_p R_s)j\omega + R_s R_p - L_1 L_p \omega^2 = R_p L_p j\omega \quad (A.10)$$

Then,

$$L_1 R_p + L_p R_s = R_p L_p \quad (\text{A.11})$$

$$R_s R_p - L_1 L_p \omega^2 = 0 \quad (\text{A.12})$$

From these 2 equations,

$$L_p = L_1 \left( 1 + \frac{R_s^2}{L_1^2 \omega^2} \right) \quad (\text{A.13})$$

Remember  $L_1 \omega / R_s = Q$  and this value of  $Q$  is typically greater than 3 for monolithic inductors. Therefore equation (A.13) can be written as

$$L_p \approx L_1 \quad (\text{A.14})$$

and for resistor

$$R_p \approx \frac{L_1^2 \omega^2}{R_s} \approx Q^2 R_s \quad (\text{A.15})$$

As a result, the parallel network has the same reactance but a resistance  $Q^2$  times the series resistance. Similar results can be derived for RC network shown in Figure A.5.

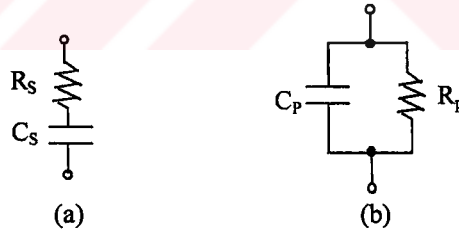


**Figure A.5** Equivalent (a) series and (b) parallel RC circuits

$$R_p \approx \frac{1}{R_s C_s^2 \omega^2} \quad (\text{A.16})$$

$$C_p \approx C_s \quad (\text{A.17})$$

In Figure A.6 the conversion of the tank to three parallel elements is shown.

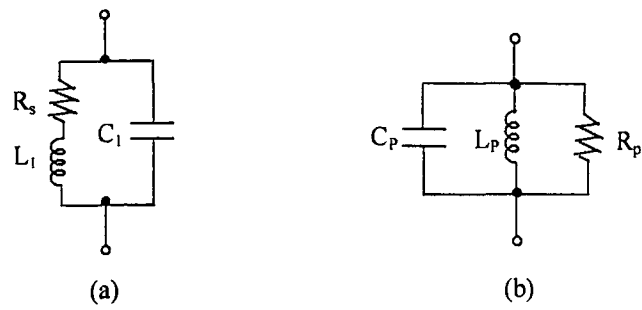


**Figure A.6** Conversion of a tank to three parallel components [21]

This equivalence breaks down as  $\omega$  departs from the resonance frequency where  $C_p=C_1$ . These transformations are also very helpful in impedance transformation.

## B APPENDIX B

As mentioned in Chapter 5, the phase noise simulations of the quadrature LC VCOs are done with different simulators. One of them is HP-ADS, which calculates in a different way. Below we are going to explain how HP-ADS calculates the phase noise

### B.1 Phase noise calculation of HP-ADS

HP-ADS calculates two kinds of phase noise [104]. These are, phase noise (in dBc) calculated from frequency sensitivity analysis and the phase noise (in dBc) calculated from mixing analysis.

Phase noise of an oscillator can be analyzed by two separate, independent methods as mentioned before. The frequency sensitivity noise, may be viewed as the oscillator acting as VCO and changing its operating frequency due to FM modulation caused by noise generated in the oscillator. This method calculates the flicker noise effects. The small signal mixing of noise comes from the nonlinear behaviour of the oscillator, where noise mixes with the oscillator signal and harmonics to mix to sideband frequencies on either side of the oscillator signal. The calculated pnm (phase noise from mixing analysis) and pnfm (phase noise from frequency sensitivity analysis) results of an oscillator are shown in Figure B.1. The red plot is calculated by frequency sensitivity analysis and the blue one is by mixing analysis.

It is shown that the result of pnfm plot has 30dBc/Hz-phase noise at 1Hz. This is not possible cause the carrier power is always higher than side bands. HPADS makes calculations for the small band FM. If you imagine the spectrum of FM/PM modulation with high modulation index, you remember a much wider spectrum than  $2 \cdot f_m$ . The amplitudes of the sidebands (multiples of  $f_m$ ) are governed by Bessel functions. Even the carrier can disappear if the modulation index is 2.3. For these kind of noisy oscillators SSB phase noise power is no longer a useful parameter.

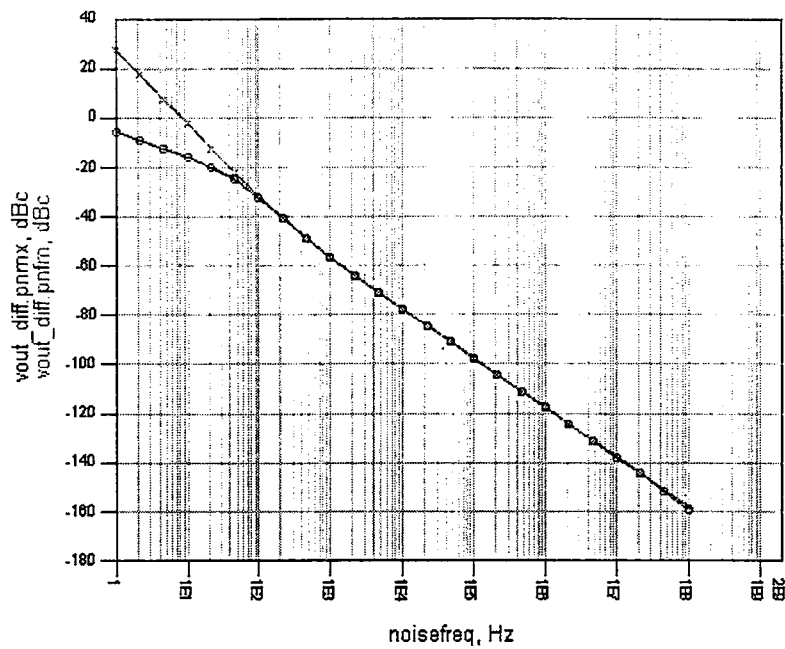


**Figure B.1** Phase noise results of an oscillator

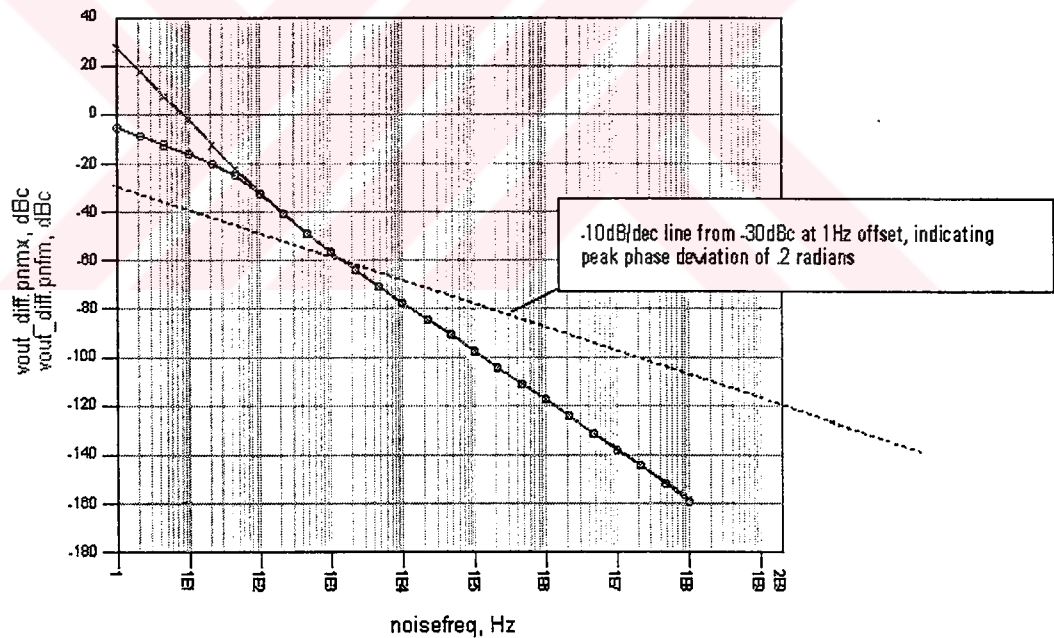


**Figure B.2** The method showing to find the valid results for phase noise of an oscillator.

The phase noise simulation result that HP-ADS outputs is the SSB power density, derived from the spectral density of the phase fluctuations, which is what HP-ADS actually calculates. So, HP-ADS calculates phase noise correctly, but the relationship to SSB phase noise power does not hold for noisy oscillators.

Therefore to learn the correct phase noise results, as shown in Figure B.2, a -10dB/decade line starting at -30dBc/Hz at 1Hz offset from the carrier, indicating

peak phase deviation of 0.2 radians, has to be drawn on your result plot. This allows estimation of accuracy of SSB phase noise power results derived from phase noise spectral density. The phase noise values below this line are valid.



166

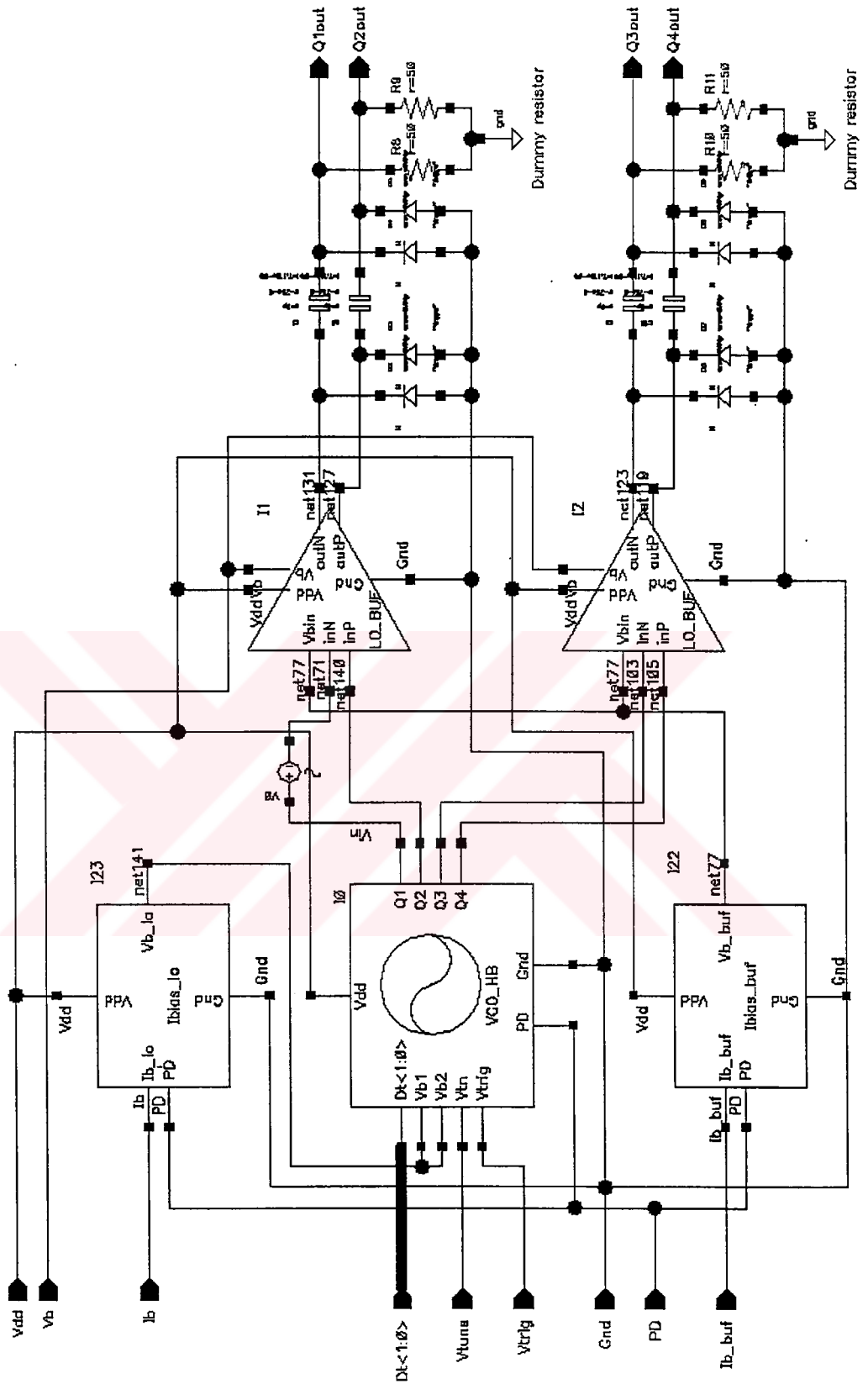
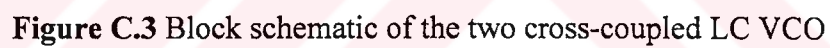


**Figure C.2** The block schematic of the quadrature LC VCO with bias and buffer circuits.





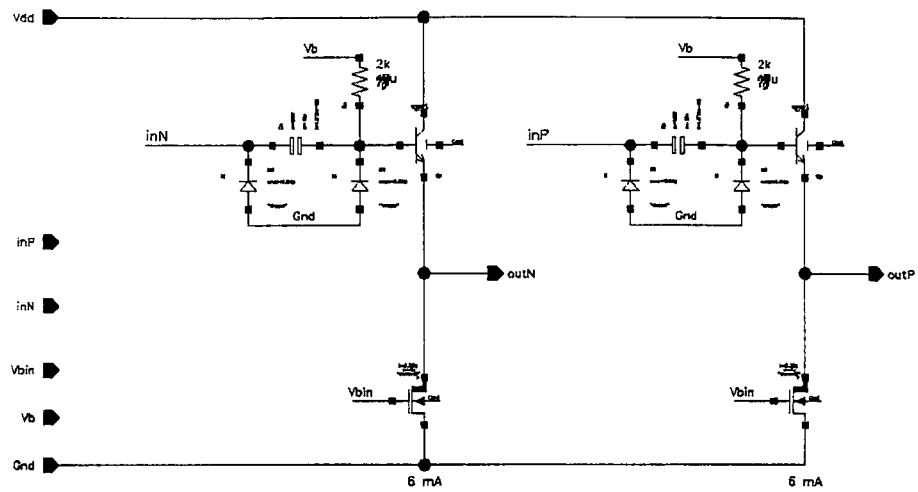


**Figure C.5** Schematic of the buffers of the quadrature LC VCO

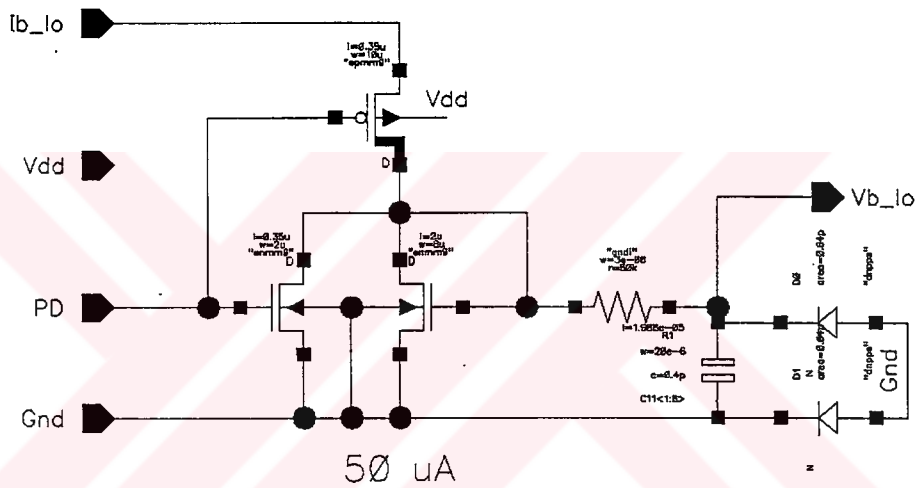


**Figure C.6** The schematic of the biasing circuit of the quadrature LC VCO

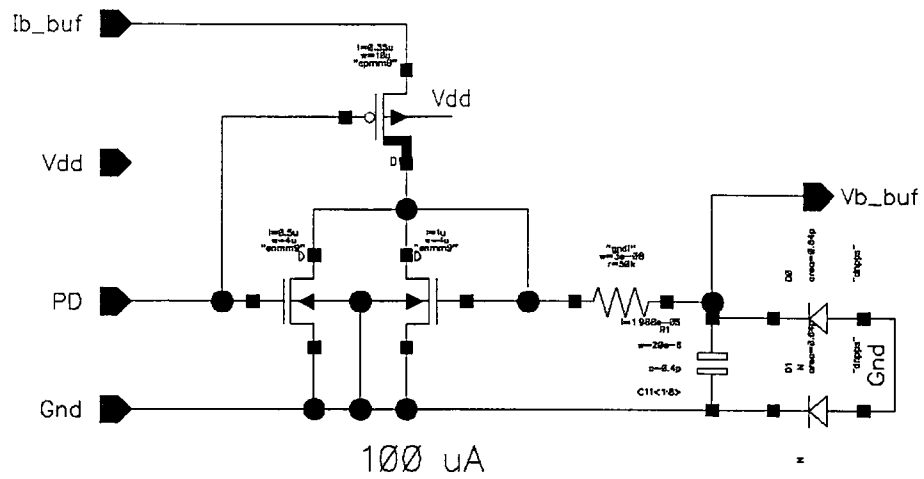


**Figure C.7** The schematic of the biasing circuit of the buffer of the quadrature LC VCO.

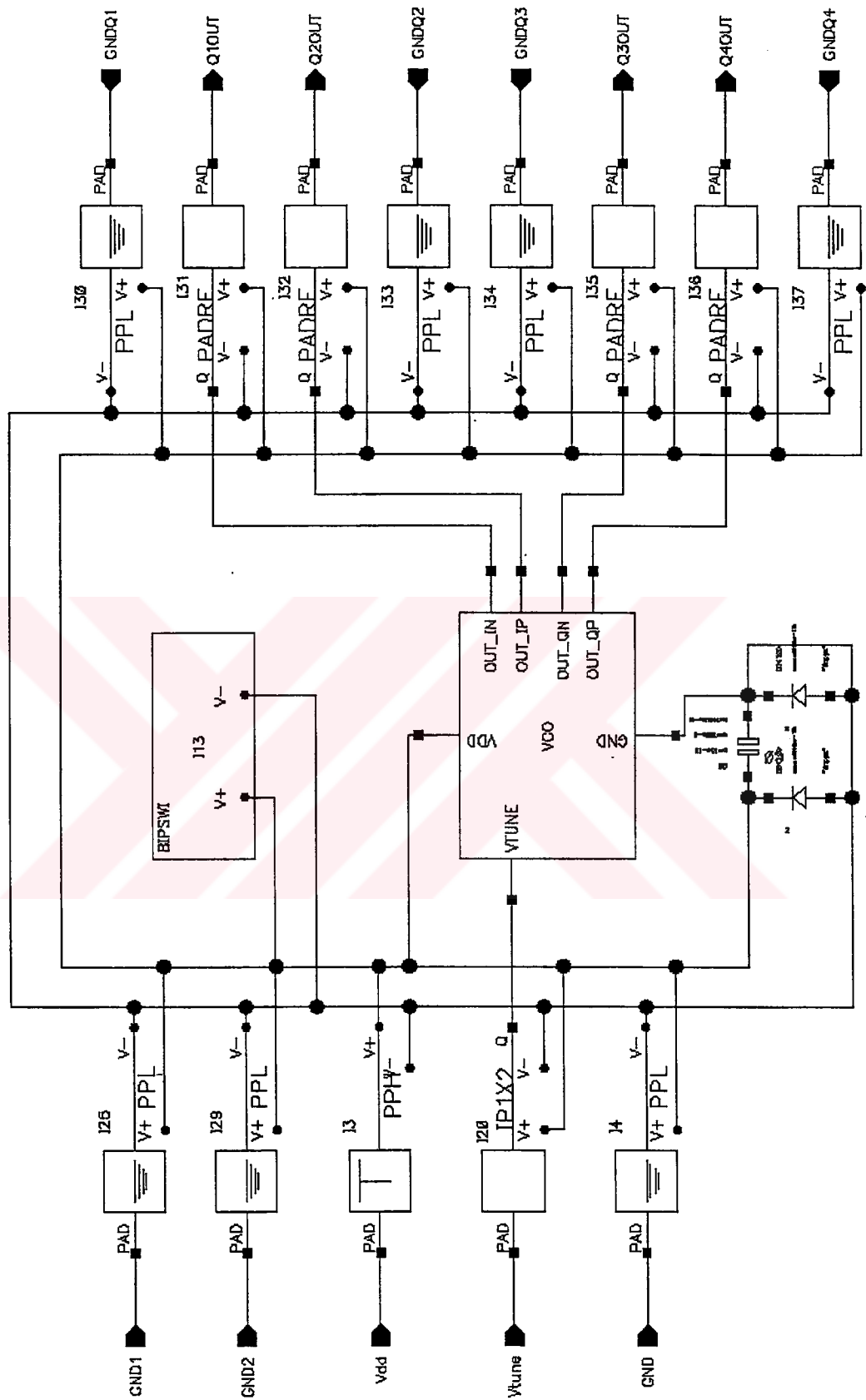


**Figure C.8** Top level block schematic of the quadrature ring VCO.

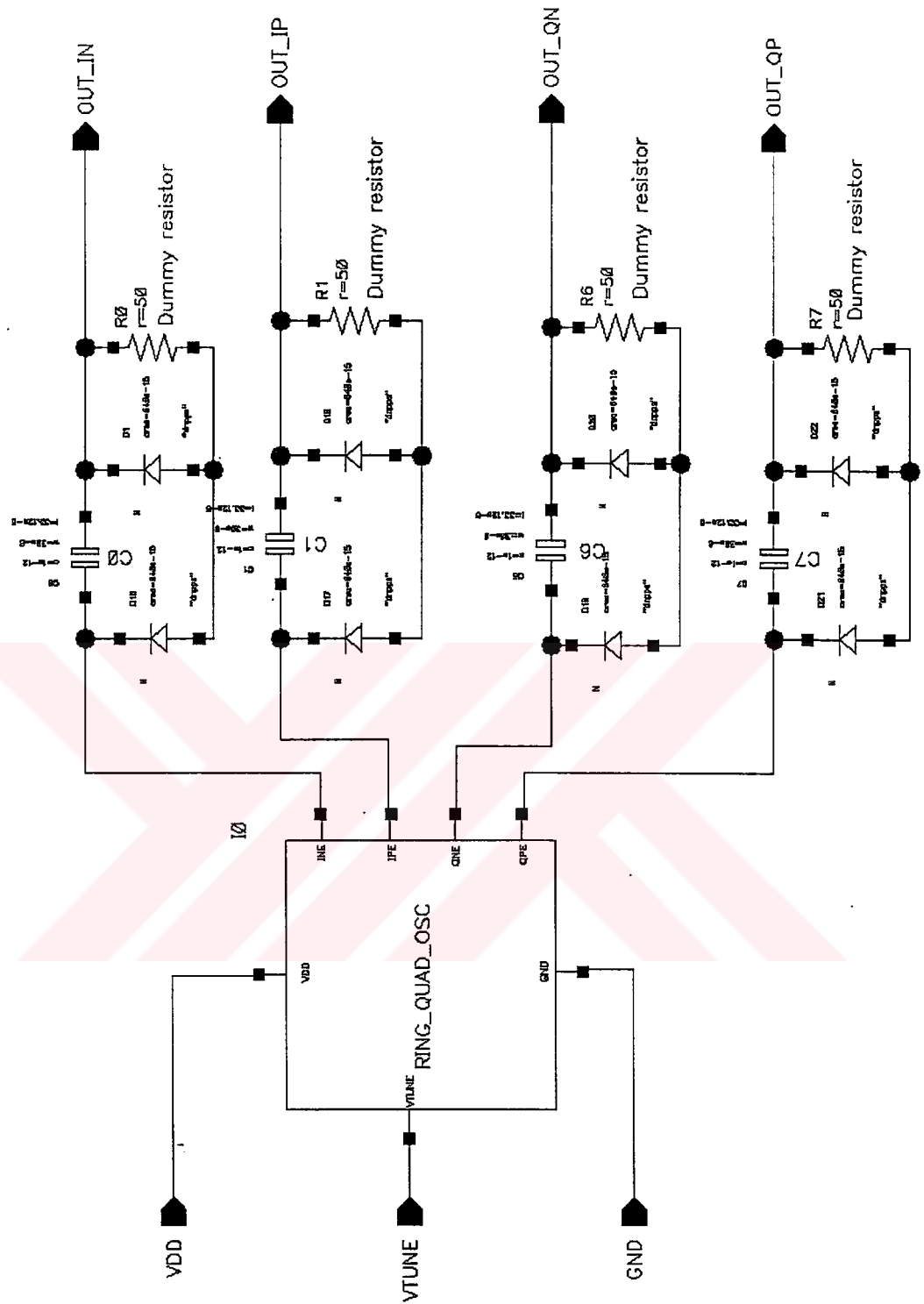


**Figure C.9** Block schematic of the quadrature ring VCO with output capacitors

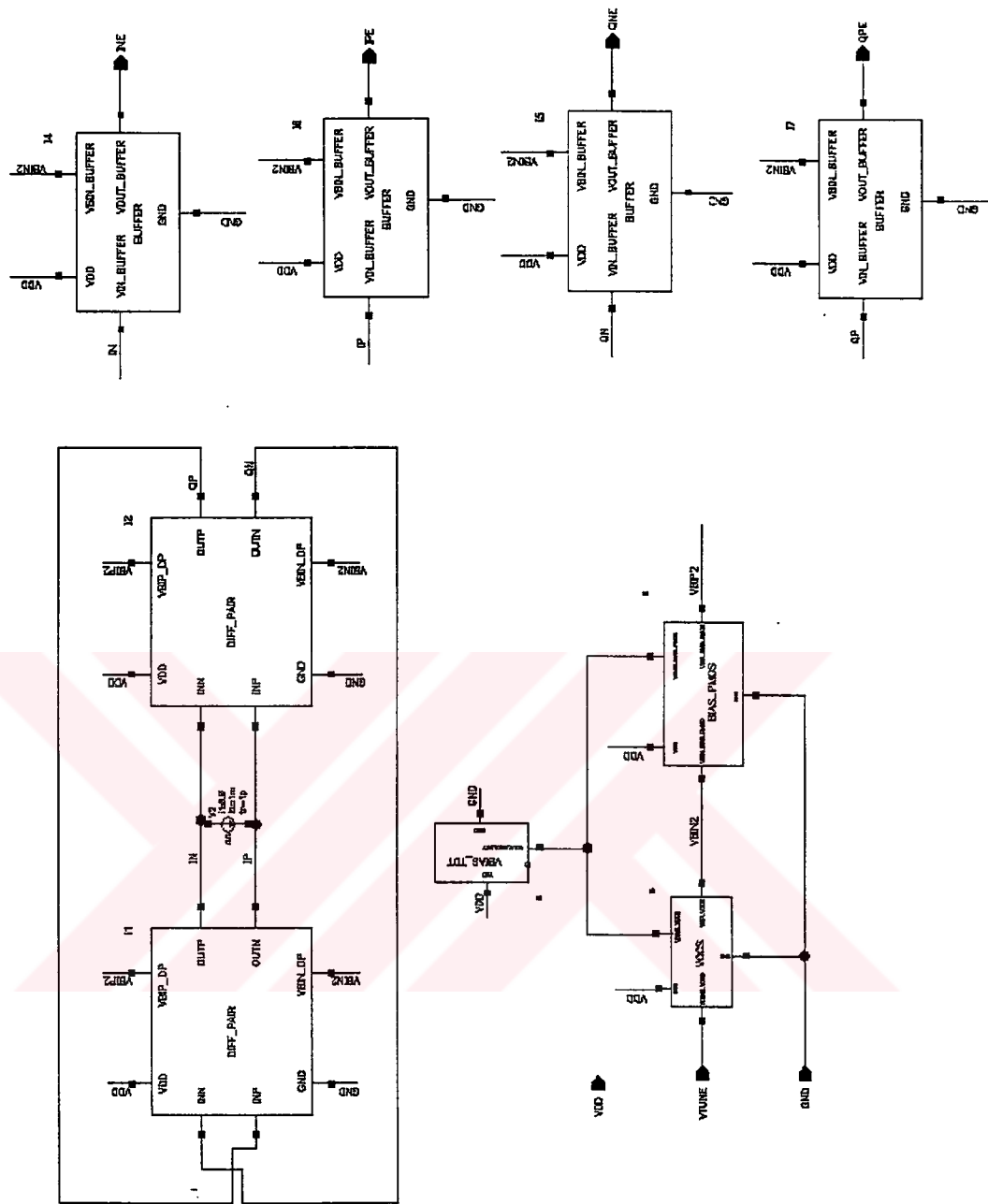


**Figure C.10** The block schematic of the quadrature ring VCO with biasing and buffer circuits.

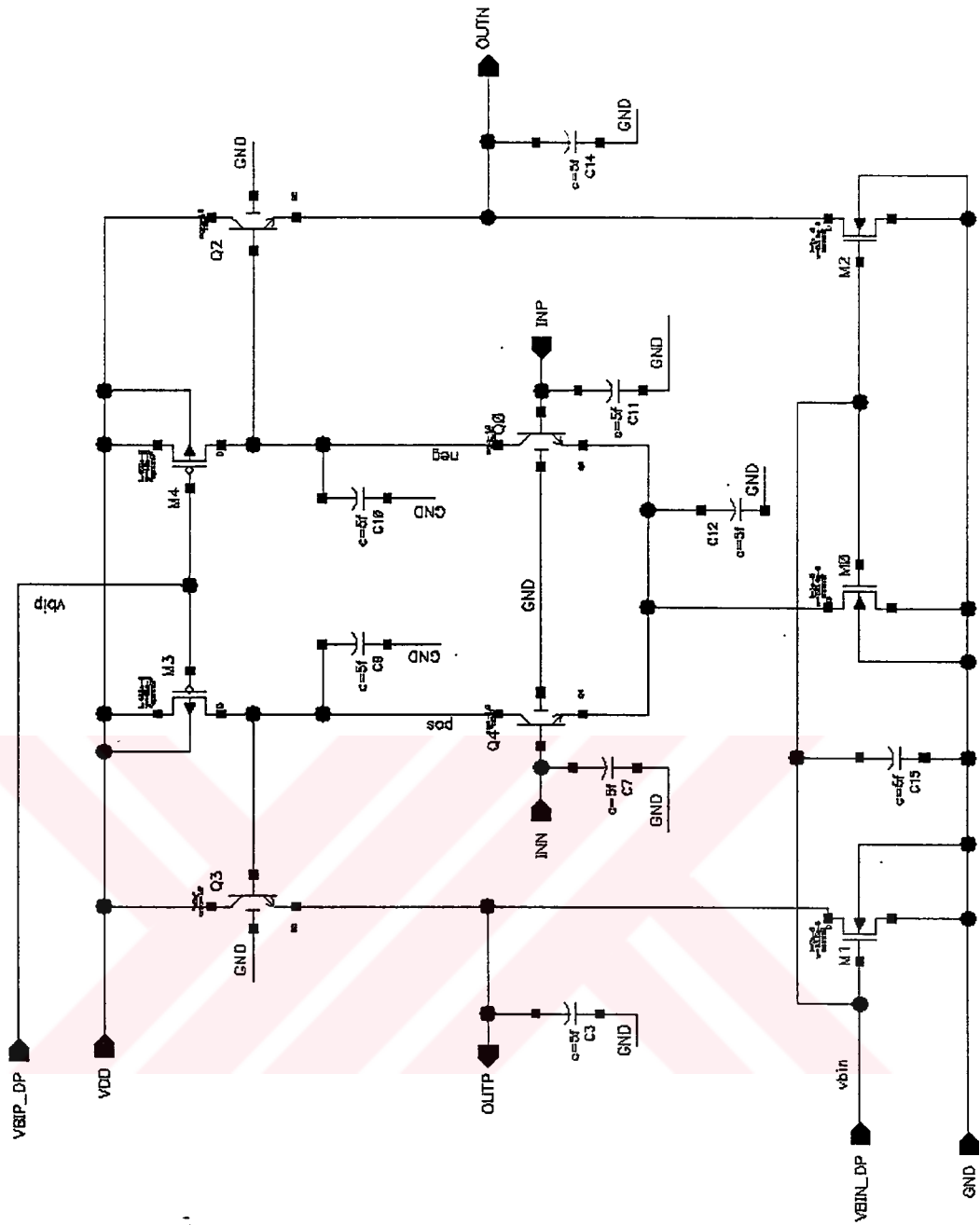


**Figure C.11** The schematic of one of the delay cell of quadrature ring VCO

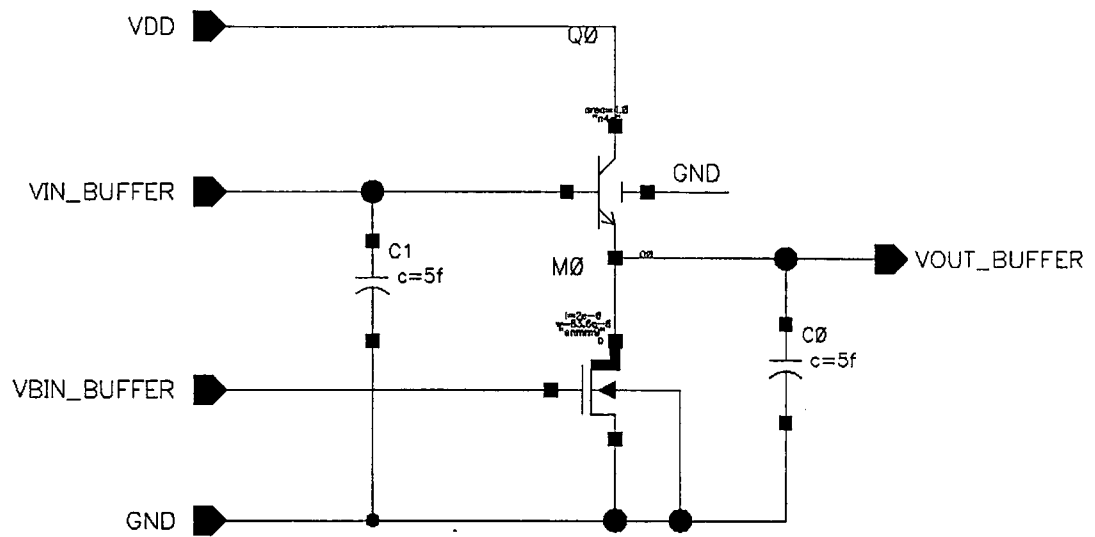


**Figure C.12** The schematic of the one of the buffer circuit of the quadrature ring VCO.

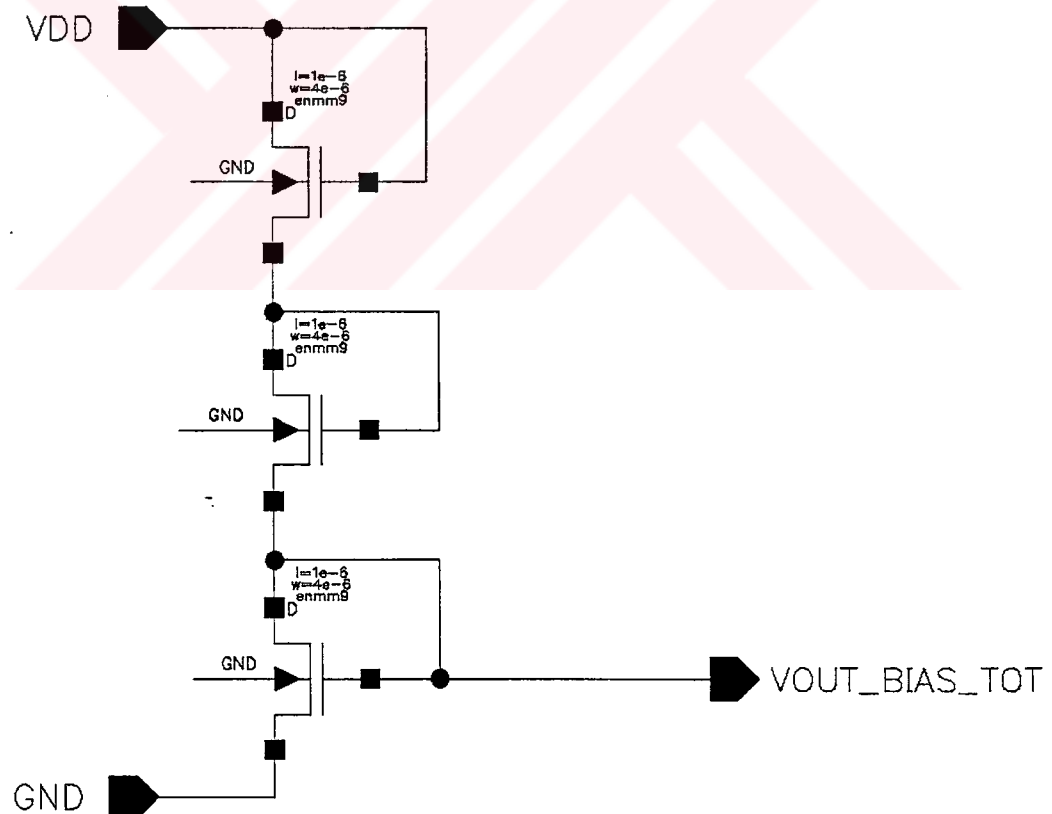


**Figure C.13** The schematic of the PMOS and NMOS biasing circuits of the quadrature ring VCO.



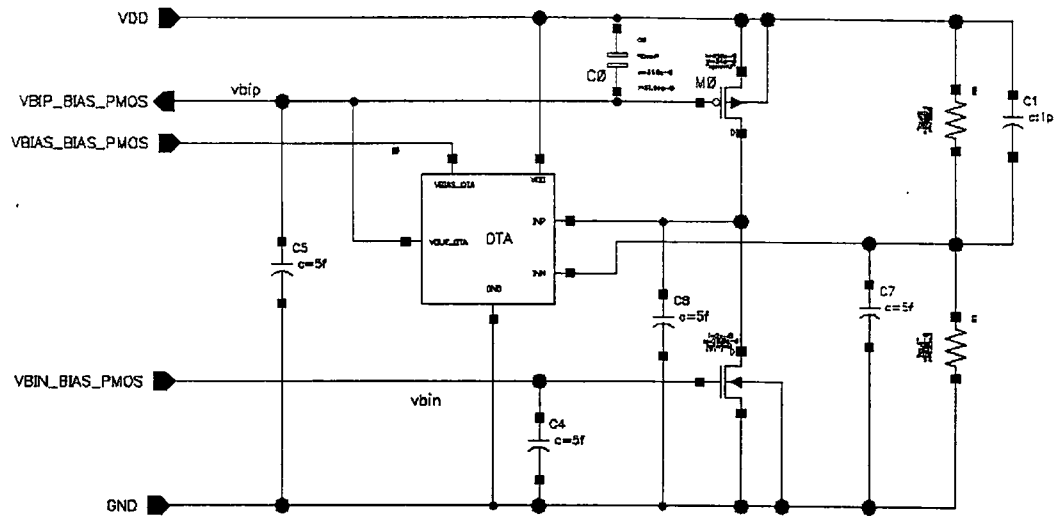


**Figure C.16** The schematic of the PMOS biasing circuit of the ring VCO

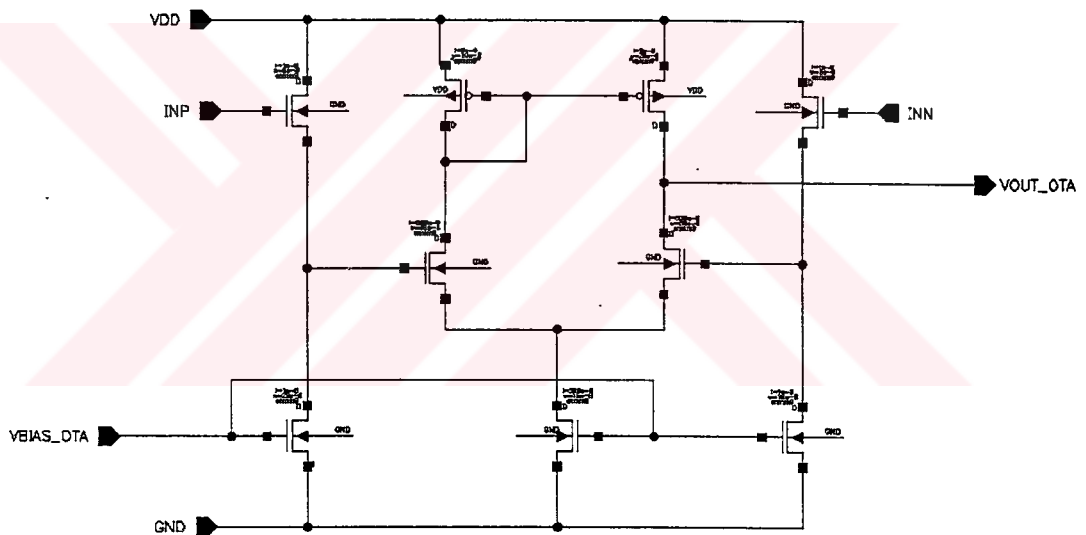


**Figure C.17** The schematic of the op-amp circuit used in the PMOS biasing circuit of the quadrature ring VCO.

## **AUTOBIOGRAPHY**

Pınar Taşcı was born in Istanbul in 1977. She completed her primary and secondary education in 50. Yıl Cumhuriyet İlkokulu in 1988 and in İSTEK Uluğ Bey High School in 1995 respectively. She received her B.Sc degree in Electronics and Communication Engineering from Istanbul Technical University, Faculty of Electrical and Electronics Engineering, Department of Electronics and Communication Engineering in 1999. She was a RF IC design engineer with Alcatel Teletaş (Istanbul) and Alcatel Microelectronics (Brussels), where she worked on RF mixers, polyphase filters for DECT project and RF VCOs for HIPERLAN2 project, from 1999 to 2001. Her research interests includes RF mixers and quadrature VCOs.



**TC YÜKSEKÖĞRETİM KURULU  
DOKÜMANTASYON MERKEZİ**