

ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

**DESIGN OF A CMOS FEEDFORWARD AUTOMATIC
GAIN CONTROL SYSTEM FOR OPTICAL FRONT-ENDS**

M.Sc. THESIS

İrem CÖMERTOĞLU

Department of Electronics and Communication Engineering

Electronics Engineering Programme

JUNE 2025

ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

**DESIGN OF A CMOS FEEDFORWARD AUTOMATIC
GAIN CONTROL SYSTEM FOR OPTICAL FRONT-ENDS**

M.Sc. THESIS

**İrem CÖMERTOĞLU
(504221204)**

Department of Electronics and Communication Engineering

Electronics Engineering Programme

Thesis Advisor: Assoc. Prof. Dr. Mustafa Berke YELTEN

JUNE 2025

İSTANBUL TEKNİK ÜNİVERSİTESİ ★ LİSANSÜSTÜ EĞİTİM ENSTİTÜSÜ

**OPTİK ÖN ALICILAR İÇİN CMOS İLERİ BESLEMELİ
OTOMATİK KAZANÇ KONTROL SİSTEMİ TASARIMI**

YÜKSEK LİSANS TEZİ

**İrem CÖMERTOĞLU
(504221204)**

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Elektronik Mühendisliği Programı

Tez Danışmanı: Doç. Dr. Mustafa Berke YELTEN

HAZİRAN 2025

İrem CÖMERTOĞLU , a M.Sc. student of ITU Graduate School student ID 504221204, successfully defended the thesis entitled “DESIGN OF A CMOS FEEDFORWARD AUTOMATIC GAIN CONTROL SYSTEM FOR OPTICAL FRONT-ENDS”, which she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor : **Assoc. Prof. Dr. Mustafa Berke YELTEN**
Istanbul Technical University

Jury Members : **Prof. Dr. Günhan DÜNDAR**
Boğaziçi University

Assoc. Prof. Dr. Nil Banu TARIM
Istanbul Technical University

Date of Submission : **30 May 2025**

Date of Defense : **30 June 2025**





To my family,



FOREWORD

I would like to express my sincere gratitude to my thesis advisor, Assoc. Prof. Dr. Mustafa Berke Yelten, for his advice and experiences during my research journey at İTÜ VLSI Laboratories. He stood by me through both the highs and the lows. I also extend my thanks to committee members Prof. Dr. Günhan Dünder and Assoc. Prof. Dr. Nil Banu Tarım for their valuable time and contributions to this project.

I am deeply thankful to Yiğit, Yusuf, Elif, Betül, Berkay, Alper, and Emre for their friendship and continual encouragement. This thesis would not have been possible without their presence and motivation. Being part of the İTÜ VLSI Laboratory family has truly been a special experience. I am grateful to Çağlar Yılmaz for his support and guidance.

I am thankful to my family for their unconditional support and love throughout my whole life. My sister and Eray have always been there when I needed them. I am deeply thankful for my family's love and presence, which is more than words can express. I truly appreciate my cousin Gülçin for standing by me during my hardest times.

Finally, I would like to thank Ali Doğuş Güngördü—not only for his valuable guidance in analog design but also for being my biggest source of strength throughout this journey. His unwavering support, kindness, and belief in me meant more than I can say. I am especially thankful to have had him by my side — as a mentor, a teammate, and someone very special in my life.

This work was supported in part by the Department of Scientific Research Projects, Istanbul Technical University, under Project 43932.

June 2025

İrem CÖMERTOĞLU
Electronics Engineer

TABLE OF CONTENTS

	<u>Page</u>
FOREWORD	ix
TABLE OF CONTENTS	xi
ABBREVIATIONS	xiii
SYMBOLS	xv
LIST OF TABLES	xvii
LIST OF FIGURES	xx
SUMMARY	xxi
ÖZET	xxiii
1. INTRODUCTION	1
1.1 Purpose of Thesis	3
1.2 Literature Review	3
1.3 Contributions of This Thesis	7
1.4 Thesis Organization	7
2. AGC FUNDAMENTALS	9
2.1 Optical Receiver System Architecture	9
2.2 AGC Performance Parameters	10
2.3 AGC with a Feedforward Loop	11
2.3.1 Variable-gain transimpedance amplifier	13
2.3.2 Peak detector	23
2.3.3 Analog-to-digital converter	28
2.3.4 Control voltage generation (CVG) circuit	31
2.3.5 The proposed AGC system	33
3. LAYOUT AND SIMULATION RESULTS	37
3.1 Peak Detector Simulations	37
3.2 Analog-to-Digital Converter Simulations	42
3.3 Control Voltage Generation Circuit Simulations	44
3.4 Feedforward Automatic Gain Control System Simulations	47
3.5 PVT Simulations	62
3.6 Monte Carlo Simulations	68
4. CONCLUSION AND FUTURE WORKS	71
REFERENCES	75
CURRICULUM VITAE	79



ABBREVIATIONS

ADC	: Analog-to-Digital Converter
AGC	: Automatic Gain Control
CDR	: Clock/Data Recovery
CMOS	: Complementary Metal-Oxide-Semiconductor
CS	: Common-Source
CVG	: Control Voltage Generator
EMI	: Electromagnetic Interference
EPON	: Ethernet Passive Optical Network
FB-AGC	: Feedback Automatic Gain Control
FF	: Fast-Fast
FF-AGC	: Feedforward Automatic Gain Control
IEEE	: Institute of Electrical and Electronics Engineers
IRN	: Input-Referred Noise
ISI	: Intersymbol Interference
LDO	: Low-Dropout Regulator
LED	: Light-Emitting Diode
MC	: Monte Carlo
NRZ	: Non-Return-To-Zero
OTA	: Operational Transconductance Amplifier
OWC	: Optical Wireless Communication
PAM-4	: Pulse Amplitude Modulation 4-Level
PD	: Peak Detector
POF	: Plastic Optic Fiber
PON	: Passive Optical Network
RF	: Radio Frequency
SS	: Slow-Slow
FF	: Typical-Typical
VGA	: Variable Gain Amplifier
VG-TIA	: Variable Gain Transimpedance Amplifier
VLC	: Visible Light Communication



SYMBOLS

A	: Ampere
A₀	: Open-loop Gain
AC	: Alternative Current
C	: Capacitor
C_{GD}	: Gate-Drain Capacitance
C_{GS}	: Gate-Source Capacitance
C_{in}	: Input Capacitance
C_{ox}	: Gate-Oxide Capacitance per Unit Area
C_P	: Photodiode Capacitance
dB	: Decibel
dBm	: Decibel milliWatt
DC	: Direct Current
F	: Farad
Gbps	: Gigabit Per Second
g_m	: Transconductance
HD	: Harmonic Distortion
Hz	: Hertz
I_D	: Drain Current
IP₃	: Third-Order Intercept Point
LPE	: Layout Parasitic Extraction
Mbps	: Megabit Per Second
P_{1dB}	: 1 dB Compression Point
Q	: Quality Factor
R	: Resistor
R_F	: Feedback Resistor
R_{on}	: On-Resistance
R_T	: Transimpedance Gain
RMS	: Root Mean Square
r_o	: Drain-Source Resistance
SCH	: Schematic
V_{DD}	: Drain Supply Voltage
V_{DS}	: Drain-Source Voltage
V_{GS}	: Gate-Source Voltage
V_{th}	: Threshold Voltage
V	: Volt
W	: Watt
W/L	: Width-to-Length Ratio
Z_{in}	: Input Impedance
β	: Feedback Factor
Ω	: Ohm
μ_n	: Mobility of Electrons



LIST OF TABLES

	<u>Page</u>
Table 2.1 : Input Signal Ranges of the Gain Settings.	22
Table 2.2 : Design Criteria of the AGC System.	36
Table 3.1 : Transistor Sizes in the Comparator.	43
Table 3.2 : Device Sizes of the Proposed CVG.	45
Table 3.3 : Device Sizes of the Proposed TIA.....	48
Table 3.4 : 1-dB Compression Point Results.	52
Table 3.5 : Variation and Compression Ratios at the Output Voltage.	67
Table 4.1 : Comparison with Literature	72



LIST OF FIGURES

	<u>Page</u>
Figure 1.1 : Simplified block diagrams of feedforward (a) and feedback (b) AGCs.	2
Figure 1.2 : FB-AGC example of an optical receiver.	4
Figure 1.3 : FF-AGC example of an optical receiver.	5
Figure 1.4 : Hybrid-AGC burst mode optical receiver [14].	6
Figure 1.5 : FB-AGC-VLC optical receiver [15].	6
Figure 2.1 : Block diagram of an optical receiver.	9
Figure 2.2 : Block diagram of the AGC in this thesis.	13
Figure 2.3 : Current-to-voltage converter models: (a) simple resistor and (b) shunt-shunt feedback TIA.	14
Figure 2.4 : (a) A single CS stage and (b) a CMOS inverter-based TIAs with resistive feedback.	17
Figure 2.5 : Parasitic capacitances in an inverter-based TIA.	18
Figure 2.6 : Schematic of the VG-TIA.	21
Figure 2.7 : (a) Conventional diode-capacitor peak detector and equivalent op-amp-source follower-based peak detector topologies (b) open-loop current-mode peak detector	25
Figure 2.8 : Input impedance problem of the conventional current-mode PD.	26
Figure 2.9 : Schematic of the proposed peak detector.	27
Figure 2.10 : Schematic of the current-mode Flash ADC.	29
Figure 2.11 : Schematic of the comparator.	30
Figure 2.12 : Schematic of the CVG.	31
Figure 2.13 : Schematic of the proposed AGC system.	34
Figure 3.1 : The layout of the proposed PD.	38
Figure 3.2 : Conversion gain of the PD.	38
Figure 3.3 : Input impedance of the PD.	39
Figure 3.4 : Attack and settling behavior for various input amplitudes.	40
Figure 3.5 : The output current with respect to the input amplitude.	40
Figure 3.6 : Transient transfer characteristic of the PD.	41
Figure 3.7 : Attack and release behavior in the transient domain.	41
Figure 3.8 : Output current transient noise.	42
Figure 3.9 : Layout of the flash ADC	43
Figure 3.10 : DC sweep with the hysteresis.	44
Figure 3.11 : Layout of the CVG circuit.	45
Figure 3.12 : Generated control voltages in the whole input range – DC sweep... ..	46
Figure 3.13 : The output voltages of the CVG for each gain setting.	46
Figure 3.14 : R_{on} of the activated triode-region transistors in the input signal range.	47
Figure 3.15 : Layout view of the inverter-based VG-TIA.	48

Figure 3.16 : Full chip layout with the pad ring.	49
Figure 3.17 : An ideal PAM-4 signal with a 10 μ A amplitude.	50
Figure 3.18 : The DC Sweep with the hysteresis	51
Figure 3.19 : The AC gain range of the schematic-level system simulation.	52
Figure 3.20 : The AC gain range of the post-layout system simulation.	53
Figure 3.21 : Transient pulse response of the AGC circuit at the schematic level. .	54
Figure 3.22 : Transient pulse response of the AGC circuit at the post-layout level. .	54
Figure 3.23 : Peak-to-peak output voltage across the input range in the schematic simulations.	55
Figure 3.24 : Peak-to-peak output voltage across the input range in the post-layout simulations.	55
Figure 3.25 : Input-referred noise over the spectrum.	56
Figure 3.26 : Attack and release time schematic simulation.	57
Figure 3.27 : Attack and release time post-layout simulation.	57
Figure 3.28 : Eye diagrams — Boundaries of the (a) first, (b) second, and (c) third gain settings.	59
Figure 3.29 : Eye diagrams — Boundaries of the (a) fourth, (b) fifth, and (c) sixth gain settings.	60
Figure 3.30 : Pie chart of the DC power consumption.	61
Figure 3.31 : Eye diagram results of four different setups (a) SCH-TT and LPE-TT, (b) LPE-FF and LPE-SS.	62
Figure 3.32 : AC transimpedance gains at the SS, TT, and FF corners.	64
Figure 3.33 : Linearity check for the FF and SS corners.	64
Figure 3.34 : Post-layout attack and release times at the SS, TT, and FF corners. .	65
Figure 3.35 : Input-referred noise plots at the SS, TT, and FF corners.	65
Figure 3.36 : Peak-to-peak output voltage amplitudes in the FF corner.	66
Figure 3.37 : Peak-to-peak output voltage amplitudes in the SS corner.	66
Figure 3.38 : The output voltage signals of the Monte Carlo simulations.	68
Figure 3.39 : Peak-to-peak output voltage amplitudes in the Monte Carlo tests.	69

DESIGN OF A CMOS FEEDFORWARD AUTOMATIC GAIN CONTROL SYSTEM FOR OPTICAL FRONT-ENDS

SUMMARY

This thesis presents the design of a high-compression feedforward Automatic Gain Control (AGC) system generated for optical front-ends operating at 1 Gbps PAM-4 modulation over Plastic Optical Fiber (POF) and Visible Light Communication (VLC). Since the amplitude of the input signal exhibits large variations in these applications, maintaining a stable output signal amplitude is crucial. The AGC system aims to ensure reliable signal processing under dynamic conditions.

There are two different methods to apply AGC: feedforward and feedback AGC. This thesis chooses a feedforward methodology for the AGC system due to its fundamental advantages in speed and stability. This choice allows the system to react almost instantly to changes in signal strength. It achieves sub-microsecond attack and release times in post-layout simulations. The primary benefit of the design is achieving a high compression ratio of approximately 30 dB.

The AGC system controls the gain of a variable-gain transimpedance amplifier (VG-TIA) by utilizing secondary circuits that sense the signal amplitude and generate the required voltages. In detail, the main building blocks of the AGC include a variable-gain transimpedance amplifier (VG-TIA), a peak detector, a current-mode Flash analog-to-digital converter (ADC), and a control voltage generation (CVG) circuit. A CMOS inverter with resistive feedback topology is employed in the TIA design. The VG-TIA supports both coarse and fine gain control through switched resistors and triode-region transistors, respectively. Since the gain is changing with respect to the amplitude, the signal level should be examined. For this purpose, a high-dynamic-range peak detector has been designed. The peak detector accurately measures the input signal amplitude with minimal ripple, ensuring fast and reliable gain updates. The ADC compares the mirrored input current against reference currents from a bandgap source to produce digital gain control signals. In parallel, the CVG circuit generates analog voltages proportional to the signal amplitude, which finely tune the TIA gain by adjusting the gates of triode-region transistors.

The entire system is implemented in a commercial 65 nm CMOS process and operates from a 1.8 V supply. Post-layout simulation results indicate that the proposed AGC achieves a 32 dB gain adjustment while maintaining a bandwidth of over 700 MHz across all gain settings. The compression ratio is approximately 30 dB, and the attack and release times are around 250 ns. The design demonstrates its effectiveness as a fast, stable, and high-performance AGC solution for next-generation optical front-ends.



OPTİK ÖN ALICILAR İÇİN CMOS İLERİ BESLEMELİ OTOMATİK KAZANÇ KONTROL SİSTEMİ TASARIMI

ÖZET

Bu tez çalışmasında, 1 Gbps veri hızında PAM-4 modülasyonunda veri iletimi amaçlanmıştır. Plastik optik fiber (POF) ve görünür ışık haberleşmesi (visible light communication-VLC) uygulamaları için ileri beslemeli otomatik kazanç kontrol sistemi (feedforward automatic gain control-FFAGC) tasarlanmıştır. Günümüzde, özellikle otomotiv ve endüstriyel uygulamalarda POF ve VLC teknolojileri çok popülerdir. Bunun en büyük nedenleri ise elektromanyetik girişime karşı bağışıklıkları ve düşük maliyetli uzun mesafe iletimde sağladıkları avantajlardır.

POF'un spektral aralığı 520 nm ve 650 nm aralığıdır. Bu aralıkta en düşük kayıpla sinyal iletimi sağlayabilir. Bunun yanı sıra VLC sistemler görünür ışığı kullandıkları için 390 nm ve 750 nm aralığında işaret iletimi gerçekleştirebilirler. İki sistem de aynı spektral aralıkta veri iletimi yapar ve iletimde kullandıkları yöntem ışıktır. İkisinde de foto detektör kullanımı gereklidir. Bu uygulamalarda, giriş sinyalinin genliği büyük değişimler göstermektedir. Bu değişkenlik, sistemlerin kararlılığı ve güvenilirliği açısından ek önlemler alınmasını gerekli kılmaktadır. Kısaca, bu ortak özellikler ışığında iki sistemde de kullanılabilen bir sistemin tasarlanmasına karar verilmiştir. Tasarlanacak sistemin ana hedefi giriş genliğindeki değişimleri optik alıcı ön tarafında azaltarak çıkışa olabildiğince sabit bir genlik iletmektir. Böylece karşılaştırmalı devresinin karar verme sırasında hata yapma olasılığı azaltılacaktır. Sabit genlikte sinyal iletilmemesi durumunda, karar verici devrenin yanlış karar verme olasılığı artar. Bu durum özellikle yüksek veri hızlarında veri iletimi yapıldığı zaman göz diyagramının kapanmasına neden olur. Ayrıca bit hata oranının artmasına sebep olacaktır. Bu nedenle, optik alıcı sistemlerde kararlı genlik seviyelerinin sağlanması temel bir gereklilik hâline gelmiştir. Özellikle VLC sistemi kablolu bir haberleşme olduğundan, çok hızlı bir şekilde giriş sinyal genliği değişebilir. VLC ortamında, ortam ışığı değişimi, engel ve yansımalar gibi dinamik etkiler ani sinyal dalgalanmalarına yol açar. Bu durumlarda, hızlı bir yerleşme zamanına sahip AGC çok önemli bir görev görür. Karar verici devrenin eşik değerlerinin ayarlanması diğer bir yaklaşım olabilir; fakat bit hata oranı (bit error rate-BER) azaltmak için en iyi yöntem, hızlı bir AGC sistemine sahip olmaktır. Eşik değerlerinin adaptasyonu, belirli koşullarda yardımcı olsa da, sistemdeki gürültü ve doğrusallık bozulması nedeniyle yetersiz kalmaktadır.

AGC sistemleri genel olarak iki şekilde uygulanabilir. Geri beslemeli AGC (FB-AGC), daha geleneksel bir yaklaşımdır. Kazancı ayarlanabilen kuvvetlendiricinin (variable gain amplifier-VGA) çıkışı, bir genlik sezici (peak detector) ile sezilir. Bu sezilen değer, ayarlanmak istenen genlik seviyesindeki bir DC referans ile karşılaştırılır. Bu karşılaştırma sonucu üretilen hata sinyali ile VGA'nın kazancı kontrol edilir. Kontrol sinyali ideal durumda DC olmalıdır. Bu sebeple bir alçak geçiren süzgeç

kullanılmalıdır. Bu tarif edilen sistem, tıpkı bir faz kilitlemeli çevrime (phase locked loop-PLL) benzer. AGC için de bir anlamda genlik kitlemeli çevrim benzetmesi yapılabilir. FB-AGC için, kararlılık açısından hızlı bir sistem tasarlamak zordur. Çünkü genlik sezici devresi hali hazırda büyük bir RC zaman sabitine sahiptir. Bu sebeple çevrim süzgecinin zaman sabiti daha da büyük olmalıdır. Böylelikle, VGA kontrolü için yeterince sabit bir kontrol gerilimi oluşturulabilir. AGC için diğer bir yaklaşım ise ileri beslemeli AGC (FF-AGC) yöntemidir. Bu senaryoda, kararlılık sorunu olmadığı için belirli bir güç harcanarak hızlı bir AGC tasarlanabilir. Bu şekilde, daha kolay bir şekilde 1 mikrosaniye yerleşme zamanından daha hızlı bir sistem elde edilebilecektir. FF-AGC yapıları, özellikle yüksek hız gerektiren optik alıcılarda daha etkin bir performans sunmaktadır. FF-AGC’de sinyal, VGA girişinde aynı zamanda genlik sezici devresine gider. Genlik sezici çıkışındaki sinyal, dijital veya analog olarak VGA kazancını kontrol eder. FF-AGC için en kritik devre genlik sezicidir; çünkü genlik sezici, VGA’nın gördüğü tüm sinyal aralığını görür. Yani giriş dinamik aralığı, sadece VGA tarafından değil, aynı zamanda genlik sezici tarafından da sağlanmalıdır. Bu tez çalışmasındaki giriş dinamik aralık isteği 36 dB, genlik sezici dinamik aralığı ise 60 dB’ye kadar çıkabilmektedir. Ayrıca giriş çıkış arasındaki sıkıştırma oranı serim sonrası benzetimlerde 31.58 dB olarak bulunmuştur. Bu çalışmanın getirdiği yeniliklerden ilki, yüksek dinamik aralıklı bir genlik sezici topolojisidir. Tasarlanan AGC sistemi ile hedeflenen 1 mikrosaniden daha hızlı AGC cevabı başarılmıştır. AGC sıkıştırma oranı, en kötü senaryoda dahi 30 dB üzerinde kalmıştır. Bu sonuçlar, tasarımın hem hassasiyet hem de hız açısından beklentileri karşıladığını göstermektedir.

Tasarlanan AGC, bir optik alıcı sisteminin parçasıdır. Kısaca, girişte düşük gürültülü bir akım tampon (buffer) devresi, fotodetektörden aldığı sinyali, geçiş empedansı ayarlanabilen bir geçiş empedansı kuvvetlendiricisine (transimpedance amplifier-TIA) aktarır. TIA devresi için bir CMOS evirici tabanlı topoloji kullanılmıştır. Bu tercihin sebebi, CMOS eviricide hem NMOS hem de PMOS gerilim-akım dönüşümüne katkıda bulunduğu için, en iyi gürültü performansı bu topoloji ile başarılabilir. Fakat CMOS evirici tabanlı yapının en büyük problemi, proses, gerilim ve sıcaklık değişimlerinde (process-voltage-temperature veya kısaca PVT) gürültü ve doğrusallık performanslarının çok fazla değişkenlik göstermesidir. Bunun sebebi, sabit bir DC akım oluşturulmamasıdır. PVT köşelerinde sabit bir akım sağlayabilmek için, adaptif bir gerilim kaynağı CMOS eviriciyi beslemiştir. Kopya kutuplama (replica-bias) ile bir LDO vasıtasıyla adaptif kaynak oluşturulur. Böylelikle, tasarlanan TIA devresinin PVT performansı iyileştirilmiştir.

FF-AGC için, girişteki akım sinyali TIA devresine ve bir kopyası genlik sezici devresine (peak detector-PD) gönderilir. Genlik sezici çıkışı da kendi içerisinde iki kopya üretir. Bu kopyalardan biri, analog-dijital dönüştürücü (analog to digital converter-ADC) devresini besler. ADC devresine gelen bilgi akım temelli olduğu için ADC tasarımında da yüksek oranda akım aynalarından yararlanılmıştır. Referans akımlar ile yapılan karşılaştırmalar ile TIA için dijital kontrol bitleri üretilir. Genlik sezici çıkışındaki diğer kopya ise bir gerilim dönüştürücü devresini (control voltage generator-CVG) besler. Bu şekilde ise analog kontrol gerilimi üretilmiştir. Gerilim dönüştürücü devresi temel olarak direnç ve diyot bağlantılı NMOS transistörleri kullanarak girişteki akım genliğine orantılı olarak çıkış gerilimi oluşturur. Diyot

bağlantılı transistörün ve direnç elemanının akım - gerilim arasındaki ilişkiyi kullanır. TIA kazancı, doğal olarak geribesleme direncini kontrol ederek ayarlanmıştır. Dijital kontrol, anahtarlar ile paralel direnç sayısını artırma ve azaltma üzerine kuruluyken, analog kontrol, her paralel direncin yanına doğrusal bölgede çalışan bir MOS eklenmesiyle elde edilmiştir. PD çıkışındaki genlik bilgisi iki kez kullanılır. CVG ve ADC devreleri ile TIA kazancı hem analog hem de dijital olarak ayarlanabilir. AGC sıkıştırma oranını artıran bu yöntem, bu çalışmanın getirdiği yeniliklerden biridir. Tasarlanan TIA, PAM-4 modülasyonu ile çalışacağından doğrusallığın sağlanması önemlidir. Bunun yanında, TIA bant genişliği, serim sonrası 700 MHz olarak elde edilmiştir. Bu değer, 1 Gbps bir PAM-4 sistemi için yeterli olmuştur. Girişe indirgenmiş TIA gürültüsü 127 nA olarak elde edilmiştir. Verilen göz diyagramı (eye diagram) benzetim sonuçları, TIA devresinin gürültü ve doğrusallık performansını güçlü bir şekilde ortaya koymuştur. Tüm alt bloklar, birbirleriyle uyumlu çalışacak şekilde sistematik olarak entegre edilmiştir. Tez çalışması 65 nm CMOS teknolojisi ile tasarlanmış olup, üretime yollanmıştır.

Sonuç olarak, serim sonrası benzetimler TIA için 32 dB kazanç aralığı, 31.6 dB sıkıştırma oranı, 700 MHz'ten daha fazla bir bant genişliği, 1 Gbps PAM-4 optik alıcı için yeterince iyi bir doğrusallık ve gürültü performansını PVT varyasyonlarına rağmen başarmıştır. Sistem girişindeki işaret 62.5 katlık bir genlik değişimine sahiptir. Bu oran çıkış gerilim sinyalinde 1.64 kata kadar indirilmiştir. TIA tarafında geliştirme, analog-dijital hibrit bir kazanç ayarlama yöntemi ve PVT varyasyonuna dayanıklı bir veri yolu sağlamak olmuştur. Bu TIA'ya uygun FF-AGC sistemi için, ADC ve analog kontrol üretici ile FF-AGC yapısına yeni bir yaklaşım getirilmiştir. Ayrıca, yüksek dinamik aralıklı bir genlik sezici tasarlanarak genlik sezicinin FF-AGC için darboğaz oluşturması engellenmiştir. AGC sıkıştırma oranı yaklaşık 30 dB olup, AGC yerleşme süresi 1 mikrosaniye altında elde edilmiştir. Kısacası, bu çalışma yeni nesil optik ön alıcılar için hızlı, kararlı ve yüksek performanslı bir AGC çözümü ortaya koymaktadır. Bu çözüm, gelecekteki yüksek veri hızına sahip iletişim sistemlerinde de temel bir yapı taşı olabilir.

Gelecek planlar içerisinde, üretime gönderilen çipin VLSI laboratuvar ortamında prototiplenmesi vardır. Ayrıca tasarlanan AGC yapısına saat-veri geri kazanımı (clock data recovery-CDR) eklenerek hassas genlik ayarlanması ve bu tezde ortaya konan çözümlerin daha yüksek veri hızına sahip optik alıcı sistemlerine uyarlanması planlanmaktadır.



1. INTRODUCTION

There has been a rise in the popularity of mobile devices, as well as the use of multimedia and music/video streaming in daily life. Consequently, overall data traffic on sub-10 GHz is expanding [1]. The predominant serial-link technique now is copper-based coaxial cables. However, these have some disadvantages, such as high-frequency attenuation caused by dielectric loss and a skin effect. Due to their weight and rigidity, coaxial cables are difficult to install in residential settings. They are also prone to electromagnetic interference [2]. Conversely, optical communication has significant advantages that will address the increasing need in the future. The key strengths are achieving high data rates with minimal loss, immunity to electromagnetic interference (EMI), and enhanced flexibility. Additionally, the nature of light reduces the usage of the spectrum. Glass optical fibers are the most widely used due to their good performance in long-distance, fast data transmission. However, for moderate data rates in short-range applications, plastic optical fibers (POF) stand out due to their lower cost and greater flexibility [3], [4].

The POF spectral range is 520 to 650 nm [4]. In comparison, optical wireless communication (OWC) systems operating within the visible light spectrum (390 to 750 nm) are commonly referred to as visible light communication (VLC) [5]. Visible light communication is gaining popularity as an eco-friendly and energy-efficient alternative to traditional RF-based systems. It is based on high-speed modulated light-emitting diodes (LEDs), which do not compromise lighting performance, enabling simultaneous lighting and data transmission. The dual feature makes VLC very suitable for short- and medium-range communication systems, including wireless local and personal area networks, as well as vehicle and body area networks. As the global focus shifts towards replacing fluorescent bulbs with energy-efficient LEDs, VLC is expected to play a key role in future communication systems by offering EMI-free communication in sensitive settings, such as hospitals, and

enabling innovative features, including wearable technology and machine-to-machine communication [6].

In short, VLC and POF systems operate within the same spectral range and utilize light to transmit information. They both use photodiodes at the receiving end to detect light signals and convert them to electrical signals. Also, POF [7] and VLC [8] have their own IEEE standards that define the fundamentals of data transmission. They must cope with massive variations in light source power, necessitating a gain control system. Automatic gain control (AGC) systems are used to dynamically adjust the receiver gain, ensuring the signal amplitude remains within the optimal processing zone at all times. This functionality is especially crucial in VLC and POF systems, as the brightness of the received light can fluctuate due to environmental changes, proximity, or mobility. Without AGC, the received power of the signal varies drastically, causing either the receiver to saturate or the signal to become too weak to detect precisely. AGC enhances the system's robustness and signal quality through continuous gain correction, ensuring dependable data reception [9].

The operating mechanism of AGC is based on adjusting the amplifier gain in response to the amplitude of the input signal. There are two different structures for implementing AGC: feedback AGC (FB-AGC) and feedforward AGC (FF-AGC). Figure 1 shows the typical block diagrams of these systems. The main difference lies in where the peak detector senses the signal. A peak detector (PD) senses the signal at the input in a feedforward AGC system. Therefore, the inputs to both the peak detector and the variable gain amplifier (VGA) are identical. After the peak

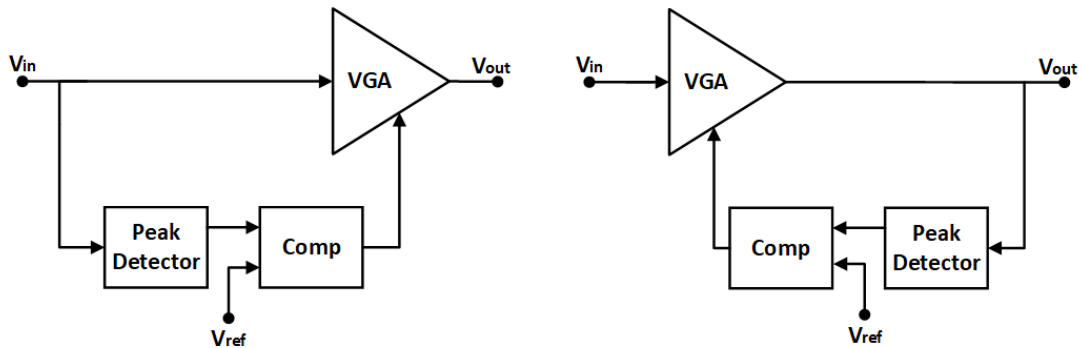


Figure 1.1 : Simplified block diagrams of feedforward (a) and feedback (b) AGCs.

detected, it is compared with a reference. The result of this comparison generates the required control voltage, which adjusts the gain of the main amplifier. Feedback AGC systems commonly use an equivalent circuit. In this case, the input of the peak detector is located at the output of the VGA. There are several differences between FB-AGC and FF-AGC. First, FB-AGC requires a loop filter to maintain stability, thus making it inherently difficult to make the system fast. Second, FB-AGC requires an exponential control voltage generator to maintain the same settling time for all input voltages. These two are the disadvantages of the FB-AGC system. Third, FF-AGC requires a large dynamic range peak detector because the peak detector is at the input and directly sees the input amplitude variation [9]. Despite this, this thesis focuses on FF-AGC due to its inherently stable operation and fast settling time, which are crucial for an optical receiver system.

1.1 Purpose of Thesis

This thesis develops an AGC system for optical receivers utilized in applications where the input amplitude may fluctuate significantly. Plastic Optical Fiber (POF) applications resemble wireline scenarios, where amplitude variations can occur due to factors such as fluctuations in driver laser amplitude, cable degradation from aging or bending, and variations in cable length that allow for the use of different POF cables within the same system. In Visible Light Communication (VLC), the anticipated amplitude variation at the receiver may be even more pronounced due to the system's wireless nature and the considerable changes in distance between the signal source and the receiver. While limiting amplifiers are suitable for Non-Return-to-Zero (NRZ) coded systems, multi-level Pulse Amplitude Modulation (PAM) systems necessitate an AGC to reduce variations in slicer threshold values. This research focuses on creating a fast-settling AGC with a high compression ratio tailored for these applications.

1.2 Literature Review

In this section, the use of Automatic Gain Control (AGC) in optical receivers will be examined. Optical receivers differ from traditional receivers due to their unipolar nature; photodetectors either inject current when light is present or produce negligible

current when light is absent. This characteristic eliminates the need for wave rectification and peak detection [10]. Fig. 1.2 illustrates an example where the output of the transimpedance amplifier (TIA) is averaged by a simple resistor-capacitor (R-C) circuit and compared with a replica TIA output using an amplifier. The output from this amplifier can then be utilized to control the transimpedance gain of the TIA.

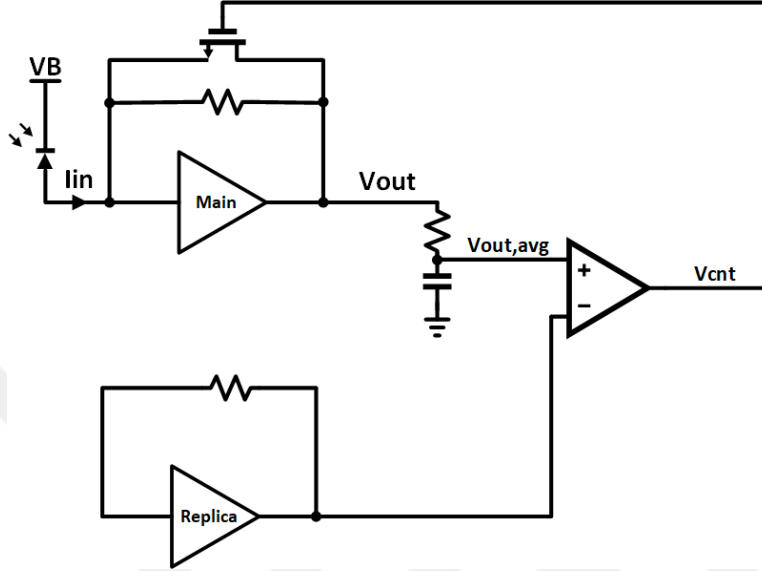


Figure 1.2 : FB-AGC example of an optical receiver.

The AGC amplifier described in [11] features a triple negative feedback open-loop amplifier and implements feedback AGC (FB-AGC). However, several challenges arise with this approach. First, tapping into the signal path requires a large resistor to minimize signal disturbance; unfortunately, this arrangement can introduce parasitic capacitance, thereby degrading the bandwidth. Second, the control signal regulates a MOS resistor, which is nonlinear and may limit the control range. Third, as an FB-AGC system, it necessitates a large time constant, leading to slow settling times. Moreover, both FB-AGC and feedforward AGC (FF-AGC) are influenced by the dynamics of the TIA, including peaking, bandwidth, and group delay, all of which vary with the gain of the TIA. To mitigate these issues, [12] proposes controlling the open-loop gain of the voltage amplifier to compensate for these variations by correlating the control voltage with the open-loop amplifier gain and employing additional MOS resistors. However, these structures depend heavily on precise adjustments, raising concerns regarding their robustness under varying process and temperature conditions.

An example of FF-AGC is shown in Fig. 1.3 [13]. Detecting a current signal at the input can be challenging; however, this example utilizes the input voltage and incorporates a large resistor to minimize current draw from the high-speed photodetector. An integrator functions as a low-pass filter for high-speed signals, extracting a direct current (DC) voltage from the input. This DC signal ultimately regulates the transimpedance gain.

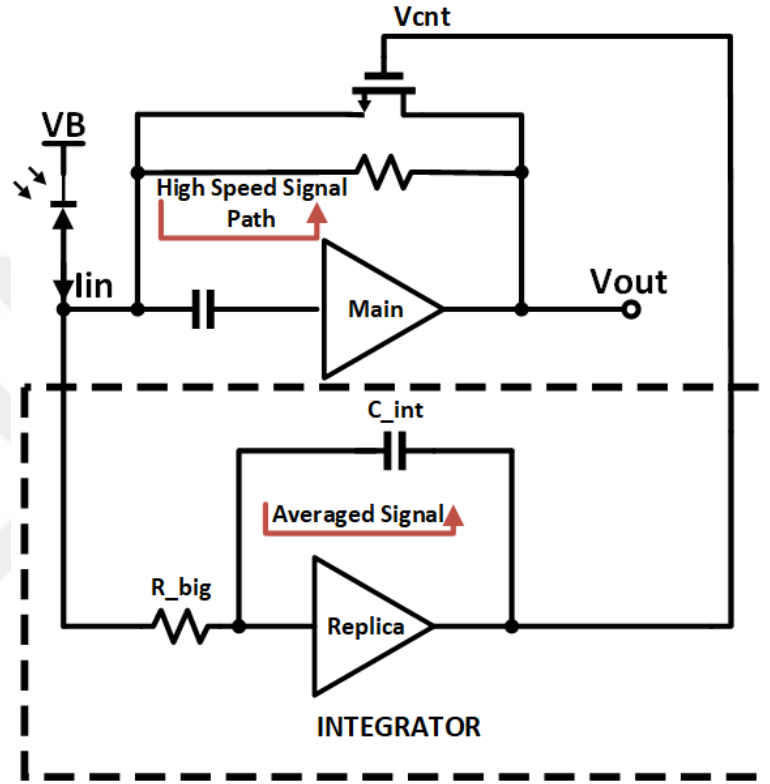


Figure 1.3 : FF-AGC example of an optical receiver.

The literature lacks information about Automatic Gain Control (AGC) in optical receivers. Even when relevant papers exist, they often do not provide details on the dynamics of the AGC loop or its specifications. A burst mode optical receiver front-end with AGC is described in [14]; this receiver employs a hybrid approach that incorporates both Feedforward AGC (FF-AGC) and Feedback AGC (FB-AGC). The feedforward control accelerates the AGC settling time, while the feedback loops enhance accuracy. The architecture of the receiver is illustrated in Fig. 1.4.

An AGC system for VLC is described in [15], utilizing a traditional feedback structure. This system incorporates an exponential control generator to maintain a constant loop

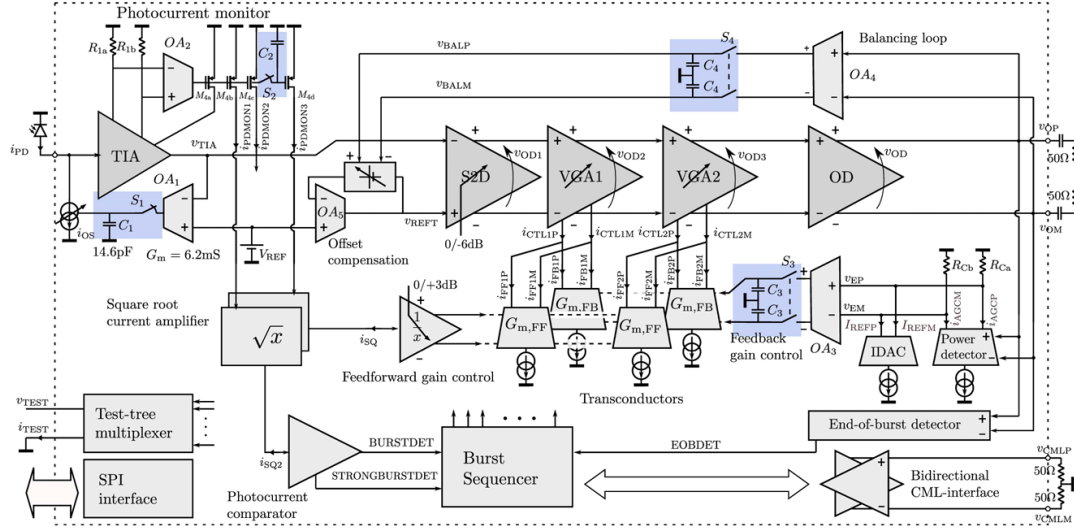


Figure 1.4 : Hybrid-AGC burst mode optical receiver [14].

settling time across varying signal amplitudes. The authors reported an impressive feedback AGC settling time of 200 ns. The receiver front-end is illustrated in Fig. 1.5. One of the key challenges in FB-AGC is generating an exponential control voltage using CMOS technology. Typically, approximations of exponential functions are employed to simplify the control circuit, as noted in [16].

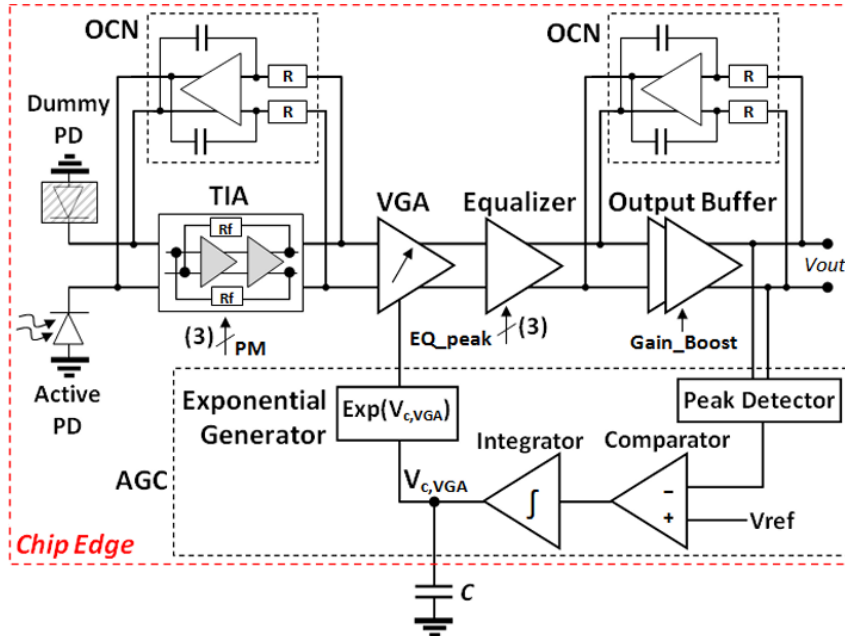


Figure 1.5 : FB-AGC-VLC optical receiver [15].

This thesis utilizes FF-AGC to simplify gain control, address stability issues, and facilitate rapid settling times while minimizing power consumption. The topology resembles that in [17], but it incorporates a hybrid approach that combines both analog and digital gain control.

1.3 Contributions of This Thesis

This thesis presents a novel AGC control scheme that integrates both analog and digital information regarding the input signal amplitude, resulting in a hybrid gain control approach. As a result, the FF-AGC achieves a significant compression ratio. Furthermore, a robust TIA structure is designed to accommodate process and temperature variations. The FF-AGC also ensures a rapid settling time for the receiver. The existing literature lacks comprehensive AGC solutions for optical receivers; this thesis provides a significant contribution to addressing this gap.

1.4 Thesis Organization

This work provides an overview of Automatic Gain Control (AGC) fundamentals in Chapter 2, which also details the Fast Feedback AGC (FF-AGC) and its associated sub-blocks, including peak detectors, variable gain amplifiers (VGAs), and analog-to-digital converters (ADCs). The proposed AGC system is outlined in the same chapter. Chapter 3 elaborates on the achieved schematic and post-layout simulation results, while Chapter 4 presents the conclusion and outlines future work.



2. AGC FUNDAMENTALS

2.1 Optical Receiver System Architecture

Automatic gain control systems are employed in numerous applications with a wide dynamic range of input signals, such as VLC and POF. Since both systems use light for transmission, a POF receiver can also be utilized for VLC. The focus of this thesis is on the design of an automatic gain control (AGC) system within an optical receiver architecture. To meet the performance standards for POF, the AGC should be fast enough for 1 Gbps PAM-4 communication.

Fig. 2.1 presents a detailed block diagram of an optical front end. The process begins with the photodiode, which detects the incoming light signal and converts it into a current based on its responsivity. The photodiode capacitance in POF and VLC applications is quite high; hence, a common-gate current buffer can be employed. The current buffer is often designed as a sophisticated circuit to meet the bandwidth and noise requirements. Since FF-AGC is more suitable for high data rates than FB-AGC, the current buffer simultaneously transmits the current signal to VG-TIA and the peak detector. The peak detector, which must be linear across a wide dynamic range, keeps the peak or RMS value of the signal. The next block, the analog-to-digital converter

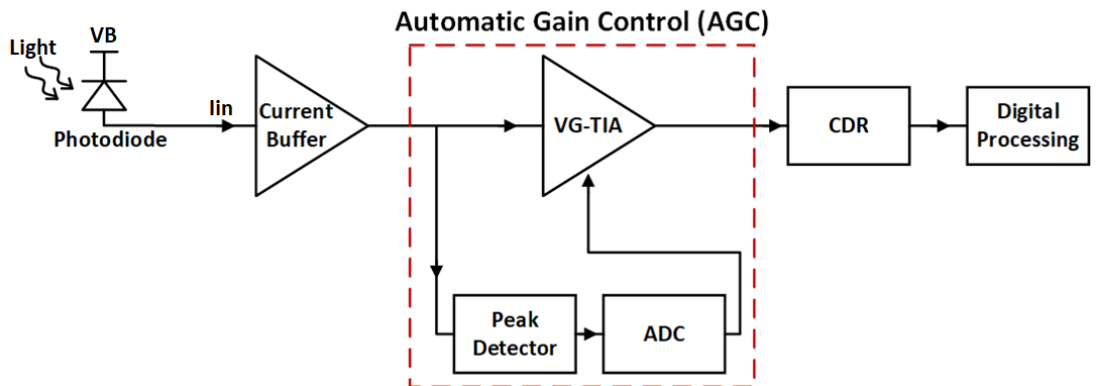


Figure 2.1 : Block diagram of an optical receiver.

(ADC), compares the peak current value with the reference currents, and the resulting bits are used to adjust the gain of the VG-TIA. Hence, the gain changes according to the amplitude of the incoming signal. The AGC transimpedance amplifier converts the incoming current to a voltage signal. Next, the clock signal is extracted from the signal, and the data is retimed using a clock/data recovery (CDR) circuit. Beyond that, data is processed by digital circuits.

2.2 AGC Performance Parameters

Several metrics illustrate the AGC performance. One of the key parameters is the compression ratio, which indicates the system tolerance across a wide range of variations [9]. The IEEE standard for POF receivers states that the input optical power can vary by up to 18 dBm, ranging from -17 dBm to 1 dBm [7]. This value corresponds to a power variation of about $20 \mu\text{W}$ to 1.25 mW and an input dynamic range ratio of 62.5. Assuming the photodiode responsivity is 0.5 A/V , the input signal amplitude varies from $10 \mu\text{A}$ to $625 \mu\text{A}$. Therefore, it is essential to achieve a high compression ratio in AGC, allowing the ADC design criteria to be relaxed somewhat. It ensures the stable amplitude of the output signal, regardless of variations in input amplitude. The compression ratio is calculated as,

$$\text{Compression Ratio} = \frac{\text{Input variation (dB)}}{\text{Output variation (dB)}} \quad (2.1)$$

Attack time is the duration for the AGC to respond to a sudden rise in the input signal level and a subsequent gain decrease. It indicates how fast the system may prevent clipping or saturation in the event of an abrupt increase in signal power. Release time refers to the time required for the AGC to increase its gain after a drop in the input signal level. Both parameters represent the system response to an abrupt change in the input signal. That is why they are crucial and should be investigated. Attack and release times reveal how fast the AGC changes its gain when the input changes. Settling time, on the contrary, indicates the duration required for the gain to fully stabilize within a specified range [18].

Another important parameter is the dynamic range of an AGC. It specifies the input signal range over which the AGC can operate linearly without introducing significant distortion or saturation [9]. It is highly important for multi-PAM modulated systems. The dynamic range is also an indicator of noise and compression. The smallest signal that can be detected without being lost in noise is the lowest limit of the dynamic range. In the receiver, the input block generally dominates the noise performance of the entire system. Consequently, if the gain control is implemented in the input block, it must be carefully designed to guarantee low noise levels and a wide dynamic range. On the contrary, linearity determines the upper limit of the range. Several tools can be employed to analyze linearity, including harmonic distortion (HD), third-order intercept point (IP3), and 1-dB gain compression point (P1dB). This thesis utilizes the 1-dB gain compression test and also the eye diagram to evaluate linearity in the Automatic Gain Control (AGC). As a result, the dynamic range parameter is extensive and provides significant insight into the system.

As discussed above, several metrics are available to test AGC performance. In this thesis, these parameters are optimized to design an automatic gain control (AGC) system with a high compression ratio and wide dynamic range.

2.3 AGC with a Feedforward Loop

Wireless and wireline receivers that use multi-PAM modulation employ AGC systems to maintain a constant output signal amplitude despite changes in the received signal strength. Chapter 1 provides a brief explanation of the two implementation techniques of AGC: feedback and feedforward control loops. FB AGC constantly controls the VGA output, detects the signal strength, and compares it with the reference values. The VGA gain is controlled according to this method. One of the key features of this method is that it requires a lower input dynamic range in the peak detector circuit since the loop compensates for input variations. Furthermore, the FB AGC is naturally more linear due to the feedback concept.

Although the FB AGC offers many advantages, this system has some disadvantages stemming from its feedback system, as well. Especially, systems with high compression ratios can experience stability problems under rapid or extreme input

changes. Moreover, the loop dynamics determine the settling and response times of the system, which can be challenging to handle for high data rates.

In contrast, the feedforward AGC senses the same input signal as the VGA. There is no feedback loop in this configuration; instead, a shunt branch processes the input data and sets the gain. This open-loop system does not have stability issues and can theoretically achieve zero settling time. This configuration enables rapid data rates. Conversely, since the peak detector senses the input signal, its dynamic range should cover the full range of possible input levels. Because there is no feedback mechanism to account for non-idealities, the whole signal path—including the gain control circuitry—should be highly linear to guarantee precise gain amounts.

Gain control can be accomplished using three distinct methods, namely continuous/analog control, digital control, and a mixed approach combining analog and digital. The choice of this method depends on the application requirements. Analog control requires challenging analog circuits for fine gain adjustments. Although this method provides precise adjustments, implementing it for a wide dynamic range input can be complex. As an alternative, digital control adjusts the gain steps discretely via logic circuits. Digital control simplifies the circuit design and is easy to implement for wide dynamic range applications. However, it may introduce quantization noise and degrade the compression ratio if the gain steps are too coarse. Combining these two methods to yield a hybrid solution is another option, which increases the system complexity. The difficulty arises from the need to integrate both digital logic and analog control circuitry. Still, this hybrid approach enables a high compression ratio in receivers with wide dynamic range inputs.

Due to the extensive dynamic range requirements of VLC and POF standards, a hybrid model that integrates both analog and digital control has been employed in this thesis. The proposed FF-AGC system receives the signal as a current, and all designed blocks operate as current-mode circuits. The variable-gain transimpedance amplifier converts the current into a voltage. Initially, the peak of the signal is detected by the PD, and the circuit generates two identical outputs, forming two parallel branches of the AGC. One path transmits the signal to a digital circuit for coarse gain adjustment. The

digital circuit is designed as a generic current-mode Flash ADC. The other path leads to a control voltage generator (CVG) circuit, which continuously adjusts the gain in fine-tuning mode. The dual-mode control leverages both methods, ensuring a high compression ratio across a wide dynamic range. Fig. 2.2 provides the block diagram of the designed system. The following sections will examine every block of the AGC in detail.

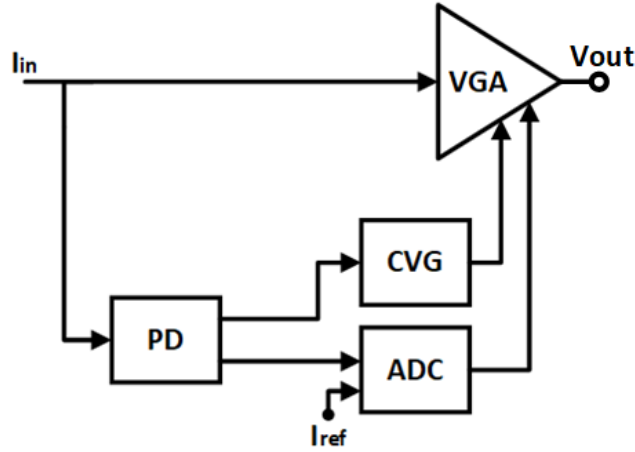


Figure 2.2 : Block diagram of the AGC in this thesis.

2.3.1 Variable-gain transimpedance amplifier

A circuit that linearly converts its input current to a voltage output is known as a transimpedance amplifier (R_T). The output voltage divided by the input current is the transimpedance gain. A higher R_T means a higher output voltage for a given input current [19]. However, as in other amplifiers, an increase in the gain leads to a decrease in bandwidth, resulting in intersymbol interference (ISI), which lowers the eye openings. Additionally, having more bandwidth than needed will increase the integrated noise and reduce the system sensitivity. The suggested optimum bandwidth for a TIA is 0.7 times the data rate [10].

Many domains incorporate TIA, including the following examples: radio frequency (RF) receivers, optical receivers, laser RADAR systems for distance estimation, and vision sensor chips [20]. Since the usage of TIAs has expanded, research in this area has also increased. There are two main categories of the TIA topologies: shunt-shunt feedback TIAs and open-loop TIAs. The regulated cascode and common-gate

methods are popular design techniques for configuring open-loop TIAs. The primary advantages of the regulated cascode TIA are less input impedance and reduced power consumption. The common-gate configuration reduces the effect of high input capacitance on bandwidth [21]. However, the noise performances of both methods are inferior to those of the shunt-shunt feedback TIAs. The bandwidth is also enhanced due to the fundamental principles of feedback. In summary, open-loop TIAs have different advantages; yet, shunt-shunt feedback TIAs often provide enhanced performance regarding bandwidth and noise reduction [19].

The basic idea in the shunt-shunt feedback TIAs is placing a resistor called R_F between the input and output terminals of an amplifier that has an open-loop gain of A_0 [10]. By using the properties of shunt-shunt negative feedback, the closed-loop input impedance can be written as

$$R_{in} = \frac{R_F}{1 + A_0} \quad (\Omega). \quad (2.2)$$

If it is assumed that $A_0 \gg 1$, the transimpedance gain can be expressed as

$$R_T = \frac{V_{out}}{I_{in}} = \frac{-A_0}{1 + A_0} R_F \approx -R_F \quad (\Omega). \quad (2.3)$$

A resistor converts the current into voltage based on Ohm's law: $V = I \cdot R$. Although a TIA and a simple resistor perform the same transimpedance gain, they differ significantly in their operation and performance characteristics. Both current-to-voltage converters are given in Fig. 2.3. The shunt-shunt feedback topology

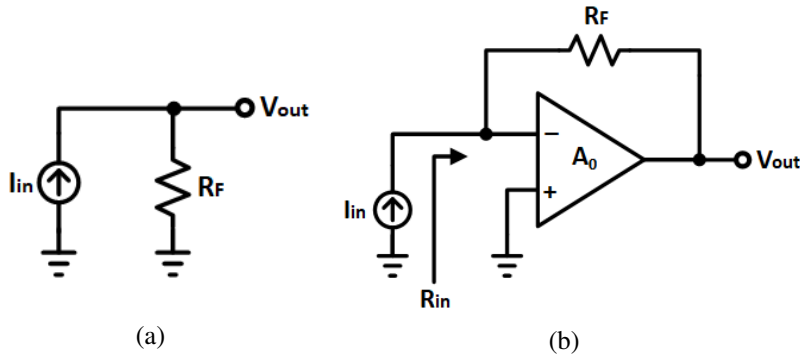


Figure 2.3 : Current-to-voltage converter models: (a) simple resistor and (b) shunt-shunt feedback TIA

in Fig. 2.3(b) reduces the input resistance and enhances the bandwidth. If the input capacitance is given as C_P , the input pole for the resistor model, which is depicted in Fig. 2.3(a), is $(R_F C_P)^{-1}$. Conversely, the input pole for the TIA is $[R_F C_P / (A_0 + 1)]^{-1}$. Moreover, if the large voltage swings are an issue for linearity, a TIA reduces them by a factor of $(A_0 + 1)$ [22].

Until now, the voltage amplifier within the shunt-shunt feedback mechanism has been considered an ideal amplifier. A more realistic circuit analysis should also be taken into account. Let us assume the ideal amplifier is a single-pole amplifier with a single stage. The time constant of the voltage amplifier is T_V [23]. The input capacitance C_{in} and the feedback resistor R_F form another pole. The input pole likely occurs at lower frequencies because the feedback resistor is large enough to ensure a sufficient transimpedance gain [20]. Hence, one can first write the open-loop transimpedance gain ($Z_{T,ol}$) as follows:

$$Z_{T,ol} = \frac{V_{out}}{I_{in}} = \frac{-A_0 R_F}{(1 + s R_F C_{in})(1 + s T_V)} \quad (2.4)$$

Next, the closed-loop gain ($Z_{T,cl}$) can be found through the feedback theory:

$$Z_{T,cl} = \frac{Z_{T,ol}}{1 - \frac{Z_{T,ol}}{R_F}} = \frac{-R_F}{1 + s/(Q\omega_0) + s^2/\omega_0^2} = \frac{A_0}{1 + A_0} R_F \cdot \frac{1}{1 + s/(Q\omega_0) + s^2/\omega_0^2} \quad (\Omega), \quad (2.5)$$

When the $s = 0$ in (2.5), the DC transimpedance gain converges to (2.3). Hence, the bandwidth of the amplifier does not affect the DC transimpedance gain. The angular frequency of the two poles ω_0 is expressed below [23].

$$\omega_0 = \sqrt{\frac{A_0 + 1}{R_F C_{in} T_V}} \quad (rad/s). \quad (2.6)$$

The Q factor in the first-degree term is the quality factor of the pole pair. The peaking in the AC response is controlled by the Q factor [20].

$$Q = \frac{\sqrt{(A_0 + 1) R_F C_{in} T_V}}{R_F C_{in} + T_V}. \quad (2.7)$$

The value of the quality factor affects the circuit behavior in both the transient and the frequency responses. A high Q implies underdamping, resulting in a frequency response with peaking and potential overshoot or ringing in the time domain. Conversely, a low Q implies overdamping, resulting in a slow response with reduced bandwidth. There are two well-known values for Q : $1/\sqrt{3}$ and $1/\sqrt{2}$. $1/\sqrt{3}$ is referred to as the Bessel response. Maximally flat group delay, no peaking in the amplitude response, and minimal overshoot are the primary characteristics of the Bessel response. Moreover, the $1/\sqrt{2}$ value for Q is represented as the Butterworth response. It aims for a larger peak in the group delay, a flat amplitude response, and more overshoot than the Bessel response. The selection depends on the application specifications. If the primary concerns are signal integrity, minimal distortion, and minimal ISI, then the Bessel response may be the more suitable choice. The Butterworth response provides a flat amplitude across a wider dynamic range [20]. More detailed analyses of a second-order TIA are given in [10] and [20].

When the A_0 , R_F , and C_{in} are held constant, selecting the Bessel response requires a voltage amplifier with 50% more bandwidth, according to [24]. The increase in bandwidth is accompanied by higher power consumption. The Butterworth response offers a practical compromise, effectively balancing performance with the amplifier bandwidth and power requirements. Therefore, the Butterworth response is selected. It ensures the gain flatness, moderate overshoot, and lower power consumption.

Before starting the design process, the criteria for the TIA should be clarified. Since the TIA will be implemented in a 1 Gbps PAM-4 communication system, each symbol carries 2 bits of information. The symbol rate is 500 Mbps. The optimum bandwidth for the TIA should be 0.7 times the symbol rate [10]. Therefore, the required bandwidth can be calculated as 350 MHz. Thus, its bandwidth must be sufficiently high to prevent limiting the overall system performance.

In conclusion, the bandwidth of the TIA criteria is set to 700 MHz. As stated above, the Butterworth response is chosen for an optimal trade-off between performance and power consumption. The Butterworth-type TIA permits moderate peaking in the amplitude response, so the peaking criterion is set at 1 dB. Furthermore, the dynamic

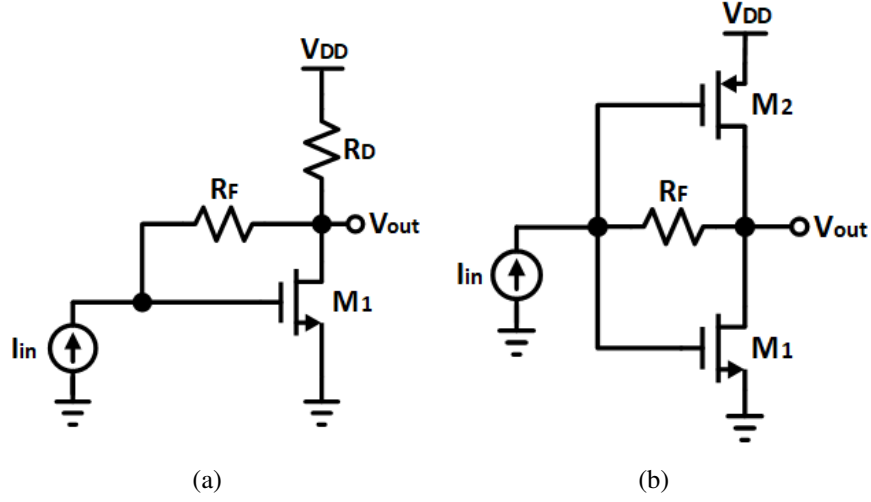


Figure 2.4 : (a) A single CS stage and (b) a CMOS inverter-based TIAs with resistive feedback.

range of the AGC, which is between $10 \mu A$ and $625 \mu A$, was discussed in Chapter 2.2. The TIA must operate linearly within this specified range, which requires meeting the 0.5 dB gain compression condition. The noise criterion is assigned based on the receiver response with the current buffer block. The designed current buffer dominates the overall noise performance of the system. When the noise limit at which the noise of the TIA begins to impact the system is analyzed, it is found that the integrated input-referred noise of the TIA should be less than 250 nA . Lastly, the open-loop gain of the TIA needs to be sufficiently high while maintaining moderate power consumption. Therefore, the power consumption limit is set to 1.5 mW .

Over the years, various TIA topologies have been developed. The simplest among them is the common-source (CS) stage with a feedback resistor, which serves as a TIA. However, in nanoscale process technologies, its open-loop gain is typically low due to the reduced intrinsic gain of CMOS transistors [19]. Additionally, the noise analysis of a typical shunt-shunt feedback TIA is a crucial aspect that requires careful consideration. There are two noise contributors in Fig. 2.3(b), namely the noise of R_F and the noise of the voltage amplifier $\overline{V_{n,amp}^2}$, both of which can be referred to the input node as follows:

$$\overline{I_{n,in}^2} = \frac{kT}{R_F} + \frac{\overline{V_{n,amp}^2}}{R_F^2} \quad (A^2/Hz). \quad (2.8)$$

When the R_T increases, the input-referred noise (IRN) decreases as expected. R_D and the input transistor M_I are the noise sources in $\overline{V_{n,amp}^2}$. Minimizing the noise of R_D is challenging due to the limited voltage drop across it [22]. Since inverter-based amplifiers can provide higher open-loop gain and better noise efficiency in modern CMOS technologies, a CMOS inverter-based amplifier can be used [25]. More precisely, using two MOSFETs doubles the input transconductance (g_m). For the CS-TIA, the output resistance is given by $r_o \parallel R_D$, whereas in the inverter-based TIA, it is $r_{o1} \parallel r_{o2}$. The voltage gain of the common-source (CS) stage is given by $g_m R_D$. Conversely, for the inverter-based stage with matched output resistances ($r_{o1} = r_{o2} = r_o$), the gain simplifies to $2g_m \cdot \frac{r_o}{2} = g_m r_o$. Since r_o is generally larger than R_D , the inverter-based amplifier offers higher gain than the CS stage. Another advantage of this topology is the elimination of an on-chip resistor in the layout, which saves area.

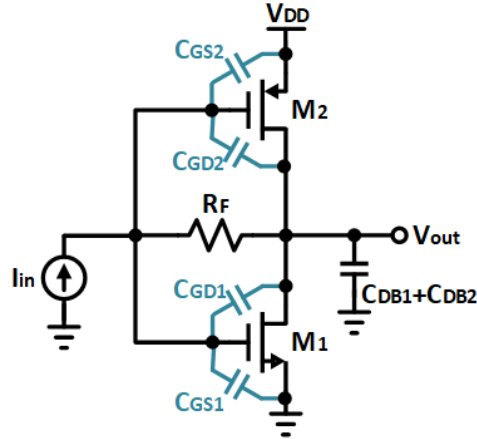


Figure 2.5 : Parasitic capacitances in an inverter-based TIA

These advantages come with several trade-offs: As discussed above, the sum of two V_{GS} equals V_{DD} , and the DC current of both transistors is equal. The relationship between I_{DS} and V_{GS} reveals that the performance of the topology is highly sensitive to process variations and biasing conditions. Moreover, both the output resistance of the inverter ($r_o/2$) and the total transconductance ($2g_m$) are dependent on process variations. To mitigate this issue, a replica-bias regulated power supply method can be used [26]. Furthermore, it is important to highlight that the input capacitance has increased compared to the CS-TIA. The parasitic capacitances of this topology

are shown in Fig. 2.5. By using the Miller Theorem, the C_{GD} capacitances may be separated. Thus, the total input capacitance is represented as

$$C_{in} = C_{GS1} + C_{GD1} \cdot (A_0 + 1) + C_{GS2} + C_{GD2} \cdot (A_0 + 1) \quad (F). \quad (2.9)$$

Being a two-pole system, the inverter requires a dominant pole for stability, typically at the input node due to its larger parasitic capacitance. A high open-loop gain naturally pushes the nondominant pole (output) far enough to ensure stability [20]. The exact pole location, however, depends on the capacitances of the preceding and succeeding circuits. After evaluating all trade-offs, a CMOS inverter with resistive feedback is selected as the optimal topology for the TIA in the AGC system.

The inverter-based TIA will be employed as a VGA. Therefore, its gain should be adjustable. When the open-loop gain is sufficiently high, the closed-loop transimpedance gain approximates the value of the shunt resistance R_F . The main idea is to switch the shunt resistance and change the R_T . Every parallel branch represents a coarse gain mode on the AGC system. The switch on-resistance (R_{on}) must be minimized to ensure the resistors dominate the gain setting on that branch. However, achieving low R_{on} requires large switch transistors, whose parasitic capacitances scale with device size. This situation yields another trade-off between R_{on} of the switches and the parasitic capacitances on the parallel branch. The fine gain adjustment is provided by a transistor that operates in the triode region. Each parallel branch combines three elements in series: a switch, a resistor, and a triode-region transistor. The R_{on} of a transistor operating in the triode region is given by,

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH} - V_{DS})} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \quad (\Omega). \quad (2.10)$$

The source and the drain DC voltages of the transistor are equal or nearly equal, and they are approximately $V_{DD}/2$. Hence, the V_{DS} term in (2.10) can be neglected. Since the gate voltage is easily adjustable, the on-resistance is primarily controlled through it. Firstly, the gate voltage range at which the transistor operates linearly is found via a DC sweep analysis. Next, the optimal transistor sizing is determined without introducing unnecessary parasitics. Adding the triode-region transistor to the

shunt feedback branch enables continuous gain adjustments. As the dominant pole of the TIA is selected as the input pole, the triode-region transistor, which brings extra parasitic capacitances, should be located near the input node. This placement ensures that the added parasitic capacitances are absorbed by the input pole. Otherwise, the nondominant output pole would approach the dominant pole, thereby increasing the Q factor and potentially leading to instability. Correspondingly, the resistance on the parallel branch is located near the output node.

The other crucial point is how the switches will be coded. Binary, Gray, and thermometric coding are digital encoding methods, each having different trade-offs. Binary coding is compact but prone to glitches because of the multiple bit changes at once. Gray coding changes only one bit at a time, reducing transition errors. However, the complexity is higher. These two methods can use all bit combinations in settings. Thermometric coding changes '0's to '1's in every step. For example, it uses the '00', '01', and '11' symbols. It does not assign anything to the '10' symbol. The method provides glitch-free operation; however, it does not utilize all possible bit combinations. The thermometric coding simplifies the ADC requirements in systems. The most suitable coding method varies depending on the specifications of the application. The proposed AGC utilizes triode-region transistors for gain adjustments, making thermometric coding a suitable choice. The complexity of the control voltage generation circuit and the ADC is significantly higher in the alternative methods.

Fig. 2.6 depicts the schematic of the VGA-TIA. It has six parallel feedback branches connecting the input and output of the inverter at DC. There are five switches to control. The switch transistors on the lowermost branch are permanently on, ensuring symmetry with the other levels. The highest gain setting is on that branch, and it amplifies the smallest signal levels. When the signal amplitude is within the second gain sector, the switches of the second branch are closed. The resistances of the two lowest branches then operate in parallel, effectively reducing the linear transimpedance gain by a factor of two. As the input signal level rises, the parallel branches are activated individually. The highest digital transimpedance mode is represented by '00000', while the lowest mode is indicated by '11111', since the DC levels of the input and output nodes are close to $V_{DD}/2$, transmission gate switches are employed.

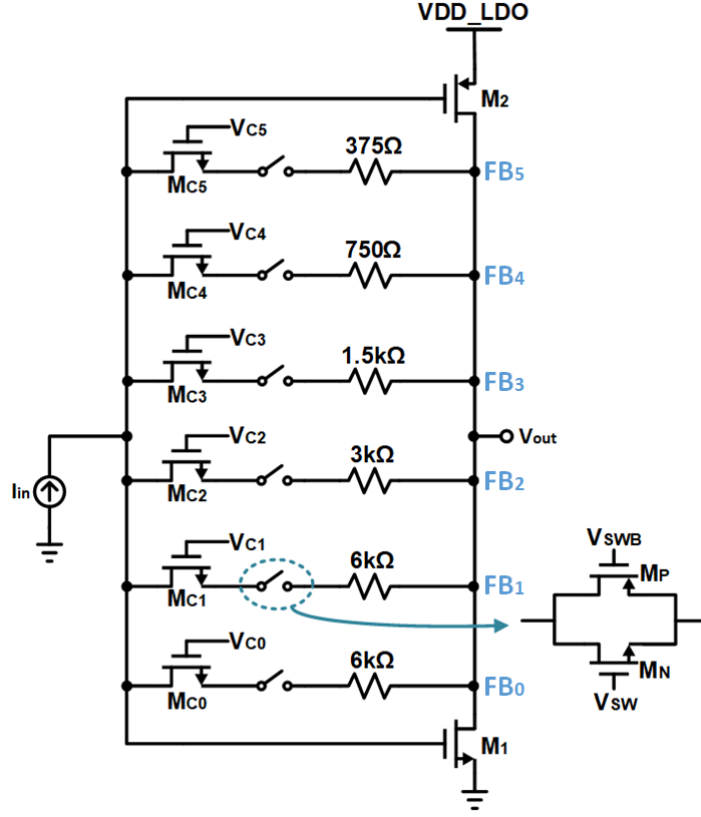


Figure 2.6 : Schematic of the VG-TIA.

Continuous gain adjustments are ensured by the control voltage V_C . There is a crucial relationship between the signal level and the gate voltage. As mentioned earlier, the aim is to match a low-amplitude signal with a high-gain setting while matching a high-amplitude signal with a low-gain setting. Within each gain sector, the gate voltage enables fine-tuning of the gain. When a low-amplitude signal is present, V_C is set low to achieve a high R_{on} , which results in a high transimpedance gain. As the signal amplitude increases but remains within the same gain setting, V_C is raised to reduce R_{on} , thereby lowering R_T .

Since the transistors used in the feedback branches must operate in the triode region, their gate-source voltage (V_{GS}) must exceed the threshold voltage (V_{th}). In a commercial 65 nm CMOS process, the core V_{DD} is 1.2 V, which places the input and output DC levels around 600 mV. With a typical V_{th} of about 300 mV, V_C should begin around 0.9 V to maintain the triode operation. The CVG circuit is responsible for generating the required gate control voltages.

The gain setting ranges are chosen to achieve the highest overall compression ratio across the whole range of input signals. There are six different gain modes, which are marked with coefficients of 0.5×, 1×, 2×, 4×, 8×, and 16×. These correspond to the increasing transimpedance gain. The ratio of the highest gain (16×) and the lowest gain (0.5×) provides a theoretical compression factor of 32 for digital control. The use of analog control also reduces the overall ratio. The lowest gain mode (0.5×) is for the highest input amplitude (625 μA), and the highest gain mode (16×) is for the lowest input current (10 μA). The boundaries between each digital gain mode are chosen to keep this compression ratio and ensure that the input dynamic range is evenly split across all the gain settings. Table 2.1 illustrates the relationship between the gain ranges and the input signal amplitudes. The thermometric coding bit settings are also given. Each $R_{on,i}$ represents the sum of the triode-region transistor resistance and the on-resistance of the corresponding switches. To maintain consistent relative contributions of $R_{on,i}$ to the total resistance in each branch, the ratio of it to the associated passive resistors is kept constant, which is accomplished by scaling their sizes proportionally: when the passive resistance is halved, the size ratio (W/L) of the MOS switches and triode devices is doubled. For instance, if the switches in the 6 k Ω branch have a size of W/L , then the switches in the 3 k Ω branch are sized at $2W/L$. This sizing strategy ensures that the relative impact of parasitic and switch resistances remains consistent across all gain stages.

Table 2.1 : Input Signal Ranges of the Gain Settings.

Coefficient	Bit Code	Transimpedance Gain	Input Amplitude (μA)
16×	00000	$6k + R_{on,0} = R_{T,0}$	10 – 16
8×	00001	$R_{T,0} \parallel (6k + R_{on,1}) = R_{T,1}$	16 – 30
4×	00011	$R_{T,1} \parallel (3k + R_{on,2}) = R_{T,2}$	30 – 62
2×	00111	$R_{T,2} \parallel (1.5k + R_{on,3}) = R_{T,3}$	62 – 124
1×	01111	$R_{T,3} \parallel (750 + R_{on,4}) = R_{T,4}$	124 – 276
0.5×	11111	$R_{T,4} \parallel (375 + R_{on,5}) = R_{T,5}$	276 – 625

There is another crucial point to emphasize: as the bit number increases, the size of the active devices is doubled at each step. As a result, their parasitic capacitances also increase significantly. Beyond a certain point, these parasitic loads begin to limit the bandwidth of the TIA. Reducing transistor sizes may help mitigate this and increase

bandwidth, but it comes at the expense of raising R_{on} values, which degrades linearity performance.

Moreover, the switch is placed between the triode-region transistor and the passive resistor, creating intermediate nodes. These nodes are loaded with parasitic capacitances, primarily gate-source (C_{GS}) and gate-drain (C_{GD}) components. The gate terminals are biased at fixed DC levels, which means they are grounded in the AC domain. A greater percentage of the signal is diverted to ground rather than following the intended feedback path as these capacitances increase. The increase in the capacitances reduces the feedback factor (β), increases the closed-loop gain, and consequently raises the quality factor of the circuit. As Q increases, the circuit nears instability. Consequently, the parallel branch number is set to 6 to cover the entire dynamic range with a high compression ratio, without limiting the bandwidth and excessively increasing the Q factor.

The simulation results and the layout considerations of the VG-TIA are discussed in Chapter 3.4.

2.3.2 Peak detector

High data rates are often supported by optical communication systems [27,28]. The desire for quick data transfer sets strict performance requirements on AGC circuits. The most important one is the settling time, which has a direct impact on bandwidth efficiency. An FF-AGC system is particularly useful in this situation. Since it is inherently faster than an FB-AGC, it has no stability issues. However, in FF-AGC systems, the peak detector is crucial as it handles the whole input dynamic range while also shaping the overall settling behavior of the AGC [9]. As a result, the development of a high-performance, quick-responding peak detector becomes vital. Furthermore, VLC imposes additional constraints. The system must adjust to varying distances between the transmitter and receiver, which increases the required dynamic range [29].

In the proposed hybrid-mode AGC system, the peak detector plays a crucial role in detecting the signal level and adjusting the gain. The current buffer circuit doubles the sensed current signal from the photodiode. Therefore, the same signal that goes to the

TIA is also received by the PD. Outputs of the PD drive both the digital Flash-ADC and the CVG circuit. The digital pathway manages coarse gain control via switching the parallel feedback branches, but the CVG facilitates precise, continuous tuning. The CVG circuit generates a voltage proportional to the amplitude. This configuration enables the peak detector to affect both control domains. Rapid reaction and precise peak tracking are essential for maintaining bandwidth efficiency and dynamic range in high-speed optical receivers. Therefore, a new peak detector topology is proposed in this thesis.

The fundamental principle of peak detector design is to provide a quick charging phase for the detecting capacitor (usually referred to as the attack time) while lowering the discharge rate (release time) to reduce droop. The capacitor is generally discharged through a low-bias current or a large resistor, a typical characteristic of class-A operation. While this method effectively reduces ripple, it results in a slower response time.

A common implementation utilizes a diode-capacitor combination, as shown in Fig. 2.7(a) [30]. It is simulated using an operational transconductance amplifier (OTA) followed by a class-A source follower. This OTA-based method achieves peak detection. But it is dependent on a high slew-rate OTA and is limited by the speed constraints of feedback-based topologies. An alternative approach involves examining open-loop circuit topologies, as illustrated in the block diagram of Fig. 2.7(b) [31]. This architecture converts the input voltage into current, requiring a current-input peak detector. It implements shunt feedback at the input to reduce the input impedance at low frequencies and uses current mirrors to duplicate the received signal at the output.

Still, this current-mode architecture has numerous inherent issues: The detection capacitor in the feedback loop reduces the gain at high frequencies. This gain reduction results in an increased input impedance, causing partial signal attenuation due to current division. As a result, the peak detector obtains a reduced portion of the received current. Secondly, as the input impedance increases, the voltage swing at the input node may become substantial. When the incoming signal amplitude is large, the transistors may exit the saturation region because of this phenomenon. Hence, it

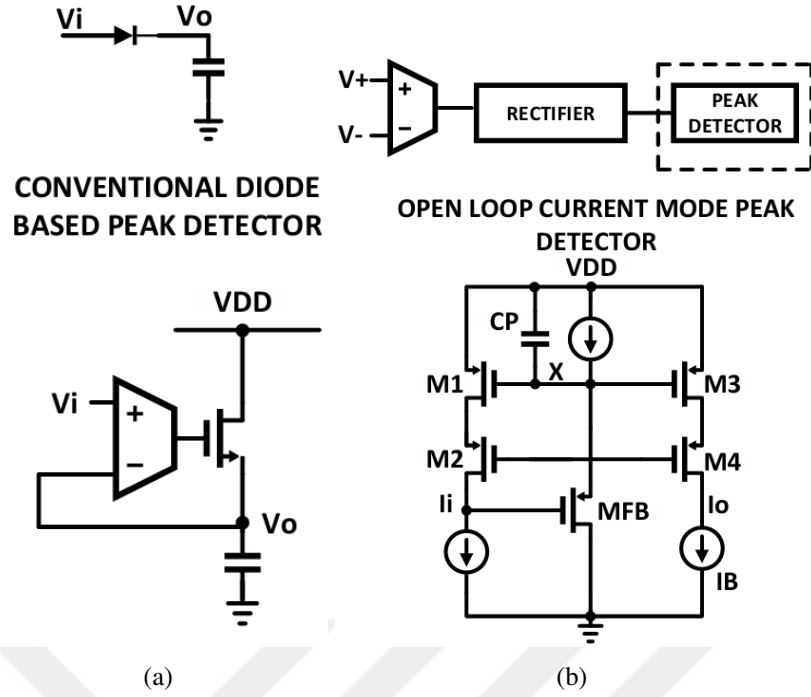


Figure 2.7 : (a) Conventional diode-capacitor peak detector and equivalent op-amp-source follower-based peak detector topologies (b) open-loop current-mode peak detector

brings nonlinear behavior. The nonlinearity reduces the detector dynamic range. The reduction of capacitance is a solution; however, in return, the ripple will increase. Consequently, there is a strong trade-off in this topology.

The issue is shown in Fig. 2.8. Z_{in} refers to the input impedance of the peak detector, and Z_{sig} indicates the output impedance of the signal path. The correlation between Z_{in} and Z_{sig} affects signal integrity. The loop gain can be analyzed via the feedback path. Node X is a high-impedance node because of two major factors: an intentionally low bias current and a large detecting capacitor. Although these design methods help reduce ripple during the release phase, they also cause a frequency-dependent characteristic. As the input signal frequency approaches the location of the open-loop pole, the feedback loop gain decreases. The drop in loop gain results in an increase in the input impedance of the peak detector. Consequently, a reduced current is directed into the PD, while an increased amount is diverted through Z_{sig} . Hence, the accuracy and the speed of the circuit degrade. The frequency-dependent impedance characteristic is a significant limitation in high-speed applications.

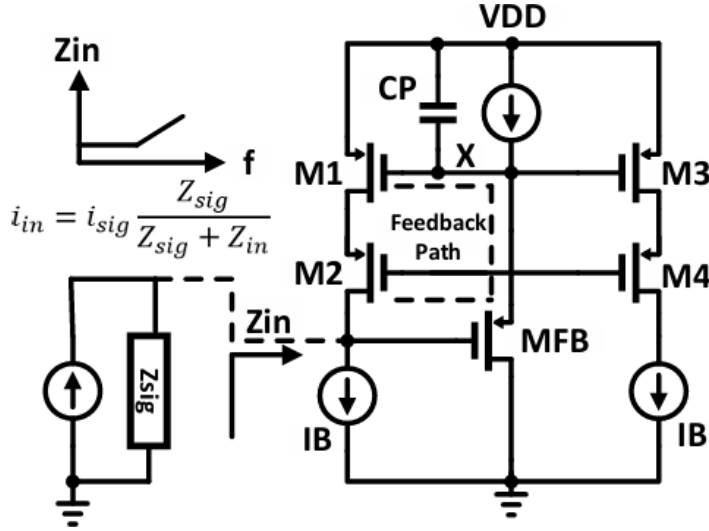


Figure 2.8 : Input impedance problem of the conventional current-mode PD.

In addition, the circuit in Fig. 2.8 suffers from active inductive behavior. This effect is due to the detection capacitor C_P being placed in the feedback path, and it forms a gyrator with transistors M_{FB} and M_1 . As a result, the input impedance increases with frequency, which is not desirable for current-input peak detectors. According to the gyrator method in [32], the input impedance is given by (2.11). It introduces a zero at $\omega_z = g_{m,FB}/C_P$, which is problematic for the circuit. Lowering the bias current helps reduce ripple, as it reduces $g_{m,FB}$. However, the reduction also shifts ω_z downward, thereby increasing the input impedance. The result contradicts the low-impedance requirement, limiting high-speed performance.

$$Z_{in,cl}(s) = \frac{Z_{in,ol}}{1 + \frac{\frac{1}{sC_P}}{\frac{1}{sC_P} + \frac{1}{g_{m,FB}}} \times g_{m,l} \times Z_{in,ol}} \simeq \frac{Z_{in,ol} \times \left(\frac{1}{sC_P} + \frac{1}{g_{m,FB}} \right)}{g_{m,l} \times Z_{in,ol} \times \frac{1}{sC_P}} = \frac{g_{m,FB} + sC_P}{g_{m,l} \cdot g_{m,FB}} \quad (\Omega). \quad (2.11)$$

By separating the input feedback loop from the detection capacitance, the proposed peak detector overcomes the gyrator issue. The offered circuit topology is derived from the preamplifier detailed in [33], where current-mode feedback lowers the input impedance and enhances the bandwidth. Fig. 2.9 illustrates that the cascode pairs M_1 and M_2 form a current-current feedback, while M_3 serves to amplify the error signal. The current gain from M_1 to M_3 is expressed as in (2.12), where A and B represent the mirroring ratios of M_1 to M_2 and M_1 to M_3 , respectively, $g_{m,l}$ stands

for the transconductance of M_I , and C_T indicates the total parasitic capacitance at the input node. The loop gain, equivalent to $1 + B$, provides gain reduction and bandwidth extension, as stated in (2.12). The input impedance of the designed circuit is detailed in (2.13), demonstrating that the circuit exhibits no inductive characteristics.

$$i_3(s) = i_{in} \cdot \left(\frac{A}{1+B} \right) \cdot \frac{1}{1 + \frac{sC_T}{g_{m,I}(1+B)}} \quad (A), \quad (2.12)$$

$$Z_{in, proposed}(s) = \frac{1}{(1+B)g_{m,I}} \cdot \frac{1}{1 + \frac{sC_T}{(1+B)g_{m,I}}} \quad (\Omega). \quad (2.13)$$

The detector includes two additional current mirror amplifiers. One is formed by M_4 and M_5 with mirroring ratio C , which uses C_{D1} as the detection capacitance. The second amplifier is formed by M_6 and M_7 with ratio D , and it utilizes C_{D2} . Those capacitances are used to suppress ripple. C_{D1} captures the high-speed current from M_3 , smoothing it into a near-DC level. Class-A behavior is achieved using I_3 , which contributes for the of M_3 and M_{3c} in addition to the diode-connected transistors M_4 and M_{4c} . When less current is flowing through the diode-connected transistors, their g_{ms} are decreased. Therefore, the equivalent impedance ($1/g_m$) is raised, and the ripple is suppressed. Moreover, M_5 amplifies the current-mode signal on M_4 . Since the bias current on M_4 is reduced, the total static power consumption will also be

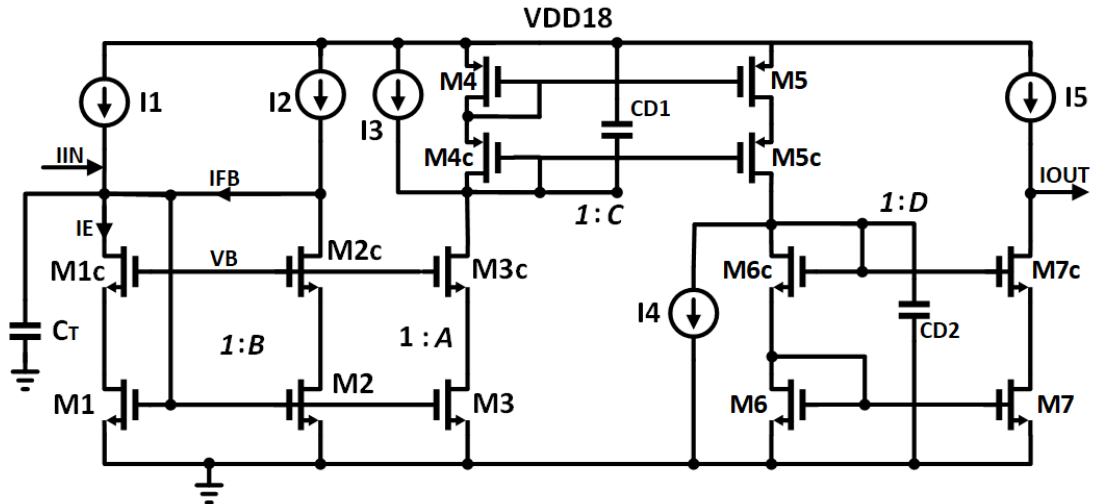


Figure 2.9 : Schematic of the proposed peak detector.

lower. Similarly, I_4 works with C_{D2} in the same spirit with I_3 , to provide further ripple suppression. This method is similar to the current bleeding technique in mixers. Furthermore, using separate detection capacitors shortens the release time. When the input signal drops, C_{D1} discharges through I_3 . A large C_{D1} would slow this process. By distributing the capacitance across different paths, the design achieves a balance between fast release time and acceptable ripple levels.

The total conversion gain is expressed in (2.14), where L denotes the loss caused by the limited bandwidth of the peak detector. If the signal frequency exceeds the detector bandwidth, L drops below 1. Assuming first-order low-pass behavior (6 dB/octave loss), L becomes 0.5 when the signal frequency is twice the bandwidth. This loss is acceptable as long as L remains sufficiently large and does not introduce distortion.

$$\text{Conversion Gain} = \left(\frac{A}{1+B} \right) \cdot C \cdot D \cdot L \quad (2.14)$$

Due to the use of basic current mirrors and negative feedback at the input, the circuit provides robust linearity and remarkable corner performance. As long as the W/L ratio of the transistors is large enough to handle high input currents, these advantages are maintained.

It is essential to note that, although a 1.8 V power supply is used to meet the AGC system requirements, the circuit is also compatible with lower voltage supplies due to the current mirrors that utilize wide-swing cascodes. Without cascode devices, the proposed circuit might even operate with a single supply of less than 1 V. However, in such a scenario, channel length modulation could lead to nonlinearity caused by signal-dependent mirroring errors, which would limit the circuit's application range to low-current signal detection only.

2.3.3 Analog-to-digital converter

The peak detector generates a current signal that represents the amplitude of the input, as previously mentioned. This current signal is routed into two separate paths: one for analog fine gain control via the CVG circuit and the other for digital coarse gain control. The digital path incorporates a current-mode Flash ADC. The block diagram

in Fig. 2.2 shows the relationship of these paths. The Flash-ADC forms the backbone of the gain quantization mechanism in this feedforward AGC architecture.

In this thesis, a Flash ADC topology is employed due to its simplicity, high speed, and suitability for near-DC signals. Since the input signal is already processed by the peak detector and displays low-frequency characteristics, the requirements of the ADC are comparatively liberal. Moreover, the coding of the TIA is chosen as thermometric to relax the criteria of the ADC. Therefore, the design focuses on robustness over high-resolution or high-speed operation.

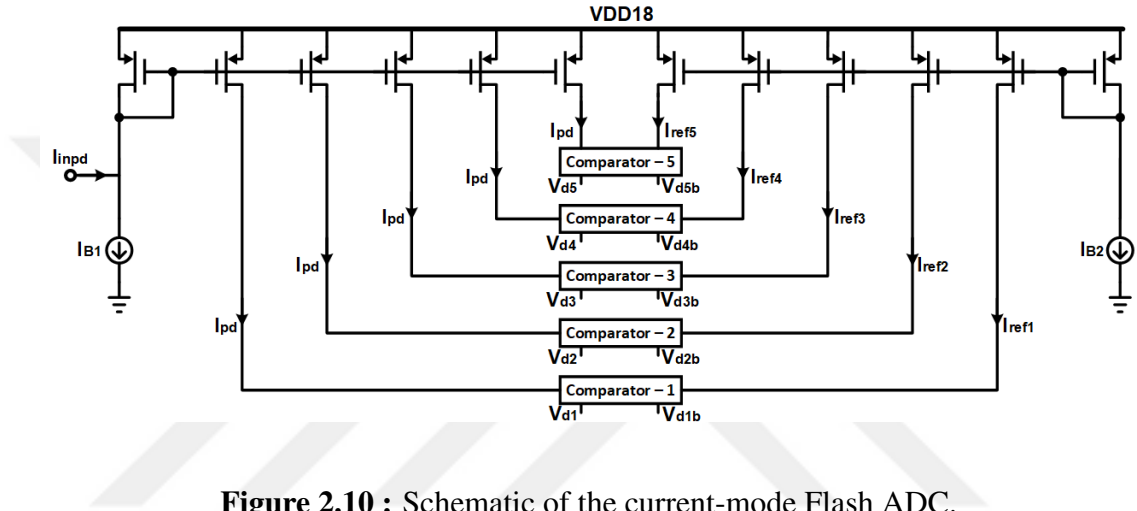


Figure 2.10 : Schematic of the current-mode Flash ADC.

The Flash ADC compares the output of the peak detector with a set of predefined reference currents, which formulate the basic operation of the circuit. The circuit schematic is shown in Fig. 2.10. The reference currents I_{B1} and I_{B2} are generated by a bandgap circuit, which ensures operation stability across the intended temperature range, process corners, and the supply voltages. The incoming signal from the PD and the references are multiplied by cascode current mirrors in the ADC. The cascode current mirrors are represented as single transistors in Fig. 2.10 for simplicity. They help ensure accurate current replication and minimize the effect of different V_{DS} values. Moreover, the comparators are designed to have current inputs and rail-to-rail voltage outputs. Fig. 2.11 provides the schematic of the comparator. M_{1A} and M_{1B} are sized larger than M_{2A} and M_{2B} . This method generates a small portion of hysteresis. It protects the ADC output from rapid and false changes in the input signal. In the decision mechanism, if the input current exceeds the reference current, the comparator

yields a logic high ("1"); otherwise, it provides a logic low ("0"). Since it is planned as a thermometer-coded circuit, there is no need to design a logic control circuit. This coding scheme eliminates glitches associated with binary encoding. The input signal and the reference are received by a latch topology in the comparator. Then, the comparison result is transmitted by the active loads. Afterward, two inverters are used to sharpen the edge of the comparator output.

Figure 2.11 : Schematic of the comparator.

The outputs of the Flash ADC are used to switch on or off the parallel gain-setting branches in the VG-TIA, enabling discrete gain steps. Each digital bit controls a specific switch in the transimpedance feedback network. When a higher signal amplitude is detected, more switches are turned on. This results in a reduction in the overall transimpedance gain, which prevents saturation. Conversely, for smaller signals, fewer switches are enabled, increasing the gain while preserving signal integrity. Hence, the variation of the output signal is intended to be smaller than that of the input signal.

The source and drain terminals of the triode transistors in the VG-TIA are biased near $V_{DD}/2$. Given that the threshold voltage (V_{TH}) of the NMOS transistors is approximately 300 mV, the control voltage (V_C) must reach around 0.9 V to keep the devices in the triode region. Therefore, V_C should start near 0.9 V for the lowest signal level within a given gain setting and gradually increase as the signal amplitude rises. However, as V_C increases further, R_{on} changes nonlinearly with V_C . To avoid this, the usable fine-tuning range of V_C is typically limited to about 200–300 mV. This baseline voltage is established through the gate-source voltage (V_{GS}) of a diode-connected NMOS transistor. Even in the absence of a PD output signal, a constant bias current (I_B) flows through a current mirror and into the diode-connected device. This procedure ensures that the transistor remains active and maintains a stable, nonzero V_{GS} , thereby setting the minimum value of V_C required for the triode-mode operation. By regarding these voltage and linear operation constraints, the CVG circuit is designed. The schematic of the proposed circuit is given in Fig. 2.12.

The CVG takes the extracted current-mode amplitude data from the PD and amplifies it through cascode current mirrors. The circuit employs a simple yet effective topology consisting of a diode-connected NMOS transistor in series with a resistor. Each branch generates a unique V_C value, which is connected to the related triode-mode transistors. When the input current increases, more current is multiplied by the current mirrors. Then, the voltage drop across a resistor (R_i) on one branch also increases.

Additionally, V_{GS} of the diode-connected transistor, which is placed in each branch, increases due to its nonlinear dependence on current. As a result, the output control voltage V_C increases proportionally to the input signal amplitude. The expression for V_C is given as

$$V_C = V_{GS,D} + I_R \cdot R = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}}} + I_R \cdot R \quad (V). \quad (2.15)$$

In 2.15, the square root term and V_{TH} represent the relationship between V_{GS} and the drain current I_D , assuming saturation operation for the diode-connected device. The final term, $I_R \cdot R$, represents the voltage drop across the resistor, contributing a linear scaling component. Most of the adjustment in V_C is achieved via this resistive drop.

Increasing the current flow through resistors allows for a reduction in resistor size, which is beneficial for minimizing area usage. The rise in diode-connected transistor current poses challenges in achieving the minimum V_C within the range. Therefore, additional current sources that are feeding the resistors are included in the design. The arrangement minimizes the resistor value while ensuring the desired voltage swing, range, and minimal area usage.

The resulting V_C voltages are connected to the gates of triode-region transistors in the VG-TIA feedback network. These voltages provide continuous fine gain tuning within each coarse gain step. While multiple branches may be operating simultaneously due to thermometer coding, the dominant V_C adjustment is made by the branch that is most recently activated. The control transistors in the former activated branches enter the saturation region; hence, their R_{on} is low and nearly constant. In low-gain scenarios, where the signal amplitude is high and many branches are active in parallel, the magnitude of V_C becomes the dominant factor in controlling the effective transimpedance gain of the amplifier.

In conclusion, the CVG circuit enables precise, fast, and continuous analog gain control based only on the PD output. It requires no additional input or feedback loops and operates entirely in the DC domain, which contributes to its speed and robustness. The CVG works in collaboration with the Flash ADC. The hybrid method reduces output signal variation, allowing the AGC system to maintain a high compression ratio and a wide dynamic range with low distortion and fast settling behavior.

2.3.5 The proposed AGC system

The proposed AGC system is designed for optical front-ends. It features a feedforward architecture, enabling rapid response and improved bandwidth efficiency. Optical systems such as POF and VLC typically involve large-area photodetectors, which introduce significant parasitic input capacitance, often in the range of tens of picofarads. Furthermore, the noise performance falls as the input capacitance increases. To address this, the input stage can be designed as a simple common-gate buffer. Although it is presented as a straightforward concept in the thesis, it is typically

a highly sophisticated circuit designed to provide the necessary bandwidth and noise performance.

The schematic of the proposed system is given in Fig. 2.13. The red rectangle highlights the range of this thesis, and the blue rectangles depict each circuit. The output of the current mirror is duplicated: one copy proceeds through the signal path toward the VG-TIA, and the other is routed to a wide dynamic-range peak detector. The peak detector generates a DC current proportional to the amplitude of the input signal. The DC signal in PD is multiplied by cascode current mirrors and then used by both a digital and an analog controller. The digital path sets coarse gain levels, while the analog path provides continuous fine adjustment within each digital gain sector. The primary benefit of the hybrid method is improving the gain compression ratio. Another benefit is that the transitions between gain settings are smoother than the digital gain control.

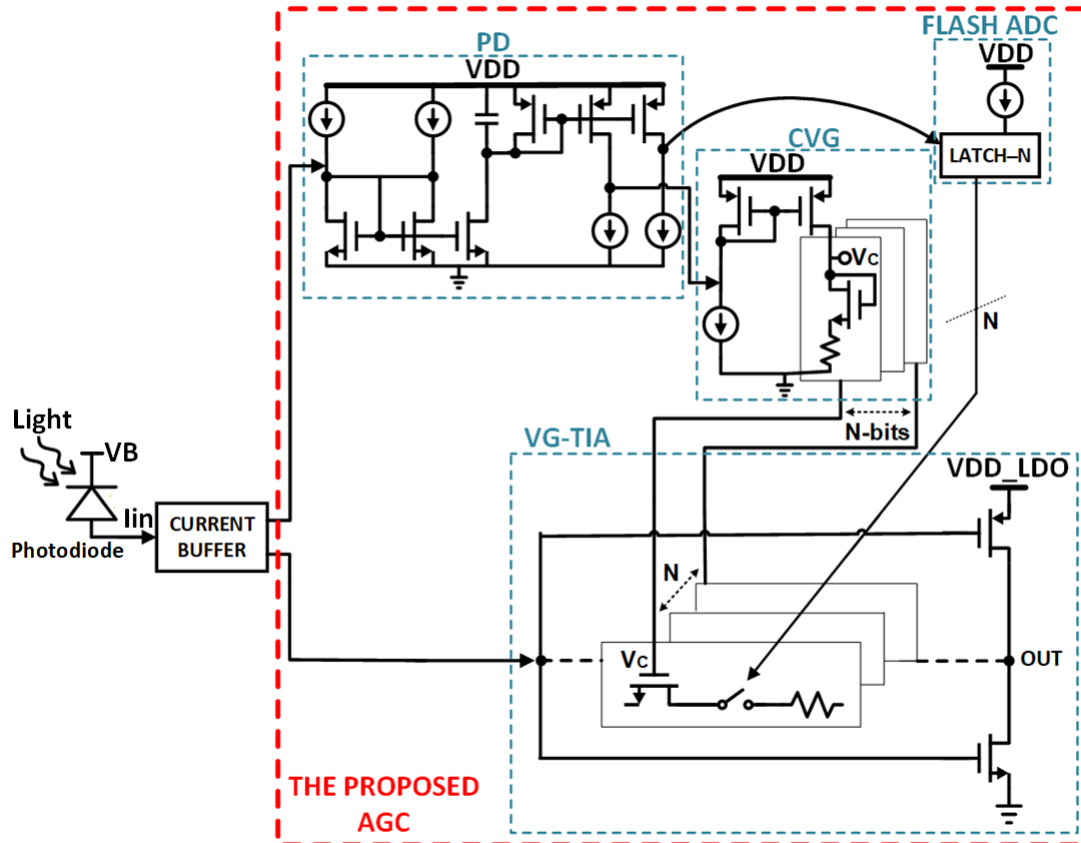


Figure 2.13 : Schematic of the proposed AGC system.

The signal path consists of a CMOS inverter-based variable-gain TIA, powered by a replica bias reference low-dropout regulator (LDO). The LDO enhances the robustness of the TIA across process, voltage, and temperature (PVT) variations. The VG-TIA feedback network includes multiple branches composed of passive resistors, switches, and triode-region NMOS transistors. The digital controller is designed as a Flash ADC. It controls the switches that form the transmission gates on the feedback branches. The ADC selectively enables parallel feedback paths based on the output of the peak detector. Simultaneously, the analog controller sets the gate voltage of the triode transistors, tuning their R_{on} to achieve fine gain control.

The peak detector circuit is a key innovation in the system design. Feedforward AGCs demand wide dynamic-range detection, but the literature on suitable peak detector designs remains limited. The proposed PD separates the feedback path and the detection capacitor paths. By using this method, the input impedance becomes insensitive to frequency. The proposed peak detector delivers a highly linear current output across a broad input amplitude range. The DC current it generates is duplicated and sent to two distinct destinations: latches used for the Flash ADC operation and the control voltage generator circuit for the analog tuning.

The current-mode Flash ADC portion is designed for speed and low complexity. The peak detector output current is compared with the reference currents in the latches. These latches are traditional cross-coupled structures with built-in hysteresis to prevent false triggering. The latch outputs drive the transmission gate switches in the VG-TIA in a thermometer-coded fashion. As the amplitude of the input signal increases, the output amplitude of the PD increases, resulting in a higher number of latches producing a logic '1' output. It enables additional feedback branches in the VG-TIA, reducing the total feedback resistance and therefore lowering the transimpedance gain. Conversely, for low signal amplitudes, fewer feedback branches are activated, resulting in a higher transimpedance gain.

The hybrid AGC architecture presents numerous benefits. The feedforward topology eliminates stability issues associated with the feedback loops and provides sub-microsecond attack and release times. The hybrid control approach enhances

resolution and compression ratio, offering roughly 30 dB of gain adjustment across an input range of 10 μA to 625 μA . Furthermore, the CMOS inverter-based transimpedance amplifier preserves linearity, and the implementation of thermometric coding guarantees glitch-free operation. Moreover, the peak detector offers a low input impedance, fast attack and release times, and linear operation over a very wide dynamic range.

Despite these advantages, the design has some difficulties. The lack of a feedback loop brings stringent requirements on the linearity of each circuit. Moreover, careful transistor sizing is crucial for controlling parasitic capacitances, particularly within the VG-TIA feedback network. The integration of digital and analog control requires precise coordination to minimize discontinuities in gain behavior. The designer should consider these effects and understand the trade-offs during the design and layout processes.

The suggested AGC system incorporates a high-speed feedforward architecture with a robust hybrid gain control mechanism, offering reliable and low-latency performance across a wide dynamic range. It is optimal for next-generation optical front-ends, where bandwidth, compression performance, and circuit robustness are crucial. The design properties and the specifications are summarized in Table 2.2. By using the simulations, the specifications are verified. The next chapter presents simulation results under various operating conditions, along with the accompanying layout considerations.

Table 2.2 : Design Criteria of the AGC System.

Design Property	Specification
Modulation Type	PAM-4
Data Rate	1 Gbps
Estimated Input Current	10 μA – 625 μA
Output Peak-to-Peak Amplitude Variation	< 6 dB
Compression Ratio	> 30 dB
TIA –3 dB Bandwidth	> 500 MHz
IIRN	< 300 nA
Settling Time	< 1 μs
Linearity	1-dB compression test and the eye height symmetry should be satisfied.

3. LAYOUT AND SIMULATION RESULTS

This chapter presents the schematic-level and post-layout simulation results of the proposed AGC system and its sub-blocks. Each subsection includes performance verification under typical operating conditions. Layout considerations for each circuit, along with the layout images, are also included. Additionally, process corner and Monte Carlo simulations are conducted to ensure the system performance under various conditions. The goal is to validate the circuit behavior and confirm compliance with design specifications. Lastly, a comparison with the systems in the literature is provided to highlight the advantages and contributions of the proposed architecture.

The hybrid AGC system dynamically adjusts the gain of the VG-TIA. As a result, the simulations of the AGC and VG-TIA are closely interrelated and should be presented jointly. Therefore, the performance verifications of the VG-TIA are included in Section 3.4.

3.1 Peak Detector Simulations

This section explains the robustness and essential performance metrics of the proposed peak detector, covering the input impedance, linearity, dynamic range, conversion gain, bandwidth, and the attack-release time. The layout of the proposed PD is illustrated in Fig. 3.1, demonstrating a chip area of $190\ \mu\text{m} \times 90\ \mu\text{m}$, which includes the on-chip detection MOM capacitors. The mirrors are protected by dummy devices at the outer edges to reduce the n-well edge effect. The PMOS and NMOS regions are separated by an n-well guard ring and a p-sub guard ring to reduce the potential of latch-up issues. Active devices occupy the most chip estate due to their notable lengths and widths, which in turn minimize random mismatch.

In the cascode unit, all NMOS devices have dimensions of $W_N = 48\ \mu\text{m}$ and $L_N = 1\ \mu\text{m}$, whereas the PMOS devices have sizes of $W_P = 64\ \mu\text{m}$ and $L_P = 1\ \mu\text{m}$. The current mirror ratios are obtained by multiplying the unit devices. The parameters for

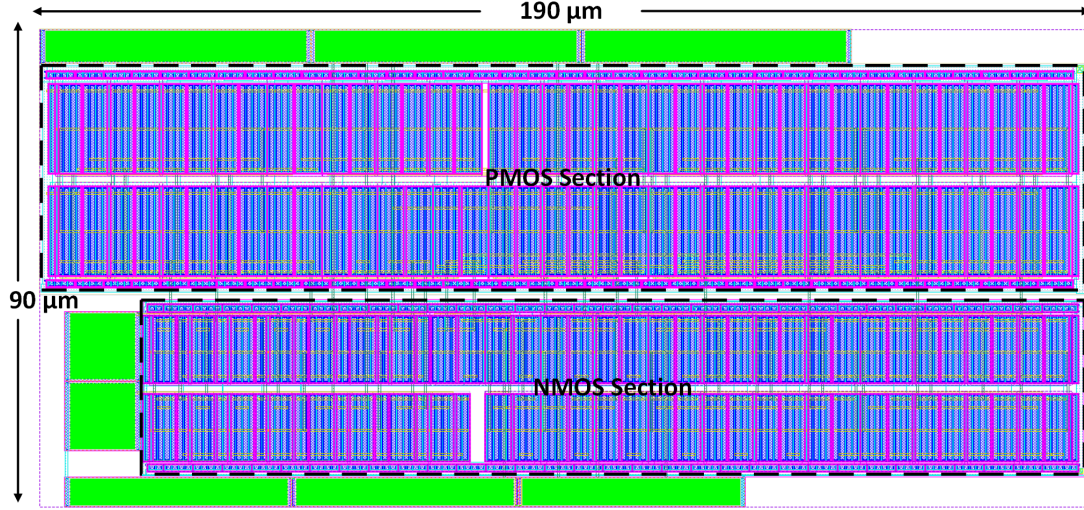


Figure 3.1 : The layout of the proposed PD.

the mirror design, indicated as A , B , C , and D in 2.14, are assigned the values of 4, 8, 2, and 2, respectively. This selection gives a conversion gain of approximately 1.8 (5 dB), excluding L , the loss parameter associated with the bandwidth. The conversion gain characteristic is given in Fig. 3.2, which shows a theoretical gain of 5 dB at the low frequencies. In Fig. 3.2 and Fig. 3.3, the red line represents the schematic simulation, and the blue line is for the LPE simulation. The detection capacitances are both selected as 1 pF. The static current drawn by the circuit is $300 \mu\text{A}$, resulting in a static power consumption of $540 \mu\text{W}$. The peak detector is simulated with a 250 MHz pulse input, which is sufficient to support 1 Gbps PAM-4 modulation. Simulations of

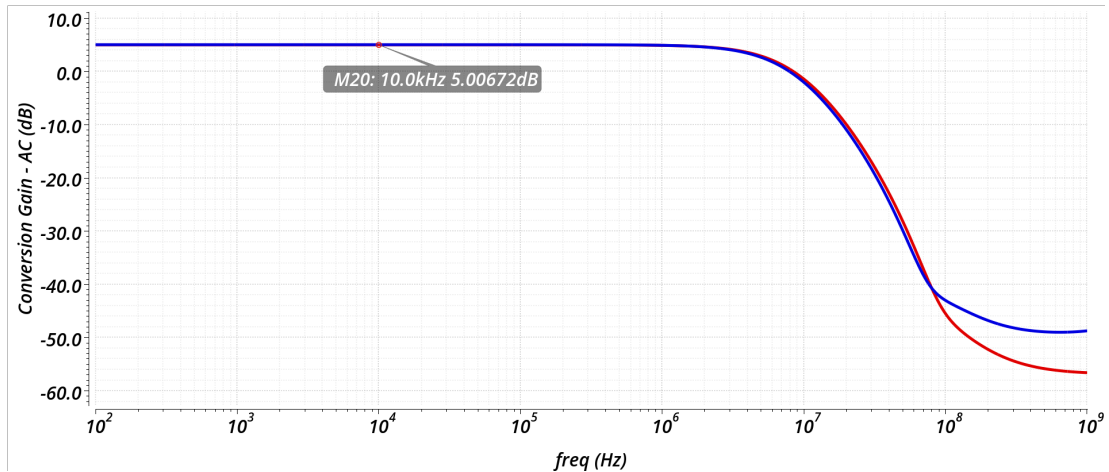


Figure 3.2 : Conversion gain of the PD.

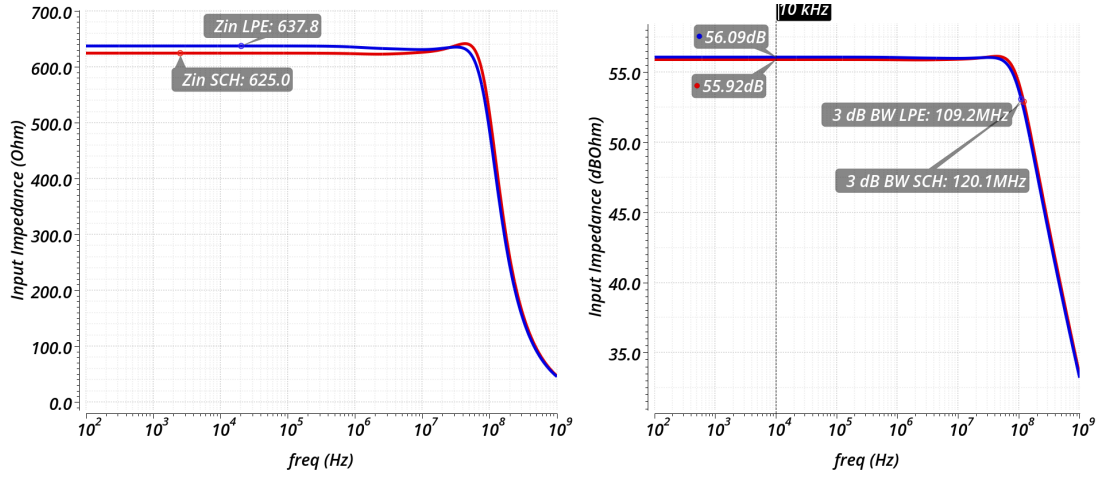


Figure 3.3 : Input impedance of the PD.

the peak detector are conducted at both the schematic level (SCH) and the following layout parasitic extraction (LPE). Additionally, Fig. 3.3 illustrates the input impedance plot. The input impedance at low frequencies is approximately 56 dBΩ (630 Ω). It exhibits a low-pass characteristic, indicating that the gyrator issue has been resolved. The conversion gain plot in Fig. 3.2 does not provide information regarding the bandwidth and high-frequency conversion gain, as the detection capacitors reduce the high-frequency content of the data. Thus, the input impedance should be used for the bandwidth of the circuit. According to Fig. 3.3, the -3 -dB bandwidth is close to 110 MHz. Moreover, the input impedance is found as 637.8 Ω in the post-layout simulation.

The transient response provides the most accurate simulation data about the high-frequency conversion gain. A 250 MHz non-return-to-zero (NRZ) signal is applied to the input for this purpose. Fig. 3.4 demonstrates the LPE attack performance for various amplitudes. The input pulse amplitudes are given as 10 μ A, 50 μ A, 100 μ A, 200 μ A, 300 μ A, 400 μ A, 500 μ A, and 600 μ A. For all amplitude levels, the attack time remains below 90 ns with a 1% settling error criterion.

Furthermore, the results of the schematic and post-layout simulations are in good agreement. It is also observed that the ripple amplitude increases with higher input levels. This observation is related to the full charging of the detection capacitors at large signal amplitudes. As a result, minor voltage ripples become unavoidable.

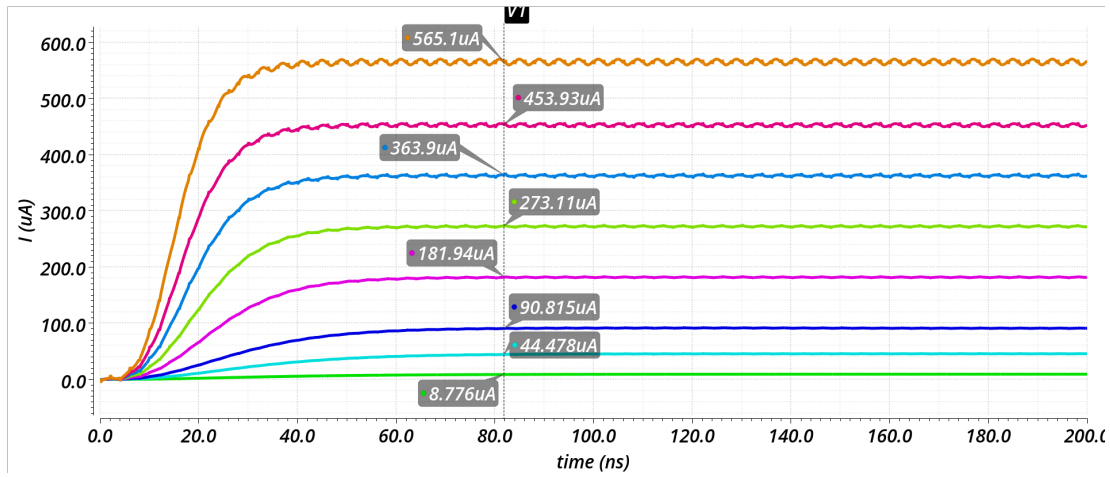


Figure 3.4 : Attack and settling behavior for various input amplitudes.

Although the ripple magnitude can be reduced, it usually comes at the cost of slower response. This situation highlights a fundamental trade-off between the settling performance and ripple suppression.

In addition, the input amplitude at 250 MHz is swept from 10 μA to 6 mA to find the transfer characteristic in transient analysis. After the settling is completed, averages of the output transient signal are calculated, where it is seen that the averaging approach effectively suppresses the ripple components, as shown in Fig. 3.5.

Moreover, the transient conversion gain is analyzed in Fig. 3.6. The gain remains around 0.9, corresponding to approximately -0.8 dB, due to the bandwidth loss (with

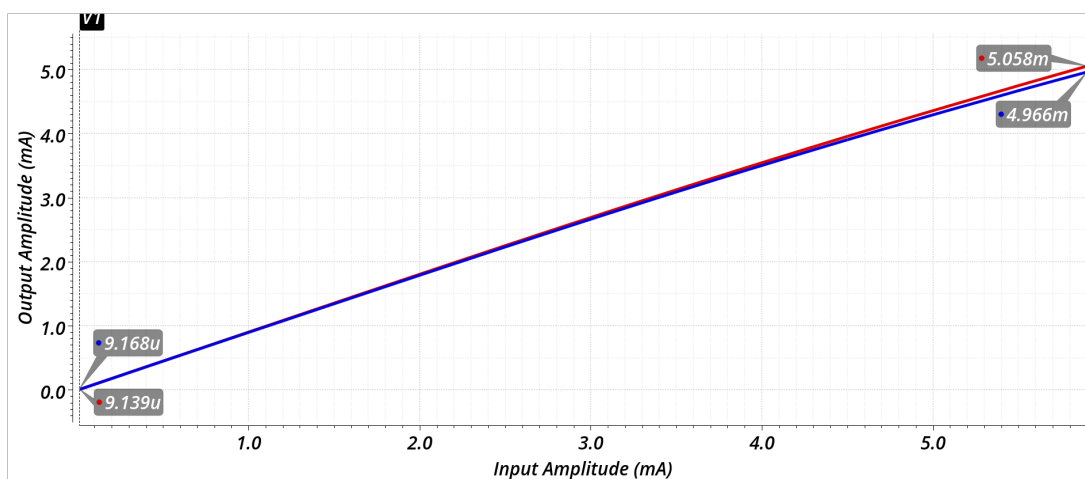


Figure 3.5 : The output current with respect to the input amplitude.

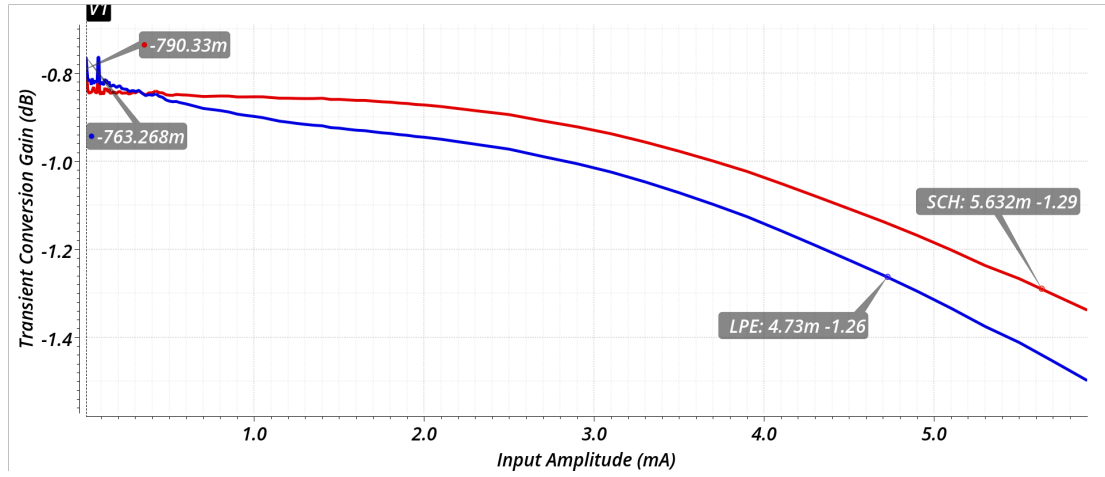


Figure 3.6 : Transient transfer characteristic of the PD.

a loss factor of $L \simeq 0.5$). A similar factor can also be observed in Fig. 3.5, especially in the slope of both lines.

Post-layout simulations in Fig. 3.7 reveal a compression of about 0.5 dB at an input current of 4.7 mA, indicating strong linearity and superior performance across a very wide dynamic range. Within the AGC target range of $10 \mu\text{A}$ to $625 \mu\text{A}$, the transient conversion gain of the peak detector remains nearly constant.

Fig. 3.7 presents the combined attack and release response of the peak detector in a single plot. In this simulation, the input signal amplitude is initially increased from $10 \mu\text{A}$ to $625 \mu\text{A}$ and then reduced to $100 \mu\text{A}$ to evaluate large transitions across the

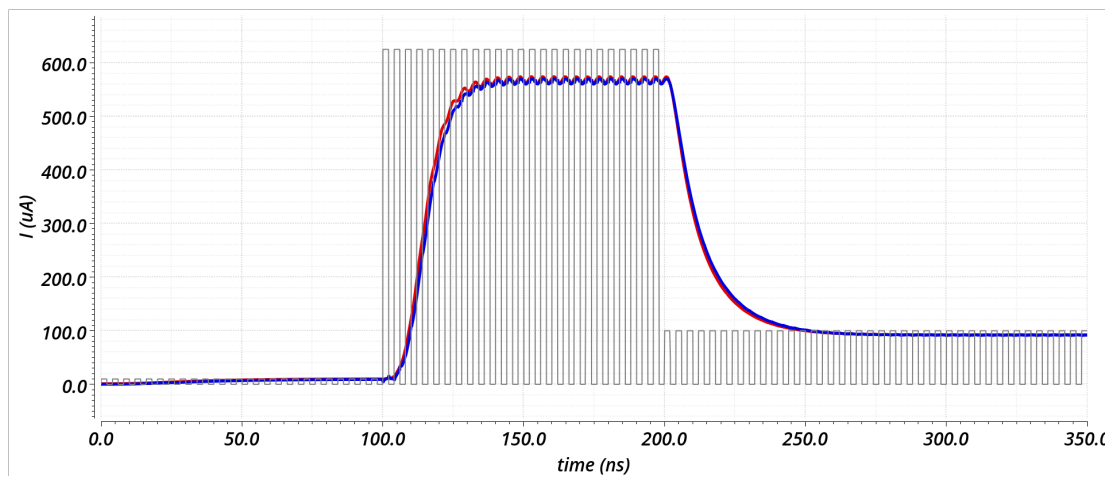


Figure 3.7 : Attack and release behavior in the transient domain.

operational range of the AGC. The schematic simulation result (red line) shows a faster response compared to the LPE result (blue line). It is primarily due to the additional parasitic capacitances introduced after the layout extraction. The simulation indicates that the attack time is slightly shorter than the release time, with both measured at approximately 50 ns. For an input amplitude of $625\ \mu\text{A}$, the ripple on the output current is around $10\ \mu\text{A}$.

Figure 3.8 illustrates the transient output noise, approximately $1\ \mu\text{A}$ (pp), for both the schematic-level and post-layout simulations. This value is crucial, as the random noise specifies the smallest signal that can be processed with a certain gain error constraint. Furthermore, the calibration of the random noise is quite challenging. Nonetheless, a final low-pass filter at the output can be used to further reduce noise and ripple, ensuring accurate operation.

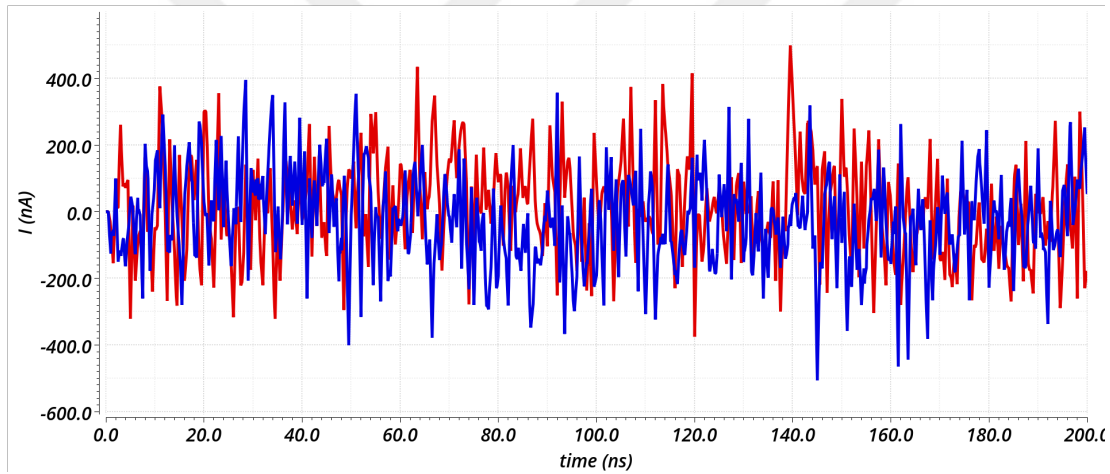


Figure 3.8 : Output current transient noise

3.2 Analog-to-Digital Converter Simulations

The layout of the Flash ADC is shown in Fig. 3.9. The area of the layout is $175\ \mu\text{m} \times 235\ \mu\text{m}$. The layout centers the comparators and reserves the left and right sides for the current mirrors. In the AGC system layout, the peak detector is located to the left of the ADC; hence, the current mirrors responsible for duplicating its output signal are placed on the left side. On the right side, current mirrors are used to generate the necessary reference currents from the current reference provided by the

BGR. Furthermore, dummy transistors are incorporated into the scheme to minimize shallow trench isolation (STI) and well proximity effects.

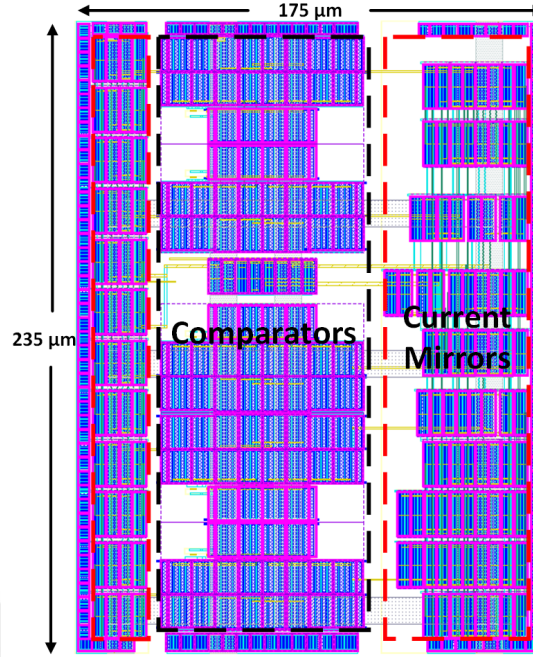


Figure 3.9 : Layout of the flash ADC

The PMOS current mirrors in the Flash ADC are sized as $W_P = 64 \mu\text{m}$ and $L_P = 1 \mu\text{m}$. To improve the output impedance and the accuracy, the current mirrors are designed using a cascode topology. Additionally, the transistor dimensions used in each comparator are listed in Table 3.1.

Table 3.1 : Transistor Sizes in the Comparator.

Transistor Name	$W (\mu\text{m})$	$L (\mu\text{m})$
M_{1A} and M_{1B}	$12.6 \cdot 8 = 100.8$	2
M_{2A} and M_{2B}	$12 \cdot 8 = 96$	2
M_{3A} and M_{3B}	$12 \cdot 16 = 192$	2
M_4 and M_5	$12 \cdot 8 = 96$	2

The DC sweep with the hysteresis response of the Flash ADC is presented in Fig. 3.10. A DC input current is swept from $1 \mu\text{A}$ to $625 \mu\text{A}$ and then back down to $1 \mu\text{A}$. As described in Section 2.3.3, the hysteresis is intentionally added to prevent spurious and rapid switching of the digital control output due to small input fluctuations. Since all comparators share identical circuit design and layout, the magnitude of the hysteresis increases with larger input amplitudes.

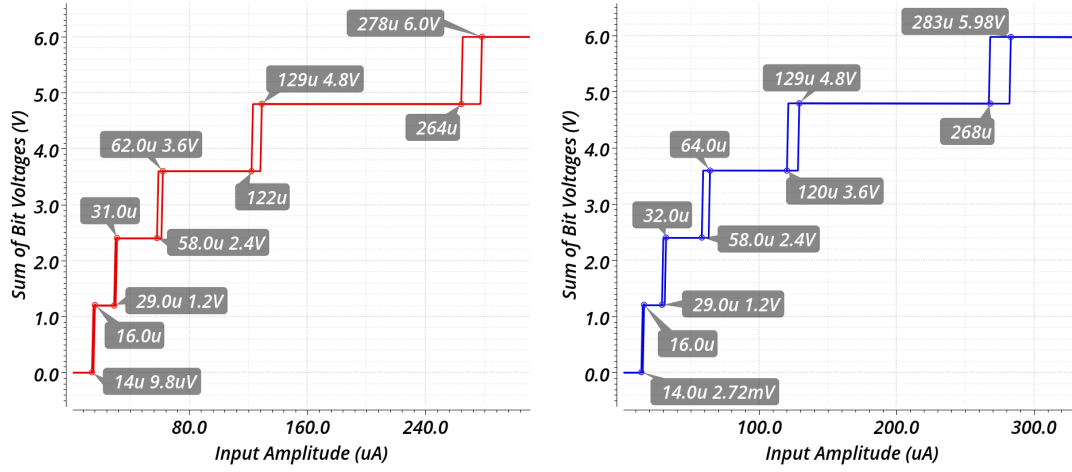


Figure 3.10 : DC sweep with the hysteresis.

Fig. 3.10 illustrates the total output voltage, which is the sum of all comparator outputs. When all comparators are off, the total output is 0 V. As comparators turn on successively, following a thermometric code pattern, the output increases stepwise. For instance, an output of 1.2 V corresponds to the activation of the second gain sector. The left plot in Fig. 3.10 shows the schematic-level simulation results, while the right plot presents the post-layout simulation outcomes. The two align closely, with the post-layout hysteresis slightly wider due to parasitic effects. Additionally, the static power consumption of the circuit is 2.23 mW due to the heavy use of current mirrors.

3.3 Control Voltage Generation Circuit Simulations

The control voltage generation circuit converts the input current into analog control voltages that define the fine gain adjustment for the VG-TIA. It consists of current mirrors, diode-connected NMOS transistors, and resistors. The circuit schematic is presented in Fig. 2.12, and the theoretical operation was previously discussed in Subsection 2.3.4. Large transistor-sized cascode current mirrors are utilized in the design to ensure precise current matching across multiple branches. This approach reduces mismatch and improves linearity. The supply voltage is set to 1.8 V, and the total static power dissipation of the CVG is 0.7 mW. The (W/L) notation in Fig. 2.12 is chosen as $64 \mu\text{m}/1 \mu\text{m}$ in the design. Moreover, the sizes of the diode-connected transistors and resistors are listed in Table 3.2.

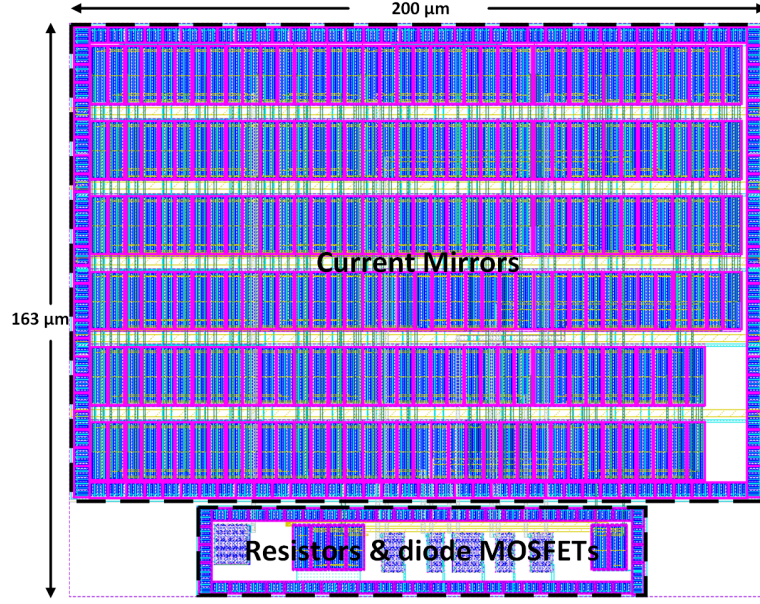


Figure 3.11 : Layout of the CVG circuit.

The layout of the CVG circuit is shown in Fig. 3.11. The total layout area is $200 \mu\text{m} \times 163 \mu\text{m}$. The majority of the area is occupied by the current mirrors, highlighting their importance in the design. To obtain a higher V_{GS} and ensure a proper output voltage range, the W/L ratios of the diode-connected transistors are kept small. Dummy transistors are added at the layout boundaries to mitigate the edge and STI effects.

Fig. 3.12 shows the voltage outputs during the DC sweep over the full input current range. The colors and corresponding signal names are indicated on the left. Each control voltage rises in its respective active region and saturates at 1.8 V. The linear portion defines its effective control voltage range. After the associated gain setting is established, the control voltage saturates and R_{on} remains nearly constant. In the next gain stage, the triode transistor in the newly activated branch dominates the gain

Table 3.2 : Device Sizes of the Proposed CVG.

Transistor Name	$W (\mu\text{m})$	$L (\text{nm})$	Resistor Name	Resistance ($k\Omega$)
M_{D0}	2.4	120	R_0	16
M_{D1}	2	120	R_1	9.9
M_{D2}	2.7	120	R_2	10
M_{D3}	3.1	120	R_3	8
M_{D4}	1.2	120	R_4	7
M_{D5}	1.5	120	R_5	13.5

adjustment. This behavior simplifies the calculations, as each gain setting is controlled by a distinct transistor in the triode region.

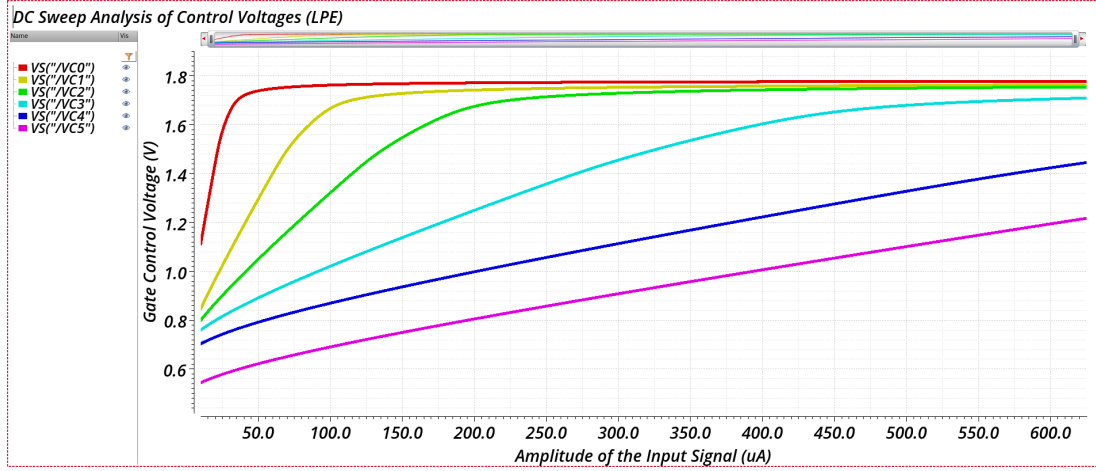


Figure 3.12 : Generated control voltages in the whole input range – DC sweep.

To focus on the relevant operating points, a clipped version of this plot is provided in Fig. 3.13. It displays only the active range for each V_C signal. For instance, V_{C0} is active between $10 \mu\text{A}$ and $15.5 \mu\text{A}$. The transimpedance gain in the first sector is determined by the first feedback branch, as there are no other feedback paths parallel to it. Therefore, R_{on} of M_{C0} highly affects the gain. Thus, V_{C0} is higher and exhibits less fluctuation compared to the other control voltages. In addition, the output voltage boundaries in Fig. 3.13 are selected around the midpoint of the ADC hysteresis regions shown in Fig. 3.10.

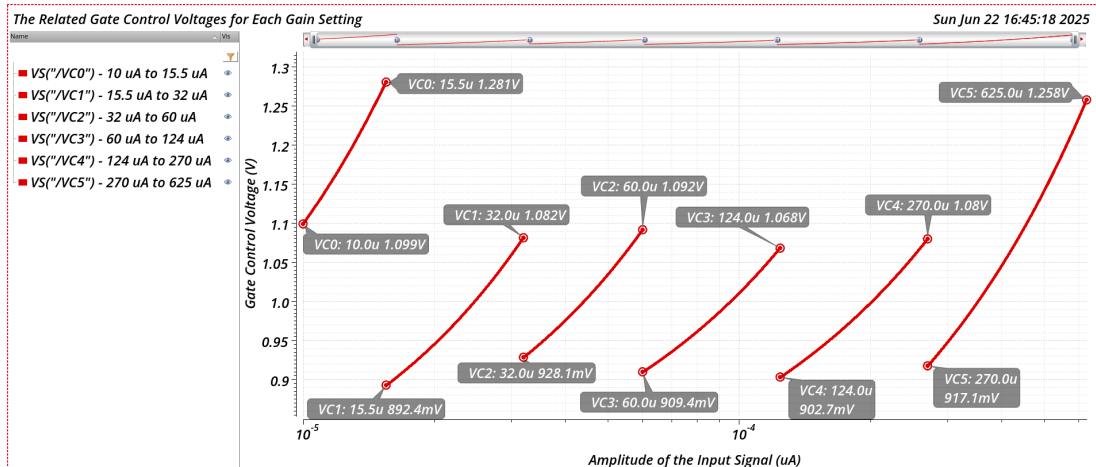


Figure 3.13 : The output voltages of the CVG for each gain setting.

The corresponding changes in the equivalent R_{on} of the triode-region transistors are shown in Fig. 3.14. As the gain stages progress from high to low gain and the transimpedance decreases, the required R_{on} also reduces. This trend ensures that each subsequent gain setting overlaps smoothly with the previous one, allowing continuous gain control without abrupt steps. Since the gain in the first sector is the highest, the highest gain in the second sector should match the lowest gain of the first sector. Therefore, R_{on} of M_{C1} is very high at the beginning of the second gain stage. As the transimpedance gain gets lower, the maximum R_{on} in each setting also decreases. All plots presented in this section are post-layout simulations that are in good agreement with the schematic results. The next section presents the system performance under these control voltages.

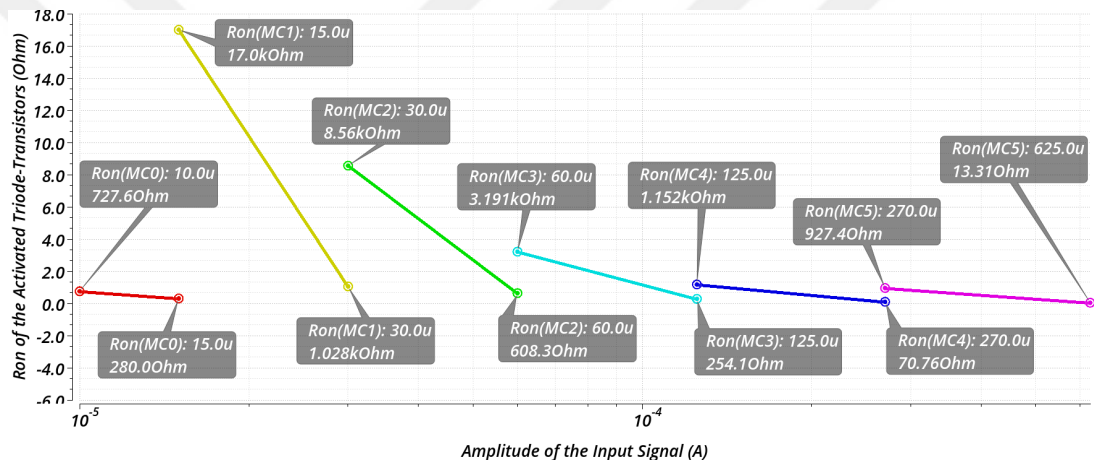


Figure 3.14 : R_{on} of the activated triode-region transistors in the input signal range.

3.4 Feedforward Automatic Gain Control System Simulations

In this section, the focus is on the VG-TIA and the full AGC system. Since the gain, bandwidth, and noise performance of the VG-TIA depend on the feedback path and control signals from the AGC, their simulations are discussed together in this section.

The layout of the VG-TIA is shown in Fig. 3.15. The overall layout size is $40 \mu\text{m} \times 120 \mu\text{m}$, following a narrow and tall aspect ratio. The floor plan helps shorten the horizontal signal path and reduce parasitic effects on it, which is important for ensuring a sufficient speed performance.

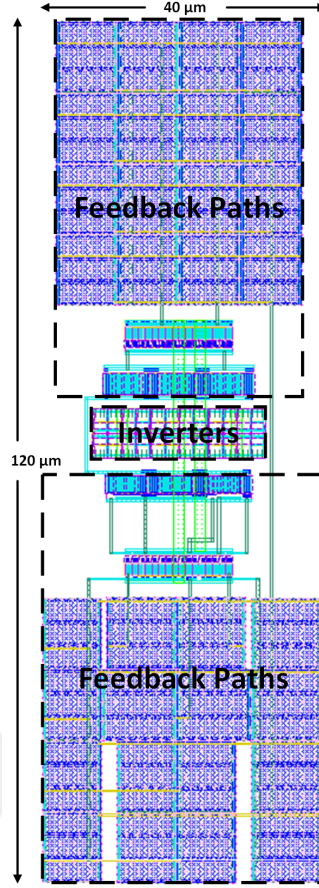


Figure 3.15 : Layout view of the inverter-based VG-TIA.

The inverter cells, which form the core amplification stage, are located at the center of the layout. The feedback paths are placed symmetrically above and below them. Triode transistors and switches are grouped along a vertical axis to keep the design organized and facilitate the routing. Poly resistors used in the feedback paths are placed at the top and bottom edges of the layout.

The same notation used in Fig. 2.6 is followed here. Transistor sizes in the gain control branches follow a binary scaling method. For instance, starting from a unit width in

Table 3.3 : Device Sizes of the Proposed TIA.

Transistor Name	W (μm)	L (nm)
M_1	$0.36 \cdot 16 \cdot 4 = 34.56$	120
M_2	$0.72 \cdot 16 \cdot 4 = 69.12$	120
M_{C0}	$2 \cdot 3 = 6$	120
M_{P0}	$1.2 \cdot 2 = 2.4$	60
M_{N0}	$0.4 \cdot 2 = 0.8$	60

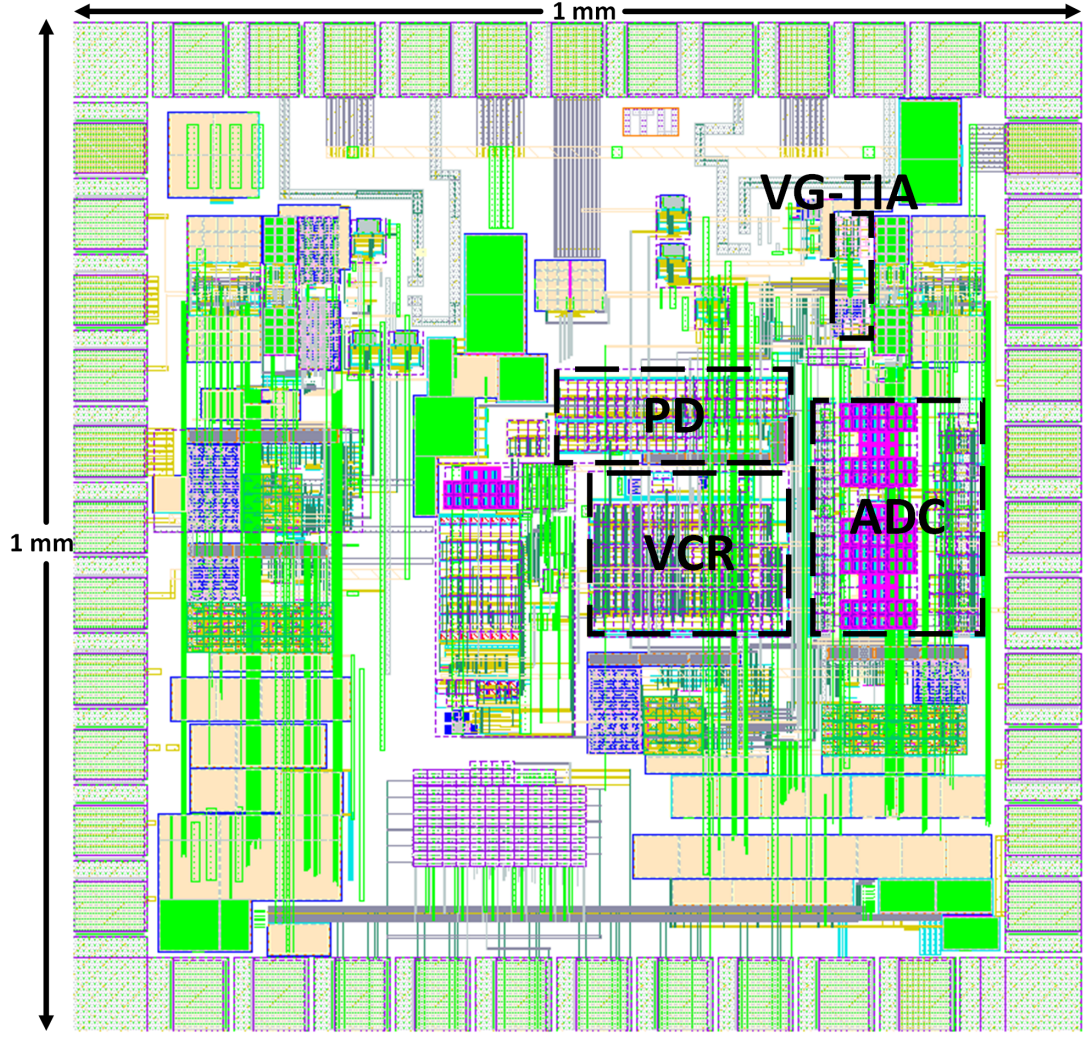


Figure 3.16 : Full chip layout with the pad ring.

the highest gain branch (FB_0), the following branches increase progressively: FB_1 retains the same size, FB_2 uses twice the width, and so on, up to FB_5 , which has sixteen times the unit size. This scaling ensures smooth gain transitions across all settings. Detailed dimensions for the inverter stage and the transistors of the FB_0 are listed in Table 3.3. The transistor sizes in different branches can be found through the corresponding multiplication factors.

The complete layout of the optical receiver chip is shown in Fig. 3.16. The design is implemented in a commercial 65 nm CMOS technology, and the total chip area, including the pad ring, is 1 mm^2 . All sub-blocks of the AGC system—VG-TIA,

PD, ADC, and CVG—are integrated within this area. Their physical locations are highlighted in the figure.

Since the VG-TIA handles the main signal path and processes a PAM-4 current, it is placed close to the pads to maintain signal integrity. The supporting blocks—PD, CVG, and ADC—are positioned below the VG-TIA for controlling the gain adjustments. The floorplan ensures compact integration while minimizing parasitic coupling between blocks.

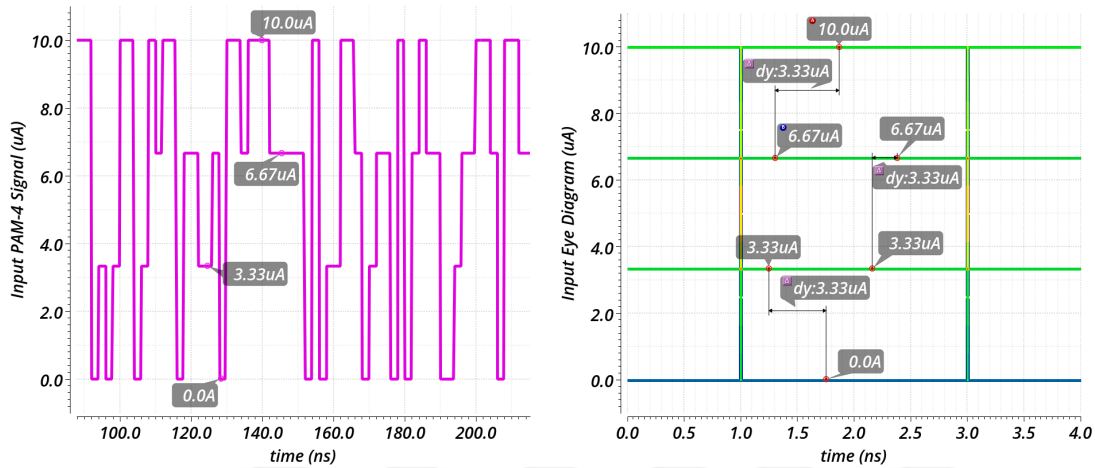


Figure 3.17 : An ideal PAM-4 signal with a 10 μ A amplitude.

Before presenting system-level simulations, it is necessary to investigate the linearity aspect. An example input PAM-4 signal is illustrated in Fig. 3.17. The left plot shows a PAM-4 waveform with a 10 μ A amplitude, clearly demonstrating the four distinct levels. The waveform is divided into 4 ns segments, corresponding to one sample period. They then overlap on another plot to generate an eye diagram. As shown in the right plot of Fig. 3.17, an eye diagram displays long transient runs within a single plot over one sample period. The symbols ‘00’, ‘01’, ‘10’, and ‘11’ are clearly distinguishable. Since the maximum amplitude is 10 μ A, each eye opening corresponds to approximately 3.33 μ A. The horizontal eye opening is primarily affected by the bandwidth and the jitter—lower bandwidth or high jitter narrows the eye opening. The vertical opening indicates the noise margin, which is reduced by inter-symbol interference (ISI). A wide, open eye suggests good signal quality and reliable data recovery.

The transimpedance gain graph is continuous in each gain setting. Therefore, the maximum and minimum levels of each gain sector should be employed in the linearity test. To verify that each gain setting uniformly amplifies the PAM-4 signal levels, a 1-dB compression point test is conducted. The VG-TIA and CVG circuits are simulated together in one test bench. The switches on the feedback paths are controlled manually. The CVG generates its control voltages in DC. The input signal is swept in DC to determine the maximum and minimum points of each sector. The derivative of the output voltage with respect to the input range reveals the change in the transimpedance gain plot, thereby illustrating the system linearity.

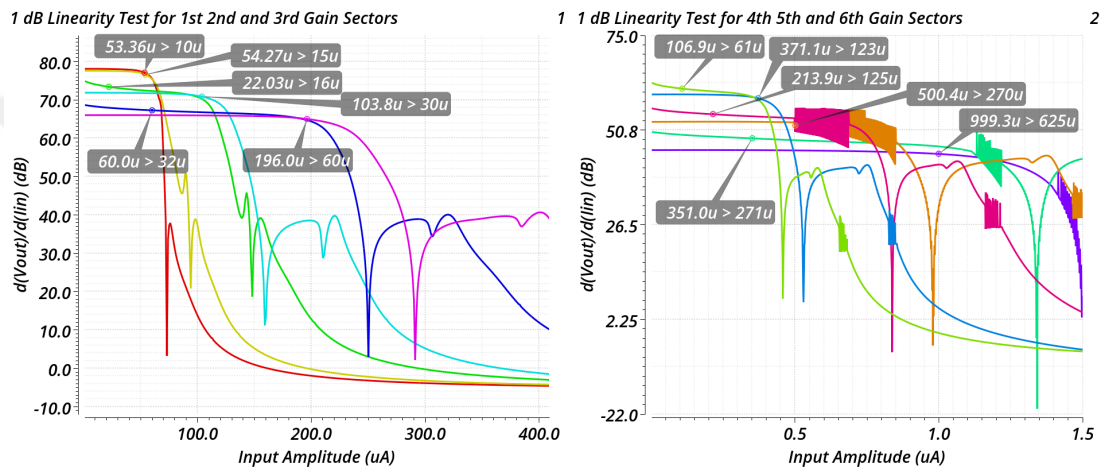


Figure 3.18 : The DC Sweep with the hysteresis

Firstly, the gain at the first eye height (input amplitude divided by 3) is found. This level reflects the lowest non-zero PAM-4 symbol. From this reference gain value, a 1-dB drop is calculated to find the compression threshold. If the full input amplitude lies below this limit, the gain sector is considered linear. It implies that the 4 different levels of a PAM-4 signal are amplified without compression. Fig. 3.18 displays the linearity test plots, which are divided into two subplots. The left side displays the first, second, and third gain sector limits, while the right side displays the remaining ones. As indicated on the plots, the associated linearity borders are exceeded. Hence, the VG-TIA is working linearly in each sector.

The presented results are obtained from post-layout extracted (LPE) simulations. To compare these outcomes with the schematic-level simulations, Table 3.4 summarizes

the outcomes. The results confirm that the VG-TIA operates linearly across the entire dynamic range of the AGC system.

Table 3.4 : 1-dB Compression Point Results.

Input Amplitude	Gain Sector	1-dB Compression Point	
		SCH	LPE
10 μA	1st	54.05 μA	53.36 μA
15 μA	1st	54.87 μA	54.27 μA
16 μA	2nd	25.34 μA	22.03 μA
30 μA	2nd	105.5 μA	103.8 μA
31 μA	3rd	49.87 μA	61.11 μA
59 μA	3rd	196 μA	196 μA
60 μA	4th	99.3 μA	106.9 μA
123 μA	4th	375.9 μA	371.1 μA
124 μA	5th	219.6 μA	214 μA
267 μA	5th	576 μA	500.4 μA
268 μA	6th	368 μA	351.1 μA
625 μA	6th	977.6 μA	999.3 μA

After the linearity test, the full AGC system simulations are conducted. Initially, the AGC system requires a transient simulation to settle. The corresponding gain setting for the input amplitude is found. Subsequently, V_C values and the Flash ADC bits are determined. Once the operating condition is settled, the AC simulation is performed. Fig. 3.19 displays the schematic-level transimpedance gain in the frequency domain.

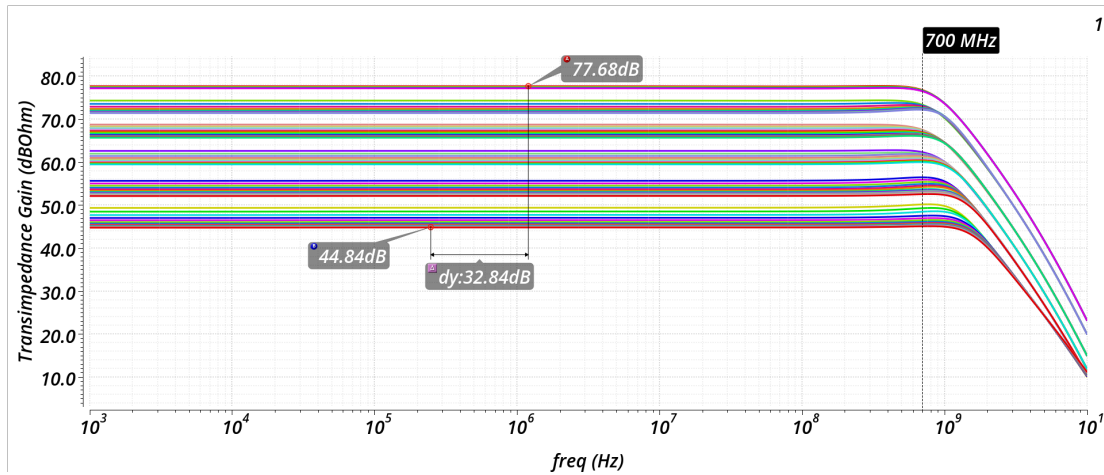


Figure 3.19 : The AC gain range of the schematic-level system simulation.

Furthermore, the minimum gain is 44.84 dBΩ, and the maximum is 77.68 dBΩ. Besides, the post-layout results of the AC gain are given in Fig. 3.20. Only the border

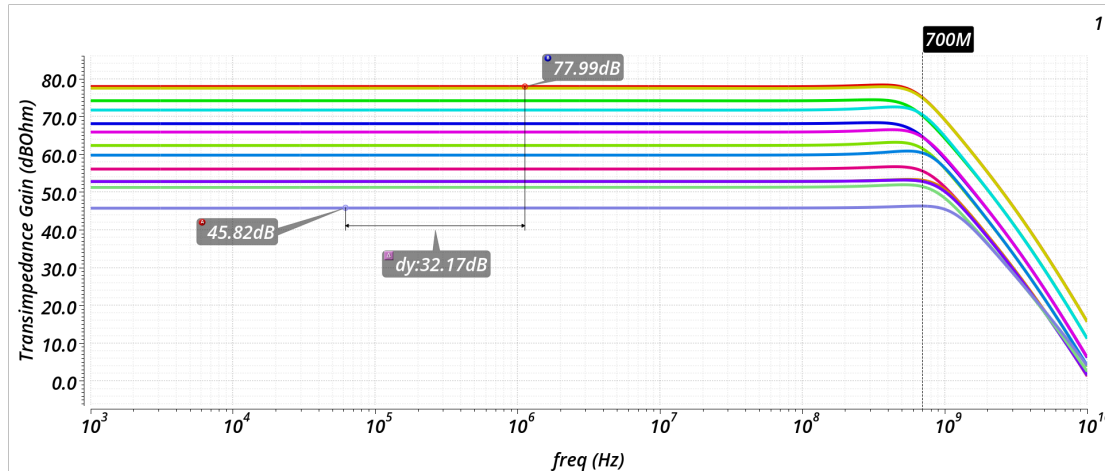


Figure 3.20 : The AC gain range of the post-layout system simulation.

input amplitudes are simulated in the RCC-extracted mode simulation. Still, continuity exists in each sector. Observations reveal that the continuity in each gain sector ensures a 32.87 dB dynamic range at the schematic-level simulations and 32.17 dB in the post-layout simulations. The plot is a basic demonstration of a hybrid-mode gain control system. There are distinct gain sectors, and the gaps between them are bridged by the analog gain control.

The peak of the AC response is approximately equal to the input-output pole spacing. It is dependent on the transimpedance gain of the VG-TIA. As the transimpedance gain changes, the stability is ensured by changing the input capacitance. Hence, all gain settings have different input capacitance values. In the highest gain mode, the capacitance is the lowest because the gain separates the poles adequately. The capacitance increases as the gain decreases. The added input capacitances ensure that the input pole is the dominant pole in the TIA. To achieve this, a capacitance bank is designed and controlled with digital bits.

A marker is placed at 700 MHz to indicate the system bandwidth. The worst-case-3-dB bandwidth in the schematic simulation is 900 MHz, which degrades to 700 MHz in the LPE simulations. This bandwidth is still sufficiently wide to accommodate a 1 Gbps PAM-4 modulated input signal. Additionally, the peaking remains below 1 dB across all gain-setting scenarios.

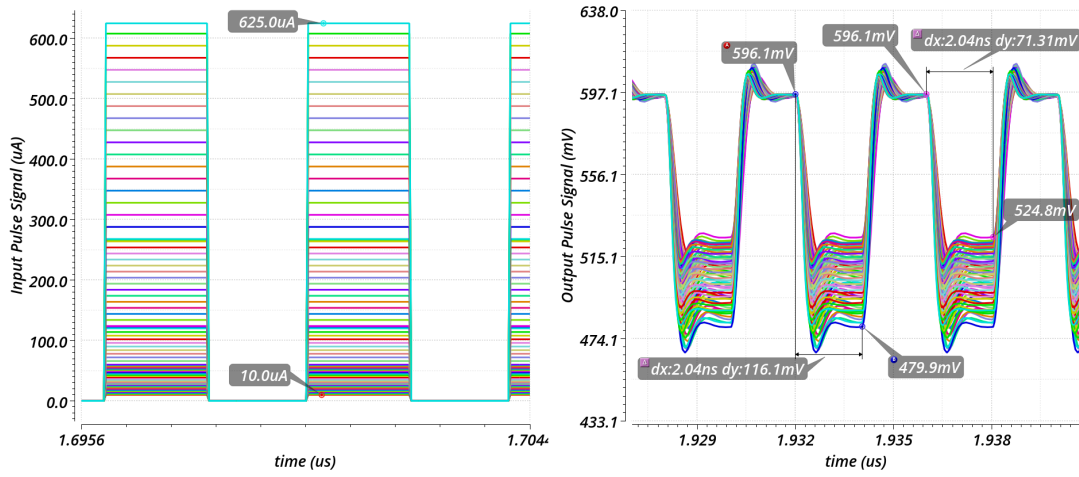


Figure 3.21 : Transient pulse response of the AGC circuit at the schematic level.

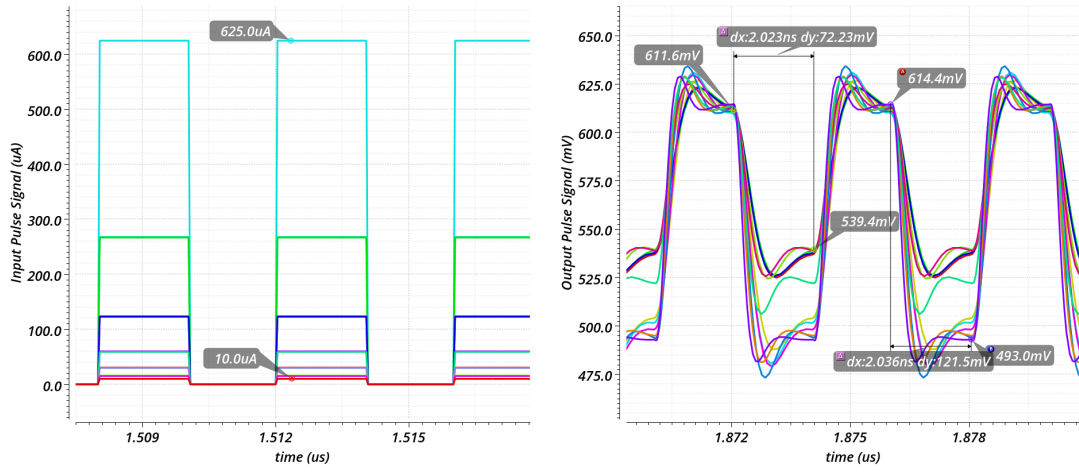


Figure 3.22 : Transient pulse response of the AGC circuit at the post-layout level.

Fig. 3.21 and Fig. 3.22 are the results of the time-domain simulations. The first one belongs to the schematic simulations, while the other one is from the LPE. The input is given as pulse signals at 250 MHz. The plots on the left side of the figures display the inputs over time. The input amplitude range is between 10 μA and 625 μA . The output pulse characteristics are on the right sides of both figures. Since LPE simulations require more time and space, only the most important boundary values are simulated using the LPE, while a wider input spectrum is simulated with the schematic configuration. The pulse response of the system is underdamped, and it settles after a peak. The size of the peak is larger in the LPE simulations. The input capacitance can be increased to reduce the peaking, but this will impact the speed of the AGC.

Another way to evaluate the effectiveness of the AGC system is by observing the peak-to-peak output voltage (V_{PP}) response, as shown in Fig. 3.23 (schematic) and Fig. 3.24 (post-layout). The x -axis represents the input signal amplitude in microamperes μA , and the y -axis shows the resulting peak-to-peak output voltage in millivolts (mV).

In an ideal linear amplifier, the output amplitude would increase commensurately with the input. However, in this AGC system, the gain is automatically adjusted depending on the received signal level. As the input amplitude increases, the system gradually lowers the gain to maintain a nearly constant output amplitude. It employs two methods

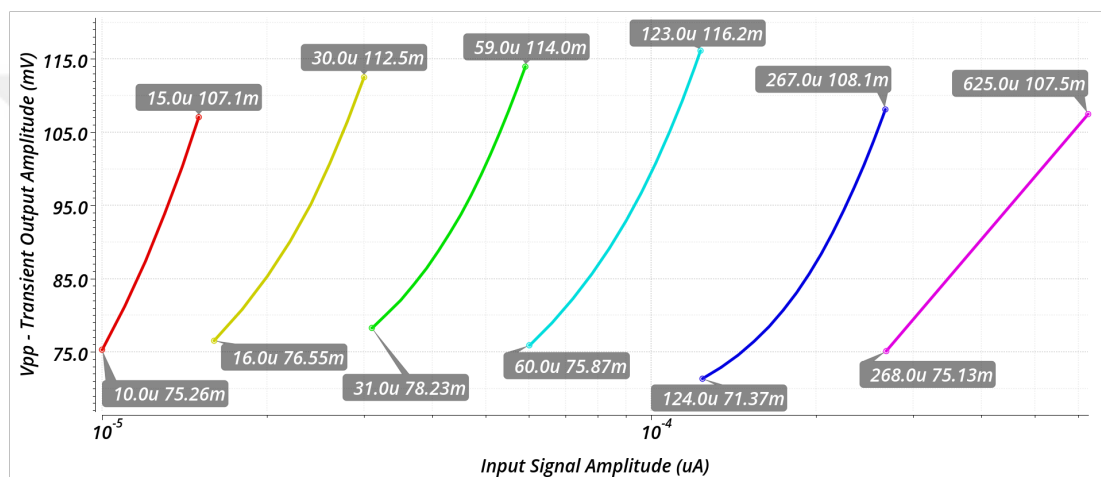


Figure 3.23 : Peak-to-peak output voltage across the input range in the schematic simulations.

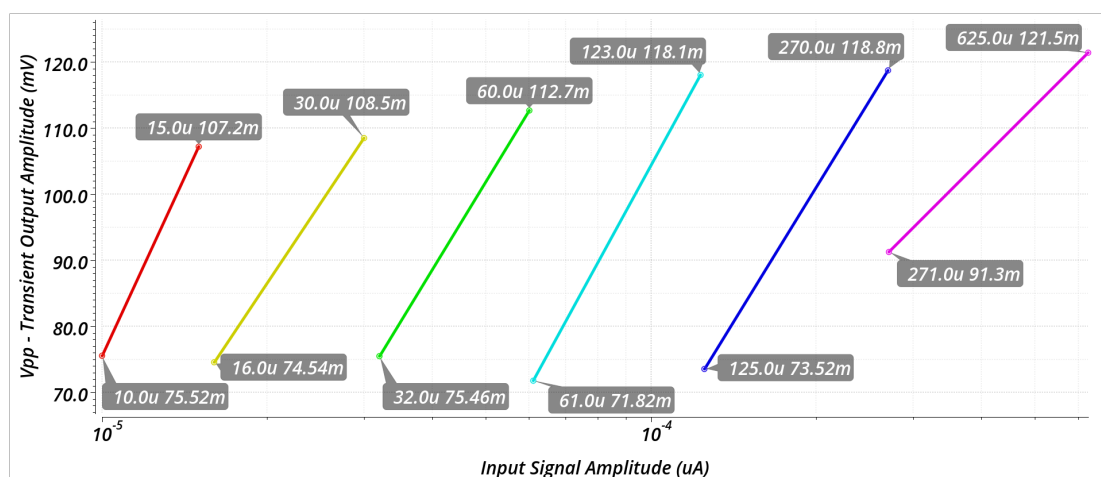


Figure 3.24 : Peak-to-peak output voltage across the input range in the post-layout simulations.

for this: one is to lower R_{on} on the feedback branch, and the other is to activate a parallel branch to decrease the transimpedance. This adaptive behavior is clearly visible in the plot: Each colored curve represents a different gain sector, and within each sector, the output voltage slightly increases before the gain shifts to the next lower level.

The compression effect of the AGC is visibly demonstrated: across a wide input current range—from $10\text{ }\mu\text{A}$ to $625\text{ }\mu\text{A}$ —the output peak-to-peak voltage remains within a much narrower span. This input range corresponds to a variation factor of 62.5, or 40 dB. In the schematic simulation, the output voltage varies approximately from 71 mV to 116 mV, resulting in a ratio of 1.63, which corresponds to 4.23 dB. In the post-layout simulations, the output ranges from 71.8 mV to 121.5 mV, resulting in a ratio of 1.7, or approximately 4.56 dB. In both cases, the output variation remains below 6 dB (or a factor of 2 in linear terms), which is a strong indicator of the effective gain compression. In summary, the variation factor reduces from 62.5 to 1.7 at the output. Minor discrepancies between the schematic and post-layout results arise from parasitic effects; however, the AGC system reliably sustains stable operation and effectively compresses the wide input dynamic range, as designed.

The input-referred noise (IRN) performance of the system is shown in Fig. 3.25. The noise is swept between 1 kHz and 2 GHz. As the frequency goes up, the noise increases as well. However, the bandwidth of the system attenuates the high-frequency

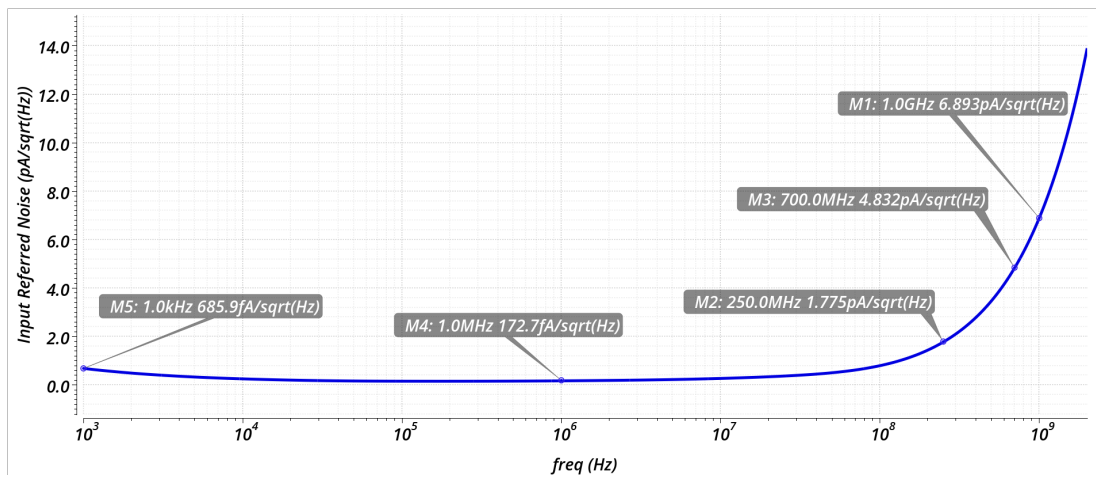


Figure 3.25 : Input-referred noise over the spectrum.

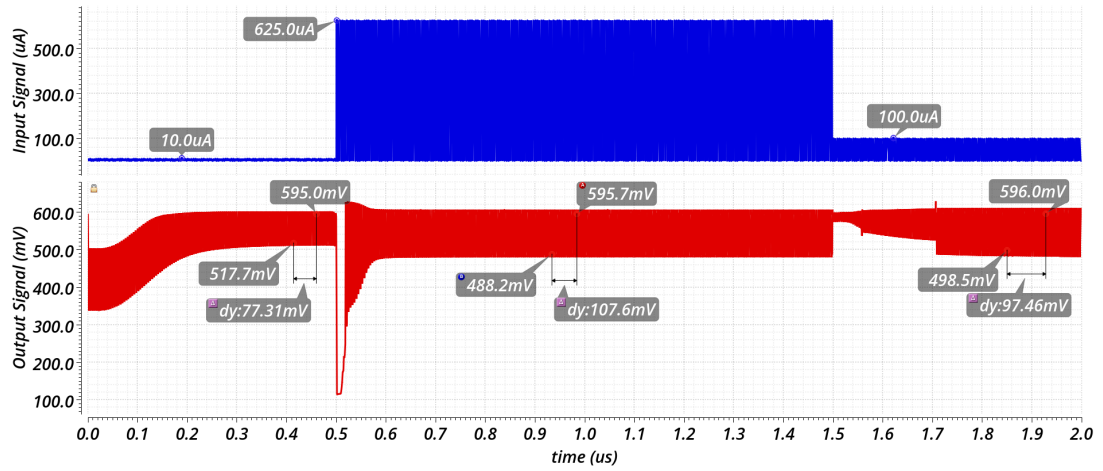


Figure 3.26 : Attack and release time schematic simulation.

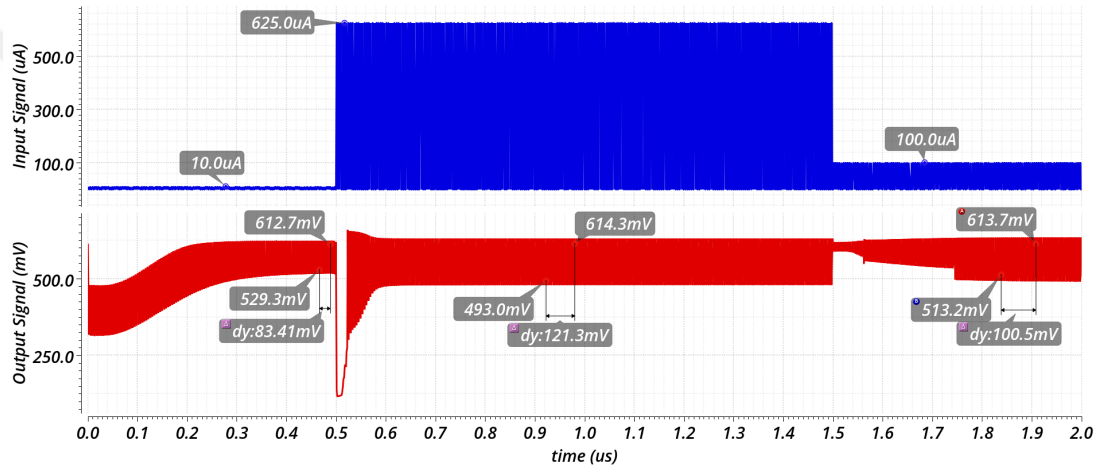


Figure 3.27 : Attack and release time post-layout simulation.

elements of noise. Excessive bandwidth can introduce additional high-frequency noise components. This situation indicates that there is an optimal bandwidth range for effective performance. The integrated input-referred noise for the smallest PAM-4 signal level (10 μ A), calculated over the frequency range of 1 kHz to 1 GHz, is 126 nA. This value remains well below the signal level, ensuring sufficient sensitivity and reliable operation.

Another critical test for evaluating the AGC system is observing the attack and release behavior during large signal transitions. The simulation follows a similar methodology to the peak detector test shown in Fig. 3.7. The input current is initially set to 10 μ A, then increased to 625 μ A at 0.5 μ s, and later decreased to 100 μ A at 1.5 μ s. Fig. 3.26

(SCH) and Fig. 3.27 (LPE) demonstrate the input and output behaviors over time. In the upper subplots, the blue graphs represent the input signals; whereas, in the subplots below, the red graphs demonstrate the output voltage behavior of the proposed AGC over time. This sequence tests the ability of the system to respond to significant amplitude changes across its entire dynamic range.

The system begins in an uninitialized state. Initially, the VG-TIA feedback path is effectively inactive, as the peak detector has not yet generated a valid output. Consequently, the Flash ADC outputs are all low, and the CVG control voltages are close to zero. In this condition, the triode-region transistors in the feedback path remain in the cutoff region, preventing the VG-TIA from operating with correct biasing. Once the peak detector settles and begins generating its output, the transistors enter the triode region, activating the feedback path. This situation enables the input and output DC levels to settle. After this initial settling phase, the system identifies the $10\ \mu\text{A}$ input level and selects the highest gain setting, as expected for the lowest signal amplitude.

At $0.5\ \mu\text{s}$, the input current is increased to $625\ \mu\text{A}$. Initially, the output saturates because the high-gain setting continues to amplify the large input. The AGC system detects this and quickly lowers the gain to prevent distortion. The attack time is measured as $80\ \text{ns}$ in both schematic and post-layout simulations.

At $1.5\ \mu\text{s}$, the input amplitude is decreased to $100\ \mu\text{A}$. At first, the system continues to use the lower gain setting from the previous high input level, resulting in a reduced output signal. Then, the AGC gradually increases the gain to match the new input. The gradual rise in the gain can be observed in the output voltage plots. The release time is calculated as $200\ \text{ns}$ in the schematic and $240\ \text{ns}$ in the LPE simulation.

The attack and release time simulations are crucial for the wide input dynamic range amplitude systems. The results confirm that the proposed AGC system operates reliably over a wide input dynamic range and demonstrate the ability of the system to quickly adapt to changing signal amplitudes, with no corruption or compression artifacts, while maintaining stable and accurate gain control.

The eye diagrams at the gain-setting boundaries are shown in Fig. 3.28 and Fig. 3.29. Fig. 3.28 presents the results for the first three gain sectors, where the input signals are

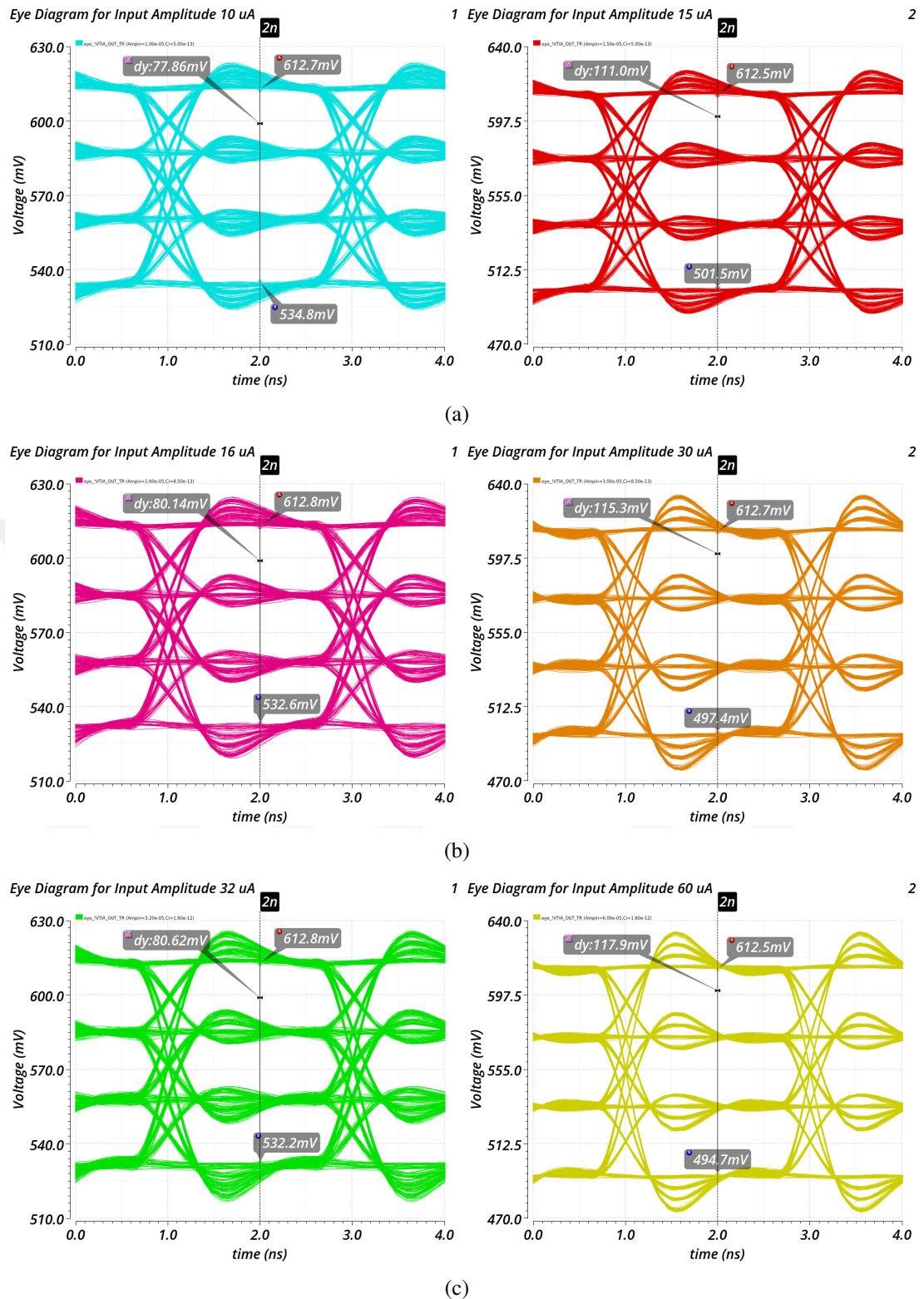


Figure 3.28 : Eye diagrams — Boundaries of the (a) first, (b) second, and (c) third gain settings

small and the gain is high. Fig. 3.29 shows higher input amplitudes with lower gain settings. A 250 MHz PAM-4 signal is used. To reflect real-world conditions, noise up

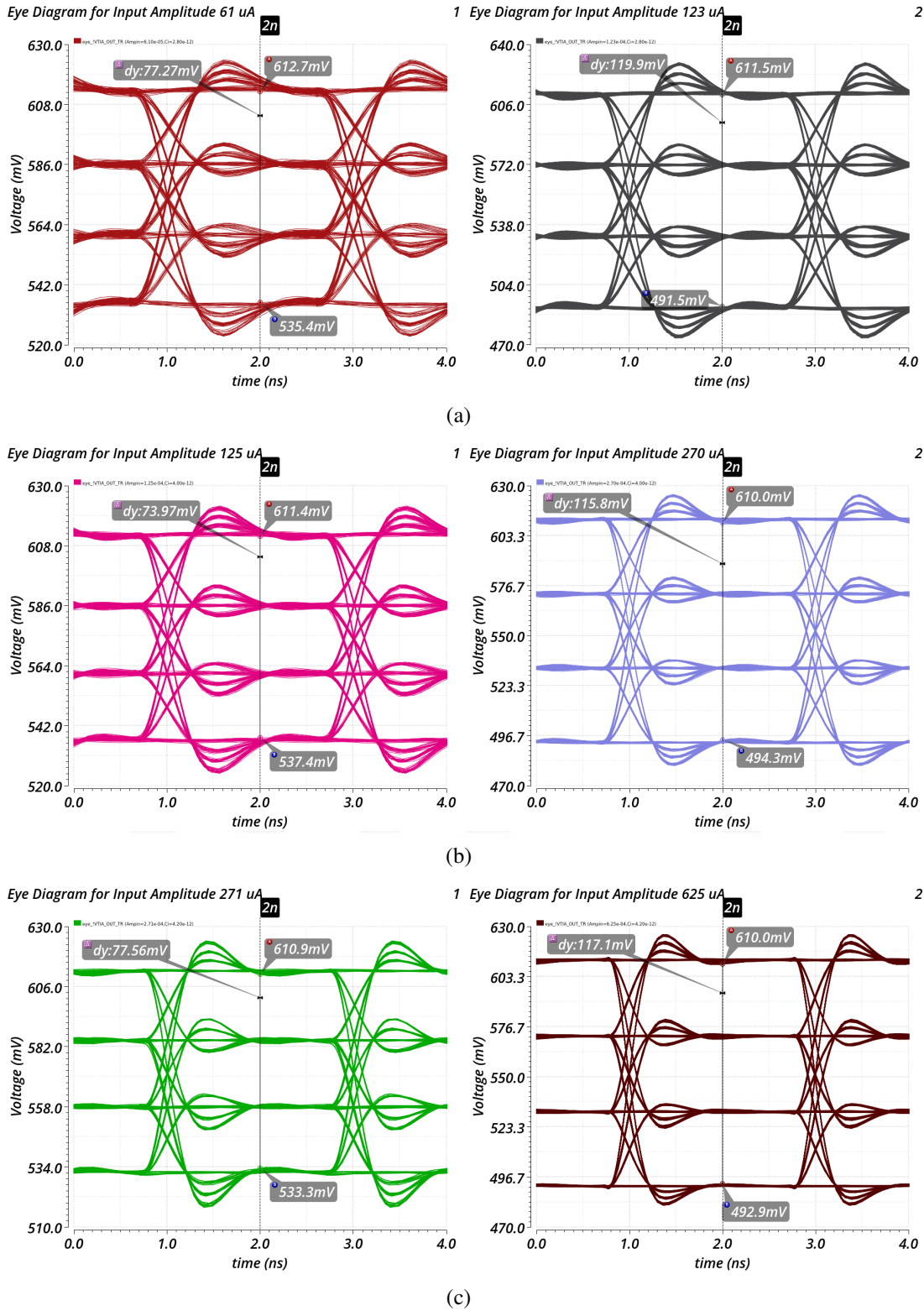


Figure 3.29 : Eye diagrams — Boundaries of the (a) fourth, (b) fifth, and (c) sixth gain settings

to 1 GHz is included in the simulations. Several effects distort the quality of the eye diagram, such as bandwidth limitations, ISI, and noise. Still, all eye openings remain

distinguishable, and the signal levels are well separated, confirming reliable detection across all gain settings.

The equal eye heights confirm a linear transimpedance gain behavior. Peaking in the diagrams can be reduced by increasing the input capacitance. This approach damps the high-frequency ringing but narrows the bandwidth. A smaller bandwidth would reduce horizontal eye opening. Therefore, a trade-off exists between the vertical and horizontal eye clarity. The peak-to-peak amplitudes in the eye diagrams are consistent with the expected values.

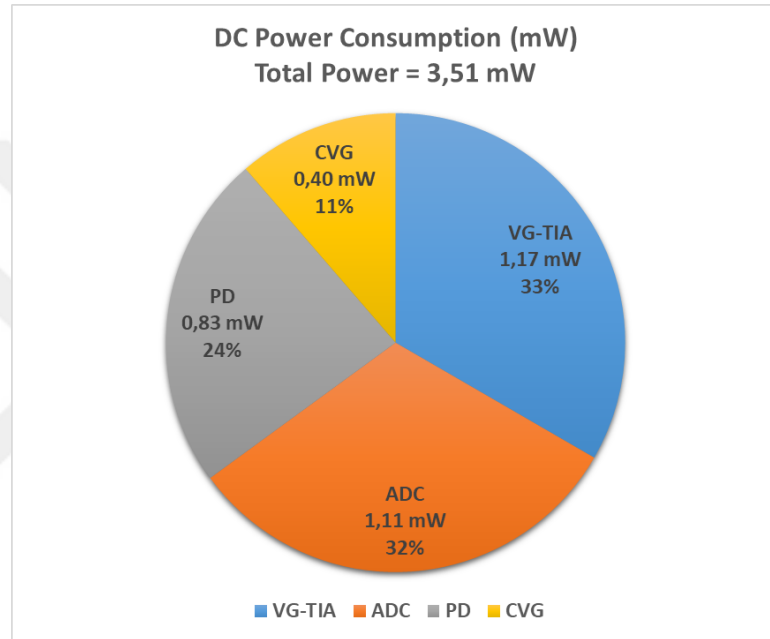


Figure 3.30 : Pie chart of the DC power consumption.

The DC power consumption distribution of the AGC system blocks is illustrated in Fig. 3.30. The total power consumption is measured as 3.51 mW. Among all sub-blocks, the VG-TIA consumes the largest share at 1.17 mW, which corresponds to 33% of the total. This proportion is expected, as the transconductances (g_m) of the transistors should be large enough to ensure a high open-loop gain. High transconductance also reduces the noise at the input. Besides, the circuit should satisfy the bandwidth requirement. So, the moderate power usage of the VG-TIA is essential. The ADC follows closely, consuming 1.11 mW (32%), primarily due to its heavy use of current mirrors. The peak detector consumes 0.83 mW (24%), primarily due to its cascode structure and biasing circuitry. Lastly, the CVG has the lowest power

consumption at 0.40 mW (11%). These results confirm that the power consumption is reasonably distributed across the system, with the VG-TIA dominating, which aligns with expectations.

3.5 PVT Simulations

This section examines the main performance parameters of the proposed AGC in different process voltage temperature (PVT) corners. Linearity, noise, transimpedance gain, bandwidth, compression ratio, eye diagram, and attack and release times are evaluated in this part.

The simulations were conducted across 27 different corners, encompassing three process variations (fast-fast (FF), typical-typical (TT), and slow-slow (SS)), three

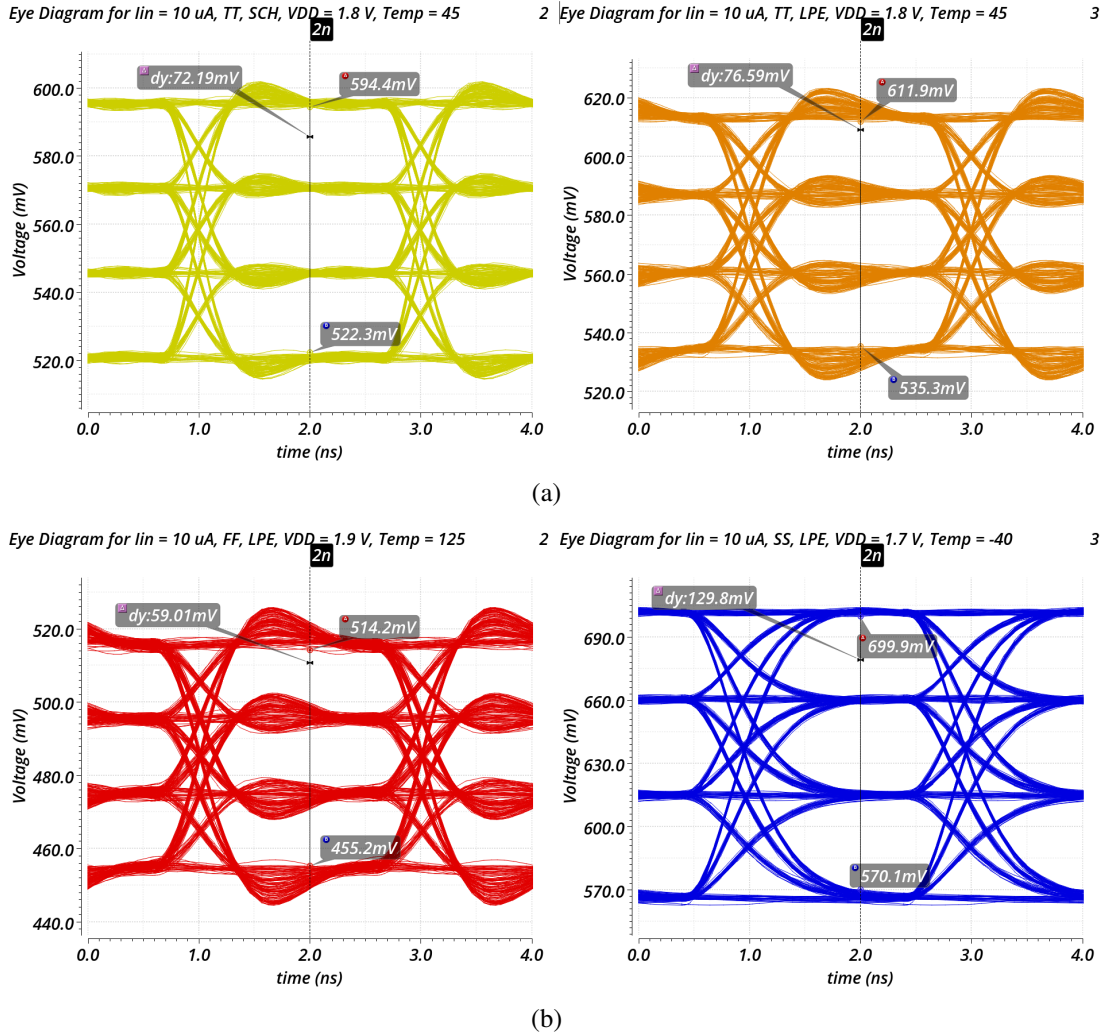


Figure 3.31 : Eye diagram results of four different setups (a) SCH-TT and LPE-TT, (b) LPE-FF and LPE-SS.

supply voltages (1.7 V, 1.8 V, and 1.9 V), and three temperature levels (-40°C , 45°C , and 125°C). Each case was evaluated with a $10\ \mu\text{A}$ input signal, which represents a typical operating point for the system and allows a fair comparison between corners.

Then, three representative corners have been chosen. The corners are a typical case (TT, 1.8 V, 45°C), a slow corner (SS, 1.7 V, -40°C), and a fast corner (FF, 1.9 V, 125°C).

Fig. 3.31 illustrates the eye diagrams for a $10\ \mu\text{A}$ input current. The top two plots (Fig. 3.31(a)) demonstrate the typical corner (TT, 1.8 V, 45°C); the left one is the schematic result, and the right plot represents the post-layout simulation outcome. The total eye heights of the schematic and post-layout simulations are approximately equal, indicating that parasitic extraction has a minimal impact on the eye diagram. The bottom left plot represents the fast corner (FF, 1.9 V, 125°C), where the reduced total eye height (59 mV) indicates a slightly degraded gain and higher bandwidth. Moreover, the transient noise is more visible due to the low output amplitude.

In contrast, the bottom right plot shows the slow corner (SS, 1.7 V, -40°C), where the eye opening significantly increases to 129 mV. Because of the high output amplitude, the noise is less significant in this case. The increased gain comes along with reduced bandwidth. The effect of the limited bandwidth is seen at the sides of the eye, which narrows the eye opening. Overall, the given eye diagrams confirm that the AGC remains functional across corners, with sufficient margin for reliable PAM-4 detection.

After determining the transient operating points and corresponding gain settings, AC-LPE simulations were performed. Fig. 3.32 shows the transimpedance gain curves for TT, SS, and FF corners at a $10\ \mu\text{A}$ input current. As expected, the TT corner falls between the SS and FF corners in both gain and bandwidth. Due to increased poly resistance at the SS corner, the transimpedance gain reaches $81.66\ \text{dB}\Omega$. It is the highest among the three, but the bandwidth ($-3\ \text{dB BW} = 461.6\ \text{MHz}$) is reduced. Conversely, the FF corner exhibits the lowest gain ($75.92\ \text{dB}\Omega$), as the resistance is lower; yet, it achieves the widest bandwidth at $717.6\ \text{MHz}$. The TT corner offers a balanced trade-off, featuring a gain of $78.09\ \text{dB}\Omega$ and a bandwidth of $658.6\ \text{MHz}$. These results confirm that process variations primarily affect the passive components,

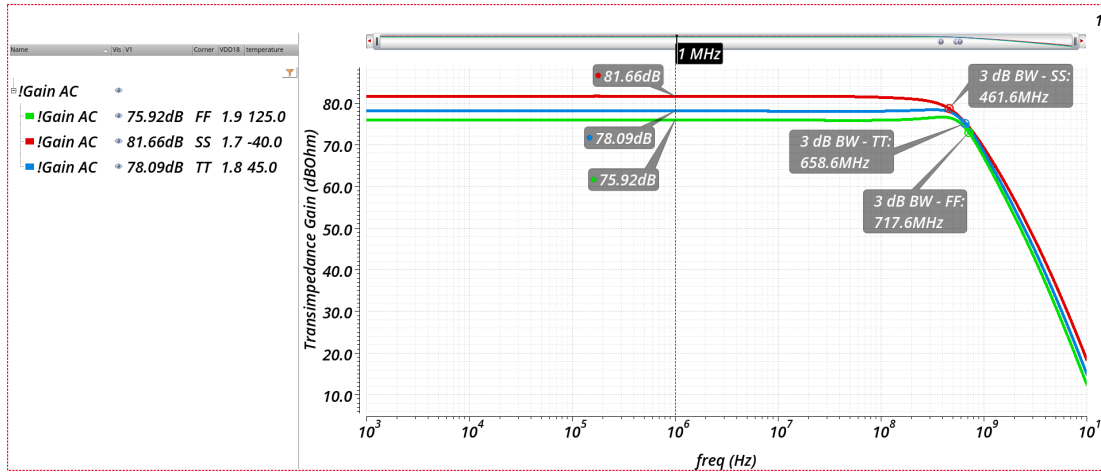


Figure 3.32 : AC transimpedance gains at the SS, TT, and FF corners.

thereby shifting the gain-bandwidth trade-off, while the overall AGC functionality remains preserved.

Linearity is another critical aspect in evaluating the performance of the proposed AGC system. Due to the high computational cost of layout-level linearity simulations, the tests were performed only at the schematic level. The typical corner results are already presented in Table 3.4, so this section focuses on the extreme process corners—FF and

VDD	temperature	Ampin	Corner	Pass/Fail	Linearity
1.9	125	10u	FF	pass	52.31u
1.9	125	15u	FF	pass	53.77u
1.9	125	16u	FF	pass	76.69u
1.9	125	30u	FF	pass	103.3u
1.9	125	31u	FF	pass	119.4u
1.9	125	59u	FF	pass	187.2u
1.9	125	60u	FF	pass	240.1u
1.9	125	123u	FF	pass	347u
1.9	125	124u	FF	pass	500.2u
1.9	125	267u	FF	pass	610.8u
1.9	125	268u	FF	pass	762.7u
1.9	125	625u	FF	pass	731.7u
1.7	-40	10u	SS	pass	27.77u
1.7	-40	15u	SS	pass	27.24u
1.7	-40	16u	SS	near	14.83u
1.7	-40	30u	SS	pass	50.09u
1.7	-40	31u	SS	pass	34.86u
1.7	-40	59u	SS	pass	100.5u
1.7	-40	60u	SS	pass	69.34u
1.7	-40	123u	SS	pass	204.4u
1.7	-40	124u	SS	fail	108.3u
1.7	-40	267u	SS	pass	412.5u
1.7	-40	268u	SS	fail	191.2u
1.7	-40	625u	SS	pass	751.2u

Figure 3.33 : Linearity check for the FF and SS corners.

SS. Figure 3.33 demonstrates that all FF operating points satisfy the linearity criteria. In the SS corner, where devices are slower and resistances are higher, some setups fail to meet the necessary linearity threshold. Two mid-range amplitude cases exceed acceptable limits, identified as "fail," while one additional point is classified as "near." Despite these corner-specific issues, the overall functionality of the AGC is preserved throughout the majority of the operating range.

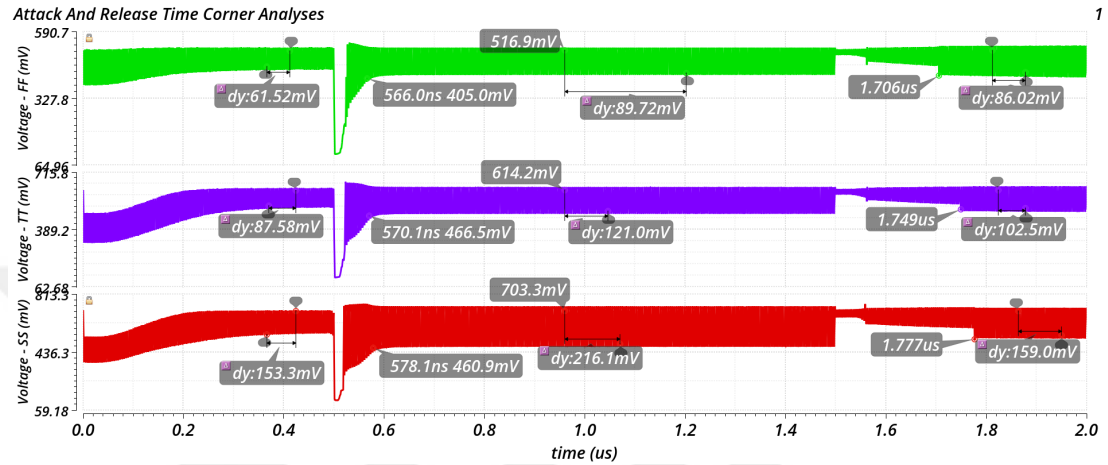


Figure 3.34 : Post-layout attack and release times at the SS, TT, and FF corners.

Next, attack and release times of the AGC are evaluated through post-layout simulations under the three PVT corners. As illustrated in Fig. 3.34, the AGC has the fastest response in the FF corner, achieving an attack time of 66 ns and a release time of 206 ns. The TT corner follows with 70 ns and 250 ns, respectively. In the

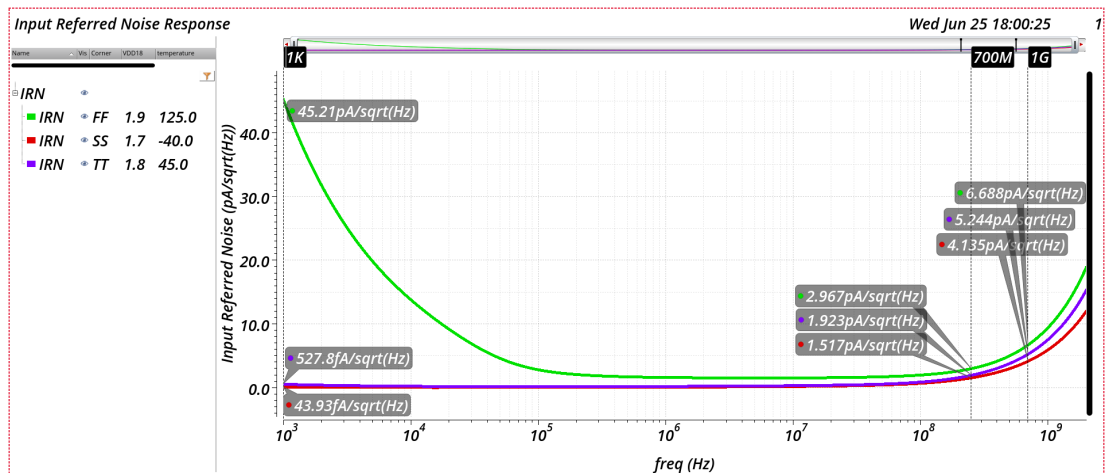


Figure 3.35 : Input-referred noise plots at the SS, TT, and FF corners.

SS corner, where transistors operate more slowly, the response is the slowest, with an attack time of 78 ns and a release time of 277 ns. As expected, process variations affect both the settling behavior and the amplitude swing during transitions.

The following simulation focuses on the noise performance at three different corners, which comes after the analysis of the attack and release behavior of the AGC system. A graphic illustration of the performances at each of the three corners can be found in Fig. 3.35. Due to the increased device speed and decreased intrinsic gain, the FF corner exhibits a higher level of noise at extremely low frequencies. SS and TT corners have similar responses. When the noise is integrated up to 1 GHz, the IIRN is found as $0.108 \mu\text{A}$ for the SS corner and $0.177 \mu\text{A}$ for the FF corner. As discussed above,

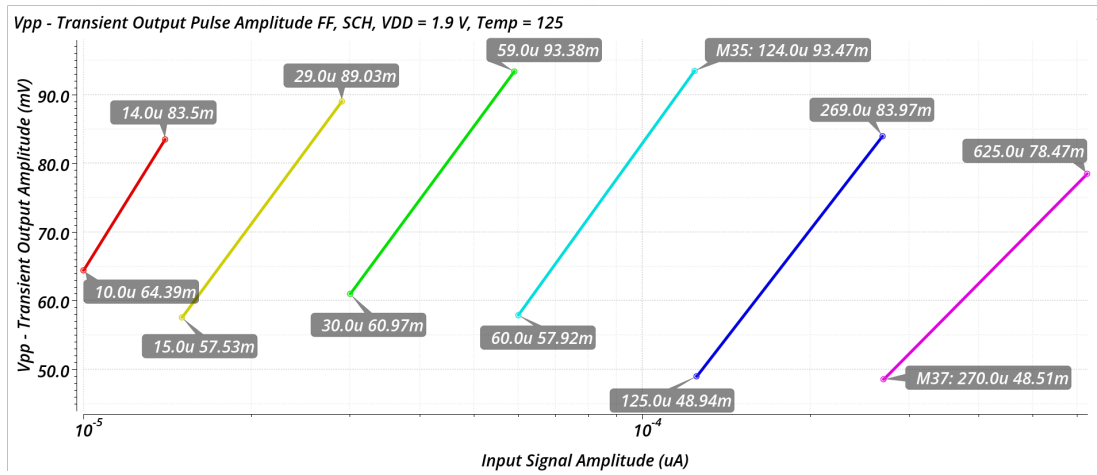


Figure 3.36 : Peak-to-peak output voltage amplitudes in the FF corner.

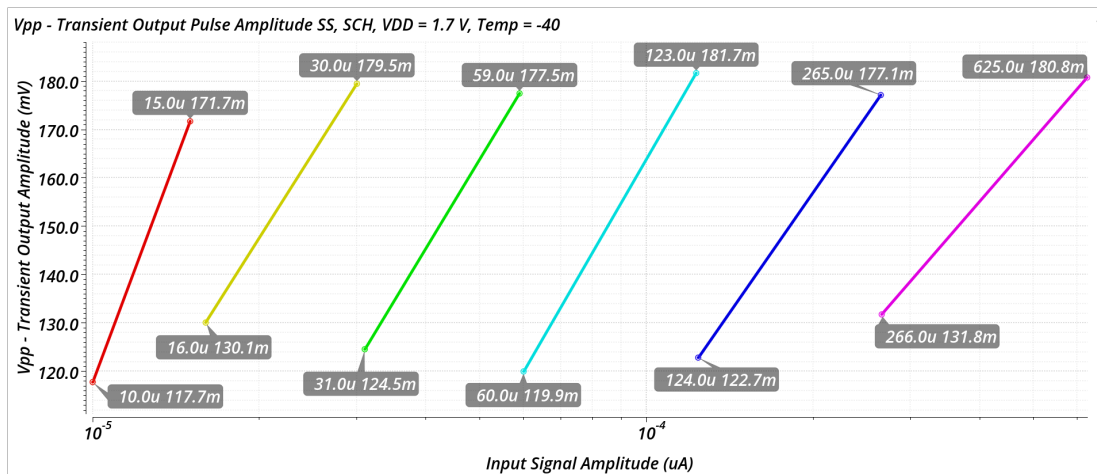


Figure 3.37 : Peak-to-peak output voltage amplitudes in the SS corner.

the IIRN of the TT corner is $0.127 \mu\text{A}$. Even though the noise in the FF corner has become more noticeable, it is still considered acceptable. As the smallest eye height is $3.33 \mu\text{A}$, the integrated input referred noise is negligible. The reflection of this is seen in Fig.3.31.

Afterward, several transient schematic-level simulations are conducted to find the output pulse amplitude range. The post-layout simulation was performed and explained in the previous section. Figure 3.23 shows the peak-to-peak output voltages in the TT corner, ranging from 71.4 mV to 116 mV, which corresponds to a linear output variation ratio of 1.63, or approximately 4.23 dB.

The same test is applied at the SS and FF corners. The FF corner results are represented in Fig. 3.36. Since the values of the poly resistors decrease in the FF corner, the transimpedance gains in all settings are reduced. Therefore, V_{pp} results are decreased as well. The output variation ratio remains consistent in the FF corner, with the values confined between 49 mV and 93.5 mV. This ratio represents $(\frac{93.5}{49} = 1.91)$ on a linear scale, which is equivalent to 5.61 dB. Conversely, Fig. 3.37 illustrates the higher voltage amplitudes in the SS corner, which result from the significant dependence on the resistors in the transimpedance gain. The output voltages are compressed between 119.9 mV and 181.7 mV, yielding a linear ratio of 1.51, or 3.61 dB. Lastly, Table 3.5 summarizes the compression performances of the three representative corners. The compression ratio formula was given in 2.1. To calculate it, the input variation in the dB scale is also necessary. It is equal for all corners to $\frac{625 \mu\text{A}}{10 \mu\text{A}} = 62.5$, or equivalently 35.9 dB. Even under extreme PVT conditions, the AGC consistently compresses the wide input dynamic range. In all cases, the output variation remains below 6 dB, corresponding to a maximum linear ratio of 2.

Table 3.5 : Variation and Compression Ratios at the Output Voltage.

Corner Type	Variation Ratio in Linear	Variation Ratio in dB	Compression Ratio
SS - SCH	1.51	3.61	32.29
TT - SCH	1.63	4.23	31.67
TT - LPE	1.64	4.32	31.58
FF - SCH	1.91	5.61	30.29

3.6 Monte Carlo Simulations

While corner simulations show systematic variations, Monte Carlo reveals the impact of local mismatches, such as V_{TH} and size variations. These effects become more critical in deep-submicron CMOS processes. Hence, Monte Carlo simulations with mismatch parameters have been conducted.

To test the robustness of the AGC, transient simulations were repeated across various input amplitudes. Since all performance parameters are changing based on the input amplitude, Monte Carlo simulations should be conducted for all gain setting boundaries. 50 Monte Carlo simulations are conducted to demonstrate the input level. A total of 1300 simulations have been completed. In the transient simulations, pulse signals are transmitted, and the output voltages are observed. These simulations illustrate how mismatches affect key performance metrics. Moreover, they help evaluate the reliability of the design under process variation.

The transient responses of the 1300 samples in the Monte Carlo (MC) simulations are given in Fig. 3.38. The peaking and amplitude of the pulses change from sample to sample. Since the peaking is correlated with the input capacitance, it can be manually adjusted to ensure compliance with design criteria. As can be seen from Fig. 3.38, all pulses settle after an overshoot. The largest and the smallest pulse amplitudes are shown with markers. The output voltage range changes minimally in the mismatch simulations.

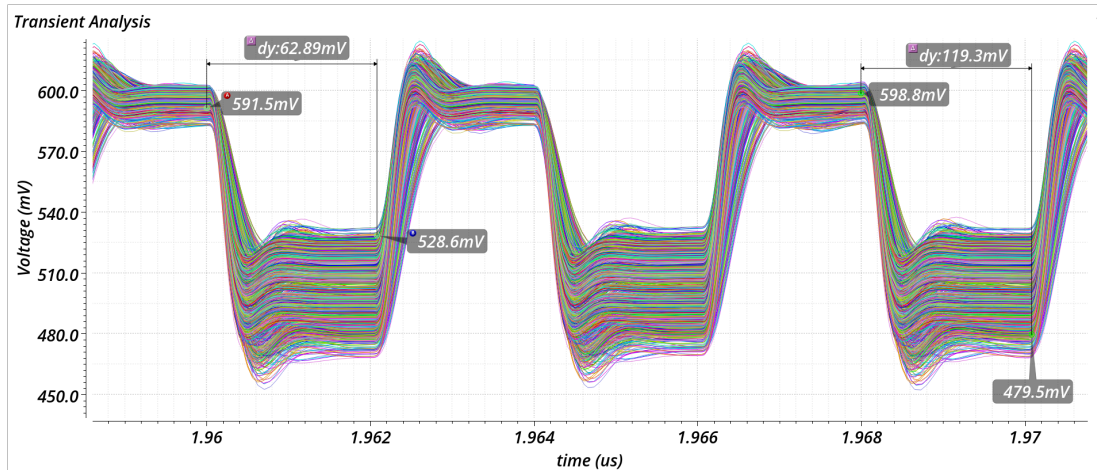


Figure 3.38 : The output voltage signals of the Monte Carlo simulations.

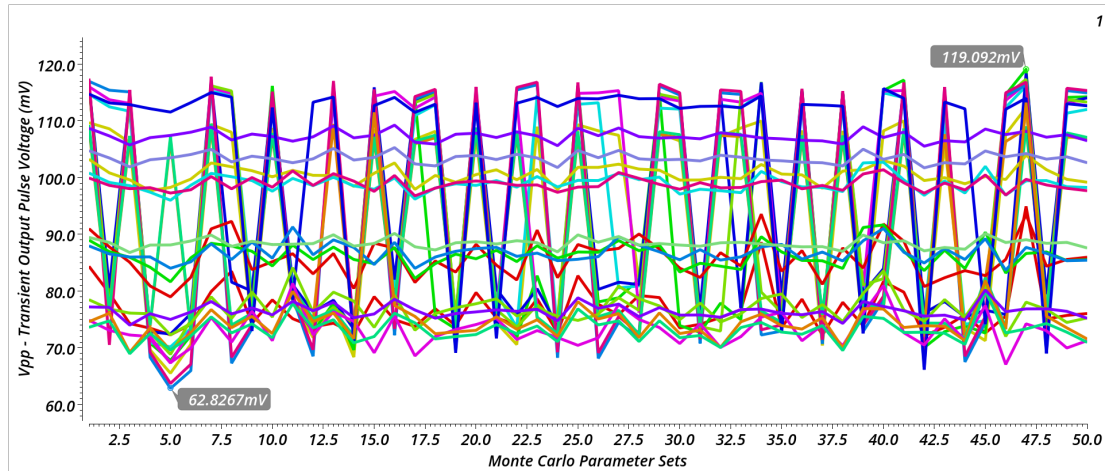


Figure 3.39 : Peak-to-peak output voltage amplitudes in the Monte Carlo tests.

To easily determine the output variation range, peak-to-peak output pulse amplitudes are calculated and plotted. Fig. 3.39 draws the output pulse V_{pp} with respect to the Monte Carlo parameter sets. Since the other parameter generates only dots on the plot and hinders understanding, the x -axis is determined as the parameter set. Since the data set is based on the border values, the gain setting change happens between the MC parameters. Still, it provides an output voltage range between 62.8 mV and 119.1 mV. Hence, the variation ratio is 1.9, corresponding to 5.56 dB. The MC simulations confirm the robustness of the proposed AGC system.



4. CONCLUSION AND FUTURE WORKS

This thesis discusses the design, implementation, and evaluation of an AGC architecture specifically developed for CMOS optical receivers. The applications of these optical receivers are designed to be involved in POF and VLC systems. Emerging technologies in this field necessitate robust front-end circuits that can effectively manage rapidly changing signal conditions while maintaining linearity, bandwidth, and signal integrity. This work details the design flow of a feedforward AGC along with its subcircuits, including the peak detector, control voltage generator for analog control, and flash ADC for digital bit control, as well as the design of the VG-TIA in the data path. The focus was not only on achieving performance specifications but also on providing robustness across process, voltage, and PVT variations to the extent possible.

The proposed AGC circuit utilizes a fully feedforward topology, effectively addressing the stability issues that can arise with feedback-based control systems. This design choice requires the peak detector to operate linearly across the entire signal range. The work presents a novel topology designed to achieve the necessary linearity, targeting an input dynamic range of 35.9 dB. The proposed peak detector offers approximately 60 dB of dynamic range, with attack and release times of 50 ns each. The overall AGC system achieves a settling time of 250 ns to maintain it under 1 μ s.

A robust VG-TIA is designed for a 1 Gbps PAM-4 optical receiver front end, utilizing adaptive transimpedance due to the aforementioned AGC system. The TIA features a hybrid transimpedance control that enhances compression performance, allowing for less than 6 dB of variation in output voltage amplitude. An inverter-based shunt-feedback TIA is implemented and further optimized through an adaptive power supply using a replica biasing LDO method.

Table 4.1 summarizes the performance of similar AGC designs. It compares the technology node, modulation and application type, AGC loop topology, data rate,

Table 4.1 : Comparison with Literature

Ref.	Technology	Modulation /Application	AGC Type	Data Rate (Gbps)	AGC Power (mW)	Dyn. Range (dB)	Settling Time (ns)
[14]	0.25 μm SiGe BiCMOS	PAM-4 / Burst Mode PON	FF+FB	50	25	15.8	82.7
[15]	0.35 μm CMOS	OOK / VLC, Burst Mode	FB	2.5	20	55	200
[16]	0.18 μm CMOS	NRZ / Burst Mode EPON	FB	1.25	43.2	24.7	1600
[17]	0.35 μm CMOS	OFDM / WLAN	FF	0.054	2.4	22	2400
This Work	65 nm CMOS	PAM-4 / POF - VLC	FF	1	2.34	35.9	250

power consumption, input dynamic range, and settling time of each work. To allow fair comparison across AGC designs, the total power in this work is calculated using only the control blocks: the PD, ADC, and CVG. This approach is commonly adopted in the literature. The VG-TIA is excluded because the power of the main circuit depends on the data rate. Increased circuit speed necessitates higher power consumption; thus, incorporating the TIA would bias the comparison. By isolating the control circuitry, the comparison becomes independent of the data rate. Based on this, the total AGC power is 2.34 mW.

The performance results in this thesis are derived from extracted layout simulations rather than silicon measurements. Consequently, although the figures are indicative and accurate, some variations may arise when fabricated samples are tested. All the referenced AGC designs in the comparison table, on the other hand, report measured results from fabricated chips, which adds significant credibility to their performance claims.

Among all the listed works, the proposed AGC achieves an excellent trade-off between power consumption and settling time. This feature highlights the strength of the fully feedforward topology, combined with an efficient CMOS implementation in 65 nm technology. While [14] operates at an impressive 50 Gbps and demonstrates strong performance in high-speed burst-mode passive optical networks (PON) systems, it

relies on a SiGe BiCMOS process, which has significantly higher power consumption. But it is reasonable for its speed class.

[15] achieves the highest dynamic range of 55 dB, making it ideal for VLC systems requiring large amplitude variation handling. However, it has a high power usage, which is 20 mW. Similarly, [16] demonstrates robustness in the burst-mode ethernet passive optical network (EPON) with a balanced 24.7 dB dynamic range but suffers from high power and slower settling. [17] excels in ultra-low power design (0.054 mW), showcasing the advantage of minimal power AGC circuits for low-throughput WLAN applications. However, it has a long settling time of 2400 ns.

In contrast, the proposed AGC stands out with a high dynamic range of 35.9 dB, a fast settling time of 250 ns, and a low power consumption of 2.34 mW, delivering an efficient operation. It achieves this performance without sacrificing linearity or robustness through its hybrid control structure and careful circuit-level optimization. This work offers a decent overall balance of speed, power, and range, thereby presenting a highly suitable alternative for compact, high-speed, and energy-aware optical receivers, such as those required in POF and VLC systems.

The AGC-TIA developed in this work is integrated into the optical receiver front end, and the prototype has been sent to production. As future work, the chip will be measured to validate the simulation results against experimental data. Furthermore, the TIA-AGC will be combined with a finely-tuned VGA and a clock-data-recovery (CDR) circuit to finalize the front end. Once these targets are accomplished, supporting higher data rates will be the next design challenge.



REFERENCES

- [1] **Tsonev, D., Videv, S. and Haas, H.** (2015). Towards a 100 Gb/s visible light wireless access network, *Optics express*, 23(2), 1627–1637.
- [2] **Dong, Y. and Martin, K.W.** (2012). A high-speed fully-integrated POF receiver with large-area photo detectors in 65 nm CMOS, *IEEE journal of solid-state circuits*, 47(9), 2080–2092.
- [3] **Dong, Y. and Martin, K.W.** (2011). Gigabit communications over plastic optical fiber, *IEEE Solid-State Circuits Magazine*, 3(1), 60–69.
- [4] **Ziemann, O., Krauser, J., Zamzow, P.E. and Daum, W.** (2013). *POF-polymer optical fibers for data communication*, Springer Science & Business Media.
- [5] **Uysal, M. and Nouri, H.** (2014). Optical wireless communications—An emerging technology, *2014 16th international conference on transparent optical networks (ICTON)*, IEEE, pp.1–7.
- [6] **Arnon, S.** (2012). *Advanced optical wireless communication systems*, Cambridge university press.
- [7] (2019). IEEE standard for ethernet amendment 9: physical layer specifications and management parameters for 1000 mb/s operation over plastic optical fiber, *IEEE Std 802.3bv-2017*, 1–140.
- [8] **Won, E.T.** (2009). *IEEE 802.15 WPAN™ Task Group 7 (TG7) Visible Light Communication*.
- [9] **Pérez, J.P.A., Pueyo, S.C. and López, B.C.** (2011). *Automatic gain control*, Springer.
- [10] **Razavi, B.** (2012). *Design of integrated circuits for optical communications*, John Wiley & Sons.
- [11] **Neuhauser, M., Rein, H.M. and Wernz, H.** (2002). Low-noise, high-gain Si-bipolar preamplifiers for 10 Gb/s optical-fiber links-design and realization, *IEEE Journal of Solid-State Circuits*, 31(1), 24–29.
- [12] **Khorramabadi, H., Tzeng, L.D. and Tarsia, M.J.** (1995). A 1.06 Gb/s-31 dBm to 0 dBm BiCMOS optical preamplifier featuring adaptive transimpedance, *Proceedings ISSCC'95-International Solid-State Circuits Conference*, IEEE, pp.54–55.

- [13] **Taylor, S.S. and Thomas, T.P.** (1994). A 2pAspl radic/Hz 622 Mb/s GaAs MESFET transimpedance amplifier, *Proceedings of IEEE International Solid-State Circuits Conference-ISSCC'94*, IEEE, pp.254–255.
- [14] **Coudyzer, G., Ossieur, P., Bauwelinck, J. and Yin, X.** (2020). A 25Gbaud PAM-4 linear burst-mode receiver with analog gain-and offset control in 0.25 μm SiGe: C BiCMOS, *IEEE Journal of Solid-State Circuits*, 55(8), 2206–2218.
- [15] **Fahs, B., Rollinson, J. and Hella, M.M.** (2022). A CMOS Fully Integrated 4×4 VLC-Compliant Receiver Array With 2.5 Gb/s per Channel, *IEEE Sensors Journal*, 23(3), 2375–2384.
- [16] **Wang, I.H. and Liu, S.I.** (2008). A 0.18- μm CMOS 1.25-Gbps Automatic-Gain-Control Amplifier, *IEEE Transactions on Circuits and Systems II: Express Briefs*, 55(2), 136–140.
- [17] **Perez, J.P.A., Calvo, B. and Celma, S.** (2009). A high-performance CMOS feedforward AGC circuit for a WLAN receiver, *IEEE Transactions on Industrial Electronics*, 57(8), 2851–2857.
- [18] **Khoury, J.M.** (1998). On the design of constant settling time AGC circuits, *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, 45(3), 283–294.
- [19] **Atef, M., Zimmermann, H., Atef, M. and Zimmermann, H.** (2016). *Optoelectronic circuits in nanometer CMOS technology*, Springer.
- [20] **Säckinger, E.** (2017). *Analysis and design of transimpedance amplifiers for optical receivers*, John Wiley & Sons.
- [21] **Razavi, B.** (2023). The design of a Transimpedance amplifier [the analog mind], *IEEE Solid-State Circuits Magazine*, 15(1), 7–11.
- [22] **Razavi, B.** (2019). The transimpedance amplifier [a circuit for all seasons], *IEEE Solid-State Circuits Magazine*, 11(1), 10–97.
- [23] **Abraham, M.** (1982). Design of Butterworth-type transimpedance and, bootstrap-transimpedance preamplifiers for fiber-optic receivers, *IEEE Transactions on Circuits and Systems*, 29(6), 375–382.
- [24] **Chen, W.Z. and Gan, R.M.** (2005). 1.8 V, variable gain transimpedance amplifiers with constant damping factor for burst-mode optical receiver, *2005 IEEE Radio Frequency integrated Circuits (RFIC) Symposium-Digest of Papers*, IEEE, pp.691–694.
- [25] **Ozkaya, I., Cevrero, A., Francese, P.A., Menolfi, C., Morf, T., Brändli, M., Kuchta, D.M., Kull, L., Baks, C.W., Proesel, J.E. et al.** (2017). A 64-Gb/s 1.4-pJ/b NRZ optical receiver data-path in 14-nm CMOS FinFET, *IEEE Journal of Solid-State Circuits*, 52(12), 3458–3473.

- [26] **Kimura, H., Aziz, P.M., Jing, T., Sinha, A., Kotagiri, S.P., Narayan, R., Gao, H., Jing, P., Hom, G., Liang, A. et al.** (2014). A 28 Gb/s 560 mW multi-standard SerDes with single-stage analog front-end and 14-tap decision feedback equalizer in 28 nm CMOS, *IEEE Journal of Solid-State Circuits*, 49(12), 3091–3103.
- [27] **Güngördü, A.D., Dündar, G. and Yelten, M.B.** (2020). A High-Performance TIA Design in 40 nm CMOS, *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp.1–5.
- [28] **Güngördü, A.D., Cömertoğlu, İ. and Yelten, M.B.** (2022). A fully-differential, flipped-voltage-follower-based (FVF) transimpedance design for optical receivers with large-area photodetectors, *Analog Integrated Circuits and Signal Processing*, 113(2), 241–248.
- [29] **Yu, T.C., Huang, W.T., Lee, W.B., Chow, C.W., Chang, S.W. and Kuo, H.C.** (2021). Visible light communication system technology review: Devices, architectures, and applications, *Crystals*, 11(9), 1098.
- [30] **Silva-Martinez, J. and Salcedo-Suner, J.** (1998). A CMOS automatic gain control for hearing aid devices, *1998 IEEE International Symposium on Circuits and Systems (ISCAS)*, volume 1, IEEE, pp.297–300.
- [31] **Steyaert, M.S., Dehaene, W., Craninckx, J., Walsh, M. and Real, P.** (1995). A CMOS rectifier-integrator for amplitude detection in hard disk servo loops, *IEEE Journal of solid-state circuits*, 30(7), 743–751.
- [32] **Yuan, F.** (2008). CMOS active inductors and transformers, *Principle, implementation, and applications*.
- [33] **Yuan, F.** (2006). Low-voltage CMOS current-mode preamplifier: Analysis and design, *IEEE Transactions on Circuits and Systems I: Regular Papers*, 53(1), 26–39.



CURRICULUM VITAE

Name SURNAME: İrem CÖMERTOĞLU

EDUCATION:

- **B.Sc.:** 2022, Istanbul Technical University - Electronics and Communication Engineering Department

PROFESSIONAL EXPERIENCE AND REWARDS:

- 2023 - Present, Research Assistant at Istanbul Technical University, Electronics and Communication Engineering Department.

PUBLICATIONS, PRESENTATIONS AND PATENTS ON THE THESIS:

- Güngördü, A. D., Cömertoğlu, İ., & Yelten, M. B. (2024, December). A High Dynamic Range CMOS Peak Detector Circuit for Feedforward Automatic Gain Control Systems, *In 2024 International Conference on Microelectronics (ICM)*. (pp. 1-6). IEEE. DOI: 10.1109/ICM63406.2024.10815711

OTHER PUBLICATIONS, PRESENTATIONS AND PATENTS:

- Güngördü, A. D., Cömertoğlu, İ., & Yelten, M. B. (2022). A fully-differential, flipped-voltage-follower-based (FVF) transimpedance design for optical receivers with large-area photodetectors. *Analog Integrated Circuits and Signal Processing*, 113(2), 241-248.
- Kirğil, H., Güngördü, A. D., Cömertoğlu, İ., & Yelten, M. B. (2024, December). A High-Linearity Constant-Bandwidth PVT-Tolerant 10 Gbps PAM-4 Inverter-Based Compact VGA. *In 2024 International Conference on Microelectronics (ICM)* (pp. 1-6). IEEE. DOI: 10.1109/ICM63406.2024.10815820.