ISTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

NEW TUNABLE LINEAR CURRENT MIRRORS

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FORWORD

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JUNE 2006 **Umut GÜVENÇ**

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NEW TUNABLE LINEAR CURRENT MIRRORS

SUMMARY

New tunable linear current mirror topologies are proposed as an alternative to the recently used tunable devices which are required in analog electronic systems, especially in filtering applications and which high performances can not be obtained by using commonly used techniques. It is thought that the proposed structures would find a very wide application areas since current mirrors are the mail building blocks of active components.

The first of the proposed tunable current mirror structures is realized with triode MOSFETs. In this structure, the input and output currents of the current mirror is converted to voltage levels on the equivalent resistances of triode MOSFETs and these voltage levels are equalized by an operational amplifier in negative feedback configuration. By changing the equivalent resistances of the triode MOSFETs, the ratio between the input and output currents is tuned. According to the results of the simulations run on this structure it is seen that the gain of the current mirror can be changed 4 times and for an input current range from 1uA to 100uA the total harmonic distortion (THD) of the circuit stays below 2%.

Although the second proposed tunable current mirror structure also contains triode MOSFETs, the resistivities of these MOSFETs are kept constant and the gain control is not achieved by using these MOSFETs. The input and output currents of the circuit are converted to voltage levels on the constant resistances of the triode MOSFETs and then by being multiplied with a controlled coefficients which are supplied by two separate variable gain amplifiers (VGA) are equalized to each other by the opamp in negative feedback configuration. By using simple VGA structures of which gains can be controlled from 1 to 3, the gain of the current mirror is controlled 9 times the circuit can satisfy a linearity of 2% THD within the range from 10uA to 100uA.

Another proposed tunable current mirror structure is realized with BJT differential pairs. In this structure, the input and output currents of the circuits is applied to two

separate differential pairs as tail currents and by changing the input voltages of the differential pairs the ratio at which the currents are divided is arranged. By equalizing the input and output currents divided with different ratios and converted to voltage levels on similar diodes, the gain of the current mirror is controlled. By using the linear transition characteristic of the BJT differential pair, the circuit can operate linearly within a very wide gain range. According to the simulations results, a gain tuning range of 5 decades for 2 decades of input current range is achieved with THD below 0.5%.

The last proposed tunable current mirror structure has the advantage of simplicity and low power consumptions among others. This architecture has been thought as the simplified form of the third proposed tunable current mirror structure. Input current is applied to the one of the branches of the single BJT differential pair present in the circuit and the ratio between two brunches of the differential pair is controlled by the voltage applied to the inputs of the differential pair. The MOSFET supplying the tail current of the differential pair is biased with a feedforward configuration to assure to steer the desired current. The simulations run on this circuit shows that the gain of the current mirror can be tuned 5 decades within an input current range of 2 decades with THD below 1%.

As an application to the tunable current mirrors, an electrically controllable second generation current conveyor (ECCII) circuit is designed with the fourth proposed tunable current mirror structure. The results similar to the previously run simulations were obtained from the simulations run on the ECCII circuit. The current gain of the ECCII circuit can be tuned 4 decades linearly.

YENI AYARLANABILIR DOGRUSAL AKIM AYNALARI

ÖZET

Analog elektronik sistemlerinde, özellikle filtreleme uygulamalarinda ihtiyaç duyulan ve yaygin olarak kullanilan tekniklerle yüksek performans elde edilemeyen ayarlanabilir yapilara alternatif olarak yeni ayarlanabilir dogrusal akim kaynagi yapilari önerilmistir. Akim aynasi yapilarinin aktif devre bloklarinin en temel yapitasi olmasi nedeniyle önerilen yapilarin çok genis bir uygulama alani bulacagi düsünülmüstür.

Önerilen yeni ayarlanabilir akim aynasi yapilarindan ilki dogrusal bölgede çalistirilan MOSFET'ler kullanilarak gerçeklestirilmistir. Bu yapida, akim aynasinin giris ve çikis akimlari dogrusal bölgedeki MOSFET'lerin esdeger iletimdirençleri üzerinde gerilim degerlerine dönüstürülerek, islemsel kuvvetlendiricili bir negatif geribesleme sayesinde bu iki gerilim birbirine esitlenmekterdir. Akim degerlerinin gerilim seviyelerine dönüstürüldü esdeger MOSFET dirençleri degistirilerek giris ve çikis akimlari arasindaki oran ayarlanabilmektedir. Yapilan benzetimlerde akim aynasinin kazanci 4 kat kontrol edilebilmistir ve 1uA ile 100uA arasinda toplam harmonik bozulmasinin (THD) %2'nin altinda kaldigi gözlenmistir.

Ikinci ayarlanabilir akim aynasi yapisi da içerisinde dogrusal bölgede çalisan MOSFET'ler içermesine ragmen bu MOSFET'lerin iletin dirençleri sabit tutulmustur ve kazanç ayari bu MOSFET'ler üzerinden yapilmamaktadir. Devrenin giris ve çikis akimlari sabit MOSFET dirençleri üzerinde gerilime çevrilerek bu gerilimler iki ayri kazanci kontrol edilebilir kuvvetlendirici (VGA) kullanilarak kontrol edilebilen katsayilarla çarpilip, daha sonra islemsel kuvvetlendiricili bir negatif geribesleme ile birbirlerine esitlenmektedir. Kazanci 1 ile 3 arasinda degisebilen basit VGA yapilari kullanilarak yapilan benzetimlerde akim aynasinin kazanci 9 kat ayarlanabilmis ve 10uA ile 100uA giris akimi araliginda devrenin %2'den daha küçük bir THD ile çalistigi görüsmüstür.

Ayarlanabilir akim aynasi olarak sunulan bir diger yapi bipolar (BJT) transistorlardan olusan uzun kuyruklu devreler kullanilarak gerçeklestirilmistir. Bu

yapida devrenin giris ve çikis akimlari iki ayri uzun kuyruklu devrenin kuyruk akimi olarak uygulanmis ve bu uzun kuyruklu devrelerin giris gerilimleri degistirilerek akimlari hangi oranlarda bölünerek kollardan akacaklari ayarlanmaktadir. Degisik oranlarda bölünerek akan giris ve çikis akimlari birbirine es dirençler üzerinde gerilime çevrilerek islemsel kuvvetlendirici yardimi ile birbirlerine esitlenmektedirler. BJT uzun kuyruklu devrenin dogrusal geçis karakteristigi sayesinde oldukça genis bir kazanç araliginda devre dogrusal olarak çalisabilmektedir. Yapilan benzetimlerde 5 dekatlik kazanç ayarlama islemi 2 dekatlik bir giris akimi araliginda %0.5'den daha küçük THD degerleri ile gerçeklenebilmektedir.

Son olarak önerilen ayarlanabilir akim aynasi basit yapisi ve düsük güç tüketimi ile dikkat çekmektedir. Bu yapi üçüncü ayarlanabilir akim aynasi yapisinin sadelestirilmis hali olarak düsünülmüstür. Yapida bulunan tek BJT'li uzun kuyruklu devrenin kollarindan birine giris aki uygulanmaktadir ve uzun kuyruklu devrenin girislerine kontrol gerilimi uygulayarak iki kol arasinda akim orani ayarlanmkatadir. Uzun kuyruklu devrenin kutuplama akimini saglayan MOSFET ise basit bir negatif ileribesleme sayesinde gerekli akimi akitabilmektedir. Bu devre ile yapilan benzetim sonuçlarinda 5 dekatlik kazanç araligi 2 dekatlik giris akimi araliginda %1'den daha küçük THD degerleri ile elde edilebilmistir.

Dördüncü olarak önerilen ayarlanabilir akim aynasi kullanilarak uyuglama olarak gerçeklestirilen elektriksel olarak control edilebilir ikici nesil akim tasiyici (ECCII) devresinin benzetim sonuçlarinda da daha önce elde edilen sonuçlara uygun sonuçlar elde edilmistir. Tasarlanan ECCII devresinin akim kazanci 4 dekatlik genis bir aralikta dogrusal olarak ayarlanabilmistir.

1. INTRODUCTION

Designing analog electronic systems, which have still well established place in electronic systems and which are the mandatory interfaces between the analog world and digital systems, is usually the bottle neck on the performance of the system. Although, highly controllable and scalable digital systems take the place of analog devices in many cases, there are many applications of which examples are filtering in analog to digital converters and digital to analog converters, high speed direct signaling systems, read channel of disk drives and applications where the low power consumption is required [1]. Despite the easily configurability and controllability of the digital counterparts, analog systems generally have the disadvantage of less flexibility and more dependency on process parameters and other environmental conditions. To improve the configurability and reduce the dependency to the uncontrollable parameters of the analog systems, tunable devices are always needed and implemented in the analog design. Using such tunable devices supply the ability to control some important system parameters and give the chance to fine tune the effects of unwanted environmental conditions and variations of process parameters on analog systems [1].

Most common application of tuning in analog devices is the continuous-time filters, at which the tunable devices are used to adjust or to fine tune the important frequencies of the filter to desired values [2]. Continuous-time filters commonly use transconductance in transconductance-capacitor (Gm-C) filters, triode mosfets in mosfet-capacitor filters and X terminal resistance in second generation current conveyor-capacitor filters as tuning devices and usually suffer from nonlinearities of these tunable devices [1]. Tunable current mirror structures have advantages of lower power consumption, smaller operating voltage and potentially higher bandwidth with respec to other tunable devices [3].

Thus, to ease the controlability problem in analog systems by bettering the methods of tuning is aimed and new tunable current mirrors are introduced as an alternative to

the commonly used tunable devices. Using current mirrors as tunable devices supply the advantage of simplicity in design and in implementation and having a wide area of use since the current mirrors are the main building blocks of almost all analog active blocks. Besides, the performances of the current-mode structures which are getting more preffered because of their wider bandwith, mainly consists of current mirrors thus felxible and high performance current-mode structures can be constructed with new tunable current mirrors [4]. The new tunable linear current mirror topologies of which design and simulations are given in this work have wider ranges of tunability and operation range while the linearity performances are also better.

2. PROPOSED TUNABLE CURRENT MIRROR STRUCTURES

In this section, four proposed new tunable linear current mirror architectures are introduced and the top-down design of these architectures is also explained. The simulations results giving the performances of these architectures are shown. Schematics of all of the circuits are constructed in the Pspice design environment with standard 0.5µm level 3 CMOS process parameters. Both the MOSFET parameters for this technology and the parameters used for the simulation of the BJT transistors were given in the Appendix.

2.1 Tunable Current Mirror with Triode MOSFETs

The first proposed tunable current mirror architecture conceptual circuit is shown in Figure 2.1. This circuit mainly consists of triode region MOSFET transistors at the input and output of the circuit, and an operational amplifier block which is responsible of equalizing the voltage drop on output triode transistors to voltage drop on input triode transistors. Tuning of the current mirror gain in this architecture is done by changing the equivalent resistances of input or output triode transistor blocks by controlling the gate voltage of one parallel triode transistor in each block. M2 transistor in this schematic is used as a current buffer to satisfy constant input resistance and voltage level. Although it is seen that the gate terminal of this transistor is connected to the ground potential in the schematic shown in Figure 2.1, it can be connected to any other voltage level to supply the desired input voltage level. Since the input current is applied to the source terminal of the M2 transistor and since the gate terminal of the M2 transistor is connected to the ground potential, the input resistance and the input voltage level of this current mirror is similar with the basic current mirror. M1 transistor works as a source degenerated super transistor with the opamp feedback, so satisfies a very high output resistance [5].

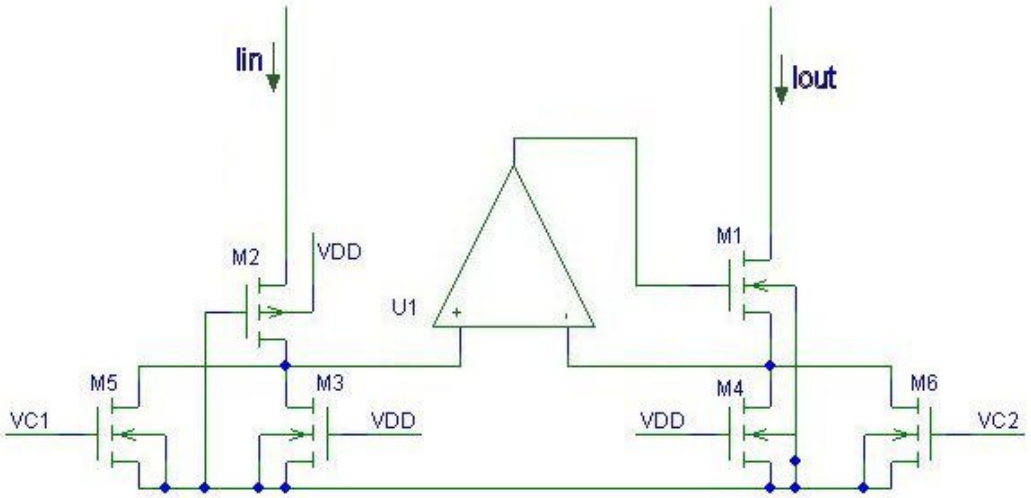


Figure 2.1 : The conceptual circuit schematic of the tunable current mirror with triode MOSFETs.

Input current flowing through the triode transistors M3 and M5 generates a voltage drop and the operational amplifier with negative feedback tries to generate the same voltage drop on the triode transistors M4 and M6 at the output by controlling the gate voltage of M1 transistor. Any instantaneous change of the voltage on M3 and M5 results in a change of the gate voltage of M1 causing the voltage drop on M4 and M6 to change in the same direction. Similarly, any instantaneous change of the voltage drop on M4 and M6 results in a change in the gate voltage of M1 in the opposite direction and compensates this change. Therefore, the output current of the current mirror which is generated on the output triode transistors precisely follows the input current.

Tuning of the circuit is achieved by separately controlling the total equivalent resistance of the parallel triode transistors at the input and output. When all the $\frac{W}{L}$ ratios of the triode transistors are selected to be same, the equivalent resistances of input triode transistors and output triode transistors change from R to $\frac{R}{2}$ while the control voltages V_{C1} and V_{C2} change from V_{TH} to V_{DD} respectively, where V_{TH} is the threshold voltage of triode transistors, V_{DD} is the supply voltage and the R is used for the equivalent resistance of one triode transistors of which gate voltage is V_{DD}. Thus, the gain of the current mirror is defined by the ratio of these equivalent resistance

values as shown in Equation 2.2a and Equation 2.2b since the equivalency of the voltages on input and output triode transistors are guaranteed by the opamp connected in negative feedback. Here, R_{X1} and R_{X2} are used to show the equivalent resistance of M5 and M6 respectively and the constant resistance R shows the resistance of M3 and M4 transistors. The value of the triode MOSFET resistance is defined by Equation 2.1 which is evaluated from the voltage-current equation of triode MOSFETs [5]. Keeping the two control voltages equal will obviously result in a current mirror gain of 1.

$$R_{on} = \frac{1}{m_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \tag{2.1}$$

$$\frac{I_{out}}{I_{in}} = \frac{R // R_{X1}}{R // R_{X2}} \tag{2.2a}$$

$$\frac{I_{out}}{I_{in}} = \frac{R_{X1}(R + R_{X2})}{R_{X2}(R + R_{X1})} \tag{2.2b}$$

By replacing Equation 2.1 in Equation 2.2b, gain equation according to the component parameters is obtained. This gain equation is given in Equation 2.3a. Equation 2.3b shows the simplified form of the gain equation when the dimensions of the constant resistance triode transistors M3 and M4 are selected to be same.

$$\frac{I_{out}}{I_{in}} = \frac{\frac{W_4}{L_4}\left(\frac{W_3}{L_3}(V_{DD} - V_{TH}) + \frac{W_6}{L_6}(V_{C2} - V_{TH})\right)}{\frac{W_3}{L_3}\left(\frac{W_4}{L_4}(V_{DD} - V_{TH}) + \frac{W_5}{L_5}(V_{C1} - V_{TH})\right)} \tag{2.3a}$$

$$\frac{I_{out}}{I_{in}} = \frac{\frac{W}{L}(V_{DD} - V_{TH}) + \frac{W_6}{L_6}(V_{C2} - V_{TH})}{\frac{W}{L}(V_{DD} - V_{TH}) + \frac{W_5}{L_5}(V_{C1} - V_{TH})} \tag{2.3b}$$

When the $\frac{W}{L}$ ratios of M5 and M6 transistors are selected to be the same with M3 and M4, RX1 and RX2 resistivities take values from R to infinity. The gain equation shown in Equation 2.2b can be reduced to simple gain equations shown in Equation 2.4a and Equation 2.4b which are dependent to only one of the variable resistances by lowering the control voltage of one of M5 and M6 transistor below the threshold voltage and making its resistivity high enough to ignore.

$$\frac{I_{out}}{I_{In}} = 1 + \frac{R}{R_{X2}}, \qquad R_{X1} >> R \tag{2.4a}$$

$$\frac{I_{out}}{I_{In}} = \left(1 + \frac{R}{R_{X1}}\right)^{-1}, \qquad R_{X2} >> R \tag{2.4b}$$

When minimum values of the variable resistances RX1 and RX2 are selected to be R, same with the resistivity of M3 and M4, the gain of the current mirror can be tuned from 0.5 to 2. By selecting the $\frac{W}{L}$ ratios of M5 and M6 greater than the $\frac{W}{L}$ ratios of M3 and M4, the minimum value of RX1 and RX2 resistances can be made smaller than R and the tuning range can be widen.

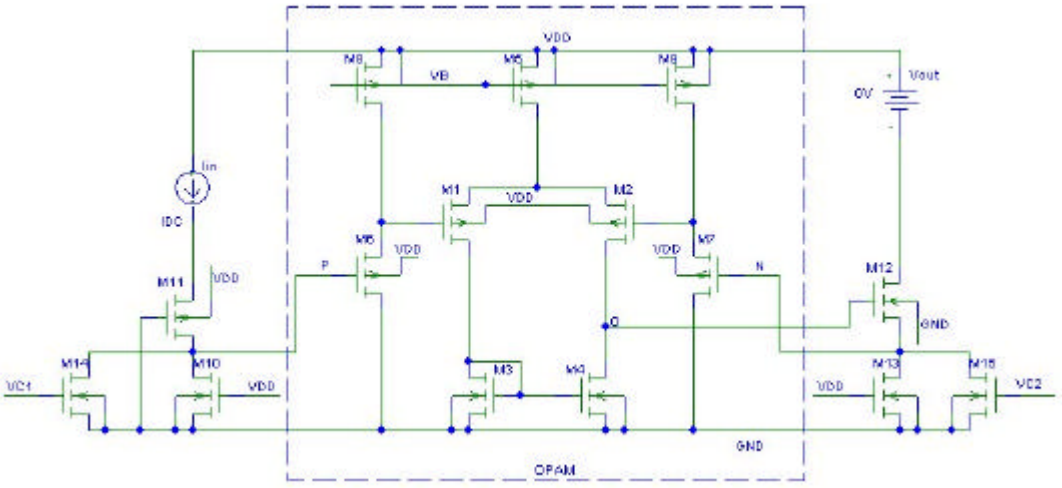


Figure 2.2: The realization of the tunable current mirror with triode MOSFETs.

In Figure 2.2, the realization of the tunable current mirror with a single stage differential amplifier is shown. Since the equivalent resistance value for both input and output triode transistors is very low, the voltage occurring on these transistors due to input and output currents is also very low. Because of this low common mode voltage level at the inputs of the differential pair the output swing of the opamp becomes narrow thus level shifter stages are used in front of the inputs of the amplifier to satisfy an operable common mode level for supplying a wide input voltage swing for M12. Also extra attention should be given to the dimensioning of the M11 transistor. The $\frac{W}{L}$ ratio of this transistor must be high enough to guarantee the operation of this transistor to take place in saturation region.

Table 2.1: Transistor dimensions of tunable current mirror with triode MOSFETs.

Transistors	**W [µm]**	**L [µm]**
M1, M2	46	2
M3, M4	10	2
M6, M7	46	1
M5, M8, M9	46	1
M11	46	0.5
M12	100	0.5
M10, M13, M14, M15	10	0.5

The simulations of the circuit shown in Figure 2.2 were made with 0.5µm standard CMOS process parameters. Transistor dimensions are given in Table 2.1. Calculation of the M10 and M13 triode transistor dimensions were made by taking highest allowable common mode voltage level of the opamp into consideration. Selecting a small $\frac{W}{L}$ ratio for the triode transistors would result in high voltage drops on these transistors while operating with high input currents and cause the opamp not to operate correctly. Determination of the dimensions of the M14 and M15 triode

transistors were made according to the desired controllable gain range. The resultant graphic of the simulation made to show the change of the equivalent resistance of input and output triode transistors according to control voltages is shown in Figure 2.4 and the schematic used for this simulation is shown in Figure 2.3.

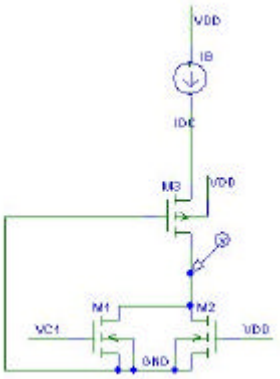


Figure 2.3: The schematic used for the simulation of the change of total equivalent resistance of the parallel triode MOSFETs.

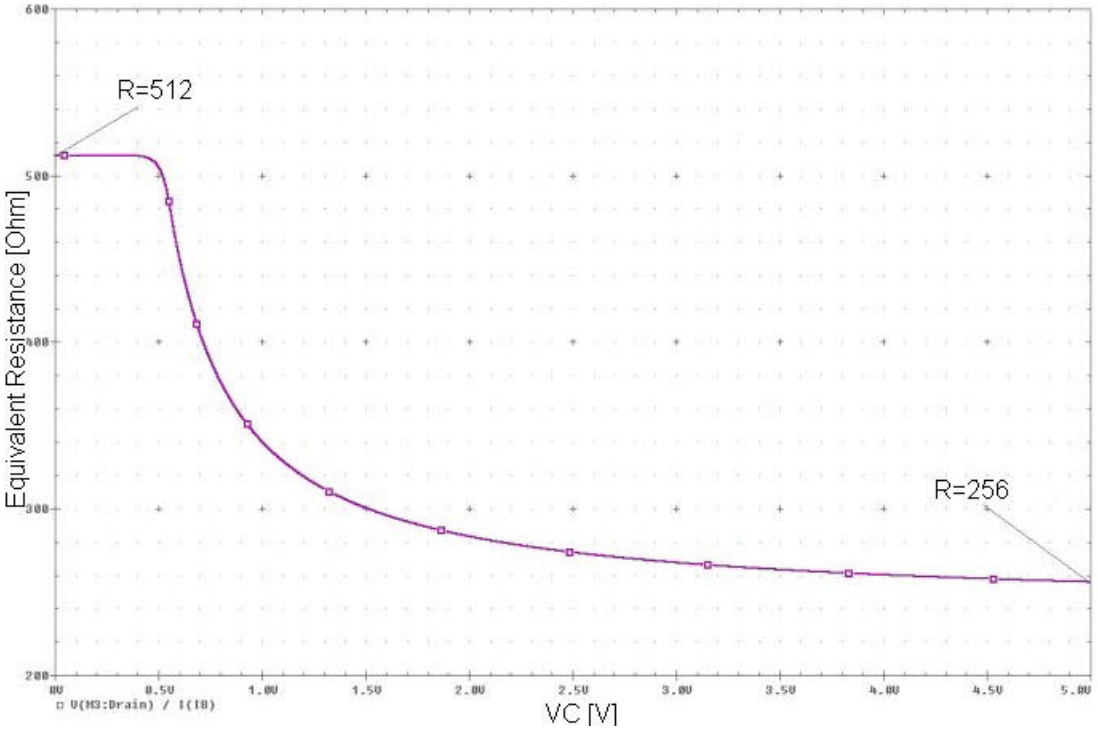


Figure 2.4: The change of the total equivalent resistance of the parallel triode MOSFETs.

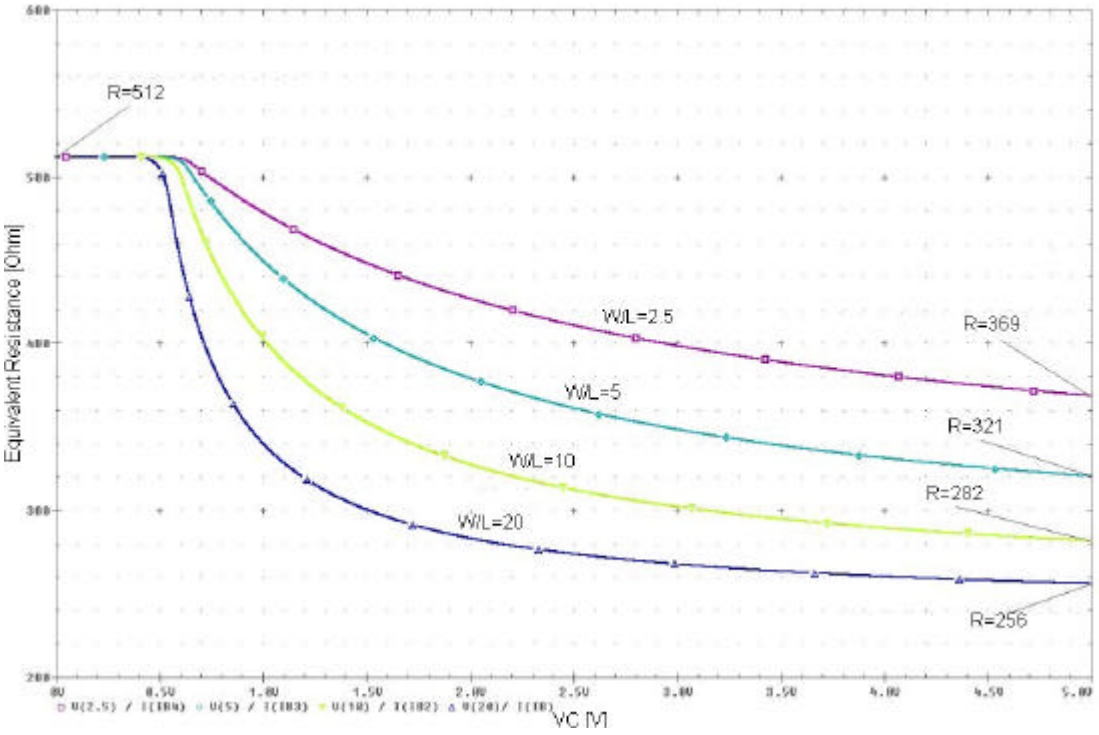


Figure 2.5: Affect of the W/L ratio of the controlled triode MOSFET over the total equivalent resistance.

As it can be seen from the graphic shown in Figure 2.4, the equivalent resistances at the input and the output of the mirror change from 512 ? to 256 ? according to the control voltage. The resistivity curve shown in Figure 2.4 can be flattened and the gain control of the current mirror can be made more linear by selecting a smaller $\frac{W}{L}$ ratio for triode transistors working as variable resistances as shown in Figure 2.5. However, this makes the gain control range narrower since minimum the equivalent parallel resistance gets higher as the $\frac{W}{L}$ ratio gets smaller.

2.1.1 Operational Amplifier

Although a high performance opamp helps to increase the accuracy of the current mirror, such a design would suffer from complexity, stability problems and bandwidth limitation. Thus, a single stage differential amplifier was used to realize the circuit and spent effort to raise the performance specs of this simple architecture. To increase the gain of the opamp, the biasing current of the differential amplifier was selected low (1µA) and to increase the output resistance of the opamp the

channel length (L) of the M1, M2, M3 and M4 transistors are selected high (2µm). This simple opamp circuit was simulated with the given transistor dimensions in Table 2.1 and the resultant AC response of the circuit was given if Figure 2.6. It can be seen from the AC simulation output graphic (Figure 2.6) that the low frequency gain of the opamp is 67 dB, bandwidth is 561 KHz and the unity gain frequency is 610 MHz. Since this single stage amplifier has only one high impedance node on the signal line, it has no stability problem. The output phase curve plotted in the graphic in Figure 2.7 shows the phase shift of the amplifier at the unity gain frequency. According to this simulation result the maximum phase shift of the circuit is approximately 120 degrees and the phase margin of the circuit is 60 degrees.

As mentioned previously, the equivalent resistance at the input and output of the current mirror is minimum 256? so the input and output currents flowing through these resistances generate very low voltages at the inputs of the amplifier. The voltage level shifter stages at the both inputs of the amplifier are used to satisfy the normal operation of the amplifier at these common mode voltage levels. The DC simulation result shown in Figure 2.8 shows change of the transconductance (gm) of the differential pair according to the input common mode voltage. It can be observed that the operation range for the input common mode voltage level is between 0V and 3.3V.

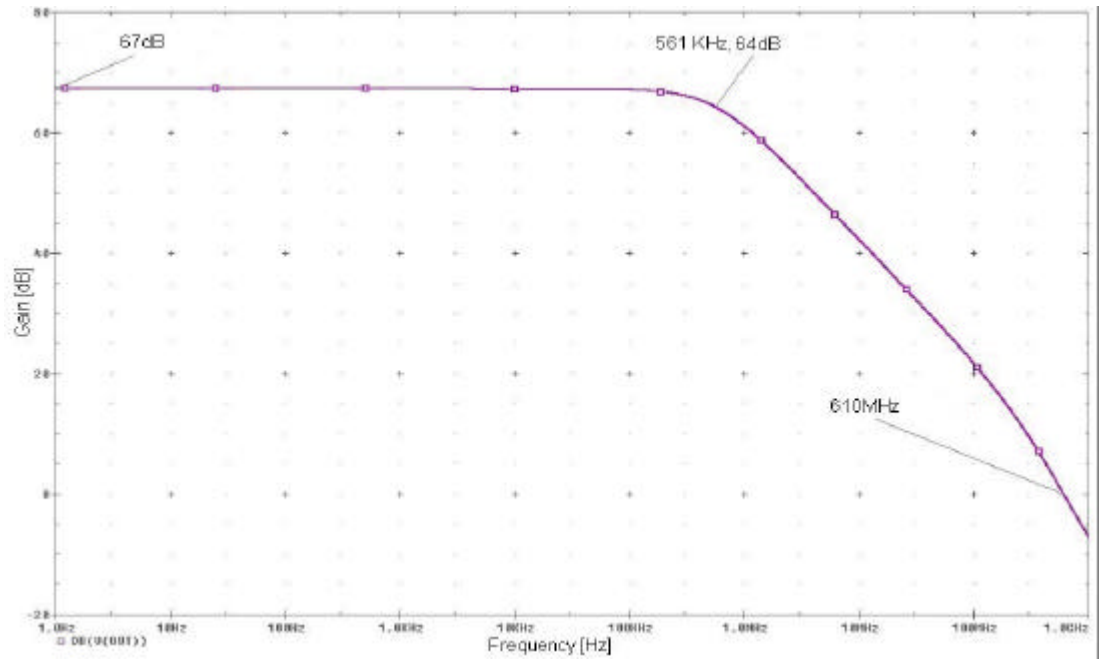


Figure 2.6: AC response of the single stage opamp.

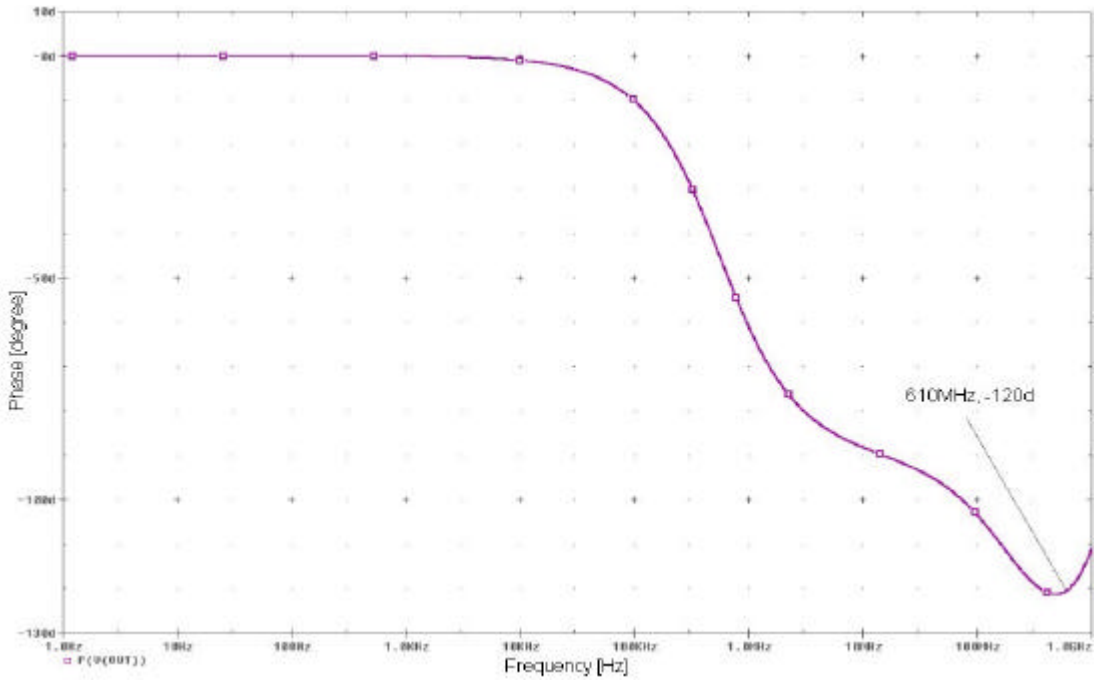


Figure 2.7: Phase response of the single stage opamp.

The swing range of the opamp is obtained from the simulation result given in Figure 2.9. This graphic shows the DC transition of the output of the circuit. According to this graphic output of the circuit can approximately vary from 100mV to 2.8V linearly.

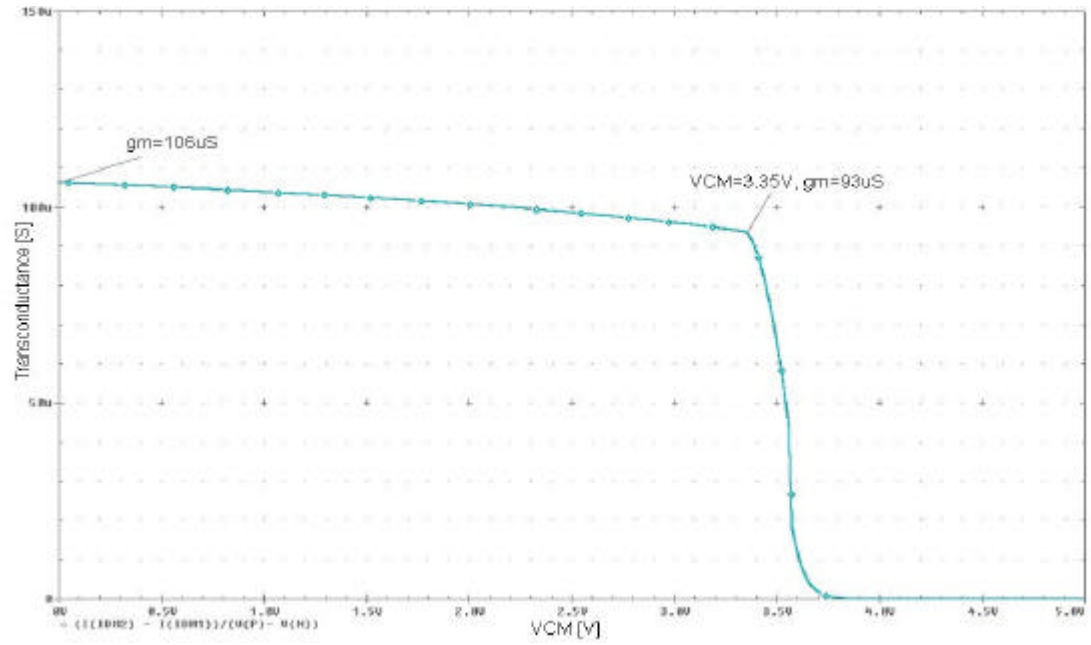


Figure 2.8: The change of the transconductance of the single stage opamp according to the input common mode voltage.

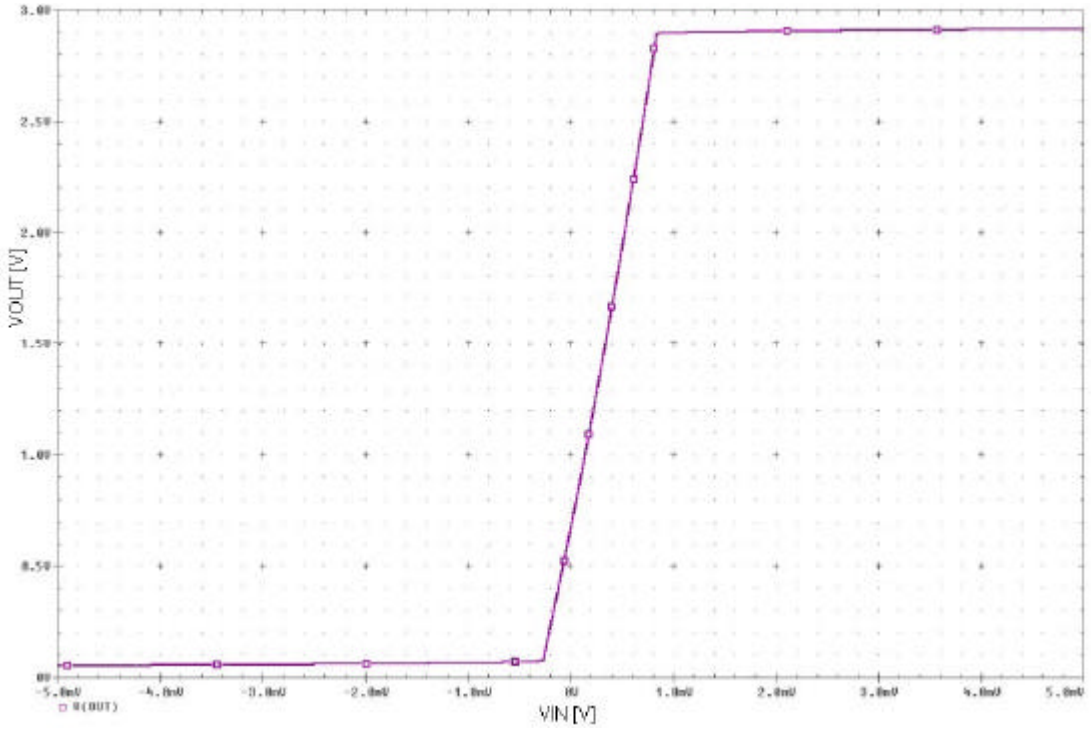


Figure 2.9: DC sweep simulation result of the opamp.

Figure 2.10 shows the change of the output resistance of the opamp according to the frequency. The output resistance value for the in band frequencies is 22M?. Expectedly, the output resistance of the opamp decreases at high frequencies like the gain of the circuit.

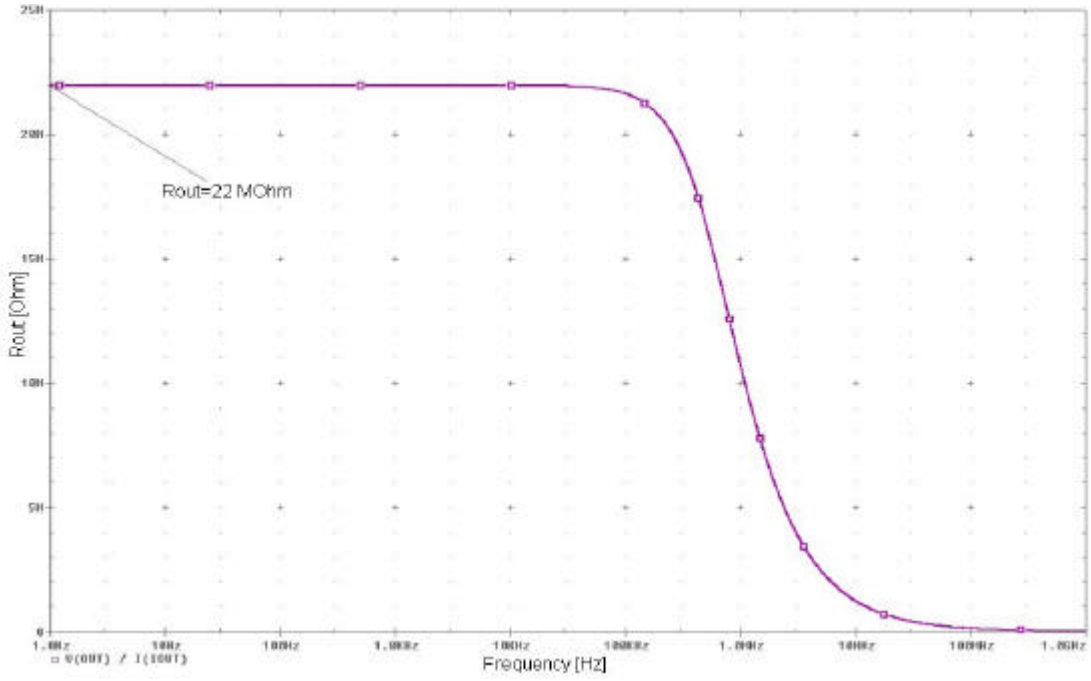


Figure 2.10: The output resistance of the opamp.

2.1.2 Simulations

Later simulations were run on the whole tunable current mirror circuit shown in Figure 2.2. The first graphic shown in Figure 2.11 was plotted to show the change of gain according to the control voltage V_{C1}. In this simulation output, second control voltage is kept constant at ground potential. In this case, as previously stated by Equation 2.2b, the variable resistance R_{X1} at the input of the circuit varies from open circuit to 512? and the equivalent resistance changes from 512? to 256? as the control voltage increases from V_{TH} to V_{DD}. Therefore, by evaluating Equation 2.2b it is found out that the gain of the circuit is controlled between 0.5 and 1. The change of the gain with second control voltage V_{C2} is given in Figure 2.12 in which it can be seen that the gain is controllable from 1 to 2. This gain range can be easily evaluated from the Equation 2.2a which is the simplified form of the total gain equation (Equation 2.1) where the condition is R_{X2}>>R.

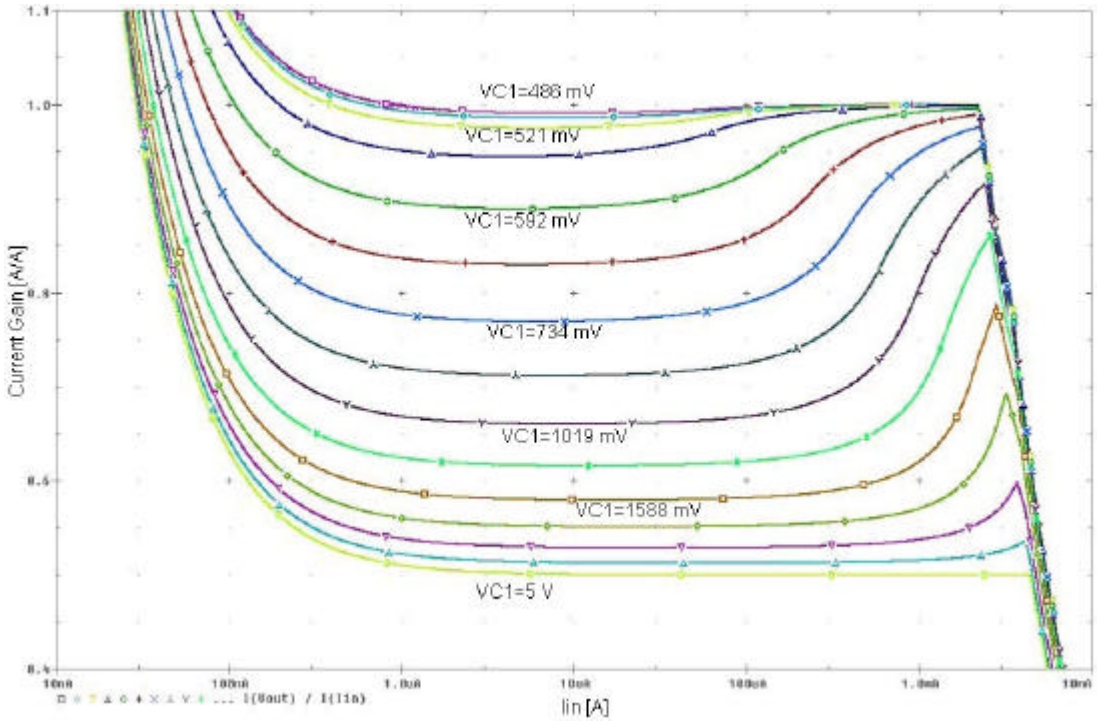


Figure 2.11: The change of the gain of the tunable current mirror with triode MOSFETs for different V_{C1} values.

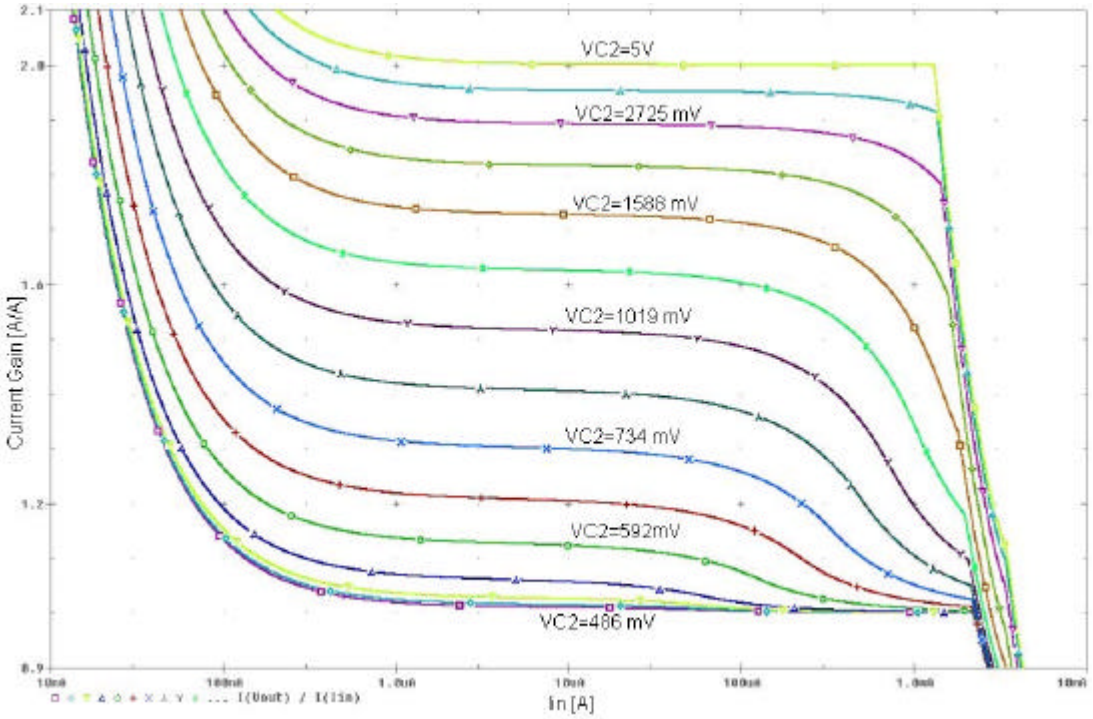


Figure 2.12: The change of the gain of the tunable current mirror with triode MOSFETs for different V_{C2} values.

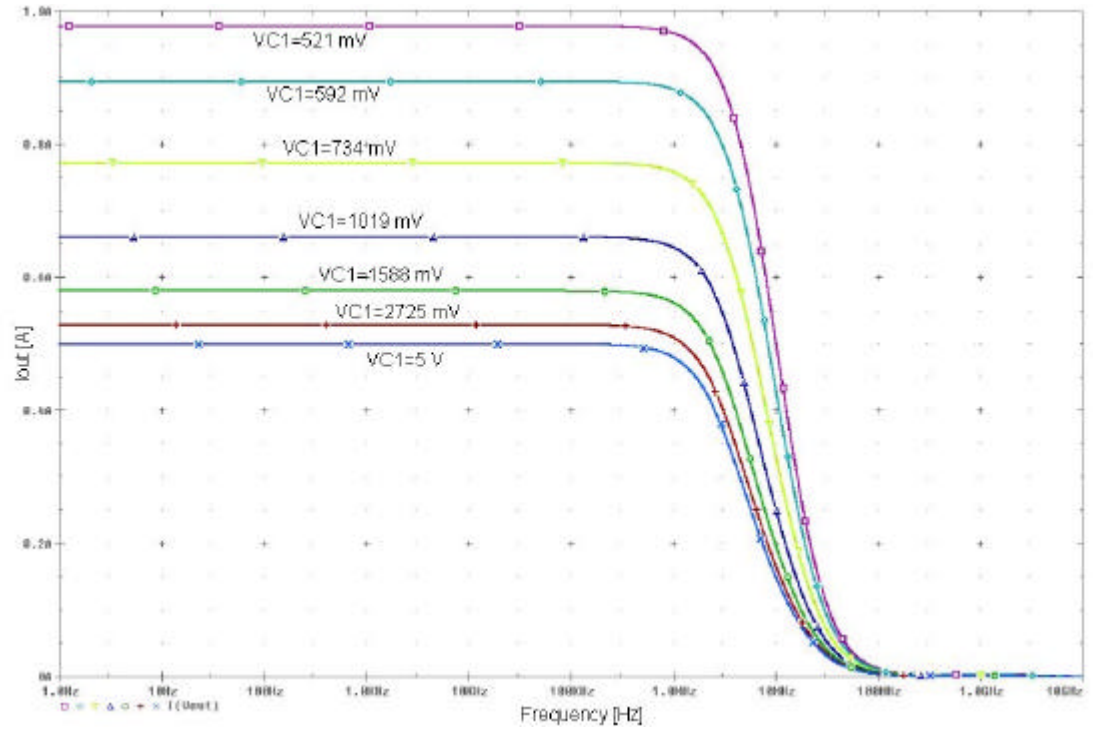


Figure 2.13: AC simulation result of the tunable current mirror with triode MOSFETs for different V_{C1} control voltage values.

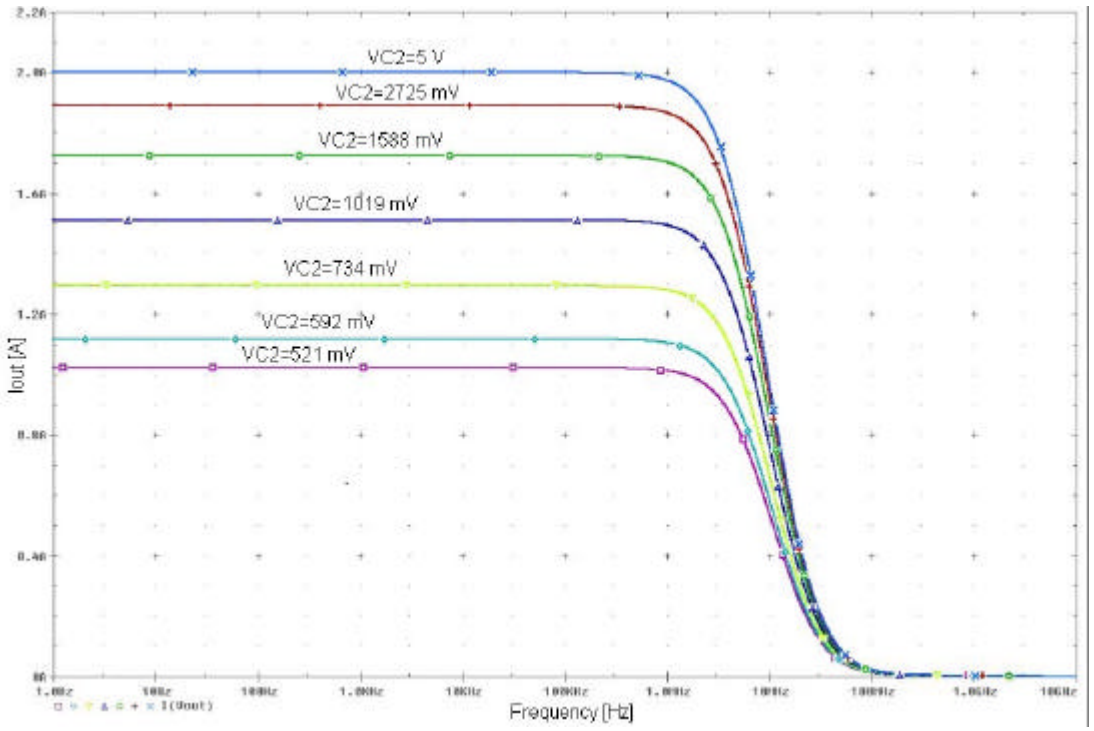


Figure 2.14: AC simulation result of the tunable current mirror with triode MOSFETs for different V_{C2} control voltage values.

The AC simulation resultant graphics for different values of V_{C1} and V_{C2} control voltages are shown in Figure 2.13 and Figure 2.14 respectively. When the circuit schematic given in Figure 2.2 is evaluated it is seen that the stability of the current mirror is independent from the current gain. It is seen in this schematic that the opamp in the current mirror topology is used with unity gain feedback so the stability of the current mirror is determined by the stability of the opamp of which AC simulation results were given in Figure 2.6 and 1.7. According to these simulations results the gain bandwidth (GBW) of the circuit is 6.4 MHz which is the frequency where the gain decreases to $\frac{1}{\sqrt{2}}$ times its value when the gain is unity.

Another simulation made on the tunable current mirror circuit is transient simulation where a 10 KHz sinusoidal current with 49.5µA amplitude and 50.5µA DC offset was applied to the input of the circuit to show the linearity of the circuit within the current range between 1µA and 100 µA.

Table 2.2: THD values of the tunable current mirror with triode MOSFETs, for the simulation made by changing V_{C1}.

V_{C1} (mV)	THD (%)
521	0.38
592	1.12
734	0.71
1019	0.39
1588	0.18
2725	0.12
5000	0.14

Table 2.3: THD values of the tunable current mirror with triode MOSFETs, for the simulation made by changing V_{C2}.

V_{C2} (mV)	THD (%)
521	0.39
592	1.17
734	0.92
1019	0.54
1588	0.27
2725	0.09
5000	0.06

The resultant graphics shown in Figure 2.15 and Figure 2.16 are obtained by changing the V_{C1} and V_{C2} control voltages from 450mV to 5V respectively while holding the other control voltage at ground potential. Thus, the graphic shown in Figure 2.12 shows the change of the gain from 0.5 to 1 and the graphic shown in Figure 2.15 shows the change of the gain from 1 to 2.

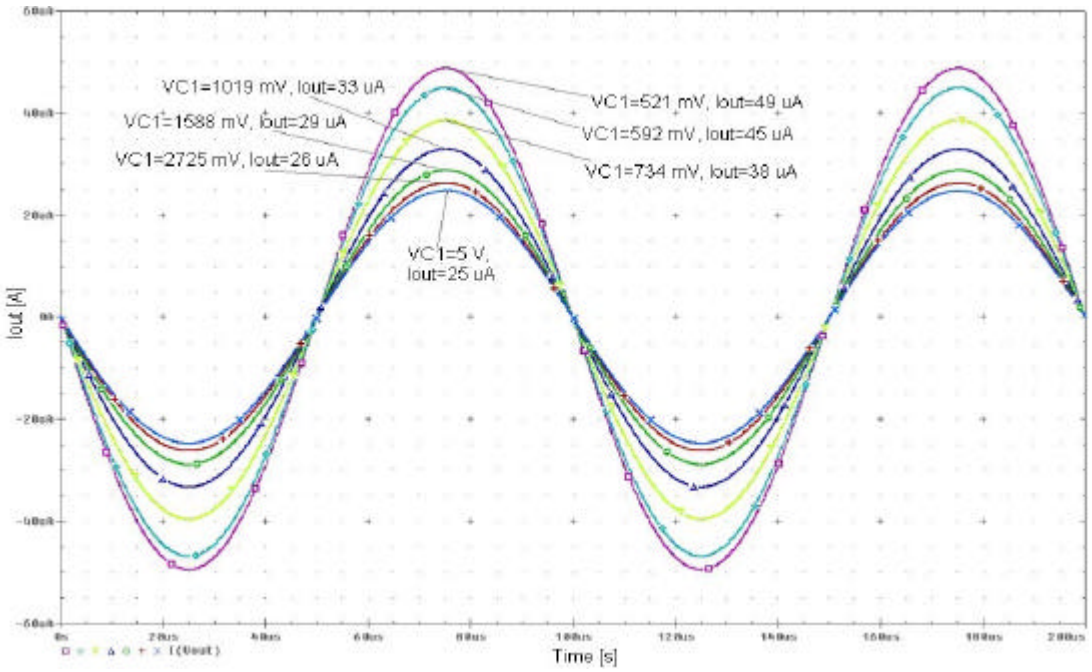


Figure 2.15: The result of the transient simulation run on the tunable current mirror with triode MOSFETs by changing V_{C1}.

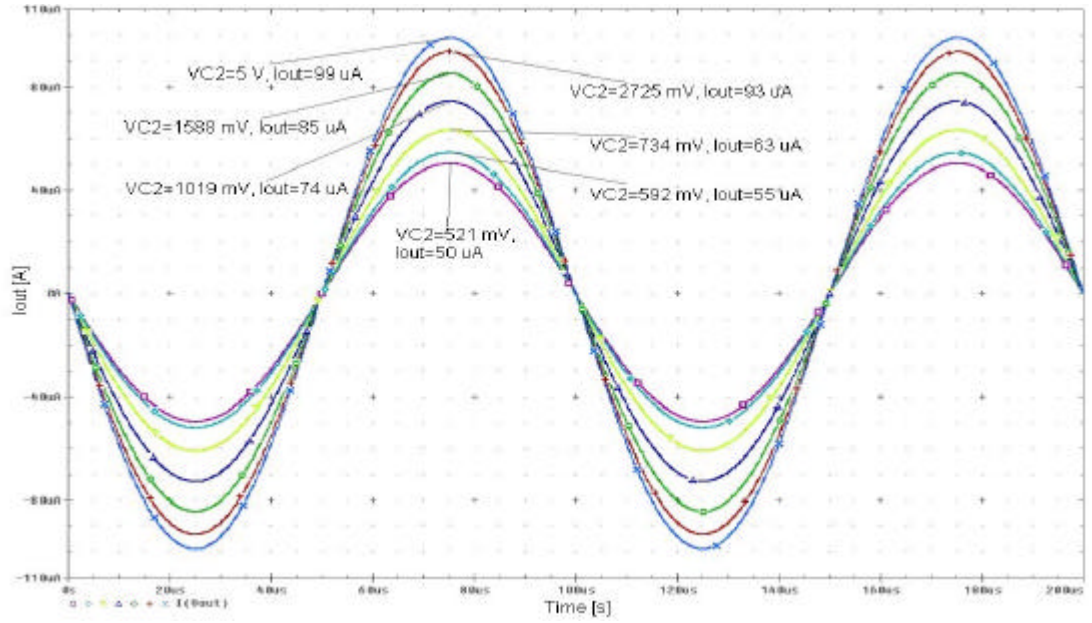


Figure 2.16: The result of the transient simulation run on the tunable current mirror with triode MOSFETs by changing V_{C2}.

To cancel the DC current the configuration shown in Figure 2.17 was made. In this configuration, the same DC offset voltage was applied to an exact replica of the tunable current mirror and the DC part of the output current was subtracted from the

total current. According to the simulation results the total harmonic distortion (THD) of both situations are roughly within 1.5% for a current sweep range of two decades. The corresponding THD values to the applied control voltages are given in Table 2.2 and Table 2.3.

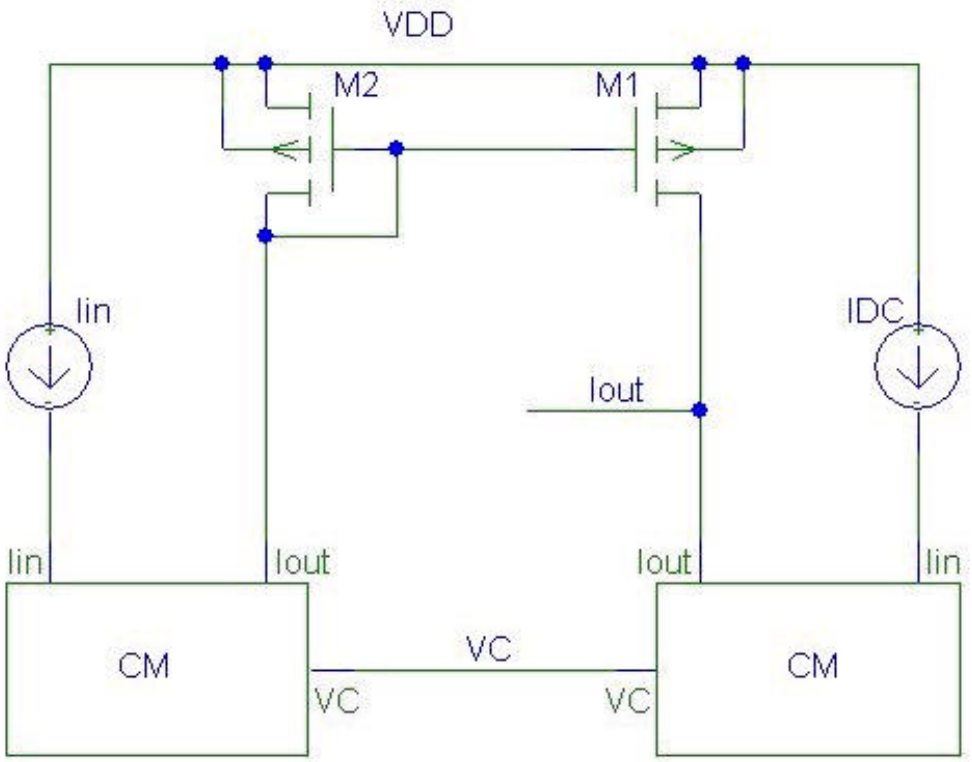


Figure 2.17: The configuration made to cancel the DC current component.

Second transient simulation was made with a pulse current source at the input and the simulations results are given in Figure 2.18 and Figure 2.19 which are obtained separately by changing V_{C1} and V_{C2} control voltages respectively. The stability of the proposed tunable current mirror can also be observed from these pulse response graphics. It is also seen from these graphics that the stability of the circuit is independent from the current gain which is tuned with V_{C1} and V_{C2}.

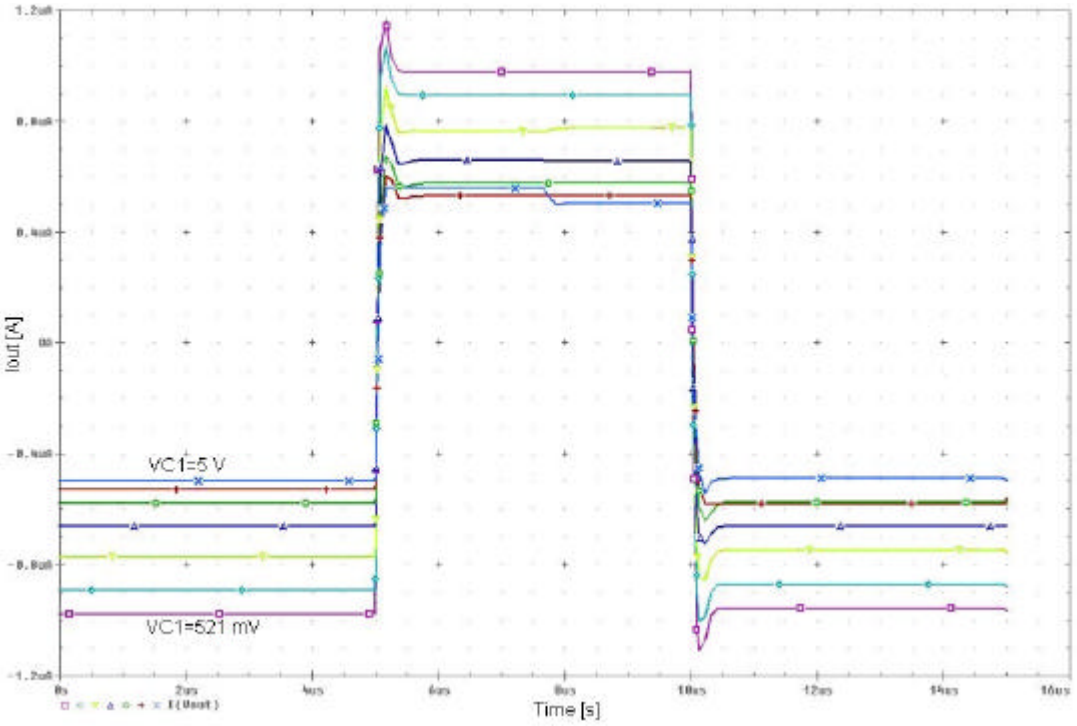


Figure 2.18: The pulse response graphics of the tunable current mirror with the triode MOSFETs obtained by changing V_{C1}.

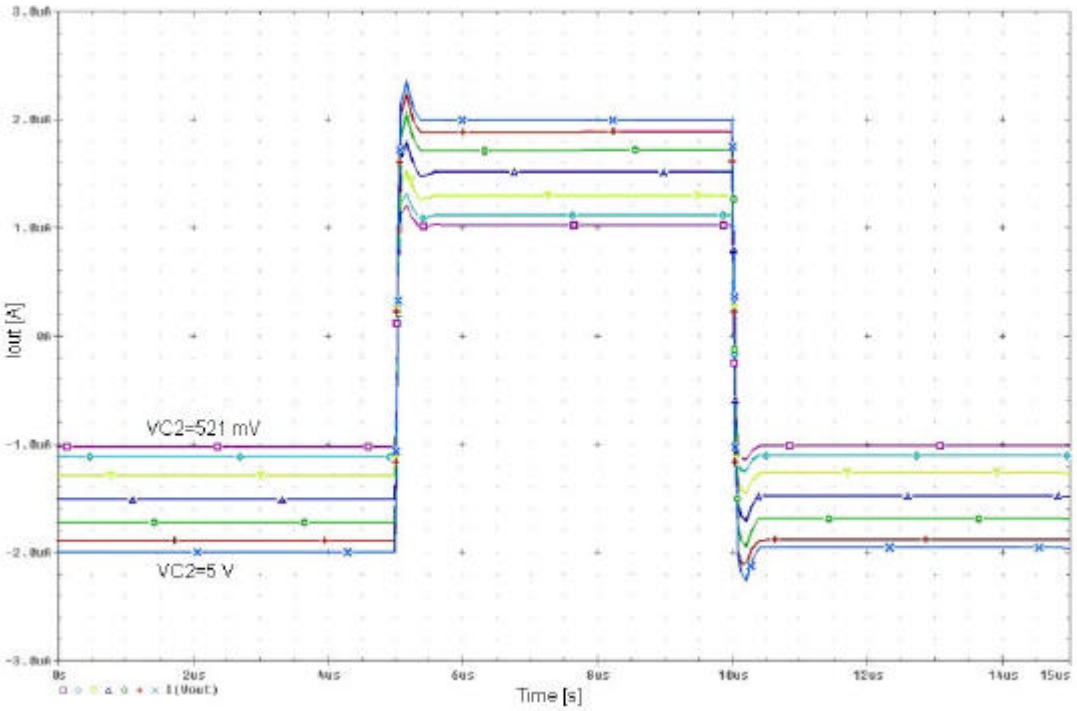


Figure 2.19: The pulse response graphics of the tunable current mirror with the triode MOSFETs obtained by changing V_{C2}.

2.2 Tunable Current Mirror with Variable Gain Amplifiers

The second proposed tunable current mirror of which conceptual circuit is shown in Figure 2.1 depends on controlling the gain of the voltages of the resistors at the input and the output when equalizing them to each other. This circuit also depends mainly on the same principle with the first proposed tunable current mirror architecture previously described. There are two NMOS transistors working in triode region at the input and output of the mirror helping to convert the input and output currents to voltage values linearly. An opamp trying to satisfy the equality of these two voltage values by a negative feedback connection is also present. The conceptual difference of this architecture is that the current gain is not tuned via changing the resistances at the both inputs of the opamp, but by multiplying the voltage of these resistances with tunable gains. According to this working principle, the equation giving the gain of the current mirror is given in Equation 2.5b. Here, A1 and A2 are the gains of the Variable gain amplifiers (VGA) at the input and output respectively and the R_{on6} and R_{on5} are the constant resistances of the corresponding triode MOSFETS. When the dimensions of the triode transistors are selected to be same, the gain equation is reduced to the form given in Equation 2.6. In this situation the gain of the current mirror is only determined by the ratio of the gains of the VGAs.

$$I_{out} R_{on5} A_2 = I_{in} R_{on6} A_1 \quad \textbf{(2.5a)}$$

$$\frac{I_{out}}{I_{in}} = \frac{R_{on6} A_1}{R_{on5} A_2} \quad \textbf{(2.5b)}$$

$$\frac{I_{out}}{I_{in}} = \frac{A_1}{A_2} \quad \textbf{(2.6)}$$

Since the current mirror part of the structure contains no changing component parameters, the tuning performance of the mirror is mainly depends on the VGAs' performance. Performance criteria such as the tuning range and the linearity of tuning are determined by the used VGA topology.

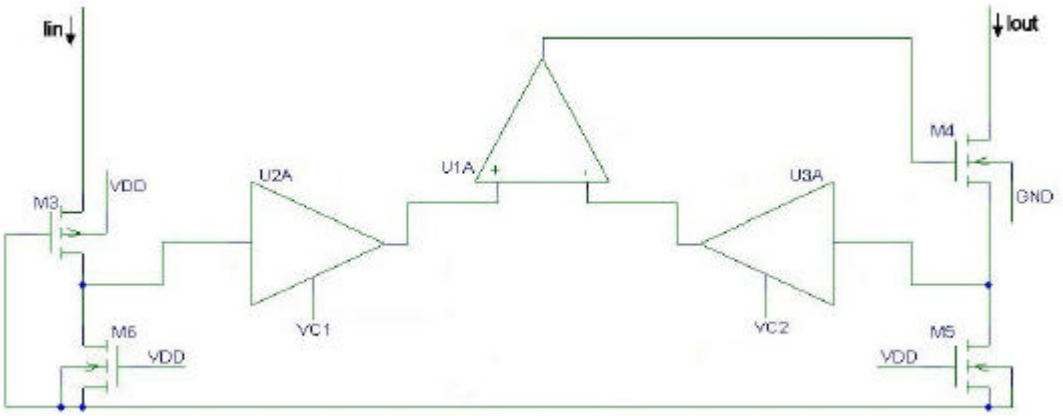


Figure 2.20: The conceptual schematic of the tunable current mirror with VGAs.

The conceptual schematic shown in Figure 2.20 was realized with the basic VGA topology [5] as shown in Figure 2.21 and Figure 2.22 simulations were run on this circuit.

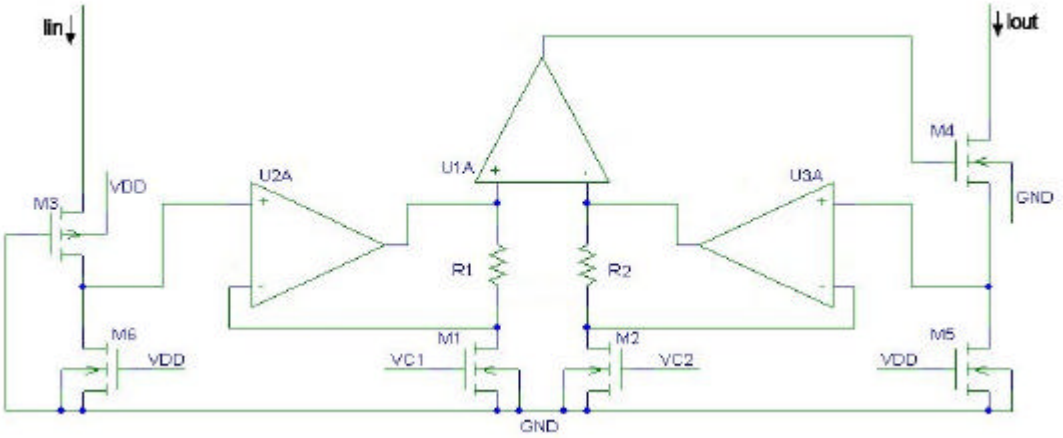


Figure 2.21: The tunable current mirror circuit with the preferred VGA topology.

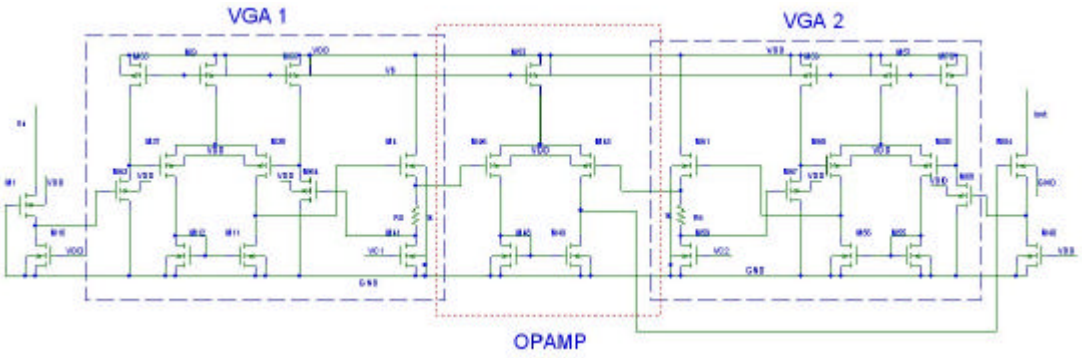


Figure 2.22: The circuit schematic of the tunable current mirror with preferred VGA topology.

2.2.1 Variable Gain Amplifier

The VGA circuits used to realize the proposed current mirror topology is shown in Figure 2.23 separately. This VGA circuit is designed to have a gain of maximum 3 to satisfy a total gain control of approximately one decade in the whole current mirror topology. The gain control of this VGA circuit is done via changing the gate voltage, therefore the resistivity, of the triode transistor M11 on the negative feedback of the circuit. The gain equation depending on the resistivity of the triode transistor is given in Equation 2.7. Here the Rx shows the variable resistivity of the triode transistor while the R is the constant resistor.

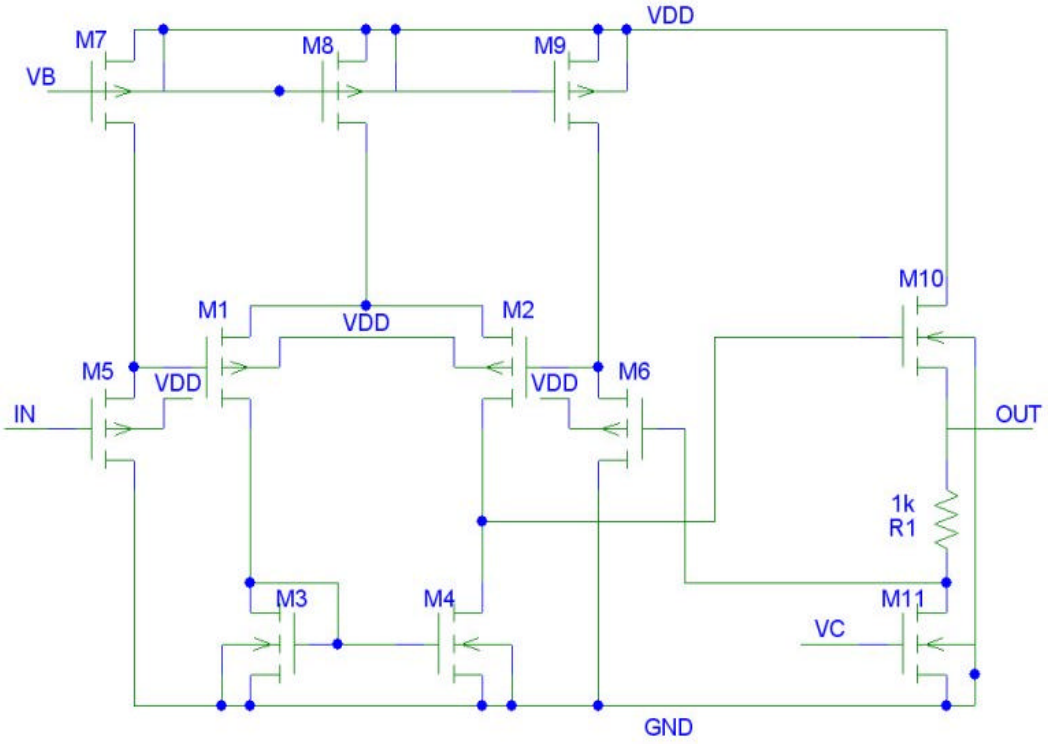


Figure 2.23: The circuit schematic of the preferred VGA topology.

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R}{R_x} \qquad \textbf{(2.7)}$$

It can be easily seen from Equation 2.7 that the gain of maximum 3 can be satisfied by selecting the constant resistance R two times the minimum resistivity of the triode transistor. The transistor dimensions of the VGA circuit are shown in Table 2.4. The biasing current of the differential pair is selected to be 1 µA and the channel lengths

of M1, M2, M3 and M4 are selected to be 2 µm to satisfy high gain. The dimensions of the output transistor M10 is selected high enough to supply the current desired to form the output voltage in the linear operating range. The dimensions of the triode transistor determine the range of the variable resistance thus have a direct affect on the gain of VGA. The resistivity range should be between reasonable values allowing the required maximum output voltage stay in the linear operation range.

Table 2.4: Transistor Dimensions of the VGA Circuit.

Transistor	**W (µm)**	**L (µm)**
M1, M2	46	2
M3, M4	10	2
M5, M6	10	1
M7, M9	230	1
M8	46	1
M10	500	0.5
M11	10	0.5

Due to the selected dimensions of the triode transistor M11, the minimum resistivity value of this transistor is 512? . Thus, using a constant resistance of 1k? achieves the desired gain range from 1 to 3. The simulation result of the VGA circuit shown in Figure 2.23 with dimensions given in Table 2.4 is given in Figure 2.24. The gain curves given in Figure 2.24 were obtained by applying DC sweep to the input of the circuit while changing the control voltage from 450mV to 5V by octave steps. It is seen from the gain curves that the circuit can operate linearly up to 570mV input voltage.

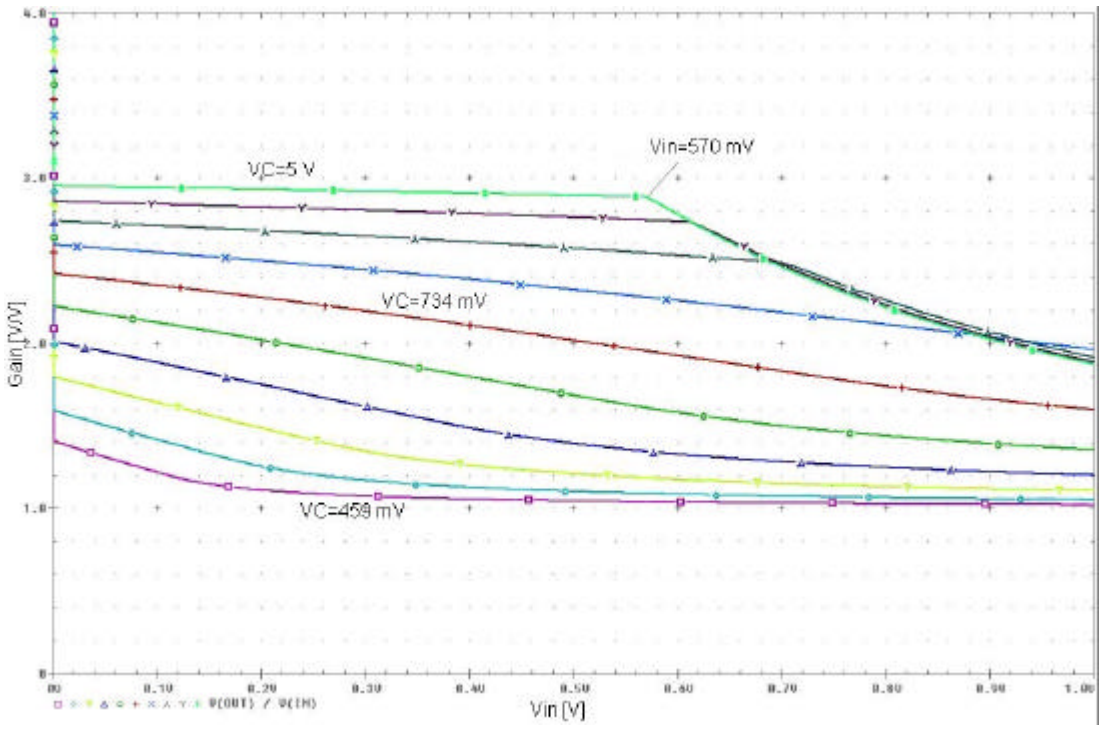


Figure 2.24: DC simulation result of the VGA circuit.

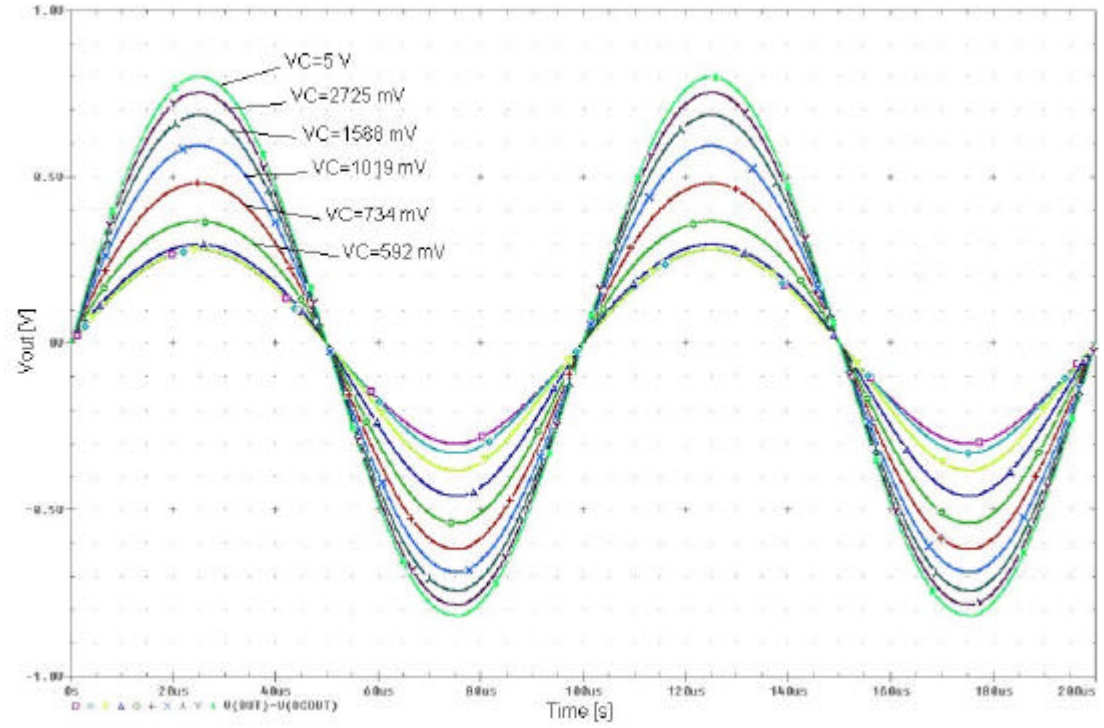


Figure 2.25: Transient simulation result of the VGA circuit.

Table 2.5: Total Harmonic Distortion of the VGA Circuit.

V_C (mV)	THD (%)
521	0.10
592	0.87
734	5.16
1019	10.99
1588	6.34
2725	2.08
5000	0.59

Another simulation run on the VGA circuit is the transient analysis. The resultant graphic of the VGA output is shown in Figure 2.25. The curves in this graphic were obtained by applying a sinusoidal voltage source varying between 0V and 560 mV at 10 kHz frequency at the input of the circuit. To cancel the DC components of the output signals the configuration shown in Figure 2.26 was used for the simulation. In this simulation, control voltage was changed from 450 mV to 5 V with octave steps.

The total harmonic distortion corresponding to the applied control voltages are given in Table 2.5.

2.2.2 Simulations

Finally, simulations have run on the tunable current mirror circuit shown in Figure 2.22. The first simulations results shown in Figure 2.26 and Figure 2.27 were obtained from DC sweep analysis by changing the V_{C1} and V_{C2} control voltages as a parameter respectively. At the graphics shown in Figure 2.26 and Figure 2.27 one of the control voltages were changed from 450mV to 5V by octave steps while the other control voltage is kept constant at 450mV. In Figure 2.26, due to triode transistor biased with V_{C2} at 450mV, below its threshold voltage, the gain of VGA2 is kept close to 1 and by changing the V_{C1} control voltage from 450mV to 5V the gain of VGA1 is controlled from 1 to 3. Thus, the opamp feedback equalizing the outputs of both VGAs causes the gain of the current mirror change from 1 to 3. Besides, in Figure 2.27 the control voltage V_{C1} is kept constant at 450mV causing

the gain of VGA1 to be close to 1 and the other control voltage V_{C2} is changed from 450mV to 5V that is tuning the gain of VGA2 from 1 to 3. In these conditions the opamp feedback equalizes 1 to 3 times the voltage over the output triode transistor to the voltage over the input triode transistor and causes to the gain of the current mirror to be controlled from $\frac{1}{3}$ to 1.

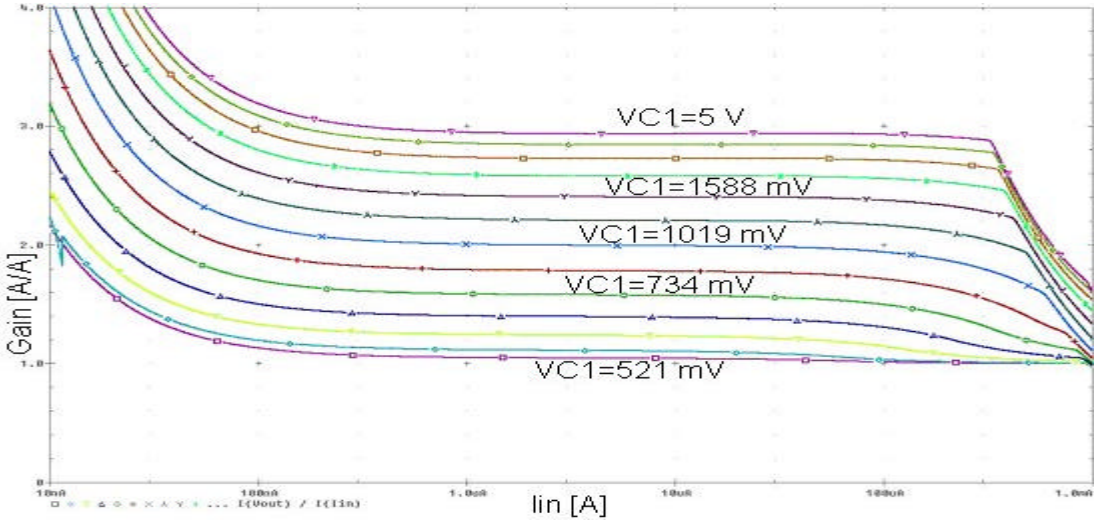


Figure 2.26: The change of the gain of the tunable current mirror with VGAs for different V_{C1} values.

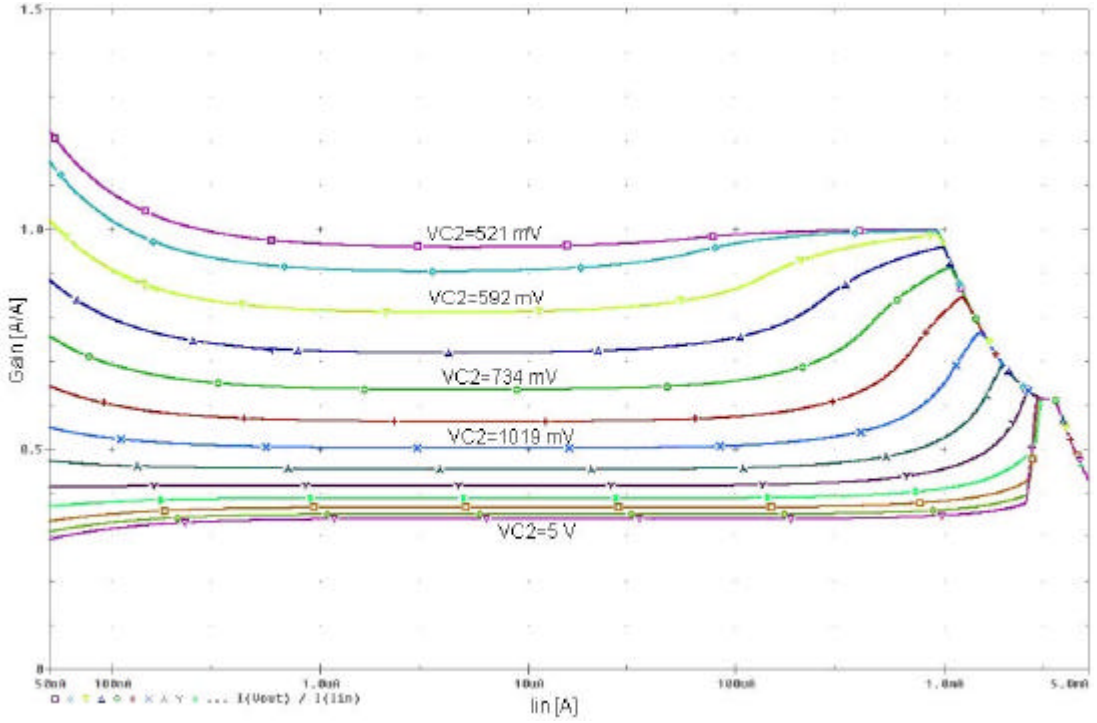


Figure 2.27: The change of the gain of the tunable current mirror with VGAs for different V_{C2} values.

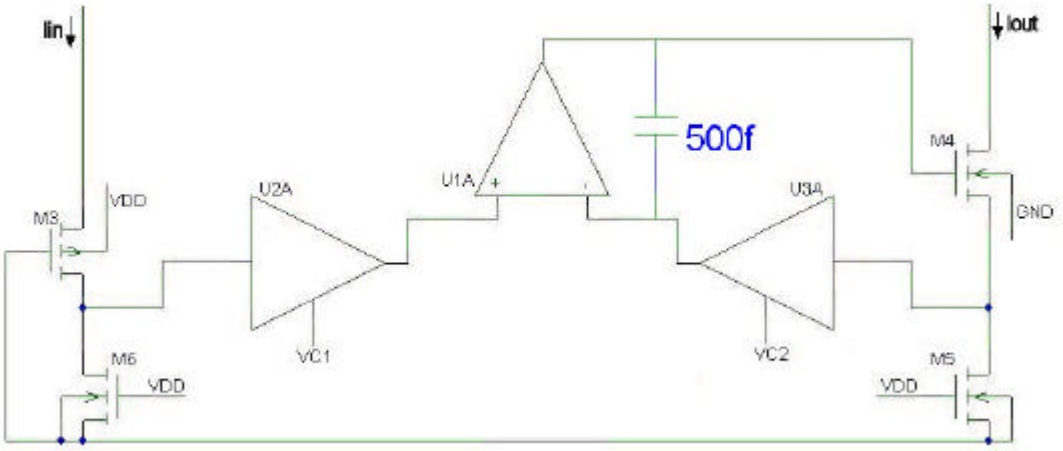


Figure 2.28: The compensation configuration of the tunable current mirror with VGAs.

In this tunable current mirror topology the opamp is used in a negative feedback configuration of which gain is above unity for high values of V_{C2} control voltage. In this architecture, to achieve the overall current gain values below unity, V_{C2} control voltage is needed to be increased thus the worst case for the stability of the current mirror is obtained for lower current gains and a compensation is need to be applied to satisfy the stability for this case.

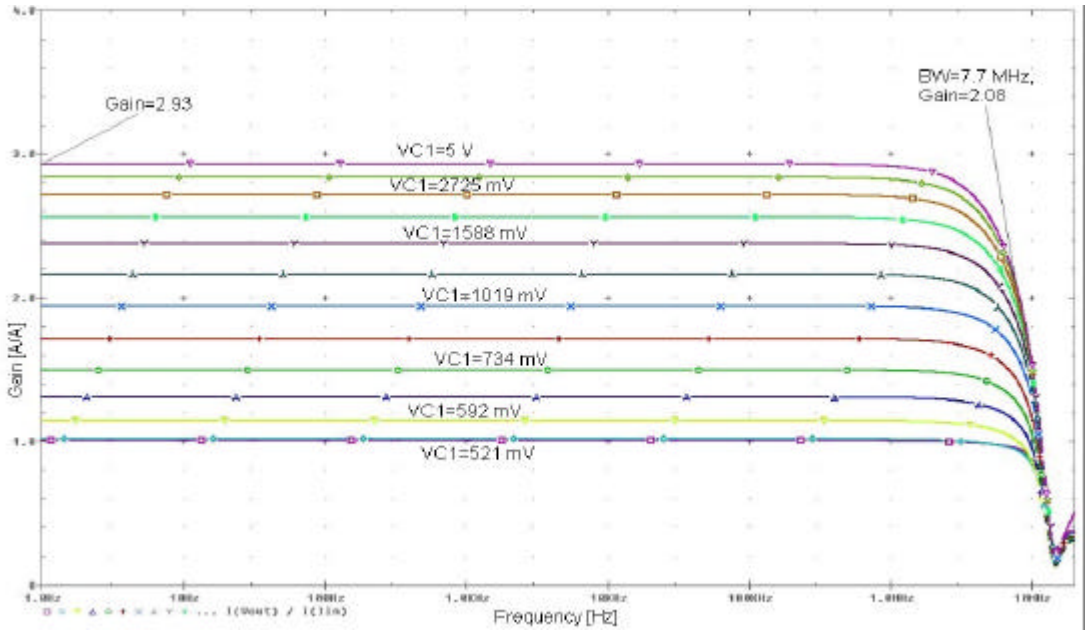


Figure 2.29: The AC simulation result of the tunable current mirror with VGAs obtained by changing V_{C1} in the uncompensated situation.

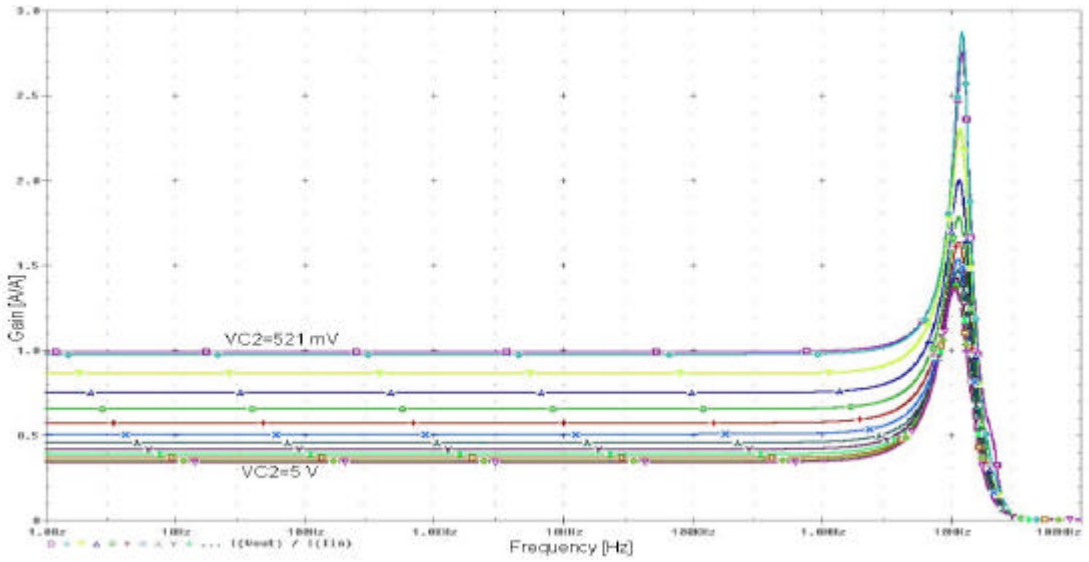


Figure 2.30: The AC simulation result of the tunable current mirror with VGAs obtained by changing V_{C2} in the uncompensated situation.

AC simulations for both uncompensated and compensated situations were run on the circuit and the results are given in Figure 2.29, Figure 2.30, and Figure 2.31. A reasonable connection for the 500 fF compensation capacitor is shown in Figure 2.28. By using this connection the advantage of using a small capacity is gained due to the miller effect of the negative gain of the opamp [5]. The unity gain bandwidth frequency of the circuit at the compensated situation is 1 MHz, at which the gain of curve decreases to $\frac{1}{\sqrt{2}}$ times to its value.

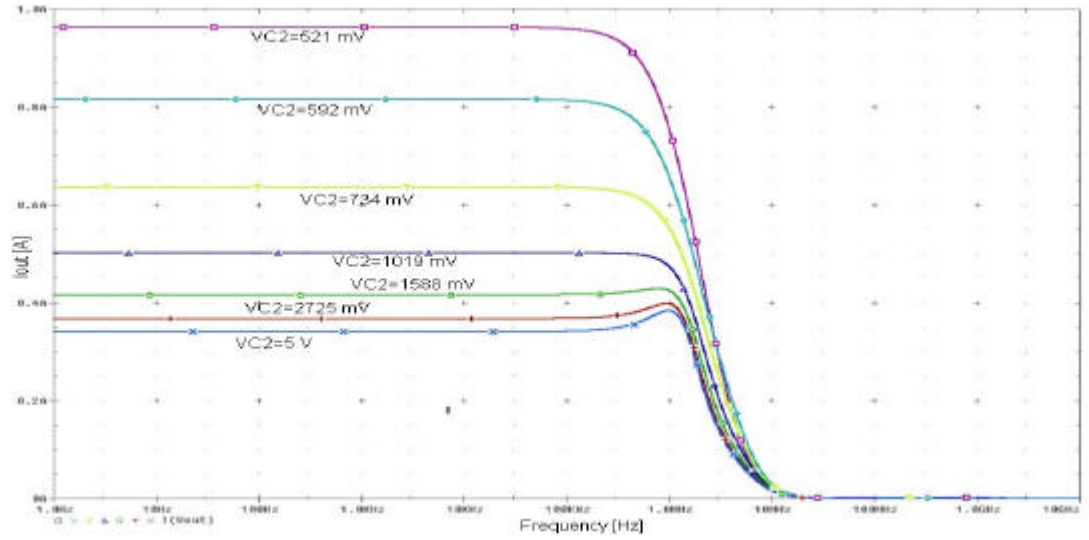


Figure 2.31: The AC simulation result of the tunable current mirror with VGAs obtained by changing V_{C2} in the compensated situation.

Transient simulations were also run on the proposed current mirror schematic and the output sinusoidal current graphics were plotted by using the DC level cancellation configuration shown in Figure 2.17. A 45µA amplitude sinusoidal current varying from 10µA to 100µA with 10 kHz frequency is applied to the input of the current mirror in these simulations.

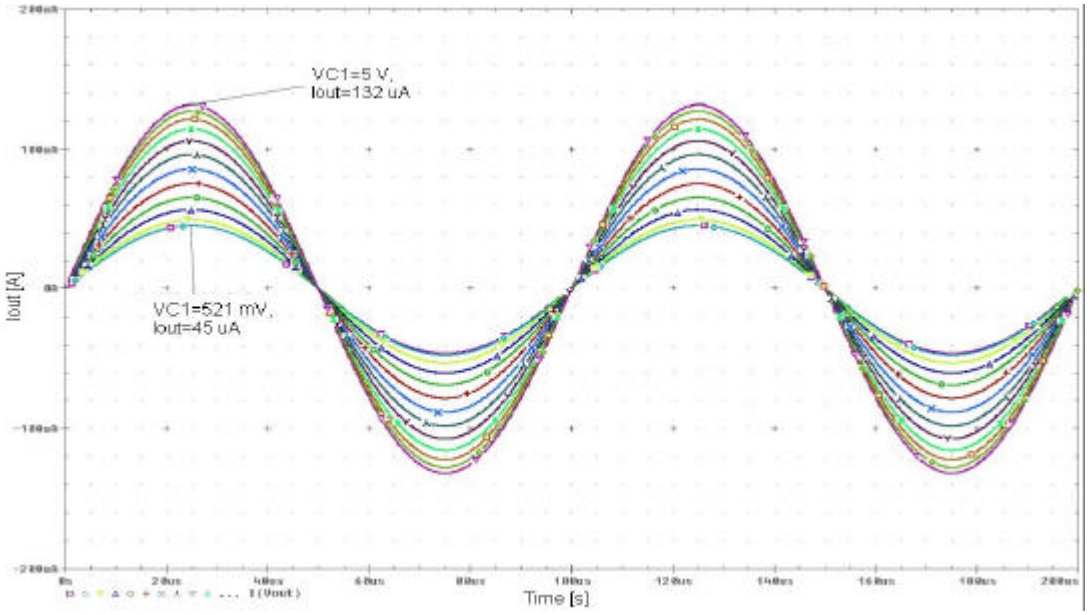


Figure 2.32: The transient simulation result of the tunable current mirror with VGAs obtained by changing V_{C1}.

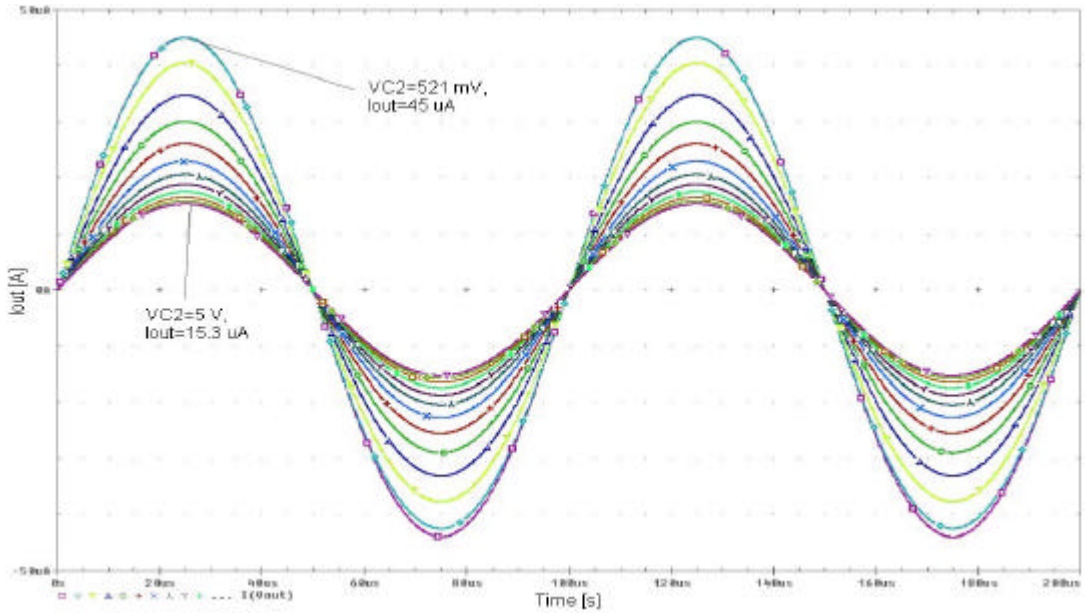


Figure 2.33: The transient simulation result of the tunable current mirror with VGAs obtained by changing V_{C2}.

The graphics showing the change of the output currents when controlling the gain with V_{C1} and V_{C2} were given in Figure 2.32 and Figure 2.33 respectively. The THD results obtained from transient simulations are given in Table 2.6 and Table 2.7. It is seen that the THD for both simulations stay below 2% for an input current range of one decade, 10µA to 100µA.

Table 2.6: THD of the tunable current mirror with VGAs when the gain is controlled by V_{C1}.

V_{C1} (mV)	THD (%)
521	0.53
592	1.95
734	1.37
1019	0.80
1588	0.41
2725	0.23
5000	0.17

Table 2.7: THD of the tunable current mirror with VGAs when the gain is controlled by V_{C2}.

V_{C2} (mV)	THD (%)
521	0.52
592	1.65
734	0.82
1019	0.31
1588	0.08
2725	0.04
5000	0.05

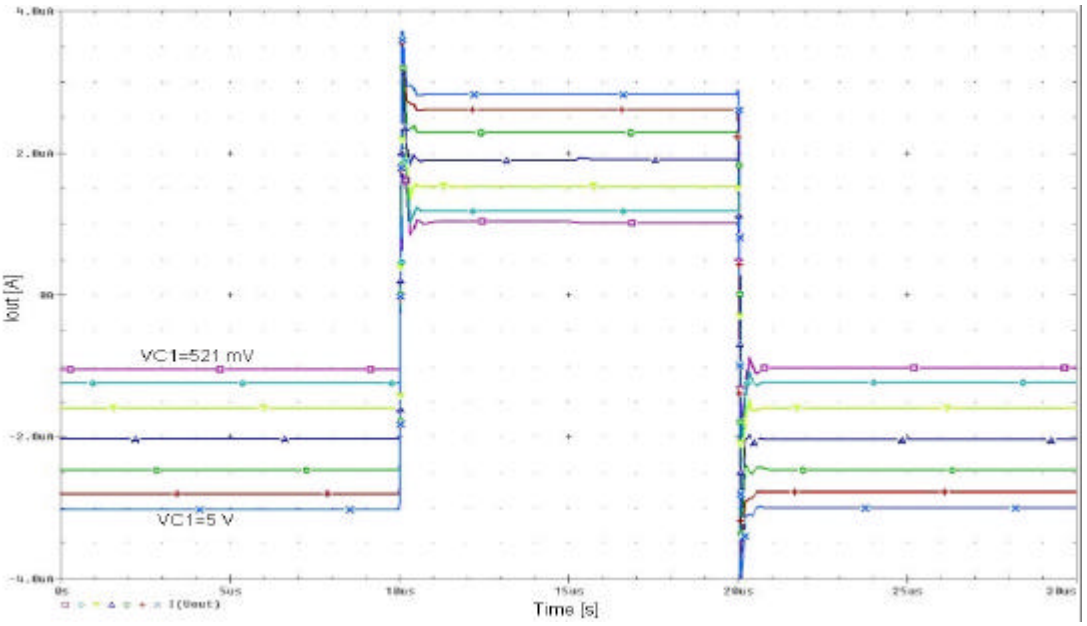


Figure 2.34: The pulse response of the tunable current mirror with VGAs for the uncompensated situation, obtained by changing V_{C1}.

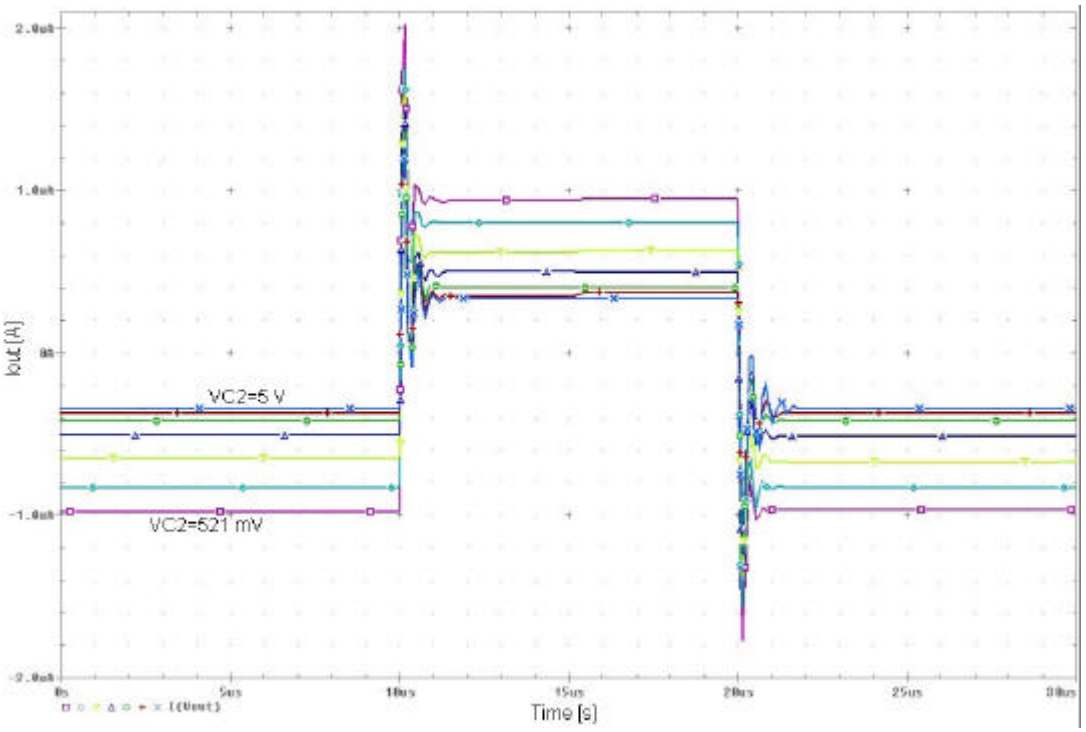


Figure 2.35: The pulse response of the tunable current mirror with VGAs for the uncompensated situation, obtained by changing V_{C2}.

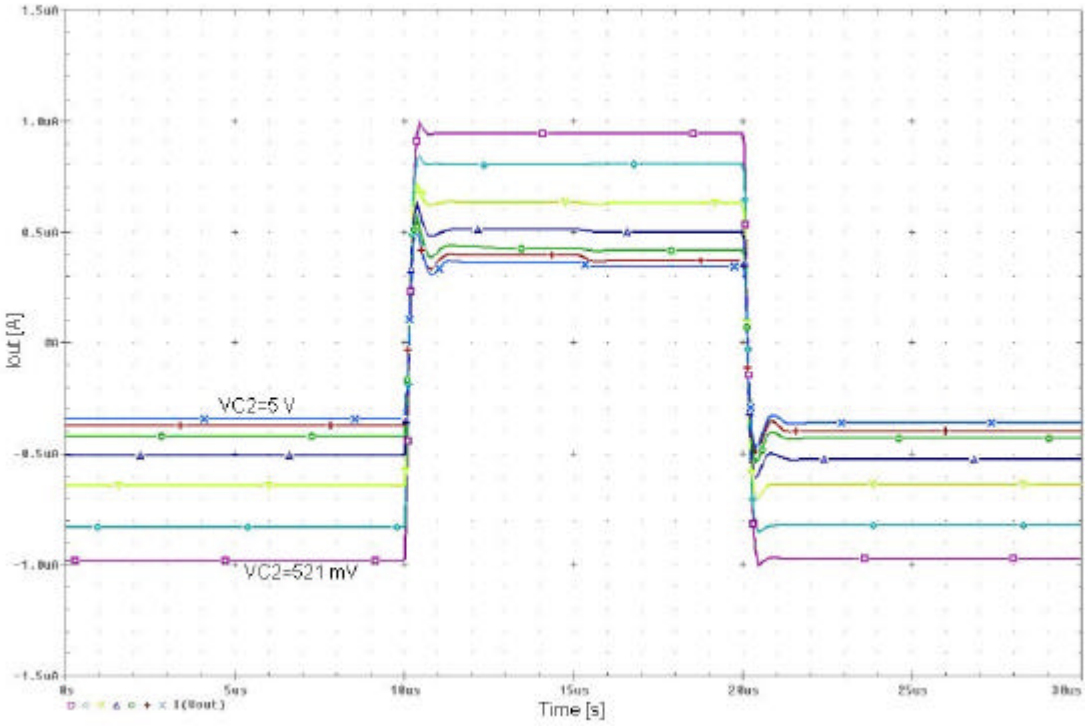


Figure 2.36: The pulse response of the tunable current mirror with VGAs for the compensated situation, obtained by changing V_{C2}.

To show the stability of the proposed tunable current mirror in uncompensated and compensated situations, transient simulations with pulse current source at the input are also run and the graphics of these simulations were given in Figure 2.34, Figure 2.35 and Figure 2.36. As it can be seen from Figure 2.35 there is a ringing in the pulse response of the circuit in the uncompensated situation. Applying the previously mentioned compensated stabilizes the circuit and the ringing does not appear.

2.3 Tunable Current Mirror with Current Dividers

The third tunable current mirror topology of which conceptual schematic is shown in Figure 2.37 is explained in this section. In this topology, the opamp feedback trying to equalize the input and output currents is also used. However the structures at the input and output which are used to achieve the variable gain are different. The current divider circuits used to arrange the amount of currents to be equalized satisfies high linearity, better accuracy in controlling, larger range of control and larger range to operate due to the linear characteristic of the divider circuit. The

current divider circuit used to realize the proposed tunable current mirror topology is shown in Figure 2.38.

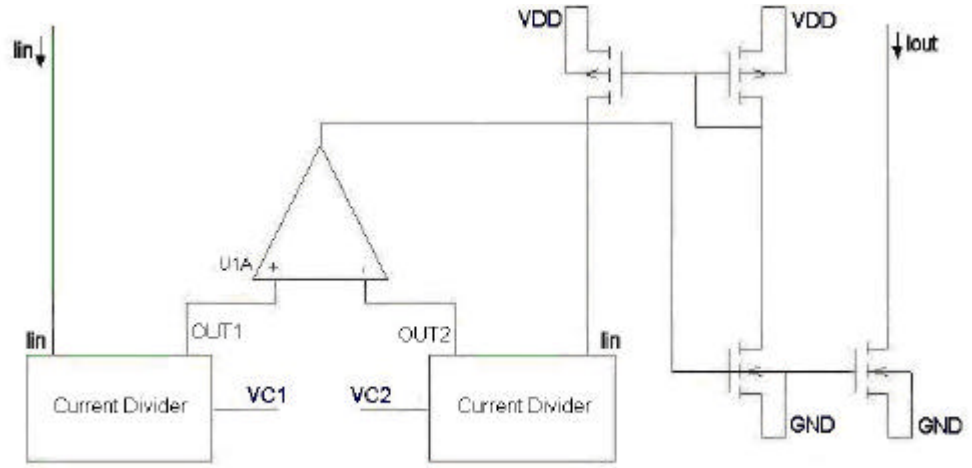


Figure 2.37: The conceptual schematic of the tunable current mirror with current dividers.

2.3.1 Current Divider

As it can be seen from Figure 2.38 used current divider circuit is a basic differential pair realized with Bipolar Junction Transistors (BJT) with diode loads. In this structure, by changing the voltage difference at the inputs of the differential pair the ratio between the current flowing through two load diodes are arranged [6].

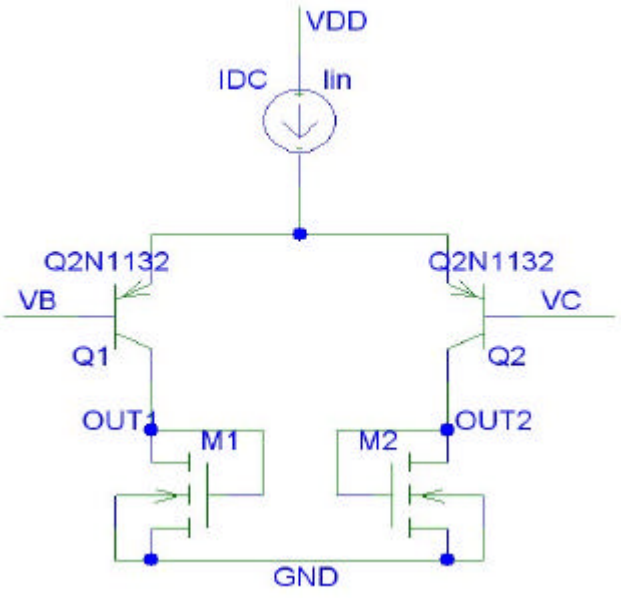


Figure 2.38: The circuit schematic of the current divider.

The currents of which ratio are arranged by the input control voltage are converted to voltage values on the diode loads. DC analysis of which resultant graphics are shown in Figure 2.39 shows the change at the output voltages according to the V_C control voltage while the VB biasing voltage is 2.5V. Figure 2.40 shows the change of the amounts of the currents flowing through two opposite sides for different values of input currents and Figure 2.41 shows the ratio between the two output currents arranged by V_C. The wide range of tuning the ratio between the currents for a wide range of input current is seen from Figure 2.41. This linear transition characteristic of the divider structure is used in the tunable current mirror to satisfy wide gain and linear operation ranges.

By using this division structure at the input and output of the proposed tunable current mirror circuit, any percent of the output current is equalized to the any percent of the input current with the help of the feedback opamp. Thus, a wide range of controllable gain is achieved. The schematic of the tunable current mirror realized with current divider structure at the input and output is shown in Figure 2.40.

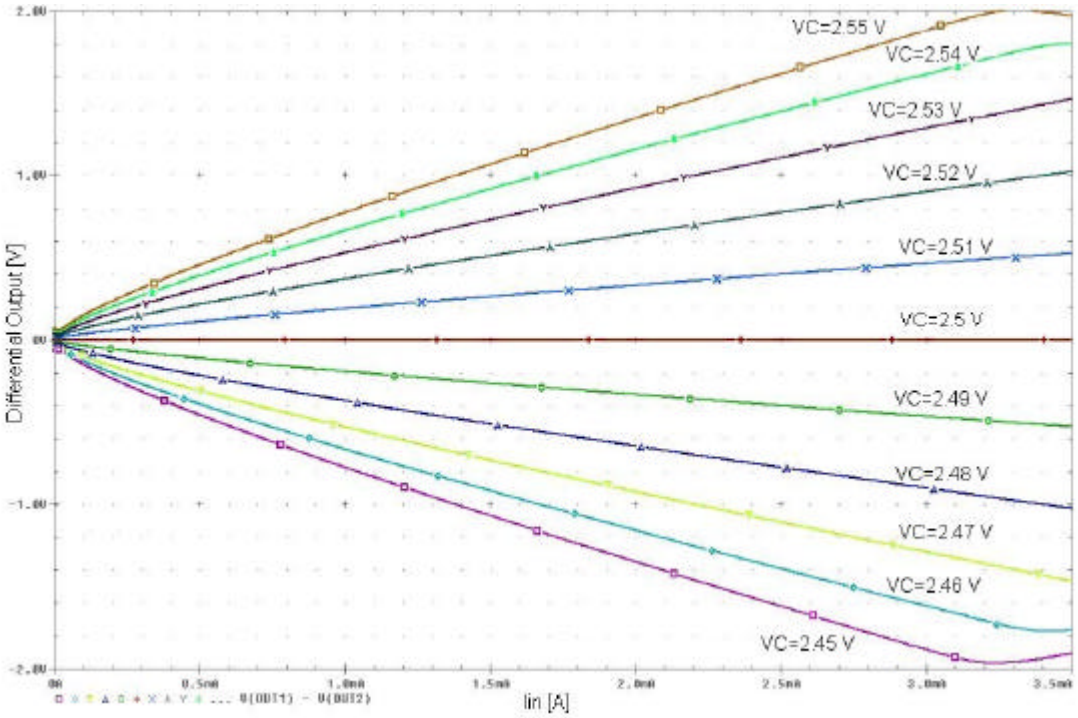


Figure 2.39: DC simulation result of the current divider.

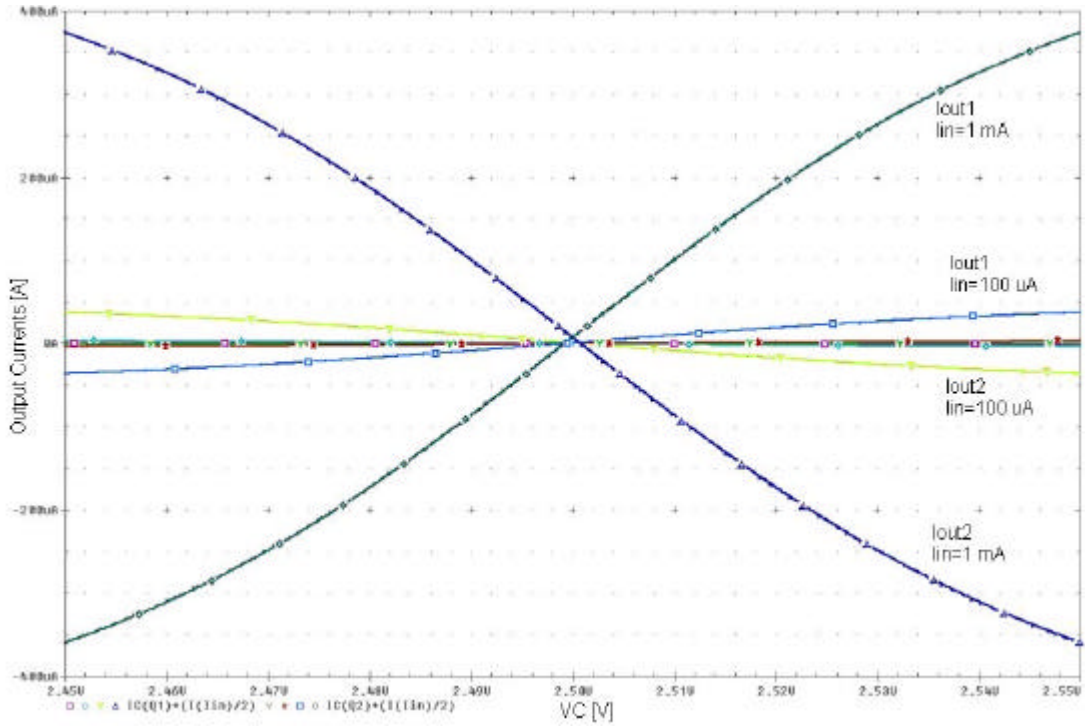


Figure 2.40: The transition characteristic of output currents of the current divider according to V_C for different values of input current (from 1uA to 1mA with one decade steps).

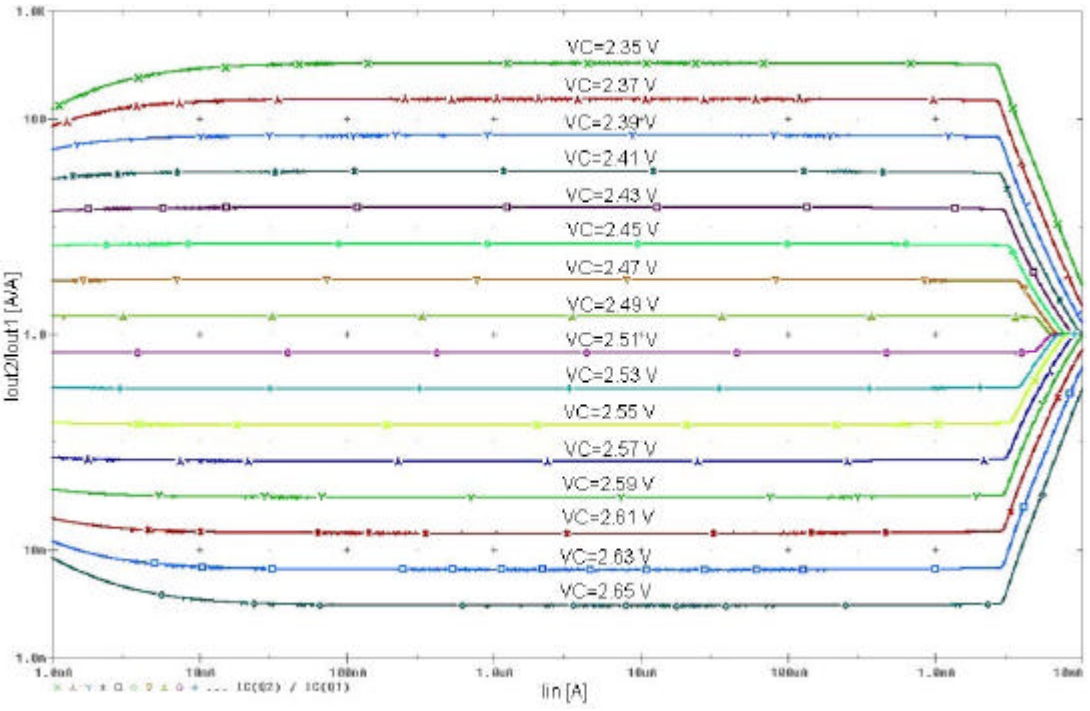


Figure 2.41: The change in the ratio between two output currents of the current divider for different values of V_C.

The equation giving the ratio between the two output currents of the current divider circuit given in Equation 2.9 is obtained from the characteristic equations of the BJT

given in Equation 2.8. By evaluating Equation 2.9 as in Equation 2.10, it is seen that the ratio between two output currents of the BJT differential pair is constant when the input voltages are constant [6].

$$I_C = I_S e^{\frac{V_{BE}}{V_T}} \tag{2.8}$$

$$\frac{I_{out2}}{I_{out1}} = \frac{I_S e^{\frac{V_C - V_E}{V_T}}}{I_S e^{\frac{V_B - V_E}{V_T}}} \tag{2.9}$$

$$\frac{I_{out2}}{I_{out1}} = e^{\frac{V_C - V_B}{V_T}} \tag{2.10}$$

By using the fact that the input current of the divider circuit, which is the biasing current of the BJT differential pair, is the sum of the two output currents, the gain between the input current and the two output currents separately is obtained for the divider circuit. The ratios of Iout1 and Iout2 currents to the input current, Iin, are given in Equation 2.11b and Equation 2.12b respectively.

$$I_{in} = I_{out1}\left(e^{\frac{V_{CB}}{V_T}} + 1\right) \tag{2.11a}$$

$$\frac{I_{out1}}{I_{in}} = \left(e^{\frac{V_{CB}}{V_T}} + 1\right)^{-1} \tag{2.11b}$$

$$I_{in} = I_{out2}\left(\frac{1}{e^{\frac{V_{CB}}{V_T}}} + 1\right) \tag{2.12a}$$

$$\frac{I_{out2}}{I_{in}} = \left(\frac{1}{e^{\frac{V_{CB}}{V_T}}} + 1\right)^{-1} \tag{2.12b}$$

The circuit shown in Figure 2.42 is the schematic of the proposed tunable current mirror structure realized with the current divider circuit shown in Figure 2.38. In this structure, a replica of the output current is generated by applying the output voltage of the opamp to another nmos transistor besides the output nmos transistor and this replica output current is applied to the output current divider circuit by inverting its

direction with a basic pmos current mirror. Since the accuracy between the real output current and the replica of the output current is very important, it is increased by using cascode transistors at both of them.

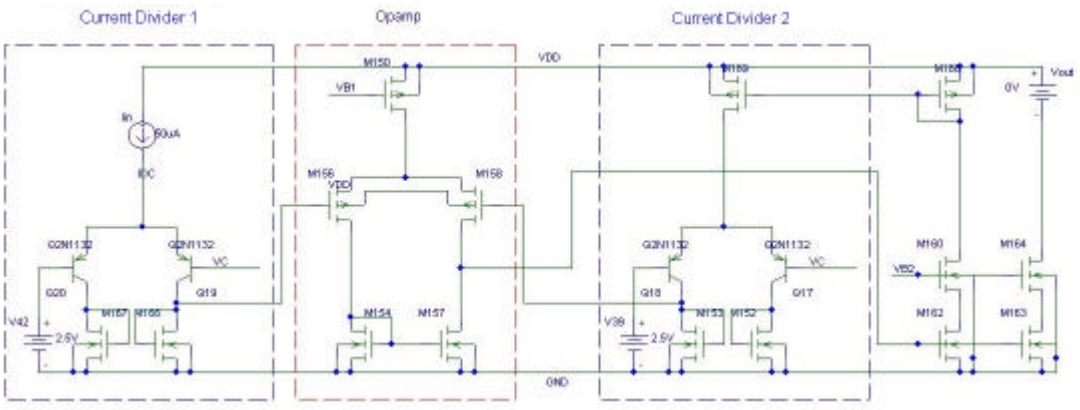


Figure 2.42: Circuit schematic of the tunable current mirror with current dividers.

The circuit can be tuned either by both of the control voltages applied to the divider circuits separately or by applying the same control voltage to the dividers. Different outputs of the divider circuit are used at input and output of the circuit so the amounts of the input and output current to be equalized change in opposite directions. Increasing the V_C control voltage makes a bigger percent of the output current to be equal to a smaller percent of the input current and causes to the gain of the current mirror to be low, while decreasing the V_C control voltage makes a smaller percent of the output current to be equal to a bigger percent of the input current and causes to the gain of the current mirror to be high. The linearity of change of the gain by control voltage is another advantage of the circuit. Equation 2.13, which gives the gain of the circuit, depends on the fact that the voltages of the diode connected transistors at the both inputs of the opamp are equalized by the opamp, so the currents of the diodes which change in opposite directions by the control voltage V_C. Thus, only equalizing the two gain equations of the divider circuit, given in Equation 2.11b and Equation 2.12b, Equation 2.13 is obtained. In Equation 2.13, Io and Ii are the output and input currents of the tunable current mirror respectively.

$$\frac{I_o}{I_i} = \frac{e^{\frac{V_{CB}}{V_T}} + 1}{\frac{1}{e^{\frac{V_{CB}}{V_T}}} + 1} = e^{\frac{V_{CB}}{V_T}} \qquad \textbf{(2.13)}$$

2.3.2 Simulations

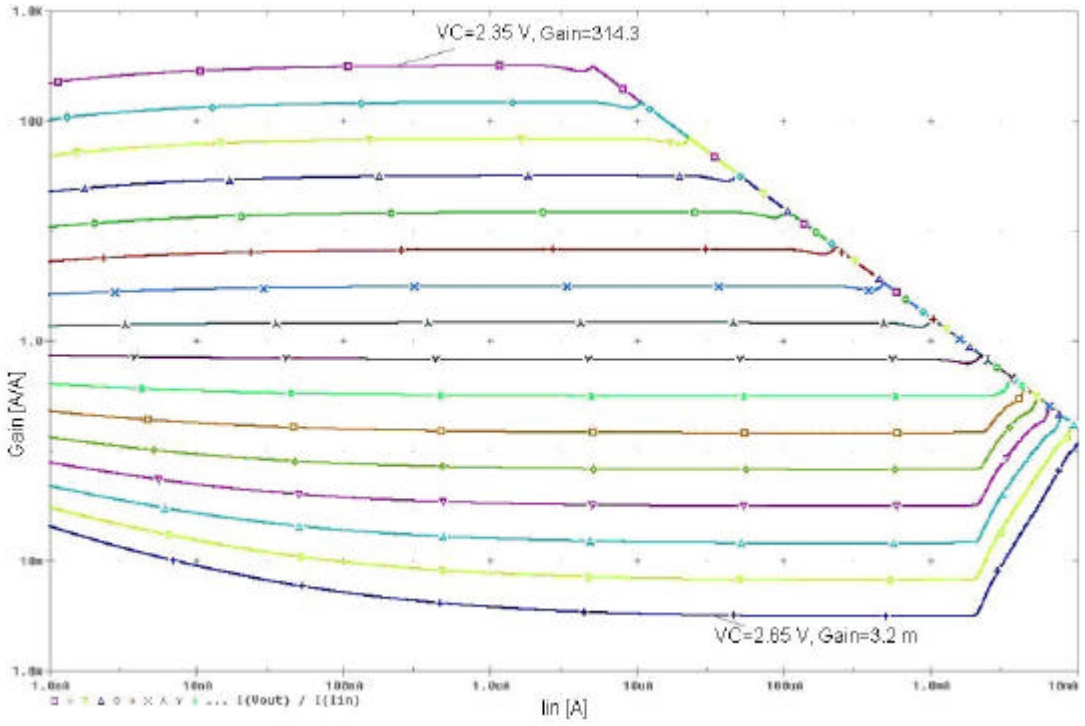


Figure 2.43: The change of the gain of the tunable current mirror with current dividers for different V_C values.

DC simulation was run on the circuit schematic given in Figure 2.42 with a sweeping current source from 1nA to 10mA by decade steps for every 20mV values of V_C from 2.35V to 2.65V. Simulation results are given in the graphic shown in Figure 2.43. The resultant graphic shows that the gain of the proposed current mirror architecture is tunable in a very wide range, from 3m to 300.

To determine the linearity of the current mirror, two separate transient simulations were run on the circuit schematic shown in Figure 2.42 with the configuration shown in Figure 2.17. One of the simulations was run for the gain values smaller than unity and the other one was run for the gain values greater than unity. It is clear that the linearity ranges of these two conditions are very different from each other because of the maximum output current limitation of the structure.

For the region were the current gain is smaller than unity, the linearity of the mirror is mainly restricted by maximum input current which is about 1mA in this simulation. Thus, to approve the linearity of the circuit within this gain range a transient simulation with a 100Hz sinusoidal current source swinging between 8µA

and 800µA. The resultant graphics and the THD percentages are given in Figure 2.44 and Table 2.8 respectively.

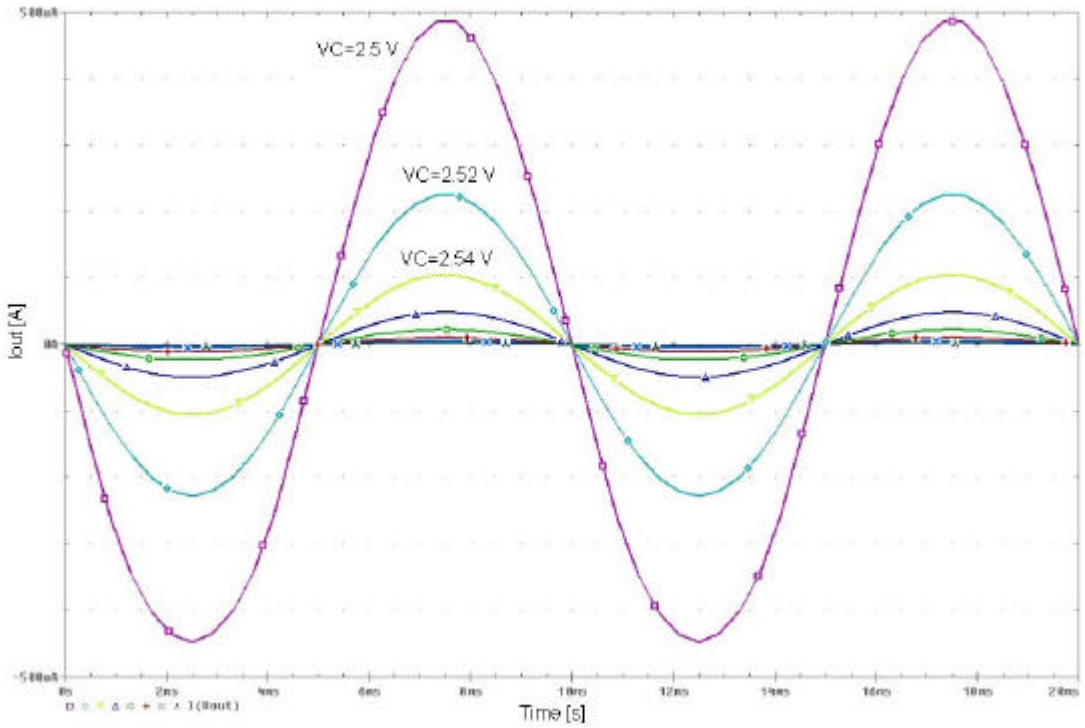


Figure 2.44: Transient simulation result of the tunable current mirror with current dividers when the gain is smaller than unity.

Table 2.8: THD of the tunable current mirror with current dividers when the gain is smaller than unity.

V_C (V)	THD (%)
2.5	0.25
2.52	0.06
2.54	0.08
2.56	0.13
2.58	0.16
2.60	0.18
2.62	0.19
2.64	0.21

The other transient simulation which is made for the gain range greater than unity was run with a 100Hz sinusoidal current source swinging between 20n and 2u. Since the gain is high in this region, to prevent the maximum output limitation, the magnitude of the input current source was selected small enough. The graphics and the THD values obtained are given in Figure 2.45 and Table 2.9 respectively.

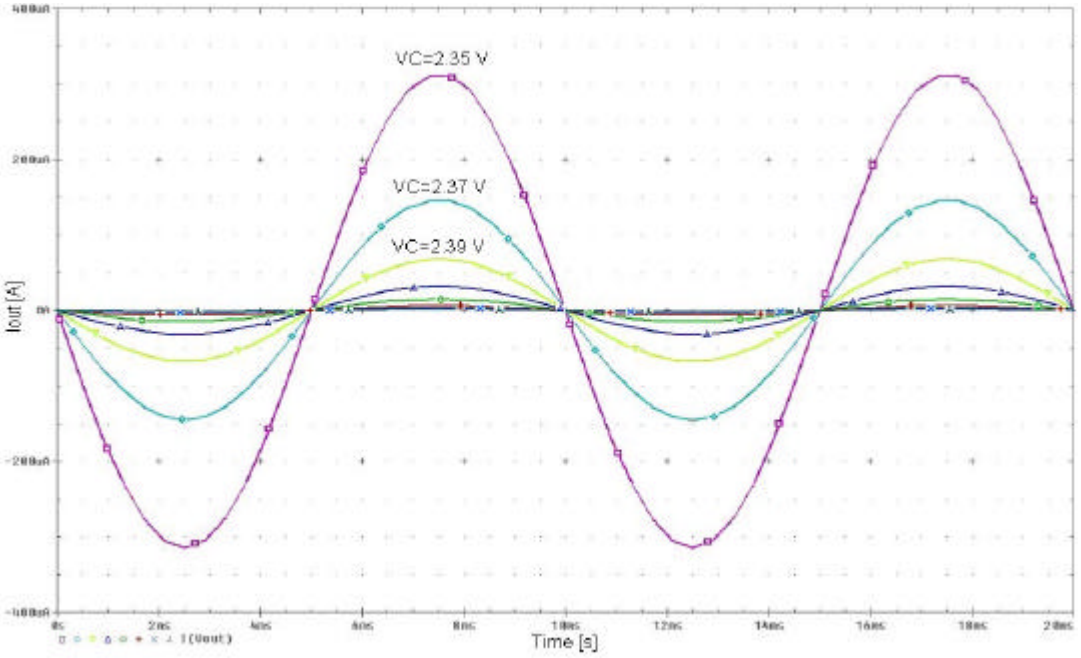


Figure 2.45: Transient simulation result of the tunable current mirror with current dividers when the gain is greater than unity.

Table 2.9: THD of the tunable current mirror with current dividers when the gain is greater than unity.

V_C (V)	THD (%)
2.35	0.21
2.37	0.21
2.39	0.20
2.41	0.21
2.43	0.21
2.45	0.20
2.47	0.16
2.49	0.07

It is seen that for the whole gain range of 5 decades the circuit can operate linearly for at least two decades of input current since the THD values stay below 1%.

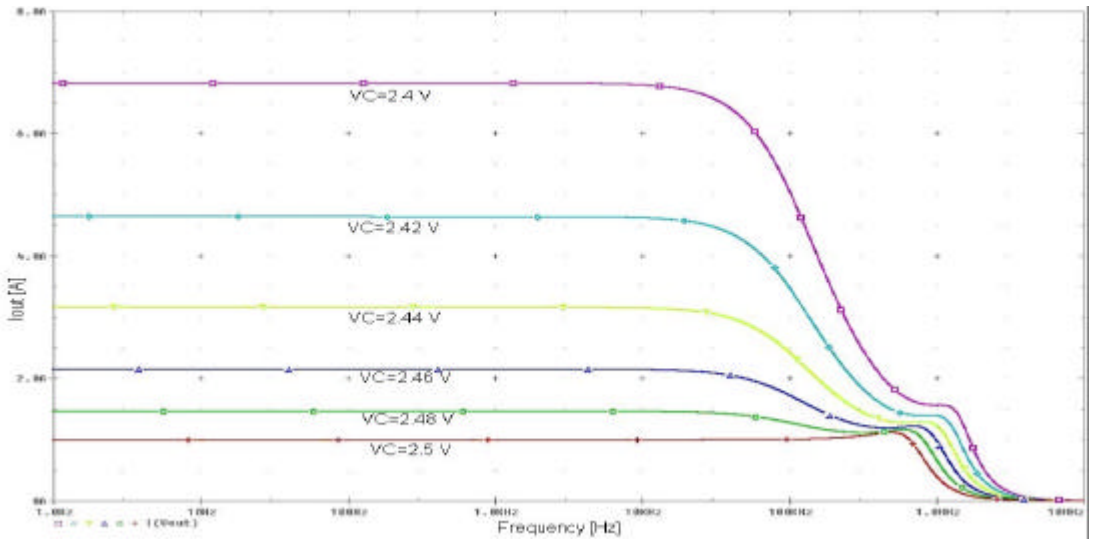


Figure 2.46: AC response of the tunable current mirror with current dividers when the gain is smaller than unity.

To evaluate the AC response of the circuit, AC simulations were run on the circuit schematic for gain ranges smaller than and greater than unity. The resultant graphics given in Figure 2.46 and Figure 2.47 show that the worst case for the stability of the circuit occurs when the gain of the current mirror is adjusted to a value smaller than unity. In Figure 2.47, which is the AC response of the circuit for this situation, a glitch near the cut-off frequency is seen.

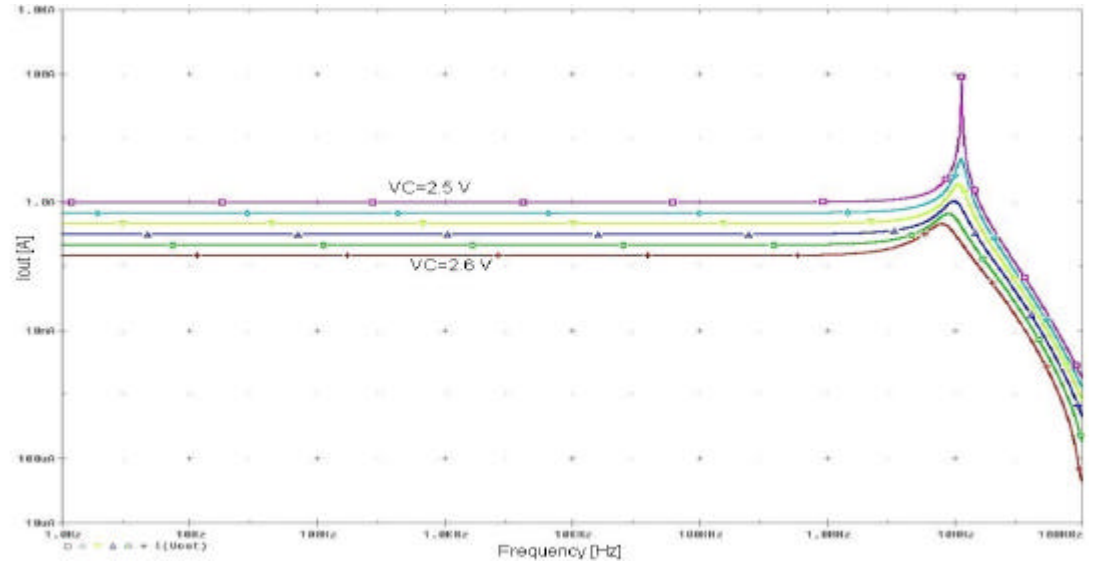


Figure 2.47: AC response of the tunable current mirror with current dividers when the gain is greater than unity.

To compensate the circuit, miller compensation can be applied to the circuit as shown in Figure 2.48. In this configuration the miller effect of the output feedback transistor is used [5]. The stability of the circuit when the proposed compensation is applied with a 2 pF compensation capacitor is shown in the AC analysis result given in Figure 2.49 obtained for the same gain range with Figure 2.47. The unity gain bandwidth of the circuit in the compensated situation is 1.5 MHz.

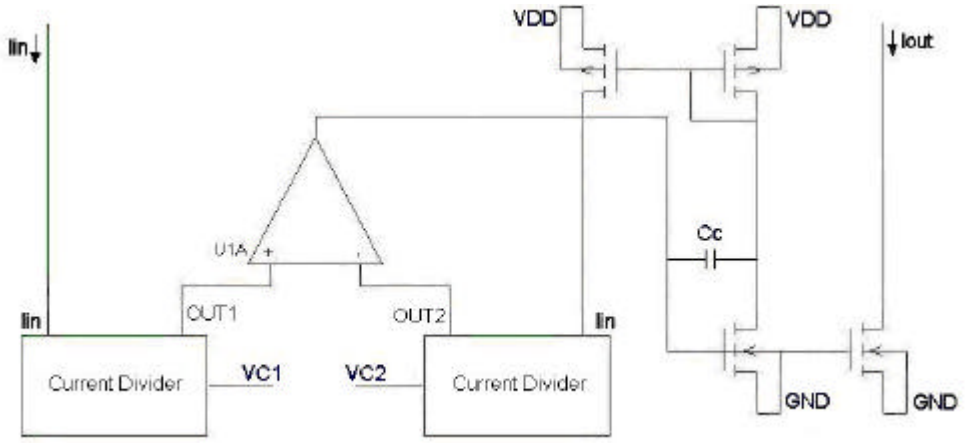


Figure 2.48: Compensation of the tunable current mirror with current dividers.

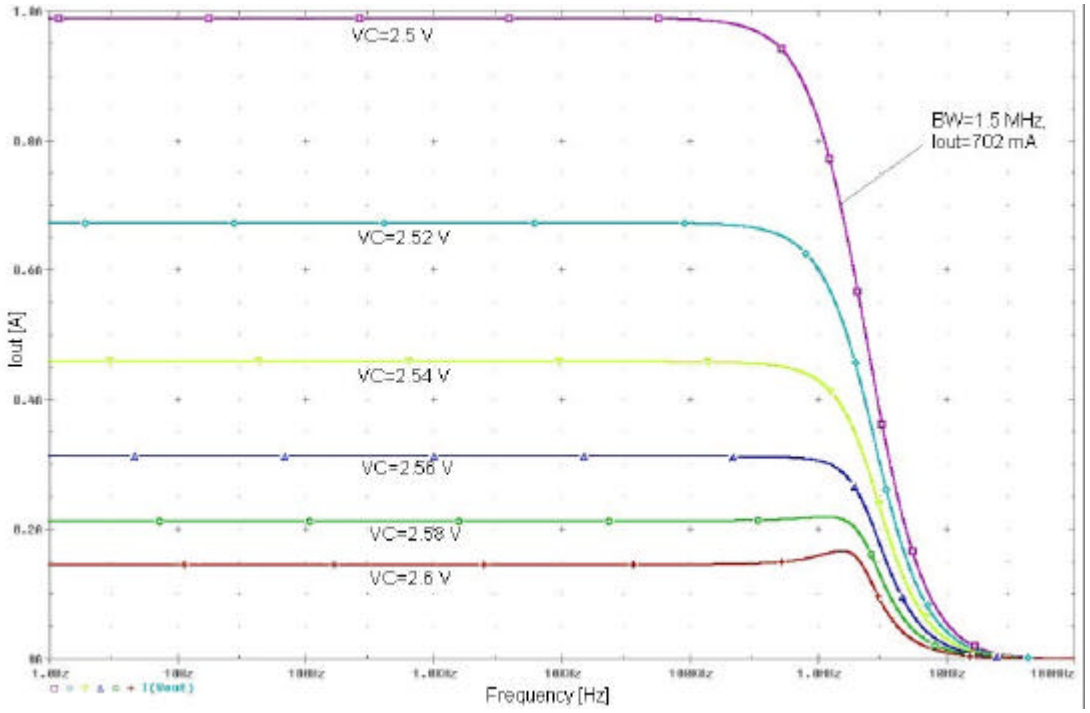


Figure 2.49: AC response of the tunable current mirror with current dividers in the compensated situation.

The effect of the compensation is seen clearly in the transient simulation results which were run for pulse input currents in both compensated and uncompensated situations. The related graphics obtained for this analysis are given in Figure 2.50 and Figure 2.51.

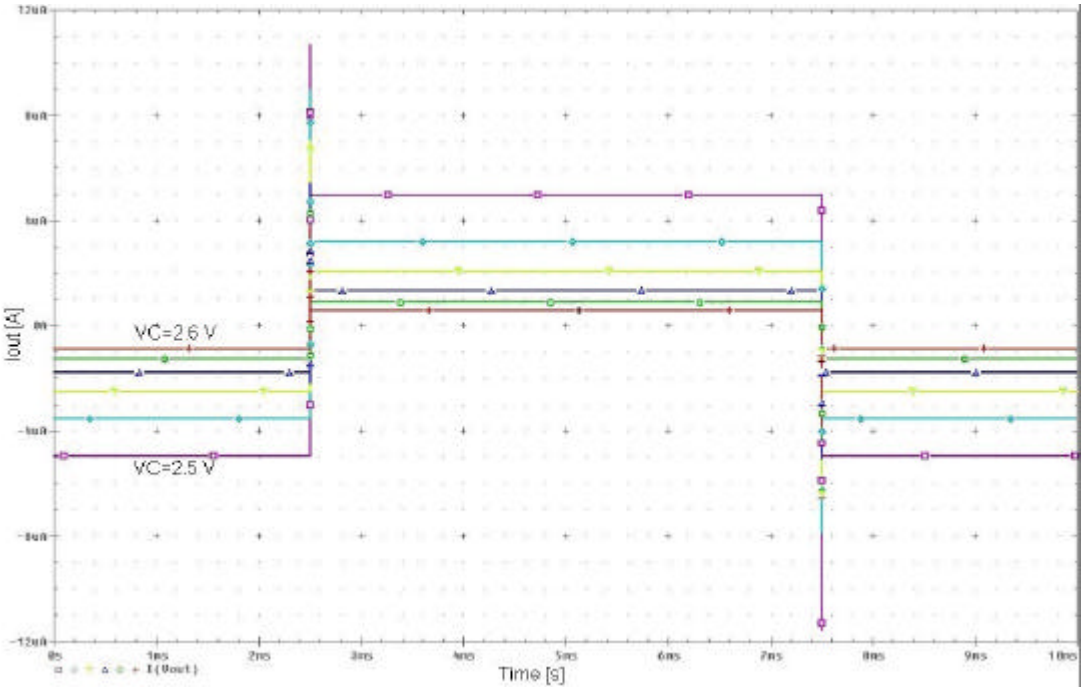


Figure 2.50: Pulse response of the tunable current mirror with current dividers in the uncompensated situation.

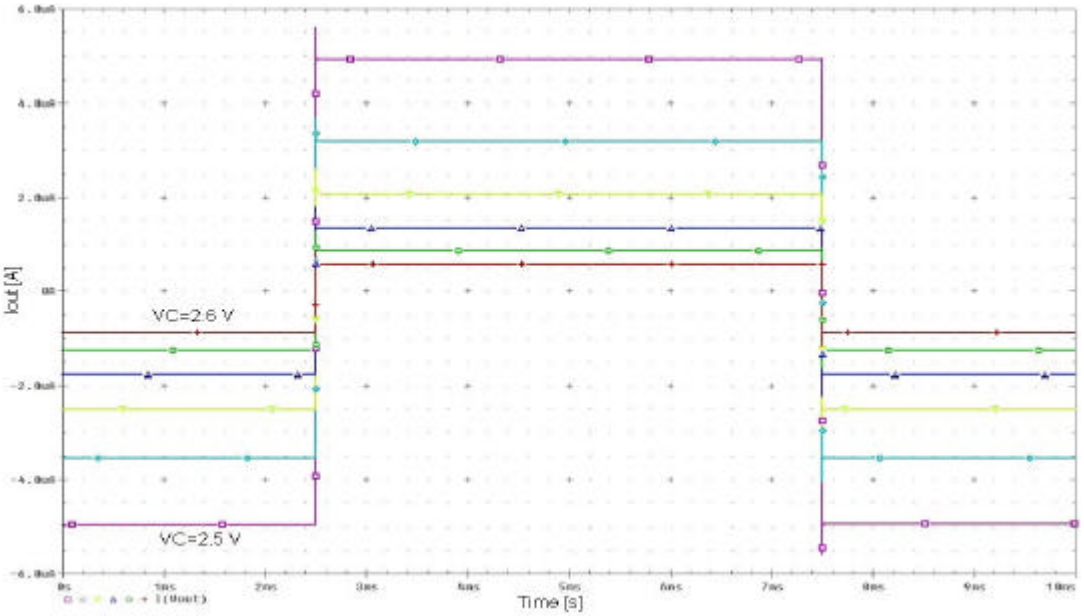


Figure 2.51: Pulse response of the tunable current mirror with current dividers in the compensated situation.

The layout of the designed tunable current mirror with current dividers topology, which is given in Figure 2.52, was created at the Cadence design environment with design rules of YITAL 1.5µm CMOS process for test circuit production. The PNP transistors in the circuit were realized by the parasitic PNP transistors as shown in Figure 2.53. Here, two p+ active regions were placed in the same n-well close to each other, which are used as the collector and the emitter terminals of the PNP transistor while the n-well is used as the base terminal of the PNP transistor.

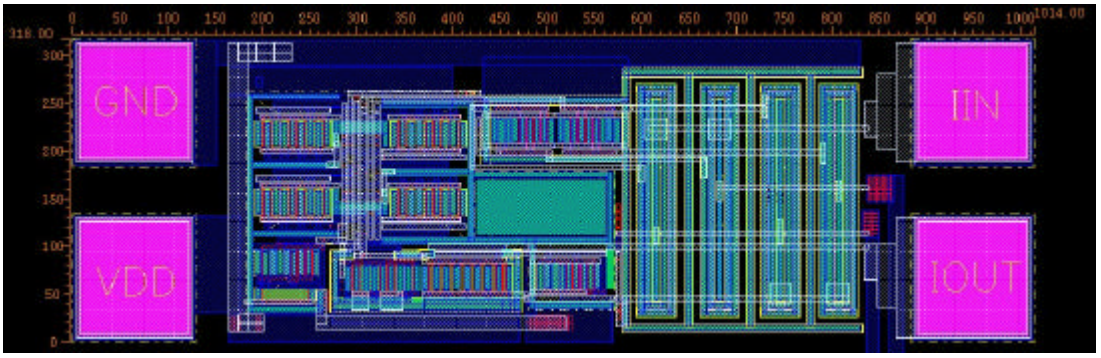


Figure 2.52: Layout of the tunable current mirror with current dividers circuit.

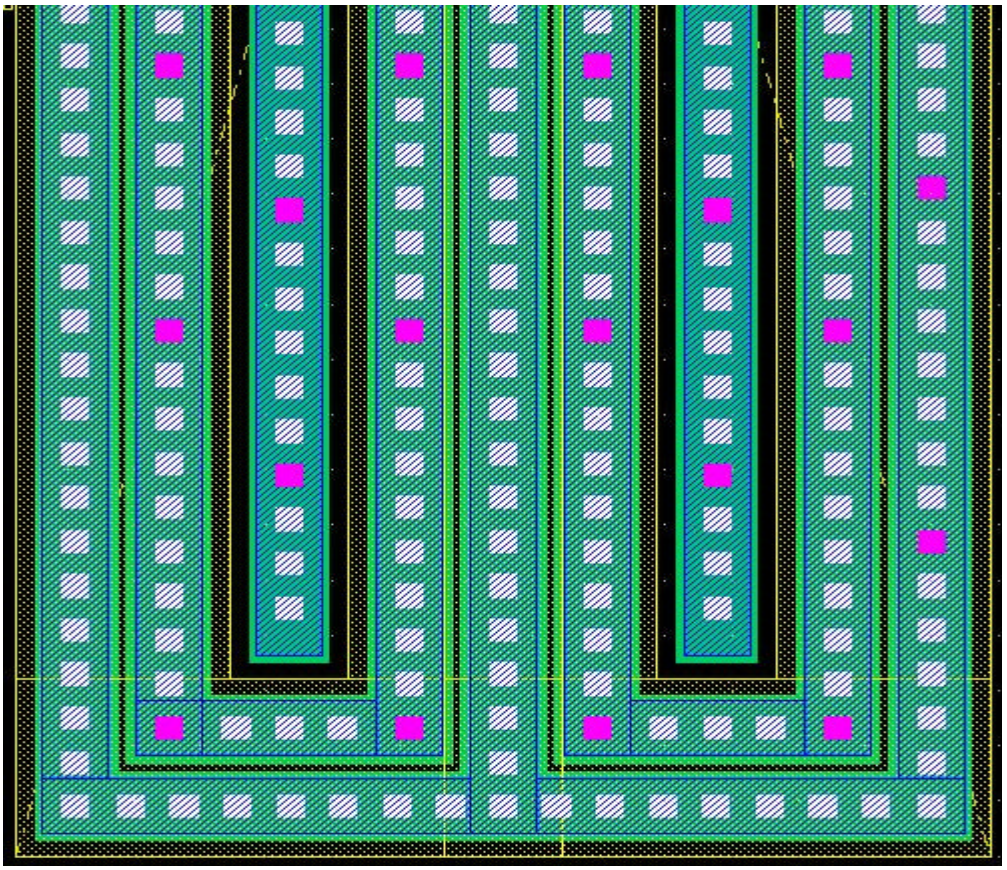


Figure 2.53: Layout of the parasitic PNP transistor.

2.4 Tunable Current Mirror with BJT Differential Pair

A new tunable linear current mirror structure using BJT differential is proposed and this structure is introduced in this section. In this topology, a very wide range of tunable current gain and a wide linear operation region can be satisfied due to linear DC transition characteristic of BJT differential pair. Besides the high operating performance, the circuit also has great advantages of simplicity and low power consumption. The circuit schematic of the new proposed topology is shown in Figure 2.54.

The circuit schematic of the proposed current mirror contains only three transistors. The aim of using BJTs in differential pair instead of MOSFETs is to use the voltage-current relation of BJTs to satisfy constant ratio between input and output currents of the circuit when a constant input voltage is supplied. When the voltage-current characteristic equation of the BJTs is evaluated, the gain of the current mirror is obtained. The gain equation of the circuit is given in Equation 2.15 [6].

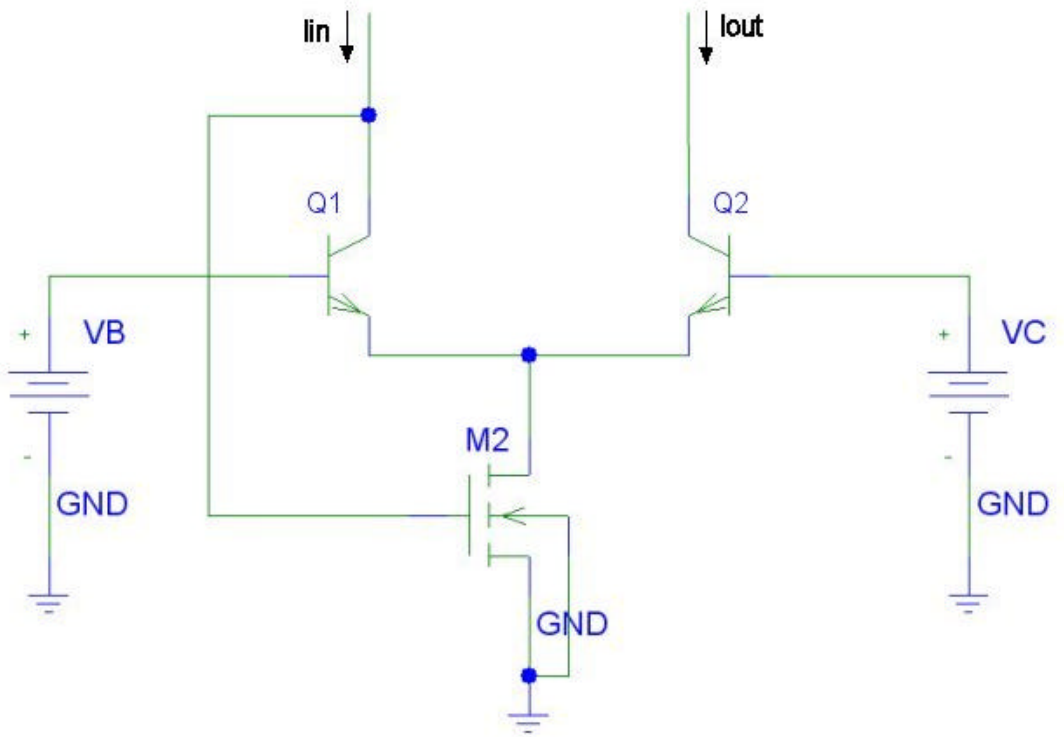


Figure 2.54: Schematic of tunable current mirror with BJT differential pair.

$$\frac{I_{C2}}{I_{C1}} = \frac{I_S e^{\frac{V_C - V_E}{V_T}}}{I_S e^{\frac{V_B - V_E}{V_T}}} = e^{\frac{V_C - V_B}{V_T}} \quad \textbf{(2.14)}$$

$$\frac{I_{out}}{I_{in}} = e^{\frac{V_C - V_B}{V_T}} \quad \textbf{(2.15)}$$

According to the gain equation, the current gain of the circuit can be determined by the differential input voltage. When the differential input voltage is kept constant, the ratio between input and output currents is independent of current values.

The NMOS transistor supplying the tail current of the differential pair is used in a negative feedback configuration that is satisfying the biasing voltage of this transistor to supply the desired total input and output currents. Any increase (decrease) in the input current would result in the increase (decrease) in the input voltage level which is the V_{GS} voltage of the NMOS transistor. Thus, the tail current of the differential pair increases (decreases) which is the sum of input and output currents. Since the ratio between the input and output currents are constant, the current flowing through the NMOS transistor is determined by input current as shown in the Equation 2.17. It is obvious that the dimensions of the NMOS transistor should be large enough to supply high currents.

$$I_{NMOS} = I_{in} + I_{out} \quad \textbf{(2.16)}$$

$$I_{NMOS} = I_{in} + I_{in}.Gain = I_{in}\left(1 + e^{\frac{V_C - V_B}{V_T}}\right) \quad \textbf{(2.17)}$$

Since the only current flowing through the current mirror is the sum of input and output currents and no extra current is needed during the operation of the mirror, this topology has the advantage of low power consumption.

2.4.1 Simulations

According to the DC simulation result shown in Figure 2.55 the gain of the circuit can be controlled over a wide range of 5 decades, from 3m to 300 within a linear

operation range of approximately 2 decades. The linear operation region of the circuit varies according to the input current when the gain of the circuit is high.

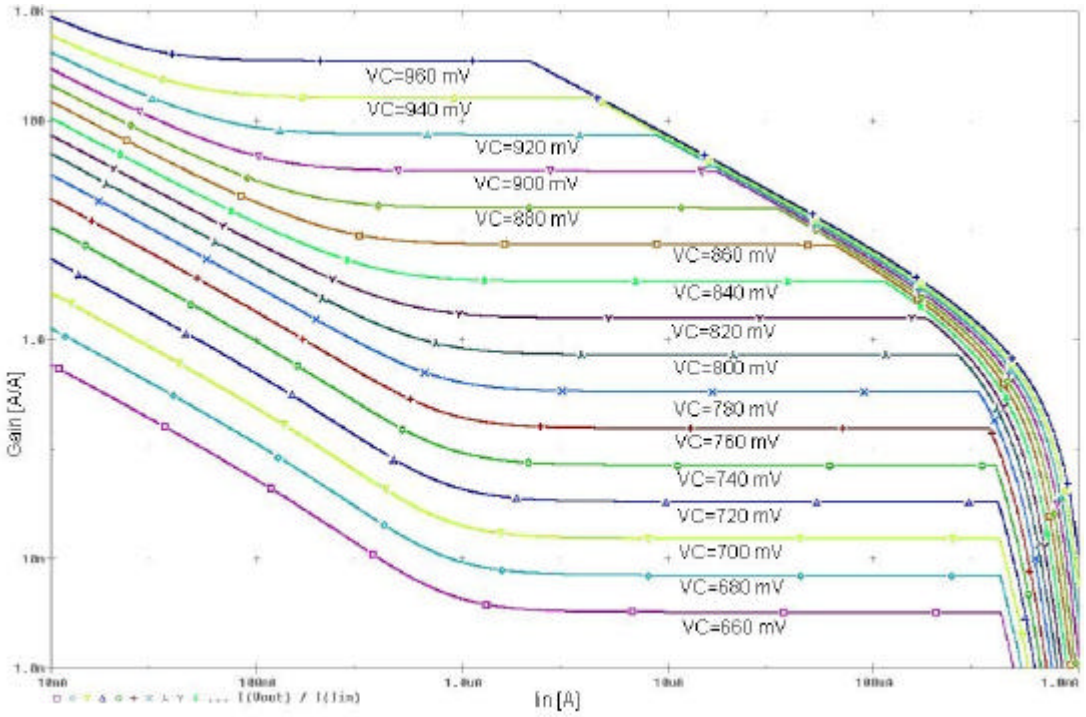


Figure 2.55: The change of the gain of the tunable current mirror with BJT differential pair for different V_C values.

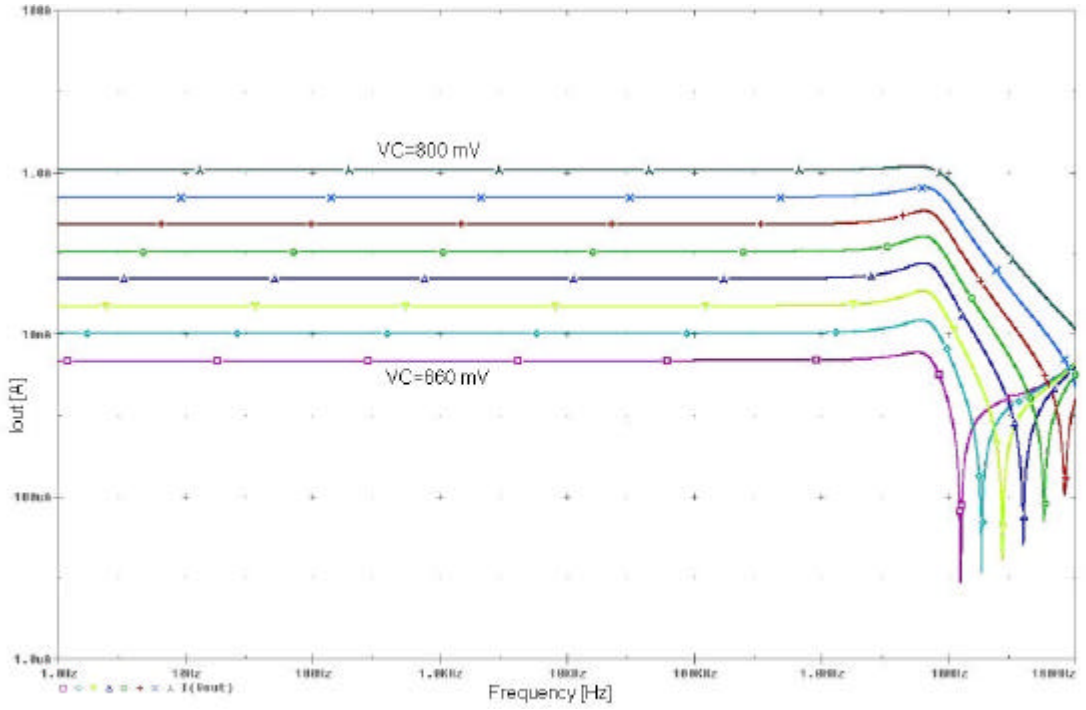


Figure 2.56: AC response of the tunable current mirror with BJT differential pair for low gain values.

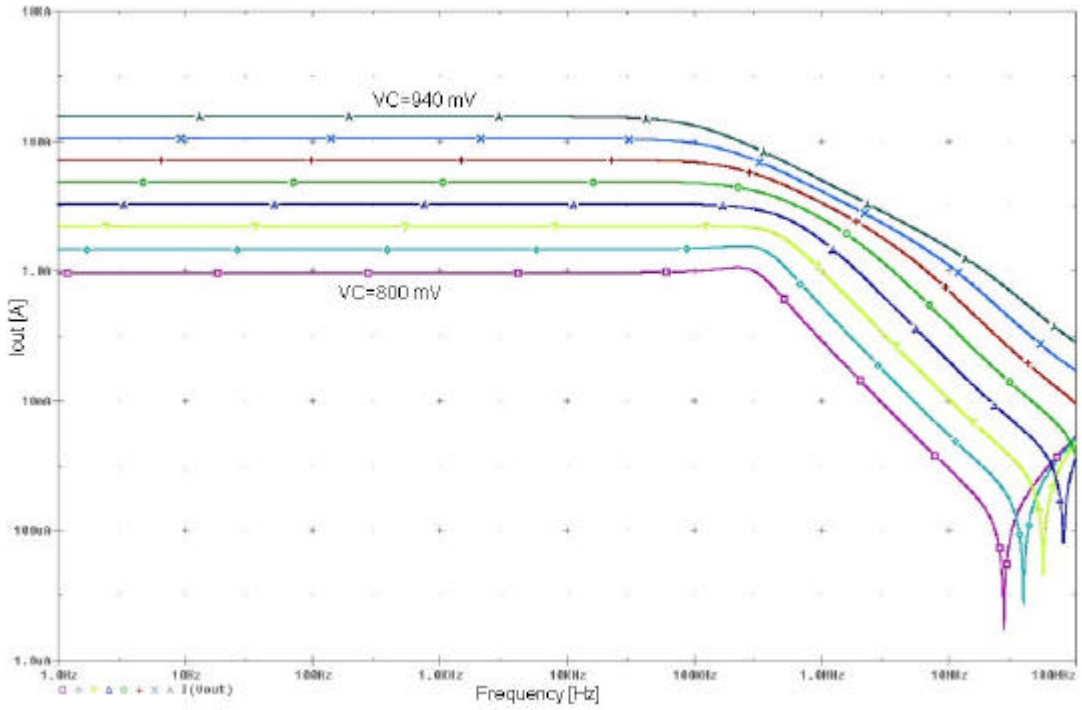


Figure 2.57: AC response of the tunable current mirror with BJT differential pair for high gain values.

The AC response of the circuit is shown in Figure 2.56 and Figure 2.57 which contain the results of the simulations made for the low gains and high gains separately. The graphics in the Figure 2.56 and Figure 2.57 shows that there is no stability problem of the circuit.

To prove the stability seen from the AC simulation results and to show the linearity of the circuit, transient analysis were also done on the tunable current mirror with BJT differential pair circuit. The transient simulations were run with sinusoidal input source and pulse input source. From the simulation done with sinusoidal input current source, the THD of the circuit is obtained and given in Table 2.10 and Table 2.11. These results show that the circuit can operate with a very low THD within a region greater than 2 decades of which boundaries vary due to high gain of the circuit. For the gains smaller than unity the circuit can operate linearly with very low THD within even 3 decades of input current range. The THD values given in Table 2.10 and Table 2.11 are obtained with different simulations by changing the input current source swing range. The used input current source swing ranges for the corresponding THD values are also given in the tables. The frequency of the

sinusoidal input current sources is 1 kHz and the biasing voltage VB used in these simulations is 800 mV.

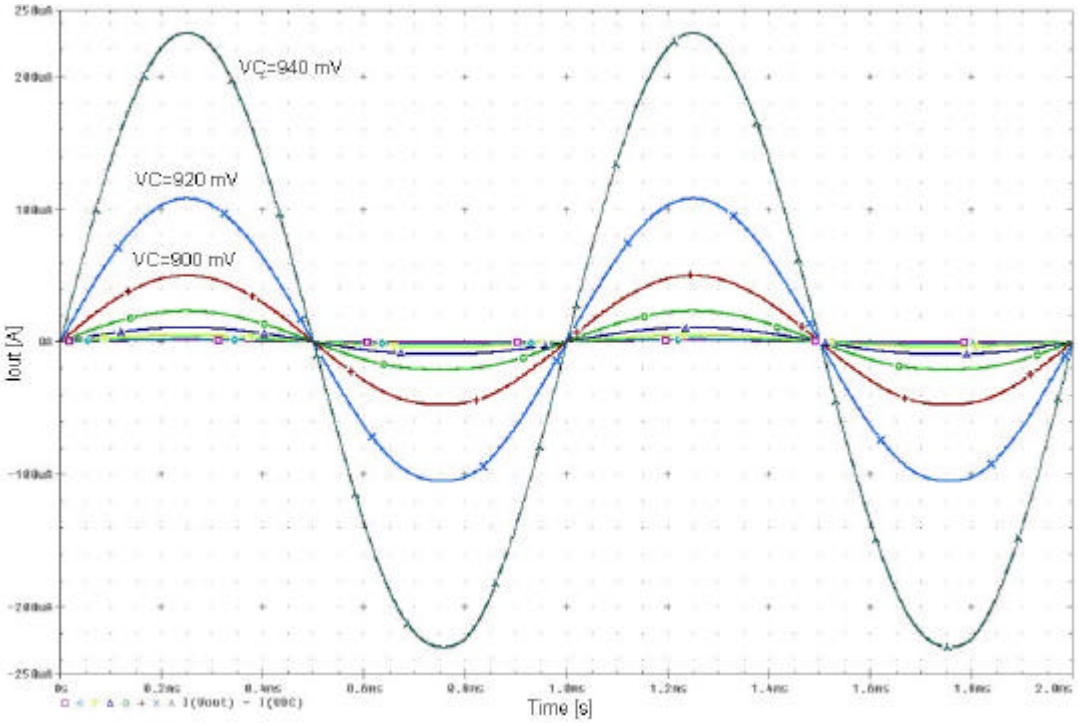


Figure 2.58: Transient simulation of the tunable current mirror with BJT differential pair with sinusoidal input for gains greater than unity.

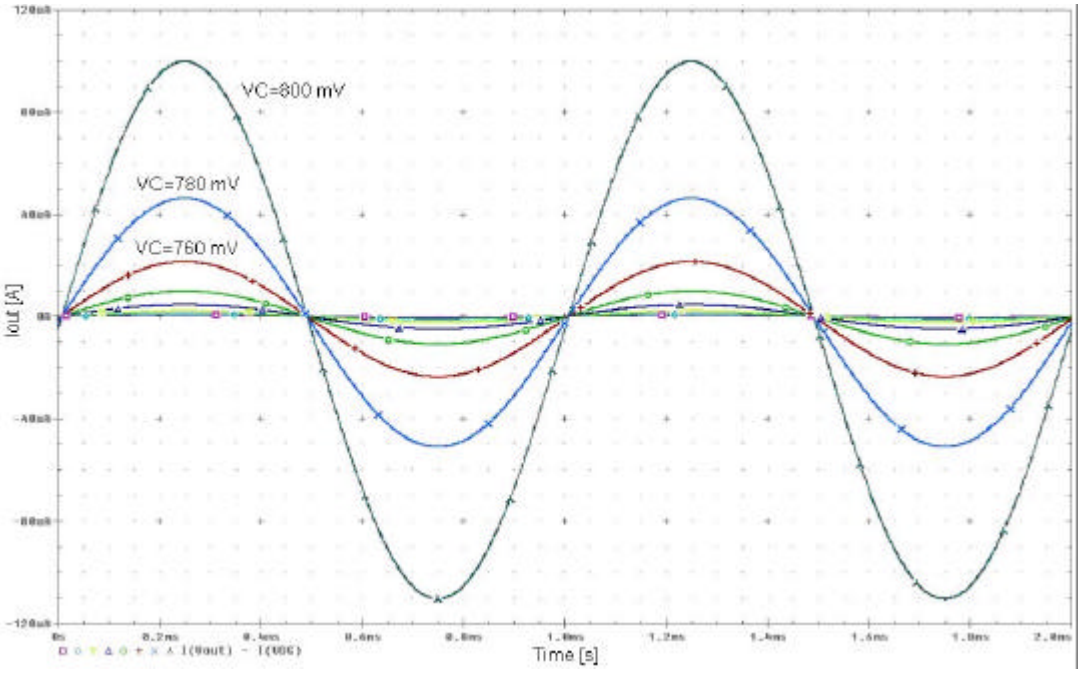


Figure 2.59: Transient simulation of the tunable current mirror with BJT differential pair with sinusoidal input for gains smaller than unity.

Table 2.10: THD values of the tunable current mirror with BJT differential pair for the gains greater than unity.

V_C (mV)	THD (%)	Input Swing
940	0.64	20nA – 2µA
920	0.37	40nA – 4µA
900	0.19	100nA – 10µA
880	0.15	200nA – 20µA
860	0.34	200nA – 40µA
840	0.14	400nA – 80µA
820	0.07	1µA – 100µA

The output current graphics which were obtained from the results of the transient simulation run with pulse input source were given in Figure 2.60 and Figure 2.61. These graphics also show the circuit has no stability problem because there is no ringing at the pulse response graphics.

Table 2.11: THD values of the tunable current mirror with BJT differential pair for the gains smaller than unity.

V_C (mV)	THD (%)	Input Swing
660	0.19	0.2µA – 200µA
680	0.18	0.2µA – 200µA
700	0.18	0.2µA – 200µA
720	0.17	0.2µA – 200µA
740	0.15	0.2µA – 200µA
760	0.12	0.2µA – 200µA
780	0.09	0.2µA – 200µA
800	0.09	0.2µA – 200µA

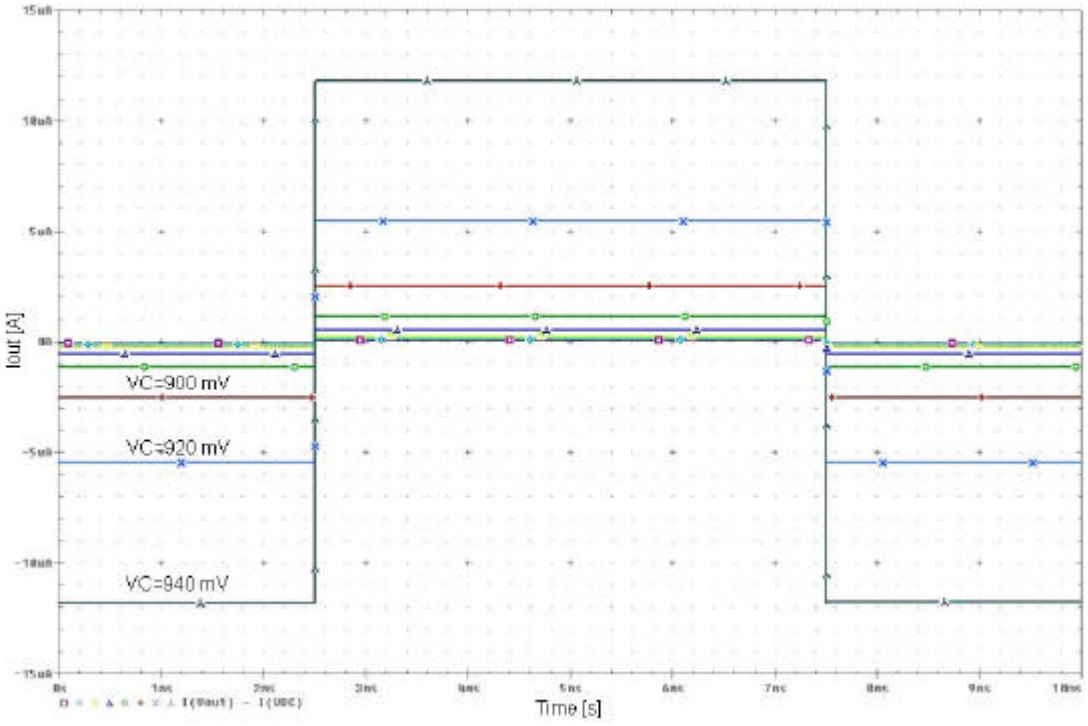


Figure 2.60: Pulse response of the tunable current mirror with BJT differential pair for the gains greater than unity.

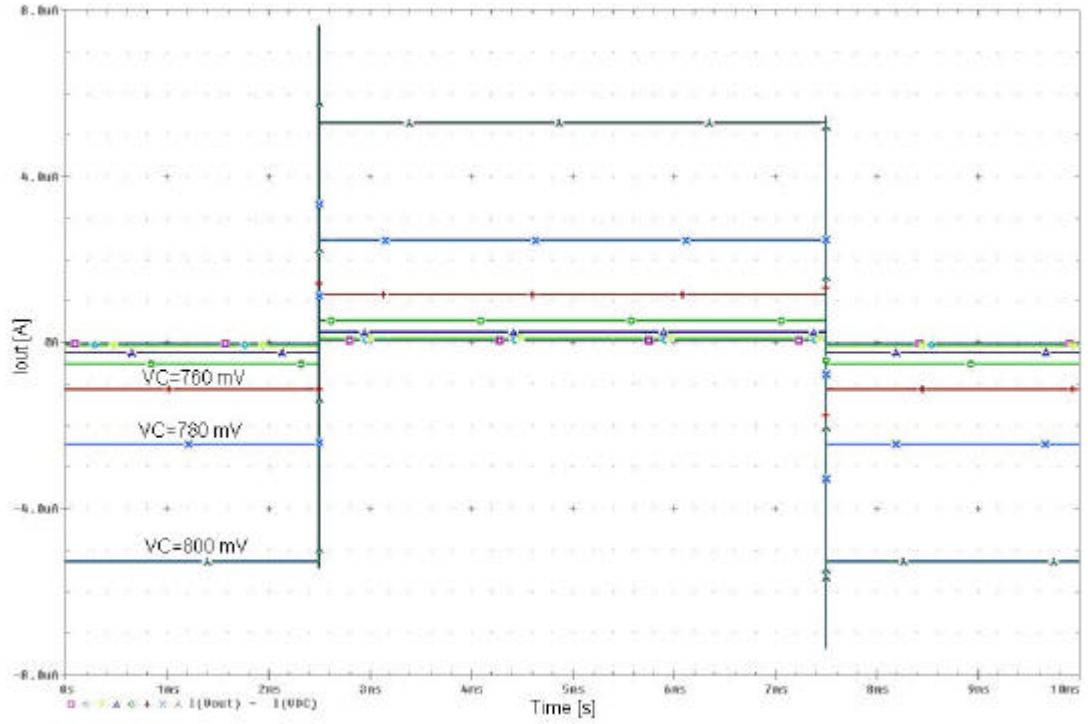


Figure 2.61: Pulse response of the tunable current mirror with BJT differential pair for the gains smaller than unity.

The layout of the PNP version of the tunable current mirror with BJT differential pair topology was created in the Cadence design environment for test circuit

production at YITAL laboratory by using the design rules of 1.5 µm CMOS process of YITAL. The PNP transistors were realized by using the parasitic transistors of the CMOS process as shown in Figure 2.53. The layout created for the tunable current mirror with BJT differential pair topology is shown in Figure 2.62 and Figure 2.63.

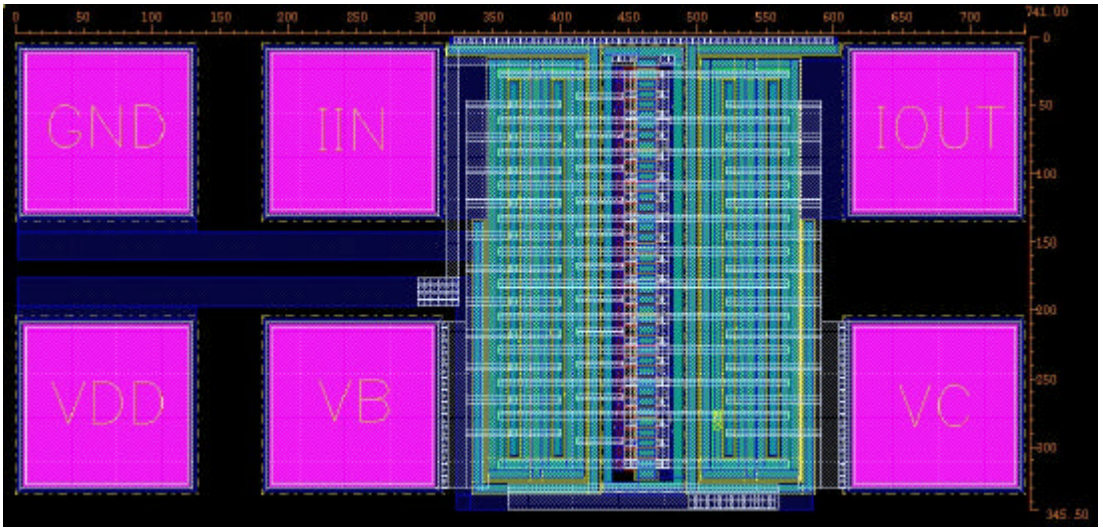


Figure 2.62: Layout of the tunable current mirror with BJT differential pair.

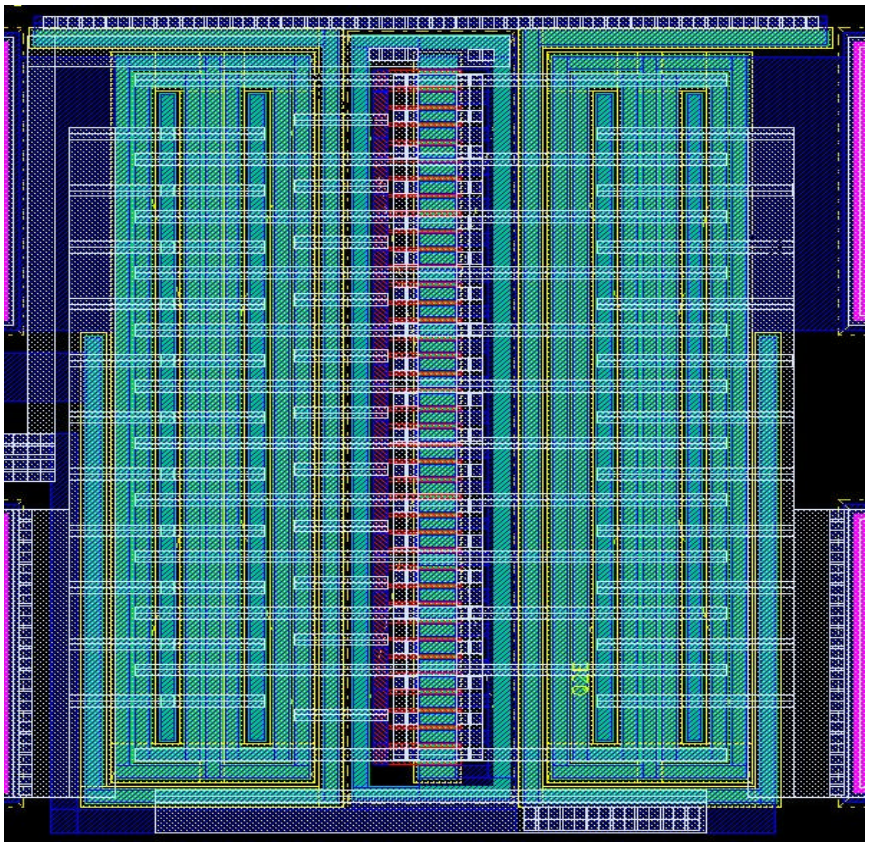
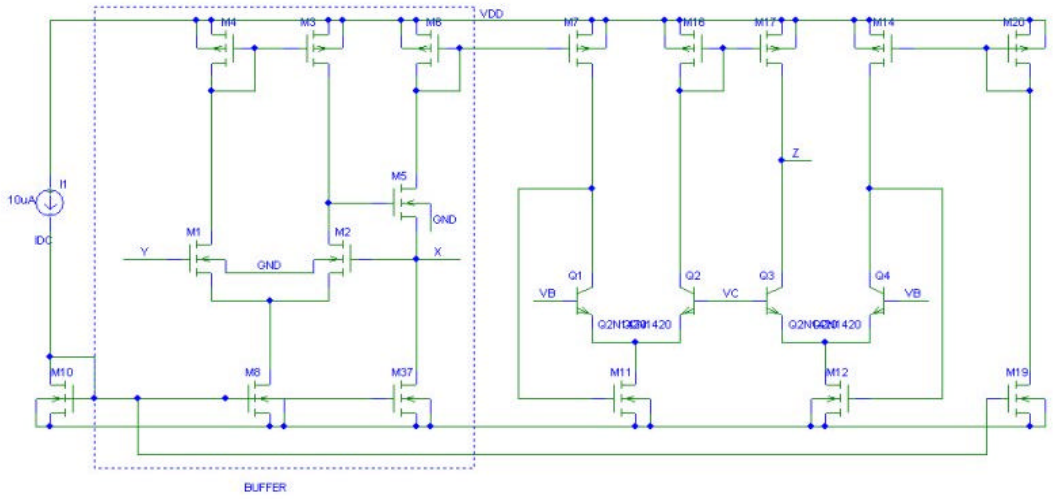


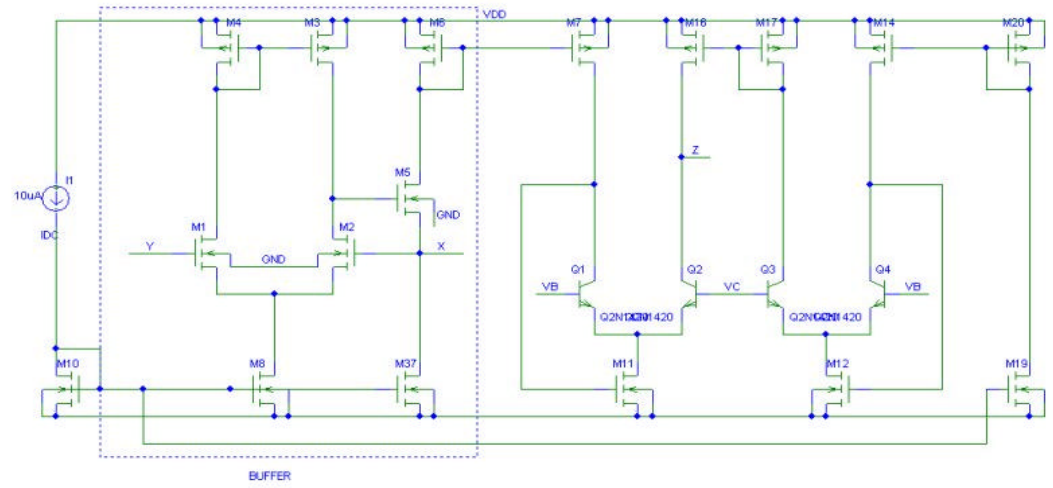
Figure 2.63: Layout of the core of the tunable current mirror with BJT differential pair topology.

2.5 Application: ECCII

Current Conveyor which is one of the main active devices used in analog system design is getting widely used due to increasing amount of current mode systems and their advantages. Designing a high performance, wide gain range Electrically Controllable Current Conveyor (ECCII) which is also used in analog filter design, provides a highly flexible tuning on analog systems [7]. To show the advantages of using current mirror as tunable devices, an ECCII realized with the proposed tunable current mirror with BJT differential pair is introduced and performance analysis are given in this section.



(a)



(b)

Figure 2.64: (a) ECCII+ schematic **(b)** ECCII- schematic.

Schematics of the designed ECCII+ and ECCII- are given in Figure 2.64(a) and Figure 2.64 (b) [7]. The input of the circuit is composed of an amplifier with a single gain stage and an output stage satisfying low output resistance connected in the unity gain configuration. The input resistance of the Y terminal of the ECCII is very high and the output resistance of the X terminal is very low due to input and output characteristic of the unity gain buffer. The Z terminal where the electrically controllability property of the ECCII is realized, is constructed by using two tunable current mirrors. One of these tunable current mirrors is used to reflect the DC current level of the output stage of the buffer while the other one reflects the output current with the same gain. As it can be seen from Figure 2.64(a) and Figure 2.64(b) the designed ECCII circuit can easily be realized in negative or positive configuration by simply changing the connection of the PMOS basic current mirror at the output.

2.5.1 Simulations

The DC simulation run to show the tunability range of the ECCII was run with a DC input voltage at the Y terminal sweeping from lower rail to upper rail. Since the gain range of the used tunable current mirror topology is very wide the current gain from X terminal to Z terminal can be very high thus to satisfy keeping the Z terminal current in the linear range of this terminal, a very low X terminal current, I_X is aimed. For this reason a very high (1M?) load resistance R_X was connected to the X terminal. The resultant graphic of the I_X current is given in Figure 2.65. This graphic shows that the buffer at the input of the ECCII can follow the input voltage at the Y terminal linearly within the range from approximately from 250mV to 3.6V.

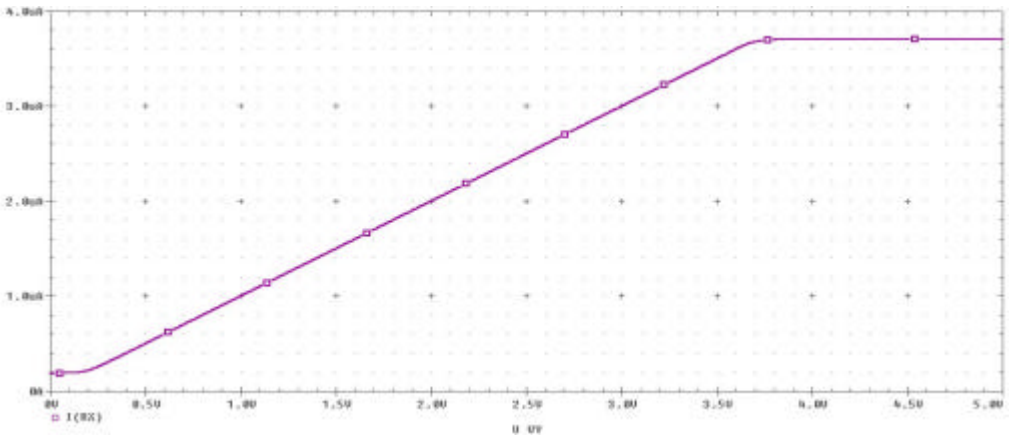


Figure 2.65: I_X current of ECCII for DC voltage sweep applied to Y.

When the DC simulation is run with V_C voltage parameter on the ECCII, the control over the ratio between the Z terminal current, I_Z and the X terminal current, I_X within the linear range of I_X can be observed. From the output graphics given in Figure 2.66, it is seen that the gain between I_Z and I_X can be controlled linearly within the operation range of the buffer. To avoid voltage clamp at the Z terminal, a small (10k?) load resistance R_Z was used. A wide gain range of 4 decades, from approximately 3.5m to 35 is satisfied.

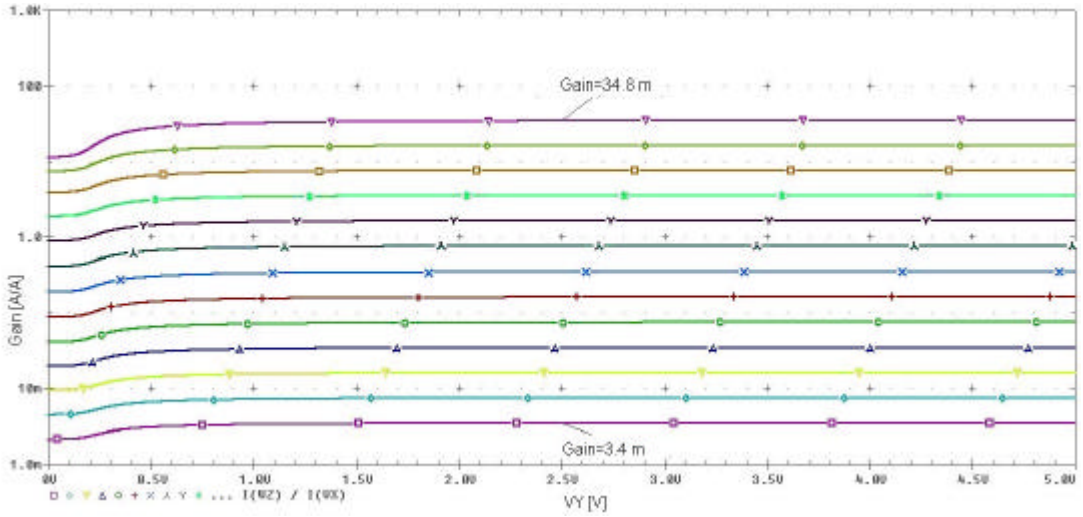


Figure 2.66: The change of the current gain of the ECCII according to V_C.

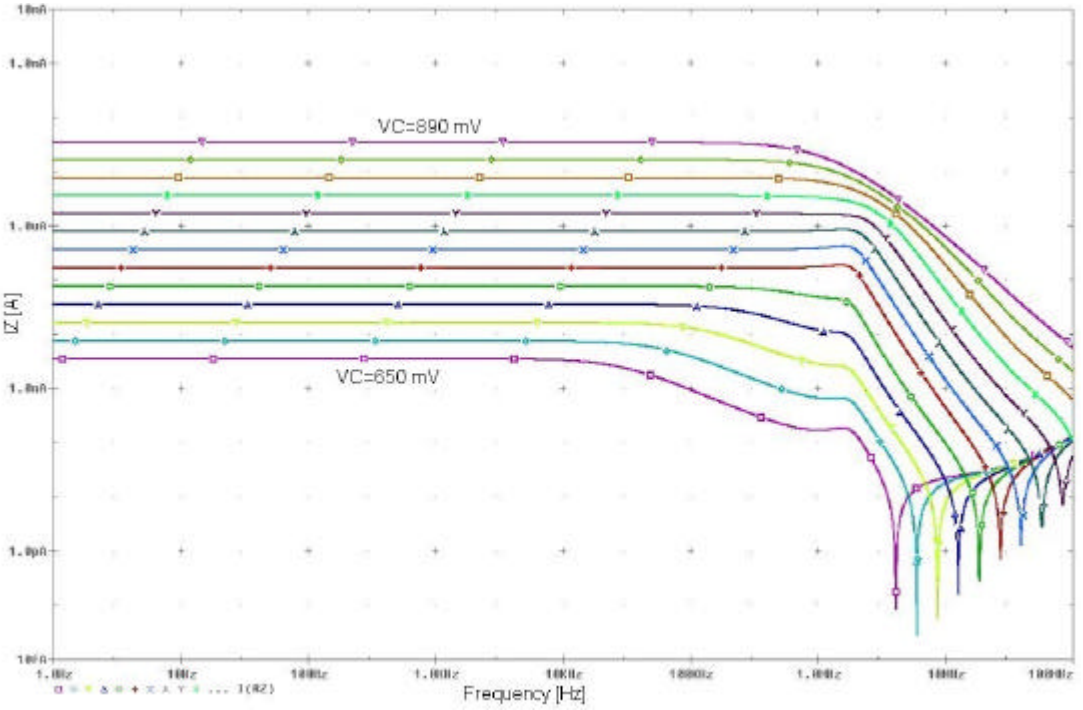


Figure 2.67: AC response of the ECCII.

The change of the tunable gain according to the frequency is obtained from the AC simulation run on the circuit. The AC simulation resultant graphics giving in Figure 2.67 also show that the circuit does not need any compensation.

For stability consideration, transient simulations with both sinusoidal and pulse input voltage sources were also run on the ECCII circuit and the obtained results are given. Since the ECCII circuits' input and output ports, Y, X and Z terminals, were biased with 2V DC voltage levels, the output graphics shown in Figure 2.68, Figure 2.69 and Figure 2.70 have a DC current level of zero ampere. Figure 2.68 shows the sinusoidal current occurred on the R_X resistance at the X terminal. For a 1 kHz sinusoidal input voltage source applied to Y terminal, with amplitude of 1.5V, swinging between 3.5V and 0.5V. The graphics in Figure 2.69 shows the Z terminal currents with for different gains for the same input source. Since a very high resistance is connected to the X terminal and a low resistance is connected to the Z terminal, the amplitude of I_X current becomes very low thus the voltage at Z terminal is not clamped.

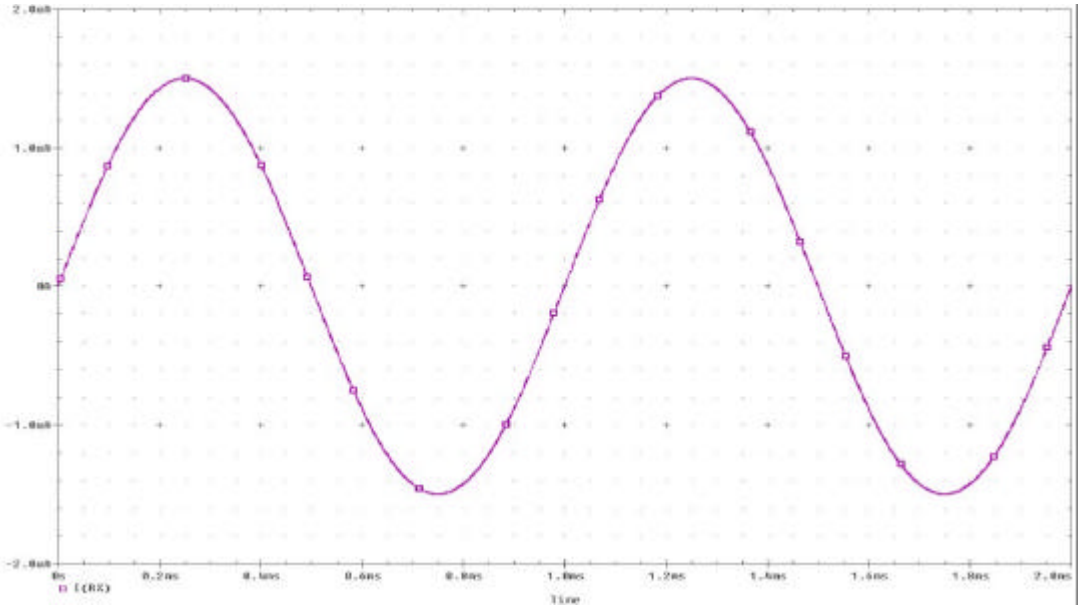


Figure 2.68: I_X current of the ECCII for sinusoidal voltage source applied to Y.

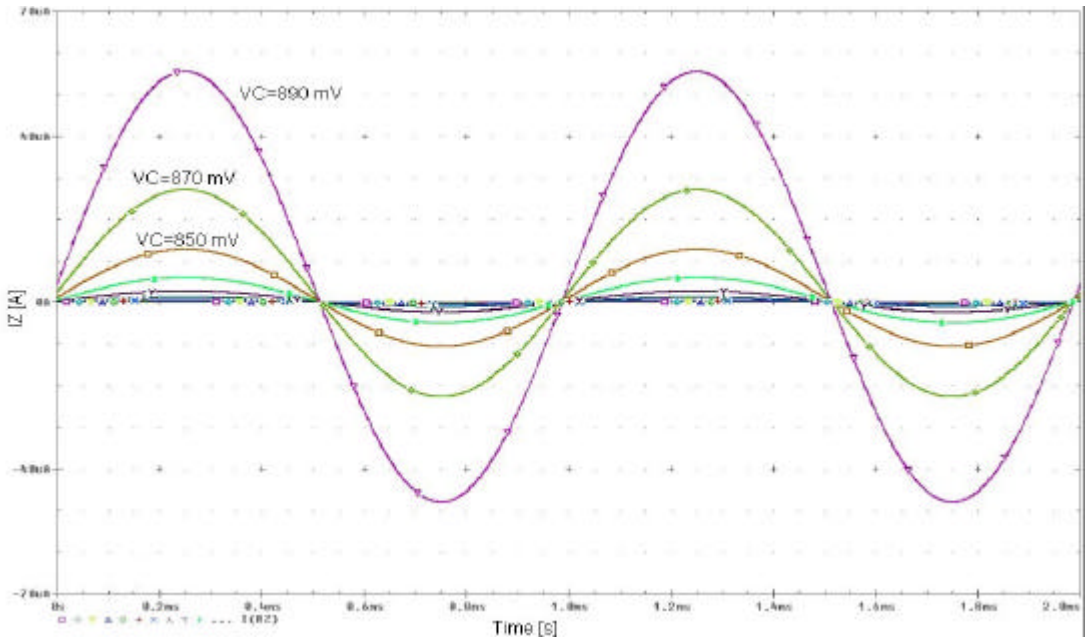


Figure 2.69: I_Z current of the ECCII for sinusoidal voltage source applied to Y.

Table 2.12: THD of ECCII.

V_C (mV)	THD (%)
650	0.69
670	0.51
690	0.47
710	0.46
730	0.45
750	0.45
770	0.45
790	0.46
810	0.47
830	0.48
850	0.51
870	0.54
890	0.70

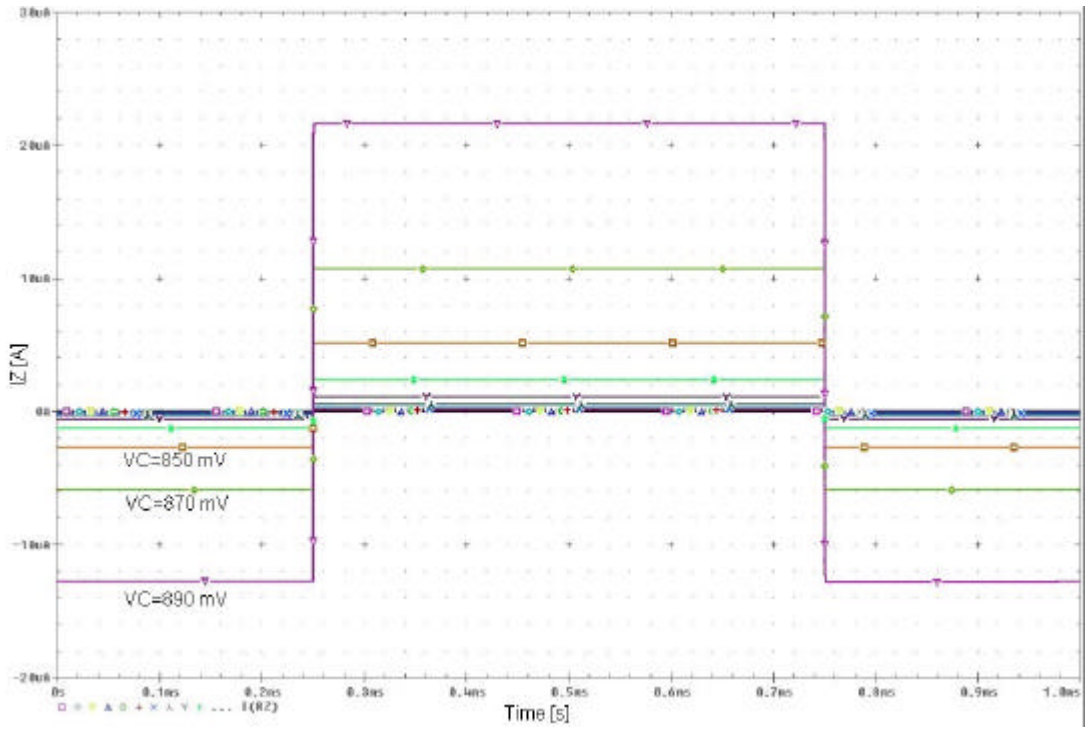


Figure 2.70: Pulse response of the ECCII.

The THD values obtained from the transient simulation with sinusoidal voltage source shows the linearity of the ECCII circuit. According to these results which are given in Table 2.12, the circuit can be tuned in a wide gain range with very high linearity.

The effect of the linearity of the circuit is seen in the pulse response graphics for different gains shown in Figure 2.70 There occurs no ringing in the pulse response of the circuit.

3. CONCLUSION

Four new tunable linear current mirror topologies were introduced as an alternative to commonly used tunable devices and their design and simulations were given in detail. According to the simulations results, wide ranges of tuning for wide ranges of linear operation were achieved. Although the first two topologies which are using triode MOSFETS to achieve tuning with different approaches can supply about a decade of tuning the gain range, the last two topologies using the BJT differential pairs' linear transition characteristic to satisfy high linearity can achieve five decades of tuning the gain range. Especially the last topology has the advantage of simplicity and low power consumption besides its highly linear operation with a very wide tuning range. However, its input resistance is higher and the output resistance is lower than the other topologies.

Table 3.1: Performance parameters of the proposed tunable linear current mirrors.

	Tunable Current Mirror with Triode MOSFETs	**Tunable Current Mirror with VGAs**	**Tunable Current Mirror with Current Dividers**	**Tunable Current Mirror with BJT Differential Pair**
Gain Tuning Range	0.5 - 2	0.33 - 3	3m - 300	3m - 300
Input Current Range (For Linear Operation)	1µA - 100µA	10µA - 100µA	8µA - 800µA	0.2µA - 200µA
THD (Maximum Value Within the Linear Operation Range)	1.2%	2,0%	0.25%	0.64%
Band Width at Unity Gain	6.4 MHz	10 MHz	1.5 MHz	9.7 MHz
Input Resistance Within Linear Operation Range	1.17k? - 27.01k?	1.17k? - 3.55k?	32.77? - 3.25k?	2.83k? - 46.81k?
Output Resistance Within Linear Operation Range	35.5G? - 48.26G?	40.73G? - 55.6G?	989.5G?	371.5k? - 0.19G?
Power Dissepation	64.4µW	83.9µW	50µW	0
Number of Transistors	15	31	19	3

In the third topology the input and output resistance performances are very high according to other topologies but it has the lowest band width among others. Some performance parameters showing the trade-off between the four proposed topology were given in the Table 3.1.

To express the easily applicability of the tunable current mirror structures, an ECCII circuit was designed and simulated as an application. Wide tuning range and high linearity are also obtained from the simulation results of the ECCII circuit.

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APPENDIX

Table A.1: 0.5µm Level 3 CMOS process parameters.

Parameter	NMOS	PMOS	Parameter	NMOS	PMOS
UO	460.5	100	GAMMA	0.69	0.76
TOX	1.0E-8	1.0E-8	KAPPA	0.1	2
TPG	1	1	AF	1	1
VTO	0.62	-0.58	WD	0.11E-6	0.14E-6
JS	1.8E-6	0.38E-6	CJ	76.4E-5	85E-5
XJ	0.15E-6	0.1E-6	MJ	0.357	0.429
RS	417	886	CJSW	5.68E-10	4.67E-10
RSH	2.73	1.81	MJSW	0.302	0.631
LD	0.04E-6	0.03E-6	CGSO	1.38E-10	1.38E-10
ETA	0	0	CGDO	1.38E-10	1.38E-10
VMAX	130E3	113E3	CGBO	3.45E-10	3.45E-10
NSUB	1.71E17	2.08E17	KF	3.07E-28	1.08E-29
PB	0.761	0.911	DELTA	0.42	0.81
PHI	0.905	0. 905	NFS	1.2E11	0.52E11
THETA	0.129	0.120			

Table A.2: Parameters used for the simulations of the BJT transistors.

Parameter	NPN	PNP	Parameter	NPN	PNP
IS	14.34E-15	650.6E-18	CJC	9.393E-12	29.52E-12
XTI	3	3	MJC	0.3416	0.5383
EG	1.11	1.11	VJC	0.75	0.75
VAF	74.03	115.7	FC	0.5	0.5
BF	255.9	70.35	CJE	22.01E-12	19.82E-12
NE	1.307	1.829	MJE	0.377	0.3357
ISE	14.34E-15	180.5E-15	VJE	0.75	0.75
IKF	0.2847	1.079	TR	46.91E-9	119.9E-9
XTB	1.5	1.5	TF	410E-12	757.7E-12
BR	6.092	4.146	ITF	0.6	0.65
NC	2	2	VTF	1.7	5
ISC	0	0	XTF	3	1.7
IKR	0	0	RB	10	10
RC	1	0.715			

BIOGRAPHY

I had the B.Sc degree from Istanbul Techinical University in 2003 at which my area of interest was VLSI design. I prepared a graduation project on Sigma Delta Analog to Digital Converters. I have attended to Istanbul Technial University again in 2003 for M.Sc. degree in Electronics Engineering master degree program where I am still enrolled in. My recent study area is analog IC design. I am working as an IC design Engineer in TUBITAK-UEKAE-YITAL since August, 2005.