İSTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

A NOVEL MICRO PIEZOELECTRIC ENERGY HARVESTING SYSTEM

Ph.D. Thesis by

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Department: Electronics and Communication Engineering

Programme: Electronics Engineering

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YENİ BİR MİKRO PİEZOELEKTRİK ENERJİ HARMANLAYICI SİSTEMİ

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August, 2007 **Tolga KAYA**

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ABBREVIATIONS

ALF : Assisted Living Facilities
ANSI : American National Standards Institute
ASK : Amplitude Shift Keying
AWGN : Additive White Gaussian Noise
BCB : Benzo Cyclo Butene
BER : Bit Error Rate
BOE : Buffered Oxide Etch
DARPA : The Defense Advanced Research Projects Agency
DFF : D-Type Flip Flop
DOD : Department of Defense
DRIE : Deep Reactive Ion Etching
ECG : Electro Cardiogram
EEPROM : Electrically Erasable and Programmable Read Only Memory
EPC : Electronic Product Code
EPROM : Electrically Programmable Read Only Memory
FCC : Federal Communications Commission
FEA : Finite Element Analysis
FeRAM : Ferroelectric Random Access Memory
FLIR : Forward Looking Infrared
FN : Fowler-Nordheim
HEI : Hot Electron Injection
HVAC : Heating Ventilating and Air Conditioning
IC : Integrated Circuit
ICAO : International Civil Aviation Organization
IEEE : Institute of Electrical and Electronics Engineering
KOH : Potassium Hydroxide
LF : Low Frequency
MEMS : Micro Electro Mechanical Systems
MNOS : Metal Nitride Oxide Silicon
MPPC : Modified Pulse Pause Coding
MR : Magnetoresistivity
MRAM : Magnetic Random Access Memory
MTJ : Magnetic Tunneling Junction
NRZ : Non-Return to Zero
NVM : Non-volatile Memory

NVRAM : Non-Volatile Random Access Memory
OOK : On-Off Keying
PDF : Probability Density Function
PDMS : Poly Di Methyl Siloxane
PECVD : Plasma Enhanced Chemical Vapor Deposition
PPC : Pulse Pause Coding
PSK : Phase Shift Keying
PVDF : Poly Vinylidene Fluoride
PZT : Lead Zirconate Titanate
RFID : Radio Frequency Identification
RIE : Reactive Ion Etching
SCCM : Cubic Centimeters per Minute
SEM : Scanning Electron Microscopy
SOI : Silicon on Insulator
SONOS : Silicon Oxide Nitride Oxide Silicon
TREAD : Transportation Recall Enhancement, Accountability, and Documentation Act
UHF : Ultra High Frequency
UMC : United Microelectronics Corporation
UPS : United Parcel Service
UWB : Ultra Wide Band

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A NOVEL MICRO PIEZOELECTRIC ENERGY HARVESTING SYSTEM

ABSTRACT

In this thesis, a novel, vibration based micro energy harvester system has been proposed. The modeling, design and fabrication of the devices have been carried out. There are several propositions in this thesis. The biggest claim is to achieve high power density levels with a mm^3 device by using a novel vibration based mechanical structure. The operating regime is non-linear unlike its conventional counterparts, which yields to generate more electrical energy. The proposed packaging method of the device is very simple and easy to realize. In addition to the mechanical propositions, a novel batteryless active RFID transponder based on the proposed design has been suggested. In this context, a new modulation method has also been proposed.

The mechanical structure of the device is based on a clamped-clamped beam where four tethers share a thick proof mass. The proof mass is used in order to bring the first eigenfrequency of the system below 50Hz; this enlarges the operating frequency range. The surface of the proof mass also acts as a platform for the sensor circuits.

Vibrations or sudden movements force the mechanical structure to not only bend but also stretch, thus it works in the non-linear regime. The piezoelectric thin film layer on the silicon tethers converts the mechanical stress into electrical energy. Microwatts of power can be achieved with a mm^3 device which yields power density levels on the same order those of solar panels. This device is named as "smart sand", because it has sensor capabilities that can store information, its size is almost that of a sand grain and the main material used for the fabrication is silicon.

The modeling and design of the mechanical structure has been developed by using COMSOL™ (a finite element analysis (FEA) tool) and SIMULINK™ (an extension tool of MATLAB™). Firstly, the stress levels have been calculated and the transient response of the structure has been investigated. Then, the theoretical analysis has been combined with these two tools and expected power density levels have been found.

The fabrication of the "smart sand" has also been developed in this thesis. Bulk micromachining techniques have been used in order to form the proof mass. The piezoelectric thin film layer has been deposited onto the tethers by a sol-gel method. Electrodes of the piezoelectric layer have been fabricated by the lift-off process. The packaging has been embedded into the fabrication process, which reduces the handling issues during the process. An elastomer (poly dimethyl siloxane, PDMS) which is cheap and very easy to pattern and handle has been used for the packaging which has not been tried before.

The "smart sand" serves as a typical accelerometer which senses the continuous vibrations or sudden accelerations. In order to further develop the sensor capabilities of the system, a new approach called "smart RFID" has been proposed; this is a

platform where the device has been combined with the RFID concept. In this context, a self-powered, energy harvesting RFID transponder has been designed. The circuitry has the capabilities of sending and receiving 64 bits of data. The 64-bit memory has been constructed with the magnetic random access memory (MRAM) cells. Several bits have been reserved for the acceleration or temperature data. When a sudden or continuous acceleration happens, the “smart sand” generates voltage and this voltage is used to write the memory bits without the need of a battery. Therefore, the “smart RFID” platform behaves like a batteryless active RFID transponder. In order to determine whether the adequate voltage level is reached or not, a mechanical relay has been proposed and its design has been investigated.

Several applications have been proposed to use the “smart RFID” platform, such as continuous acceleration monitoring in package delivery, self-powered sensors for homeland security, temperature monitoring of perishable food item delivery and a batteryless heart rate sensor. Their feasibilities have been investigated and discussed.

As a result, mechanical structure has been designed, modeled and fabricated. On the other hand, circuit level simulations have been performed but not implemented.

At the end of this work, attained results have been discussed and recommended future works have been given.

YENİ BİR MİKRO PİEZOELEKTRİK ENERJİ HARMANLAYICI SİSTEMİ

ÖZET

Bu tezde, yeni bir titreşim tabanlı mikro enerji harmanlayıcı sistemi önerilmiştir. Elemanların modellemesi, tasarımı ve üretimi gerçekleştirilmiştir. Tez içerisinde bir çok yeni öneri getirilmiştir. En büyük iddia; yeni, titreşim temelli mm^3 boyutunda mekanik bir yapı kullanarak yüksek güç yoğunluğuna ulaşmaktır. Sistem, geleneksel eşdeğerlerinden farklı olarak doğrusal olmayan bir çalışma rejiminde çalışarak daha çok elektrik enerjisi üretmektedir. Önerilen kılıflama yöntemi çok basittir ve gerçeklemesi kolaydır. Mekanik önerilere ek olarak, önerilen yapı tabanlı yeni bir pilsiz aktif RFID etiketi düşünülmüştür. Bu bağlamda, yeni bir modülasyon yöntemi de önerilmiştir.

Elemanların mekanik kısmı iki taraftan kıskaçlı bir kiriş yapısına benzer; dört adet ince bağlantı kalın bir kütleyi paylaşmaktadır. Bu kütle, ilk özdeğer frekansını 50Hz'in altına çekerek çalışma aralığını genişletmek için kullanılır. Kütlenin yüzeyi aynı zamanda algılayıcı devreleri için bir zemin görevi görür.

Titreşimler ve ani hareketler mekanik yapının sadece eğilmesine değil, aynı zamanda gerilmesine yol açarak doğrusal olmayan rejimde çalışmayı sağlar. Silikon bağlantılar üzerindeki piezoelektrik ince film tabakası mekanik gerilmeyi elektrik enerjisine çevirir. Mikrowatt mertebesinde güç seviyeleri mm^3'lük elemanlarla elde edilebilir, bu da güneş panellerinde elde edilen güç yoğunlukları kadar yüksektir. Algılayıcı kabiliyeti sayesinde bilgi depolayabilen, kum tanesi büyüklüğünde olan ve üretiminde kullanılan temel malzeme silikon olan bu elemanlar "zeki kum" olarak isimlendirilmiştir.

Mekanik elemanların modelleme ve tasarımı COMSOL™ (bir sonlu eleman analizi programı) ve SIMULINK™ (MATLAB™ programının bir uzantısı) kullanılarak geliştirildi. İlk olarak, gerilme seviyeleri hesaplandı ve yapının geçici hal cevabı incelendi. Daha sonra, teorik analiz, bu iki program ile birleştirildi ve beklenen güç yoğunluk seviyeleri bulundu.

Bu tezde "zeki kum" elemanlarının üretimi de yapılmıştır. Kütlenin oluşturulmasında taban aşındırma yöntemleri kullanılmıştır. İnce piezoelektrik film tabakası jel çözeltisi kullanılarak serilmiştir. Piezoelektrik tabakanın elektrotları ise kaldırma yöntemi kullanılarak yapılmıştır. Kılıflama işlemi, üretim sürecinin içine gömülmüştür; bu da süreç esnasındaki taşıma problemlerini azaltmıştır. Kılıflamada, daha önce denenmemiş bir yöntem olarak şekillendirilmesi çok kolay ve ucuz bir malzeme olan bir elastomer (poly dimethyl siloxane, PDMS) kullanılmıştır.

Zeki kum elemanları sürekli titreşimleri ya da ani ivmelenmeleri algılayan tipik bir ivmeölçer gibi davranmaktadır. Sistemin algılayıcı kabiliyetlerini daha da geliştirmek için yeni bir yaklaşım olan ve RFID kavramını içeren "zeki RFID" platformu önerilmiştir. Bu bağlamda, bir RFID etiketi tasarlanmıştır. Devre 64 bitlik bir veriyi gönderebilmekte ve alabilmektedir. 64 bitlik bu bellek manyetik yaz-oku bellek

(MRAM) hücreleri ile oluşturulmuştur. Bazı bitler ivme veya sıcaklık bilgisi için ayrılmıştır. Ani veya sürekli bir ivme oluştuğunda, “zeki kum” elemanları gerilim üretir ve bu gerilim pile ihtiyaç duymadan bellek bitlerinin yazılması için kullanılır. Bu nedenle, “zeki RFID” platformu pilsiz aktif RFID etiketleri gibi davranır. Yeterli gerilim seviyesine ulaşılıp ulaşılmadığını belirlemek amacıyla mekanik bir röle önerilmiş ve tasarımı incelenmiştir.

“Zeki RFID” platformunun kullanılması mümkün birçok uygulama önerilmiştir. Bu uygulamalar, paket taşımacılığında sürekli ivme denetleme, sınır güvenliği için kendinden beslemeli algılayıcılar, çabuk bozulan yiyeceklerin taşımacılığında sıcaklık denetleme ve pilsiz kalp atışı algılayıcı olarak sayılabilir.

Sonuç olarak, mekanik yapının tasarımı, modellemesi ve fabrikasyonu yapılmıştır. Öte yandan, devre düzeyi benzetimler gerçekleştirilmiş fakat üretime gidilmemiştir.

Bu çalışmanın sonunda, ulaşılan sonuçlar tartışılmış ve gelecekte yapılması öngörülen çalışmalar verilmiştir.

1. INTRODUCTION

1.1 History and Motivation

The development of Micro Electro-Mechanical Systems (MEMS) has opened up the possibility of making and using micro sensor networks and actuators in many application fields, which has led to a large research effort recently. Most current designs use batteries as power sources, which have a relatively short life time and require replacement after depletion. However, the micro sensor devices are often placed at locations without easy access, and true micro devices are of very tiny sizes (~mm^3). For these devices, battery changing is not easy, often impractical, and even impossible for some applications. Concerns over relatively short battery life have restricted wireless device applications. Therefore, researchers have been looking for alternative power sources. A possible and promising solution is based on the idea of harvesting or scavenging ambient energy from the environment and converting it to electricity, thus eliminating the need for batteries and extending the device lifetime deployment duration dramatically or even indefinitely.

Among the many ambient energy sources, solar power has been considered and studied intensively. It is environmentally friendly; life time is potentially infinite, and has a relatively high energy density. There have been quite a few successful designs utilizing solar energy **(Raffaelle et al., 2000)**. However, the applications are limited to outdoors or outer space applications where sun light is abundant.

Vibration energy is a good alternative where direct sunlight or large collection surfaces are not available. HVAC systems (heating, ventilating and air conditioning), motors, heavy traffic, military equipments, human movements, etc. can all be considered as vibration energy sources. Various research groups have been working on development of micro harvesters using vibration as an energy source.

The conversion of mechanical vibration energy to electrical energy using electromagnetic coil **(Williams et al., 1996)**, variable capacitors **(Meninger et al., 2001)** or piezoelectric material **(Umeda et al., 1994)** have been studied. **Kymissis et**

al. (1998) demonstrated that heel strikes can be used as a vibration source by inserting piezoelectric stacks into shoe heels and energy can be collected by a human walking.

Other energy harvesting mechanisms include electricity generation through gas flow using a MEMS rotor **(Wiegele, 1996)**. **Holmes et al. (2004)** combines an axial-flow turbine with an axial-flux electromagnetic generator to generate electrical power when placed in an air-stream. **Strasser et al. (2003)** demonstrated a micro-scale thermoelectric generator based on polysilicon surface micromachining converting waste heat into electrical power. **Qu et al. (2001)** demonstrated the fabrication of thermoelectric generators on flexible foil substrates. **Yang et al. (2004)** showed that electricity can be generated by forcing water through a ceramic rod with no moving parts or emissions; the system utilizes the natural occurring phenomena of charge separation near a solid-liquid interface. More interestingly, energy can be also harvested from microorganisms **(Tayhas and Palmore, 2004, Rabaey et al., 2003)** by utilizing glucose as a carbon source in a microbial fuel cell. However, automated power generation from microbial glucose has not been implemented.

Among the collectable ambient energy sources discussed above, mechanical vibration energy is a very promising power source. Basically, vibration is ubiquitous in ambient environment. Under many circumstances, such as on most transportation vehicles (cars, airplanes, submarines and so on) or in many public constructions (dams, bridges, buildings and so on), vibration is significant and can be easily utilized as energy sources to support MEMS devices for various purposes.

Besides the ambient environment, human body is also a vibration source. Heart beats (~1Hz) can also create an infinite vibration which can be used as temperature and heart rate monitoring.

Sudden accelerations can also be thought as vibration sources. Considering package delivery, sudden acceleration means that the package is dropped or hit somewhere that may cause damage. This information can be written on a non-volatile memory embedded in a MEMS vibration energy harvester, and may be probed when desired. On the other hand, if those MEMS chips are spread out to the soil along the borders, human or animal tracking can be performed for surveillance monitoring.

Embedded smart sensors are used extensively from batteryless tire pressure sensors for cars to package transportation. Smart RFID tags can store their own history such as temperature changes or acceleration that the system is exposed to. Many applications are possible for such kind of tags. For example, those tags would greatly reduce the efforts on insurance issues during package delivery.

Wireless tire pressure sensors embedded with RFID technology monitor each tire pressure continuously and inform the driver in case a replacement or air is needed. U.S. Transportation Recall Enhancement, Accountability, and Documentation Act (TREAD) mandated that such kind of sensors should be embedded into front panel of each new car **(TREAD, 2004)**. Therefore, those sensors have become popular. **Roundy (2003)** has demonstrated a system that charges the sensor battery through vibrations of the moving car.

Mechanical vibrations have received great attention from various researchers as a promising power source for energy harvesting applications. The conversion from vibration energy to electric energy can be of many forms. Electrostatic energy harvesting devices are the easiest to integrate in micro systems, but they need a separate voltage source, which brings practical difficulties in many cases **(Meninger et al., 2001, Roundy et al., 2002, Miyazaki et al., 2003)**. Unlike electrostatic design, electromagnetic devices can work independently and don't require external voltage sources. But electromagnetic energy conversion can only provide an electric potential up to several tenths of a volt **(Roundy et al., 2003, Williams et al., 1996, Shearwood and Yates, 1997, Amirtharajah and Chandrakasan, 1998, El-hami et al., 2001)**. Even if piezoelectric conversion based vibration energy harvesters are claimed to be more difficult to integrate with MEMS, designs have attractive advantages including no need for voltage source and relatively high output voltage, as high as 8 Volts **(Roundy et al., 2003, Schmidt, 1986, Shenck et al., 2001, Glynne et al., 2001, Ottman et al., 2003)**.

In the rest of Chapter 1, a brief overview on energy harvesters is given. Vibration energy harvester systems are discussed and state of the art works are introduced. Examples of some commercial applications are also investigated.

1.2 MEMS Energy Scavenger Concept

1.2.1 Introduction

Wireless sensor networks are widely used for gathering and processing the information from environment **(Philipose et al., 2005)**. Using self-powered, battery-less wireless sensor nodes would greatly minimize the cost of monitoring and controlling.

In order for these nodes to be cheap and easily deployable, some specifications for the batteries can be given as follows:

- Long life time,
- Small size and form factor[1],
- No need of changing or recharging especially at hard-to-reach locations.

Due to these requirements, chemical battery cells, solar panels or other fixed energy sources are not suitable for wireless sensor nodes. Therefore, nodes that are using ambient energy sources other than solar have attracted interest in recent years.

A comparison of ambient and fixed energy sources are given in Table 1.1, adopted from **Roundy et al., (2005)**. Upper part of the table shows the fixed-energy sources and lower part (gray entries) displays the ambient energy sources.

1.2.2 Examples of Commercial Energy Harvesters

Solar panels are one of the most commonly used energy harvesters. Each solar panel cell consists of photodiodes which generate current when exposed to light. Those semiconductor components are connected in series and parallel in a matrix form in order to get high power. The BP Solar panel shown in Figure 1.1a occupies 1593mm x 790mm area and 5cm of thickness and generates 170W under direct sunlight which corresponds to 2.7μW/mm^3 **(BP Solar, 2000)**. They are warranted to 25-40 years. By covering the house roof with those panels, electricity necessary for home use can be generated. This system, including rechargeable batteries and converters, costs about $30000. Besides home use, they can be used for water

[1] The linear dimensions and configuration of a device, as distinguished from other measures of size.

pumping, marine and highway information panels. Another solar panel example is the light-powered calculators as shown in Figure 1.1b **(Casio)**.

Table 1.1: Comparison of the fixed-energy and ambient energy sources **(Roundy et al., 2005)**.

Power Source	Power density ($\mu W/cm^3$)	Energy density ($Joules/cm^3$)	Power density per year ($\mu W/cm^3/yr$)	Secondary storage needed?	Voltage regulation?	Readily available?
Primary battery	N/A	2,880	90	No	No	Yes
Secondary battery	N/A	1,080	34	N/A	No	Yes
Micro fuel cell	N/A	3,500	110	Maybe	Maybe	No
Ultra capacitor	N/A	50-100	1.6-3.2	No	Yes	Yes
Heat engine	1×10^6	3,346	106	Yes	Yes	No
Radioactive (^{63}Ni)	0.52	1,640	0.52	Yes	Yes	No
Solar (outside)	15,000*	N/A	N/A	Usually	Maybe	Yes
Solar (inside)	10*	N/A	N/A	Usually	Maybe	Yes
Temperature	40*†	N/A	N/A	Usually	Maybe	Soon
Human power	330	N/A	N/A	Yes	Yes	Soon
Air flow	380‡	N/A	N/A	Yes	Yes	No
Pressure variation	17•	N/A	N/A	Yes	Yes	No
Vibrations	375	N/A	N/A	Yes	Yes	No

* Measured in power per square centimeter, rather than power per cubic centimeter.

† Demonstrated from a 5^oC temperature differential.

‡ Assumes an air velocity of 5m/s and 5 % conversion efficiency.

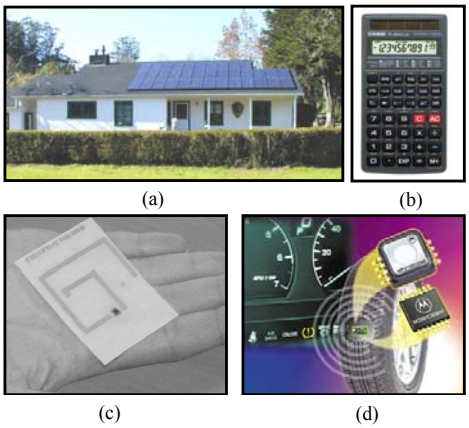


Figure 1.1: Examples of commercially available energy harvesters: (a) Solar panels for powering home appliances **(BP Solar, 2000)**; (b) Light-powered calculators **(Casio)**; (c) RFID tags **(Microchip)**; (d) Tire pressure monitoring sensors **(Motorola Inc., 2000)**.

Radio frequency powered identification (RFID) tags are used to track and monitor packages, assets, people and animals **(Sorrels, 1998)**. Passive RFID tags are battery-less as shown in Figure 1.1c. A reader sends power pulse at a specific frequency (Commonly used frequencies are 130kHz, 13.56MHz, 900MHz, 2.45GHz.) to "wake up" the reader. This power signal is converted to energy by inductive or magnetic coupling through a coil (antenna) and harvested energy is stored in a capacitor and used for powering communication circuitry. During communication, electronic product code (EPC) can be written on the memory embedded in the tag or a written data can be sent via backscattering. Therefore, RFID tags can be considered as energy harvesters, but not energy scavengers because they do not use ambient energy sources.

Motorola (2000) has already developed wireless tire pressure sensors combining RFID energy harvesters with battery powered sensors to report on the pressure of each tire to a central computer in a vehicle (Figure 1.1d). Efforts have been carried out to create a tire pressure monitoring system that recharges the battery through a vibration energy scavenger **(Roundy, 2003)**.

Smart shoes convert the heel-strike energy of a walking or running person into electricity. **Shenck and Paradiso (2001)** reported that their prototype produces 8.4mW/foot strike using Lead-Zirconate-Titanate (PZT) stacks. Taking into account the given dimensions, proposed harvester yields to 0.2μW/mm^3 of power density. Department of Defense (DOD) of U.S. is also interested in using these transducers in order to decrease the heavy battery load of a soldier (A 40kg equipment consists of 1-2kg of battery.) as shown in Figure 1.2 **(DARPA, 2002)**. Sport shoes companies (such as Nike Corporation) also find the idea attractive and work on it **(Adidas)**.

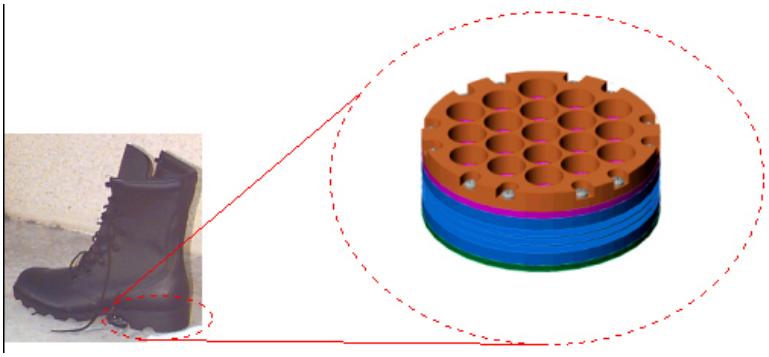


Figure 1.2: In a DARPA funded project, SRI International is developing heel-strike generators that will eventually reduce the battery weight that a soldier needs to carry during a mission.

There are few companies that have been developing piezoelectric transducers including energy scavengers. Mide Company's product, called "Volture", is capable of generating 20mW power in the presence of a significant vibration (10mm@50Hz) but the package is very large degrading the power density to 3.2nW/mm^3 **(Mide, 2005)**. Perpetuum Company has also developed piezoelectric MEMS microgenerators that have the power density of 2.7μW/mm^3 **(Perpetuum, 2004)**.

1.2.3 Piezoelectricity

The piezoelectric effect was discovered by Jacques and Pierre Curie in 1880. Piezoelectric behavior is defined as the generation of electricity from a material under pressure; it is also referred to as "direct piezoelectricity". "Converse piezoelectricity" can be defined as the phenomenon where applied voltage causes a material to change its shape. This behavior has been used in many applications such as transducers, microphones, buzzers, sensors and actuators **(Senturia, 2001)**.

There are many crystals and ceramic structures that exhibit the piezoelectric phenomena, such as crystalline quartz (SiO_2), zinc oxide (ZnO), lithium niobate ($LiNbO_3$), poly-vinylidene fluoride (PVDF), lead-zirconate-titanate ($Pb[Zr_xTi_{1-x}]O_3$ $0<x<1$, also called PZT), barium titanate ($BaTiO_3$), lead titanate ($PbTiO_3$, called PT).

Piezoelectric crystals have perovskite structures. Above the Curie temperature[2], the crystal has a cubical symmetry and does not have a piezoelectric effect (Figure 1.3a). Below this critical temperature polarization creates a net dipole as illustrated in Figure 1.3b.

A typical piezoelectric ceramic crystal lacks inversion symmetry; it can consist of an array of aligned electric dipoles within its structure when polarized as explained in Figure 1.3. Figure 1.4 illustrates the polarization effect. Without polarization, electric dipoles in the piezoelectric crystal are randomly oriented as shown in Figure 1.4a. When a strong electric field is applied, dipoles are well-oriented along the polarization axis (Figure 1.4b). Removing the electric field partially randomizes the dipoles but the crystal still consists of an electric charge because of the structure (Figure 1.4c).

[2] Above the Curie temperature, perovskite ceramic exhibits a simple cubic symmetry with no dipole moment (Moheimani and Fleming, 2006). This temperature changes with the material propery, however, it ranges between 200^{o}C to 400^{o}C (Ferroperm Piezoceramics).

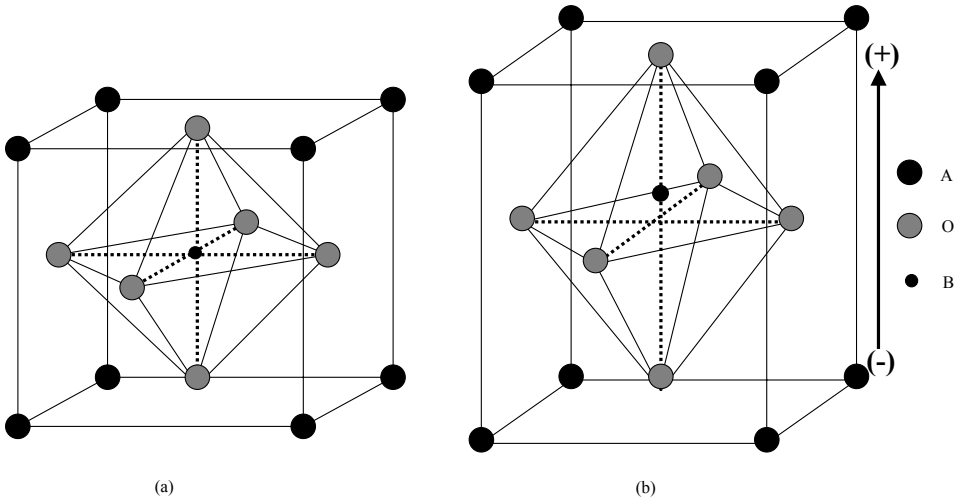


Figure 1.3: Perovskite crystalline structure which is the form of ABO_3; (a) cubic symmetry above the Curie temperature, (b) tetragonal symmetry after polarization below the Curie temperature.

After polarization, if a strain is applied to the ceramic along the polarization axis, a voltage will be generated. However, if the strain is quasi-static or DC, this voltage will be discharged through the parasitics of small DC leakage currents **(Arnau, 2004)**. Therefore piezoelectric materials are mostly effective for sensing of vibratory or resonant motions **(Senturia, 2001)**.

Analytical formulations will be given in Section 2.4.

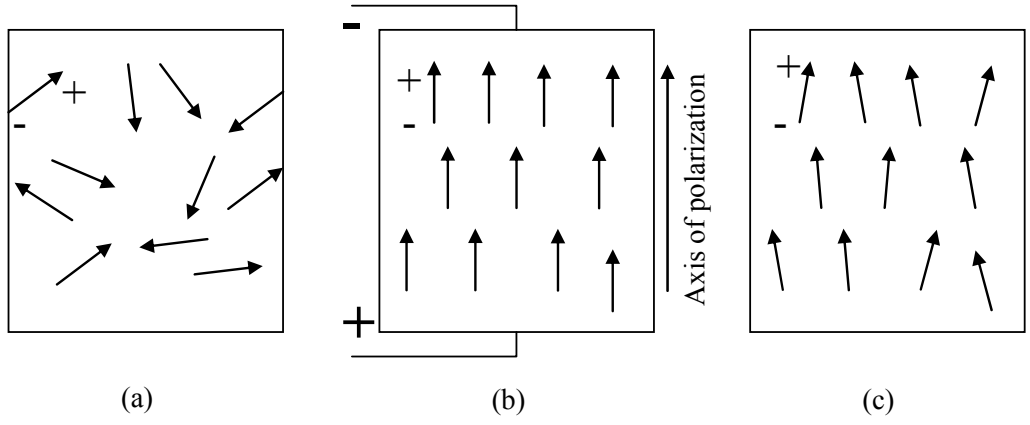


Figure 1.4: Poling procedure of the piezoelectric crystal: (a) Prior to polarization, dipoles are random oriented, (b) A large DC electric field polarizes the structure so that dipoles are oriented in the same direction, (c) Permanent polarization remains after removing the DC field.

1.2.4 Vibration Energy Scavengers

Vibration energy is a very promising alternative to solar energy where direct sunlight is not available. Furthermore, vibration based energy scavengers take outperform of solar systems at hard-to-reach locations where small form factor (~1mm^3) nodes are needed. There are three types of transducers that convert vibration into electricity: electromagnetic, electrostatic and piezoelectric, as shown in Figure 1.5.

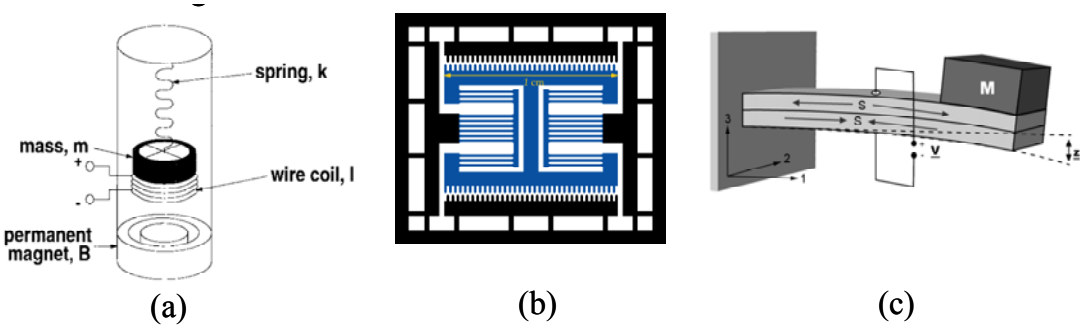


Figure 1.5: Examples of different types of vibration energy scavengers: (a) Electromagnetic **(Williams and Yates, 1996)**; (b) Electrostatic **(Miranda, 2004)**; (c) Piezoelectric **(Roundy et al., 2005)**.

Electromagnetic scavengers consist of a coil and a permanent magnet as shown in Figure 1.5a. When vibration occurs, coil moves and changing magnetic field causes a current to flow along the coil. The voltage on the coil is simply determined by Faraday's Law. Considering low-level vibrations (up to 200Hz) and a form factor of 1cm^3, an output voltage of only about 100mV can be generated. Therefore, electromagnetic vibration harvesters are not suitable for micro scale.

Electrostatic generation depicted in Figure 1.5b relies on the change of the capacitor value between its conductor layers which are moving relative to one another. Even if micro scale electrostatic transducers can generate voltages on the order of volts, there is a disadvantage that a separate voltage source is needed to start-up the charge sharing.

Piezoelectric generation uses a piezoelectric material which generates a voltage under a mechanical stress. Cantilever-based beam structures are generally used as illustrated in Figure 1.5c. The main disadvantage of this type of transducers is the fabrication complexity. If it can be tolerated, those would be very attractive for wireless sensor nodes. Table 1.2 compares these three vibration scavenging approaches.

Table 1.2: Comparison of vibration scavenging approaches.

Mechanism	Advantages	Disadvantages
Piezoelectric	No voltage source needed Output voltage 1-8V	More difficult to integrate in microsystems
Electrostatic	Easier to integrate in microsystems	Separate voltage source needed
Electromagnetic	No voltage source needed	Output voltage 0.1-0.2V

1.2.5 Current State of the Art in Piezoelectric-based Harvesters

As mentioned in the previous section, piezoelectric transducers are one of the most attractive miniature energy harvesters. Therefore, various research groups have been working to develop such transducers to use them in sensors, low-power microprocessors and wireless communication nodes **(Amiratharajah et al., 1998, Lal et al., 2005, Jeon et al., 2005, Roundy and Wright, 2004)**. Most of designs use a cantilever beam undergoing deflections and a proof-mass to tune the system to work at resonance. Resonance frequency of the transducer is adjusted to the dominant frequency component in the ambient where the system is planned to work. This tuning ensures that the mechanical response and resulting harvested energy is maximized under linear limits.

The frame where the beam is clamped is excited by the ambient vibrations. Mechanical bending of the beam creates stress and it is converted to electric energy by the piezoelectric material.

Diode bridge rectifiers are used to generate a DC voltage which is stored on a large capacitor (up to micro farads) that is used to power the wireless sensor node circuitry.

These types of transducers can be built in cm scale; however, if mm-sized devices are of concern, scaling issues arise. In order for a system to maintain the same resonant frequency after scaling, thickness of the cantilever beam should be decreased with length and width. Doing this makes the beam thickness comparable with the piezoelectric thin-film layer and affects the mechanical response of the system. Because the ambient vibration amplitude is inversely proportional to the frequency, high quality factors (Q) are needed for low frequencies. Further than a few kHz, vibration amplitudes are only on the order of nanometers.

Figure 1.6 illustrates two piezoelectric-based transducer designs. Figure 1.6a shows a cm-scale device **(Roundy and Wright, 2004)**. The 365μm thick PZT bimorph is used as a cantilever and a heavy Tungsten proof mass is attached on it to lower the resonance frequency. The vibration of the base or frame is 200μm@100Hz. Transducer generates 80μW at 13.1V for a 200kΩ load which corresponds to 40μW/cm^3 considering the packaging and the external capacitor (32μF). Figure 1.6b is a MEMS cantilever with a smaller proof mass comparing the form factor of the previous design, thus higher resonance frequency of 13.9kHz **(Jeon et al., 2005)**. The device is 170μm x 260μm without the packaging and electronics. It is reported to generate 1μW at 2.4V for a 5.2MΩ load.

1.2.6 Fundamental Limitations and a Solution Potential

There are several physical obstacles to achieve high-power density and small form factor devices with those state-of-the-art piezoelectric-based transducers. As depicted in Table 1.3, most ambient vibration sources have vibration frequencies below 200Hz. It is difficult to achieve low resonances with linear design approaches. In order to get high power efficiency, system should be operated at resonance and have high quality factor (Q) which introduces tight design specifications.

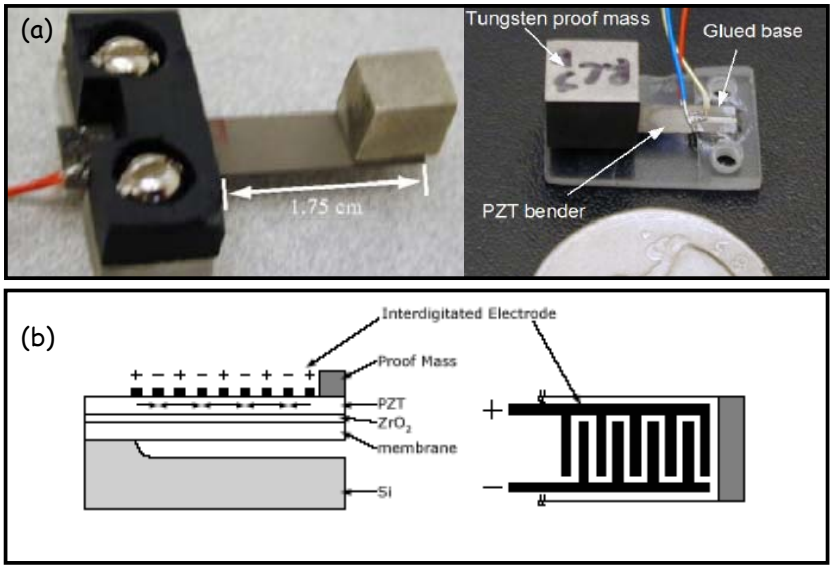


Figure 1.6: Piezoelectric vibration energy scavengers, both at (a) meso-scale **(Roundy and Wright, 2004)** and (b) micro-scale **(Jeon et al., 2005)**.

Table 1.3: Vibration frequencies and amplitudes on the surface of various typical vibration sources **(Roundy and Wright, 2004)**. The peak acceleration is at frequency below 200 Hz for almost all sources, with the peak displacement being at even lower in frequency.

Vibration source	a (m/s^2)	f_{peak}
Car engine compartment	12	200
Base of 3-axis machine tool	10	70
Blender casing	6.4	121
Clothes dryer	3.5	121
Person nervously tapping their heel	3	1
Car instrument panel	3	13
Door frame just after door closes	3	125
Small microwave oven	2.5	121
HVAC vents in office building	0.2-1.5	60
Windows next to a busy road	0.7	100
CD on notebook computer	0.6	75
Second storey floor of busy office	0.2	100

Furthermore, ambient vibration sources are practically stochastic; frequency and amplitude may vary, which shifts the optimum power generation operating point. **Elvin et al. (2001)** have proposed an adaptive tuning approach to alleviate this problem but it obviously increases the design complexity and degrades the small form factor approach.

As previously mentioned, all harvester structures in the literature are linear designs. Linearity makes the system modeling and design easier and straightforward. Therefore, vibration amplitudes are assumed not to exceed the beam thickness. Due to the fact that the maximum bending stress is located on the beam support attachment points, only a small portion of cantilever can be used for power generation, causing low efficiency. Therefore, one approach is to increase the beam width to the point where the anticlastic curvature effects show up[3] (due to a finite Poisson ratio). When the width increases, resonance frequency should be tuned again by increasing the length or making the proof-mass bigger which results an increase of the device volume.

[3] As a rule of thumb, if the beam width is 5 times larger than its thickness, anticlastic curvature affects the mechanical properties of the material; Young's modulus (a measure of the stiffness of a given material) changes with Poisson ratio (a measure of the tendency of stretching).

Several attempts have been done to increase the power efficiency by various adaptive power conversion circuitries for linear designs **(Amirtharajah et al., 1998, Elvin et al., 2001)**. However, such electronics increase the overall system volume and complexity and also the power needed for the circuitry. In some cases, power consumption of the circuits is larger than the power generated by the harvester itself **(Amirtharajah et al., 1998)**.

Considering all of the issues above, it has been discovered that nonlinear deformations are necessary to achieve high power generation. As will be described in Chapter 2, large deformation approach diminishes the dependence of the operation at resonance frequency.

1.3 Contribution

In this work, a new vibration based micro piezoelectric energy harvester system is developed with a high power density and a wide application area. In order to increase the power density;

(i) Mechanical structure is allowed to move in large amplitudes, thus working in nonlinear regime,

(ii) Thanks to the large deformation, power can be collected from stretching instead of bending, which gives higher energy levels,

(iii) (i) and (ii) ensure there is no need for the system to operate at the resonance frequency (on the order of kHz, whereas ambient vibrations are up to 200Hz) which enables the system find wider spectrum of usage.

The basic idea of the proposed system is to allow the structure to not only bend as in linear designs, but also stretch. Mechanical structure is basically a clamped-clamped beam design. Supporting beams share one proof-mass from its corners and each beam is deflected few times larger than their lengths causing non-linear deformations (This behavior will be described in detail later).

Mechanical part of the device is fabricated using standard MEMS processes such as bulk micromachining and photolithography. Silicon is used as the substrate material. All the processes are carried out taking into account that they are CMOS compatible. The proof-mass also serves as a substrate for power conditioning, sensing and

wireless transmission circuitries. Furthermore, depending on the application, a large, low leakage external storage capacitor (few nano Farads, up to micro Farad) can be placed onto the proof-mass. The antenna that is used for wireless transmission can also be part of the package.

In order to achieve high power density levels using large deformations, a novel mechanical structure is proposed in this thesis. The proposed design was modeled and simulated considering nonlinear effects. Mechanical simulations were performed using a finite element analysis (FEA) tool, COMSOL MULTIPHYSICS^{TM}[4]. Data gained from FEA was used as an input for obtaining a complete system model which was built in SIMULINK^{TM}. The cantilever based mechanical part was fabricated and preliminary tests were performed. Results have shown that the system is feasible and viable.

It is possible to power a sensor node with the scavenged energy collected from the environment. In this context, a smart RFID platform is proposed in order to use the harvester system as a self-powered sensor. This approach ensures that the sensed data is transmitted using well-known RFID protocols. Acceleration data is sensed by the mechanical part and the generated voltage enables a MEMS cantilever switch. This switch connects the voltage to a non-volatile random access memory (NVRAM) and data is written on this memory. Because all the circuitry can be fit onto the proof-mass, the RFID chip is fully integrated and suitable to batch fabrication. In order to investigate the power budget, an RFID chip was designed and simulated. The chip is also capable of writing, storing and sending 64bit ID data. In addition, a new modulation technique has been proposed and its theoretical analysis and circuit level simulations have been performed.

As part of this thesis, several potential applications were considered and their feasibility and viability were discussed; these include continuous acceleration monitoring in package delivery, self-powered sensors for homeland security, and a batteryless heart rate sensor. Besides the RFID approach, a temperature sensor which is one of the building blocks of a wireless sensor node was also designed, fabricated and tested. This node will be powered via the harvester system.

[4] COMSOL Multiphysics is a modeling software for the simulation of physical processes that can be described with partial differential equations (PDEs).

1.4 Thesis Organization

Chapter 2 focuses on the design of the proposed novel MEMS energy harvester system −called “Smart Sand”− in detail; the basic idea, configuration, and design approach. System advantages, modeling approach and mechanical part simulations are also given. The chapter concludes with the optimized structure parameters.

Fabrication of the mechanical part of the system is explained in Chapter 3. Process flow is given and processing steps are shown. Packaging method and stress test results are discussed. This chapter also gives a brief explanation on the ongoing fabrication and test results run by the project colleagues.

Chapter 4 focuses on the potential applications. After a brief introduction, the proposed smart RFID platform is introduced. RFID-based applications are proposed. Then, non-volatile memory alternatives are discussed. Design, simulation and optimization results of a power switch based on the cantilever beam are given. Afterwards, building blocks of the RFID system are shown, including the communication protocol, read/write channels, antenna considerations and simulation results. In this chapter, a wireless temperature system is also proposed and simulation, fabrication and test results are given.

Chapter 5 concludes the thesis and gives future work suggestions.

2. A NOVEL MEMS ENERGY HARVESTER SYSTEM DESIGN

2.1 The Underlying Concept

In this thesis, large deflection approach is used to achieve high power density over a wide frequency range. When using large deformations, stress is dominated by tensile stretching instead of bending. Figure 2.1 illustrates the proposed "smart sand" concept. It is smart because the proof mass also serves as a substrate material for the CMOS circuitry and generated voltage is used to sense temperature, acceleration, etc. Its size is in the order of $1mm^3$ which is the size of a large sand grain. The proposed design is based on clamped-clamped beam structure; but instead of two tethers, there are four tethers sharing one proof mass. Tethers are clamped to the proof mass at one end and to the frame on the other end.

Figure 2.2 depicts a finite element analysis (FEA) simulation where the proof mass is deflected 100µm. Here, the proof mass has an area of 2.5mm x 2.5mm and a thickness of 500µm which is a typical Silicon wafer thickness. Each tether is 3.5mm long, 100µm wide and 5µm thick. For visual inspection, rotational modes are not shown in the figure, however, they are considered in simulations.

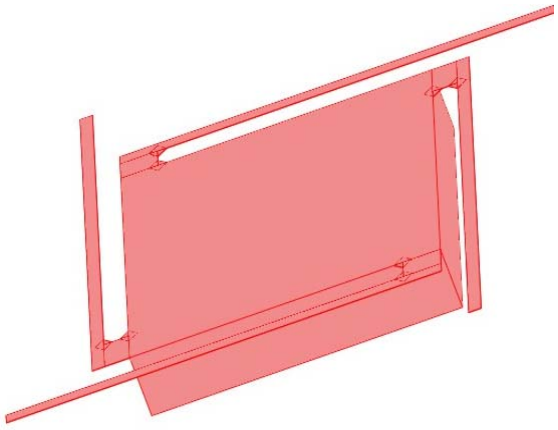


Figure 2.1: The mechanical transducer part of the "smart sand" depicting one possible design. Tethers are 3.5mm long, 100µm wide and 5µm thick.

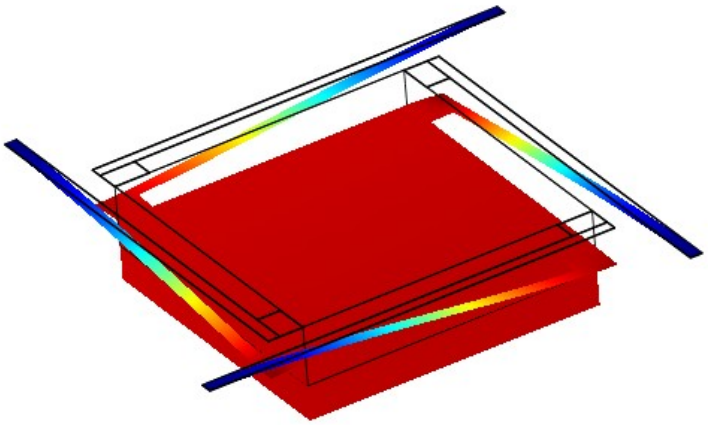


Figure 2.2: A finite element simulation that illustrates a large, nonlinear deflection (100 μm) of the proof mass. Tether clamp points not deflected are denoted with blue. Proof mass is deflected 100μm which is red.

2.2 Inherent Advantages of the Proposed Design

If a beam is deflected more than its thickness, nonlinear deformation occurs and stretching stress dominates over bending stress over most of the beam's surface. Near the beam ends, bending stress dominates and maximum stress levels appear. This behavior is illustrated in Figure 2.3 where 3mm long, 100μm wide and 5μm thick Silicon cantilever beam is deflected 100μm from one end. It can be seen that over 80% of the beam has an average uniform stress. If the piezoelectric thin-film layer covers over this area, uniform mechanical strain can be converted to voltage. It should be noted here that previously mentioned linear designs use only the beam ends which correspond to 20% of area usage.

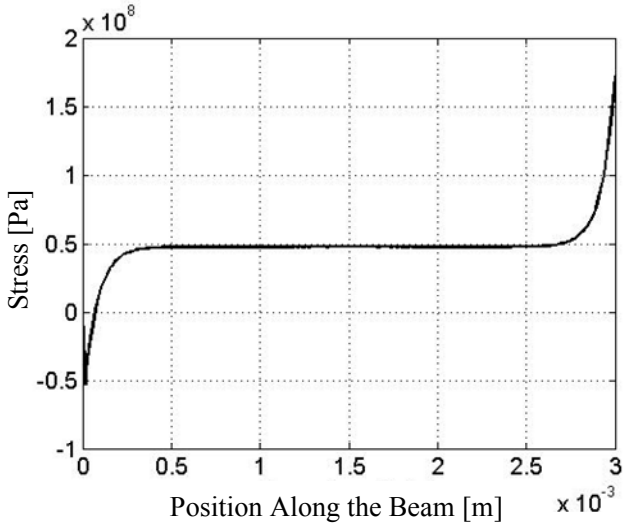


Figure 2.3: Surface stress along the length of one of the 3mm long tethers under a 100μm deflection.

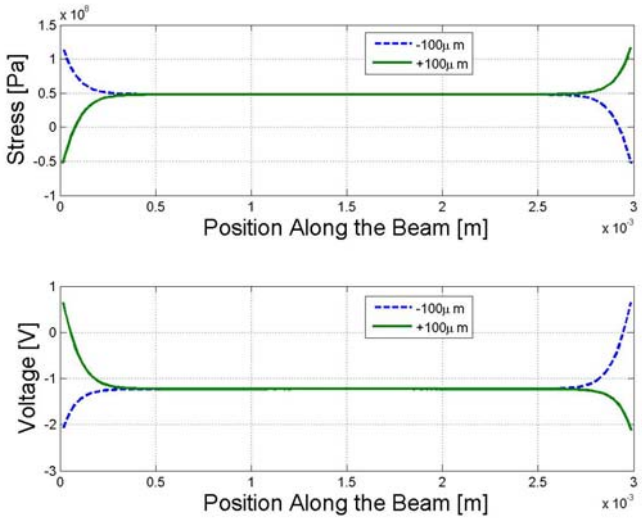


Figure 2.4: Stress and voltage values along one of the tethers.

Another inherent advantage of the system is that the generated voltage is single polarity under positive and negative deformations because both directions of deformations yield a tensile stress, but not compressive. This result is shown in Figure 2.4. Here, using COMSOL MULTIPHYSICS^{TM}, structural mechanics and piezoelectric physics domains are combined and resulting stress due to ±100μm of deflections are plotted together with the generated voltage by 2μm thick piezoelectric film.

All materials have a specific fracture strength. If this specific level is exceeded, the material can be broken or its mechanical properties can be degraded. Therefore, both piezoelectric thin-film layer and silicon should be examined in terms of their fracture strength. **Wilson et al. (1996)** reports that the fracture stress is about 500 MPa for thin silicon structures bulk micromachined from the back side. But for PZT sol-gel thin film, this value is only 50MPa **(Fett et al., 1999)**. Because uniform stress level can be maintained over beams except beam ends, for efficient energy conversion, average stress is set to 50MPa which corresponds to 100μm deflection. At the beam ends, resulting stress reaches to 100MPa which is far below the silicon fracture strength.

Figure 2.5 shows the first 6 eigenmodes[5] of the "smart sand". The structure is designed to be highly compliant so that the first set of linear resonances are below

[5] If a deformable structure is disturbed at its one of resonance frequencies, it oscillates at that frequency. Those frequencies are known as eigenfrequencies and the shapes of the oscillations are called eigenmodes.

50Hz. In this fashion, oscillations at higher frequencies (until the next set of resonances above 3kHz) result in proof mass deflections that are out of phase with the input vibrations. In this mode, the proof mass inertia proves too large for its oscillations to keep up with the frame vibrations. Hence, for most deflection amplitudes, the proof mass does not move much at all in its own reference coordinates, and the vibration amplitude of the frame becomes the deflection amplitude of the tethers. The tether deflections are not exactly sinusoidal due to spring stiffening (i.e., nonlinear effects) at large deflections. For very large vibration amplitudes (i.e., above a few tens of micrometers) the spring stiffening near the maxima of the deflections is severe enough to cause the proof mass to move in its own reference coordinates in the direction of the frame motion. An effective rule of thumb, however, is to assume that the vibration amplitude between 50Hz and 3kHz is the deflection amplitude of the tethers.

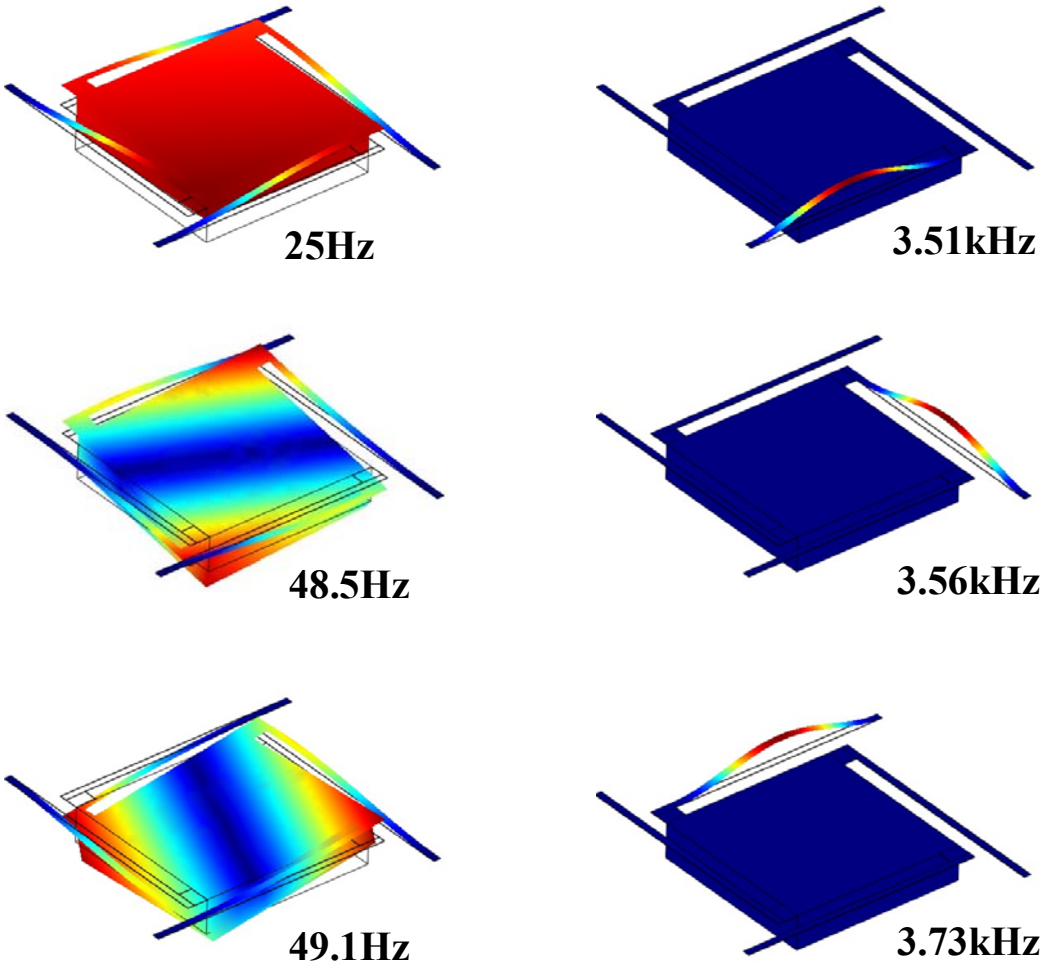


Figure 2.5: First 6 eigenmodes and eigenfrequencies of the “smart sand”.

2.3 Analytical Modeling

2.3.1 Basic Simplification for Models

As the designed geometry is complex, it is difficult to directly analyze its dynamic behavior. Therefore, the design with four tethers sharing a proof mass, *m*, shown in Figure 2.6a, is simplified to a pair of tethers that carries a proof mass, *m*/2, at the center, illustrated in Figure 2.6b. This approach is further modified as shown in Figure 2.6c where the proof mass is removed and a point load (*F*) is applied to the center of the double clamped beam. It will then be practical to make analytical studies on dynamic behavior of the mass-tether system. The beam considered in the model has a length of $L_0 = 2L$ where L is the length of each tether in the real design. The beam is clamped on both ends, and a point load is applied at the center of the beam.

2.3.2 Small Deflection Linear Model

At first, considering small deflections, a linear beam model was built. After that, the small deflection assumption was examined for its validity and necessary corrections were made for large deflections.

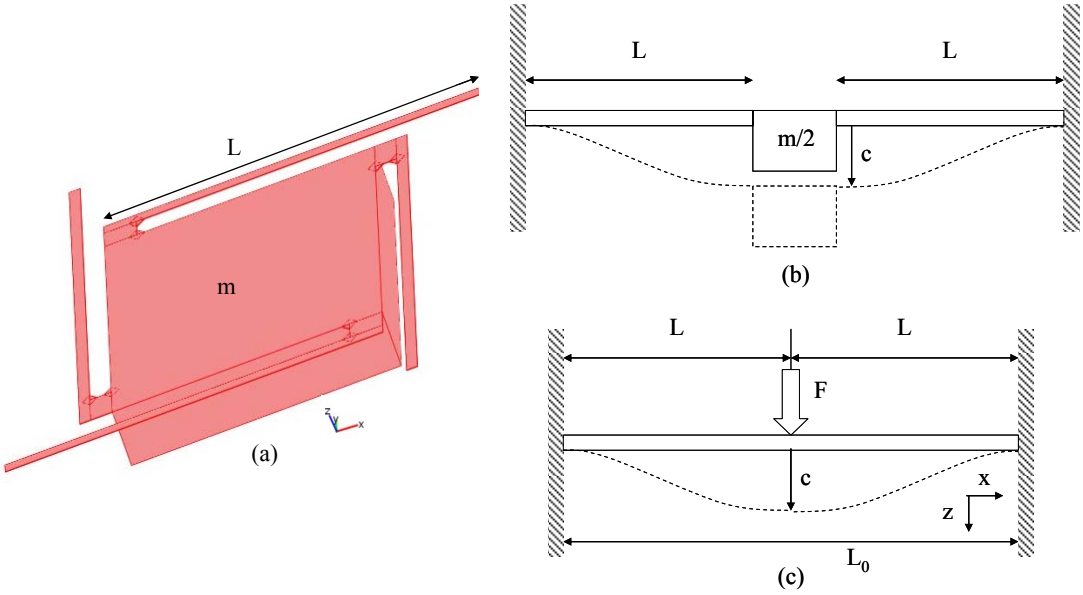


Figure 2.6: The simplification flow of the modeling procedure.

For a double-clamped beam with a point force load, F, at the center (as depicted in Figure 2.6c), it is easy to obtain its center deflection (maximum deflection) c as a function of force load **(Gere and Timoshenko, 1984)**:

$$F = 16\frac{EWH^3}{L_0^3}c \tag{2.1}$$

where E is the Young's modulus of the material. Dimension are denoted as, W is the width, H is the thickness and L_0 is the length of the beam, as shown in Figure 2.7.

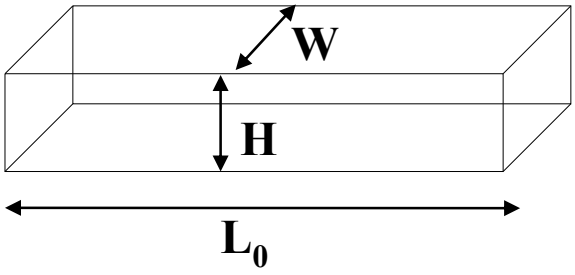


Figure 2.7: Specified beam dimensions of the beam.

The effective spring constant k can be defined by using (2.1) and the spring equation $F = kc$,

$$k = 16\frac{EWH^3}{L_0^3} \tag{2.2}$$

The system in Figure 2.6c can be modeled as a spring-mass-dashpot system as illustrated in Figure 2.8. Here, k is the effective spring constant of the entire system, and c is the displacement of the proof mass. The damping coefficient b_m corresponds to the mechanical damping; and b_e represents the damping mechanism through the piezoelectric energy conversion. Finally, y represents the base excitation of the frame where the beam ends are clamped.

The dynamic behavior of the system described above can be modeled by

$$m\ddot{c} + (b_m + b_e)\dot{c} + kc = -m\ddot{y} \tag{2.3}$$

For simplicity, damping terms b_m and b_e are combined and one damping parameter is defined;

$$b \equiv b_m + b_e \tag{2.4}$$

The base excitation is assumed to have the form;

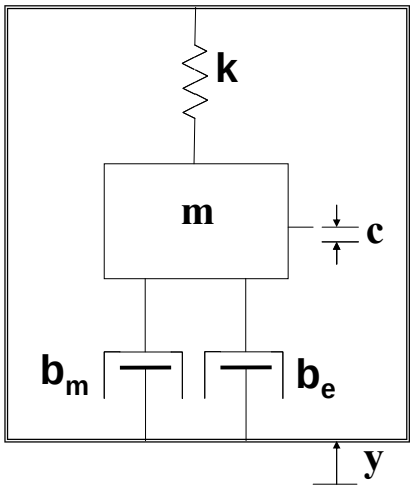


Figure 2.8: Spring-mass-dashpot model of the beam.

$$y = Y_0 e^{j\omega_b t} \tag{2.5}$$

Here, Y_0 is the amplitude of the base excitation and ω_b is the vibration frequency. Then *c(t)* becomes;

$$c(t) = \frac{m\omega_b^2 Y_0}{-m\omega_b^2 + jb\omega_b + k} e^{j\omega_b t} \tag{2.6}$$

And the magnitude of the deflection, denoted by *C*, is given as

$$C = \frac{m\omega_b^2 Y_0}{\sqrt{\left(-m\omega_b^2 + k\right)^2 + b^2\omega_b^2}} \tag{2.7}$$

Since the natural frequency of the dynamic system, ω_0, is defined as $\sqrt{k/m}$, (2.7) becomes;

$$C = \frac{m\omega_b^2 Y_0}{\sqrt{m^2\left(\omega_0^2 - \omega_b^2\right)^2 + b^2\omega_b^2}} \tag{2.8}$$

(2.8) states that, if the system is designed to resonate at the ambient vibration frequency ($\omega_b = \omega_0$), the amplitude of the vibration, *C*, tends to reach its maximum. When there is no damping ($b = 0$), the amplitude of vibration will be infinity at resonance.

If the mechanical damping is omitted (valid if the system vibrates in vacuum), then $b \equiv b_e$, and all mechanical energy lost will be converted into electric energy through piezoelectric material.

The mechanical power lost in the dynamic system of (2.6) can be expressed by

$$P = \frac{1}{2} b \dot{c}^2 \tag{2.9}$$

which reads

$$|P| = \left| \frac{1}{2} b \dot{c}^2 \right| = \frac{b}{2} \frac{m^2 \omega_b^6 Y_0^2}{m^2 \left(\omega_0^2 - \omega_b^2 \right)^2 + b^2 \omega_b^2} \tag{2.10}$$

or,

$$|P| = \frac{b\omega_0^2 \left(\frac{\omega_b}{\omega_0} \right)^4 Y_0^2}{2 \left[\left(1 - \left(\frac{\omega_b}{\omega_0} \right)^2 \right)^2 + \frac{b^2 \omega_b^2}{m^2 \omega_0^4} \right]} \tag{2.11}$$

Furthermore, if the system is designed to resonate at $\omega_b = \omega_0$, which is valid for linear designs, then above equations can be further simplified to:

$$|P|_{\omega_b = \omega_0} = \frac{m^2 \omega_b^4 Y_0^2}{2b} \tag{2.12}$$

On the other hand,

$$C_{\omega_b = \omega_0} = \frac{m \omega_b Y_0}{b} \tag{2.13}$$

or

$$b = \frac{m \omega_b Y_0}{C_{\omega_b = \omega_0}} \tag{2.14}$$

Then, substitution of (2.17) into (2.15) leads to

$$|P|_{\omega_b = \omega_0} = \frac{C_{\omega_b = \omega_0} m \omega_b^3 Y_0}{2} \tag{2.15}$$

(2.15) is important, since it links piezoelectric converted mechanical power P with deflection amplitude C, proof mass m, ambient vibration frequency ω_b and amplitude Y_0. When the system is designed to resonate at $\omega_b = \omega_0$, one will be able increase the power output through enlarging the proof mass (m), or operating the energy harvester with an ambient vibration at a higher frequency or vibration amplitude. However, it

is well known that vibration amplitude decreases with f^2. Another important result is that the power pulled out from this dynamic system (P) is linearly proportional to the deflection amplitude C. To get high power output, one needs to make the energy harvester vibrate at a large amplitude C. Based on this linear model, to achieve $0.1\mu W/mm^3$ (assuming tethers are 100μm wide, 5μm thick and 3.5mm long, sharing a 2.5mm by 2.5mm square proof mass with a thickness of 300μm) at 100Hz, the deflection amplitude will be in the order of hundreds of micrometers and thus be larger than the thickness of the tether by a factor of 100, which significantly exceeds the small deflection assumption. Hence, one will need to rebuild the mathematical model based on a large deflection assumption.

2.3.3 Large Deflection, Nonlinear Model

Since the proof mass is big compared to the tethers, typical deflection amplitudes will be at least on the same order of the tether thickness H. For such large deflection, one must include two sources of strain effects: bending and stretching. That is, if the beam bends, its length will also increase. This length increase produces some axial stress, which will stiffen the structure. It is difficult to directly solve the beam differential equation while taking into account the increase in length produced by bending. An alternative and straightforward approach based on energy methods is more appropriate for investigating the large-amplitude load deflection behavior of the doubly clamped beam **(Senturia, 2001)**.

Initially, a trial function is chosen. Because large deformations are considered, two sources of strain energy are defined; bending and stretching. Using boundary conditions and energy methods, combined with the variational solution approach, load-deflection characteristic of the beam can be found **(Senturia, 2001)**.

Using the trial shape function;

$$w(x) = \frac{c}{2}\left[1 + \cos\left(\frac{2\pi x}{L_0}\right)\right] \qquad \textbf{(2.16)}$$

The nonlinear displacement (c) as a result of a point force (F) as illustrated Figure 2.6c can be calculated as **(Senturia, 2001)**;

$$F = \left(\frac{\pi^4}{6}\right)\left(\frac{EWH^3}{L_0^3}\right)c + \left(\frac{\pi^4}{8}\right)\left(\frac{EWH}{L_0^3}\right)c^3 \quad \textbf{(2.17)}$$

(2.17) shows that the relation between the applied load force, F, and the resulting deflection c is nonlinear. The first term, linear in c, is the small-deflection bending result, proportional to the moment of inertia (i.e., to WH^3); the second term, is the stretching term, which is proportional to WH. The transition from bending-dominated behavior to stretching-dominated behavior occurs when $c \approx H$ **(Senturia, 2001)**. The thickness of the beam serves a metric to determine whether the deformation is "small" or "large".

It should be noted that (2.17) is an approximate solution. High-meshed FEA simulations should be carried out to fine-tune those approximations. These optimizations are discussed in the following section.

On the other hand, the natural frequency of the system can be estimated by using the Rayleigh-Ritz method **(Bathe, 1982)**, which states that the maximum kinetic energy and the maximum potential energy are equal at resonance **(Senturia, 2001)**. The kinetic energy of a lumped mass (W_k) is given as

$$W_k = \frac{1}{2}mv^2 = \frac{1}{2}m\left(c\omega_0\right)^2 \quad \textbf{(2.18)}$$

The maximum potential energy (W_e) is calculated at $t = 0$. Hence, this equates to the total strain energy **(Senturia, 2001)**

$$W_e = \frac{EWH\pi^4\left(8H^2 + 3c^2\right)c^2}{96L_0^3} \quad \textbf{(2.19)}$$

or,

$$\omega_0 = \sqrt{\frac{EWH\pi^4\left(8H^2 + 3c^2\right)}{48L_0^3 m}} \quad \textbf{(2.20)}$$

Here, (2.20) indicates that in order to decrease the resonance frequency, thickness of the tethers should be decreased which brings difficulties to the fabrication. Another way is to increase the length of the tethers or use bigger proof mass causing larger area consumption.

2.3.4 Optimization of the Non-linear Spring Constant

(2.17) states that the spring constant of a clamped-clamped beam has a linear and a non-linear (cubic) term. (2.20) can be simplied as

$$F = C_1\left(\frac{EWH^3}{L_0^3}\right)c + C_2\left(\frac{EWH}{L_0^3}\right)c^3 \qquad \textbf{(2.21)}$$

where C_1 and C_2 are constants which will be determined. Hence, high-meshed FEA simulations are performed and a curve fit approach is used. The displacement of one of the tethers resulting from a force applied to the center of the proof mass is plotted together with the expression in (2.21), as shown in Figure 2.9. Simulation data is obtained from COMSOL MULTIPHYSICS^{TM}. 5µm silicon tethers are covered with a 2µm PZT thin film. Here, constant terms are modified so that the fit curve is attained.

The unitless constant terms C_1 and C_2 are found to be 30 and 1.5, respectively. Hence, (2.21) becomes;

$$F = 30\left(\frac{EWH^3}{L^3}\right)c + 1.5\left(\frac{EWH}{L^3}\right)c^3 \qquad \textbf{(2.22)}$$

Here, it should be noted that, H is taken 7µm and E is considered as the Young's Modulus of the silicon for simplicity. However, it is known that PZT thin film layer is softer than silicon **(Senturia, 2001)**. Therefore, the constant terms also includes this multilayer effect.

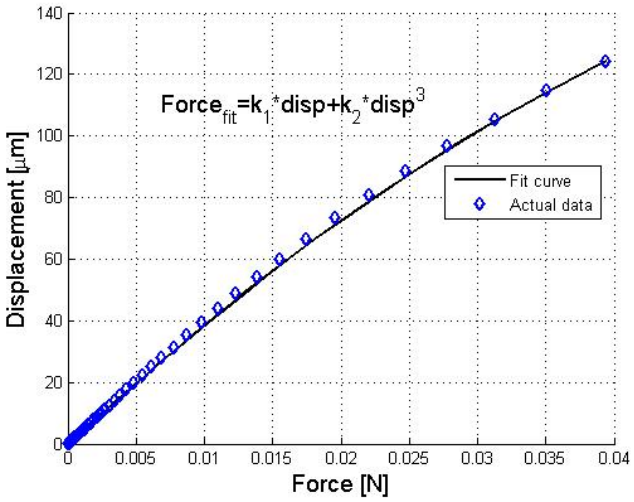


Figure 2.9: Actual force versus displacement curve on one of the tethers that are 5µm Si/2µm PZT with the fit curve.

2.4 Simulink Model

The constitutive relationship of piezoelectric materials can be modeled by two linearized equations relating mechanical and electrical behaviors. Following the piezoelectricity standards of IEEE **(IEEE-176, 1987)**, direct and converse effects can be expressed as:

$$\{S\} = [s^E]\{T\} + [d]^t\{E\} \tag{2.23}$$

$$\{D\} = [d]\{T\} + [\varepsilon]^t\{E\} \tag{2.24}$$

where $\{S\}$ is the strain vector, $\{T\}$ is the stress vector, $\{D\}$ is the electric displacement vector, $\{E\}$ is the electric field vector, $[s^E]$ is the compliance matrix evaluated at constant electric field, $[d]$ is the three by six matrix of piezoelectric strain coefficients and $[\varepsilon^T]$ is the three by three dielectric constant matrix evaluated at constant stress.

The current design converts strain energy from axial stress to electrical charge. Therefore, only the axial stress/strain component is considered in analyses. For the tethers, the relation between strain, electric displacement, stress and electric field can be simplified as **(Senturia, 2001)**:

$$S_1 = s_{11}^E T_1 + d_{33} E_3 \tag{2.25}$$

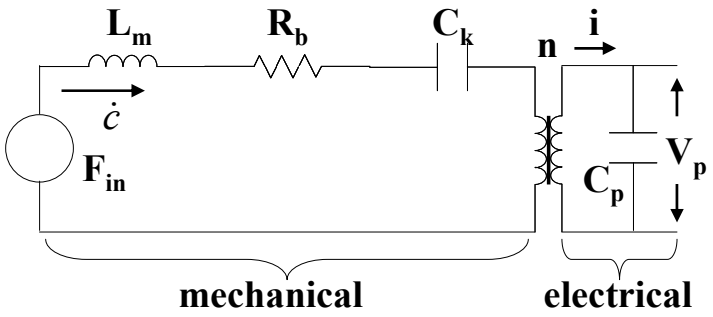


Figure 2.10: Circuit representation of the electromechanical coupling of the cantilever beam with PZT layer.

$$D_3 = d_{33} T_1 + \varepsilon_3^T E_3 \tag{2.26}$$

The electromechanical coupling can be conveniently modeled as a transformer. An equivalent circuit for the bender system is shown in Figure 2.10.

The equivalent inductor L_m represents the mass or inertia of the generator. The equivalent resistor R_b represents the mechanical damping. The equivalent capacitor C_k represents the mechanical stiffness. The force developed as a result of the vibrations in the environment is denoted with F_{in}. The transformer links the mechanical and electrical domains. Here, n represents the equivalent turns ratio of the transformer, which links the stress to the voltage. The capacitance of the piezoelectric material is C_b. The voltage across the piezoelectric device is V_p. The deflection of the beam is denoted with c. Applying Kirchhoff's law for two loops in Figure 2.10 yields:

$$F_{in} = L_m\ddot{c} + R_b\dot{c} + \frac{1}{C_k}c + nV_p \tag{2.27}$$

where,

$$F_{in} = -m\ddot{y} \tag{2.28}$$

$$L_m = m = \rho_{pm} W_{pm} H_{pm} L_{pm} \tag{2.29}$$

$$\frac{1}{C_k} = k \tag{2.30}$$

$$C_p = \frac{\varepsilon_p W_p L_p}{H_p} \tag{2.31}$$

Here, m is the mass of the proof mass and W_{pm}, H_{pm}, L_{pm} denote the dimensions of the proof mass. The density of the proof mass is denoted with ρ_{pm}. Damping coefficient, R_b, is chosen to be smaller than the air damping to avoid numerical difficulties. The capacitance value of the PZT film is C_p and it is calculated in terms of ε_p, the dielectric permittivity of PZT, and W_p, L_p, and H_p, the dimensions of the PZT.

The lumped capacitance C_k in (2.30) links the applied force to the resulting displacement, (can be interpreted as the effective spring constant) which is nonlinear as can be seen in (2.22).

The transformer relates stress to voltage at zero strain **(Roundy and Wright, 2004)**. Applying this condition to the piezoelectric constitutive relationship in equation (2.25) yields,

$$0 = s_{11}^{E} T_1 + d_{33} E_3 \tag{2.32}$$

Hence,

$$T_1 = -d_{33} E_3 E \tag{2.33}$$

where E is the Young's modulus of the piezoelectric material. The electric field is related to the voltage across the beam, as

$$E_3 = \frac{V_p}{H_p} \tag{2.34}$$

Substituting this into equation (2.33) gives;

$$T_1 = \frac{-d_{33} E}{H_p} V_p \tag{2.35}$$

Because the transformer relates stress (T) to voltage (V) at zero strain, the equivalent turns ratio n is:

$$n = \frac{-d_{33} E}{H_p} \tag{2.36}$$

The current, i, in Figure 2.10 represents the current generated as a result of the mechanical stress evaluated at zero electric field **(Roundy and Wright, 2004)**. Applying this condition to equation (2.26) yields

$$D_3 = d_{33} T_1 \tag{2.37}$$

The current i can be solved from the electric displacement as:

$$i = W_e L_e \dot{D}_3 = W_e L_e d_{33} \dot{T}_1 \tag{2.38}$$

(2.27) and (2.38) are the main system equations and it is difficult to solve these equations analytically. MATLAB SIMULINK^{TM} is used to build a system-level model. However, there are still some parameters not defined clearly.

The base excitation, y, in (2.28) is assumed to be sinusoidal for large deformations as different from (2.5)

$$y = Y_0 \sin(\omega_b t) = Y_0 \sin(2\pi f_b t) \tag{2.39}$$

where Y_0 is the amplitude and f_b is the frequency of the base excitation. Therefore;

$$\ddot{y} = \frac{d^2 y}{dt^2} = -Y_0 (2\pi f_b)^2 \sin(2\pi f_b t) \quad \textbf{(2.41)}$$

(2.38) consists of $\dot{T}$, which is the derivative of the stress with respect to time. It is hard to calculate $\dot{T}$, however, stress with changing displacements can be found easily from FEA simulations:

$$\dot{T} = \frac{dT}{dt} = \frac{dT}{dc}\frac{dc}{dt} = \frac{dT}{dc}\dot{c} \quad \textbf{(2.41)}$$

If the same approach is used while optimizing the spring constant, an equation which links the stress over the displacement can be found. Hence, average stress values on one of the tethers are obtained for displacement amplitudes up to 200μm, as shown in Figure 2.11.

A second order function can be fit to this plot. The curve fitting approach yields:

$$T = 1.0710^{16} c^2 \quad \textbf{(2.42)}$$

and the derivative of the equation with respect to the deflection gives:

$$\frac{dT}{dc} = 2.1410^{16} c \quad \textbf{(2.43)}$$

Since the generated voltage changes with the base excitation, a voltage rectification scheme should be used. Therefore, electrical part of the lumped modeling in Figure 2.10 should be expanded so that it includes the rectification behavior. Figure 2.12 shows the full-wave rectifier block that links the piezoelectric capacitance (C_p) which is defined in (2.31) with a parasitic leakage resistance (R_p) and storage capacitance (C_S) with its parasitic leakage resistance (R_S). Storage capacitance is used to power the circuitry. It should be noted here that the storage capacitance is very large with respect to the piezoelectric capacitance.

Full-wave rectifier circuit works as follows: When the input voltage (V) is larger than the output voltage (V_S) by an amount of two diode voltage drops, the diodes are "ON" and V is shorted to V_s and the current i charges the capacitor C_S, while they are discharged by R_P and R_S. Otherwise, the diodes are "OFF", the current charges only C_p, and C_S is discharged by R_S. State equations can be defined for both cases. When the diodes are "ON:"

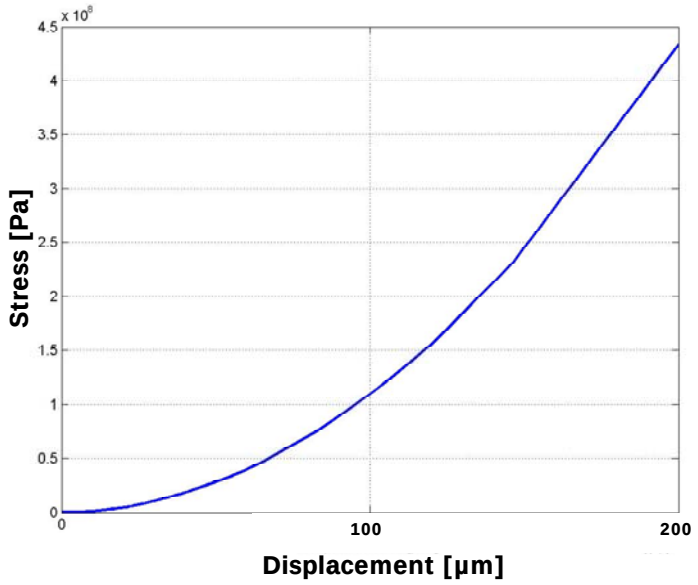


Figure 2.11: Displacement versus the average stress along one of the tethers.

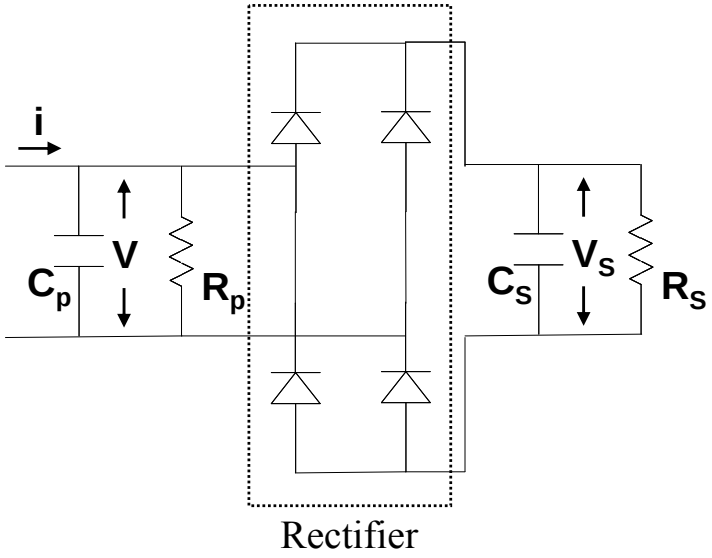


Figure 2.12: Modified electrical part of the lumped modeling.

$$\dot{V} = \frac{dV}{dt} = \frac{\left(i - \frac{V}{R_p}\right) - \left(\frac{V - 2V_D}{R_S}\right)}{C_p + C_S} \tag{2.44a}$$

$$\dot{V}_S = \left|\frac{dV}{dt}\right| \tag{2.44b}$$

where V_D is the voltage drop of the diodes when they are "ON". If the diodes are "OFF:"

$$\dot{V} = \frac{\left(i - \frac{V}{R_p} \right)}{C_p} \tag{2.45a}$$

$$\dot{V}_S = -\frac{V_S}{R_S C_S} \tag{2.45b}$$

All the equations obtained above are used to construct the SIMULINK™ model. The model parameters used in the model are summarized in Table 2.1. It is known that the parasitic leakage resistances of the piezoelectric film and the storage capacitance are on the order of GΩ, thus can be neglected.

The suspended mass-spring-dashpot system is modeled as shown in Figure 2.13. Here, F_p denotes the piezoelectric feedback force. The model is constructed based on (2.3). Basically, displacement is taken the independent variable and the displacement is attained from its second derivative by the integration blocks. The damping factor is represented by b.

The overall block diagram is drawn in Figure 2.14. Notice that piezoelectric force is fed back to the mass-spring-dashpot system. Diode bridge function is created by using (2.44). Here, V_D is taken 0.3V as the threshold voltage of a diode-connected transistor. In order to simulate a more realistic case, an output load resistance, R_L, is connected in parallel to the storage capacitance which replaces R_S in (2.44) and (2.45) since R_L is much lower than R_S.

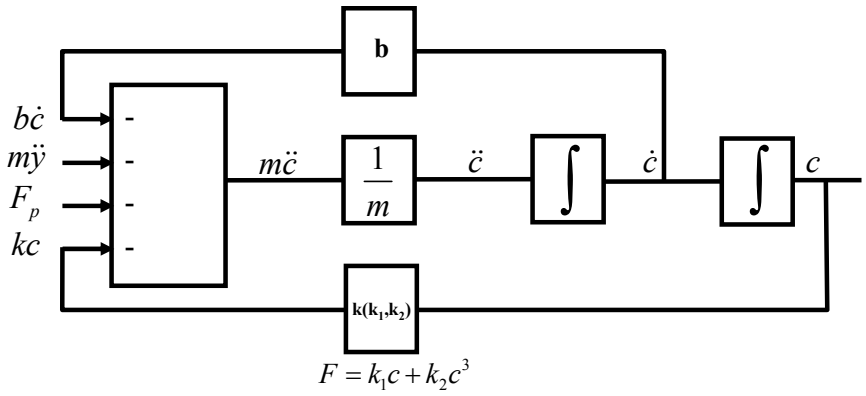


Figure 2.13: The suspended mass-spring-dashpot system model.

Table 2.1: SIMULINK™ model parameters of the "smart sand" system.

Density of the proof-mass (ρ_{pm})	2330 kg/m^3
Width/Length of the proof-mass (L_{pm}, W_{pm})	2.5 mm
Height of the proof mass (H_m)	500 μm
Young's modulus of silicon (E_{Si})	131 GPa
Width of the tether (W)	100 μm
Height of the tether (H)	5 μm
Length of the tether (L)	3.5 mm
Amplitude of the base excitation (Y_0)	60 μm
Frequency of the base excitation (f)	100 Hz
Electrical permittivity of PZT (ε_p)	1700 ε_0
Piezoelectric coefficient (d_{33})	0.18 nm/V
Length of the PZT film (L_p)	2.5 mm
Height of the PZT film (H_p)	2 μm
Width of the PZT film (W_p)	100 μm
Piezoelectric capacitance (C_P)	1 nF
Storage capacitance (C_S)	4 nF
Parasitic leakage resistance of the piezoelectric film (R_P)	7MΩ
Parasitic leakage resistance of the storage capacitance (R_S)	10MΩ

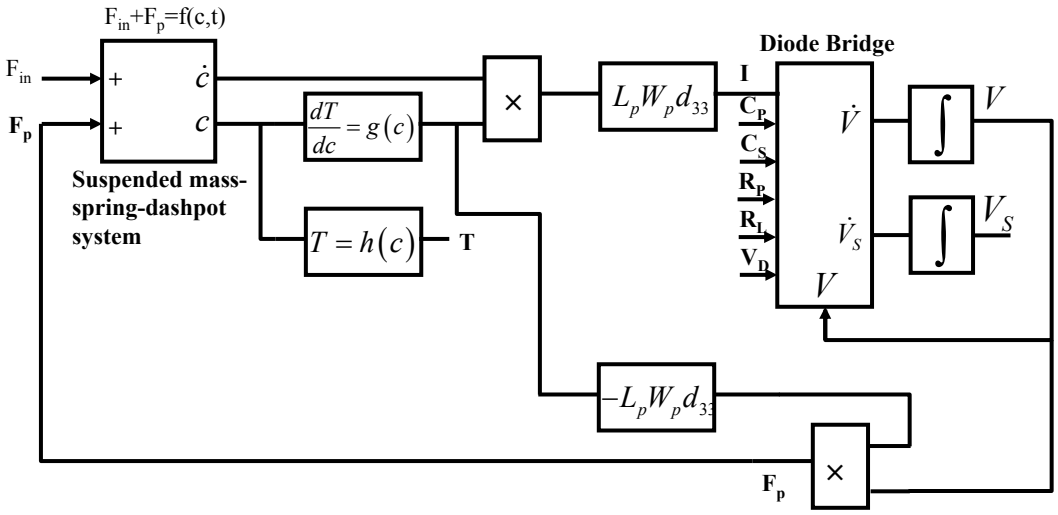


Figure 2.14: The block diagram of the "smart sand".

2.4.1 Simulation Results for Continuous Vibration Inputs

The system is simulated for the continuous vibration amplitudes with a 60µm@100Hz of base excitation. Figure 2.15 shows the displacement of the suspended proof mass.

It can be seen from Figure 2.15 that the displacement is non-linear. The average stress on the tethers is shown in Figure 2.16.

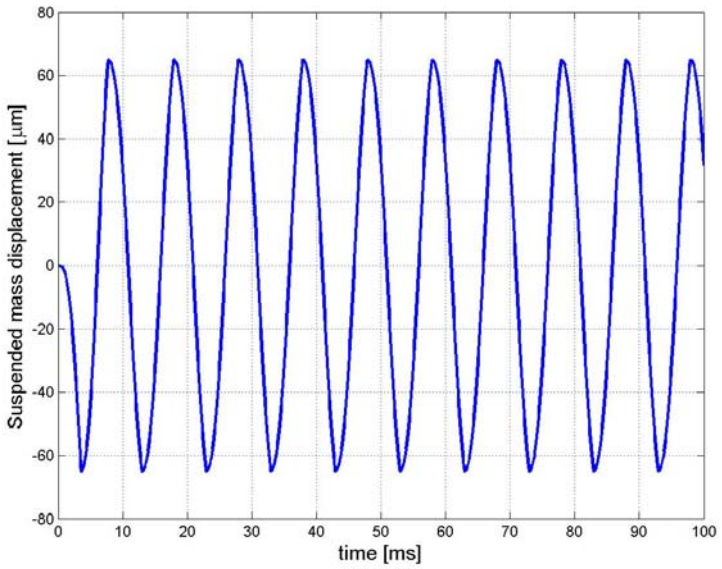


Figure 2.15: The displacement of the suspended proof mass under a 60µm@100Hz of base excitation.

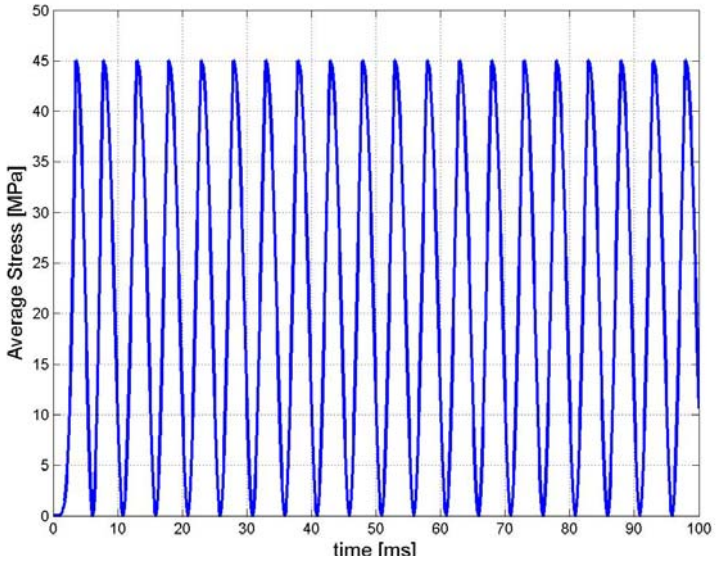


Figure 2.16: The average stress on the tethers.

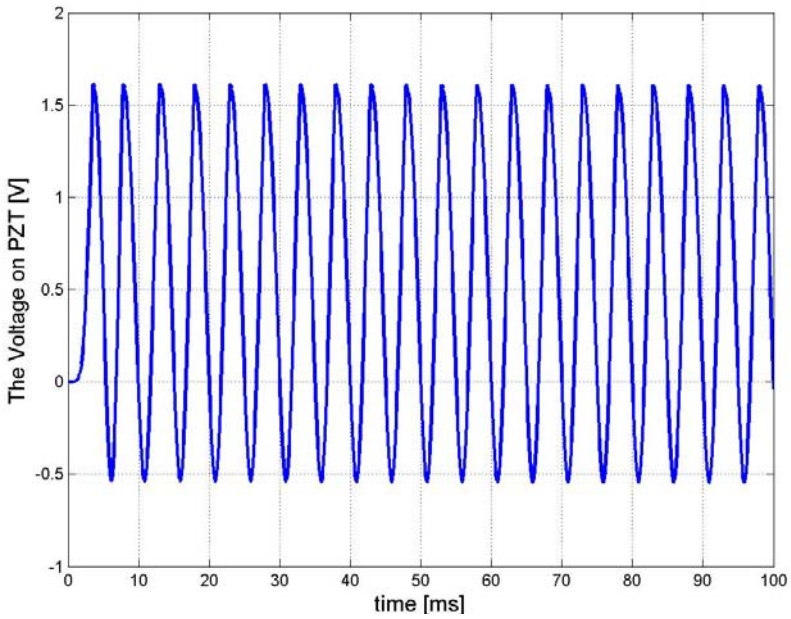


Figure 2.17: The voltage on the PZT layer.

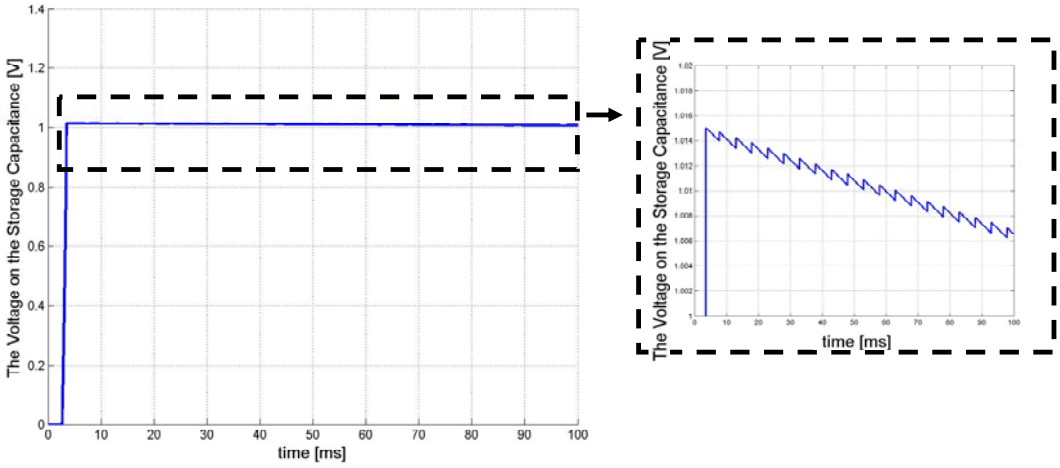


Figure 2.18: The voltage on the storage capacitance.

The voltage generated by the piezoelectric thin film layer is shown in Figure 2.17. Finally, the voltage on the storage capacitance is given in Figure 2.18. Because the output load resistance, there is a decay at the output.

These simulations have been conducted with vibration amplitude that results in tether surface stresses just below the fracture limit of a sol-gel deposited PZT film **(Fett et al., 1999** states that it is about 50 MPa) in the middle section of the tethers. Therefore, these results represent a practical performance maximum for the "smart sand" devices if they are fabricated today using a simple sol-gel fabrication technique.

Notice that, even with the relatively poor mechanical strength of the sol-gel deposited PZT, the devices can produce up to 1V on the storage capacitor (after the diode voltage drops) at a low frequency of 100Hz. Given that it takes about 3.7ms to charge up the 4nF storage capacitor (and much shorter to discharge it through a 100kΩ representative load), the average power generated can be computed through calculating the electrical energy stored on the capacitor, and dividing it with the minimum time necessary between recharges – which yields an average power generation of about 2μW. For the initial prototype device dimensions yielding a volume of about $6mm^3$, the corresponding power density is $0.3\mu W/mm^3$, or $0.3mW/cm^3$.

Operation at higher frequencies results in relatively higher power generation and power density levels, because the current output from the piezoelectric layer is basically proportional to frequency and higher current output means faster charging of the storage capacitor. This observation suggests that performance comparison with other vibration energy harvesters should also be conducted with the numbers normalized for a given frequency. Table 2.2 depicts the comparison of proposed and other vibration based energy harvesters including normalized power density for an input vibration frequency of 200 Hz.

Table 2.2: Performance comparison of various vibration energy harvesters.

Harvesting Method	Power	Power Density	Power Density (including packaging and electronics)	Base Vibration	Normalized Power Density at 100Hz
Proposed System: Piezoelectric vibrations (Kaya and Koser, 2005)	2μW	$300\mu W/cm^3$	$200\mu W/cm^3$	200Hz	$100\mu W/cm^3$
Electrostatic vibrations (Miranda et. al., 2004)	1.3μW	$65\mu W/cm^3$	$50\mu W/cm^3$	2.5kHz	$4\mu W/cm^3$
Piezoelectric vibrations (Sood et.al., 2004)	1μW	$5mW/cm^3$	$0.6mW/cm^3$	13.9kHz	$8.6\mu W/cm^3$
Piezoelectric Vibrations (Jeon et.al., 2005)	1μW	$3mW/cm^3$	$1.5mW/cm^3$	13.9kHz	$10\mu W/cm^3$

Based on the comparison shown in Table 2.2, the nonlinear vibration energy harvester proposed here promises the largest power density at a given operating frequency. Considering that it does not need frequency tuning for different vibration sources and offers a completely integrated system in a millimeter-scale package, the "smart sand" design is very attractive for a wide range of applications.

The power conversion efficiency of the energy scavenger can be calculated with the obtained results. The potential energy of a system is given as;

$$U = \int F dc \tag{2.46}$$

Here, F is the nonlinear force which is determined in (2.22). Considering E is 160GPa, each tether is100μm wide, 5μm thick and 3.5mm long and the deflection amplitude, c, is 60μm, the potential energy is found to be 0.18μJ. On the other hand, it has been calculated that the storage capacitor is charged to 1V in 2.3ms, which yields 47μW of mechanical power. Because the generated power by the smart sand for the same dimensions and conditions is 2μW, the power conversion efficiency is calculated to be 4.3%.

2.4.2 Simulation Results for Shock Inputs

The "smart sand" devices have been tested for continuous vibration sources. However, devices can be experienced shocked inputs. Therefore, different "g-levels" are applied as the base excitation. In this "shock pulse" mode, the device operates as an one dimensional accelerometer. The duration of the shock pulse is assumed to be 10ms which can vary for different environments. The damping ratio is taken to be 0.0015. Figure 2.19 shows the pulse input response of the device. The acceleration here is almost 1*g*.

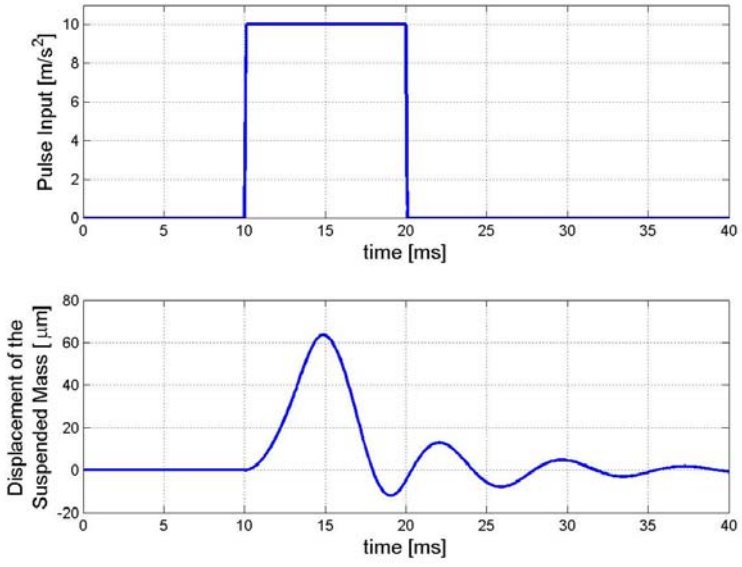


Figure 2.19: The resulting displacement of the proof mass for a ~1*g* pulse input.

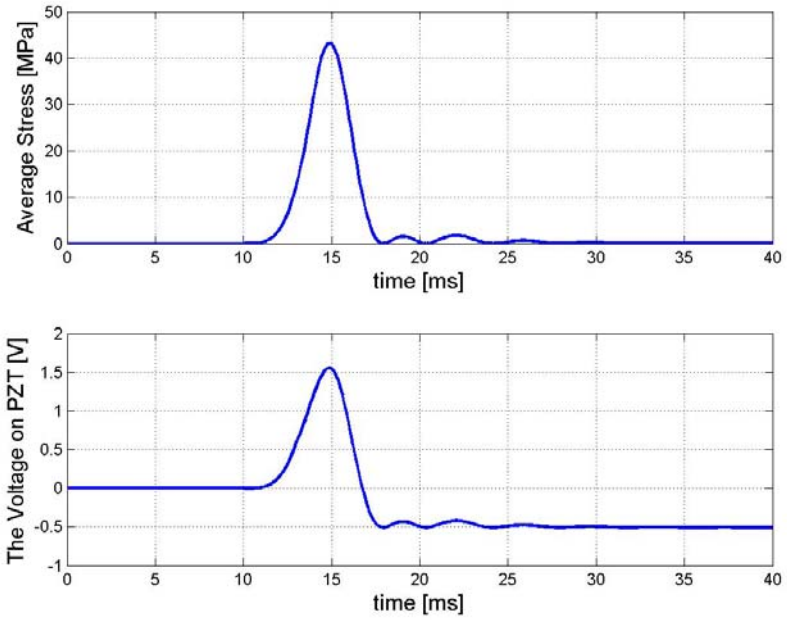


Figure 2.20: The stress on the PZT film and resulting voltage out in response to ~1*g* pulse input.

The stress on the PZT film and resulting voltage out from it is shown in Figure 2.20.

Finally, the voltage on the storage capacitance is plotted in Figure 2.21. It can be seen that the voltage is almost 0.95V.

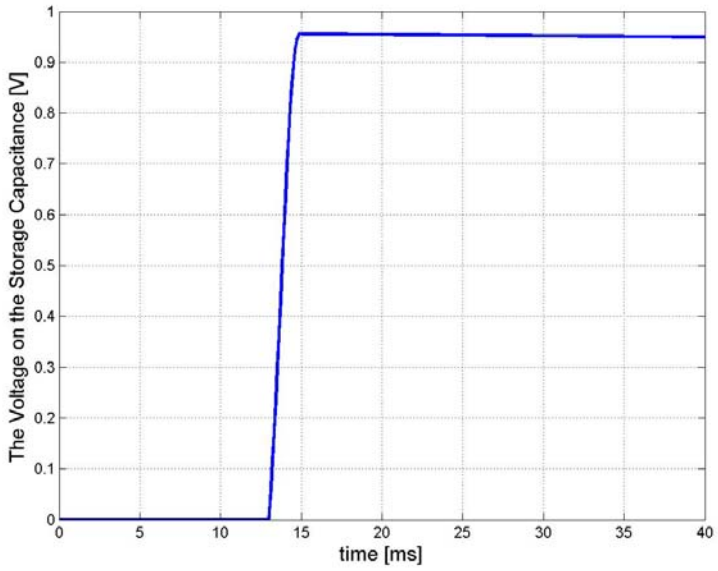


Figure 2.21: The voltage on the storage capacitance in response to ~1*g* pulse input.

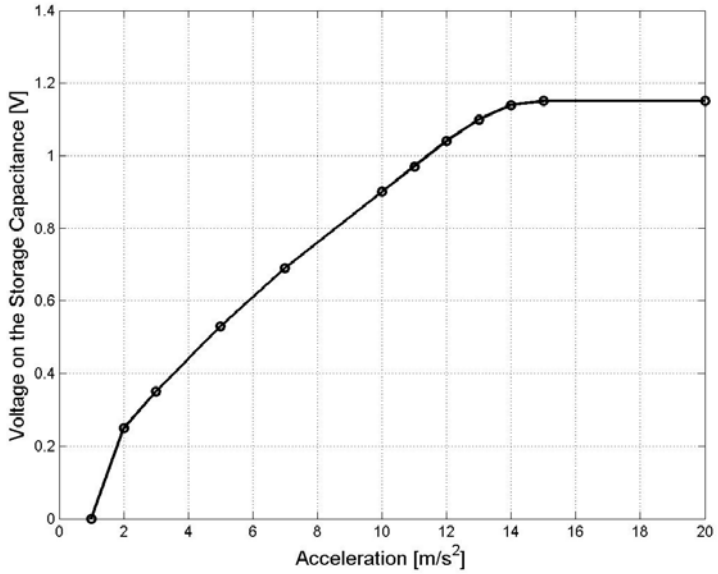


Figure 2.22: The voltage on the storage capacitance with the acceleration amplitudes.

Figure 2.22 shows the voltage change due to the different acceleration amplitudes. If a switch that turns on for a specific voltage level, then this system can be used as an acceleration sensor. If the tethers are made stiffer, higher g-levels can be sensed.

In this thesis, a mechanical switch is proposed to be integrated into the "smart sand" device. Next section will discuss the modeling approach of this mechanical switch.

2.5 Mechanical Switch

As the previous simulations have shown that continuous vibrations or shock impulses result a voltage output around 1V under the assumption that the vibration or impulse amplitudes are large enough, on the order of 50μm or 10m/s^2, respectively. If the base excitation is low, the generated voltage levels will be low, as well. In this case, the sensor circuitry does not operate well, since it is designed for supply voltages of between 0.7V and 1V. Therefore, a switch is used to transfer the generated voltage by the piezoelectric material to the circuitry when a specific threshold voltage is exceeded.

This switch should meet some specifications:

- Its series contact resistance should be low when it is ON, on the order of 10Ω,

- It should be turned on at 1V and off at 0.7V in order to give a range of operation for the circuitry through its hysteresis,
- Its hysteretic behavior should not be affected by the mechanical movements of the smart sand.

This switch can be implemented by mechanical or electronically. Electronic switches consist of hysteretic switches and a power transistor to transfer the generated voltage. However, there is always a voltage drop on the power transistor due to its finite "on" resistance. Therefore, mechanical switch has been chosen for this thesis and its feasibility has been explored in detail.

One possible design of the mechanical switch is sketched in Figure 2.23. The high resistive polysilicon cantilever acts as a mechanical relay or switch. The grounded metal electrode is covered on the cantilever and another metal is put under the cantilever which is floating. When the voltage on the PZT electrode rises, electrostatic force between the PZT electrode and ground electrode causes the cantilever bent and the floating electrode shorts the PZT electrode to the power supply line of the circuitry.

This operation is achieved by the electrostatic pull-in instability. Here, the powered electrode and the ground electrode are called bottom and top plates, respectively. By

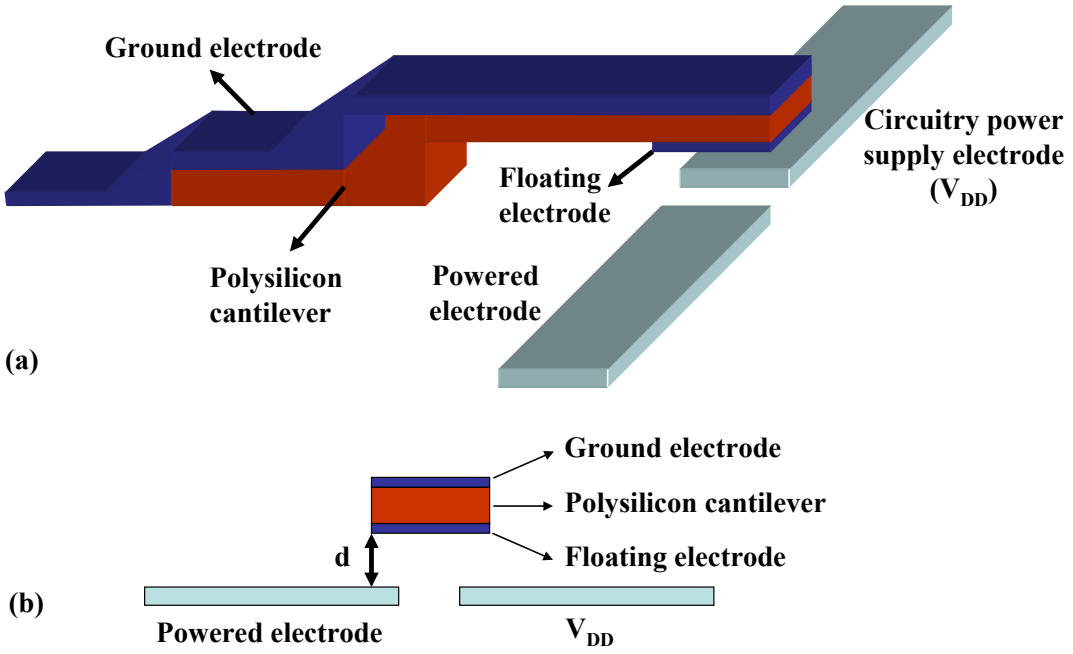


Figure 2.23: One possible design of the mechanical switch; a) 3-d view, b) 2-d front view.

applying a dc voltage V_{dc} across the plates, an electrostatic attractive force F_{el} is induced which leads to a decrease of the gap spacing (d in Figure 2.23), thereby stretching the spring **(Pamidighantam et al., 2002)**. This results in an increase of the spring force F_s which counteracts the electrostatic force. Pull-in instability occurs as a result of the fact that the electrostatic force between the plates increases non-linearly with decreasing gap spacing ($F_{el} \sim d^{-2}$), whereas the spring force is a linear function of the change in the gap spacing ($F_s \sim d$). When a specific voltage level is achieved (referred to as the pull-in voltage), the restoring spring force can no longer balance the attractive electrostatic force **(Pamidighantam et al., 2002)**. Thus, the gap spacing goes to zero, which causes the floating electrode to connect the power and V_{DD} lines.

2.5.1 The Hysteresis Behavior

Determining the pull-in voltage in terms of design parameters has been studied extensively **(Chowdhury et al., 2005, Pamidighantam et al., 2002)**. Under the parallel-plate assumptions, the basic formulation can be derived by balancing the electrostatic and spring forces and minimizing the potential energy which yields a simple equation:

$$V_{PI} = \sqrt{\frac{2\hat{E}H^3d^3}{27\varepsilon_0 L^4}} \qquad \textbf{(2.47)}$$

where d is the initial gap, H and L are the height (or thickness) and length of the cantilever beam, respectively, and ε_0 is the dielectric constant of the air. It can be noticed that width of the cantilever beam does not appear in (2.47), however instead of Young's modulus, E, plates modulus, $\hat{E}$ is used for wide beams because of the anticlastic curvature effect[6]. It should be noted here that (2.47) is valid for only parallel-plate assumptions however it still gives reasonable view of perspective.

It is evident that stiffer beam yields higher pull-in voltages. MEMS relays have practically pull-in voltages on the order of 10V. If 1V is desired for the pull-in

[6] If w>5h, then the plate modulus, $\hat{E}$ is used instead of Young's Modulus; $\hat{E} = E/1-\nu^2$, where ν is the Poisson's ratio.

voltage, it is clear that the cantilever beam should be made soft which dictates thin and long beam dimensions and narrow gap spacing.

It can be shown that the cantilever beam is pulled in where the gap is decreased to 2/3 of the gap spacing under parallel-plate assumptions. After that point, electrostatic force becomes dominant over the mechanical spring force and the beam suddenly approaches to the bottom electrode and pull-in occurs. In order for the beam not to stick to the bottom electrode, an insulating layer is used. The mechanical switch proposed in this thesis does not use such kind of a layer but the polysilicon layer acts as an insulating layer since its resistance is large enough. Increasing the voltage further results a flat contact between the bottom electrode and the beam. When the voltage is decreased, the spring force becomes equal to the electrostatic force at a voltage level which is primarily determined by the insulating layer thickness and the beam spring constant. This voltage is known as pull-out voltage and it is smaller than the pull-in voltage. This behavior introduces the hysteresis which is strongly desired.

Switch hysteresis has been studied by the researchers. **Gilbert et al., (1996)** have discussed the modeling of MEMS hysteresis in devices which exhibit contact between components. The effects of an intermediate dielectric layer on possible configurations of actuator and transitions between them have also been studied **(Gorthi et al., 2006)**.

If parallel-plate assumptions are used, the pull-in voltage can be arranged as follows **(Rocha et al., 2004)**:

$$V_{PI} = \sqrt{\frac{8}{27}} d \sqrt{\frac{k}{C_0}} \tag{2.48}$$

where k is the spring constant and C_0 is the capacitance at the initial position. The pull-out voltage can be calculated as a function of the normalized position of the dielectric stopper, or the insulating layer, y_n **(Rocha et al., 2004)**:

$$V_R = (1 - y_n) \sqrt{2 y_n} d \sqrt{\frac{k}{C_0}} \tag{2.49}$$

Here, y_n is equal to y/d. It can be seen from (2.50) and (2.51) that V_{PI} and V_R are in the same form. The ratio of V_R to V_{PI} gives a figure of merit of the hysteresis interval. Assuming the pull-in voltage is 1V and the desired release voltage is 0.7, V_R/V_{PI} ratio

should be 0.7. In order to find the stopper position, V_R/V_{PI} is plotted with respect to the normalized thickness of the insulating layer as shown in Figure 2.24.

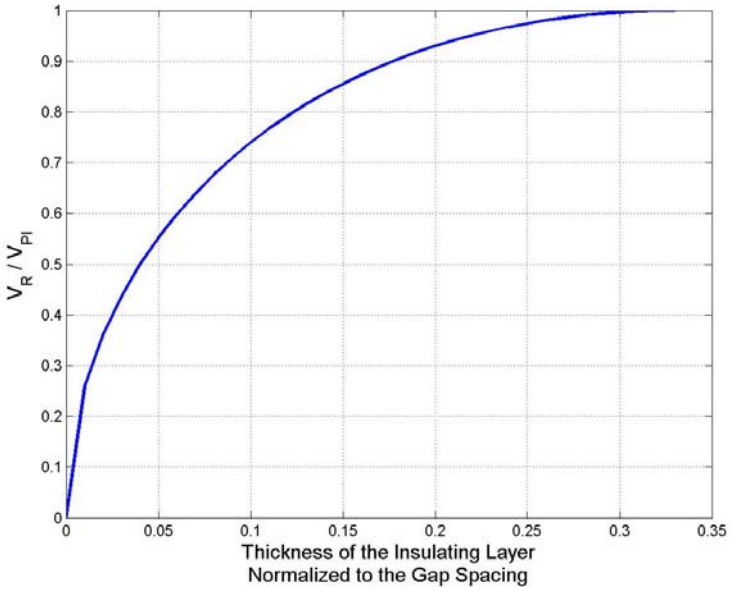


Figure 2.24: V_R/V_{PI} ratio with respect to the normalized thickness of the insulating layer.

It can be seen from Figure 2.24 that, assuming the gap spacing is 0.5µm, 0.05-0.06µm of polysilicon layer is sufficient to create a hysteresis interval of 300mV.

There are more complicated (thus more precise) models that take into account axial stress, non-linear stiffening, charge-redistribution and fringing fields **(Pamidighantam et al., 2002)**. Even though (2.49) gives reasonable results, a modified version of the pull-in voltage model which is more accurate, proposed by **Gupta (1997)** has been used in this thesis:

$$V_{PI} = \sqrt{\frac{4c_1 B}{\varepsilon_0 l^4 c_2^{\,2}\left(1 + c_3 \frac{d}{w}\right)}} \qquad \textbf{(2.50)}$$

The constants c_1, c_2 and c_3 have been determined by COMSOL MULTIPHYSICS™ that are 0.07, 1.00, and 0.42, respectively **(COMSOL, 2005)**. The width of the beam, w, is also included into (2.50). The term B comes from

$$B = \hat{E} h^3 d^3 \qquad \textbf{(2.51)}$$

Further investigations can be found in **Tekin, (2006)** [7].

The pull-in voltage is then plotted according to (2.46) with respected to the length of the beam and various beam thicknesses, as shown in Figure 2.25. Focusing on the beam thickness of 60nm, 20μm long cantilever beam has the pull-in voltage of 1V. Here, $\hat{E}$ is taken 155GPa where the Poisson's ratio is 0.17. Width of the beam is taken 50μm.

2.5.2 The Frequency Response

After determining the dimensions of the cantilever beam, it is important to analyze the structure in the frequency domain. When the "smart sand" device is vibrated, the mechanical switch will also vibrate. If the cantilever is displaced around 1μm before exceeding the pull-in voltage, the switch goes on and undesired voltage levels may be applied to the circuitry. Therefore, the eigenfrequencies should be determined first. The first eigenfrequency of the cantilever beam should be far enough from the excitation frequency. The first eigenfrequency of the beam is calculated as follows **(Tekin, 2006)**:

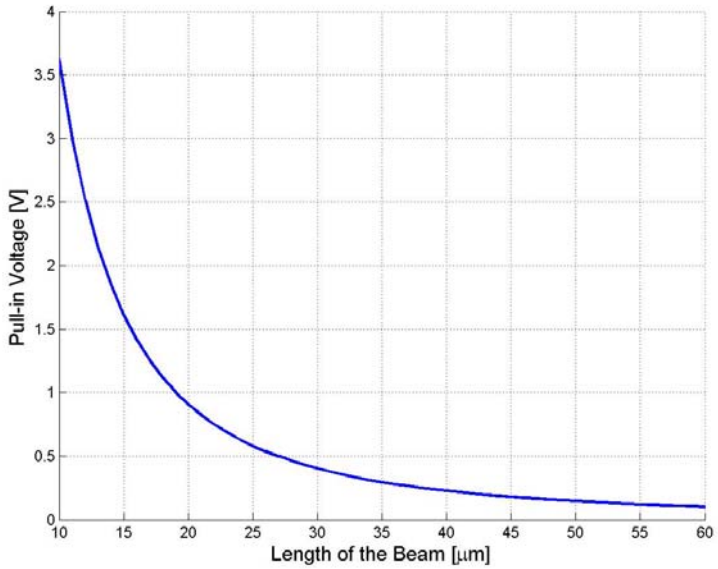


Figure 2.25: Pull-in voltage variation with respect to the beam length for various beam thicknesses.

[7] The mechanical switch is designed by Halil Tekin, an M.S..student supervised by Tolga Kaya.

$$f_1 = \frac{1}{2\pi}\left[\frac{3.5156}{l^2}\right]\sqrt{\frac{\hat{E}I}{\rho}} \tag{2.52}$$

where I is the moment of inertia which is equal to $wh^3/12$ and ρ is the mass per length. Considering w, h and l are 50μm, 60nm and 20μm, respectively, the first eigenfrequency, f_1, is found to be 100kHz which is far away from the excitation frequency that are around 200Hz.

The displacement of the tip of the cantilever beam can also be attained by applying a continuous vibration signal. Assuming the cross sectional area of the beam is A, the dynamic behavior of a cantilever beam can be described as **(Chen et al., 2006)**:

$$\rho A\frac{\partial^2 V(x,t)}{\partial t^2} + \alpha\frac{\partial V(x,t)}{\partial t} + \beta I\frac{\partial^5 V(x,t)}{\partial x^4 \partial t} + EI\frac{\partial^4 V(x,t)}{\partial x^4} = 0 \tag{2.53}$$

where ρA is the mass density of the beam, α is the mass damping coefficient and β is the stiffness damping coefficient. The homogenous solution of (2.53) can be obtained by the separation of the variables. The deflection of the tip of the beam can be expressed as **(Chen et al., 2006)**:

$$V(L) = A_0\frac{\cos kL + \cosh kL}{\cos kL\cosh kL + 1} \tag{2.54}$$

where

$$k^4 = \frac{\omega^2\rho A - j\omega\alpha}{\beta I j\omega + EI} \tag{2.55}$$

It is well known that the vibration amplitude decreases with f^2. The input deflection amplitude of the beam, thus, is calculated as a function of the frequency. It is assumed that the vibration amplitude reaches 50μm at 200Hz of base excitation which is considered the worst case. Figure 2.26 demonstrates the tip displacement with respect to the frequency. Even though the vibration amplitude decreases after 200Hz, the tip displacement exhibits some peaks which are at the resonance frequencies of the cantilever beam. It can be seen that the tip displacement is on the order of nanometers which can be neglected.

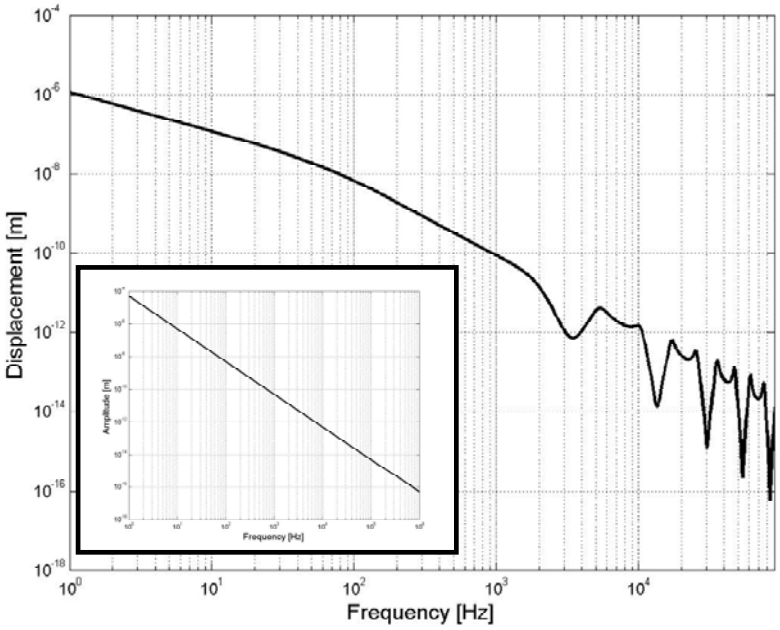


Figure 2.26: The frequency response of the cantilever beam. The base excitation at 200Hz is 50μm.

3. FABRICATION

The processes for microelectronic fabrication has been developed incredibly fast since the first transistor has been realized at Bell Laboratories in 1947. MEMS process engineers have first inspired from these well-known microelectronic process methods but not contented with them and started developing their specific fabrication methods including bulk and surface micromachining processes.

Although the cantilever based structures have been fabricated with recently developed MEMS processes, fabrication of the novel mechanical structures always introduce new challenges. In this thesis, a novel piezoelectric based mechanical structure has been proposed. Therefore, its process steps have some challenges.

This chapter is focused on the fabrication of the "smart sand" including the issues that have been faced and solutions that are come up. Because the overall device will contain the circuitry, mechanical system (including the MEMS switch), piezoelectric material, and package, a fabrication flow is proposed at first. Then, the fabrication of the mechanical system will be explained in detail. PZT (Lead Zirconate Titanate) thin film deposition will be discussed and its fabrication results will be given. For preliminary prototyping, a novel packaging approach will be proposed. Following the primary testing results, ongoing fabrication and testing progress will be reported.

3.1 Fabrication Flow

The fabrication flow has been created after several optimization steps. Different process methods have been considered and tested. Each step has process limitations such as temperature and sensitivity to the method. For example, high temperature is needed for the deposition of PZT layer which harms the CMOS circuitry. Therefore, the sequence of the process steps should be determined carefully.

The bulk material for the fabrication is chosen to be Silicon-on-Insulator (SOI) wafer as shown in Figure 3.1a. Here, the 300μm thick silicon is called handle wafer and thinner one (3 to 10μm) is the device wafer. The insulator layer is 1-2μm of silicon dioxide (SiO_2) called buried oxide layer. These wafers are commercially available.

The buried oxide layer acts as an etch stop layer for bulk micromachining. Because the CMOS fabrication is highly sensitive to preceding processes, first step of the fabrication is anticipated to be the CMOS realization.

The next step is to deposit the PZT layer on tethers. This step also determines where the tethers will take (Figure 3.1b). During PZT deposition, CMOS part should be protected and PZT process should be carried out carefully in order not to harm the circuitry. The top view is given in Figure 3.1c. Then, bulk micromachining is performed and the proof mass is shaped. The front side of the wafer is protected at this step in order to prevent etching or damaging from the top of the wafer. The bulk micromachined silicon wafer is placed onto the PDMS (poly dimethyl siloxane) patterned glass slide which serves as a carrier, as shown in Figure 3.1d. The metals for CMOS are patterned at this step together with the electrodes of the PZT layer and top side of the wafer is etched which causes the structure to be released, as illustrated in Figure 3.1e. Finally, as shown in Figure 3.1f, another PDMS patterned glass slide is attached on top of the device which completes the packaging. This packaging also puts limits for the proof mass that should not be displaced more than the fracture limits of the PZT layer.

3.2 MEMS Back-Side Fabrication

One of the main fabrication steps is the formation of the proof mass. Because the proof mass is realized from the bulk silicon of the handle wafer, the 300μm thick handle wafer is etched and patterned. For this purpose, bulk etch methods will be briefly discussed in the following section.

3.2.1 Bulk Etchant Alternatives

There are several Silicon bulk etchants available in the literature. A comprehensive discussion has been carried out by **Kovacs et al., (1998)**. Here, two methods that are widely used will be compared; alkali-OH solutions and deep reactive ion etching (DRIE). Other etchants are listed and their properties are compared in Appendix A.

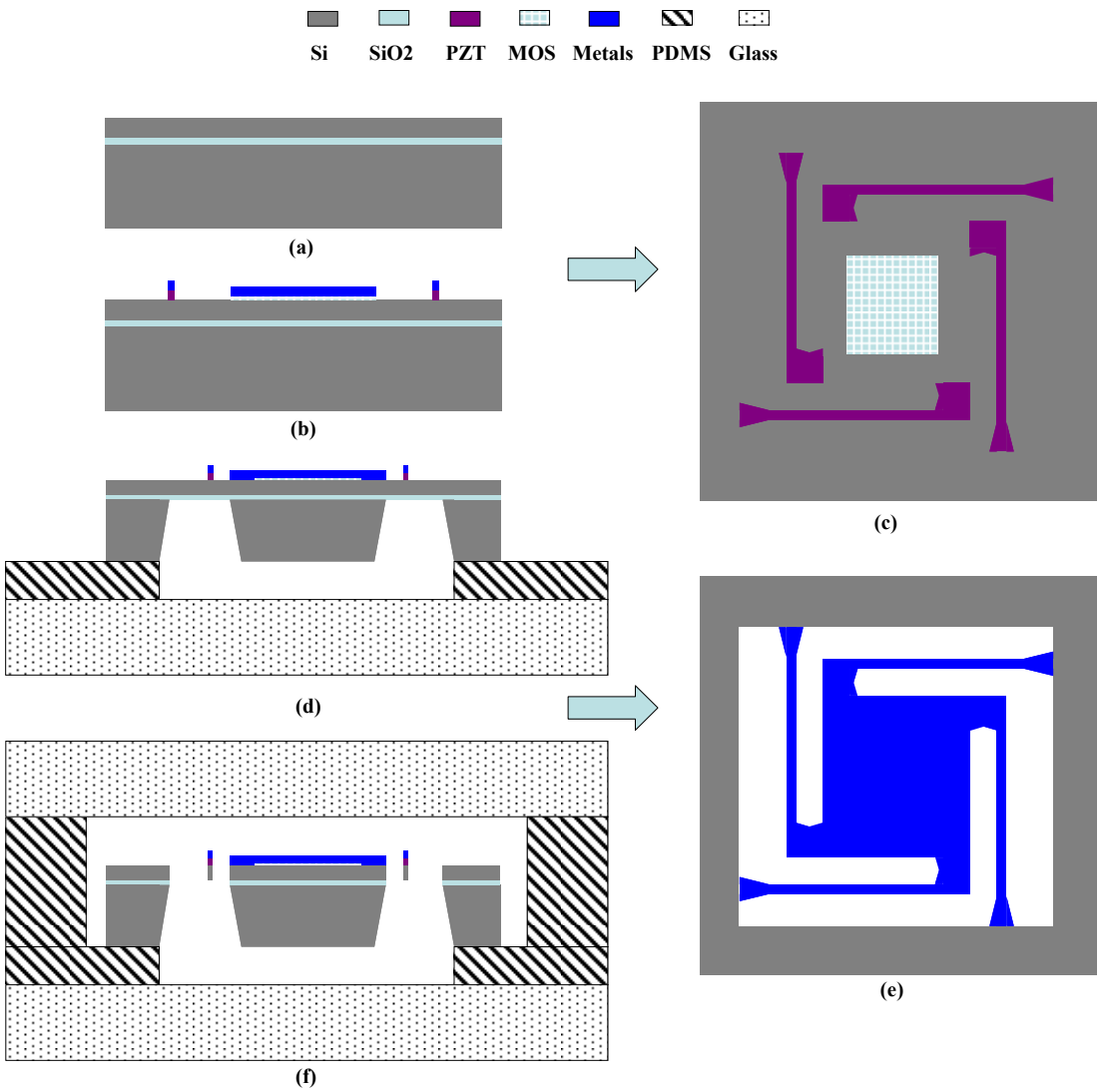


Figure 3.1: Fabrication flow for the "smart sand" devices.

The main difference between alkali hydroxide etchants and DRIE is the etching type. DRIE is basically known as dry etching, since gases are used as etchants. Silicon etch rate is more than 1μm/min which is pretty fast. Because DRIE cannot etch oxide, buried oxide layer can serve as a good etch stop. Another important property is its CMOS compatibility.

On the other hand, alkali-OH solutions are wet etchants. Sample is placed into the solution and etching starts. Silicon etch rate is 1-2μm/min. Although the oxide etch rate is not very low, it is still selective to oxide in the ratio of around 1:200. The main disadvantage is that it is not compatible with CMOS processing since alkali metals are heavy metals that contaminate the gate oxide during processing. But, if the etching process is introduced after the gate oxide is formed and diffusions are created, contamination does not affect the process that much.

It seems that the DRIE process is better than alkali-OH etchants. However, one and unique issue is the cost. The cost for a wet etch setup including the solution is around $100. DRIE equipments are sophisticated machines that control the gas flow rates and should ensure there is no gas leak. Therefore, a DRIE machine can cost up to $500K.

Considering all these issues, wet etch was chosen for bulk micromachining. The most common alkali metal used in the wet etch processes is Potassium. Therefore, KOH solution will be explored in the following section.

3.2.2 KOH Etch Overview

KOH is an anisotropic wet etchant that is primarily used for silicon substrates. It is also known as orientation dependent etchant where etching happens faster in one direction than in another. If the <100> crystal orientation is chosen, <111> plane is etched slower and uni-directional etching can be achieved. Figure 3.2 illustrates the anisotropic silicon etching schemes. It is well known that the angle of sidewalls is 54.74º **(Seidel et al., 1990)**. In practice, silicon is masked with an insulating layer such as nitride or oxide where KOH can hardly etch and windows are opened where KOH is desired to etch. When the substrate is immersed into the KOH solution, etching starts. Depending on the size of the opening, inclined wells or V-groove shapes can be attained.

Sample scanning electron microscope (SEM) photographs are shown in Figure 3.3 that demonstrates the inclined wells and small V-groove shapes.

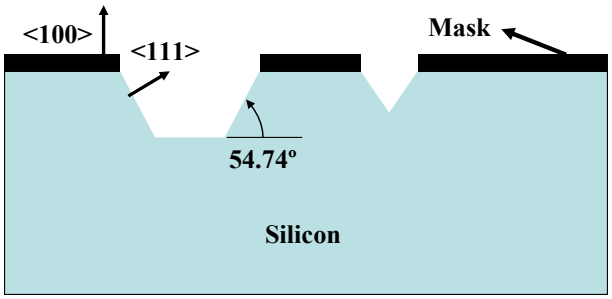
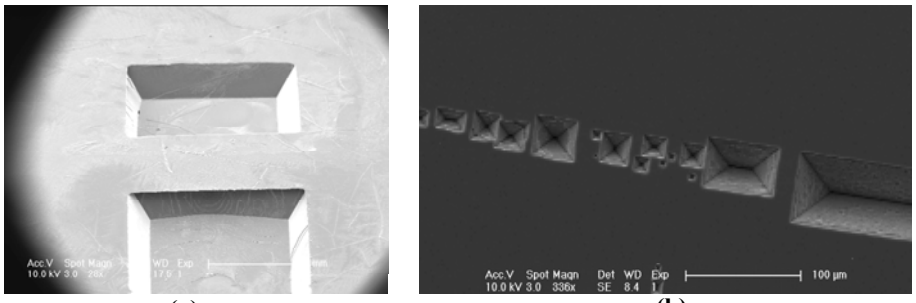


Figure 3.2: Anisotropic etching of silicon creating V-grooves and inclined wells.



(a) (b)

Figure 3.3: SEM observation of KOH etched shapes; a) inclined wells, b) V-groove shapes.

The basic chemistry behind the etching mechanism is as follows: Silicon atoms at the surface react with hydroxyl ions in the solution. Silicon is oxidized and injected electrons from silicon atoms into the conduction band react with the water leading to the evolution of hydrogen. The overall reaction is given as **(Kovacs et al., 1998)**:

$$Si + 2OH^- + 2H_2O \rightarrow Si(OH)_2^{2+} + 2H_2 \quad \textbf{(3.1)}$$

The weight percentage of KOH (wt %) in the solution and temperature directly affect the etch rate. Increasing temperature and decreasing KOH percentage in the solution increase the etch rate. However, concentrations below 20% are not preferred, as increasing etch rates result in higher surface roughness. Therefore, solutions in the range of 20-30% are generally used. The temperature of the solution is usually kept around 70-90ºC. Depending on the solution dilution and temperature, etch rates vary between 0.1-3µm/min **(Seidel et al., 1990)**.

3.2.3 Back Side Etch Procedure

The fabrication is carried out with <100> oriented p type SOI wafer pieces. Even though the fabrication flow depicts that PZT and CMOS processes are done first, in order to overcome the specific issues for each process step, plain wafers without the front side pattern were used. Pieces are first cleaned with the industry standard RCA wafer clean procedure (explained in detail in Appendix B) in order to clean the wafer surface from the dust and dirt. It also removes the native oxide on the wafer. Then back and front sides of the wafer are coated with oxide and nitride with PECVD (Plasma enhanced Chemical Vapor Deposition). Before KOH etch, back side of the wafer is patterned. For this purpose, wafer back side is coated with photoresist and this resist is patterned using a mask. Oxide/nitride layer that is not protected by

photoresist is etched with BOE[8] (Buffered Oxide Etch). In order to protect the front side of the wafer, this side is also covered with the photoresist before BOE etch. Each process recipe is given in detail in Appendix B.

A 25% KOH solution is prepared and 90°C bath is used. The bath is put onto a temperature controlled hot plate. A temperature probe is inserted into the solution and its temperature is set to the desired value. Here, it is important to note that precautions should be taken against the evaporation of the solution. Since the temperature is near the evaporation temperature of water, solution dilution changes with decreasing water proportion of the solution. Therefore, a simple condensation chamber is used which condenses the water vapor and feeds it back to the solution. The etch rate is around 80μm/hour so 300μm silicon handle wafer is etched in under 4 hours. Buried oxide layer serves as an etch stop layer for KOH. Because proof-mass is suspended by 5μm thick membrane layer, wafer should be handled very carefully.

After KOH etch, wafers should be cleaned and hard masks should be removed. BOE is again used for this purpose. BOE does not only clean the KOH residue but also removes the hard masks and buried oxide layer in 30minutes.

The mask design issues including convex corner optimization procedure will be explained in the following section.

3.2.4 Design of the Back Side Mask

In order to attain the proof mass geometry depicted in Figure 3.1d, a mask for the back side is initially designed which is shown in Figure 3.4. Here, it should be noted that the mask dimensions are modified taking into account the sidewalls. As previously mentioned, the sidewalls make an angle of 54.74º with the horizontal plane, thus in order to achieve the proof mass dimensions which are 2.5mm by 2.5mm and considering the handle wafer is 300μm thick, the square in the mask should be

$$2.5\text{mm} - 2\frac{300\mu\text{m}}{\tan 54.74^{o}} \cong 2.1\text{mm} \qquad \textbf{(3.2)}$$

[8] Buffered oxide etch is a mixture of NH_4F and HF used to isotropically etch SiO_2 in microfabrication.

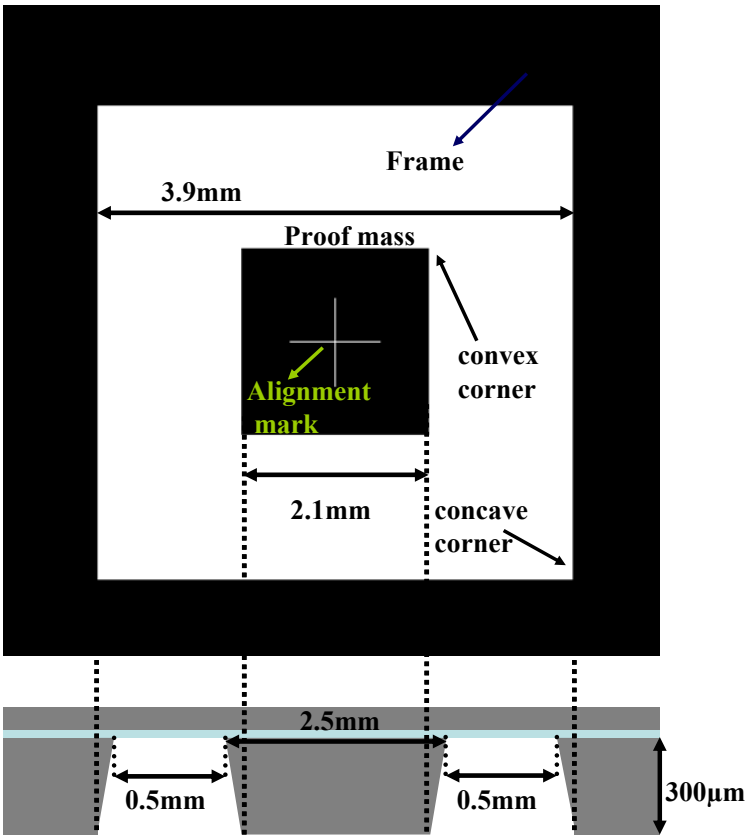


Figure 3.4: Back side mask for KOH etch.

The opening in the frame is also modified. The spacing between proof mass and the frame is designed to be 500µm allowing enough space for tethers. Therefore, the frame window is enlarged to 3.9mm instead of 3.5mm.

However, it is known that etching at concave corners on <100> silicon stops at <111> intersections, while convex corners are undercut **(Kovacs et al., 1998)**. In order to show this phenomenon, the initial mask in Figure 3.4 is used and resulting shape is given in Figure 3.5. It can be seen that square proof mass area has changed completely into a octagon.

The undercutting of convex corners is due to the fact that <411> planes are etched faster than <100> planes, almost twice as fast **(Enoksson, 1997)**. Therefore, corner compensation methods are used to alleviate this problem. The idea is to enlarge the convex corners to some extend so that KOH can etch this corner to the limit of a square.

Different corner compensation schemes have been tried. These are illustrated in Figure 3.6.

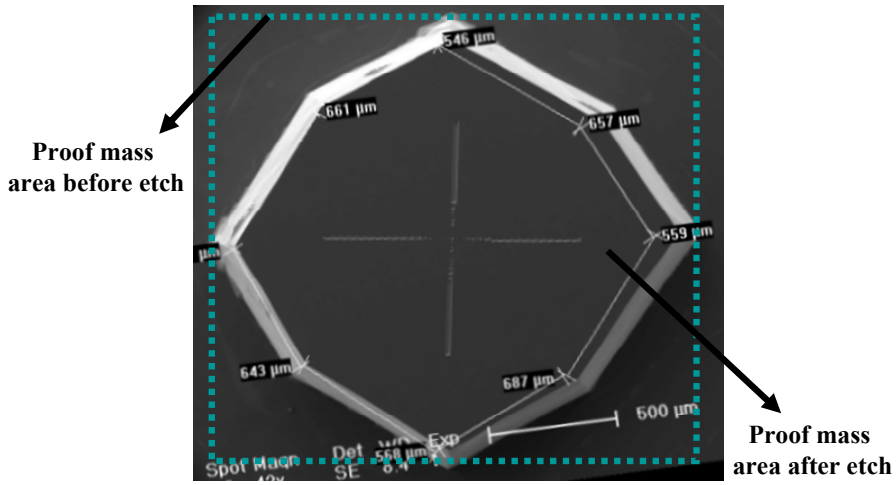


Figure 3.5: The undercutting phenomena of the convex corners.

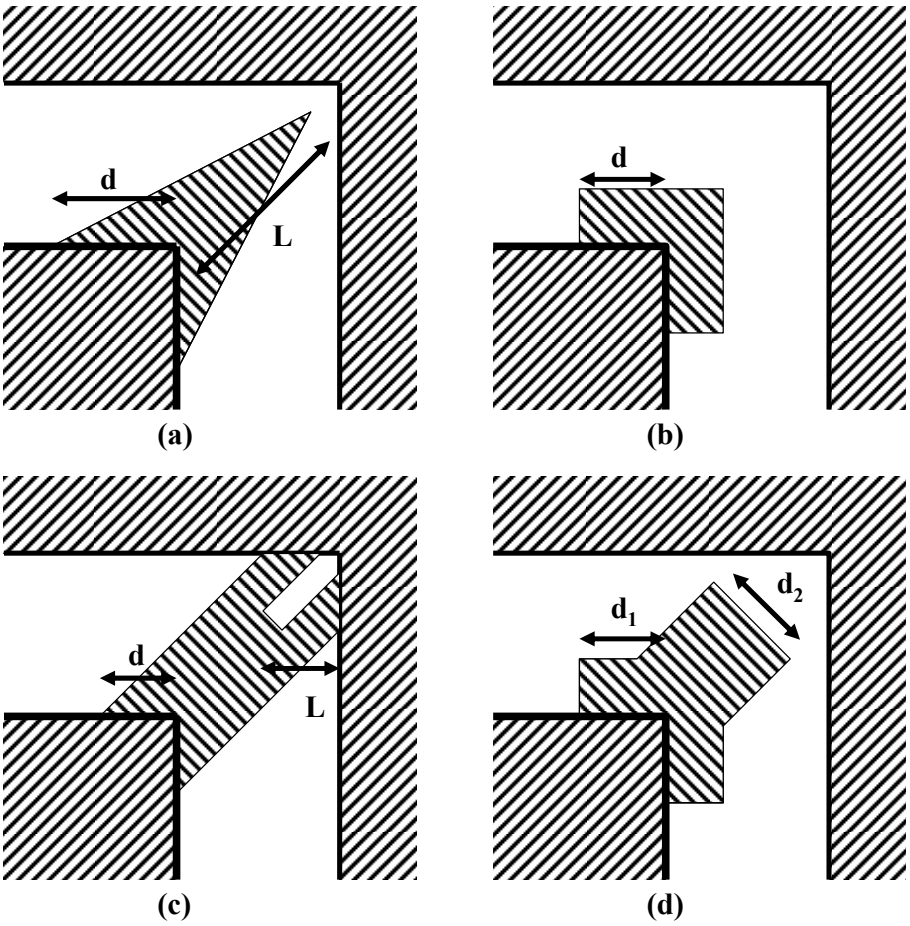


Figure 3.6: Corner compensation schemes; a) Triangular **(Long et al., 1999)**, b) Square **(Puers and Sansen, 1990)**, c) Strip with slit **(Enoksson, 1997)**, d) Square strip **(Puers and Sansen, 1990)**.

The dimensions of each corner compensation scheme illustrated in Figure 3.6 can be determined by the calculations provided by the authors, in terms of the wafer thickness. However, these schemes have been designed considering the convex

corner is near to the concave corner. Because the distance between the proof mass and the frame is relatively large, the proposed structures in the literature as shown in Figure 3.6 are modified by changing their *d* and *L* parameters. These parameters are summarized in Table 3.1.

Figure 3.7 shows the results of each scheme. Here, selected design geometries are the best cases for each corner compensation. It can be seen that Figure 3.7a is slightly over-etched while others are under-etched and need more etching.

Therefore, the triangular corner compensation method would the best choice. The overall mask is shown in Figure 3.8. Here, *d* is 950μm and *L* is 1.8mm.

In order to align the back side wafer to the top side during front side etching, an alignment mark with a plus sign is used. However, intersection of the lines of the plus sign also forms convex corners. Therefore, the plus sign is modified; a discontinuity is created at the center.

Table 3.1: Various design parameters for corner compensation schemes.

Corner compensation schemes	d	L
Triangular	950μm	1mm
	950μm	1.8mm
	500μm	1mm
	500μm	1.8mm
Square	500μm	-
	750μm	-
	1mm	-
	1.5mm	-
Strip with slit	450μm	550μm
	450μm	550μm
	750μm	750μm
	750μm	750μm
Square strip	d_1	d_2
	250μm	450μm
	250μm	450μm
	500μm	750μm
	500μm	750μm

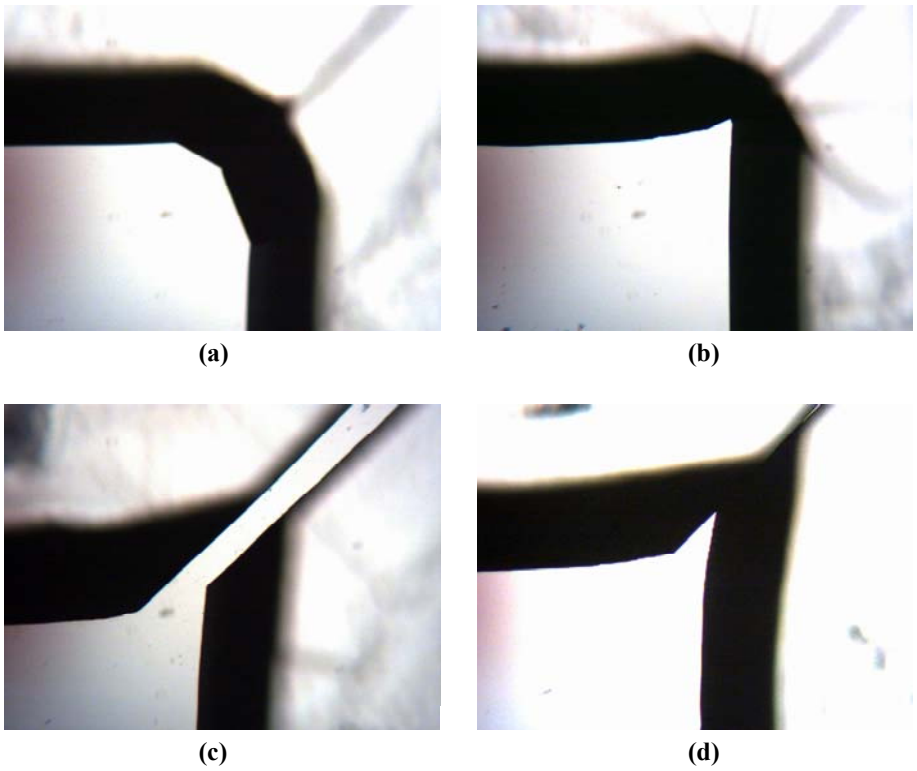


Figure 3.7: Photographs of the KOH etched samples with different corner compensation schemes; a) Triangular (d=950µm, L=1.8mm), b) Square (d=750µm), c) Strip with slit (d=450µm, L=850µm), d) Square strip (d_1=500µm, d_2=750µm).

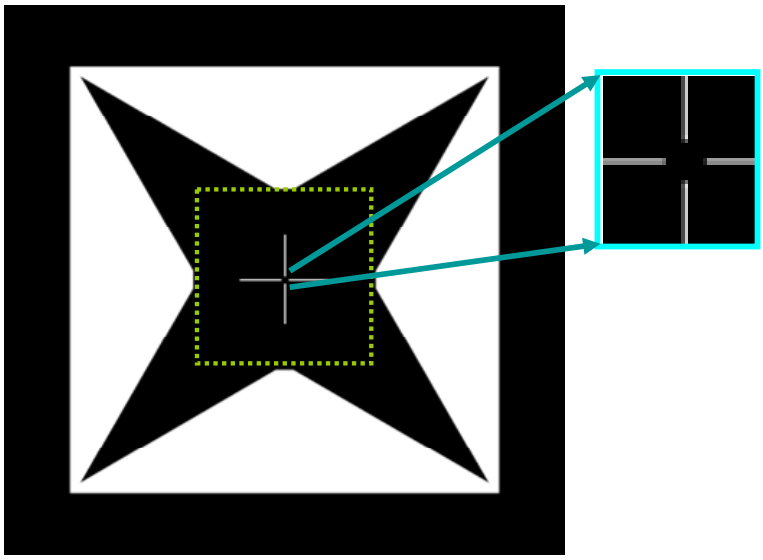
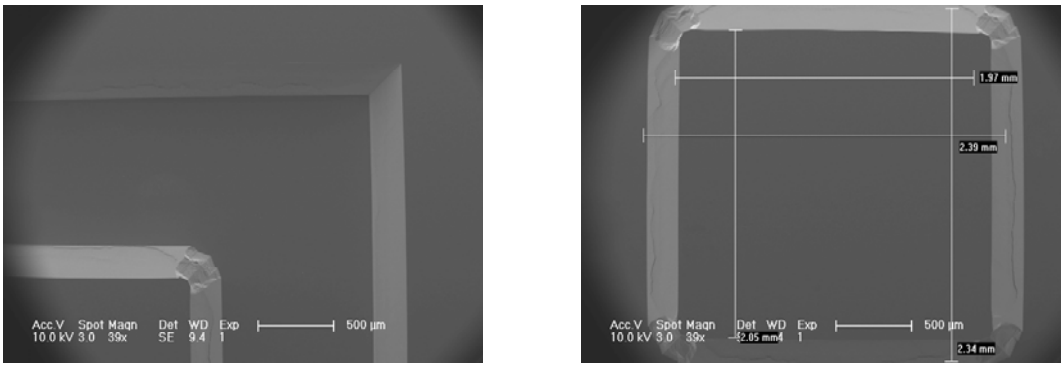


Figure 3.8: The mask for the KOH etch with the triangular corner compensation.

The SEM photograph of the successfully etched silicon piece is shown in Figure 3.9. Even though the corners of the proof mass are still not sharp, this result is satisfactory.



(a) **(b)**

Figure 3.9: The SEM photographs of the proof mass after successful corner compensation; a) Zoomed to the edges of the proof mass and frame, b) The whole proof mass.

3.2.5 Front Side Protection

While the back side is being etched with KOH, it is crucial to protect the front side from etching. During the optimization, the front-side of the plain SOI wafer was coated with oxide and nitride as done for back side but no windows were opened. By doing this, front side has been protected successfully. However, as the fabrication flow depicts, back side etching is performed after CMOS and PZT are processes. Therefore a protective coating method should be developed.

The protective coating layer should meet some specifications. It is very important that it does not harm the front side patterns during depositing and stripping. Moreover, it should be able to cover the patterns which are assumed to be 5µm high. Oxide and/or nitride, therefore, are not suitable. It is hard to deposit 5µm of insulating layer.

In the past, some fabricators have chosen to use available materials such as BCB (Benzo Cyclo Butene), waxes, and thick photoresist to protect the front side of the substrate **(Ruben et al., 2004)**. There are problems associated with the use of any one of these materials. BCB is very difficult to remove after the process. Waxes are relatively inexpensive to purchase but are messy and difficult to remove. In addition, the wax can sometimes contaminate future processing steps. Lastly, photoresists are sometimes soluble in the etchants and do not offer acceptable protection.

Spin applied polymeric coatings have been designed recently to give maximum protection against harsh etchants during the long etch processes, and are easy to

remove. Brewer Science, Inc. has developed a polymer coating which is called Protek™ **(Ruben et al., 2004)**. Protek can be coated over more than 6μm thick and can be easily removed by N-Methyl Pyrrolidone (NMP) or simply acetone. The process starts with the spin coating of Protek Prime which serves as an adhesive layer for Protek Base. After pre-bake of the primer, base material (Protek B1-25) is spun and several post-bake steps are performed. Detail process recipe is given in Appendix B.

Some difficulties have been encountered during Protek process. As long as there is no pattern on the front side of the wafer, Protek works perfectly. However, if the front side is patterned, then, Protek may peel off from the substrate during etching. On the other hand, Protek does not work very well if non-circle shaped wafer pieces are used. As soon as whole round wafers are used, this problem is not seen. The peel-off problem has been solved by bonding another plain wafer piece onto the front side of the wafer to be protected. After coating the base material, a dummy wafer piece bigger than the device wafer is attached on the device wafer and baking process is carried out with this "sandwich" structure.

Another way to protect the wafer from etching during KOH is to use a mechanical structure. The wafer to be etched is placed into a small teflon casing with an o-ring which prevents fluid going underneath the wafer. By this method, there is no need to coat the front side of the wafer.

3.3 MEMS Front Side Fabrication

Following the back side etching, front side of the wafer is etched in order to release the suspended beam structure. In this step, front side of the wafer needs to be aligned to the back side, since the tethers should start right above the edges of the proof mass. The alignment marks that exist in both the front side and the back side masks are used for this purpose.

Once the front side is etched, the device is suddenly released and suspended structure is free to move. Therefore, in order to handle the devices, support structures are needed. Initially, photoresist coated dummy wafers had been considered but two problems had been realized. First of all, in order to align the front side to the back

side, both sides of the wafer should be visible. Moreover, it would be hard to detach the dummy wafer from the mechanical structure.

Then, considering the packaging issues, glass slides have been found to be feasible. In order to attach the devices onto the glass slides, a silicon elastomer which is called PDMS is used. PDMS is the most widely used silicon-based organic polymer. It is optically clear, and is generally considered to be inert, non-toxic and non-flammable. Its commercial name is Sylgard **(Dow Corning, 2002)**.

3.3.1 PDMS Patterning

PDMS is used mostly in microfluidic applications with its superior capability of filling the micron sized channels or wells. However, in the context of this thesis, it is used as a support layer. Therefore, it is spun onto the glass slides. The spin recipe is given in Appendix B. Successive spins give thicker PDMS films, as shown in Figure 3.10.

PDMS can be detached from the glass slides if the glass slides are silanized[9]. Therefore, hard-baked PDMS thick film (200-500μm) is basically cut with a razor to open a window. After PDMS has been patterned on the glass slide, wafer and PDMS coated glass slide are put into a plasma system in order to make their surface hydrophilic[10] so that they will be able to attach to each other. Pressure of 300mTorr

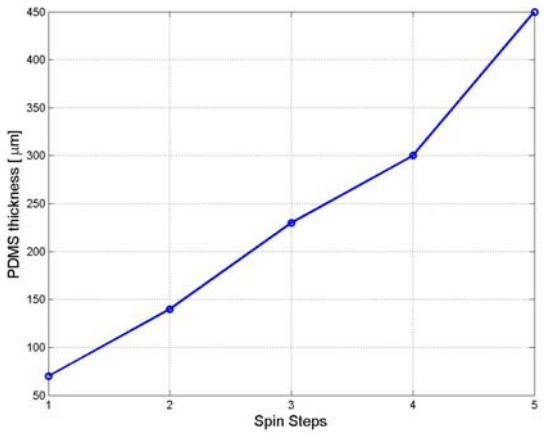


Figure 3.10: PDMS film thickness with the successive spins.

[9] Silanisation is a treatment of a surface by adding tri-methyl-chloro-silane (TMCS), which makes sure that PDMS can be detached from the surface afterwards.

[10] A hydrophilic molecule or portion of a molecule is one that is typically charge-polarized and capable of hydrogen bonding, enabling two hydrophilic surfaces to be bonded.

and the power levels of 30W are already enough to create a plasma. The device and the carrier are attached to each other gently after one minute of plasma treating. This bond is pretty strong and almost irreversible.

3.3.2 Reactive Ion Etching

Following the attachment of the device onto the PDMS coated glass slide, front side etching is performed with reactive ion etching (RIE). Photoresist is coated and exposed by using EVG 620 Mask Aligner. EVG has the capability of alignment from the back side of a substrate to the top side with the aid of its top and bottom side microscopes. The front side mask is inserted on top of the substrate, and alignment mark on the back side of the already formed proof mass is aligned to the front side mask pattern. Front side mask is shown in Figure 3.11. Here, tethers are 200μm thick and 3.5mm long.

Following the photoresist pattern, Nextral parallel plate plasma reactor with an RF of 13.56MHz RIE equipment is used to etch the 5μm thick device wafer and release the beam structure. For silicon etching, SF_6 is used. The gas flow rate is 25 sccm (cubic centimeters per minute). The plasma is generated under a 200W of RF power with a 200mTorr pressure. Photoresist is then stripped using RIE again with a different recipe (10 sccm O_2, 100W, 100mTorr). Figure 3.12 shows the SEM photograph of the successfully released beam structure.

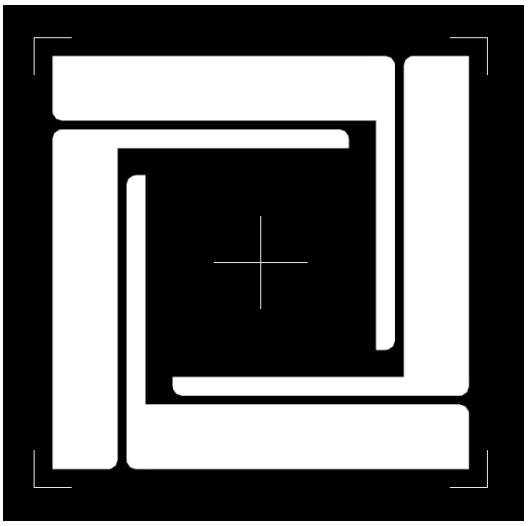


Figure 3.11: Front side mask of the smart sand.

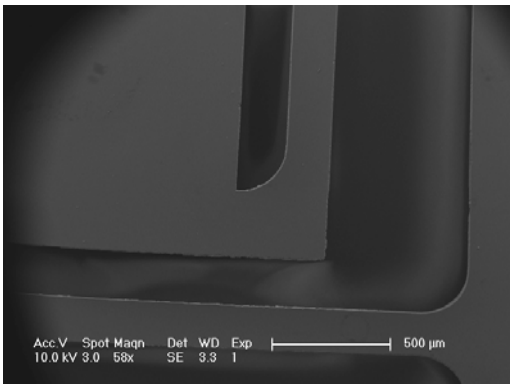


Figure 3.12: SEM photograph of the successfully released beam structure.

RIE is a dry etching technique and its etching type is anisotropic. However, sidewalls are slightly undercut in practice. In order to show this issue, a plain silicon wafer was covered by a photoresist and a window was opened. RIE has been performed so that the resulting silicon etched well is 5µm. The sample has been cut and observed under SEM as shown in Figure 3.13. Resulting side wall etch is around 1µm. This undercut becomes important where the photoresist protected areas are narrow. Because the tethers are 50-100µm wide, this issue would not cause a significant problem.

It is important to optimize the RIE process including choosing the gases, their flow rates and plasma conditions. If sufficient power and plasma settings are not achieved, etching may not work well. Figure 3.14 shows an under-etched beam device where RIE did not work properly. Because the gas flow rate is not sufficient, small remainders could not be etched.

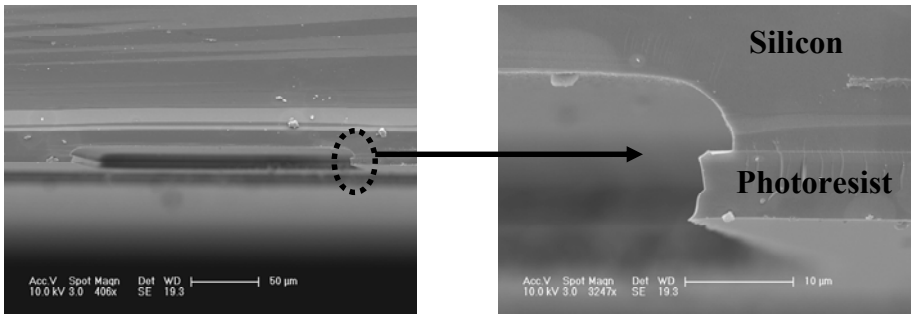


Figure 3.13: Undercut phenomena of the anisotropic RIE process; a) Side view of the well, b) Side view of the etched sidewall.

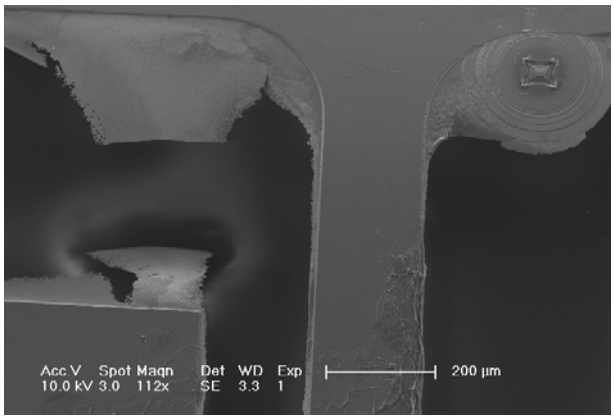
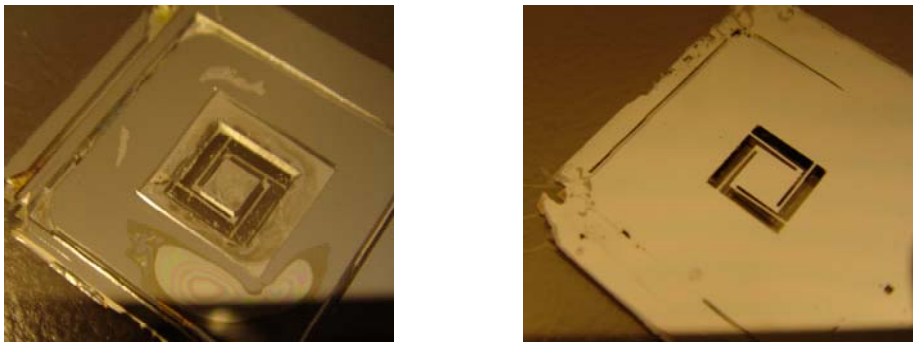


Figure 3.14: SEM photograph of an under-etched beam structure during RIE.



(a) **(b)**

Figure 3.15: Photographs of the beam structure; a) Back side view, b) Front side view.

Whole device photographs after the release procedure are given in Figure 3.15. Here, Figure 3.15a is the back side view. It can be seen from the front side view (Figure 3.15b) that the tethers are slightly displaced due to the gravitational force on the proof mass.

During the process, several beam structures have been cracked, damaged and malfunctioned due to mainly the improper handling. It has been shown in Chapter 2 that the maximum stress occurs at the edges of the tethers. Therefore, most of the device failures arise at the high stress points. Figure 3.16 shows a cracked sample.

3.4 A Novel MEMS Packaging Method

MEMS packaging methods differ from the microelectronic packaging since they have moving parts. In this thesis, a novel packaging approach is proposed which is suitable for preliminary prototypes. It has already been explained that PDMS patterned glass slides are used as a carrier which facilitate the handling. The depth of

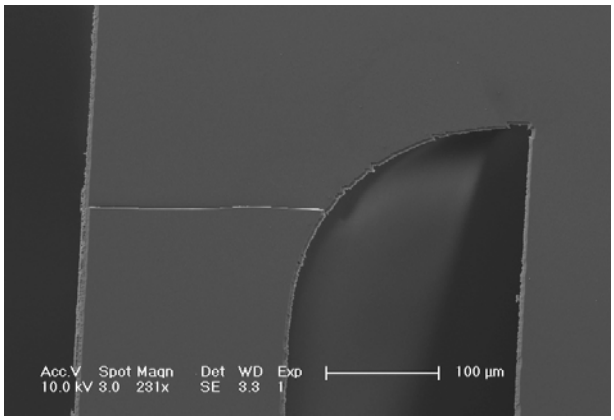


Figure 3.16: SEM photograph of a cracked sample.

the PDMS well also determines how much the proof mass bends downward. But same limitation should be utilized so that upward bending can be limited, too.

For 300µm proof mass, the bottom PDMS well is fabricated to yield a depth of 500µm which limits the proof mass downward bend to 200µm. On the other hand, the top PDMS well has a depth of only 200µm. In order to determine the spinning conditions required to get the desired thickness of the PDMS layer, Figure 3.10 is used.

The top PDMS patterned glass slide is attached to the bottom one after the plasma treating. PDMS to PDMS bonding is pretty strong and irreversible. Because the glass slides and PDMS layer are transparent, it is not hard to align the top PDMS well to the device. Figure 3.17 shows a photograph of the proposed packaging method. Here, the "smart sand" device is surrounded by two PDMS patterned glass slides.

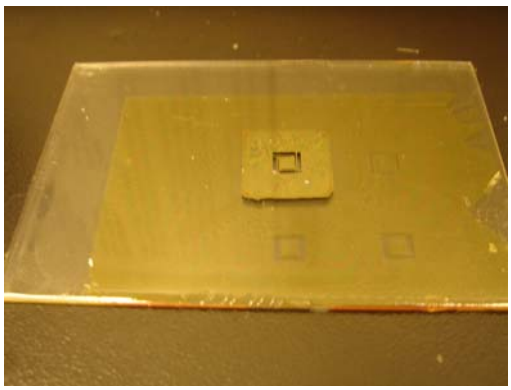


Figure 3.17: The proposed packaging method including "smart sand" and two PDMS patterned glass slides.

3.5 Silicon Stress Tests

As previously mentioned in Chapter 2, silicon cantilevers can stand up to 500MPa **(Wilson et al., 1997)** under the assumption of the bulk micromachining processes. In this thesis, SOI wafers are used as the bulk material. Therefore, in order to clarify whether this assumption is valid for SOI substrates, some simple tests have been carried out.

Cantilever beams have been fabricated using SOI substrates. Following the back side etching with KOH, front side of the wafer is etched with RIE and the cantilever is released as shown in Figure 3.18a. The cantilever is 5µm thick, 425µm wide and 1mm long. Beam has been deflected around 200µm with a micromanipulator as shown in Figure 3.18b. This process has been repeated more than hundred times and beam has not been damaged. COMSOL MULTIPHYSICS™ simulations show that 200µm of displacement corresponds to 700MPa which is already more than the fracture strength of the silicon beam.

Same tests have also been carried out for the "smart sand" devices without PZT layer on them. It has been observed that increasing displacements up to 200µm results in proof mass rotation, which is expected. When the point load (the tip of the micromanipulator can be assumed a point force load) is not applied to the exact center of the proof mass, the rotation and bending of the tethers increase dramatically and tethers have broken in some tests. In practice, though there will be a distributed force on the proof mass from vibrations or shock loads, and such point force effects are not anticipated.

(a) **(b)**

Figure 3.18: Silicon cantilever failure tests.

3.6 PZT Deposition

PZT deposition is one of the main fabrication challenges during this thesis. Piezoelectric layer will be deposited onto the tethers and they will generate voltage under stress. Simulations have shown that 1-2μm thick piezoelectric layer is necessary to achieve sufficient voltage levels. For this purpose, Lead-Zirconate Titanate (PZT) was chosen for piezoelectric layer, since it can be coated as relatively thick layers.

It is known that piezoelectric thin films that are micrometers thick are hard to fabricate and pattern. There are mainly two ways to deposit the PZT layer onto the silicon substrates. One way is to use a PZT crucible and evaporate it onto the substrate by magnetron sputtering. But this process takes hours and it gives only 50nm of good quality PZT layer for one step. In order to achieve thicker films, several steps are needed, which would take days.

Another way is sol-gel deposition. It is faster than the evaporation method. Sol-gel PZT is commercially available from Mitsubishi Materials. Basically, it is spun onto the substrates and baked, similar to the photoresist coating processes. However maximum thickness of a PZT layer for one coat is 250nm. So, several coating steps are needed to reach the desired thickness.

Because the compounds of PZT solution can react with the silicon substrate, it cannot be deposited directly on silicon wafers. Therefore, a protective layer, called "seed layer", is used. These seed layers can be insulator layers such as zirconium oxide (ZrO_2) and titanium oxide (TiO_2), or metals such as titanium and platinum.

If the piezoelectric material is stretched or bent, it creates an electrical charge. In order to probe this charge, electrodes are needed. Depending on the electrodes' orientation, different directions of the electric displacement are sensed. If the electrodes are above and below the piezoelectric layer, then, the mechanical stress can be converted to the voltage as shown in Figure 3.19a. In this case, d_{31} is valid as the piezoelectric strain coefficient in (2.26). On the other hand, electrodes can be placed onto the piezoelectric layer like a fingered shape as illustrated in Figure 3.19b. The piezoelectric strain coefficient, then, becomes d_{33}. Basically, these two modes are distinguished by whether the electric field direction is perpendicular to the input strain direction (d_{31}) or parallel to it (d_{33}).

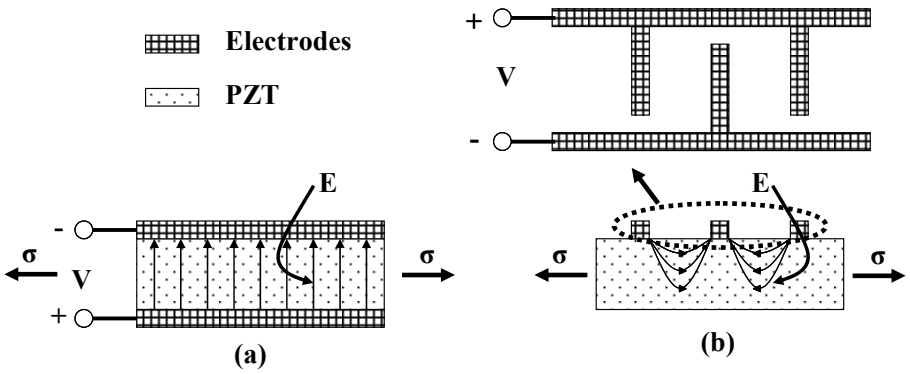


Figure 3.19: Two modes of the piezoelectric conversion from the mechanical stress; a) d_{31} mode, b) d_{33} mode **(Jeon et al., 2005)**.

The voltage generation by the piezoelectric layer is directly related to the distance between the electrodes; film thickness for d_{31} mode and electrode spacing between fingers for d_{33} mode. Increasing the piezoelectric thin film thickness results in more voltage for the d_{31} case, but it is hard to achieve a PZT layer thicker than 2µm. Jeon et al. (2005) depicts that distance between fingered shaped electrodes can be ten times longer the PZT thickness. In addition, the magnitude of the d_{33} coefficient is 2–2.5 times higher than the d_{31} coefficient **(Jeon et al., 2005)**. On the other hand, the electrodes for d_{31} case can be covered the PZT surface entirely, however for d_{33} case, electrodes do not cover all the PZT surface, which result less voltage generation from the electric field lines. Therefore, both cases give almost same levels of voltage values.

In the concept of this thesis, the fabrication of both modes is investigated. Therefore, fabrication method for the metal electrodes will be explained in the next section.

3.6.1 Fabrication Method for the Metal Electrodes

Electrodes are used to make contacts to the piezoelectric layer. Electrodes are usually made of inert metals such as noble metals. Noble metals are resistant to corrosion or oxidation, unlike most base metals. They tend to be precious metals, often due to perceived rarity. Examples include gold, silver, tantalum, platinum, palladium and rhodium. Mostly used metals for the piezoelectric applications are gold and platinum.

These noble metals can be dissolved in “aqua regia”, a highly concentrated mixture of acids (1:3 nitric acid: hydrochloric acid). This solution can be used as an etchant. However, introducing acid based etchants to the process is not preferred because they

may harm the previous processes such as MOS circuitry. Therefore, a patterning method, called lift-off, is used, as it does not require any acid processing. Unlike the standard lithography process, first the photoresist is coated and developed, and metal is deposited on top; undesired metal is then flushed away during photoresist removal. Photoresist is coated onto the lift-off resist which is isotropically etched with the photoresist developer. MicroChem's line of LOR lift-off resists are based on the PMGI (polydimethylglutarimide) platform and are well suited for a variety of critical and non-critical level lift-off processes. Used in combination with conventional positive resists, LOR series are available in a wide range of film thicknesses and undercut rates **(Microchem, 2002)**.

The process flow for the lift-off process is shown in Figure 3.20. Firstly, LOR is spin coated onto the substrate and baked. Then, the photoresist is spun and pre-baked (Figure 3.20a). After exposing and post-baking of the photoresist, sample is put into the developer. Developing time is adjusted so that all the unexposed photoresist is developed and LOR is slightly undercut (Figure 3.20b). Then, metal is deposited onto the patterned photoresist. Because the photoresist and LOR form a mushroom shape, metal cannot fill the undercut parts of LOR (Figure 3.20c). It is important to note that the metal thickness should be lower than the LOR+photoresist thickness. Finally, photoresist and LOR are removed by a solvent such as acetone or NMP (Figure 3.20d).

In this thesis, platinum is used as the electrodes. In order to enhance the adhesion of platinum to the surface of the substrate or PZT thin film layer, titanium is used. Practical values are 50nm of titanium and 100-200nm of platinum.

In the d_{31} mode case, electrodes are placed above and below the piezoelectric layer. Titanium/platinum (Ti/Pt) electrode also serves as a seed layer which eliminates an extra process step. However, lift-off technique cannot be used for bottom electrode since the PZT fabrication requires high temperature which melts the photoresist.

3.6.2 Fabrication of the Electrodes for d_{33} Mode

In the d_{33} mode case, electrodes are placed above the piezoelectric layer only. Therefore, a seed layer should be used at the bottom. Zirconium oxide (ZrO_2) and titanium oxide (TiO_2) are the most used insulating and seed layers for sol-gel

piezoelectric thin films. Fabrication results have been shown that ZrO_2 is the best choice for 1-2µm of piezoelectric layer.

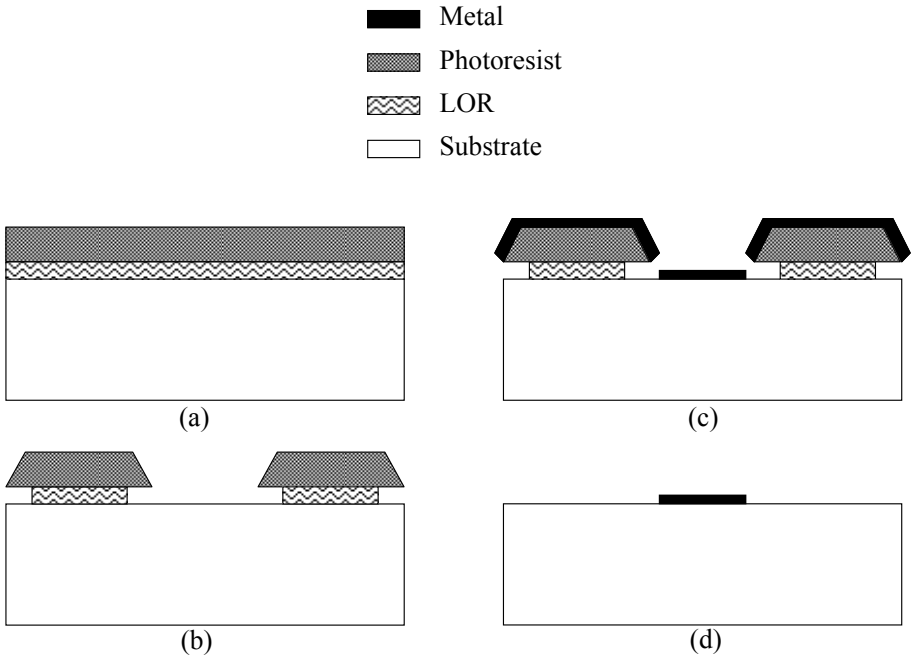


Figure 3.20: Lift-off process flow; a) LOR and photoresist are coated and baked, b) Photoresist is exposed and developed, LOR is isotropically developed, c) Metal is deposited, d) Photoresist and LOR are stripped.

Firstly, test structures with plain silicon wafers are fabricated. They are coated with ZrO_2 and sol-gel PZT is coated. Figure 3.21 shows an SEM photograph of one layer sol-gel PZT coated silicon wafer. It can be seen that there are cracks where no seed layer exists. This layer is 250nm thick.

In order to attain thicker PZT film, multiple coatings are performed. Figure 3.22 shows the top and cut view of the 750nm PZT layer obtained in three successive coats.

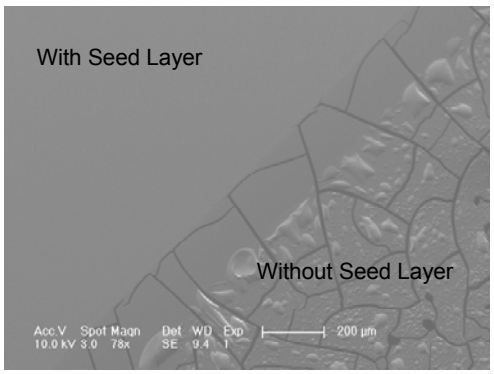


Figure 3.21: SEM photograph of sol-gel PZT coated silicon wafer. There are cracks where no seed layer exists.

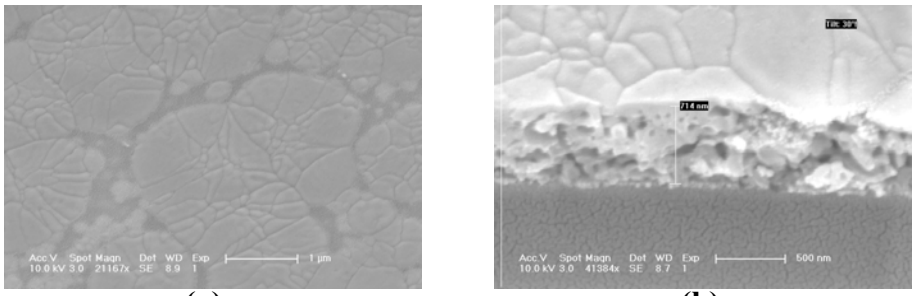


Figure 3.22: SEM photographs of 750nm (3 coats) of PZT film, a) top view, b) cut view.

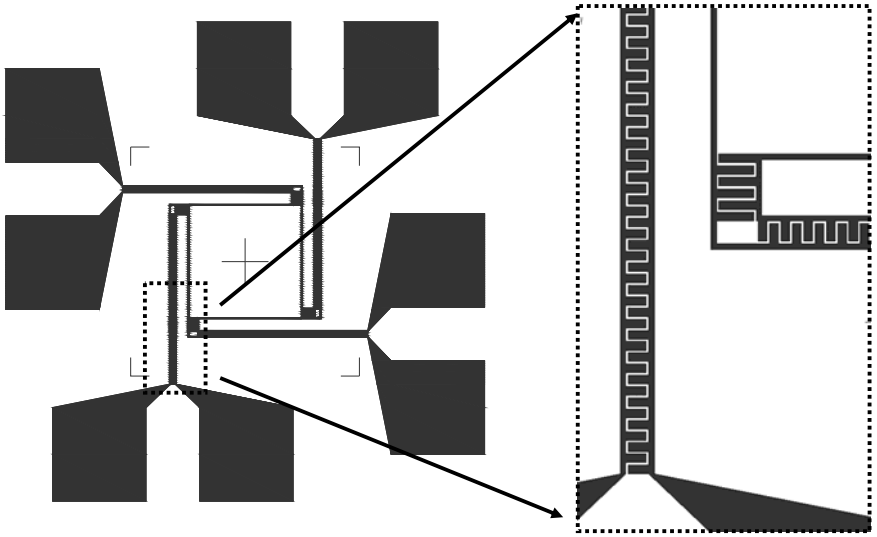


Figure 3.23: Electrodes mask used for the top layer of the PZT film.

The interdigitated electrodes are patterned with lift-off technique. The mask used for the exposure is given in Figure 3.23. Metal pads are used to measure the voltage generated by each tethers.

3.7 Ongoing Fabrication and Tests

Yet the main fabrication challenges were overcome, the integration of the fabrication has been carried out by the project colleagues[11]. In this process flow, DRIE was used for the bulk micromachining and d_{31} mode was targeted which entails to use electrodes at top and bottom. SOI wafers are first cleaned with RCA clean recipe. Oxidation is performed with furnaces at 1000ºC for an hour which yields a 100nm thick thermal oxide. Back side oxide is removed with RIE (O_2, He, CF_4; 100W) and

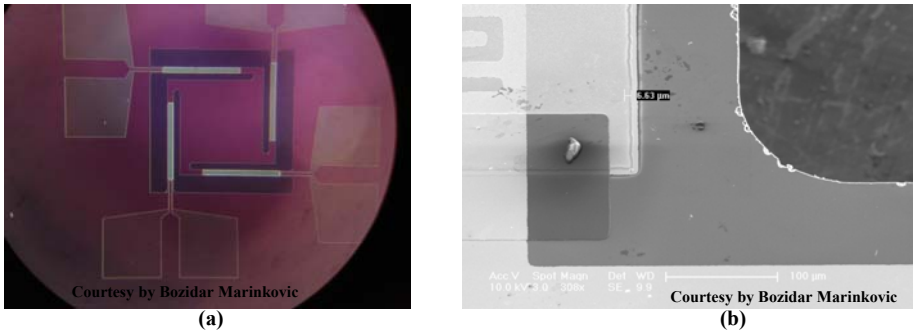
[11] Bozidar Marinkovic, PhD student at Yale University workin with Prof. Köşer, has been working on the integration of "smart sand" devices since the beginning of 2006.

bottom electrodes are deposited by the e-beam evaporator (Ti/Pt; 25nm/75nm). These electrodes are patterned with lift-off and sol-gel PZT is coated for 500nm in three coats. PZT is patterned with acid etch mixture (HCl:BOE:DI; 100:16:200) and annealed at 400ºC for 10 minutes. Then, PECVD oxide/nitride (50nm/200nm) is deposited and patterned so as to prevent contacting top and bottom electrodes. Top electrode is patterned with Ti/Au lift-off and proof mass is formed with DRIE. The SEM photograph of the beam is shown in Figure 3.24.

In this process, 3 layers of sol-gel PZT have been achieved. A cross-section of the PZT thin film is shown in Figure 3.25.

Finally, in order to test the PZT voltage under deflections, simple cantilever beams were fabricated and tested by the colleagues, as shown in Figure 3.26.

Dimensions are 3cm in length, 2.5mm in width and 500µm in thickness. 500nm of PZT is spun. Tests were performed and displacement-voltage graphics are obtained as shown in Figure 6.



(a) (b)

Figure 3.24: The SEM photograph of the beam; a) Whole device, b) Zoomed to the edge of the tethers with interdigitated electrodes.

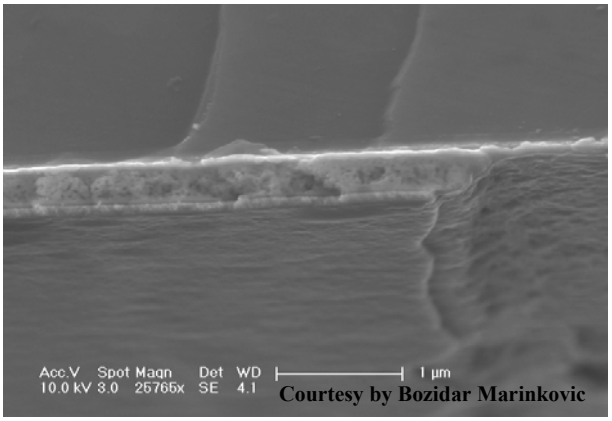


Figure 3.25: Cross-section of the PZT film.

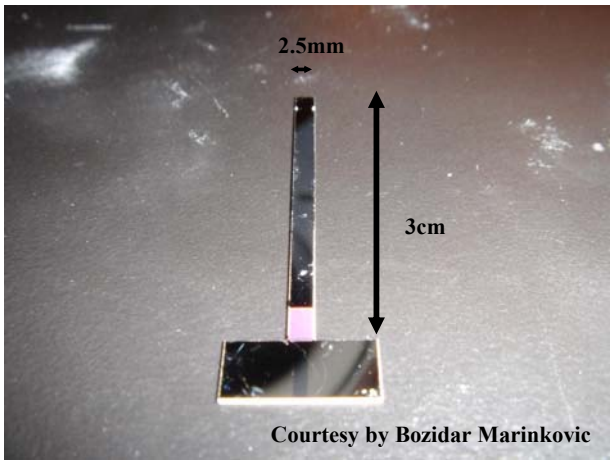


Figure 3.26: Silicon cantilever beam used for voltage tests.

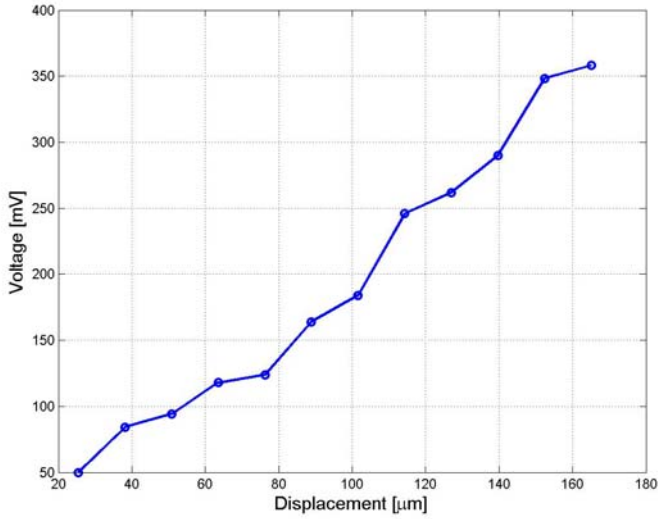


Figure 3.27: Displacement versus peak voltage coming from PZT courtesy by Bozidar Marinkovic.

COMSOL MULTIPHYSICS simulations show that for 100μm deflection, stress level is around 10MPa. Considering 50MPa is tolerable by the piezoelectric thin film layer, it is predicted that 1V of voltage can be attained.

4. COMBINING "SMART SAND" WITH THE RFID CONCEPT

After "smart sand" concept was introduced, system simulations were given and fabrication and preliminary test results were explained in Chapter 2 and 3, respectively. This chapter is focused on potential applications using the "smart sand" design. First, wireless data transmission possibilities are explored; later, an introduction to the RFID concepts will be explained. Then, a new concept -namely "smart RFID"- will be introduced and potential application alternatives will be discussed. Finally, a design example of a CMOS RFID circuit will be given.

4.1 Wireless Data Transmission Possibilities

Once data exists in a sensor system, it should be possible to probe it when desired. Data communication can be achieved by connecting wires; however, this approach is limited to considerably large systems. In small form factor devices, even the communication wires may be larger than the whole system, which would degrade the advantage of the small form factor.

Thus, wireless communication is highly preferred for small systems. Wireless sensor networks have opened new application areas, enabling continuous performance monitoring of large systems, controlling and debugging systems that are hard-to-reach locations.

"Smart sand" devices are mm-sized; hence, in order to create a communication link between the "smart sand" and the user, wireless data transmission possibilities are considered.

Modern communication systems contain transceivers that have capabilities of both transmission and reception. Due to the nature of the "smart sand" devices, transmission is the main concern. Because the generated power levels are on the order of microwatts, a low-power transmission scheme is needed. Most common systems use a power amplifier to transfer the power to the antenna. However, considering the range of meters, milliamps of current is necessary, which is not

possible for the proposed system. In order to alleviate this issue, low-power ultra wide band (UWB) communication is one candidate.

UWB is defined as a signal that occupies a bandwidth wider than 500 MHz or a fractional bandwidth[12] larger than 20% **(FCC, 2002)**. The FCC has approved the use of Ultra-Wideband technology, allowing deployment primarily in the frequency band from 3.1GHz to 10.6GHz **(FCC, 2002)**. UWB technology is expected to improve the performance and reduce the power consumption and cost of short-range wireless communications in applications such as remote controllers and sensor networks **(FCC, 2002, Win and Scholtz, 1998)**. There are several UWB designs that are considered low-power for the range of meters **(O'Donell et al., 2002, Terada et al., 2006)**.

As the short pulses of transmission are enough for UWB systems, it seems suitable for "smart sand" based communication. However, because the scavenger system can only generate power under continuous vibrations or sudden shock impacts, it cannot be guaranteed that the transmission can be performed when desired. Moreover, there should be an invoke procedure so that the transmission is performed.

Considerations of the approach of combining UWB systems on the "smart sand" have opened a new alternative. Since the system should be invoked on demand and any data that has been successfully stored by the scavenger should be probed, RFID systems have been considered as a great possibility for use in several applications. As previously mentioned, RFID systems are energy harvesters since they are powered by an external wireless power source. Besides the well-known operation of the RFID systems, they can be fit into small chips on the order of millimeter, which makes them very attractive to be embedded into the "smart sand" device. Combining RFID concepts into "smart sand" does not only solve the communication issues, but also brings more capabilities to the whole system -such as storing ID information of individual items.

4.2 Introduction to RFID Systems

Radio Frequency Identification (RFID) systems use radio frequency to identify, locate and track people, assets, and animals. Passive RFID systems do not need

[12] The fractional bandwidth is the ratio of the signal bandwidth at 10 dB to the center frequency.

battery like their active counterparts. They are mainly composed of an interrogator (reader) and a passive tag (transponder), as simply shown in Figure 4.1. The transponder is composed of an antenna coil and an integrated circuit (IC) that includes power generation/rectification and modulation/demodulation circuitries and non-volatile memory with its digital logic. The transponder is energized by a radio frequency (RF) wave that is transmitted by the reader. This RF signal is called the carrier signal. When the RF field passes through an antenna coil on the transponder, an AC voltage is generated across the coil. This voltage is multiplied and rectified to supply power to the transponder. The information stored in the transponder is transmitted back to the reader. This is often called backscattering. By detecting the backscattering signal, the information stored in the transponder can be fully identified. Information can also be written onto the transponder during this communication. Practically, the reader sends a signal which can be identified by the transponder as "read" or "write". If the read signal is received, the transponder sends the data by backscattering. When the write signal is detected, the transponder switches to the write mode and sequential data sent by the reader is written onto a non-volatile memory.

The reader is usually a microcontroller-based unit with an output coil, peak detector hardware, comparators, and firmware designed to transmit energy to a transponder and read information back from it by detecting the backscatter modulation.

Unlike passive RFID transponders, active RFID transponders have a battery which is used to power the IC. Active transponders, thanks to their onboard power supply, transmit at higher power levels than passive transponders, allowing them to be more effective in "RF challenged" environments like water, metal, or at longer distances. Another advantage of the active transponders is that they can include sensors such as temperature logging which have been used in concrete maturity monitoring or to

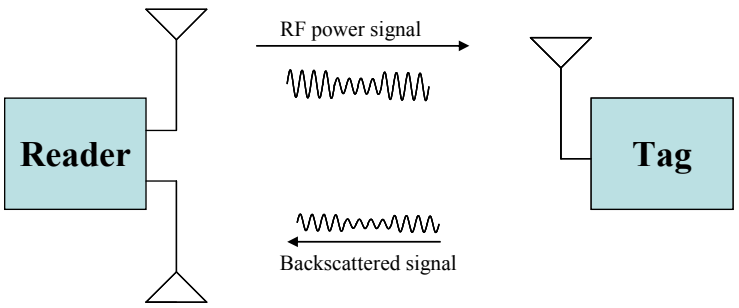


Figure 4.1: A simplified block diagram of the RFID system.

monitor the temperature of perishable goods. Other sensor applications are also possible, such as humidity, shock/vibration, light and radiation sensing. Active transponders typically have much longer range and employ larger memories than passive transponders, as well as the ability to store additional information sent by the reader. The life time of an active RFID transponder is less than 10 years, whereas, it is unlimited for passive transponders. It is also obvious that the cost is higher than passive transponders, which restricts their use in supply chains.

The carrier signal is an RF sinusoidal wave generated by the reader to transmit energy to the transponder and retrieve data from the transponder. This carrier signal is modulated by changing its amplitude (Amplitude Shift Keying, ASK) or phase (Phase Shift Keying, PSK).

There are various frequency ranges that are used in RFID systems. They can be basically divided into three groups in terms of their center frequency; low, high and ultra high frequency systems. Low frequency (LF) systems include 130kHz and 145kHz. High frequency (HF) is 13.56MHz. Finally, ultra high frequency (UHF) systems operate at 433.92MHz, 915MHz or 2.45GHz.

The wavelengths of the LF and HF frequencies are very big (larger than 10 meters, up to kilometers) considering the distance between the reader and the transponder. Therefore, these systems operate in near-field region[13], and the reader should be inductively or capacitively coupled to the transponder. Antennas are composed of many coil turns to achieve high coupling. In this region, the magnetic field strength attenuates with d^{-2}, where d is the distance between the reader and the transponder; hence the operating distance is practically restricted to less than 1 meter.

In order to achieve a higher operating range, system frequency should be raised so that it operates at the far-field region where the magnetic field strength attenuates with d^{-1}. In the far field region, electric and magnetic fields are in phase and electromagnetic waves constitute an electromagnetic field. Therefore, UHF passive tags are usually radiatively coupled (backscattering) to the reader antenna and can be employed with conventional dipole antennas. Operating ranges can go up to several meters and antenna sizes get smaller since the wavelength is on the order of

[13] If the radiation distance is smaller than $\lambda/2\pi$, electromagnetic waves have near-field propagation characteristics, otherwise, they exhibit far-field characteristics. Here, λ denotes the wavelength of the carrier frequency.

centimeters. Furthermore, for dipole antennas, the real part of the antenna impedance is almost constant[14].

Although the operating range is higher in UHF systems, shorter wavelengths are more susceptible to absorption by liquids. A UHF tag can be used for water- or liquid-bearing containers, but its effective read range would be drastically reduced. Conversely, LF waves can travel even through brick and stone.

4.2.1 Current Uses of RFID Tags

RFID systems are used extensively in several applications. As the cost of an individual passive tag goes down from 50¢ to 5¢, RFID tags become attractive and start to share the market of the barcodes **(Sarma, 2001)**.

Since the standards for RFID passports have been determined by the International Civil Aviation Organization **(ICAO, 2006)**, many countries have started to use RFID tags in the passports – so called e-passports. In addition to information contained on the visual data page of the passport, those tags can record the travel history (time, date and place) of entries and exits from the country as well.

RFID has been used in the motorways and bridges as a payment system for over ten years. Besides the public transportation payments, RFID systems can be adapted by most of the payment applications. For example, embedding the RFID tags into ski passes provide skiers hands-free access to ski lifts. Skiers don't have to take their passes out of their pockets.

RFID tags are used in library book or bookstore tracking, pallet tracking, building access control, airline baggage tracking, and apparel and pharmaceutical item tracking. Some credit card companies are also putting RFID tags into their cards, replacing the magnetic stripe cards **(ExpressPay, 2005)**.

Since the 1990s, RFID tags have been used in car keys. The car does not start unless the RFID tag data is matched. Furthermore, Toyota has developed a smart key **(Toyota, 2004)**. The key uses an active RFID tag allowing the car to detect the key

[14] In the far field region, dipole antenna's real part impedance approaches to free space impedance, η_0, which is equal to $\sqrt{\mu_0/\varepsilon_0}$, where μ_0 and ε_0 are free space permeability and permittivity, respectively. The impedance value is 375Ω.

approximately at 1m from the sensor. The driver can open the doors and start the car with the key in a purse or pocket. As TREAD Act mandates, each car should have a tire pressure sensor **(TREAD, 2000)**. Car and tire companies such as Michelin and Ford and some electronics companies such as Motorola and Philips Semiconductors have been working on such sensors with embedded RFID tags so that a wireless communication can be established between the sensor and the front panel of the car **(Philips Semiconductors, 2002)**.

Even though barcodes are used in item level tracking, starting from the case and pallets, RFID tags penetrate the market. One of the biggest supermarket chains in the U.S., Wal-mart, decided to use RFID tags for case and pallet tracking and mandated to its top 100 suppliers to put RFID tags carrying Electronic Product Codes (EPC) on pallets and cases **(Manish and Shahram, 2005)**.

RFID system has also many applications in libraries that can be highly beneficial, particularly for circulation staff. Since RFID tags can be read through an item, there is no need to open a book cover or DVD case to scan an item. Additionally, inventory checking can easily be done while the materials are on the shelf.

4.2.2 Potential Uses of Active and Passive RFID Tags

RFID tags have already started being a rival against the barcodes. The data that a barcode can contain is limited; however, RFID tags can have kilobits of memories embedded into the IC. Therefore, companies have recently started using RFID tags at pallet and even at case levels. Because of the cost, barcodes are still dominant at item level tracking.

Hospitals can also use RFID systems to identify patients or permit relevant hospital staff to access medical records.

Active RFID systems with sensor capabilities can be deployed on bridges and they can warn if the bridge reached its critical structural stress point (stress sensor) or the bridge is icy (temperature sensor). These sensors can also be embedded into the bricks and temperature or vibrations can be sensed and data can be transmitted wirelessly.

The main motivation in this thesis is to combine the “smart sand” concept with the RFID systems and realize an RFID transponder with sensor capabilities but without the need of a battery, unlike the conventional active RFID systems.

4.3 A New Proposed RFID Concept: Smart RFID

In this thesis, the “smart sand” approach is incorporated with RFID technology so that an RFID system with sensing capabilities is constructed without a battery. The system is called “smart RFID” because the resulting RFID tag has sensor capabilities, such as temperature and acceleration. RFID circuits, including a rectifier, memory and a local oscillator are placed onto the proof mass. If the RF carrier frequency is selected to be high (2.45GHz or higher), antenna can be small (on the order of a centimeter) and placed around the frame. By this method, antenna becomes a part of the package. Otherwise, like conventional RFID tags, antenna is put on a sheet and assembled with the circuitry.

Smart RFID operates in two modes; offline and online. In the offline mode, there is no transmission happening, i.e., system is not invoked by the RFID reader. However, ambient vibration energy is scavenged and used for the circuitry. The basic idea for the harvester is to use sudden accelerations or continuous vibrations as energy sources. The main goal is to write a bit of memory if the predetermined value (temperature or acceleration) is exceeded. When the system is in the online mode, this means a reader invokes the smart RFID tag and the written data with the ID on the memory is sequentially backscattered to the reader or an ID is written onto the memory.

4.3.1 System Overview

Most of the RFID transponders have the similar architecture as shown in Figure 4.2. However, building blocks vary mostly in terms of frequency, modulation/demodulation methods and memory arrangements.

Each block in this architecture will be briefly introduced and design specifications will be given in the following sections.

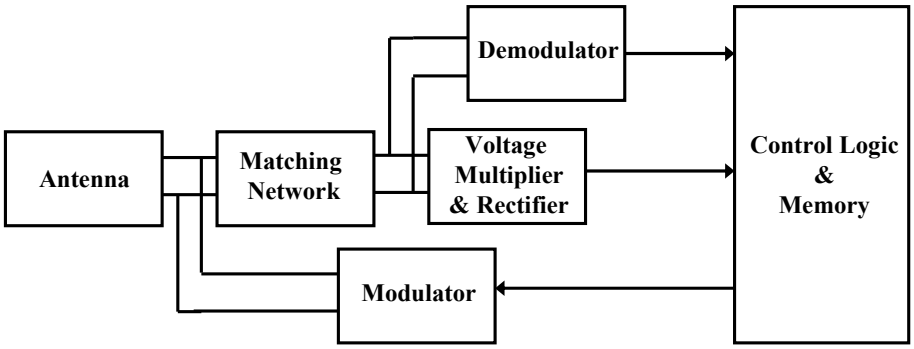


Figure 4.2: The architecture of the passive RFID transponder.

Here, it should be noted that process selection is also a key factor. Because low voltage and low power operation are needed, it is better to use small channel length processes, preferably smaller than 0.35µm. On the other hand, if UHF operation is considered, than, fast transistors should be used in some blocks. However, for LF operation, 0.35µm or even higher processes can be used.

4.3.2 Antenna and the Matching Network

Communication over the free space is achieved by antennas. Depending on the frequency of operation, appropriate antenna type and size are selected. LF and even HF operation systems operate in near field since the wavelengths are long and attenuation of the electric and magnetic fields are proportional to d^{-3} and d^{-2}, respectively. Therefore, communication is ensured via either capacitive coupling through interaction with the electric field or inductive coupling through interaction with the magnetic field. Inductively coupled systems, which are preferable, use small loop antennas. Basically two small loop antennas at the transponder and the reader side form a transformer. The communication range is practically limited to 1 meter. For example, close proximity cards use inductive coupling.

On the other hand, UHF systems operate in far field region. Reader radiates the signal and transponder receives this electromagnetic wave. Half dipole, folded dipole and microstrip patch antennas are widely used. The received power by the transponder, P_r, is given as **(Curty et al., 2007)**;

$$P_r = P_{EIRP} G_t \left(\frac{\lambda}{4\pi d} \right)^2 \qquad \textbf{(4.1)}$$

Here, P_{EIRP} is the effective isotropic radiated power by the reader which can be 500mW, 2W or 4W depending on the communication regulations. The gain of the antenna is denoted with G_T, which is in the range of 0-2.15dB. The distance between the transponder and the reader is represented with d. If 4W reader operates at 2.45GHz and the transponder's antenna has a gain of 0dB, then the received power from 1 meter will be 400μW. It is obvious from (4.1) that increasing the distance causes the received power to decrease. Therefore, the power consumption of the transponder itself basically determines the communication range.

The received power equation in (4.1) is not the available power for the transponder if the antenna impedance is not matched to the input impedance of the transponder. Therefore, it is crucial to use a matching network. The impedance of the antenna depends on its type. If the antenna size is selected as the fixed ratios of the wavelength of the frequency of the operation, then its impedance can be well defined. Hence, the input impedance of the transponder becomes critical. After a well characterization of the input impedance, a matching network is used. Maximum power transfer between two nodes is achieved when the impedances are complex conjugates **(Lee, 2004)**. For this purpose, passive devices (inductance and capacitance) are used to get this relationship.

4.3.3 Voltage Multiplier and Rectifier

Since the passive transponders do not have an external power supply, the incoming RF signal power should be converted to DC to be used for all circuitries. The basic idea is to store the charge on a large storage capacitor (on the order of hundred picofarads). However, because the RF signal is sinusoidal, if the storage capacitor is directly connected to the RF line, then, capacitor is not only charged but also discharged. In order to prevent discharges, diode bridges are used. Moreover, the signal at the RF front end of the transponder may go low due to the power degradations as the range increases. Therefore, voltage multiplier circuits are used.

An N-stage voltage multiplier, shown in Figure 4.3, consists of N cascaded voltage multipliers which are also known as peak detectors **(Karthaus and Fischer, 2003)**. Each stage has 2 diodes and 2 capacitors. Last stage's capacitor, indicated as C_S, is significantly larger because its stored charge is used as supply voltage. Diodes are

eventually transistors that are diode connected, i.e., their gates are shorted to their drains. The load current is represented by a current source, I_L.

The voltage at the N-stage multiplier output can be simplified as

$$V_{DD} = N\left(V_{in,p} - V_D\right) \tag{4.2}$$

where, N represents the number of multiplier stages cascaded and V_D is the diode voltage drop when it draws current. It can be seen from (4.2) that the peak input voltage, $V_{in,p}$, should be higher enough than each diode voltage drop so that the supply voltage can reach the desired voltage level. Here, the storage capacitance, C_S, should be selected carefully. The charge on C_S is the supply voltage for the circuitry and as V_{DD} goes down, circuitry performance degrades. Minimum storage capacitance is determined considering the current consumption of the transponder and the tolerable voltage drop for the power supply. For example, 200pF of C_S is enough if 0.3V voltage drop is acceptable while circuit draws 100μA during a short period of 600ns.

On the other hand, increasing the power signal as the reader approaches to the transponder causes higher voltage levels that may exceed the voltage limits of the active devices. Therefore, limiter or regulator circuits should also be used. A simple clamping circuit is shown in Figure 4.4.

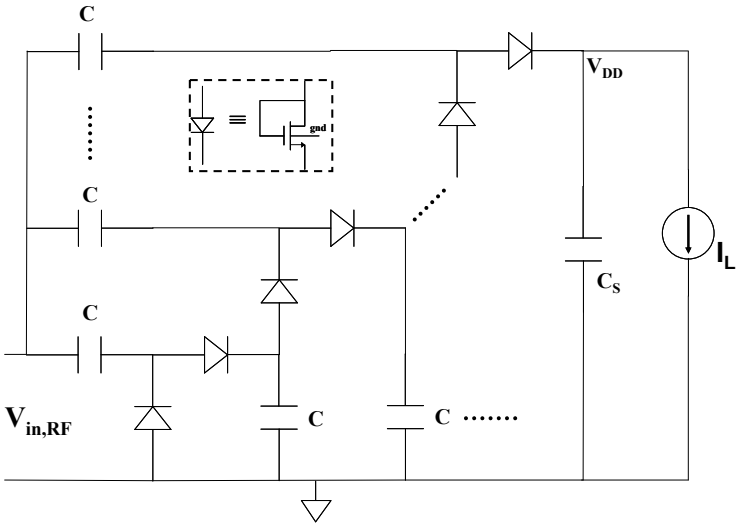


Figure 4.3: An N-stage voltage multiplier.

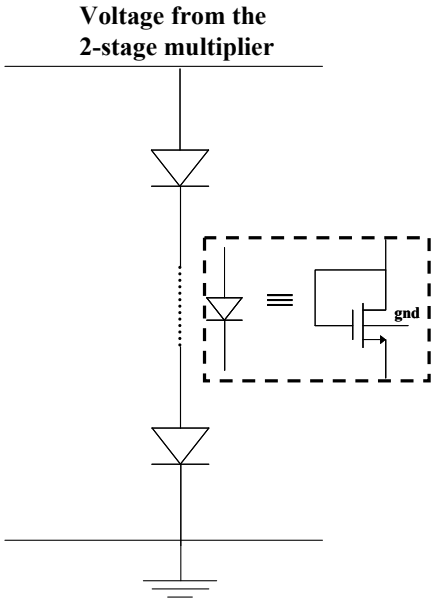


Figure 4.4: The clamping circuit representation.

4.3.4 Demodulator

The transmission from the reader to the transponder is based on the modulation of the carrier signal which is a sinusoid. This signal is modulated by a coding scheme. Then, the transponder demodulates the data and operates as what the reader says. ASK is the most commonly used modulation method for reader-to-transponder communication. The principle of the ASK relies on modulating the amplitude of the carrier signal with the incoming data, as illustrated in Figure 4.5. The representations of logic "0" and logic "1" change with the modulation type.

Modulation index can be varied typically from 10% to 100%. Demodulation from the signal with a high modulation index is easier and less susceptible to the noise. However, higher modulation index means that less or even no power is transmitted to the transponder. If this issue can be tolerated by the demodulation circuits, 100% modulation can be chosen. ASK with 100% modulation is also called on-off keying (OOK).

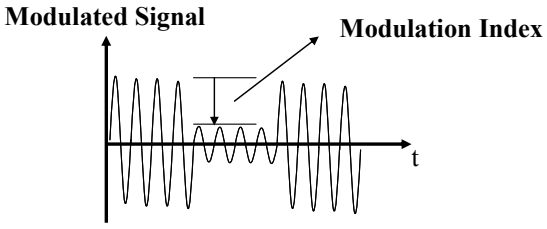


Figure 4.5: ASK modulated carrier signal.

There are several coding schemes as sketched in Figure 4.6. In non-return to zero (NRZ) coding, logic "1" is represented by a "high" signal and "low" signal means logic "0" (logic "1" and logic "0" will be represented by "1" and "0", respectively, for simplicity). Manchester coding has transitions for each bit; if the transition is a rising edge, this corresponds to "0" and falling edge is "1". It is also known as split-phase coding and a self-clocking coding; clock can be generated from the data. Therefore, this scheme is generally used for transponder-to-reader transmission based upon load modulation using a subcarrier, which will be discussed later. In modified Miller coding, each "1" causes a short pulse with respect to the period of the data at half bit. A "1"-"0" code transition does not generate a pulse. For a sequential "0" that is "0"-"0", one pulse is generated at the start of the bit. Pulse-pause coding (PPC) is similar to modified Miller, but in this case, each "1" is represented with a short pulse of duration t_{pulse} in a period of T ($T >> t_{pulse}$) and each "0" is represented with a short pulse of duration t_{pulse}, but in a period of 2T.

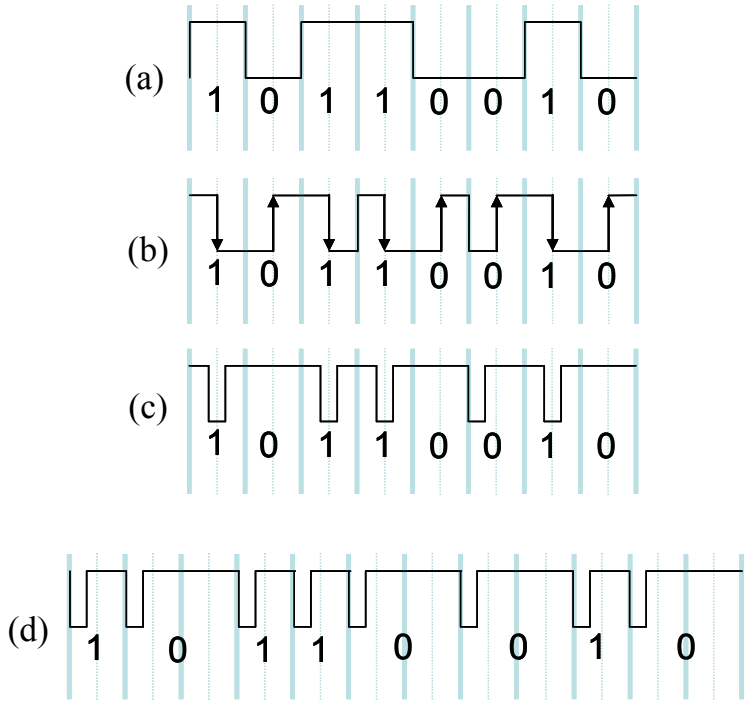


Figure 4.6: Different coding schemes; a) Non-return to zero (NRZ), b) Manchester, c) Modified Miller, d) Pulse-Pause (PPC).

Pulse coding methods are suitable for the transmission from the reader to the transponder. It is important to note that, pulse durations should be short enough to

avoid long power cuts for the transponder and long enough to give the necessary time to the transponder for evaluating the operation dedicated by the reader.

After the demodulation scheme is selected, an envelope detector is used to construct the data from the demodulated information. For this purpose, average detectors are primarily used. A simple envelope detector is shown in Figure 4.7. The *RC* time constant is adjusted so that the incoming demodulated data can be recognized.

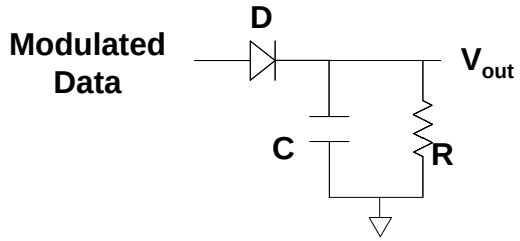


Figure 4.7: A simple envelope detector.

Here, it is also important to demodulate the data with a synchronized clock signal. Pulse coding schemes or transition codes are suitable for this purpose. Using appropriate circuits, clock can also be generated while data is reconstructed.

In this thesis, a new pulse-pause coding scheme that simplifies the clock generation and demodulation is proposed. Detailed analysis and simulations will be given in 4.5.3.

4.3.5 Modulator and Clock Generation

Most of the RFID transponders use backscatter modulation in order to send the data from the transponder to the reader. The basic idea of the backscattering modulation is to change the input impedance of the transponder. If matching is ensured, this means the incoming signal power is absorbed by the transponder and no reflection occurs. However, if the matching cannot be established, incoming signal is reflected by the transponder. If the matching condition is intentionally corrupted, the reader can sense these corruptions and reconstruct the data. This method is also known as “load modulation”. There are two popular methods: PSK and ASK modulations. The schematic representations of these two methods are shown in Figure 4.8.

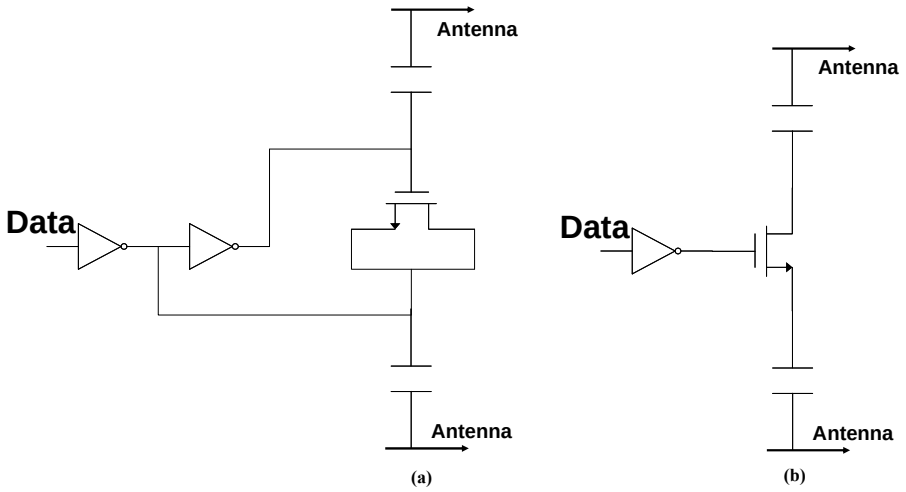


Figure 4.8: The load modulation schemes, a) PSK, b) ASK.

The clocked data coming from the control logic is applied to the input of the modulator and antenna impedance is changed. If PSK is used, a MOS varactor is used as shown in Figure 4.8a and depending on the logic level of the data, phase of the antenna is changed. If ASK is used, incoming data changes the input resistance.

The clock signal is recovered by the demodulator while demodulated data comes. However, during communicating from the transponder to the reader, the reader only sends the power signal that does not contain a data clock. There are two ways to generate a clock signal for modulation; internal clock generation or extraction clock from the incoming power signal using divider.

If a divider is chosen, the RF signal should be divided so that the resulting frequency of the clock is low enough to ensure data rate is not so high. Using an asynchronous divider, each stage gives the half of the input. So, the number of stages needed to attain low data rates would be around 10. It is well known that the dynamic power consumption of a CMOS digital circuit is directly related to the frequency of the operation **(Kang and Leblebici, 2003)**. Therefore, the power consumption of the divider would be considerably high.

Thus, internal clock generation circuits are preferred since the power consumption can be lowered. The simplest way is to use a ring oscillator as an internal local oscillator. The major disadvantage of the ring oscillator is that the oscillation frequency depends on the power supply. Since the propagation delay of an inverter is directly related to V_{DD}, variation on the power supply will change the frequency of oscillation **(Kang and Leblebici, 2003)**. However, readers are designed to tolerate

clock variations and complex data and clock recovery circuits embedded to the readers ensure to detect the clock frequency successfully since the power consumption of the readers are flexible because they use external power sources such as batteries.

4.3.6 Control Logic

Passive RFID transponders include a small memory, usually 64-bit or 96-bit. This memory is used to store the ID of the individual item. After production of transponders, specific IDs should be written onto this memory. Also, ID information can be read by the readers. Because the communication between the reader and transponder can be performed through a bit channel, data transfer should be carried out serially.

Memory cells are placed in rows and columns so that each cell has a specific address. Thus, a control logic is needed. The main function of the control logic is to control which memory cell is to be written or read. But some functions such as collision detection and encryption are also embedded into the control logic block.

Memory access by the control logic can be in two ways: The simplest way is to increase a counter built in the control logic and sequentially read or write data. This way, however, it is not possible to access a specific memory cell. Second and more complex method is to select an address first, then read or write data. This method allows to access to a specific memory cell at the cost of speed, because several clock cycles are needed in order to read/write data.

4.3.7 Memory

Since portable devices are used in the market extensively, non-volatile memories (NVM) have become very attractive and researches have focused on developing highly efficient, high density, low power and high endurance memories. Non-volatile random access memories (NVRAM) are non-volatile and also re-writable. Therefore, this section will focus on NVRAM alternatives.

There are a few NVRAM cells those of which are EPROM (Electrically Programmable Read Only Memory), EEPROM (Electrically Erasable and Programmable Read Only Memory), Flash, MRAM (Magnetic Random Access

Memory), MNOS (Metal Nitride Oxide Silicon), SONOS (Silicon Oxide Nitride Oxide Silicon), FeRAM (Ferroelectric RAM).

First, floating gate based memories will be explained. Then, MRAM approach will be discussed. Later, other alternatives will be briefly introduced and an extensive comparison will be performed considering the "smart RFID" platform.

4.3.7.1 Floating Gate NVRAM Topologies

The floating gate NVRAM device has a floating gate that is isolated within the gate dielectric as illustrated in Figure 4.9. Except the floating gate layer, device is similar to the MOSFET. The top gate is used to control the device, called control gate. The idea of the floating gate memory is to inject and store a charge on the floating gate that alters the effective threshold voltage of the transistor. By applying high electric fields to the control gate, electrons are forced onto the floating gate which results an increase of the threshold voltage. After the electric field is removed, this charge is trapped by the surrounding insulator. Therefore, the transistor has two states whether the floating gate is charged or not. Applying a voltage between these two threshold voltages causes the transistor on or off depending on its state and this state is recognized by appropriate circuitry.

There are two mechanisms to force a charge through the insulating oxide layer; hot-electron injection (HEI) and Fowler-Nordheim (FN) tunneling **(Pavan et al., 1997)**. In HEI, a lateral electric field between the source and the drain is created by applying a high voltage onto the drain to accelerate the electrons in the channel, i.e. heats the electrons. At the same time, a transversal electric field is created between the channel and the control gate and injects the carriers through the oxide. FN tunneling is based on generation of a high electric field through a thin oxide

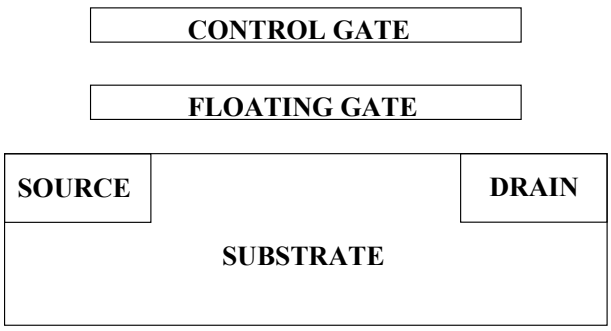


Figure 4.9: The floating gate NVRAM device.

(~10-20nm). When the oxide is thin, the potential barrier of the oxide gets small and high electric fields make the tunneling possible.

There are evolutionary three devices incorporating the floating gate approach; EPROM, EEPROM and Flash memory **(Murray and Buchan, 1998)**. EPROM devices are programmed using HEI but they can only be erased by an external UV light. Electrically erasable version of the EPROM has then been developed which is called EEPROM. The device has thinner oxide layer on top of the drain diffusion that allows FN tunneling during both program and erase operations. Each EEPROM cell contains two transistors; one is for addressing and the other for memory. Flash memories have combined the EPROM and EEPROM with few changes to achieve high density memory cells. Flash memory architecture is constructed in sector formats to enable block erases. Moreover, it has only one transistor for each memory cell. Also, in order to prevent the breakdown of the source-substrate junction, source diffusion is realized larger and deeper than the drain diffusion, which adds one more mask to the fabrication.

The voltage levels for source, drain and the control voltage for operation modes are given in Table 4.1. Typical reference values are 5V for V_{CC}, 12V for V_{PP}, 5-7V for V_{DD} and 1V for V_{read} **(Pavan et al., 1997)**.

While programming, in order to have 3-3.5V voltage shift on the threshold voltage, a pulse width of typically 10-100μs must be applied. Considering the NF tunneling currents are on the order of nano-Ampers, this corresponds to the charge levels of pico-Coulombs.

4.3.7.2 Magnetic RAM Cells

MRAM devices are composed of magnetic tunneling junctions (MTJ). An MTJ cell consists of two ferromagnetic layers separated by a thin tunnel dielectric. The bottom layer is fixed, implying that its magnetic orientation cannot be changed during

Table 4.1: Bias conditions during operation modes of a typical Flash cell, adapted from **Pavan et al., (1997).**

Operation	Source	Control gate	Drain
Read	GND	V_{CC}	V_{read}
Program	GND	V_{PP}	V_{DD}
Erase	V_{PP}	GND	Floating

operation. However, the top layer is called the "free layer" and the magnetic orientation can be changed by the application of a sufficiently large magnetic field. The long axis of the free layer is oriented parallel to the magnetic orientation of the fixed layer, resulting in a magnetic orientation of the free layer in two stable states: in the same direction as the fixed layer (parallel) or in the opposite direction (anti-parallel).

When a bias voltage is applied between the fixed and free layers, a tunneling current flows through the thin dielectric layer. The magnitude of the current depends on the state of the free layer where the parallel state gives higher current. The current-voltage characteristic of the device can be modeled as a nonlinear resistor, with the resistance being dependent upon the state of the free layer. The fractional change in the effective resistance is known as the magnetoresistance (MR), which is defined by

$$R_1 = R_0\left(1 + MR\right) \tag{4.3}$$

where R_1 is the effective resistance of the anti-parallel state and R_0 is that of the parallel state. The values of MR for integrated devices are typically in the range of 30–100% **(Maffitt et al., 2006)**.

The change in the effective resistance (relative to the low-resistance) as a function of the applied magnetic field is illustrated in Figure 4.10. The MR for this particular example is 60%. As can be seen from Figure 4.10 that the switching between the two states is hysteretic, which allows the device to be used as a memory element.

A sample process cut-view is shown in Figure 4.11, this is IBM's 1 transistor 1 MTJ (1T1MTJ) device **(Gallagher and Parkin, 2006)**. The bit line (BL) and write word line (WWL) are used to create necessary the magnetic field by drawing current. Read word line (RWL) is connected to the gate of the transistor which is used to read the resistance value of the MTJ cell. In order to write a data onto the MTJ cell, a pulsed voltage is applied. The current level is determined how much electric field is needed to switch the state of the memory. It has been reported that 5-10ns of pulsed currents in the range of 2.5mA for each plate of the MTJ is adequate **(Maffitt et al., 2006)**. The specifications depict that 20pC of charge should be supplied to the circuitry.

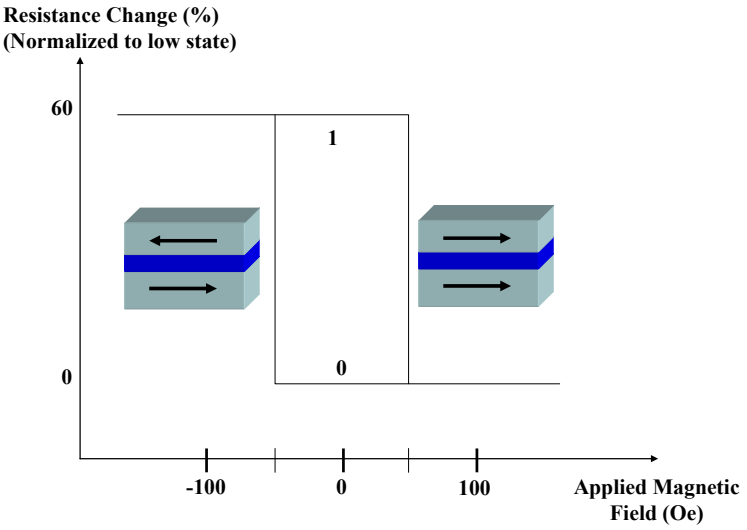


Figure 4.10: MTJ device switching characteristic **(Maffitt et al., 2006)**.

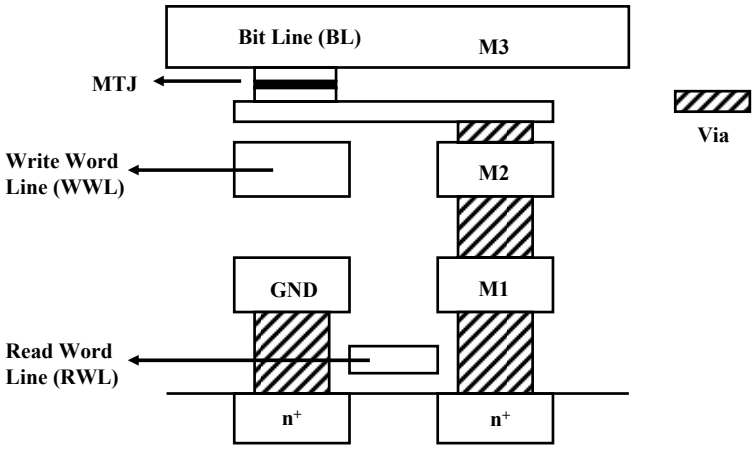


Figure 4.11: 1T1MTJ architecture for MRAM array **(Gallagher and Parkin, 2006)**.

There are several manufacturers working on MRAM such as Freescale, Cypress, Samsung, Honeywell, NEC/Toshiba and Sony. Most of their processes are CMOS compatible.

4.3.7.3 Other Memory Alternatives

Even though they are not as popular and well-known as floating gate and magnetic memory cells, there are also few other alternatives. The MNOS and SONOS devices, for example, have been considered an alternative when first EPROM cells were published, however, they could not reach a big market sizes **(Murray and Buchan, 1998)**. These devices primarily operate based on the traps in the silicon nitride insulating layer. The charges in MNOS memories are injected from the channel

region into the nitride by quantum mechanical tunneling through an ultra-thin oxide which is typically 1.5-3nm.

Ferroelectric memories are also a promising alternative which primarily suffers from the disadvantage of compatibility issues with the standard CMOS processes. The polarization of a ferroelectric material such as PZT can be changed by an applied voltage and retain the charge.

4.3.7.4 Comparison of the Memory Cells

In order to find which memory cell is more suitable for the "smart RFID" system, firstly, memory specifications should be determined.

One of the main concerns is the power limitation of the "smart RFID" during the offline mode. Because the energy is scavenged for only short durations, generated power will be limited. The storage capacitor should be big enough to write a bit of memory in that short duration. On the other hand, because the RFID circuits will be realized by a standard CMOS process, memory device should be CMOS compatible.

The comparison between EEPROM, MRAM and FeRAM are listed in Table 4.2 **(Lenssen et al, 2000)**. Even if the EEPROM is widely used in transponders, their long write and erase times bring difficulties. EEPROM also suffers from the need of high voltage during programming. In order to reach 12V, in practical, a charge pump circuit is used together with a bandgap reference. However, starting from 1-2V up to 12V, startup and pumping take significant time which hardens to use an EEPROM cell to write a bit of data during short durations.

Table 4.2: The comparison of the memory devices **(Lenssen et al, 2000)**.

Specifications	EEPROM	MRAM	FeRAM
W/E time	10-100µs/1ms	5-50ns	5-50ns
W/E voltage	5-7V	1-3V	1-3V
W/E current	nA	mA	nA
Cell size	2-3µm^2	1-2µm^2	2-3µm^2
Extra mask	9	3	3
CMOS compatibility	+	+	-
Maturity	++	+	+

Then, when MRAM and FeRAM are compared, it seems FeRAM has better performance characteristics except the CMOS compatibility which is important. There is only one demonstrated design by Fujitsu that incorporates FeRAM into a transponder **(Nakamoto et al., 2007)**. It seems ferroelectric memory is very promising but obviously not mature to use in the standard CMOS processes. Therefore, MRAM has chosen to be the memory device for the "smart RFID" system.

4.4 Potential Applications of "smart RFID"

In order to clarify the usefulness of the proposed "smart RFID" concept, several application alternatives are considered; namely continuous acceleration monitoring in package delivery, self-powered sensors for homeland security and a battery-less heart rate sensor. It must be noted that potential applications are not limited to these four examples, yet, the concept can be applied to various applications.

4.4.1 Package Delivery: Drop Sensor

Package delivery market is rather large. UPS (United Parcel Services) only delivers 15.6 million packages per day (UPS, 2007). Assuming 10% of those packages are fragile; over one million shipments a day should need extra care. Although insurance can cover some of the damages, there are strict rules in order to get paid. Firstly, fragile item should be packed properly and double boxed. Insurance rates through UPS/FEDEX for high-cost fragile items from $500 up to $50K is $0.50 per $100 value. For a $2K package, this cost reaches $20. Even if this insurance is paid, the package delivery company may still claim that the damage could have been caused by the packaging or that the item was "too fragile" to send with standard delivery methods. On the other hand, even though the package itself may not be damaged, drops or sudden hits may cause damage on the fragile items. Therefore, in order to determine whether the package is dropped or hit, an accelerometer-based sensor can be placed onto or into the package. This method is not only beneficial for customers but also for the delivery companies; it shortens the claim process and saves time and money. Furthermore, this is also a good marketing strategy to take advantage among competitors.

This sensor does not only detect the accelerations, but also it serves as an RFID tag which eliminates the barcode.

When a package is dropped from the carrier to a hard surface floor, it will undergo a sudden change of its momentum. The velocity of the mass can easily be calculated by equating potential energy before it drops and the kinetic energy when it drops:

$$mgh = \frac{1}{2}mv^2 \quad \textbf{(4.4)}$$

Here, m is the mass of the package, g is the gravitational constant (9.8m/s^2), h is the height of the package before it drops and v is the velocity of the package when it hits to ground. It can be seen that the impact velocity is independent of the mass. Assuming the package is carried at a height of 1m, velocity reaches 4.2m/s at the ground. On the other hand, force is equal to the rate of change of momentum:

$$F = \frac{dP}{dt} = \frac{d(mv)}{dt} = m\frac{dv}{dt} = ma \quad \textbf{(4.5)}$$

The momentum of the package changes within a very short time; so dv is assumed to be 4.2m/s as calculated above. The impact duration, dt, is measured around 0.2ms for MEMS packages **(Hauck et al., 2006)**. However, this value reaches up to 10ms for box level items. Therefore, accelerations are on the order of 40-50g. The mechanical system is adjusted so that it generates the necessary voltage level (around 1V) under specific acceleration amplitude.

There is one commercial device that monitors shock loading of fragile packages; these devices contain a tube filled with red liquid held in a suspension **(Shockwatch, 2005)**. When the device is subjected to an impact exceeding a specified level, the shock disrupts the surface tension of the liquid, releasing the highly visible red dye into the length of the tube — creating a permanent and immediate indication of mishandling. Normal movement or road vibrations do not affect the device. Once activated, the device cannot be reset. These shock sensors are available in label, clip, or tube form and acceleration levels of 0.1g up to 100g.

4.4.2 Homeland Security: Surveillance Monitoring

As the security is one of the big issues for countries, a lot of companies are supported by the governments to develop new products for safety and security. After the

terrorist attacks all over the world have peaked in recent years, border security became more important and additional cautions are being sought by ways of law, human source and technology investments.

The U.S. has a very long border with Mexico (3141km long, stretching from California to Texas). Illegal border crossing from this border has reached 500,000/year on average since 1992 after US military withdrew to invest borderline security. Turkey also faces illegal border crossing from Iraq and Iran. There are only few border security points along the border and the rest of the area is practically not protected well, as shown in Figure 4.12. Since these countries are separated mostly by deserts or mountains, the borders are hard to control.

Illegal border crossings cause several impacts. Because those who enter the country are illegal, they work without insurance and do not pay taxes. Furthermore, unqualified citizens suffer from those cheap workers. Besides the economic impact, there are also health issues. Because of no health checks and no chest x-rays for illegal immigrants, there is also a high risk of tuberculosis and other infectious diseases. Abandoned cars and trash during 20-40 kilometers of walk through deserts to reach a U.S. city also affect the environment. Crime such as drug smugglers and terrorism are also consequences of the illegal border crossings.

One of the solutions is to use forward looking infrared (FLIR) cameras which are used for surveillance monitoring (Figure 4.13). A network of thermal imaging cameras enables long-range detection. FLIR Systems offers fixed or patrol vehicle-mounted systems and a wide range of handheld systems, helping ensure the border's integrity 24 hours a day. Each camera has a range of 3km and costs $20,000.

(a) **(b)**

Figure 4.12: Border areas from a) US-Mexico and b) Turkey-Iraq.

Figure 4.13: FLIR cameras **(FLIR Systems, 2000)**.

In this thesis, a new surveillance monitoring scheme is proposed. The approach is essentially based on the smart RFID. **Shenck and Paradiso (2001)** has measured that an average person (68kg) walking at a brisk pace (two steps per second with the foot of 5 cm vertically) generates approximately 100ms of bursts. The operating principle of the smart RFID at borders is similar to land mines. When a certain pressure is applied onto the system, it generates voltage and integrated memory records that a passing has occurred. Adjusting the device dimensions can set the lower limit of the pressure and be limited to the human average weight.

If a reader is placed near spread of devices, continuous monitoring may be possible. Otherwise, each transponder is read periodically to determine the crossing points and gather statistical information.

4.4.3 Perishable Food: Temperature Monitoring

Transportation specifications for perishable food items are among the tightest regulations. The most critical parameter of the delivery is temperature. Frozen foods should be kept below -15ºC. Thawing occurs if the package is exposed to non-freezing environment for more than 2 hours and the item should be disposed in this case. Depending on the food type, refreeze may cause perishing or bacteria formation in even less than 2 hours.

There are a few commercially available products that have temperature logging capabilities. TG-100 is a $40 temperature sensor that displays date, time and temperature for either first or last 100 days, hours or minutes **(Tip Temperature, 2003)**. Another product is Syscan Tempesor™ **(Tip Temperature, 2003)**. It is an active RFID based temperature sensor operating at 13.56MHz. Its read range is 10cm. Each tag costs $10.

The idea of using smart RFID as a temperature sensor is basically similar to Syscan Tempesor™. The smart RFID is assumed to be placed onto or inside the box that contains the perishable food while the box is shipping. Deliveries are carried out with trucks that are equipped with fridges so they can provide a frozen environment. During shipping, there is plenty of vibration and accelerations. **Roundy (2003)** has shown that vibrations in cars are sinusoidal in nature and have fundamental frequencies between about 75 and 200Hz. Therefore, it can be claimed that during movement of a truck, smart RFID can generate its own energy. This energy may be used to operate a temperature sensor and if a predetermined temperature is exceeded, this data will be written onto the memory inside the transponder. When the box is delivered, its ID is read together with the temperature data so that customer ensures that the food has not been exposed to high temperatures.

In this case, in addition to the RFID blocks, a temperature sensor is also needed. For this purpose, a low-voltage low-power temperature sensor was fabricated and tested **(Kaya et al., 2006, Kaya et al., 2007)**.

4.4.4 Heart Rate Sensor

Continuous monitoring of the vital health functions for patients in hospitals or elder people live in nursing homes or assisted living facilities (ALF) is one of the popular research and development subjects in the world. Although full-equipped devices can monitor a person's health, if the person is not in a bed and in a moving condition, it is difficult to use complicated equipments. Instead, small sensors that can be attached to human body are considered a solution. Using RFID in healthcare systems is not new. Some hospitals are using RFID wrist tags to define each patient. A complete wireless network system has also proposed **(Song et al., 2006)**. However, these systems suffer from battery shortcomings, size of the sensors and necessity to be close to the sensor reader.

Heart rate monitoring is a clinically-relevant measurement. Continuous monitoring of heart rates in an ALF greatly helps to foresee heart attacks. If an RFID transponder with a heart rate sensor is attached to an elder person and the ALF is covered with several readers, each person can be successfully tracked. Furthermore, these transponders can also be used for the health history with their embedding memory.

Smart RFID can easily be modified to be used as a heart rate sensor. Heart rates are mostly measured by electrocardiogram (ECG) method. 2 or more leads are attached to the body and electrical activity of the heart is recorded over time. American National Standards Institute (ANSI) provides sample ECG data for ECG machine self tests. A sample data is plotted in Figure 4.14.

Each different shape of peak represents an operating mode of the heart. These different peaks are named waves with the letters, P, Q, R, S and T depending on their characteristics. The QRS complex (the shape from Q wave to S wave) is a structure on the ECG that corresponds to the depolarization of the ventricles. QRS complex has the maximum peak on the ECG. These peaks are usually used for heart rate measurements. The duration of the peak of the QRS complex is around 100ms.

The smart RFID can be placed onto the chest or other impulsive places in terms of heart beads. QRS complex generates a pulse for the smart sand and it generates voltage. Since the QRS complex is continuous, smart sand can continuously monitor the heart rate whether it is under or below a critical limit. These limits can be adjusted by changing device dimensions.

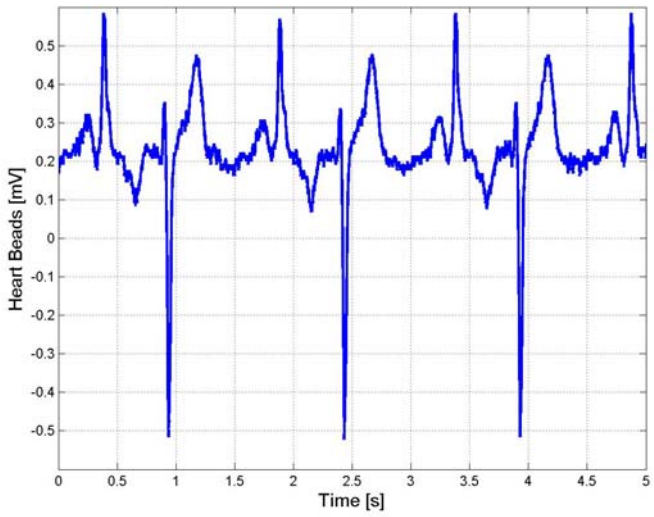


Figure 4.14: An ECG data provided by ANSI.

4.5 RFID Circuit Design

In order to investigate the power considerations, circuit level design is done and necessary studies are carried out. For this concept, the system overview of the RFID tag design is given with a focus on power limitations. What is aimed of this section is

to show the feasibility of using RFID platform in the "smart sand" approach. The circuit design is based on standard CMOS processes.

4.5.1 System Overview and Design Considerations

The block diagram of the RFID transponder is shown in Figure 4.15. The power signal is sent by the reader and reaches the power circuitry (includes voltage multiplier and clamper) and the demodulator. The modulation from the reader to the transponder is on-off keying (OOK) using pulse-pause coding (PPC) which will be analyzed in detail, later. If a write signal (W) is detected by the demodulator, the counter starts with a clock signal synchronized with the incoming data and the data is written onto the addressed memory cell. Here, it must be noted that a few bits of the memory are reserved for the offline data which store the information of vibration, drop or temperature. Those bits are set to "0". If a read signal (R) is sent from the reader, then an internal local oscillator is used as the clock signal and stored information in the memory block is backscattered to the reader.

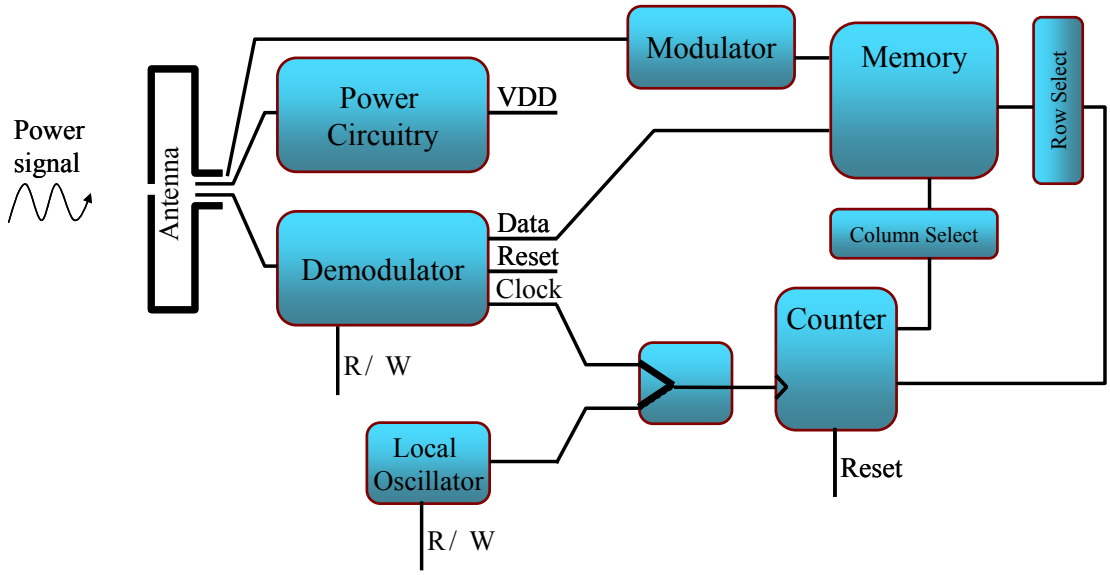


Figure 4.15: The block diagram of the RFID transponder.

Before the R/W signal, a reset is sent and each shift register in the counter is reset. Modulation method from the transponder to the reader is backscattering using modified Miller coding which ensures clock recovery during data transmission from the transponder to the reader. Coding and modulation schemes will be discussed in the following sections.

For the circuit simulations UMC (United Microelectronics Corporation) 0.13µm CMOS process is used.

4.5.2 2-Stage Voltage Multiplier and Clamper

In order to achieve sufficient voltage levels from the RF power signal, a 2-stage voltage multiplier and clamper are used as previously explained in 4.3.3. As the stage number increases, the output voltage of the multiplier increases according to (4.2). However, transistors at the cascoded stages suffer from the body effect and their threshold voltages increase which results in higher voltage drops. The nominal recommended power supply voltage for the selected UMC process is 1.2V. Assuming the available voltage level at the antenna is 0.7V and 1V of power supply is said to be adequate, 2-stage multiplier satisfies the requirement of the voltage level. Storage capacitance, C_S, is selected to be 200pF. Other capacitances are chosen to be 900fF. The gate lengths of the transistors are set to the technology minimum which is 0.12µm whereas the widths are chosen to be 40µm and the multiplier is characterized for various load currents.

In order to obtain the settling behavior of the multiplier, an input voltage with a frequency of 2.45GHz and amplitude of 0.7V is applied. In order to limit the higher voltage levels, a clamper was used. Simulations are performed long enough (5µs) to allow the output reach its final output voltage. The settling behavior of the output voltage for various output load currents is shown in Figure 4.16.

One important parameter for the multiplier is what percentage of the power available to the input can be delivered to the circuitry to be powered from the multiplier. Therefore, the power efficiency, together with the settled output voltages, is plotted with respect to the output load current, as shown in Figure 4.17. The power efficiency reaches its maximum value of 22% at 100µA current. At this load current, the output voltage goes down to 0.8V which can be perceived as a lower limit for circuits to be able to operate.

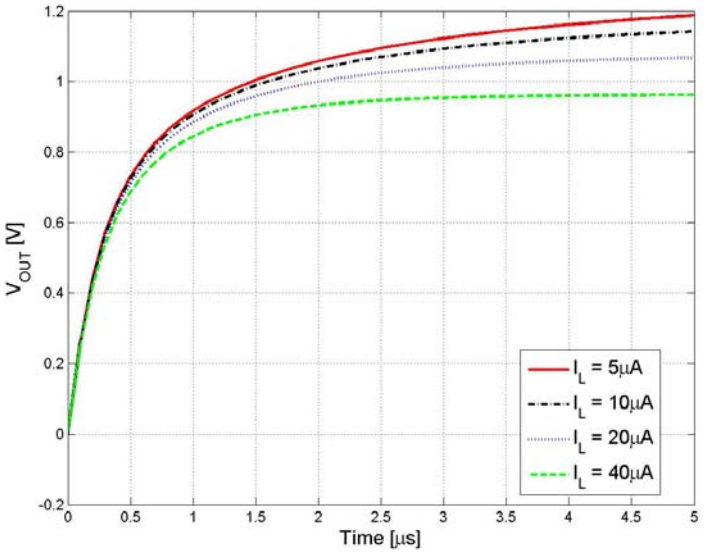


Figure 4.16: The output voltage of the 2-stage multiplier for different load currents.

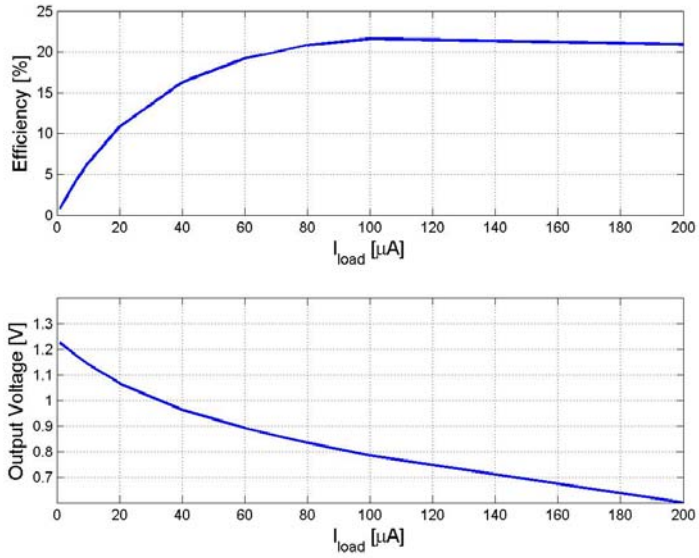


Figure 4.17: Power efficiency together with the settled output voltage with respect to the output load current.

Here, it must be noted that the input resistance is also important. The power available at the input of the multiplier is maximized if the antenna impedance is matched to the multiplier's impedance. Imaginary part of the impedance of the multiplier can be matched with an external inductance and capacitance; however, real part should be at least close to the antenna's resistance in order to decrease the power loss. As shown in Figure 4.18, input resistance is around 250Ω. If a dipole antenna which has a resistance of 375Ω is used, matching can be adjusted by trimming the transistor

dimensions. If lower resistance is desired at the input of the multiplier, it can be adjusted by demodulator's input resistance; it is connected in parallel with the multiplier and its design parameters are pretty flexible compared to the multiplier.

There is a trade-off between the input resistance and the power efficiency. In order to get higher power-efficiency, transistors should not be made very wide, which puts a limit on the input resistance and degrades the available power. Therefore, the optimization should be done taking into account the antenna type.

Another important issue is process variations. Due to fabrication tolerances, the parameters of the active and passive devices are scattered in a Gaussian distribution. Furthermore, temperature also shifts the parameters. UMC provides worst and best cases for their active and passive devices. Therefore, several conditions are tested as shown in Figure 4.19. Temperature is changed from 0ºC to 100ºC together with the worst case (*ss*: slow transistor meaning high threshold voltage and low leakage current), the best case (*ff*: fast transistor meaning low threshold voltage and high leakage current) and typical (*tt*) transistor parameters. The efficiency degrades with the slow transistor parameters. Therefore, other circuit blocks should be designed taking into account this degradation.

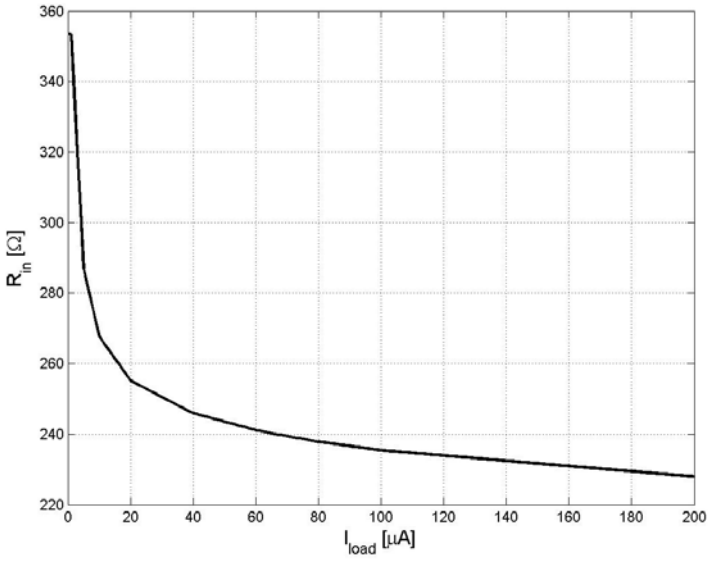


Figure 4.18: The input resistance of the 2-stage multiplier for the optimized design parameters.

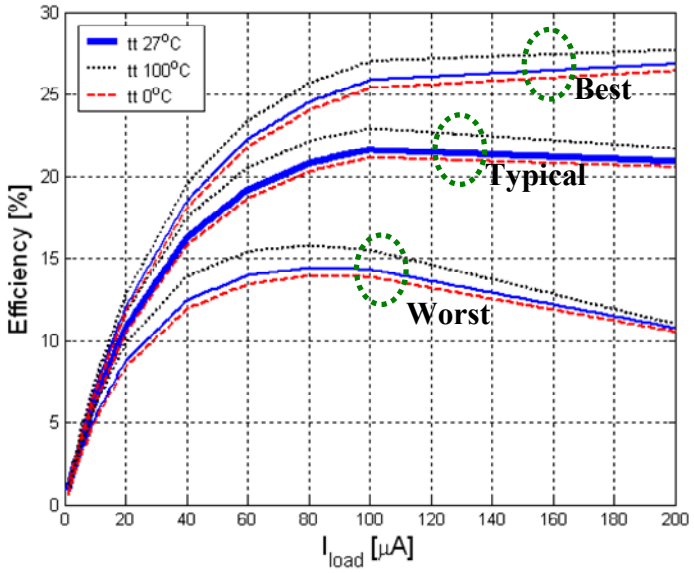


Figure 4.19: Effect of the process and temperature variations on the multiplier efficiency.

All the simulations for the 2-stage multiplier were carried out using an input voltage amplitude of 0.7V. However, as soon as the reader gets closer to the transponder, induced current through the antenna gets larger and the voltage amplitude available for the multiplier increases. The oxide thickness in UMC process is around 2nm and voltages higher than 1.3V is a limit for the oxide breakdown. Therefore, output voltage of the 2 stage multiplier should be limited. For this purpose a simple clamping circuit is used as shown in Figure 4.20. The transistor dimensions are selected to be 25µm/0.12µm. When the total voltage drops for the transistors are exceeded, clamper draws more current and the output voltage is limited. It is known for the process that voltage drops are around 0.4V at 20µA for a diode connected transistor that is 25µm/0.12µm. Considering the body effects, it seems 2 cascaded transistors that are diode connected are sufficient to clamp the output voltage.

Figure 4.21 shows the output voltage of the multiplier with the clamp. Here, input voltage is varied from 0.5V to 1.5V to see the effect of the clamper. It is obvious that the clamper successfully limits the output voltage with the price of efficiency degradation because the clamper draws current when operating.

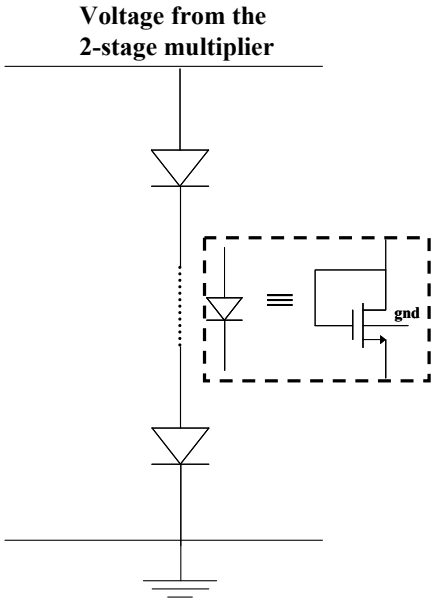


Figure 4.20: The clamping circuit representation.

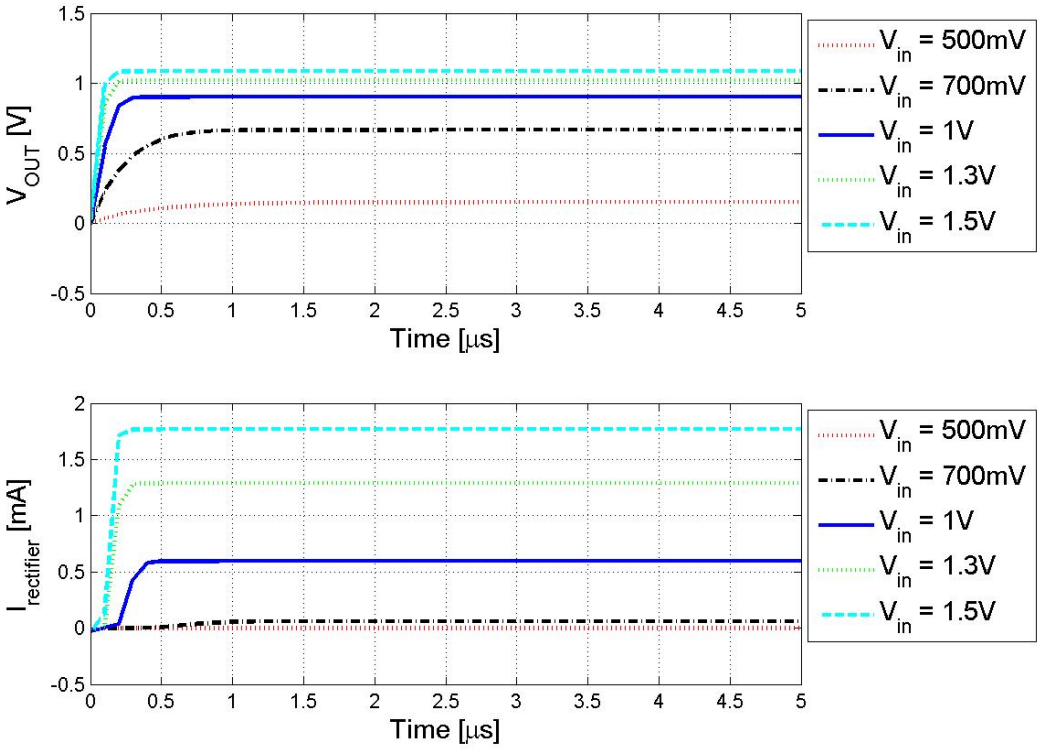


Figure 4.21: The output voltage of the 2-stage multiplier connected to the rectifier.

4.5.3 Demodulator Circuit

In this thesis work, a modified pulse-pause coding (MPPC) which greatly simplifies the clock generation is proposed. This scheme is based on short pulses as explained

in 4.3.4 but instead of changing the bit period, duration of the pulse is changed. A simple MPPC data coding is illustrated in Figure 4.22. A short pulse that is duration of Δt_1 in a period of T represents "1" and Δt_0 for "0". There is also a reset signal defined whose pulse duration is Δt_r which will be explained later.

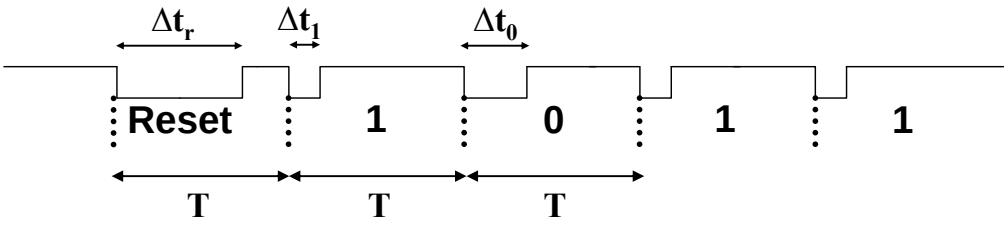


Figure 4.22: Modified pulse-pause coding (MPPC).

In order to obtain the functionality of the demodulator, a modulated signal is applied to its input, as shown in Figure 4.23. The keying signal is sequentially corresponding to reset, logic "0" and logic "1". This signal is multiplied with the carrier signal of 2.45GHz and the demodulated signal is attained.

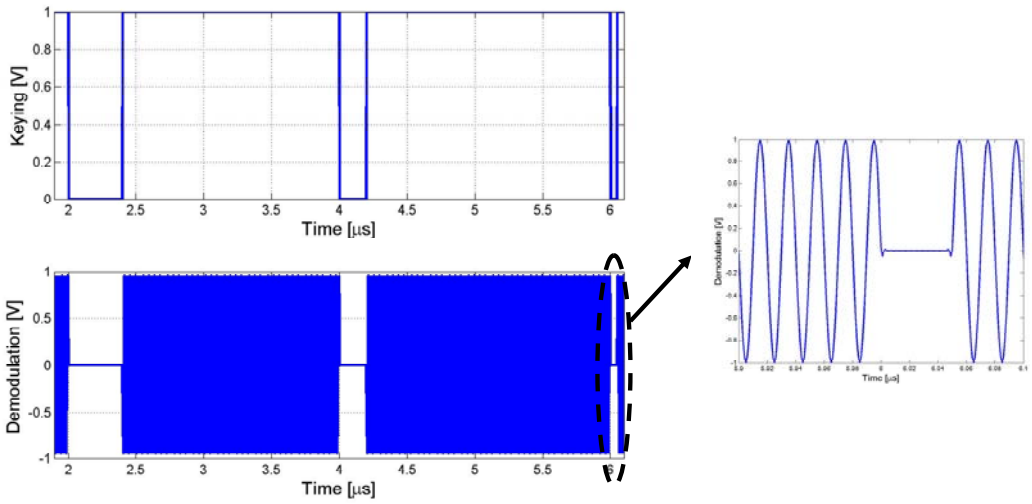


Figure 4.23: The generation of the modulated input signal. Serial inputs are reset, logic "0" and logic "1".

The basic idea behind the demodulation is to recover the data embedded into the carrier signal. It is also important to recover the data clock from the modulated data so that there will not be a need for a clock synchronization circuit in the transponder which will decrease the power consumption. In practice, the data rate is 3 or 4 orders of magnitude lower than the carrier signal frequency. In this design, 2.45GHz is

chosen for the communication. Therefore, the data rate will be on the order of 100kHz.

The demodulation circuit for MPPC is shown in Figure 4.24. Here, there are two circuit branches; V_{ref} is the reference point and V_o stands for the output voltage of the demodulator.

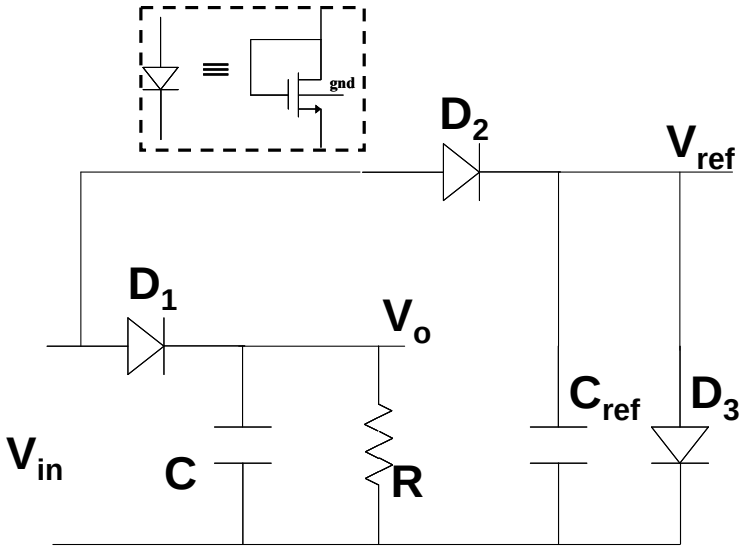


Figure 4.24: Demodulation circuit for MPPC.

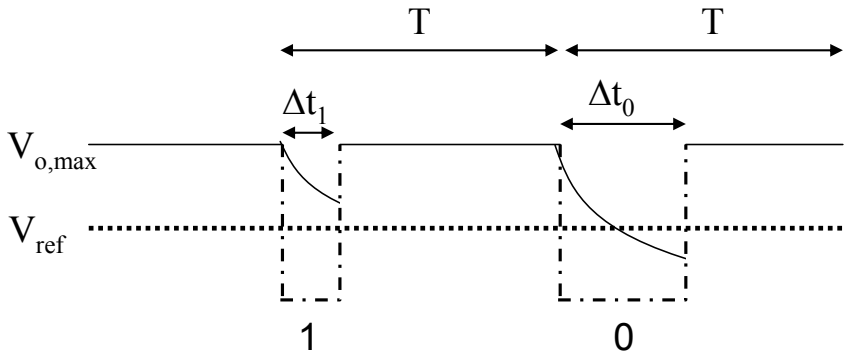


Figure 4.25: The principle of the demodulation of "1" and "0".

Diodes D_2 and D_3 together with C_{ref} generate the reference voltage level, V_{ref}. When full-power input signal comes to the input of the demodulator, V_{ref} takes its maximum output voltage that is $V_{o,max}$. However, when the carrier signal is modulated by the incoming data, then no power reaches to V_{in} and C_{ref} stores the charge determined by two diodes. This voltage level is around the mid range of 0 and $V_{o,max}$. On the other hand, D_1 and C serve as a peak detector with a leakage of R. Adjusting the time constant of RC ($\Delta t_1 < RC < \Delta t_0$), "1" and "0" can be easily

detected by using an analog comparator whose inputs are V_{ref} and V_o. An illustration for this case is shown in Figure 4.25.

The analog front-end of the demodulator is shown in Figure 4.26. There are four circuit branches yielding the following outputs: Reference voltage, V_{ref}, clock signal, V_{clk}, incoming data reconstruction, V_{data}, and the reset signal, V_{reset}. As illustrated in Figure 4.22, reset and data signals are modulated with different pause intervals. A detailed analysis of the MPPC considering the error probabilities of the coding is given in Appendix C. The analyses have shown that the ratio of the pause intervals for logic "1" and logic "0" should be around 4-5 in order to obtain a bit error rate (BER) of close to the binary coding. Here, in Figure 4.26, resistor and capacitance values are determined so that the intervals are 400ns, 200ns and 50ns for reset (Δt_r), logic "0" (Δt_0) and logic "1" (Δt_1), respectively.

The reference signal is generated with the diode-connected NMOS transistors, D_3 and D_4, whose dimensions are 2µm x 0.12µm. The capacitance, C_{ref}, is chosen to be 5pF in order to alleviate the ripples on the DC part of the reference signal. The clock signal is generated from the incoming data signal. Therefore, minimum pause interval of Δt_1 is considered as the clock signal instead of the logic "1" representation. However, the data output is used for both logic "1" and logic "0" detection. If 50ns pause arrives, then, V_{data}, cannot go below V_{ref} and this is considered as logic "1". If 200ns interval happens, V_{data} goes below V_{ref} and logic "0" is detected. In order to prevent the data and reset from being charged before the reference and clock signals, capacitances C_{data} and C_{reset} are chosen significantly larger than C_{clk} and C_{ref}. Overall dimensions are given in Table 4.3.

Table 4.3: Demodulator front-end design parameters.

D_1, D_2	2µm x 0.12µm
D_3, D_4, D_5	20µm x 0.12µm
C_{ref}, C_{clk}	5pF
C_{data}, C_{reset}	80pF
R_{clk}	10kΩ
R_{data}	2.5kΩ
R_{reset}	5kΩ

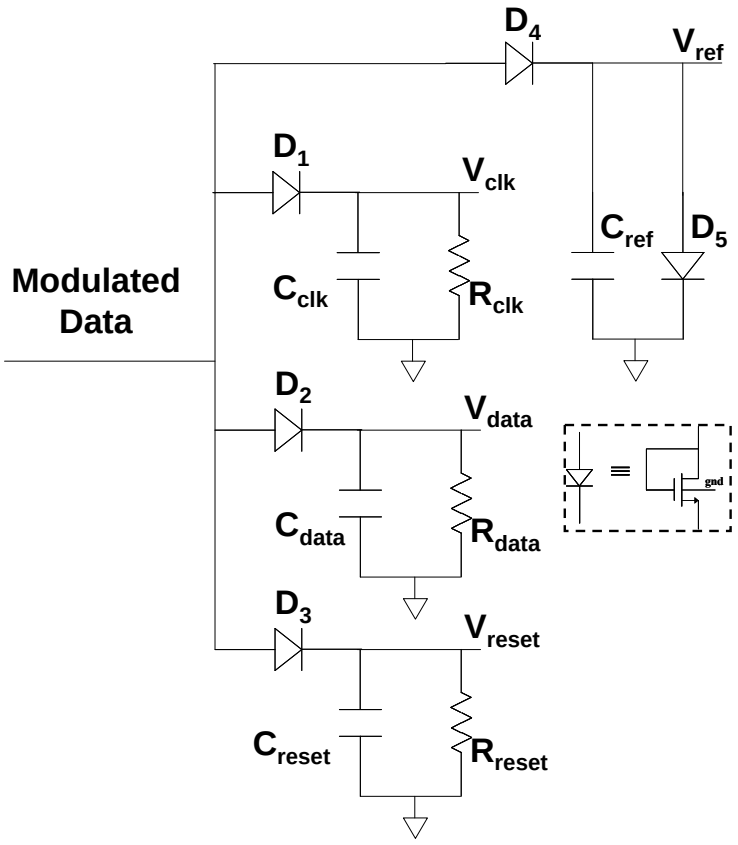


Figure 4.26: The demodulator analog front-end circuit.

The output signals of the demodulator front-end are shown in Figure 4.27. The input sequence here is reset, logic "0" and logic "1". As can be seen from Figure 4.27 that as soon as the signal is demodulated, *Clock* signal goes to low state regardless of the pause duration. However, the *Data* signal gets lower than the *Reference* signal only if the logic "0" (or reset) is detected. Those signals should be converted to digital signals in order to take the advantage of the full-scale voltage levels. On the other hand, comparator circuits are used in order to construct the *Reset* or *Data* signal. The clock is reconstructed from the *Clock* signal depicted in Figure 4.27. Because the clock signal reaches to the low state for any demodulated data, using cascaded inverters, the clock signal can be scaled to V_{DD} and ground.

The comparator circuit is shown in Figure 4.28. The circuit is based on regeneration. PMOS transistors M_{P1} and M_{P2} are cross-coupled and form a positive feedback loop. The comparator is biased with the incoming clock signal so power is consumed only if the clock signal is high. The PMOS transistors M_{P3} and M_{P4} are used to reset the comparator for the next comparison. A D-type flip-flop (DFF) is used at the output to

store the output logic value until the new comparison starts. DFF is a well-known master-slave positive edge triggered flip-flop **(Kang and Leblebici, 2003)**.

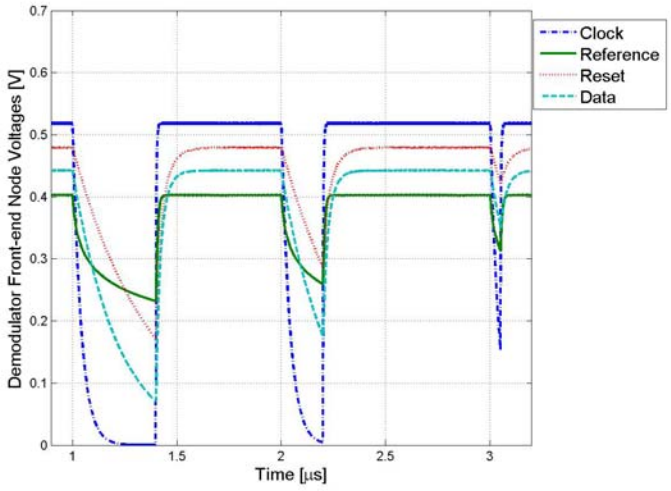


Figure 4.27: Demodulator front-end simulated output waveforms.

The operation of the circuit is as follows: When *CLK* signal is low, no current flows through M_{N3} and M_{P3} and M_{P4} pull-up the output nodes to V_{DD} which also equates the two output nodes and make them ready for the comparison. When *CLK* is high, M_{N1} starts drawing current and the input signals v_n and v_p are compared. With the aid of the positive feedback, v_o reaches its final value. If v_p is high, then v_o goes to high. This output voltage is stored as soon as the *CLK* is low. It is important to note that the clock signal of the DFF should be delayed to allow the comparator to reach its final value. Therefore, *CLK* is buffered and a delayed clock signal, CLK_d is generated.

The input and output voltages of the comparator for the data signal is shown in Figure 4.29.

It is important to note that *Data* signal is also activated with an output of the incoming reset signal. In order to prevent this issue, a two-input (one is inverted) NAND gate is used, hence, as soon as *Reset* is 1, data is not evaluated. The digital output generation from the demodulator front-end output voltages is illustrated in Figure 4.30.

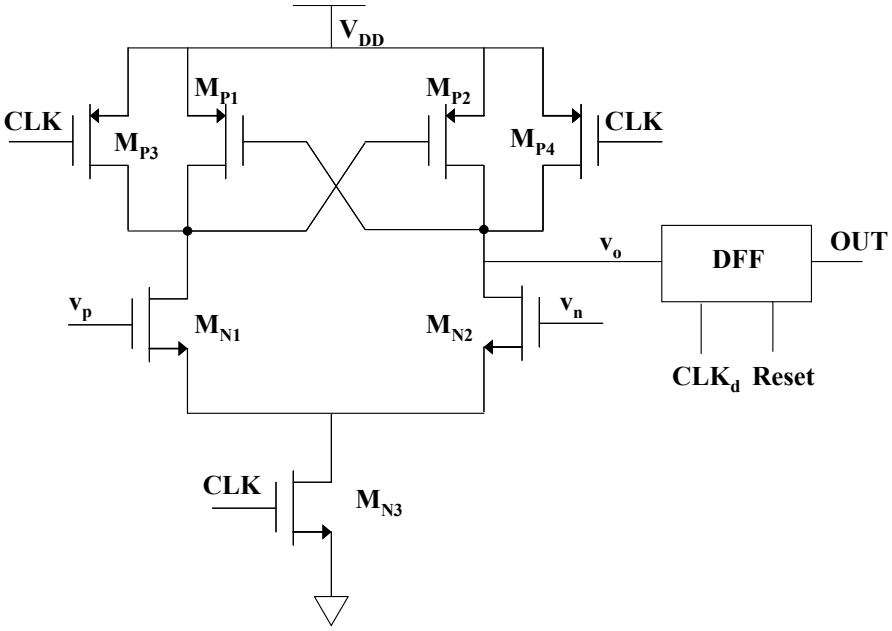


Figure 4.28: The regenerative latched comparator circuit.

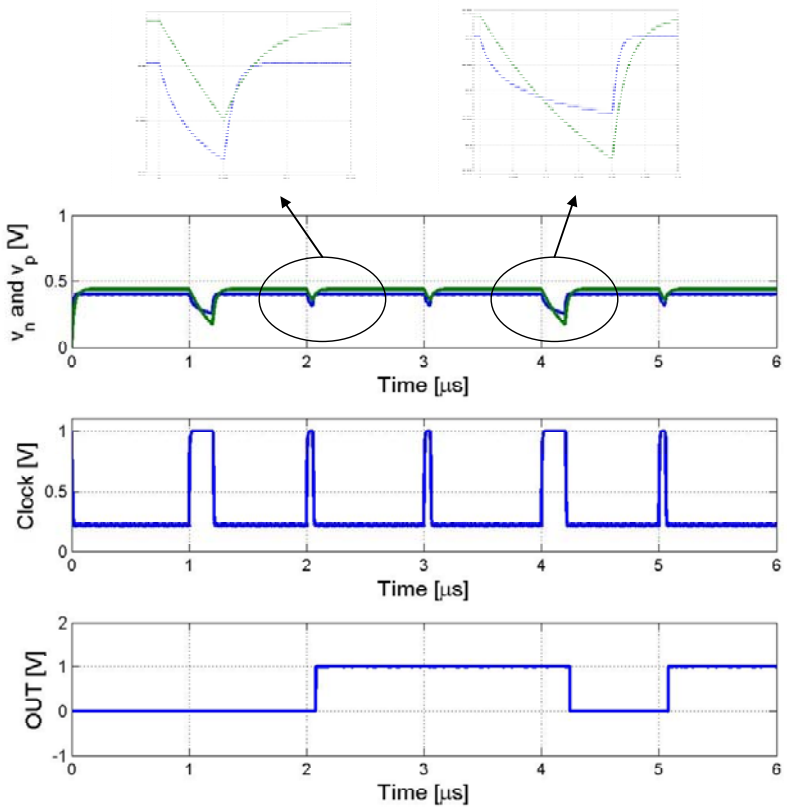


Figure 4.29: The input and output voltages of the comparator for the data signal.

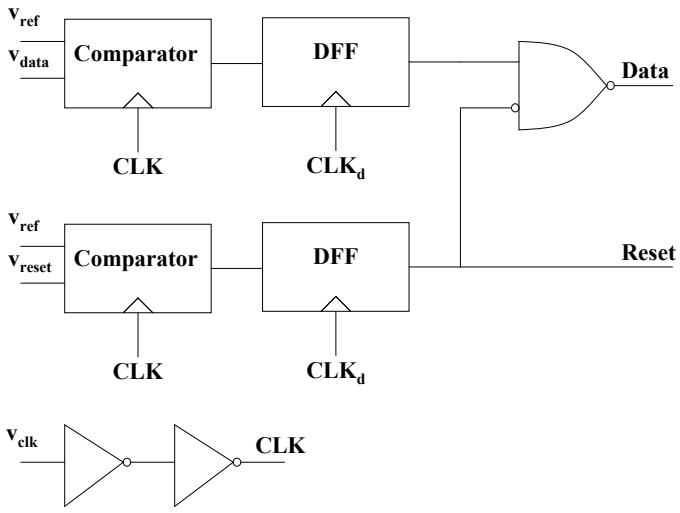


Figure 4.30: The digital output generation from the demodulator front-end output voltages.

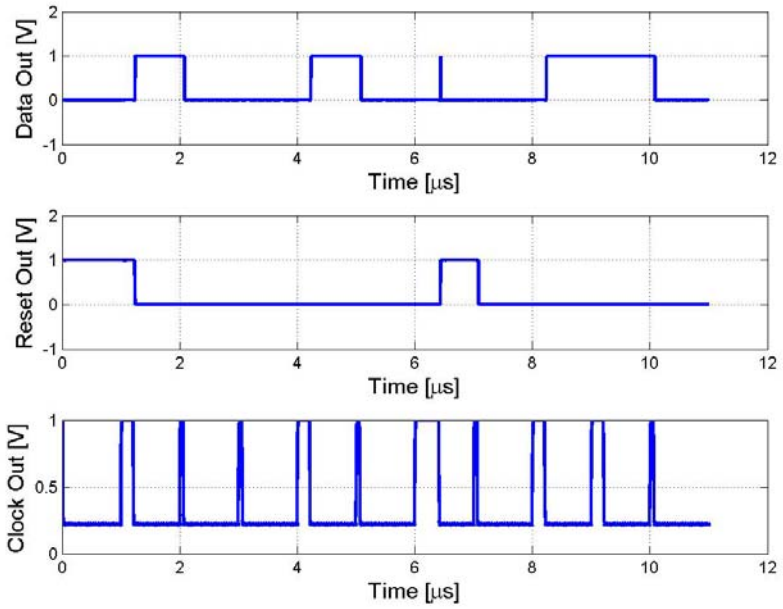


Figure 4.31: The outputs of the demodulator.

The overall demodulator is simulated as shown in Figure 4.31. The incoming data is sequentially 1-0-0-1-0-reset-0-1-1-0.

4.5.4 Control Logic

The demodulated signal is used to read or write (R/W) the data from/to a memory cell. In this design, a 64-bit MRAM block is considered. Memory block is constructed in matrix format that has 8 rows and 8 columns. Because the data

communication is serial, one memory cell can be written or read at each clock cycle. As previously mentioned, the clock signal is reconstructed from the demodulated data during write or from a local oscillator during read operation. The control logic for R/W operations is illustrated in Figure 4.32.

In order to select one memory cell, row and column select encoders are used. Each encoder has 3-bit inputs and 8-bit outputs. Only one output of each encoder is enabled at a clock cycle so that one column and one row are selected. Rows and columns are called word lines (*WL*) and bit lines (*BL*), respectively. Once a *WL* is selected, each *BL* is selected sequentially. After finishing the selected *WL*, next *WL* is selected and the operation is repeated. Therefore, most significant bits (MSB) of the counter are connected to the *WL* select encoder. In order not to select multiple word or bit lines, 1-of-n encoders are used. The truth table and a possible synthesis of the 1-of-n encoder are explained in Figure 4.33. Here, B_i (i=0,1,2) represents the encoder inputs and D_j (j=0,1,2,3,4,5,6,7) are the outputs. The resulting outputs can be implemented with simply 3 input AND gates. Each AND gate takes non-inverting (*BiP*) or inverting (*BiN*) inputs as shown in Figure 4.33.

The clock signal is the input of a 6bit counter which counts from 0 to 63 so that memory addresses are selected sequentially. The counter circuit is a simple asynchronous divider consisting of 6 DFF blocks **(Kang and Leblebici, 2003)**. Each DFF input is fed from its own inverted output where each of the non-inverted outputs is used as the clock signal for the following DFF, frequency of the input clock signal is halved at each stage, as illustrated in Figure 4.34.

The clock signal together with the outputs of the counter is shown in Figure 4.35. It can be seen from Figure 4.34 that the duty cycle of the clock signal is intentionally selected different from 50% because the clock signal constructed from the demodulator has a characteristic of different pulse widths.

Figure 4.36 shows each word line select outputs. Notice that multiple outputs are never high at the same time.

Because the bit line inputs are LSB outputs of the counter, each signal of the BL outputs will be re-enabled with the changing word line outputs. Figure 4.37 shows the bit line outputs corresponding to two consecutive word lines, WL_i and WL_{i+1}.

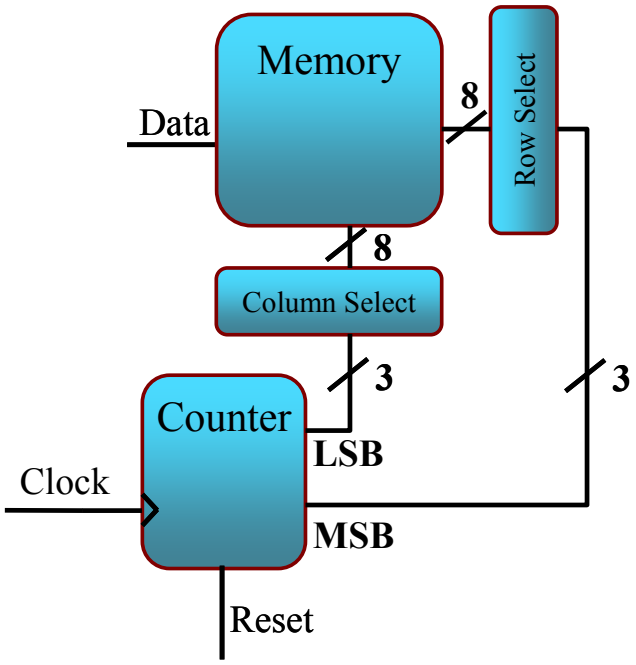


Figure 4.32: The control logic of the memory R/W.

$B_2\,B_1\,B_0$	$D_7 \ldots D_0$	
000	00000001	D0 = B0P B1P B2P
001	00000010	D1 = B0N B1P B2P
010	00000100	D2 = B0P B1N B2P
011	00001000	D3 = B0N B1N B2P
100	00010000	D4 = B0P B1P B2N
101	00100000	D5 = B0N B1P B2N
110	01000000	D6 = B0P B1N B2N
111	10000000	D7 = B0N B1N B2N

Figure 4.33: The truth table and a possible synthesis of the 1-of-8 encoder.

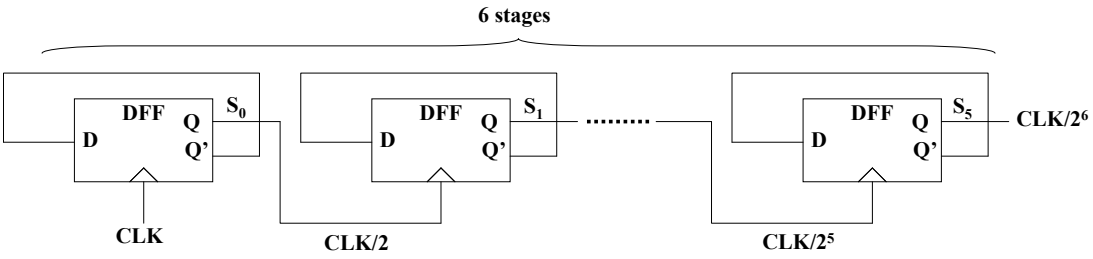


Figure 4.34: Building a counter from cascaded flip-flops.

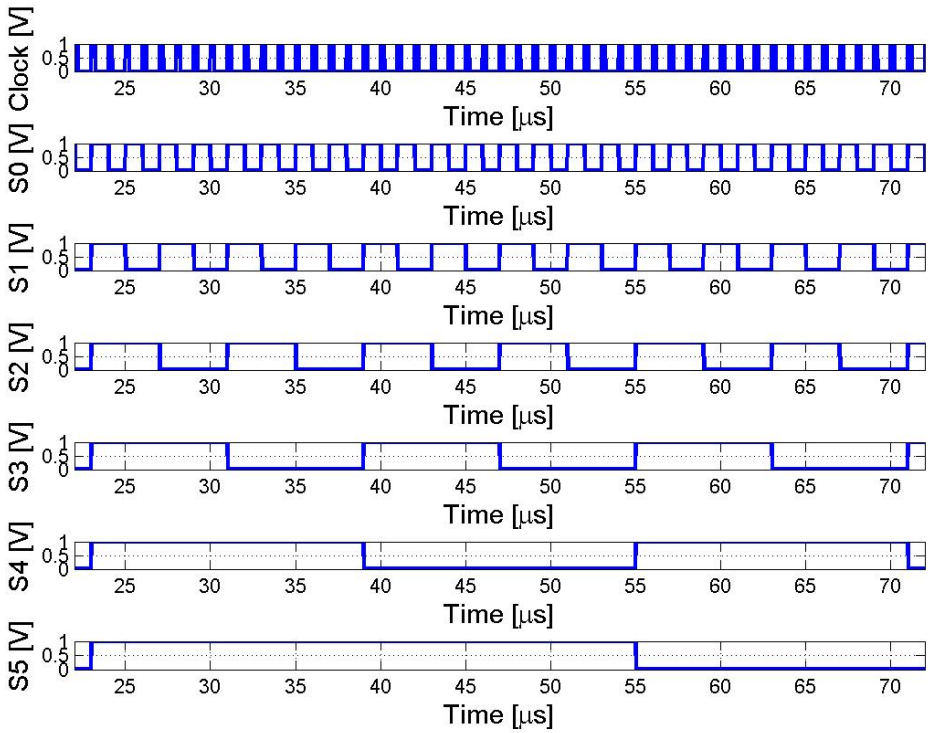


Figure 4.35: The clock signal and the outputs of the counter.

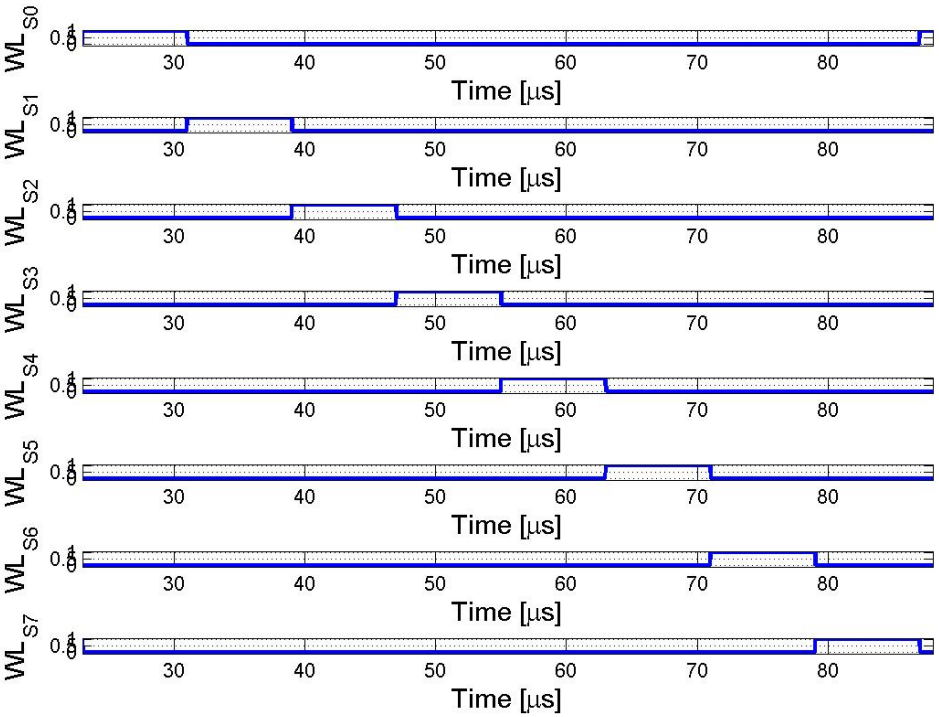


Figure 4.36: Word line select encoder outputs.

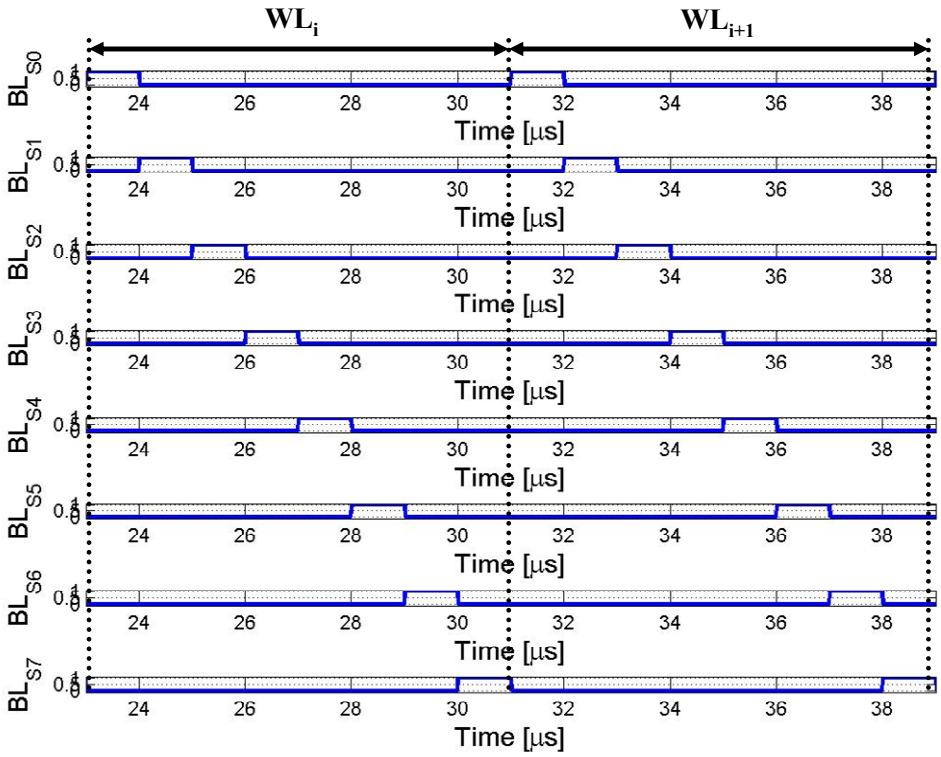


Figure 4.37: Bit line select encoder outputs.

4.5.5 64-bit MRAM

4.5.5.1 Memory Write

As previously explained, in order to write data on an individual MRAM cell, two current paths should be created; one is the word line (which is always in the same direction) and the other is the bit line, which can be parallel or anti-parallel to the word line. The circuit of the individual MRAM cell is shown in Figure 4.38. Here, the bit line is activated by the data signals, *DataP* and *DataN*, which are complementary of each other. Select signals, WL_{SP} and WL_{SN} (indices *P* and *N* mean those signals are complementary of each other), are used to activate the individual MRAM row in the memory block. After selecting a row, a column should be specified to write the data on it. The enable signal BL_{en} is used for this purpose. The other enable signal, WL_{en}, is also activated with BL_{en} to ensure simultaneous current drawing for word and bit lines. Depending on the data value, bit line current flows through path 1 or path 2.

Once the row is selected, a large amount of current will be drawn from both word and bit lines. On the other hand, as explained in Section 4.3, a 10ns pulse of current

is adequate for the MRAM to be written. Therefore, by using inverters, short pulses are generated as shown in Figure 4.39. Notice that, BL_{en} is delayed with respect to WL_{en} to ensure that the word line is de-activated before the bit line so as to avoid writing a data on another MRAM cell in the same row.

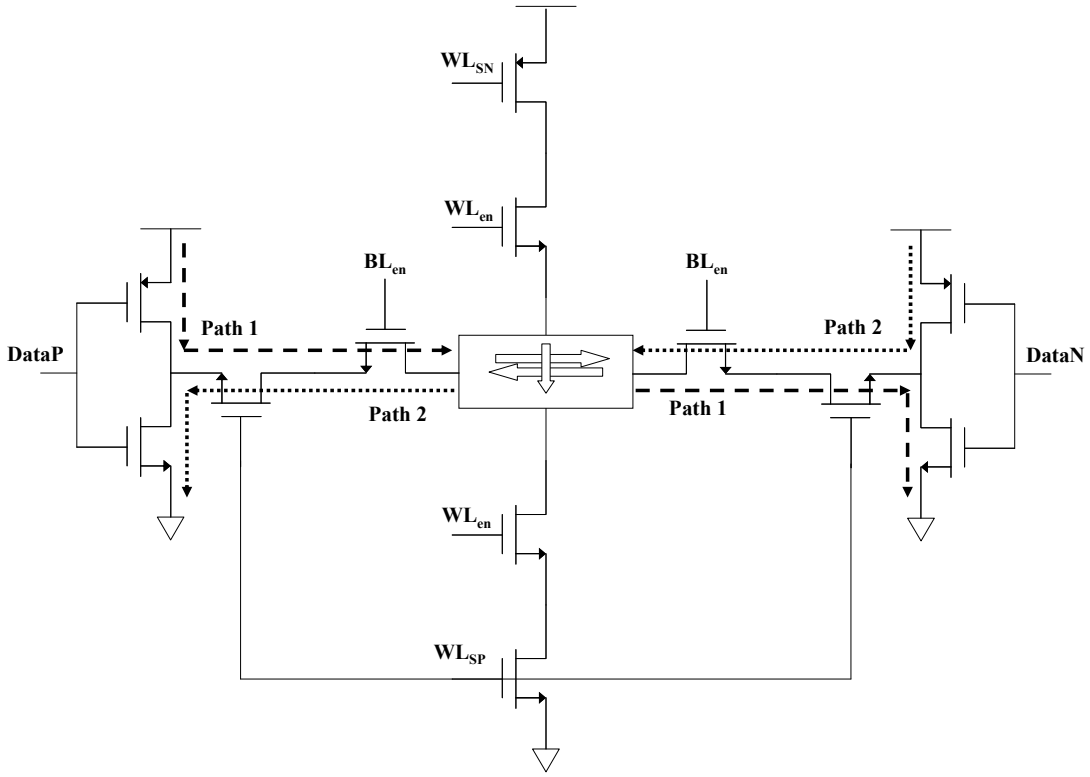


Figure 4.38: MRAM writing circuit.

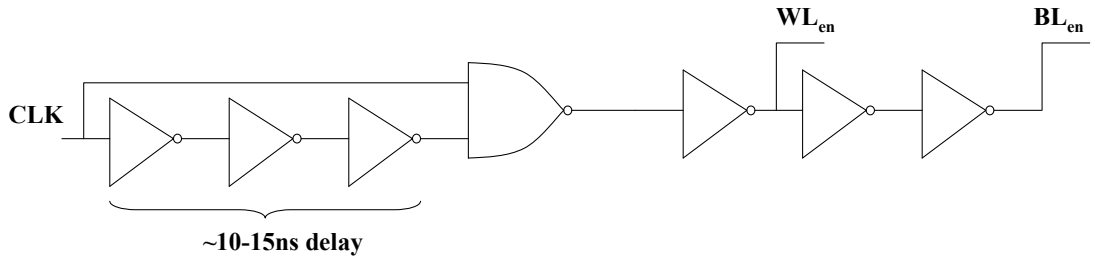


Figure 4.39: The pulse generator for the MRAM enable signals.

The simulation results for an individual MRAM cell are given in Figure 4.40. In order to show the current change on the bit line, *DataP* and *DataN* are changed and clock signal frequency is set to 10MHz. It is obvious that the pulse durations of the enable signals will not change with the clock period as soon as the half of the clock period is not shorter than 10-15ns. It can be seen from Figure 4.40 that when the data changes, the direction of the bit line current also changes while word line current remains the same.

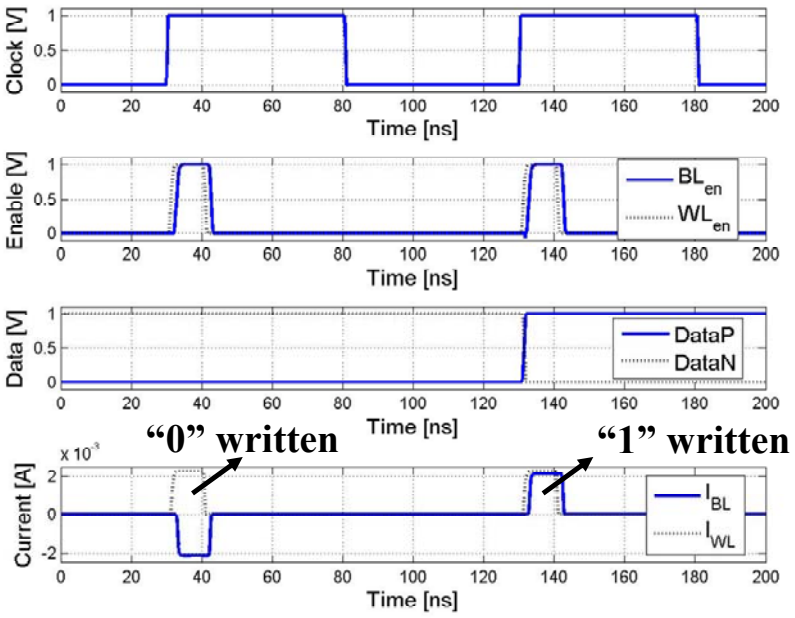


Figure 4.40: The simulation results for an individual MRAM cell.

Here, it is important to analyze the circuit performance considering worst case simulations. In section 4.3, it has been shown that 20pC (10ns of 2mA for 1V) is adequate to write a data onto an individual MRAM cell. Worst case simulations are summarized in Table 4.4. It is clear that all the worst case results are greater than or equal to 20pC.

4.5.5.2 Local Oscillator

Considering the issues discussed in 4.3.5, the ring oscillator is chosen for local oscillator design. The ring oscillator circuit is shown in Figure 4.41.

Table 4.4: Worst case simulation results.

Case (Device Parameters & temperature)	Figure of Merit [pC]
Fast [0ºC, 27 ºC, 100 ºC]	[23, 24, 23.5]
Typical [0ºC, 27 ºC, 100 ºC]	[21, 22, 21.4]
Slow [0ºC, 27 ºC, 100 ºC]	[20, 20.5, 20.2]

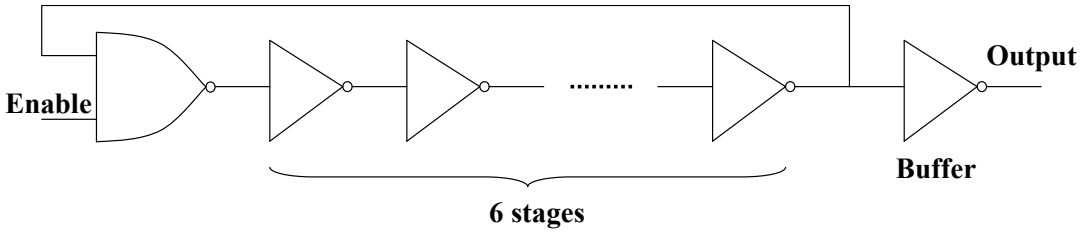


Figure 4.41: The schematic representation of the ring oscillator.

One of the inverter stages is replaced with a NAND gate where one of its inputs is used as an enable signal. When the *Enable* is "1", NAND gate simply behaves as an inverter. If the *Enable* is "0", then, NAND gate always produces an output of "1" and the circuit does not oscillate, i.e., it is disabled. If the gate length of the inverters is set to the technology minimum (0.12µm), the propagation delays of each inverter would become very low causing high frequency of oscillation with respect to 200kHz. Therefore, gate lengths are selected to be 15µm. But, in this case, the rise and fall times get larger which deforms the square wave. In order to achieve sharper rise/fall edges, a buffer inverter is used whose dimensions are 2µm/0.12µm.

The simulation result of the ring oscillator is shown in Figure 4.42. It can be seen that the circuit starts to oscillate as soon as V_{DD} switches to 1V. The oscillation output is buffered successfully. Oscillator can be disabled in order to prevent any unstability during transitions. The current while the circuit is oscillating is 2µA and almost zero while it is disabled.

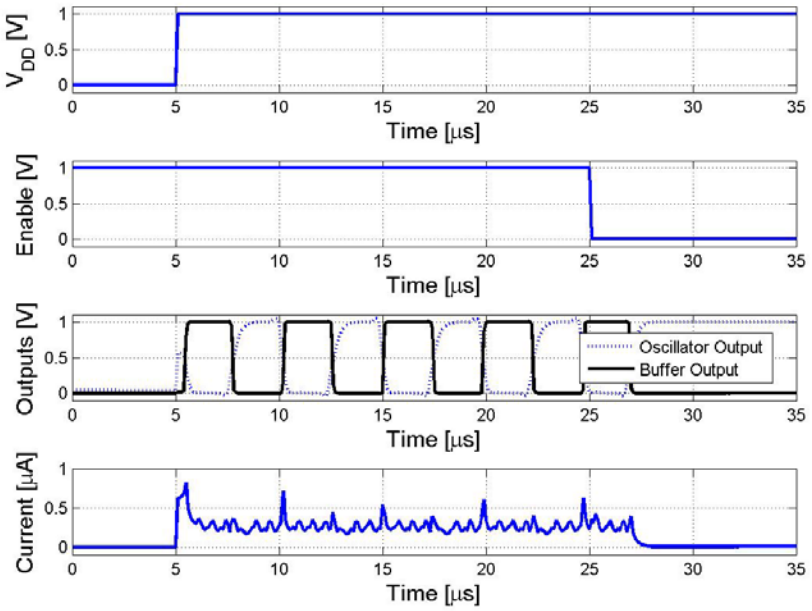


Figure 4.42: The response of the ring oscillator to the sudden V_{DD} and *enable* switchings.

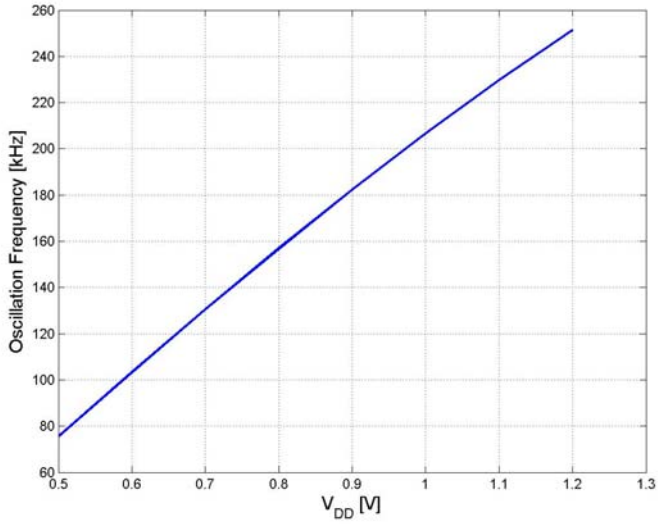


Figure 4.43: Oscillation frequency variation with the changing power supply.

The oscillation frequency dependence on V_{DD} is given in Figure 4.43. If the supply voltage variation is between 0.7V and 1.2V, 200kHz to 1.6MHz of oscillation frequency change occurs.

Furthermore, the circuit should also be analyzed considering worst cases. Same analysis is performed as done in MRAM writing circuit. Based on the different parameter selections as previously done in Table 4.4, the minimum and maximum oscillation frequencies are attained 29kHz and 2.5MHz.

4.5.5.3 Memory Read

When a read signal for the transponder is detected, stored information on MRAM memory is read sequentially. As previously described, the resistance of an individual MRAM cell changes depending on its data. To read the bit value on the memory unit, a reference cell is used **(Gallagher and Parkin, 2006)**. The idea is to use 2 reference MRAM cells; one's data is "1" and other's is "0". In order to do this, a simple layout is shown in Figure 4.44. Here, the direction of the current is determined by the data to be written onto the individual data cell. Reference cells, therefore, store "1" and "0".

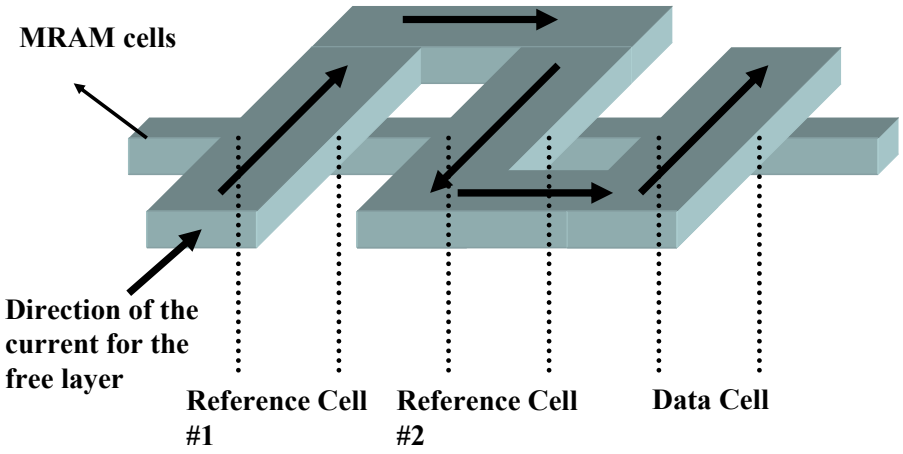


Figure 4.44: The concept of reading an individual MRAM cell.

The sense circuit is shown in Figure 4.45. Reference cells are represented by the resistors, R_0 and R_1 and the data cell is represented by the resistor R_{data}. When the cell is activated (*Enable*, *RWL* and *BL* are set to "1") a bias current flows from the each branch. However, because the reference cell branches are shorted, the voltage at this node is proportional to a resistance value which is between R_0 and R_1. This voltage is compared with the voltage that is proportional to R_{data}.

The comparator circuit is based on Figure 4.28 but PMOS transistors are used as the input transistors. The reference resistors R_0 and R_1 are set to 5kΩ and 10kΩ, respectively for the simulations. Each word line is composed of 8 data lines sharing

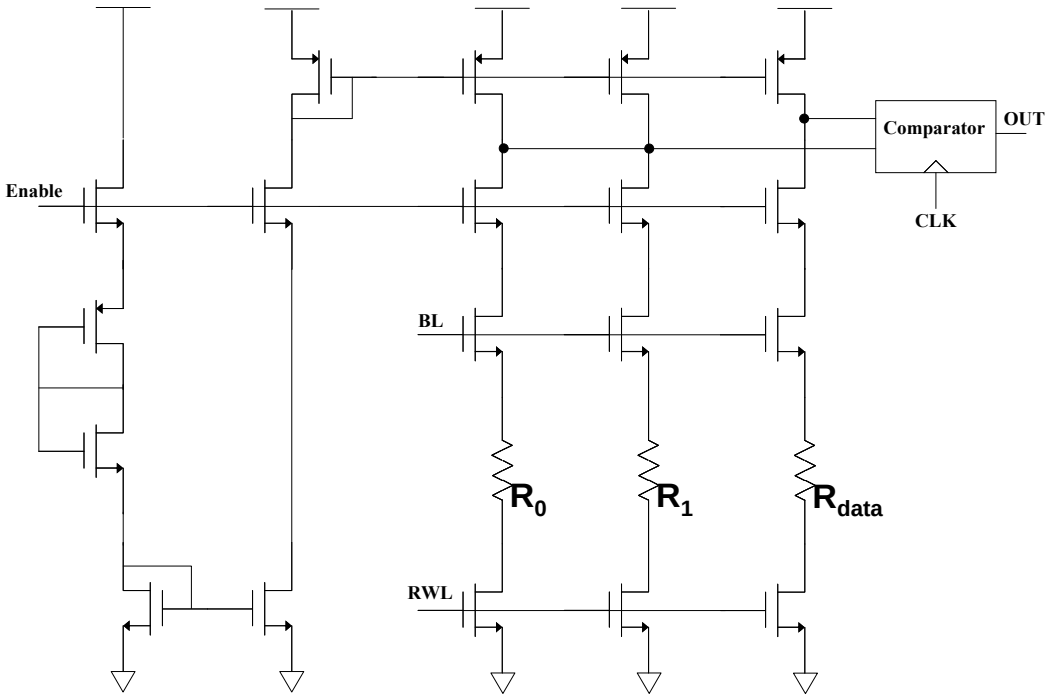


Figure 4.45: The MRAM reading circuitry.

the same reference cells. The memory read block is same as the write block. The column and row selects are generated from the counter but its clock signal is taken from the local oscillator. When the transponder is in write mode, read circuitries are disabled by the *Enable* signal.

4.5.5.4 Memory Read/Write Select

The transponder should be able to detect which operation is performed. Therefore, a coding sequence should be defined for read and write operations. For this purpose, first data after the reset is reserved for R/W selection. If the data is "1", memory is read and otherwise memory is written. In order to realize this operation, a multiplexer is used as shown in Figure 4.46.

The reset signal is stored for one clock cycle in order to synchronize its value with the following data. The sample simulation is shown in Figure 4.47.

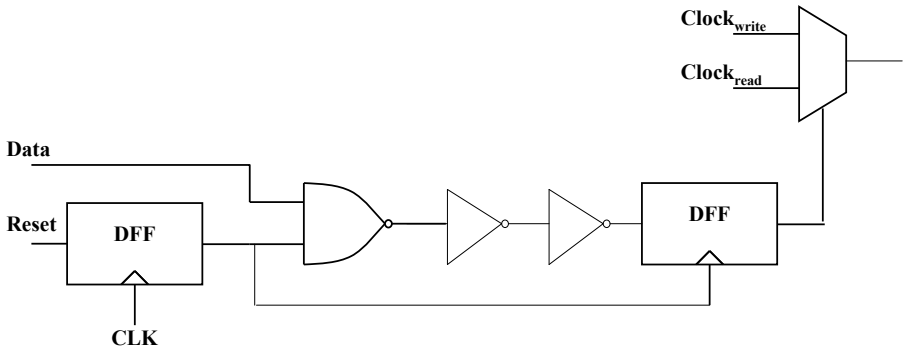


Figure 4.46: The schematic representation of the read/write select.

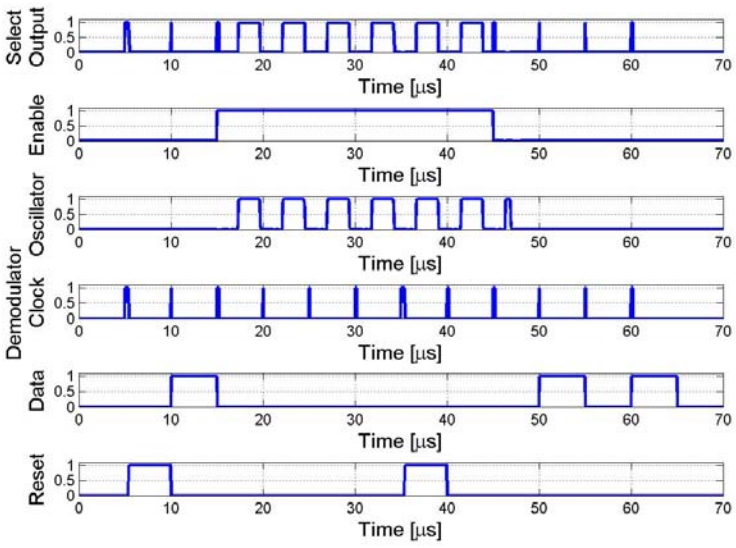


Figure 4.47: The read/write selection procedure.

4.5.6 Power Budget for the Online Mode of "Smart RFID"

In order to analyze the power budget of "smart RFID" while it is working online, i.e., as transmission happening, the power available to the system should first be determined. As explained in the Section 4.3.2, 400μW of power is available for a transponder whose 4W reader is 1 meter away that is operating at 2.45GHz. The power signal from the reader is detected by the antenna, then, it is multiplied and rectified. Figure 4.19 shows that the average power efficiency of the multiplier is 20% for current levels of around 100μW. Therefore, the power available to the RFID circuitries is decreased to 80μW.

As depicted in the Section 4.3.3, the storage capacitance should be chosen properly considering the tolerable voltage drop on the V_{DD} signal. Assuming the nominal voltage of V_{DD} is 1V and tolerable voltage drop is 0.3V, storage capacitance is set to 200pF taking into account the current levels for each transmission mode.

There are basically two transmission modes: read and write. During read mode, demodulator, local oscillator, control logic and memory read circuits operate and consume 75μA of current. This current is drawn when the power signal is not received because the modulation is based on power cuts. Considering the longest power cut is 800ns, which is for reset signal, the resulting voltage drop is 0.3V. When the write mode is active, then, memory bits are written. In this case, 5mA of current is drawn for duration of 10ns is needed to write a memory bit, which results 0.28V of voltage drop.

The data is sent by the reader with a time intervals of 5μs. Except the power cuts, the power signal is used to charge the storage capacitor. This mode can be called standby and 5μA current is needed, which is used for demodulator, local oscillator and other biasing circuits. The voltage drop for this mode would be 0.13V, however, because the power available to the circuits are large enough, this voltage drop will not happen.

5. CONCLUSION and FUTURE WORK

In this thesis, a novel, vibration based micro energy harvester system has been proposed. The modeling, design and fabrication of the system devices have been carried out. Firstly, the most important result was to achieve high power density levels with a mm^3 device by using a novel vibration based mechanical structure. Secondly, a wireless communication scheme based on the well-known RFID technology has been combined into the power harvester system as a first time.

This is the first attempt to use a nonlinear approach in power harvesters. In order to increase the power density; mechanical structure is allowed to move in large amplitudes, thus working in nonlinear regime. Thanks to the large deformation, power can be collected from stretching instead of bending, which gives higher energy levels. Furthermore, there is no need for the system to operate at the resonance frequency (on the order of kHz, whereas ambient vibrations are up to 200Hz) which enables the system to find wider spectrum of usage.

Mechanical modeling and simulations by COMSOL™ and SIMULINK™ have shown that the corresponding power density is $0.3\mu W/mm^3$, or $0.3mW/cm^3$ for the initial prototype device dimensions yielding a volume of about $6mm^3$. Each tether is 3.5mm long, 100μm wide and 5μm thick whereas the proof mass is 2.5mm by 2.5mm in surface and 500μm thick. The power density is limited with the fracture strength of the piezoelectric material, which is 50MPa.

Mechanical part of the device has been fabricated using standard MEMS processes such as bulk micromachining and photolithography. Silicon has been used as the substrate material. All the processes have been carried out taking into account that they are CMOS compatible. The packaging has been embedded into the fabrication process, which reduces the handling issues during the process. PDMS has been used for packaging. The proposed packaging method of the device is very simple and easy to realize. The problems encountered and solutions to come up during the fabrication have been discussed in detail.

The “smart sand” serves as a typical accelerometer which senses the continuous vibrations or sudden accelerations. In order to further develop the sensor capabilities of the system, a new approach has been proposed: the “smart RFID” platform where the device has been combined with the RFID concept. In this context, the methods with which the RFID concept can be used in the proposed system has been investigated in detail and an RFID transponder has been designed. UMC 0.13µm CMOS process has been utilized and CADENCE™ has been used during the simulations.

The circuitry has the capabilities of sending and receiving 64 bits of data. The 64-bit memory has been constructed with magnetic random access memory (MRAM) cells. Few bits have been reserved for the acceleration or temperature data. When a sudden or continuous acceleration happen, the “smart sand” generates voltage and this voltage can be used to write the memory bits without the need of a battery. Therefore, the “smart RFID” platform behaves like a batteryless active RFID transponder. In order to determine whether adequate voltage levels are reached, a mechanical switch has been proposed and its design has been investigated.

Several applications have been proposed in order to illustrate the usefulness of the proposed system; such as continuous acceleration monitoring in package delivery, self-powered sensors for homeland security, temperature monitoring of the perishable food item delivery and a batteryless heart rate sensor. The feasibility of each application has been investigated and discussed.

As a summary, the contributions in this thesis can be listed as below:

- The power density of a vibration based power harvester system has been enhanced at least an order of magnitude thanks to the operation in the nonlinear regime,
- The proposed architecture does not need any frequency tuning and operating at the resonance is not necessary,
- A novel packaging scheme using PDMS has been proposed,
- A new batteryless active RFID transponder, called “smart RFID”, has been proposed.

The recommendations of the future works can be listed as below:

- The mechanical switch has been investigated in detail in this thesis. Its fabrication method is trivial and not included in this thesis. It would be beneficial to fabricate and characterize its performance.
- Mechanical structure fabrication and the design of the RFID transponder have been carried out separately. Integration of the antenna, circuitry and external capacitance with the mechanical structure will be a good work for another thesis.
- Each application proposed in this thesis would be excellent development projects for the “smart sand” and/or “smart RFID” systems.

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APPENDIX A: BULK ETCHANTS

Table A. 1: Comparison of example bulk Silicon etchants is given below, adapted from Kovacs et al., (1998).

	HNA ($HF+HNO_3$ +Acedic Acid)	Alkali-OH	EDP (ethylene diamine pyrochat-echol)	TMAH (tetramethyl-ammonium hydroxide	XeF_2	SF_6 Plasma	DRIE (Deep Reactive Ion Etch)
Etch Type	wet	wet	wet	wet	dry[1]	dry	dry
Anisotropic?	no	yes	yes	yes	no	varies	yes
Availability	common	common	moderate	moderate	limited	common	limited
Si Etch Rate μm/min	1 to 3	1 to 2	0.02 to 1	≈ 1	1 to 3	≈ 1	> 1
Si Roughness	low	low	low	variable[2]	high[3]	variable	low
Nitride Etch	low	low	low	1 to 10 nm/min	?	low	Low
Oxide Etch	10 to 30 nm/min	1 to 10 nm/min	1 to 80 nm/min	≈ 1 nm/min	low	low	Low
Al Selective	no	no	no[4]	yes[5]	yes	yes	Yes
Au Selective	likely	yes	yes	yes	yes	yes	yes
p++ Etch Stop?	no (n slows)	yes	yes	yes	no	no (some dopant effects)	no
Electrochemical Stop?	?	yes	yes	yes	no	no	no
CMOS Compatible?[6]	no	no	yes	yes	yes	yes	Yes
Cost[7]	low	low	moderate	moderate	moderate	high	high
Disposal	low	easy	difficult	moderate	N/A	N/A	N/A
Safety	moderate	moderate	low	high	moderate?	high	high

[1] Sublimation from solid surface.

[2] Varies with wt% TMAH, can be controlled to yield very low roughness.

[3] Addition of Xe to vary stoichiometry in F or Br etch systems can yield optically smooth surfaces.

[4] Some formulations do not attack Al, but are not common.

[5] With added Si, polysilicic acid or pH control.

[6] Defined as 1) allowing wafer to be immersed directly with no special measures and 2) no alkali ions.

[7] Includes cost of equipment.

APPENDIX B: RECIPES

1. RCA wafer Clean

- 3min Acetone in agitation
- 1min DI water rinse
- 1min Methanol in agitation
- 2min DI water rinse
- 30sec BOE (Buffered Oxide Etch) soak
- 3min DI water rinse
- Nitrogen blow dry

2. Hard Mask for KOH

PECVD oxide and nitride deposition:

- 1μm oxide: 400ºC, 5min, Nitrogen, Nitrous Oxide and Silane
- 300nm nitride: 400ºC, 5min, Nitrogen, Ammonia, and Silane

Hard Mask Pattern:

Back side photoresist pattern:

- Shipley SPR 220-7 spin: 10sec@500rpm, 40sec@2000rpm (7μm)
- Pre-bake: 3min@110ºC on hot plate
- Exposure: EVG Mask Aligner, exposure energy: 400mJ/cm^2
- Hold time: 30min wait in order to allow photoresist settled
- Post-bake: 3min@110ºC on hot plate
- Developing: 2min in Shipley Microposit developer MF 453

Front side photoresist coat:

- Shipley SPR 220-7 spin: 10sec@500rpm, 40sec@2000rpm (7μm)

- Pre-bake: 3min@110ºC on hot plate (on support glass slides in order wafers not to touch to the hot plate because back side has also photoresist)
- Hard bake: 5min@110ºC on hot plate (on support glass slides)

Oxide/Nitride etch:

- 6:1 BOE (Buffered Oxide Etch) for 20min
- Soak in DI water

3. Protek coating

Protek Prime Coating:

- 60sec@1500rpm (5000rpm/sec)
- 60sec@160ºC on hot plate

Protek Base (B1-25) Coating:

- 90sec@2000rpm (5000rpm/sec) results 6μm thick film.
- 2min@110ºC on hot plate
- 2min@160ºC on hot plate
- 1min@205ºC on hot plate

4. PDMS pattern on glass slide

- Mix 1:10 curing agent: base of Sylgard 184 PDMS (Poly-dimethyl-siloxane) for 2min
- Pour 2 droplets of TMCS on 2inch x 3inch glass slides and wait 10min for evaporation
- Spin PDMS solution onto the glass slide: 15sec@500rpm, 30sec@1000rpm (60μm)
- Bake for 5min@110ºC on hot plate
- Repeat spin and bake processes 3 times to reach 200μm thick PDMS
- Final bake: 1hour@110ºC on hot plate
- Cut a 1cm x 1cm square piece of PDMS from the glass slide with a razor and remove it out

5. Front Side Pattern

Front side photoresist pattern:

- Shipley S1813 spin: 45sec@4000rpm (1μm)
- Pre-bake: 3min@110ºC on hot plate
- Exposure: EVG Mask Aligner, exposure energy: 50mJ/cm^2
- Post-bake: 3min@110ºC on hot plate
- Developing: 45sec in Shipley Microposit developer MF 312 (1:1 with DI)

RIE Silicon etch:

- 25sccm SF_6
- 200W
- 200mTorr
- Etch rate: 0.3μm/min ~20min needed

Photoresist strip with RIE

- 10sccm O_2
- 100W
- 100mTorr
- Strip rate: 0.1μm/min ~10min needed

6. PZT deposition:

- Thermal oxidation of wafers, 1hour@1000ºC (~400nm of oxide)
- ZrO_2 deposition using e-beam evaporator
- Sol-gel (Mitsubishi Materials F2 solution) PZT spin: 3sec@500rpm, 1min@1000rpm (250nm)
- Drying: 5min@90ºC
- Pyrolsis: 1min@370ºC
- Repeat the steps spin/drying/pyrolsis to reach the desired thickness
- Annealing: 15min@700ºC with oxygen flow

7. Lift-off process of the PZT electrodes:

LOR deposition:

- Microchem LOR10A spin: 45sec@3500rpm (700-800nm)
- Bake: 10min@170ºC on hot plate

Photoresist+LOR pattern:

- Shipley S1813 spin: 45sec@3500rpm (800nm)
- Pre-bake: 3min@90ºC on hot plate
- Exposure: EVG Mask Aligner, exposure energy: 20mJ/cm^2
- Developing: 45sec in Shipley Microposit developer MF 312 (1:1 with DI) + 30sec for LOR

Metal Deposition:

- E-beam evaporator, pressure less than 1μTorr
- 50nm titanium
- 150nm platinum

Photoresist+LOR removal:

- Microposit Remover PG (NMP): 2hours@60ºC

APPENDIX C: MPPC ANALYSIS

In order to analyze the efficiency of a coding scheme, probability of the error should be investigated. For this purpose, firstly NRZ coding is discussed and compared with the MPPC.

The signal s_0 denotes the data of "0" received from the demodulator and s_1 is for "1". If an additive white Gaussian Noise (AWGN) which has zero mean and variance of $N_0/2$ (the unit is W/Hz) is added on both s_0 and s_1, the power density functions for the signals become as shown in Figure C.1.

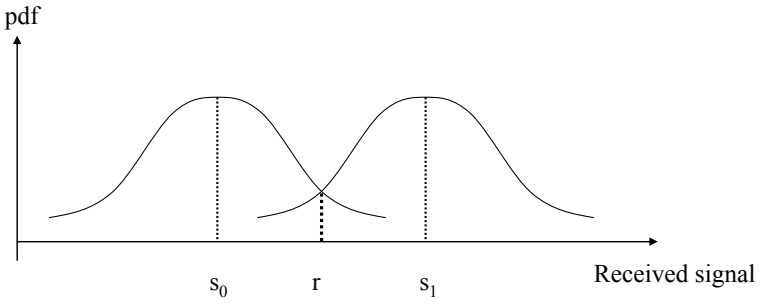

Figure C.1: Probability density functions (pdf) of two received signals for "1" and "0" from the demodulator.

Here, r is the threshold between the code transitions, i.e., the error boundary. If a received signal is smaller than the threshold, then, the signal is counted as s_0 and s_1 if the signal is bigger than r.

Now, considering NRZ coding in Figure 4.6a, s_0 and s_1 are equal to 0 and A, respectively. On the other hand, threshold is put in the middle of the two signals, i.e., A/2. The probability of the error where s_1 is transmitted but s_0 is received can be simply shown as:

$$P(e \mid s_1) = \frac{1}{\sqrt{\pi N_0}} \int_{-\infty}^{r} e^{-(r-A)^2 / N_0} dr \qquad \textbf{(C.1)}$$

Using variable exchange;

$$x = \sqrt{\frac{2}{N_0}}(r - A) \tag{C.2}$$

$$\frac{x^2}{2} = \frac{(r - A)^2}{N_0} \tag{C.3}$$

$$dx = \sqrt{\frac{2}{N_0}}dr \tag{C.4}$$

and using the assumption of $r = A/2$;

$$x = -\sqrt{\frac{A^2}{2N_0}} \tag{C.5}$$

Putting (C.3), (C.4) and (C.5) into (C.1) yields

$$P(e \mid s_1) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{-\sqrt{\frac{A^2}{2N_0}}} e^{-x^2/2}\,dx = \frac{1}{\sqrt{2\pi}} \int_{\sqrt{\frac{A^2}{2N_0}}}^{\infty} e^{-x^2/2}\,dx \tag{C.6}$$

This result can be expressed in terms of Q function or complementary error function, *erfc*.

$$P(e \mid s_1) = Q\left(\frac{A}{\sqrt{2N_0}}\right) = \frac{1}{2}erfc\left(\frac{A}{\sqrt{4N_0}}\right) \tag{C.7}$$

The overall probability of the error, *P(e)*, is the average of the individual probability of the errors of s_0, *P(e|s1)*, and s_1, *P(e|s1)*.

$$P(e) = \frac{P(e \mid s_0) + P(e \mid s_1)}{2} \tag{C.8}$$

Assuming the modulated data is equally distributed (the numbers of zeros and ones are equal),

$$P(e \mid s_1) = P(e \mid s_0) \tag{C.9}$$

Then, (C.8) becomes:

$$P(e) = \frac{1}{2}erfc\left(\frac{A}{\sqrt{4N_0}}\right) \tag{C.10}$$

Now, same analysis will be carried out for MPPC coding. Different from NRZ, s_0 and s_1 should be defined as exponentially drop functions, as illustrated in Figure 4.24:

$$s_1 = Ae^{-\Delta t_1 / RC} \quad \textbf{(C.11)}$$

$$s_0 = Ae^{-\Delta t_0 / RC} \quad \textbf{(C.12)}$$

The threshold is chosen to be the same as NRZ, which is $A/2$. The time constants are related to each other with a constant multiplicand, n:

$$\Delta t_0 = n\Delta t_1 \quad \textbf{(C.13)}$$

Assuming incoming energy is sufficiently high to charge V_o, charging time Δt_c is small enough so that

$$T - \Delta t_0 >> \Delta t_c \quad \textbf{(C.14)}$$

On the other hand, it should be noted that, the pause intervals are only a small portion of the period:

$$\Delta t_1 = \frac{T}{m} \quad \textbf{(C.15)}$$

Using the same analysis method that is used for NRZ, probability of the errors can be found as below:

$$P(e \mid s_1) = \frac{1}{2} erfc\left(\frac{A}{\sqrt{4N_0}} e^{-\Delta t_1 / RC} \right) \quad \textbf{(C.16)}$$

$$P(e \mid s_0) = \frac{1}{2} erfc\left(\frac{A}{\sqrt{4N_0}} e^{-\Delta t_0 / RC} \right) \quad \textbf{(C.17)}$$

Using (C.8), (C.16) and (C.17) together with (C.13) and (C.15) yields:

$$P(e) = \frac{1}{4}\left(erfc\left(\frac{A}{\sqrt{4N_0}} e^{-T / mRC} \right) + erfc\left(\frac{A}{\sqrt{4N_0}} e^{-nT / mRC} \right) \right) \quad \textbf{(C.18)}$$

The output voltages of the demodulator at Δt_1 and Δt_0 can be defined as αA and βA where α is between 0.5 and 1 and β is between 0 and 0.5, as shown in Figure C.2.

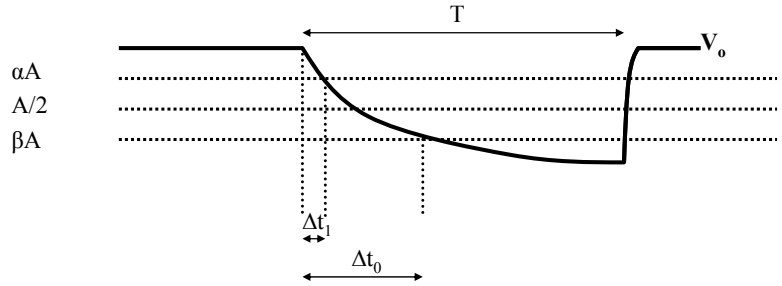

Figure C.2: Zoomed view of the discharged output voltage of the demodulator.

Using these definitions;

$$t = 0 \Rightarrow V_o = A \tag{C.19}$$

and,

$$t = \Delta t_1 \Rightarrow V_o = Ae^{-\Delta t_1 / RC} = \alpha A \tag{C.20}$$

$$t = \Delta t_0 \Rightarrow V_o = Ae^{-\Delta t_0 / RC} = \beta A \tag{C.21}$$

can be attained. Using (C.20) and (C.20), the definition, *n* in (C.13) can be rewritten as:

$$n = \frac{\Delta t_0}{\Delta t_1} = \frac{\ln \beta}{\ln \alpha} \tag{C.22}$$

Assuming the time intervals are equal with respect to the reference point, the variation of *n* with the parameters α and β is given in Table C.1.

Table C.1: Different *n* ratios with respect to the different time constants for logic "1" and logic "0".

α	0.9	0.8	0.75	0.7	0.6	0.55	$\rightarrow 0.5^+$
β	0.1	0.2	0.25	0.3	0.4	0.45	$\rightarrow 0.5^-$
n	21.8	7.2	4.8	3.4	1.8	1.33	$\rightarrow 1^+$

The probability of errors for NRZ based on (C.16) and MPPC based on (C.29) are plotted in Figure C.3. In order to see the effect of the *n* ratio on MPPC performance, different *n* ratios are plotted.

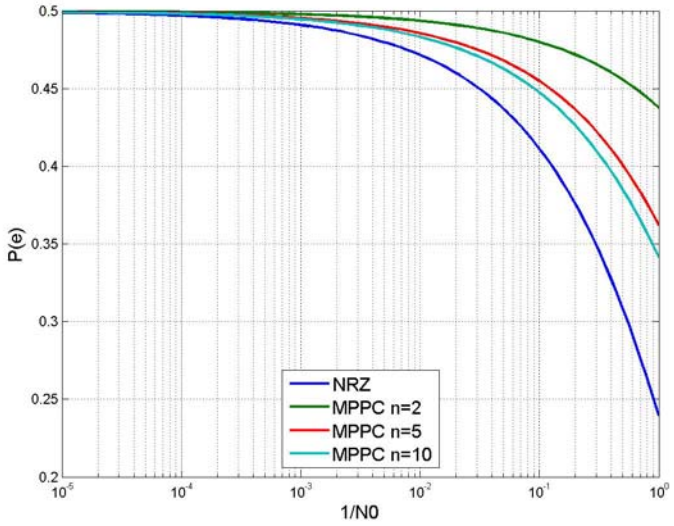

Figure C.3: The probability of errors for NRZ and MPPC with different *n* ratios.

It can easily be seen from Figure C.3 that increasing n yields better error performance for MPPC that approximates to NRZ. If α and β are selected 0.75 and 0.25, respectively, then, Δt_0 should be selected 4.8 times larger than Δt_0.

CURRICULUM VITAE

Tolga Kaya was born in Edirne, TURKEY in 1977. He graduated from Kabatas Erkek High School in 1994. In 1999, he received his B.Sc. degree in Electronics and Communication Engineering from Istanbul Technical University. He obtained his M.Sc. degree in Electronics Engineering from Istanbul Technical University on the design of analog-to-digital converters based on current-mode algorithmic techniques. He has been working as a research and teaching assistant at the Electronics and Communication Engineering Department of Istanbul Technical University since 1999. He worked as a visiting assistant in research at Yale University in 2005 on MEMS modeling and fabrication. He worked as a senior design engineer at MICROELECTRONICS R&D Inc. ETA-IC DESIGN CENTER between 1999 and 2006. He got the SIEMENS Excellence Award, "Best MS Study" with his MS Thesis in 2002. He obtained 6 months scholarship from The Scientific and Technological Research Council of Turkey to do research at Yale University. He has one journal and 5 conference papers. He took an efficient role on supervision of more than 20 senior and several master projects. His research interests include ASIC VLSI design and testing focusing high-frequncy applications, MEMS design, fabrication and testing on micrufluidics and accelerometer based energy scavengers.