

**A FULLY INTEGRATED
SAMPLED-ANALOG FUZZY CONTROLLER**

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**TÜMLEŞTİRİLMİŞ
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PREFACE

I wish to express my sincere gratitude to everyone who has contributed to my life.



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Banu Pamir

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A FULLY INTEGRATED SAMPLED-ANALOG FUZZY CONTROLLER SUMMARY

During past two decades, different implementation alternatives covering a very wide spectrum from software emulations to application specific integrated circuits have been developed for the realization of fuzzy logic based controllers. Previously designed prototypes have become highly mature controllers as time went by, and today, daily usage of fuzzy logic is frequently encountered in many indoor and outdoor products, such as washing machines, elevators, air conditioners, cameras, metro networks, etc. Fuzzy logic is preferred in solutions of many control problems because it offers some advantages over classical control approaches. Inexpensiveness, power saving, convergence time reduction, proper accuracy and speed are some of them. In order to decide on the most suitable implementation style for a specific application, some influential issues should be considered; (a) system complexity; number of inputs/outputs and membership functions, and interfacial and internal resolutions, (b) response time of overall system, (c) programmability, (d) compatibility with the outer world, (e) memory requirements, (f) cost, and (g) portability.

Fuzzy controller realization styles reported up to today can be found in the forms of software emulations, microprocessor and microcontroller implementations, reconfigurable or programmable fuzzy processor chips and application-specific fuzzy processor chips. Software emulations offer maximal flexibility in programming and they are adequate for low-volume production, however they are not portable and their response times do not permit fast controlling. Very flexible microprocessor and microcontroller implementations are suitable for low-volume productions and also portable but they are still slow for most applications. Reconfigurable or programmable fuzzy processor chips offer flexibility to some extent, high speed, portability, but they are feasible again for low-volume productions. Application-specific fuzzy controller chips can be considered as the ultimate solutions for best performance, they offer high speed, good compactness, low cost in high-volume production and portability.

In this work, a summary of reported implementations has been given and a novel approach based on sampled-analog circuit techniques has been proposed for the implementation of application-specific fuzzy controllers. A set of seven subcircuits comprising a sample-and-hold amplifier, positive and negative ramp amplifiers, an inference cell, adder and weighted-adder amplifiers, and a divider unit has been explored. These subcircuits form a complete library. By using the proposed library, any fuzzy controller expert system with piecewise linear input membership functions, conjunctive rules, and singleton output classes can be implemented onto silicon. The library was implemented in a 1.2 μm double-metal double-poly CMOS technology. Test results indicate excellent linearity and accuracy in full 0V-5V rail-to-rail operation in all units. A controller of four inputs, 16 rules and two outputs fabricated with these library units occupies 1.76mm² silicon. Test results indicate full functionality. The measured speed was 85 k sample per second.

TÜMLEŞTİRİLMİŞ ÖRNEKLEMELİ-ANALOG PUSLU DENETLEYİCİ ÖZET

Puslu mantık 1960'ların ortalarında Lotfi A. Zadeh tarafından ortaya atıldı. Son yirmi yılda ise puslu mantık tabanlı denetleyiciler için yazılımlardan uygulamaya özel tümdevrelerin tasarımına varan çok geniş bir aralıkta birçok gerçekleştirme yöntemi geliştirildi. Önceleri prototip olarak üretilen denetleyiciler zamanla geliştirildi ve günümüzde denetleyici içeren birçok ürünü kapsayacak oldukça geniş bir yelpazede kullanım alanı buldu. Birçok denetim probleminin çözümü için puslu mantık tercih edilmektedir çünkü ucuzluk, enerji tasarrufu, yakınsama süresinin azalması, uygun doğruluk ve hız gibi birçok avantaj uygulama alanlarına bağlı olarak geleneksel denetim yaklaşımlarından daha etkin bir biçimde sağlanabilmektedir.

Puslu denetleyici gerçeklemleri genel olarak dört sınıfa ayrılabilir; yazılım benzetimleri, mikroişlemci ve mikrodenetleyici gerçeklemleri, programlanabilir puslu işlemciler ve uygulamaya özel kırmıklar. Yazılım benzetimleri programlama açısından en fazla esnekliği sağlamaları ve az miktarlardaki üretimler için uygun olmalarına rağmen taşınabilir ürünlerde kullanılamazlar ve cevap süreleri de birçok denetim problemleri için uzundur. Mikrodenetleyici ve mikroişlemci gerçeklemleri programlama esnekliği sağlamaları ve taşınabilir ürünlerde kullanılabilmelerinin yanı sıra yine düşük miktarlardaki üretim hacimleri için uygundur ve hala birçok uygulama için yeterli hıza sahip değildirler. Programlanabilir puslu işlemciler sınırlı programlanabilirlik özelliğine sahip olmalarına rağmen taşınabilir ürünler için elverişli ve hızlı işlemler için uygundur. Uygulamaya özel kırmıklar taşınabilir, hızlı, yoğun olarak tümleştirilebilirler. Yüksek hacimli üretimler için en uygun çözümleri sunarlar.

Bu çalışmada, literatürde şimdiye kadar yapılan uygulamaya özel puslu denetleyici gerçeklemleri özetlendikten sonra, örneklenmiş-analog devre tekniklerine dayanan yepyeni ve özgün bir yaklaşım önerilmiştir. Bir örnekle-ve-tut kuvvetlendiricisi, pozitif ve negatif rampa kuvvetlendiricileri, bir çıkarım hücresi, toplayıcı ve ağırlıklı toplayıcı kuvvetlendiricileri ve bir bölücü alt devrelerinden oluşan yapı incelenmiştir. Bu alt bloklar beraberce eksiksiz bir kütüphane oluşturmaktadırlar. Önerilen bu kütüphaneyi kullanarak, parça parça lineer giriş sınıfları, 'AND' ile bağlanmış kuralları ve tek değerli çıkış sınıfları olan herhangi bir puslu denetimli uzman sistem silikon üzerinde gerçekleştirilebilir. Kütüphane 1.2 μm çift-poli çift-metal CMOS teknolojisi ile gerçekleştirilmiştir. Yapılan testlerin sonucunda hem tüm modüllerin ayrı ayrı hem de bu modüllerle integre edilen denetleyicinin tamamıyla fonksiyonel olduğu saptanmıştır. Yüksek doğruluk özelliğinin sağlandığını gösteren test sonuçları, iki besleme gerilimi arasında hiçbir kayıp olmaksızın çalışan bütün birimlerin lineerliklerinin de bozulmadığını doğrulamıştır. Denetleyicinin toplam 4 girişi, 2 çıkışı vardır ve 16 kural gerçekleştirilmektedir. 1,76 mm^2 silisyum alanı kaplayan örnek denetleyici saniyede 85 000 örnek olarak çalışabilmektedir.

1. INTRODUCTION

Since fuzzy logic theory was proposed in the mid-1960s, several implementation alternatives have been developed for fuzzy logic based controllers to be used in industrial and commercial applications. Previously designed prototypes have become highly mature controllers as time went by, and nowadays, they take their place in industry and commercial production lines, so, daily usage of fuzzy logic is frequently encountered in many kind of indoor and outdoor products, such as washing machines, elevators, air conditioners, cameras, metro networks, etc. Fuzzy logic is preferred in solutions of many control problems because it offers some advantages over classical control approaches. Inexpensiveness, power saving, convergence time reduction, proper accuracy and speed are some of them.

Fuzzy controller realization styles reported up to today can be found in the forms of software emulations, microprocessor and microcontroller implementations, reconfigurable or programmable fuzzy processor chips and application-specific fuzzy processor chips. Software emulations offer maximal flexibility in programming and they are adequate for low-volume production, however they are not portable and their response times do not permit fast controlling. Very flexible microprocessor and microcontroller implementations are suitable for low-volume productions and also portable but they are still slow for most applications. Reconfigurable or programmable fuzzy processor chips offer flexibility to some extent, high speed, portability, but they are feasible again only for low-volume productions. Application-specific fuzzy controller chips can be considered as the ultimate solutions for best performance. They offer high speed, good compactness, low cost in high-volume production and portability.

In the bulk of this thesis, a novel sampled-analog approach proposed for the implementation of application-specific fuzzy controllers is investigated. In Chapter 2 a brief description of fuzzy control is given. Chapter 3 is dedicated to a summary of

hardware implementation examples reported in the literature. The novel sampled-analog application-specific fully integration approach proposed is examined in detail in Chapter 4. The description of a prototype chip designed with the novel modules, and, its simulation and test results form the subject matter of Chapter 5. Concluding remarks are given in Chapter 6.



2. FUZZY CONTROL IN BRIEF

The underlying theory of fuzzy controlling was suggested by Lotfi A. Zadeh in the mid-1960s to develop a suitable model for human reasoning. The first successful industrial application of fuzzy logic theory was a cement kiln control system developed in 1979, and the first fuzzy chip was designed by Togai and Watanabe and prototyped in 1985.

Using fuzzy logic, one can perform meaningful and reasonable operations on the concepts outside the definitions available in conventional Boolean logic. Fuzzy logic deals not only with true and false but also with the range between true and false. From this point of view, the traditional binary or multi-valued logics can be considered as the special cases of fuzzy logic [1, 2].

In spirit, fuzzy logic is much closer to human thinking and natural language than the traditional logical systems [3-11]. In essence, human concepts and linguistic terms construct the frame of this logic imitating human reasoning and controlling skills. Whereas the conventional (binary or multi-valued) logic paradigms prescribe sharp boundaries between the classes in the input and output spaces, the transition from one class to another is gradual in fuzzy logic. Classes overlap with their neighbors, i.e., intersection of two neighboring classes is not empty in contrast to the case in the conventional ones. This gradual transition between neighboring classes results in continuous and smooth variations in the control surfaces of fuzzy controllers. That is why, for controlling of continuously varying systems, such as electric motors, this kind of logic may be considered as the most convenient approach. Furthermore, it suggests very simple solutions to very complicated nonlinear control problems.

The degree of membership on a class is specified with a number between 0 and 1, where 0 and 1 correspond to full nonmembership and full membership, respectively. Classes are labeled by linguistic variables but not numbers, and

inference is achieved by using IF-THEN rules which are simply the control instructions of a skilled human operator. In this respect, fuzzy logic offers the most appropriate and reasonable way to construct a controller with only an expert's knowledge and without any need of a crisp mathematical model of the system. In almost all cases, a human operator does not need to know how the system under his control works technically, but he only needs to learn which inputs yield which outputs, such as a driver does. Moreover, for many purposes, a very approximate characterization of collected data is sufficient because humans do not require a high degree of precision during their controlling executions. This type of imprecision has its own advantages, such as in the case of handwriting recognition. The human is able to recognize the characters written by either different style or different people, but a machine has considerable difficulties in recognizing even fairly similar characters.

In traditional control modeling, the first step is to derive a mathematical model describing the system. To do this one needs a detailed understanding of all variables in the system, but that is not easy if the system is complicated. In contrast, fuzzy modeling deals with the relationship between inputs and outputs lumping many parameters together. Thus, an exciting simplification in the solution of the control problem may appear by approaching the problem simply as an operator but not as an engineer.

In general, fuzzy logic is best applied to nonlinear and/or ill-defined systems. Mostly, control of these type of systems can not be modeled by mathematical equations, or even if those can be modeled, it might be impossible to realize them by conventional control techniques. Besides, for some mathematically modeled complex controllers, traditional proportional, integral and derivative (PID) techniques may be possibly applied, but fuzzy solutions suggest some advantages over these conventional methods. Power reduction, convergence time reduction, rapid prototyping, inexpensiveness, proper accuracy and speed are some of them [7, 8, 10, 12].

The typical fuzzy controller architecture is given in Fig.2.1. Essential inference mechanism is stored in the rule base which consists of the extract rules derived from the expertise on the system under control. The fuzzifier can be

considered as an interface which transforms the numerical input data collected from the input sensors into input membership grades with associated class labels. The fuzzified data (fuzzy inputs) are available to be processed by the inference engine. Control rules are executed during the inference and at the end of this process the resulting fuzzy domain control information (fuzzy outputs) should be converted into real control signals by a defuzzifier. The defuzzifier transforms the output membership grades with associated class labels into the crisp control signals of the physical system.

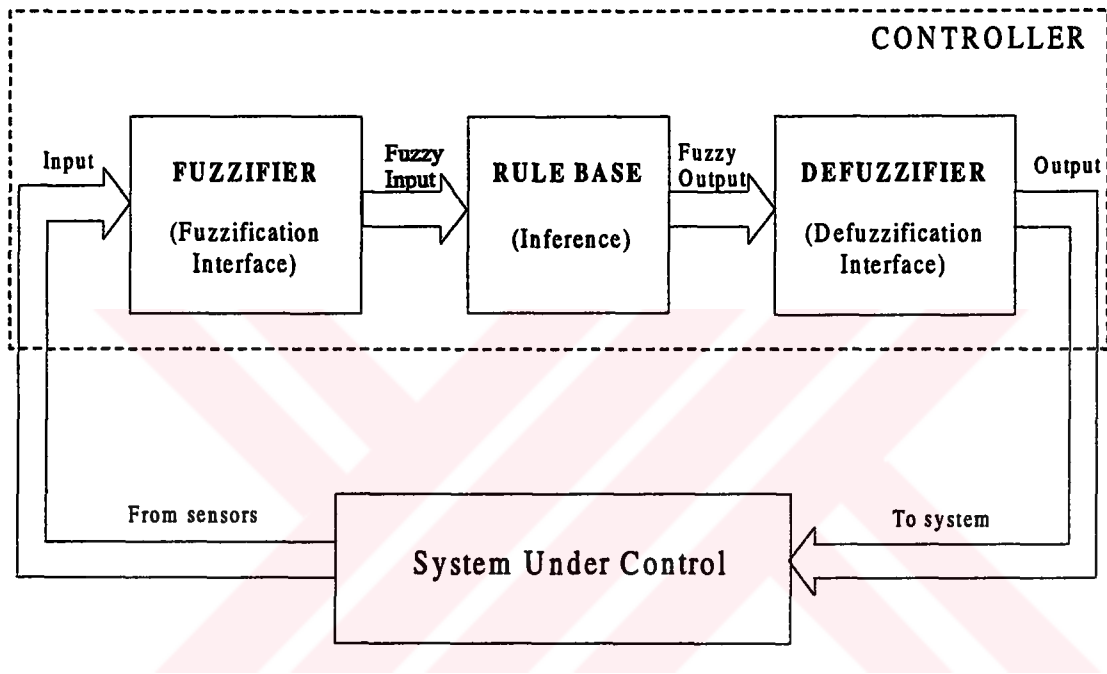


Figure 2.1 Typical architecture of a fuzzy controller.

A descriptive schematic of fuzzy inference mechanism with fuzzification and defuzzification interfaces is shown in Fig.2.2 for the rules;

Rule-1: IF (x_1 is A_1) AND (x_2 is B_1) THEN (y is C_2)

Rule-2: IF (x_1 is A_2) AND (x_2 is B_2) THEN (y is C_1).

Here, x_1 and x_2 , represent the input variables, y is the output variable, A_1 , A_2 , and B_1 , B_2 are input class labels belonging to the input variables x_1 and x_2 , respectively, and C_1 and C_2 are the output class labels for y . In a rule, IF clause contains antecedent terms and THEN clause contains consequent terms; " x_1 is A_1 " is an antecedent term and " y is C_1 " is a consequent one, etc. Theoretically, connection of the antecedent

terms may be done both “AND” (disjunction) and “OR” (conjunction) operators. These connectives correspond to minimum and maximum selection operations on the membership degrees conveyed by the antecedent terms. In above given exemplar rules, however, only “AND” connection is used.

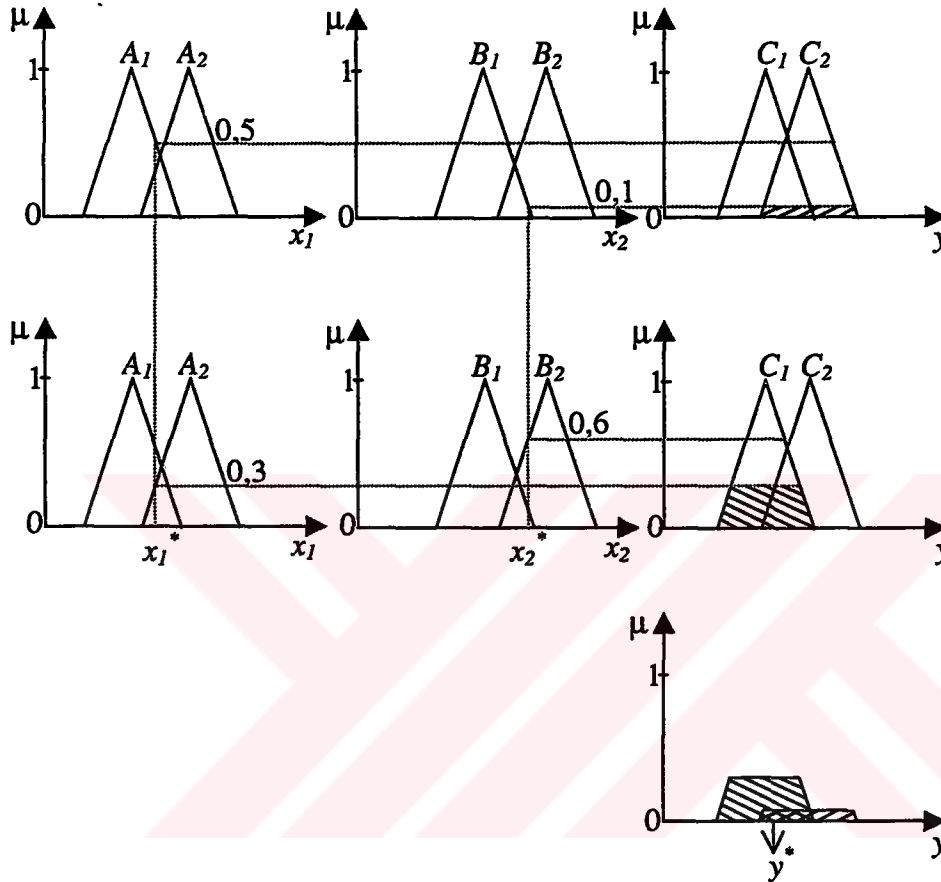


Figure 2.2 Graphical representation of fuzzy inferencing.

In fuzzy logic, a decision is made by aggregating all the rule contributions within the inference mechanism, so, both given rules should participate to decide the control action for this example. In the first rule, for the given x_1^* and x_2^* depicted in Fig.2.2, first antecedent term gives a membership degree (μ) of 0,5 while the second one gives 0,1. AND operation results in a dominant degree of 0,1 which is the IF part outcome of this rule. This value is effective on the output class C_2 (this is the execution of THEN part of the first rule) with the same membership degree of 0,1 that is drawn in the right-hand side of the figure. Similarly, in the second rule, for the same input values, first antecedent term gives a membership degree of 0,3 and the

second one gives 0,6. IF part outcome of this rule is determined by the first term as 0,3 and the output class C_I is affected by this membership degree. As a result of the following defuzzification, aggregation of these two outcome yields the value for y as y^* . This is the center of gravity of the shaded areas, but in most cases output classes are chosen as singletons, so, center of gravity calculation is converted to find the weighted average of singletons.



3. HARDWARE SOLUTIONS FOR FUZZY LOGIC CONTROLLERS

Different implementation alternatives covering a very wide spectrum from software emulations to application specific integrated circuits have been developed for the realization of fuzzy logic based controllers. In order to decide on the most suitable implementation style for a specific application, some influential issues should be considered; (a) system complexity; number of inputs/outputs and membership functions, and interfacial and internal resolutions, (b) response time of overall system, (c) programmability, (d) compatibility with the outer world, (e) memory requirements, (f) cost, and (g) portability [13].

Software implementations on standard general-purpose microcontrollers offer a complete flexibility stemming from ease of programming but do not suit time-critical applications because the computation times are around seconds or subseconds [14,15]. An alternative approach is to program a RAM, in which the precomputed outputs for every quantized input value for the entire control surface of the controller are stored. In this look-up table implementation, response time is very short but the required memory grows exponentially with the number of input and output variables and/or with resolution. Usually the use of look-up tables is limited to applications with 2-3 input and 1-2 output variables and a resolution of 4-8 bits. Another option is to configure a fuzzy dedicated coprocessor and a processor together. This approach yields high speed and some extent of flexibility but the cost is still high. Special purpose coprocessors usually adopt triangular membership functions, however, the construction of arbitrary membership functions has been reported [16]. In general, programmability provides some extent of flexibility for different usage purposes, but only at the expense of poor functional density on silicon and in some cases low speed. The ultimate solution for the best performance is to develop a dedicated hard-wired architecture committed to a single application. Application specific integrated circuit implementations can arrive at a collection of high speed, good compactness and low cost satisfying the tight optimization

conditions in the design [17]. However, a considerably high production volume is needed to achieve cost targets.

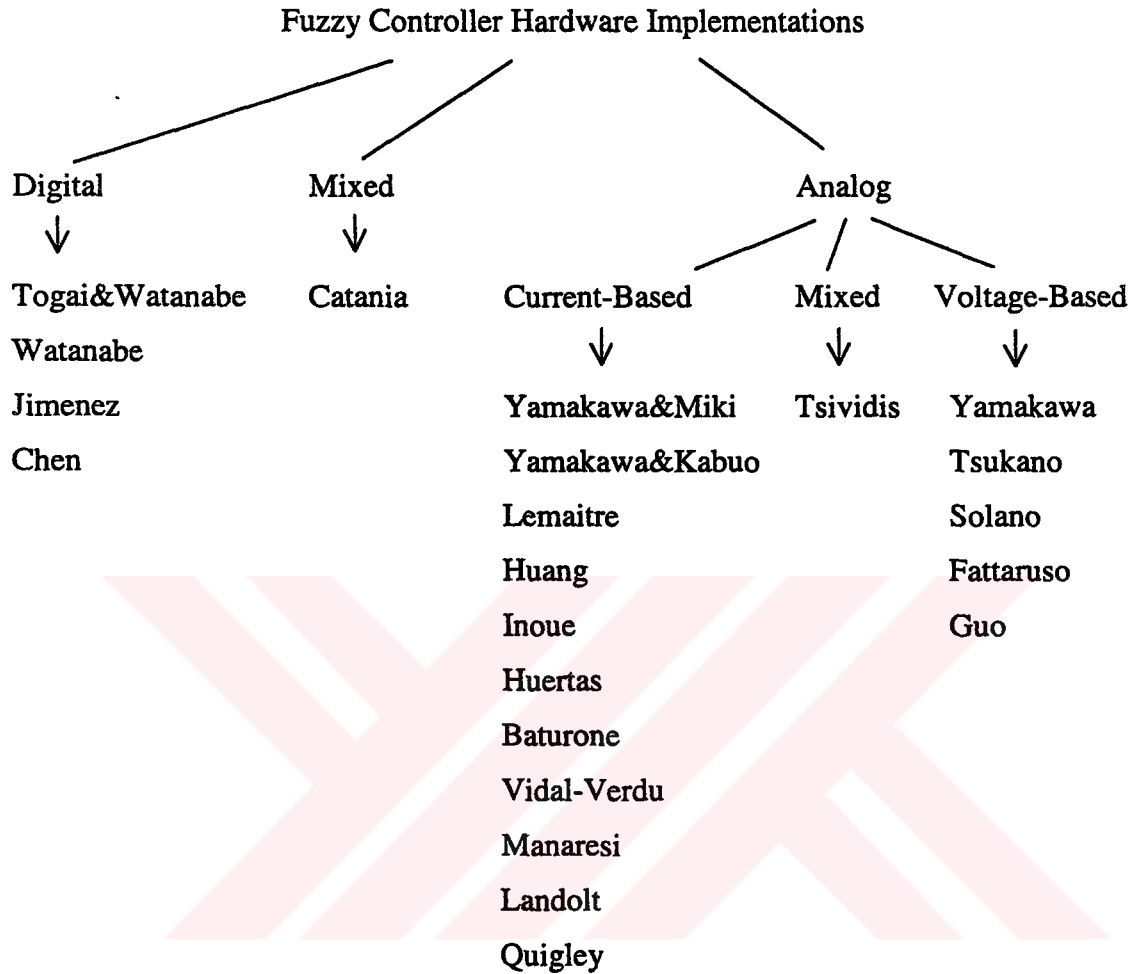
Fuzzy logic controller implementations may be investigated by categorizing them according to their circuit level execution methods of the fuzzy operations. Namely, digital and analog. Some analog designs incorporate digital parts mostly for the purpose of facilitating interfacing problems, but this does not prevent them from being categorized as analog designs.

Although digital realization approach is not the native implementation style for analog-like natured fuzzy logic control, it takes a significant place among hardware implementations. There is one main reason; this type of realization permits the application of very simple and straightforward digital circuit design and implementation techniques. Since high performance controllers are essential, improved design architectures and algorithms have been proposed for digital implementations [18-22]. Once the architectural configuration is determined, circuit and layout level design can be automatically generated by utilizing standard cells and existing design tools. Thus, fully digital integration becomes a very useful and powerful technique with many aspects such as easy and rapid design and prototyping, good programmability, accuracy, safe signal processing of the data and compatibility with digital systems. However, it is not so effective in such respects as the speed of the operation time, consumed power, functional density, silicon area and consequently fabrication cost. Indeed, digital fuzzy controller chips occupy larger silicon areas in comparison with their analog counterparts.

On the other hand, analog realization approach is pretty close to the nature of fuzzy logic control. Although implementation of fuzzy operations by analog circuits has the inherent difficulties of analog design, it is very powerful in arriving at high operation speed, low power consumption, high functional density, good compatibility with analog sensors and actuators, small silicon area and hence, low fabrication cost.

In the rest of this chapter, hardware implementations of fuzzy controllers reported in open literature will be reviewed. Implementation styles can be

categorized into subgroups as follows. Each implementation style will be mentioned with the author's name in the manuscript.



3.1 Digital Hardware Implementations

3.1.1 Togai&Watanabe Implementation

The first fully digital implementation of a fuzzy inference engine was introduced by Togai and Watanabe [23]. Universe of discourse of a fuzzy set was limited by 31 elements, i.e., input and output spaces are discretized into 31 levels. Membership function degrees were also quantized into 16 levels by using 4 bits. In this case 124 bits are necessary for digitization of a membership function as represented below.

	u_1	u_2	u_3	...	u_i	...	u_{31}
$A_i :$	0010	0100	0010	...	$\mu_{A_i}(u_i)$	...	0000

In this application, the rule set was stored in a ROM. The inference is obtained by intersection and union operations, which are realized by digital AND and OR circuits. Each of the 31 quanta is scanned sequentially and 4 bit membership degree information is processed in parallel for an inference. Fig.3.1 shows the (a) graphical representation, and (b) functional architecture of the inference mechanism. As depicted in the figure, in the first level, each of the 31 membership class value of observation is compared with the stored membership class value with the AND operation. The following OR operation is for determining the maximum intersection grade which indicates the rule output. AND-OR operations are repeated 31 times until the input stream ends. In the second level, rule outputs representing the rule activation levels, truncate the output membership classes with an AND operation and the final OR gives the aggregated output.

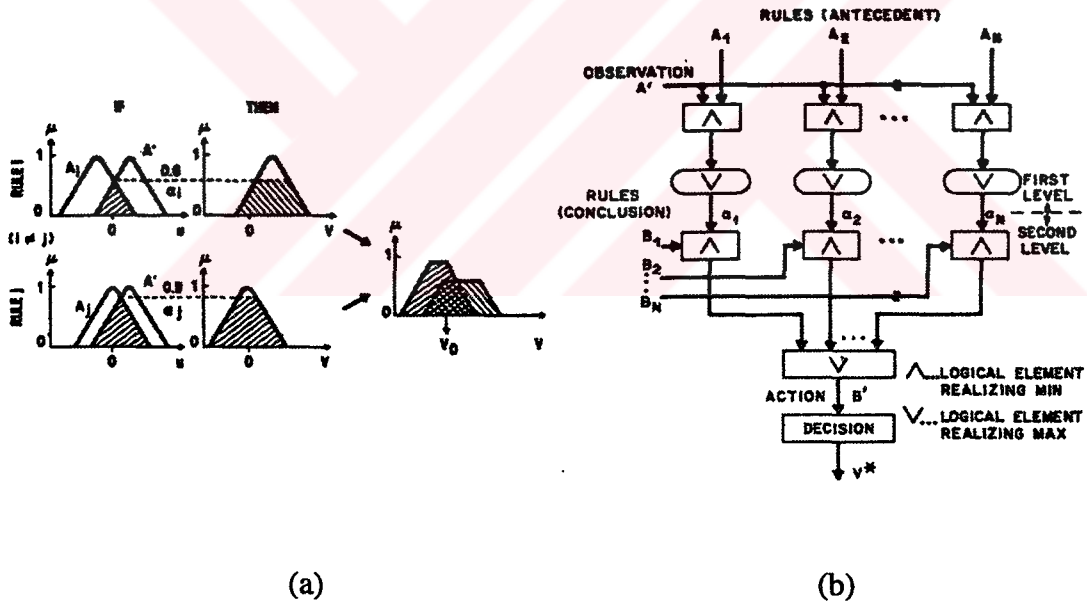


Figure 3.1 (a) Graphical representation, and (b) functional architecture of the inference mechanism in [23].

This implementation stores 16 rules, each consisting of 124 bits for antecedent and 124 bits for consequent with 1 input and 1 output. The active area of the chip is 2.99 mm by 3.48 mm. A 68-pin package was used but only 8 pins are used for I/O operations, many of the others are for the observation of some critical nodes.

The engine can perform approximately 80 kFLIPS (Fuzzy Logic Inferences per Second).

3.1.2 Watanabe Implementation

Continuation of this implementation can be found in [24, 25] which has a reconfigurable and cascable architecture for general purpose applications and includes the defuzzification in this case. In this study, input and output spaces are discretized into 64 levels instead of 31, 6b D/A and A/D converters are utilized for analog communication with the outside of the controller, but internal membership degree resolution is the same 4 bits. The chip can be set to one of the following two individually programmable configurations: i) 4-input/2-output with 51 rules, ii) 2-input/1-output with 102 rules. The rules can be programmed and stored in a RAM. It was fabricated in 1.1 μm CMOS technology and includes about 688k transistors. The chip occupies 7.75 mm x 9.05 mm silicon area in a 68-pin package. It consumes 1.2W@0°C with 3V power supply and can perform 580 kFLIPS. The center of gravity method is used for defuzzification, and it is achieved by using digital adder and divider circuits which compute the equation

$$C^* = \frac{\sum_{n=0}^{63} n \cdot \mu(n)}{\sum_{n=0}^{63} \mu(n)},$$

which can be decomposed as

$$\begin{aligned} \sum_{n=0}^{63} n\mu(n) &= \mu(63) + \\ &\quad \mu(63) + \mu(62) + \\ &\quad \dots\dots\dots + \\ &\quad \mu(63) + \mu(62) + \dots\dots\dots + \mu(0). \end{aligned}$$

3.1.3 Chen Implementation

Another defuzzifier circuit computing the above equation and a minimum circuit are presented in [26], and [27], respectively. They are both BiCMOS dynamic circuits. The defuzzifier circuit was laid out onto a silicon area of size 4.796 mm x

5.219 mm in 2 μ m BiCMOS technology. It performs a conversion time of 1.6 μ s. A 4-input 4b minimum circuit occupies an area of 0.955 mm x 1.112 mm and it can select the minimum within 7.4 ns.

3.1.4 Jimenez Implementation

In [28-30] some programmable fully digital fuzzy controller architectures are given. Block diagram is given in Fig.3.2. Computing strategy is to drive only the active rules, the rest of all possible rules that yield zero activation levels are not taken into account.

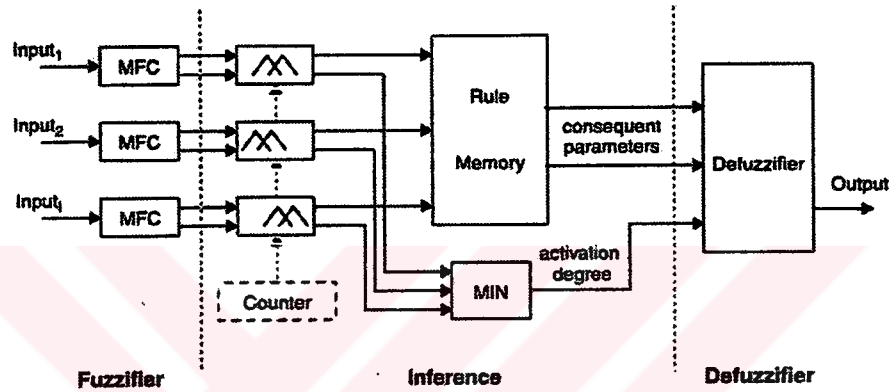


Figure 3.2 Block diagram of the achitecture proposed by [28-30]

Two different membership function construction approaches are presented. Namely, vectoral storage and arithmetic generations. These are represented in Fig.3.3.

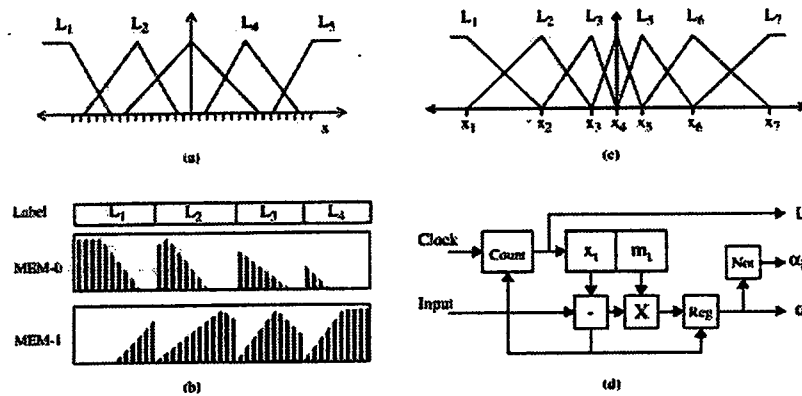


Figure 3.3 Memory-based membership function construction; (a) fuzzy sets, (b) memory organization. Arithmetic membership function construction; (c) fuzzy sets, (d) block diagram of the generator.

While memory-based membership functions allow the programmer to define unrestricted fuzzy set shapes, the arithmetic generators offer limited options but they bring a considerable area gain. In the first case all the membership values should be stored in a memory, while in the second, only breakpoints and slopes define the function but an arithmetic calculator must be designed. The inference block is composed of an active rules selection circuit, a multi-input min circuit and a memory for storage of the rules. The defuzzification contains digital multiplication, division and addition.

Based on the two types of construction methods, two different fuzzy controller prototypes have been implemented by using standard-cells, the first uses memory-based membership functions. Both of them consist of 3-input/1-output controllers which can construct up to 8 membership functions by 6b resolution. All possible rules can be programmed with different consequent values. Both prototypes have been implemented in 1 μm CMOS technology. The total area is 14.36 mm^2 for the first and 12.53 mm^2 for the second. Respectively, 3 MFLIPS and 2.77 MFLIPS operation speeds have been measured for two prototypes with an 8% maximum error.

FPGA implementations of similar digital design architectures can be found in [31-33].

3.2 Analog Hardware Implementations

3.2.1 Yamakawa&Miki Implementation

The first examples of current-based analog fuzzy controller circuits have been introduced in [34]. Nine basic fuzzy logic functions (bounded difference, complement, bounded product, max, bounded sum, min, implication, absolute difference and equivalence) were defined by max, min, algebraic sum and algebraic difference on the membership degrees. Realizations of these functions with fuzzy logic circuits employing current mirrors and diode connected transistors have been proposed. The basic logic cell is depicted in Fig.3.4 (b). The others are derived from this circuit. Other functions can be expressed only with the bounded difference and algebraic sum. They are respectively expressed as

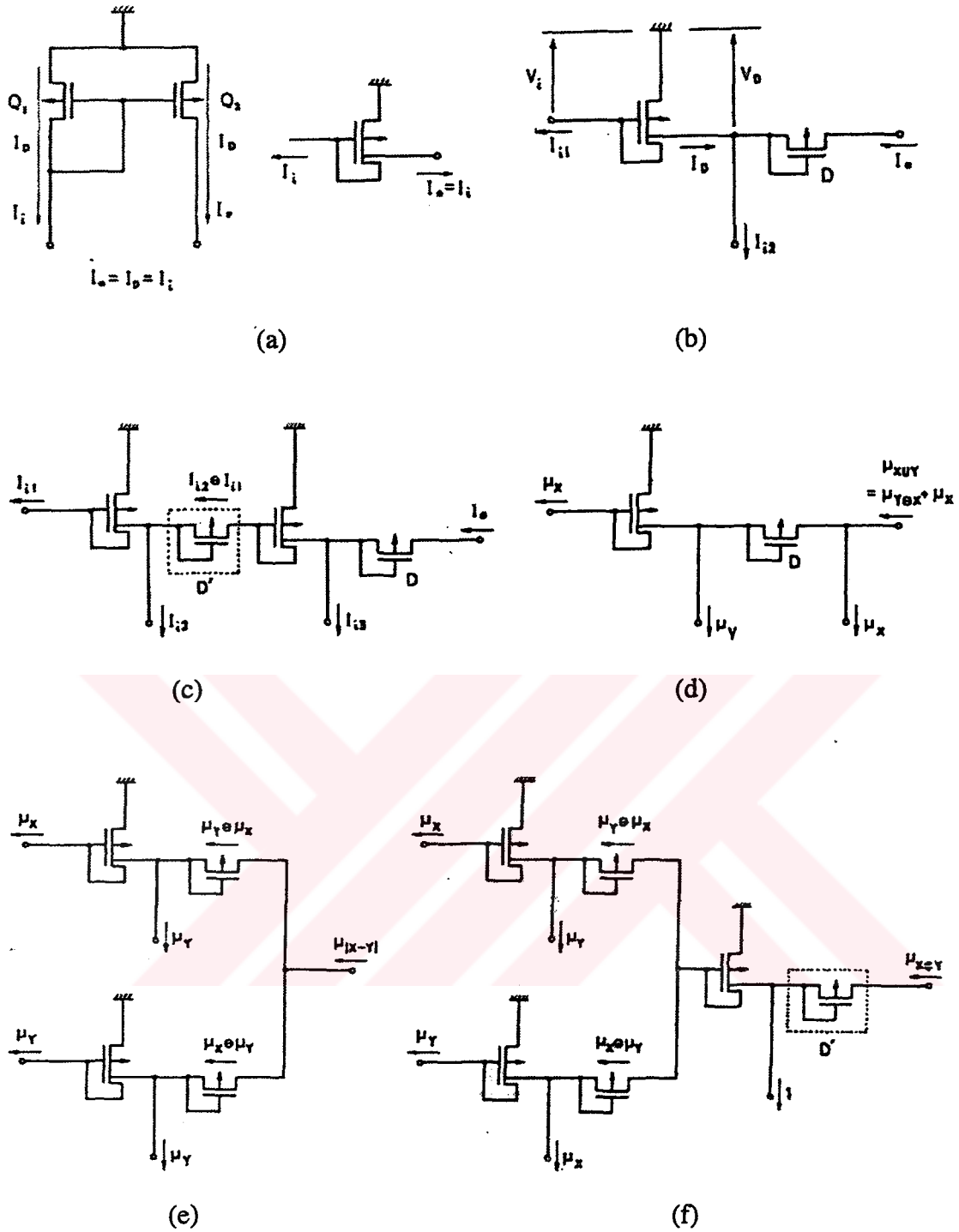


Figure 3.4 The circuits implementing nine basic fuzzy logic functions; (a) simple current mirror circuit and its symbolic representation, (b) basic logic cell circuit realizing the functions given by Table 3.1, (c) cascade connected basic logic cells realizing the functions given by Table 3.2, (d) max circuit, (e) absolute difference circuit, and (f) equivalence circuit.

$$\mu_{x \ominus y} \equiv \max[0, (\mu_x - \mu_y)] = \mu_x \ominus \mu_y, \quad \mu_{x + y} \equiv \mu_x + \mu_y.$$

The algebraic sum is implemented only by wiring in the current mode circuits.

Some of the functions can be realized by changing the terminal connections of the circuits, these are shown in Table 3.1 and Table 3.2 associated with Fig.3.4(b) and (c), respectively. Fig.3.4(a) shows PMOS current mirror circuit and its symbolic representation which is used in circuit descriptions, (d), (e), (f) show the max, absolute difference and equivalence circuits, respectively.

Table 3.1 Functions of the basic logic cell.

Functions	Input; I_{i1}	Input; I_{i2}	Output; I_o
Bounded-difference	μ_Y	μ_X	$\mu_X \ominus \mu_Y$
Complement	μ_X	1	$\mu_X' = 1 \ominus \mu_Y$
Bounded-product	1	$\mu_X + \mu_Y$	$\mu_X \odot_Y = (\mu_X + \mu_Y) \ominus 1$

Table 3.2 Functions of the cascade-connected basic logic cells.

Functions	Input; I_{i1}	Input; I_{i2}	Input; I_{i3}	Output; I_o
Bounded-sum	$\mu_X + \mu_Y$	1	1	$\mu_X \oplus_Y = 1 \ominus [1 \ominus (\mu_X + \mu_Y)]$
Intersection	μ_Y	μ_X	μ_X	$\mu_X \cap_Y = \mu_X \ominus (\mu_X \ominus \mu_Y)$
Implication	μ_Y	μ_X	1	$\mu_X \rightarrow_Y = 1 \ominus (\mu_X \ominus \mu_Y)$

CMOS current source based circuits exhibit good linearity and supply voltage insensitivity. Short term of design and fabrication can be reached by this implementation approach, because the design of a controller can be completed only by connecting basic function blocks.

3.2.2 Yamakawa&Kabuo Implementation

A programmable membership function circuit consisting of the circuit structures given above were presented in [35]. Cascoded current mirrors were adopted because of their better mirroring performance than normal current mirrors. With 2 μ m CMOS technology and 12V supply voltage, 8-14% fullscale sensitivity to supply voltage fluctuations between 8V-14V and 15% fullscale error were measured when the temperature was changed from -55°C to 125°C. Response time is around 30 ns. Good integration density, fast response and some extent of insensitivity to the

supply voltage can be obtained by these structures, but, each programming current occupies one pin.

3.2.3 Lemaitre Implementation

A fully integrated current-based analog implementation was given in [36-39]. The controller was constructed with CMOS current mirrors. Primitives are defined in a different fashion as positive cut, negative cut and sum operations. Sum operation corresponds to hard wiring of the signals, and the others are expressed as

Positive-cut operator N ;

$$N(x) = \begin{cases} -x & \text{if } x \geq 0 \\ 0 & \text{otherwise.} \end{cases}$$

Negative-cut operator P ;

$$P(x) = \begin{cases} -x & \text{if } x \leq 0 \\ 0 & \text{otherwise.} \end{cases}$$

Electronic implementations of the primitive operators and basic building blocks are given in Fig.3.5.

A 2-input/1-output (three membership functions for each) controller with 9 rules was implemented. The rules can be programmed with current sources. The core occupies 0,4 mm² area with 1,2 μm CMOS technology including about 500 transistors, but a 40-pin package was used. The chip consumes 10mW with 5V supply voltage. The performance of the achitecture reaches 10 MFLIPS. This approach provides considerably fast design from functional description to layout, but it needs lots of pins for externally applied reference currents for programming. The proposed fuzzy block library is independent of the technology and appropriate for synthesis and design automation.

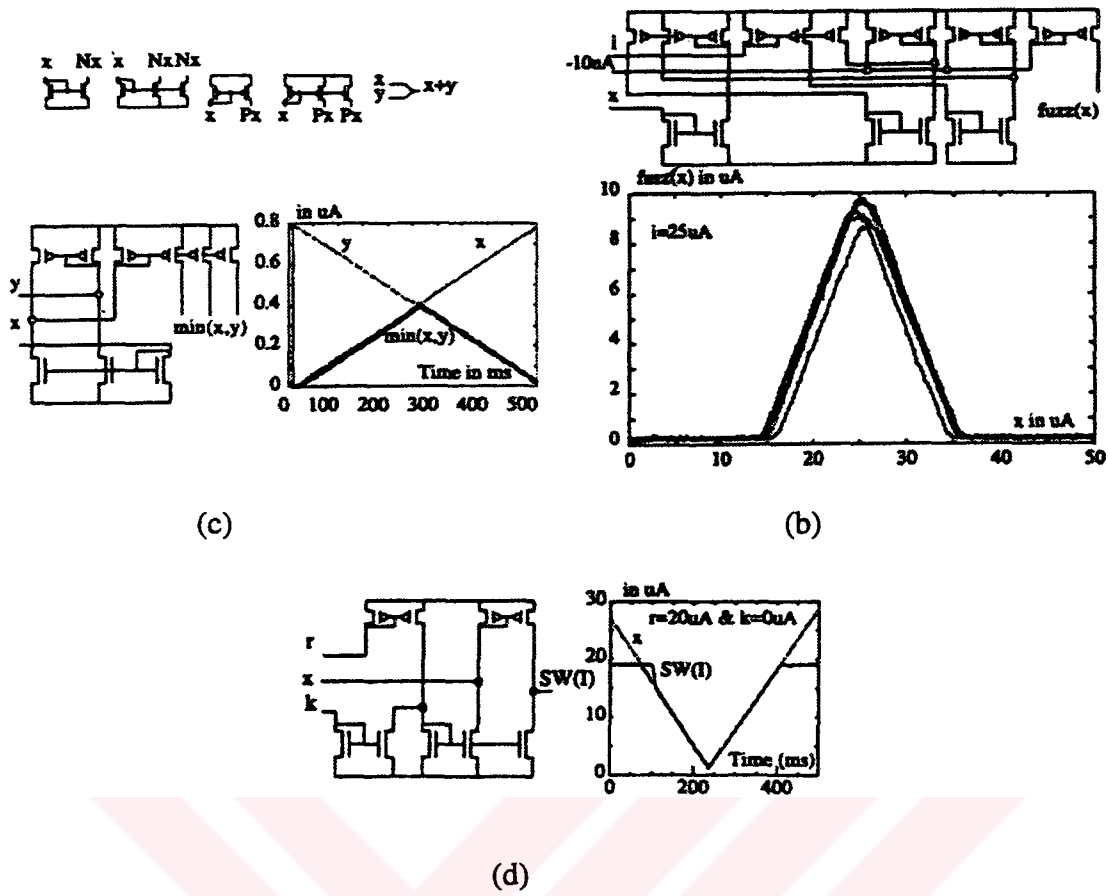


Figure 3.5 (a) Primitive operator circuits, (b) a membership function circuit and measured current, (c) a min circuit and measured current, and (d) a switch circuit and measured current.

3.2.4 Huang Implementation

More than two antecedent terms necessitate multiple input minimum and maximum circuits to avoid a binary-tree realization. Binary-tree realization also is a solution, but, inefficient usage of silicon area, lowering of the processing speed and accumulation of the error when the signal passing through the tree stages result in design of multiple input structures. With regard to these obvious requirements, current-based multiple input minimum and maximum circuits for fuzzy logic controllers have been proposed in [40–42]. Presented modular-structured multiple input minimum circuits were designed with $4n+1$ transistors for n inputs. A three-input min select structure is illustrated in Fig.3.6. By assuming the minimum current is I_1 , the circuit works in the following way: V_1 becomes the highest voltage among the all three in the cells, hence, all of the bias current I_b flows through the transistor

$$C = \frac{\sum_{i=1}^n \mu_{xi} \times x_i}{\sum_{i=1}^n \mu_{xi}}$$

$$C = \frac{\mu_{x1} \times x_1}{\sum_{i=1}^n \mu_{xi}} + \frac{\mu_{x2} \times x_2}{\sum_{i=1}^n \mu_{xi}} + \dots + \frac{\mu_{xn} \times x_n}{\sum_{i=1}^n \mu_{xi}}.$$

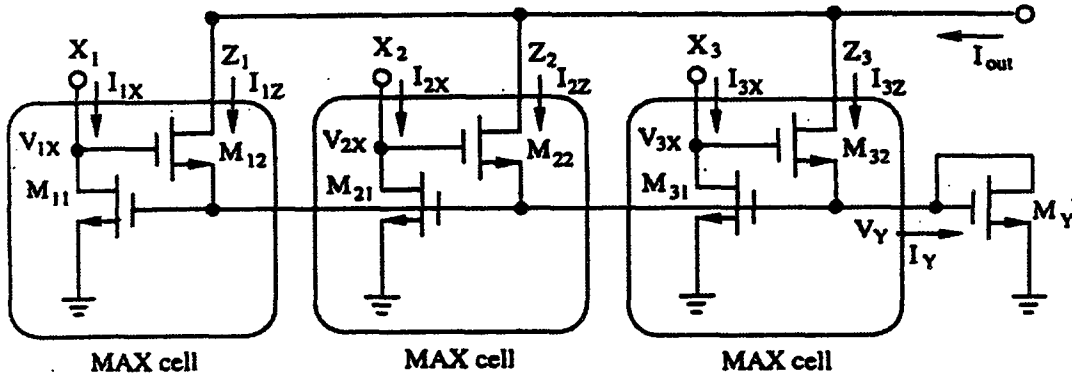


Figure 3.7 The current-mode 3-input maximum circuit proposed in [42].

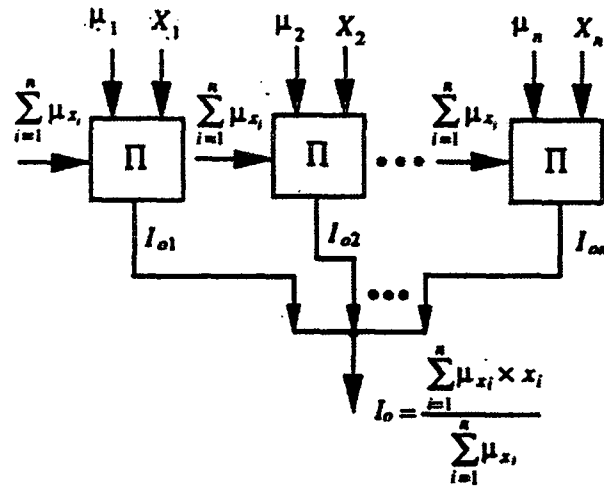
The corresponding block diagram and the contents of one multiplier block are given in Fig.3.8. Shown in (b) are current-based square-rooting and squaring circuits, which calculate the equations

$$I_Y = 2\sqrt{I_\mu \times I_X},$$

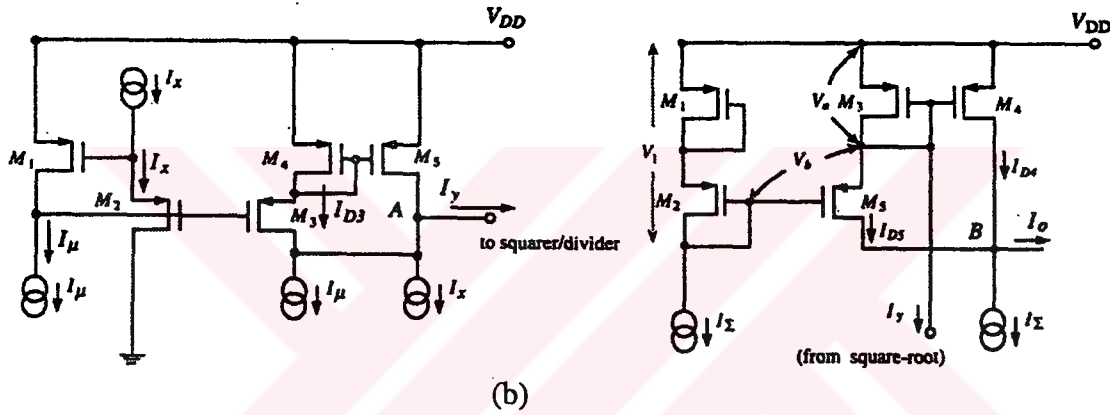
$$I_O = \frac{I_Y^2}{4I_\Sigma},$$

respectively, when the transistor dimensions are properly selected.

The circuits were designed by taking advantage of the square-law MOS characteristics proposed in [44]. Only simulation results were reported which indicate 90ns response time for a multiplier block. Continuation of the studies above can be found in [45-47]. A programmable membership function generator was proposed in [47], but, there was no attempt for physical implementation.



(a)



(b)

Figure 3.8 (a) Block diagram for center of gravity method and (b) square-rooting and squaring circuits used in [43].

3.2.5 Inoue Implementation

Different current-based multiple input minimum and maximum circuit structures were proposed in [48, 49]. A maximum operation can be implemented with $(n+1)n$ transistors and a minimum one with $(n+1)n+2n$ for n inputs with the circuits presented in [48]. In this realization, a max selection structure was proposed (Fig.3.9(a)), because the min selection circuit includes a max circuit inside anyway, relying on De Morgan's law (Fig.3.9(b)). The operation of the circuit in Fig.3.9(a) can be explained by assuming that I_1 increases and becomes the max current, which means that the largest increase occurs in x_1 , ID_2 and ID_3 increase, so x_2 and x_3 decrease, hence ID_1 decreases. By this positive feedback mechanism, x_2 , x_3 and ID_1

eventually become zero and I_{out} approaches I_1 . It was reported that step response takes 140ns and maximum full scale error was within 1% based on the simulations.

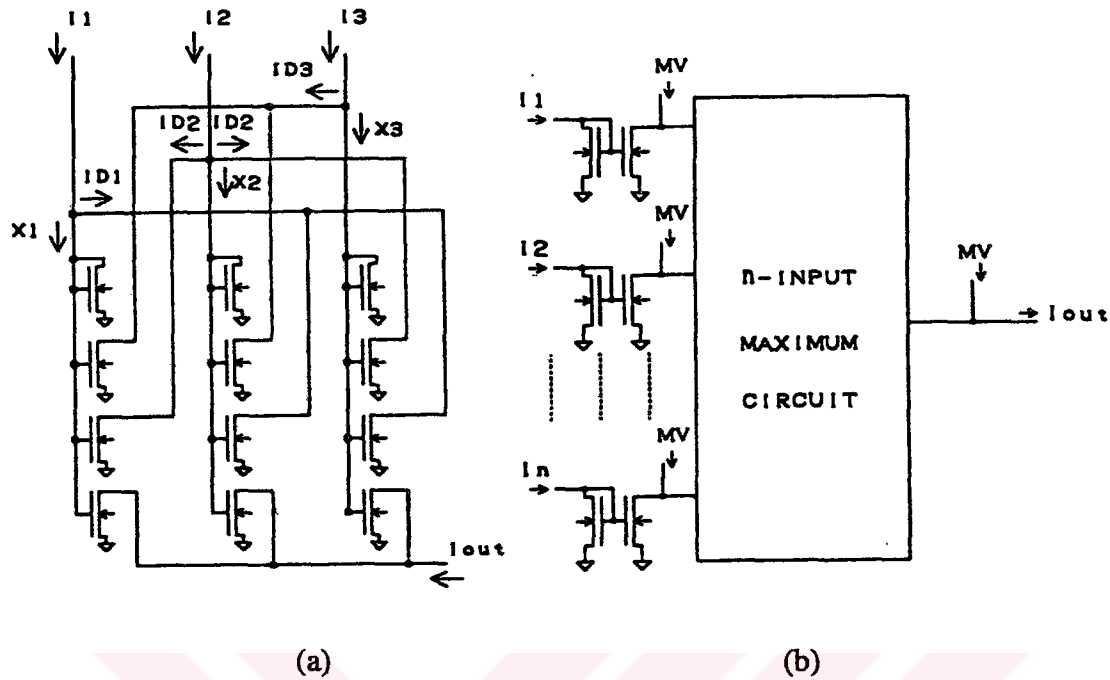


Figure 3.9 (a) Three-input max circuit and (b) n-input min circuit proposed in [85].

3.2.6 Huertas Implementation

A fully integrated programmable fuzzy controller was implemented with current-based circuits [50-57]. The architecture given in Fig.3.10. Individual programming flexibility for membership functions, rules and consequent weights is provided. Basic building bloks in this structure are given in Fig.3.11. The proposed membership function circuit is given in Fig.3.11(a). Digital programmability is added via current-mode DACs into the structure. The inverter is used for biasing both transistors T_1 and T_2 in conduction. From the output of the maximum selector in Fig.3.11(b) only the maximum current can be taken if such an input current exist. Otherwise, when there are p equal maximum input currents, the cells, having the maximum current in their inputs, share equally this current so I_{max}/p flows from each as the output current, hence, total I_o is equal to I_{max} . The current-input/voltage- output defuzzifier was configured by using two circuits depicted in Fig.3.11(c) and (d). The circuit in Fig.3.11(c) converts the difference of input currents into voltage through a voltage-controlled resistance made of four matched transistors biased in triode region. Its transfer characteristics can be expressed as

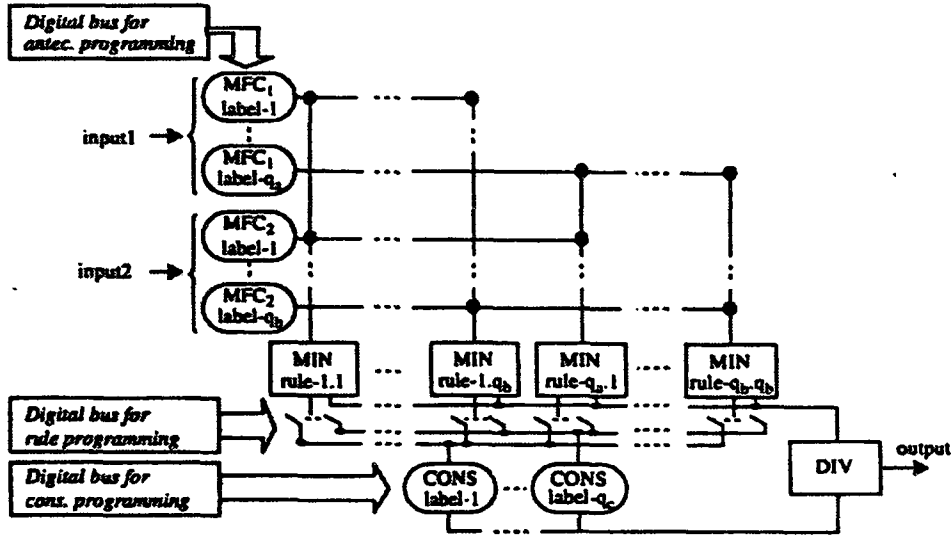


Figure 3.10 Rule, consequent and membership function programmable architecture proposed in [50-57].

$$V_1 - V_2 = \frac{I_a - I_b}{\beta(V_a - V_b)}$$

where β is the transconductance factor of MOS transistors. The I/V converter in Fig.3.11(d) completes the current division operation and yields an output voltage (differential output voltage) as

$$V_o = k_d \frac{I_a - I_b}{I_c - I_d} = k_d \frac{I_{num}}{I_{den}}$$

in which k_d is determined by the transconductance factors.

A 2-input/1-output/9-rule (3 labels per each) rule chip and a divider chip have been prototyped separately with 2,4 μm CMOS technology by employing the proposed circuits. Rule chip's analog core occupies an area of 0,90 mm by 1,05 mm and divider size is 0,0497 mm². The length of digital words for programming antecedent and consequent parameters is 8 bits (4b for I_{aux} , 2b for I_{sat} and 2b for m) and 4 bits, respectively, while the rule set is fixed to a typical arrangement covering all possible rules. The equivalent precision of the entire controller is 6b and the inference speed can reach 2 MFLIPS.

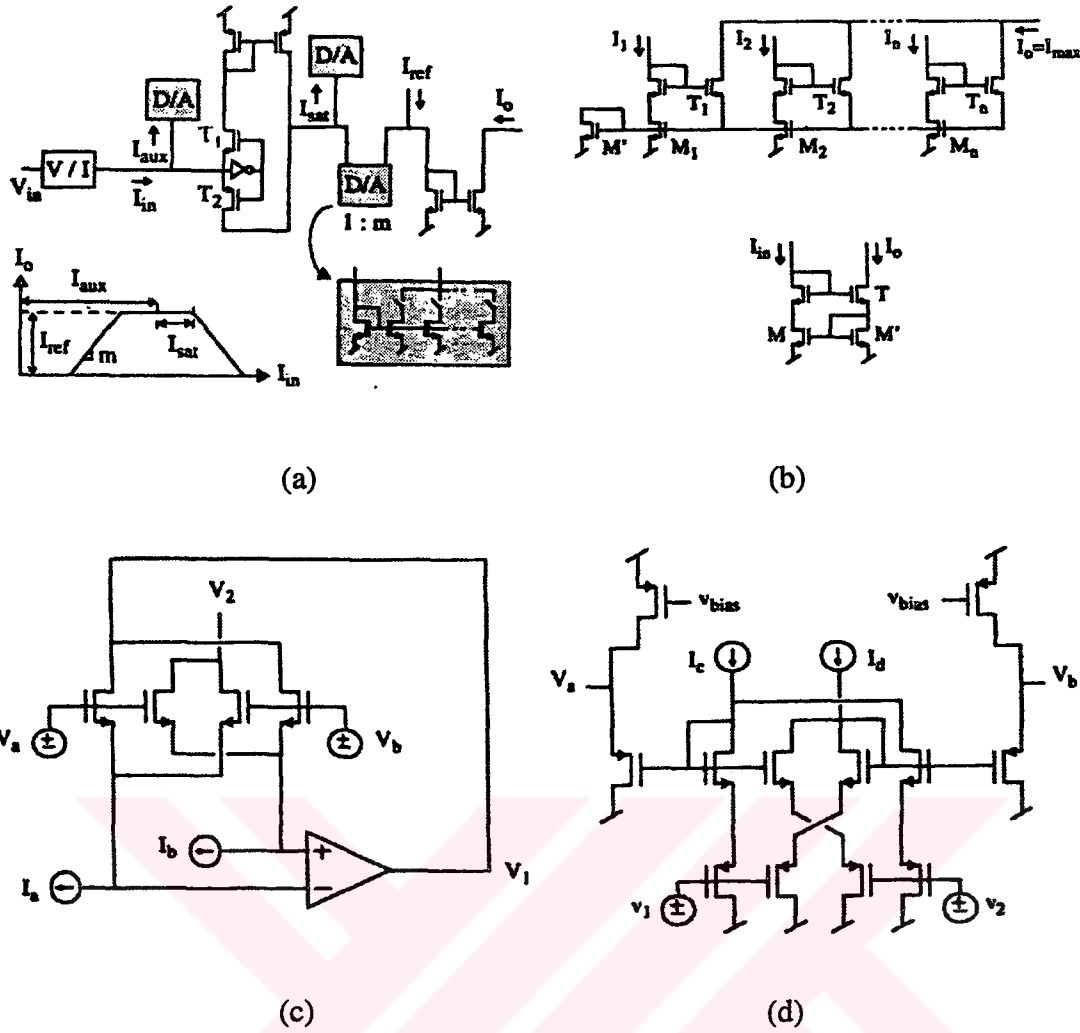


Figure 3.11 Building blocks; (a) membership function generator with parameters to define a trapezoid, (b) maximum selection circuit derived from improved Wilson current mirror (below), (c) transresistance amplifier, and (d) I/V converter.

3.2.7 Baturone Implementation

A different defuzzification method for current-based analog architectures was developed [58-64]. This method uses A/D and D/A converters for division operation. Numerator (input current) and denominator (reference current) are applied to a current-based ADC as shown in Fig.3.12, and digital outputs of this converter are applied into a current-based DAC. By this approach, not only a quantized analog output can be handled, but also the digital equivalent of this value may be taken from the output of ADC. Data processing speed can reach up to only 0,5 MFLIPS with this different divider structure.

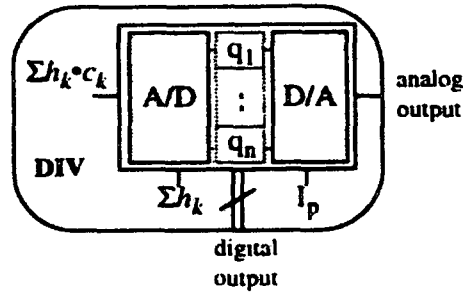


Figure 3.12 Block diagram of the proposed ADC/DAC divider.

3.2.8 Vidal-Verdu Implementation

In [65-67], the key of the proposed strategy lies on the concept of active rules which determine the controller output. The architecture is given in Fig.3.13 which finds the effective rules corresponding to the inputs via an interval selector first and then calculates the output from these rules. By this method, since only the active rules are needed to be taken into account, the analog core is structured on the basis to perform 2^M rules for M inputs instead of L^M , where L depicts the number of the labels in each input (assuming that every input has the same number of membership classes). Digital memory configures the rule block with the consequent singleton values that can be programmed externally.

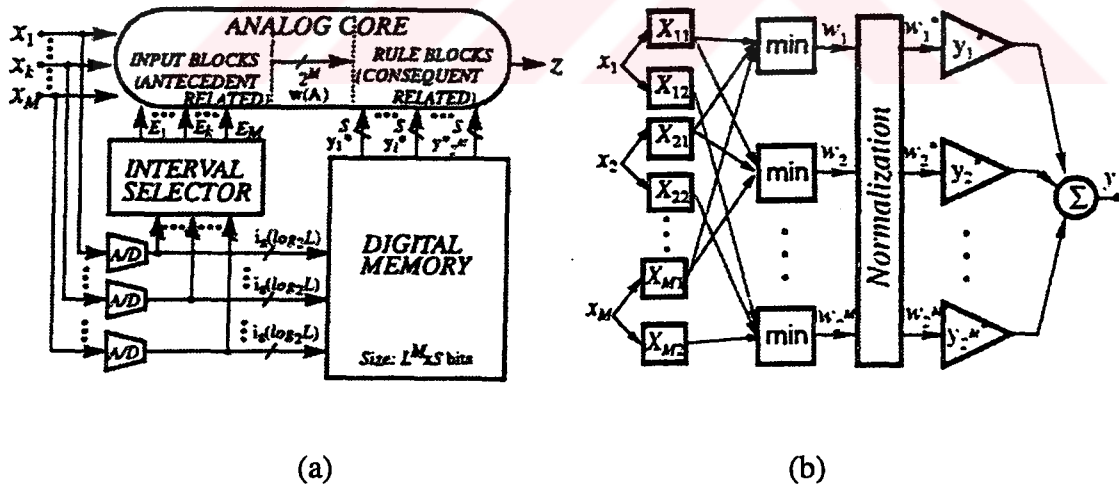


Figure 3.13 (a) General achitecture of the controller, and (b) analog core architecture.

Circuit level implementations of the functional blocks are shown in Fig.3.14. Voltage input is converted into current by the input block and processing of the data is in current-mode in the rest of the controller. A membership function is generated

by a differential pair in an input block as depicted in Fig.3.14 (a). Minimum selection and normalization (which is used for division in the defuzzification) circuits are also shown in the same figure.

A 2-input/1-output/64-rule (8 membership classes per input) 4-bit singleton controller was implemented in 0,7 μm CMOS technology. A/D conversion was implemented with 3 bits. Chip size is 1 mm^2 , power consumption is 16 mW and operation speed is 2 MFLIPS with 1% accuracy.

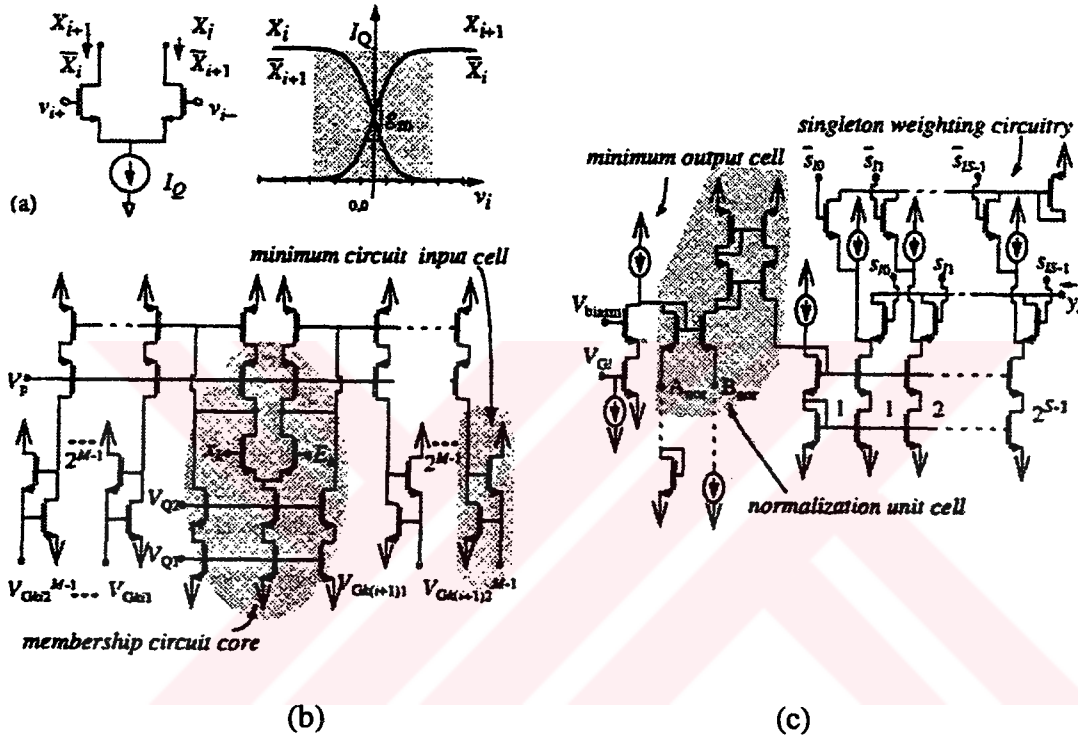


Figure 3.14 (a) Membership function generation, (b) input block, and (c) rule block.

3.2.9 Manaresi Implementation

An OTA-based membership function generator can be found in [68-70]. Quantized analog voltages were employed for programming the membership functions. In this current-based implementation, again OTA circuits were used for defuzzification by connecting all the outputs of multiplier OTA's at the same node as shown in Fig.3.15. Singleton weights (C_i) are applied to one input of the OTA and the other input is used as common output node. The transconductance is tuned by the rule output which determines the tail current; I_{gi} . The total current at the

defuzzifier output should be equal to zero, hence the voltage at this node can be expressed as

$$V_{out} = \frac{\sum_{i=1}^R g_{mi} C_i}{\sum_{i=1}^R g_{mi}}.$$

Although the controller is of a voltage-input/voltage-output type, the data is processed in current mode internally. A 3-input/1-output/15-rule chip was implemented in 0,7 μm CMOS technology. Analog core occupies 2,2 mm^2 , while total chip size is 32 mm^2 . Input and output voltage range is 0V-2V, supply voltage is 5V, power consumption is 45mW and operation speed is reported as 1,6 MFLIPS.

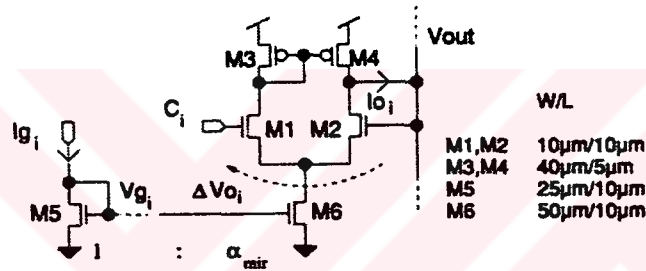


Figure 3.15 OTA based defuzzification in [68-70].

3.2.10 Landolt Implementation

The same defuzzification structure was employed in another implementation [71, 72]. In this study, fuzzification and inference were approached from a different strategy. A direct description of a “fuzzification and inference” subspace may be done by using the concept of distance between the input vector of a fuzzy controller and the center point of the subspace. For instance, the condition in Fig.3.16(a) may be considered an Euclidean measure of proximity, i.e., the complement of an Euclidean distance, which can be depicted in Fig.3.16(b).

For n input, the membership degree with inference (combined input membership degrees) can be written as

$$\mu(x_1, \dots, x_n) = 1 - \frac{(x_1 - A_1)^2}{K_1} - \dots - \frac{(x_n - A_n)^2}{K_n}$$

if the quantity is positive, and

$$\mu(x_1, \dots, x_n) = 0$$

otherwise, where $(x_1, \dots, x_n)$ is the input vector and $(A_1, \dots, A_n)$ is the central position vector. Condition evaluation by this approach for one input is realized by the current-mode circuit given in Fig.3.17. In the circuit, input is represented by I_{in} , position vector by I_A , and parameter K corresponds to I_K . Handling more inputs can be done simply by duplicating the main body and summing the output currents.

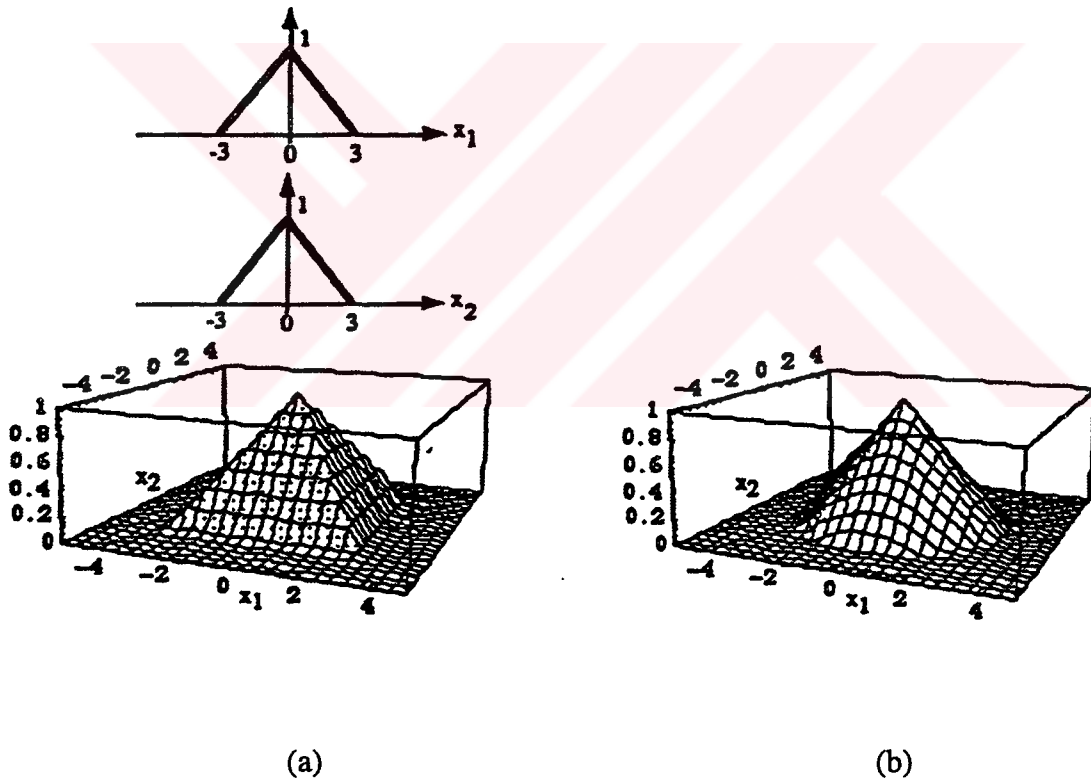


Figure 3.16 (a) Membership function of each single statement and overall degree of truth for the combination (at the bottom), and (b) Euclidean measure of proximity of the condition in (a).

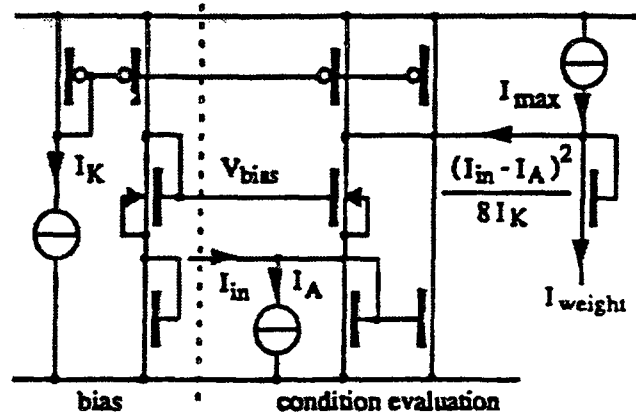


Figure 3.17 Current-mode implementation of the condition evaluation in [71, 72]

3.2.11 Quigley Implementation

A current-based analog fuzzy inference processor has been proposed in [73]. It has adopted the defuzzification strategy given in [74] which calculates center of gravity on trapezoidal consequent membership classes. In this work, only the active rules influence the output. Its 4-rule processor has been designed with OTA based membership function circuits. A normalization circuit configuration and D/A multipliers (normalized currents and the centers of the consequent classes are multiplied in A/D converters), given in Fig.3.18, are utilized for defuzzification. Defuzzification involves trapezoidal consequent classes in which normalized truth value is calculated according to the expression

$$I_{wt} = C(I_C^2 - I_t^2)$$

where C is a factor, I_C is a constant representing unity and I_t corresponds to truth level. Normalized truth value can be taken from the output of the weight circuit which is a derivative of current squaring circuit given in [44].

A complete 2-input/1-output/4-rule (7 classes in each) inference processor was implemented in 2 μm CMOS technology on a 2 mm x 2 mm chip, with the core circuitry occupying 900 μm x 1100 μm . Processing speed can reach 400 kFLIPS. 10V and 5V supply voltages are necessary for the operation.

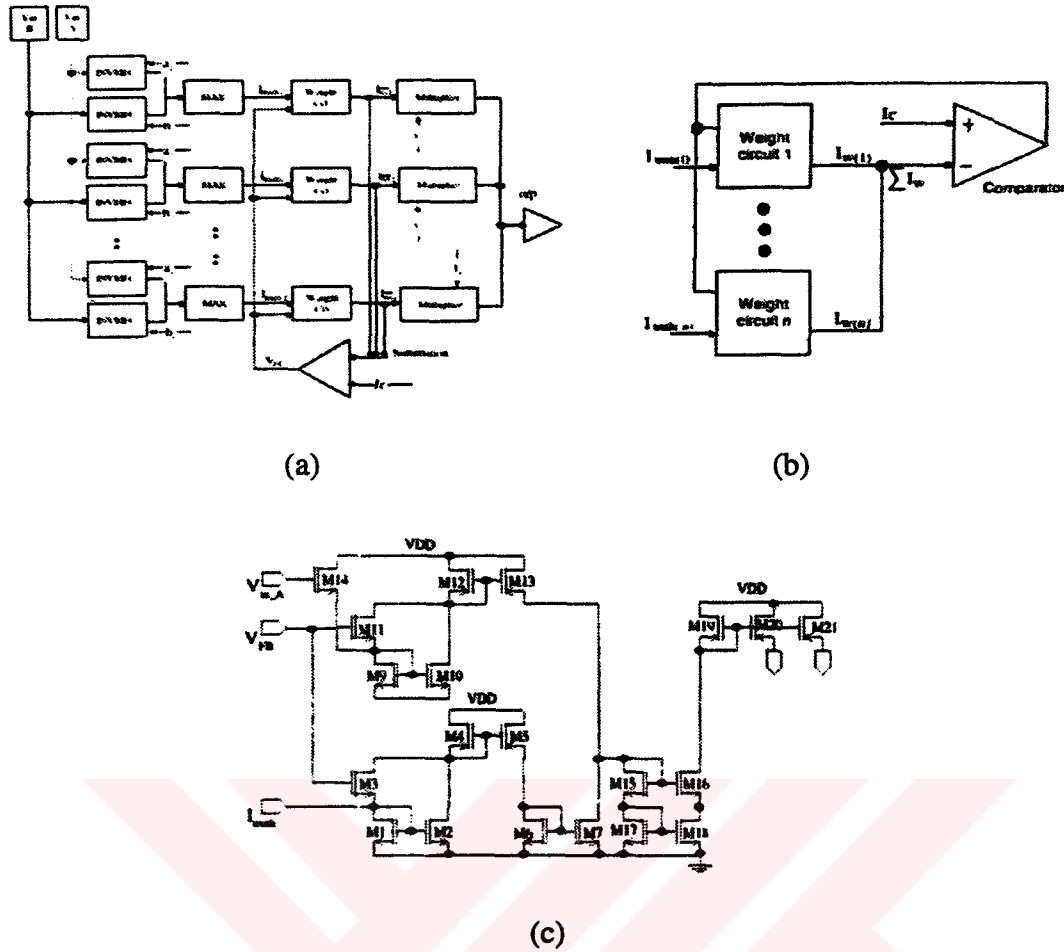


Figure 3.18 (a) Proposed processor architecture, (b) normalization configuration, and (c) weight circuit.

3.2.12 Yamakawa Implementation

A voltage-mode programmable fuzzy controller designed with bipolar junction transistors was presented in [75, 76]. Descriptive configuration of the system is given in Fig.3.19. Fig.3.20(a) shows the membership function generator, involving resistors (r_{E1} , r_{E2} , r_{B1} and r_{B2}) for programming the shape of the generated class and voltage M for determining the label. Fig.3.20 (b) and (c) depict multiple input voltage-based MIN and MAX circuits which guarantee a large fan-out which is very significant in voltage-mode circuits.

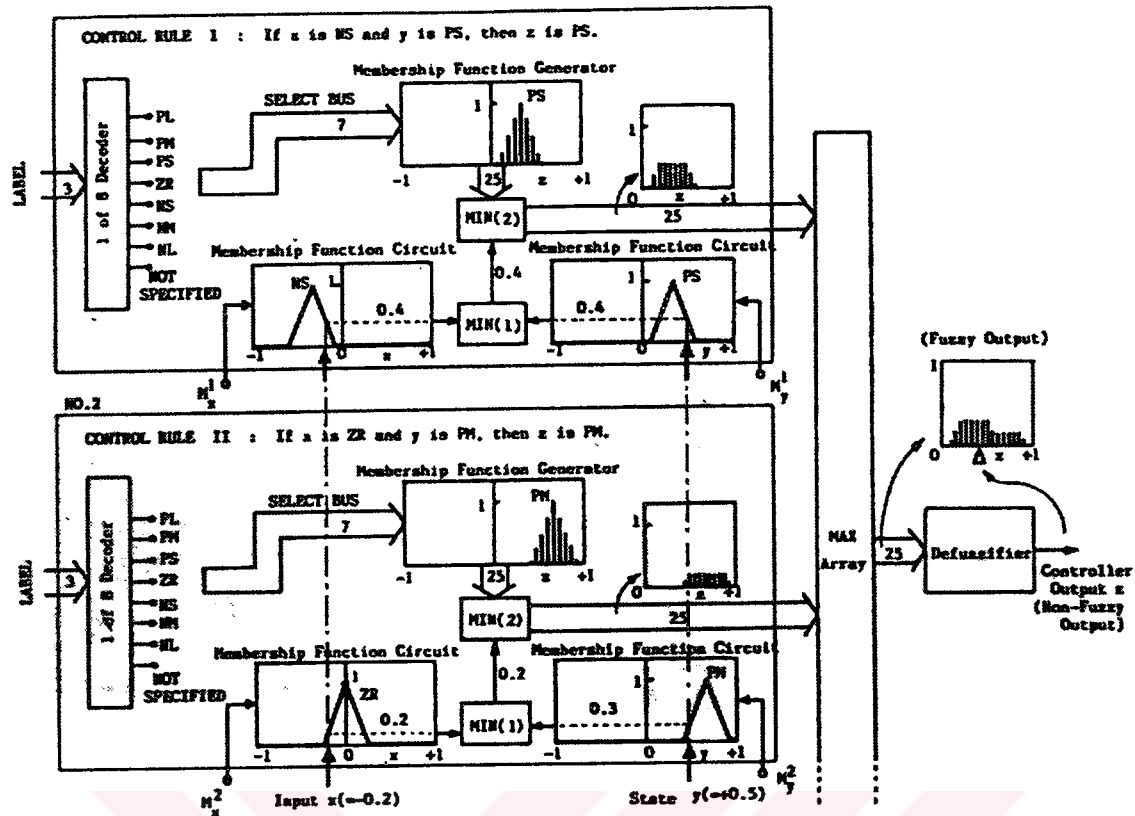


Figure 3.19 Configuration of the proposed system in [75].

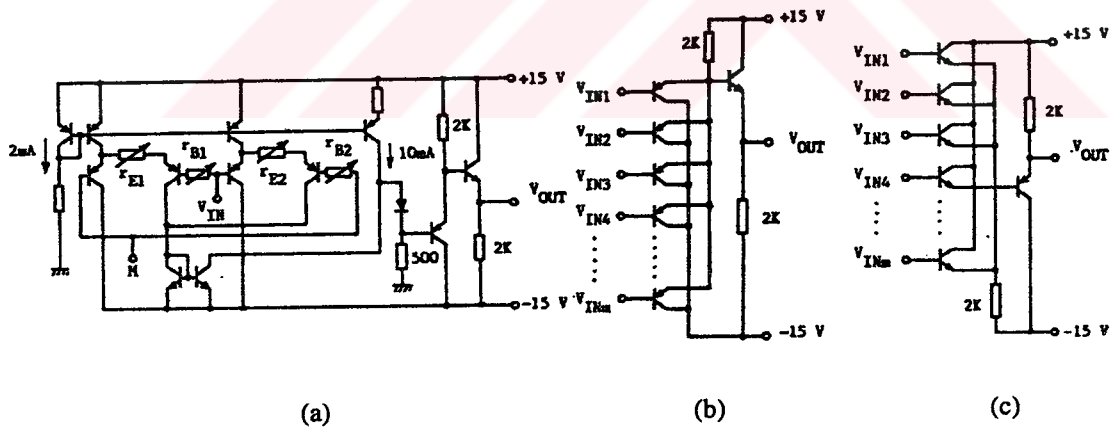


Figure 3.20 (a) Membership function generator, (b) MIN circuit, and (c) MAX circuit.

Membership function generator for consequent classes has 25 output signal lines, a switching matrix and a select bus which is connected to the output of the 1-of-8 decoder is shown in Fig.3.21. The select bus consists of the output class labels.

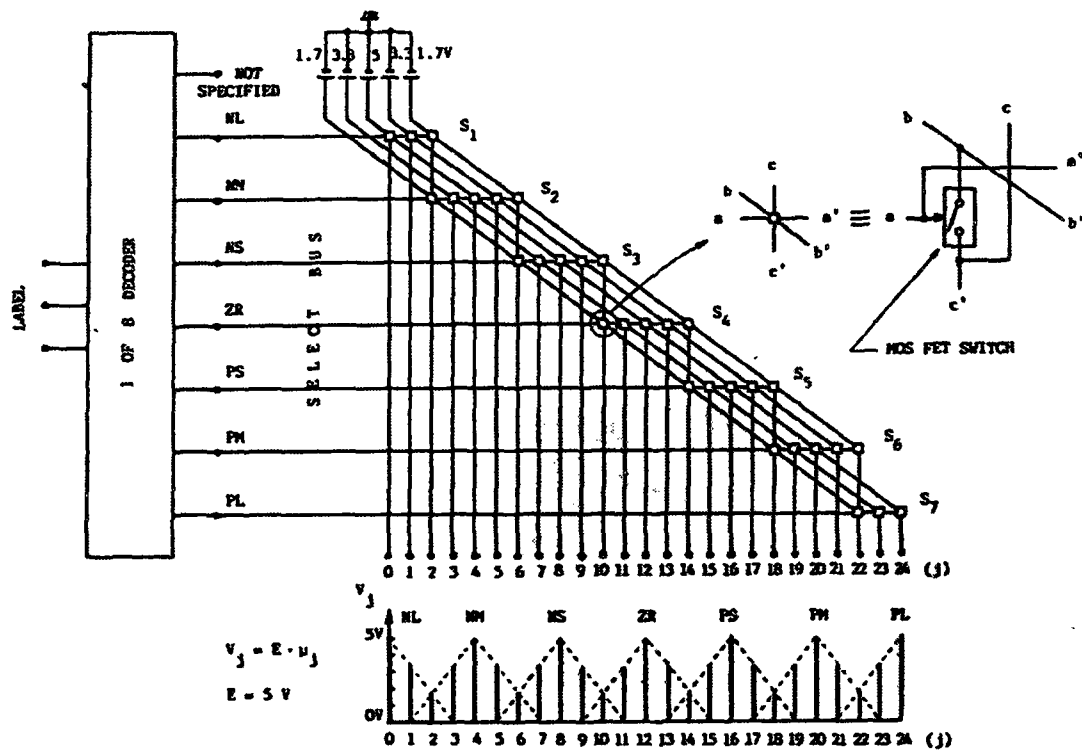


Figure 3.21 Consequent membership function generator.

The defuzzifier in the system fulfills two roles; one is the conversion of 25 parallel signal lines into one signal line and the other is to calculate the crisp output by center of gravity method. Fig.3.22 shows defuzzifier configuration and the current-mode divider employed in it. Divider circuit satisfies the bipolar transistor version of the translinear circuit principle given in [77], so the output current can be expressed as

$$I_4 = K \frac{I_1}{I_2}$$

where K is a scaling factor. This programmable fuzzy controller can achieve a speed of 1 MFLIPS.

A programmable hardware implementation of the style introduced above is given in [78] with some differences in membership function generation and in application of defuzzification. In this case, input membership classes are constructed by combining negative and positive ramps. The circuit schematic of a positive ramp is shown in Fig.3.23. Defuzzification is done over 7 output singletons instead of 25.

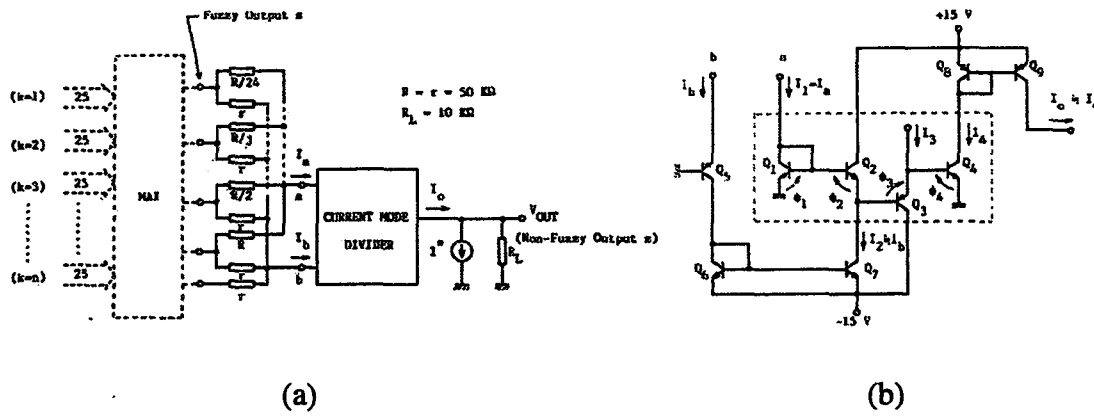


Figure 3.22 (a) Defuzzifier configuration and (b) current-mode divider.

Two separate chips were implemented; one for inferencing and one for defuzzification. The rule chip was implemented with $2 \mu\text{m}$ BiCMOS technology on a $11 \text{ mm} \times 10.9 \text{ mm}$ area by including digital programming units. The fuzzy grade of membership $[0,1]$ corresponds to the voltage range of $[5\text{V}, 7.5\text{V}]$ while the analog input voltage as a universe of discourse ranges from 2.5V to 7.5V . Rule chip works with 5V and 10V supply voltages and uses a 2.5V reference voltage. The hardware contains 3 inputs with which can generate up to 7 classes and executes 4 rules.

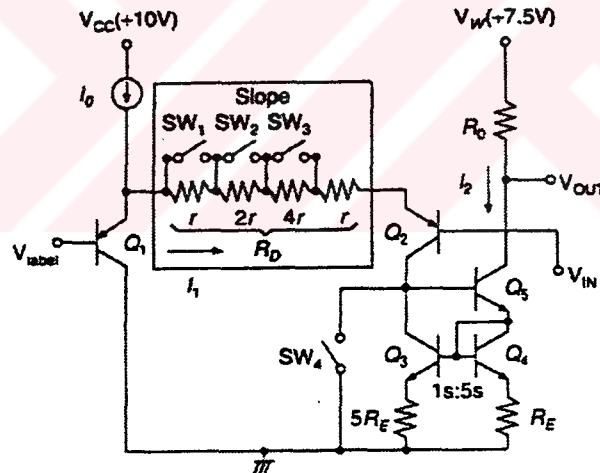


Figure 3.23 Proposed positive ramp function circuit in [78].

The defuzzifier chip was implemented on a $3.4 \text{ mm} \times 2.9 \text{ mm}$ area with $3 \mu\text{m}$ bipolar technology. The output classes are formed with 7 singletons. Input voltage ranges from 5V to 7.5V corresponding to $[0,1]$, and output voltage can vary between $[2.5\text{V}$ to $7.5\text{V}]$. This chip also works with 5V and 10V supply voltages. Operation speed of the controller can reach up to 600 kFLIPS.

3.2.13 Tsukano Implementation

An OTA based voltage-mode realization and its building blocks were introduced in [79-82]. In this study, complementary operations on membership functions and maximum selection are adopted which are based on bounded difference equations. Block schematics of the circuits are illustrated in Fig.3.24.

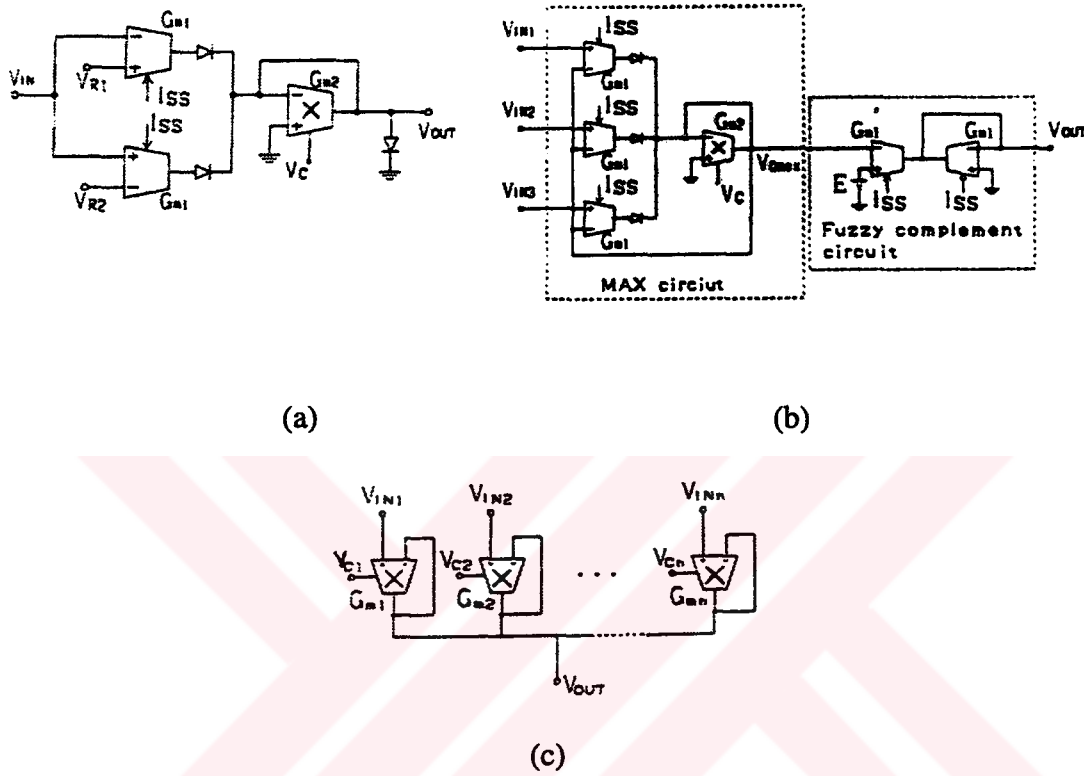


Figure 3.24 OTA based; (a) Complementary membership function, (b) complementary MAX function, and (c) defuzzifier circuits.

A 2-input (3 classes per each) and 1-output (9 classes) controller with 9-rule was synthesized. Simulation results have shown 1,6 MFLIPS operation speed, 28.2mW power dissipation and 8,2% full-scale error with power supplies +5V and -5V. Input and output ranges were set to [0V, 0,2V] and [0V, 0,9V], respectively. This realization has some disadvantages, which can be summarized as i) narrow dynamic ranges of input and output voltages and internally process signals (within 900mV), ii) a large number of externally applied analog voltages with very high resolution, as required by OTA biasing, iii) sensitivity of operation point conditions to device dimensions, and iv) large amount of nonlinearity observed in both simulation and measurement results.

3.2.14 Solano Implementation

Some switched-capacitor based singleton fuzzy-controller building blocks have been introduced in [83, 84]. Architecture and the circuit schematics of basic blocks are shown in Fig.3.25. In the first phase, input X and parameter voltage V_c are compared in the membership function circuit. The output of the circuit is generated in the following phase. m represents the slope of the trapezoid and it is determined by capacitor ratios.

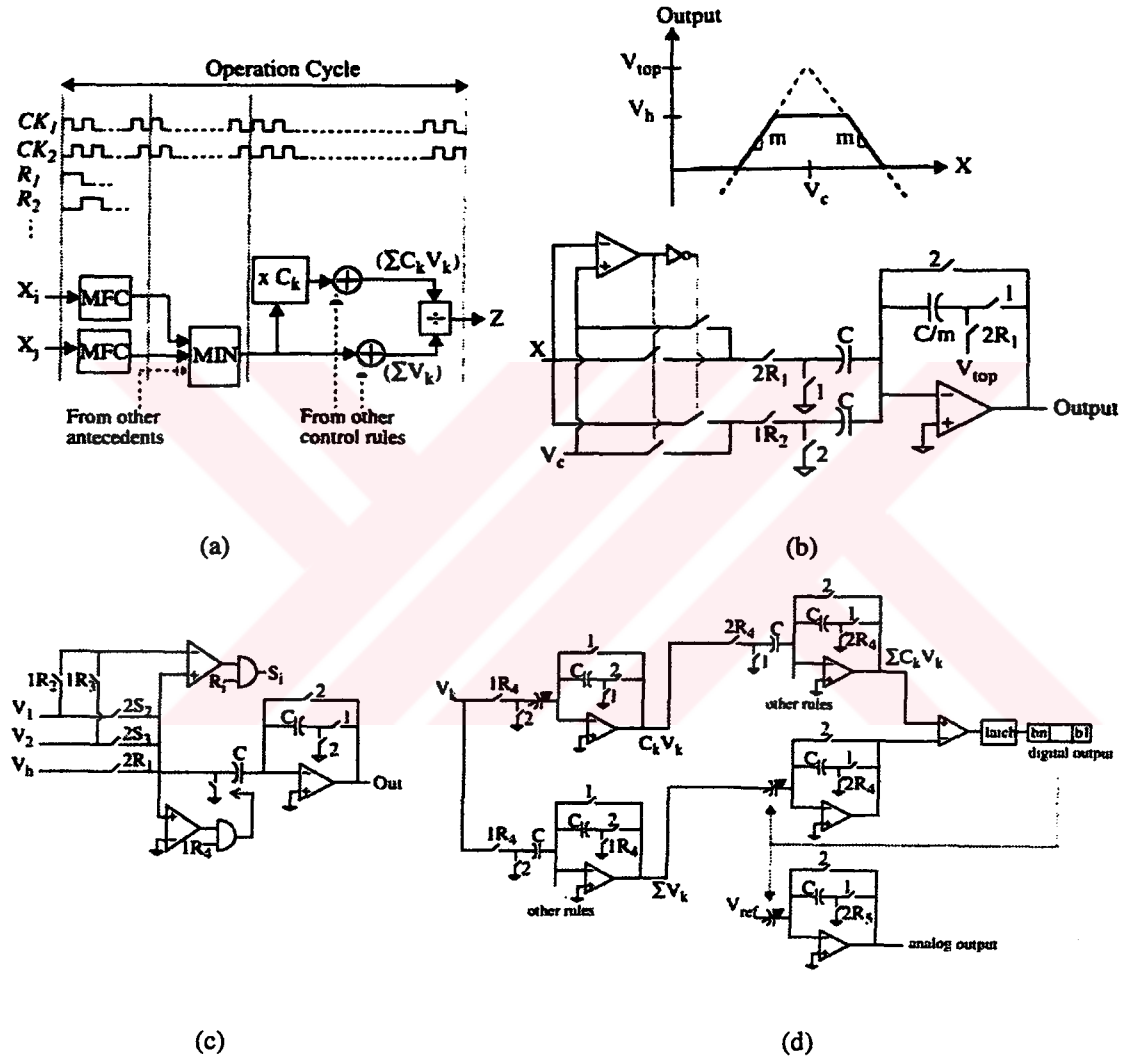


Figure 3.25 (a) Architecture of the proposed controller, (b) trapezoidal membership function and its generator, (c) MIN serial operator for two inputs, and (d) final stage circuit.

Input voltages are compared sequentially with that stored in capacitor C in MIN circuit, meaning that response time increases with the increasing number of inputs. If the input voltage is less than the stored value, the corresponding switch is closed and the new value is stored. Otherwise, the stored voltage is not modified. In

the final block, values of C_k are digitally programmed as capacitor ratios. After finding the two sums an A/D converter is employed as divider. For the analog output a D/A converter is used. Hence, both digital and analog signals are available at the output.

A 1-input/1-output function approximator (a function approximator finds the value of the function, for instance, $f=\sin(x)$ for given value of x , which can be used instead of function calculators or look-up tables) with 4-rule was implemented with 2,4 μm CMOS technology. 5-b converters were used with 3% absolute error. The chip occupies 3,4 mm^2 area without pads and the speed of the approximator has been reported as 250 kFLIPS. Note that, no minimum selection operation is necessary for this application.

3.2.15 Fattaruso Implementation

Another voltage-mode fully programmable analog fuzzy controller implemented by switched-capacitor circuits can be found in [85]. Input membership functions are realized by switched-capacitor DAC configurations which is shown in Fig.3.26. Four corner points of a trapezoidal membership function are stored in a RAM with 6-b resolution. These words are used to program binary-weighted capacitor sets. Maximum selection circuit is also given in Fig.3.26. Note that only the opamp having maximum voltage at its input will be in the linear region and the rest will be saturated. Center of gravity calculation in defuzzification is accomplished by an ADC shown in the same figure. The 6-b digital output word is stored in a successive approximation register.

The switched-capacitor techniques described in previous paragraphs have been employed in a controller design which can be configured up to 8-input/4-output/32-rule including 7 classes in each variable. The design has been implemented on a 7 mm by 10 mm chip in 0,8 μm CMOS technology. Simulated speed is about 500 kFLIPS [85].

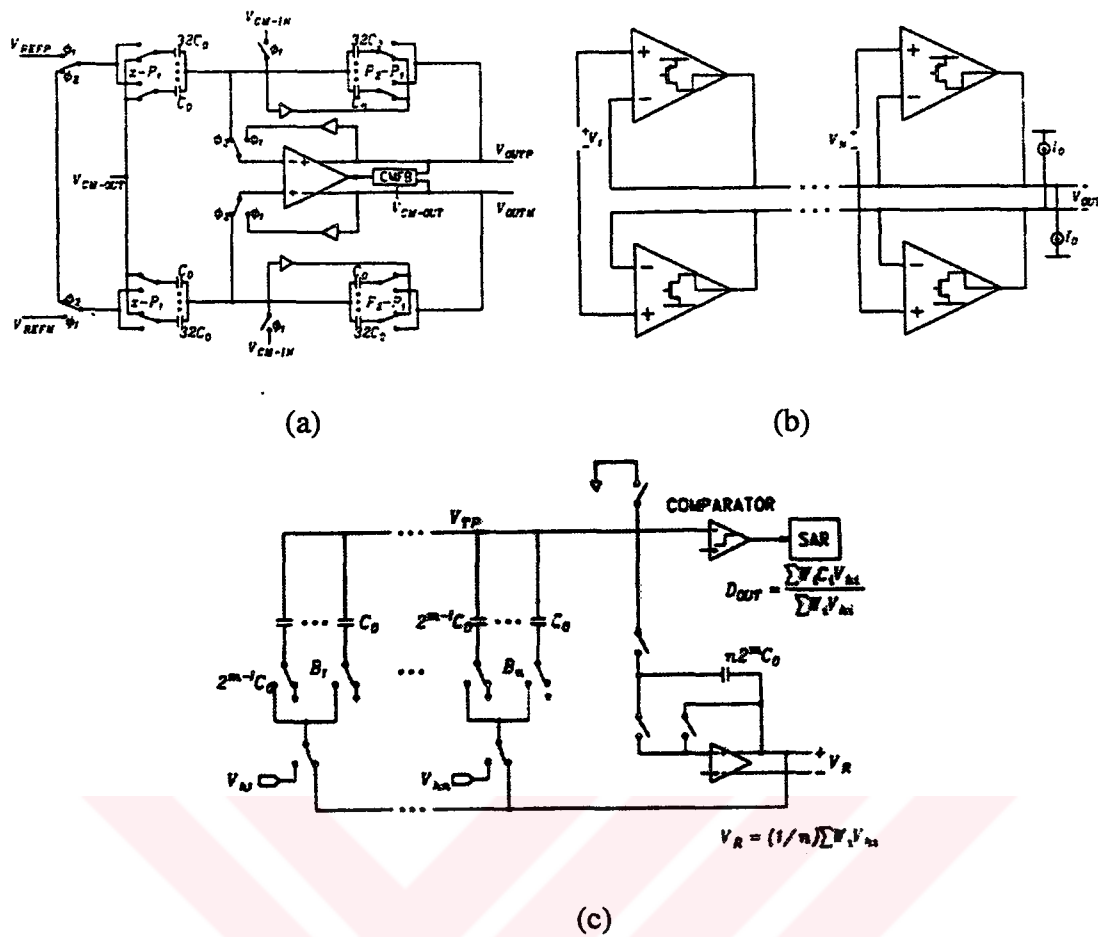


Figure 3.26 (a) Switched-capacitor DAC for to generate a membership function, (b) maximizer, and (c) center of gravity calculator, in [85].

3.2.16 Guo Implementation

A different fuzzy controller and its basic building blocks implemented with voltage-mode circuits were reported in [86-90]. A membership function circuit, minimum and maximum selection circuits and defuzzifier configuration are given in Fig.3.27. Trapezoidal membership function circuit can be adjusted by analog voltages. Rule selection is possible by programming the multiplexers, and consequent singleton classes may be tuned by analog voltages in the proposed architecture. Each of min and max circuit has an offset about the threshold voltage of a MOS transistor, but, during the serial processing of analog data it is possible to compensate for this offset because the threshold voltages of NMOS and PMOS transistors are of opposite signed. Employed strategy for defuzzification was explained previously which relies on the current nulling at the common output node of the transconductance amplifiers as shown in the same figure.

To confirm the performance of the presented architecture, a reconfigurable controller with 3-input (3-class), 1-output (5-singleton) and 13-rule was fabricated with 2,4 μm CMOS process. The controller occupies 3,6 x 4,5 mm^2 area. By using two (+5V and -5V) supply voltages it consumes 550mW and it reaches a speed of 6 MFLIPS.

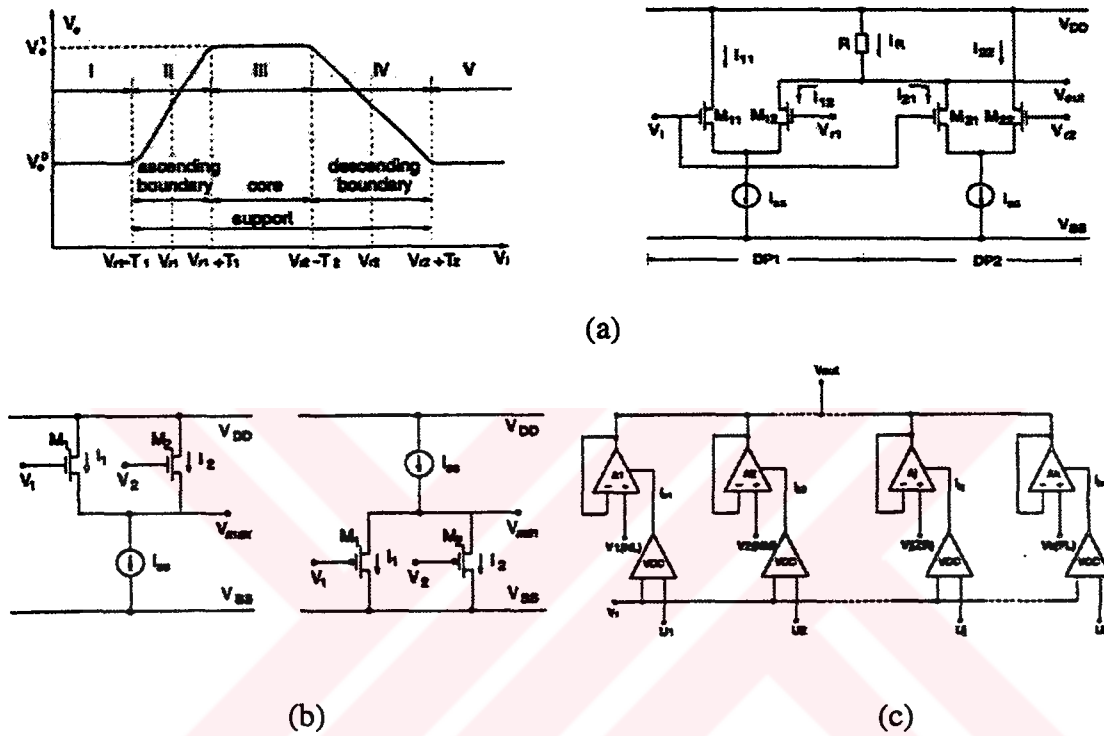


Figure 3.27 (a) Described membership function and the circuit generates it, (b) basic min and max operators, and (c) defuzzifier configuration.

3.2 17 Tsividis Implementation

A mixed-signal programmable fuzzy controller including both analog current and voltage mode circuits was presented in [91]. Programmable membership function generators which can specify triangular and trapezoidal functions contain OTA based circuits and the defuzzifier calculates the center of gravity. Operation of an inference unit is based on sequential sampling of the inputs as shown in Fig.3.28. Three inputs are processed sequentially starting from the first, and the linear sweep signal is used by the defuzzifier. At the end of the process, the circuit finds the minimum of the inputs and generates a rule output current. As can be seen IF clause output is in the form of current and it is converted to voltage prior to defuzzification.

Continuous analog components of the defuzzifier are integrator, multiplier, divider and I-V converter. Rule programming is accomplished via a switching matrix.

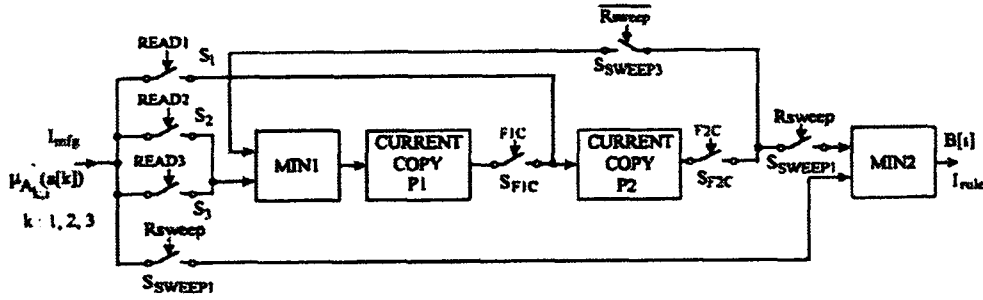


Figure 3.28 An inference unit proposed in [91].

A sample controller was fabricated in 0,7 μm CMOS technology, containing 3 inputs, 1 output (5 classes in each) and 5 rules. Two separate chips; one for inference and one for defuzzification have been implemented. Memory and timing blocks have not been integrated at this time. Input and output ranges of the controller are limited to the interval $[-1\text{V}, 0\text{V}]$. Supply voltages are +2,5V and -2,5V. The controller can reach 21 kFLIPS. Inference and defuzzification circuits occupy 1,68 mm^2 and 2,4 mm^2 silicon area, respectively.

3.2.18 Catania Implementation

Mixed analog-digital circuits were employed for the execution of the fuzzy operations in [92, 93]. In the presented architecture, first, the membership degree is determined by a quantizer which finds the digital word corresponding to one of 8 discrete analog voltage levels for given input, and then, this digital data is processed digitally through inferencing. The following defuzzification is achieved by converting these digital data into currents, and a current based divider with an I/V converter finally yields a crisp output as a voltage. No clear information about the area and speed can be found in the publications.

3.2.19 Other Implementations

Some basic building block circuits for fuzzy controllers have been given for BiCMOS technology in [94-97], but no sufficient information about either simulation results or hardware implementation can be found in these publications. A dynamic

current adder structure and a tunable CMOS membership function circuit can be found respectively in [98], and [99] but supported with very limited information.

A digital-like architecture but with current-based circuits implemented fuzzy logic microprocessor was introduced in [100]. Configuration is very similar to digital ones, but the operations are executed by analog CMOS current-based circuits instead of digital circuits. Voltage inputs are first converted into 2-b currents, and then current mirror-based circuits, which have been introduced before, are employed for the operations. It has been estimated that the operation speed could reach 1 MFLIPS by 2 μm CMOS technology.

An application-specific fuzzy controller was implemented with the proposed switched-capacitor circuits in this study. The dedicated configuration of this chip is 4 input, 2 output and 16 rules. It contains a total of 11 input and 7 output classes. The proposed fuzzifier architecture can generate ramp, triangular or trapezoidal input membership classes. The defuzzifier calculates weighted-average of singletons (center-of-gravity) by using a quantized divider. Inference engine executes the rules defined by AND connective. The voltage-mode data are processed totally analog along the entire controller. The chip occupies 1.76 mm^2 with 1.2 μm CMOS technology. The controller can reach 85kFLIPS. It uses 5V supply voltage for the operation and consumes 50mW.

Features of fully integrated controllers, including the one designed with the proposed sampled-analog approach in this study, are summarized in Tables 3.3 and 3.4. Digital implementations are given in Table 3.3 and analog implementations are given in Table 3.4. Digital implementations mostly occupy larger silicon area than analog ones. Typically, current-based analog implementations occupy smaller areas and they are faster than voltage-based ones. Three basic circuit structures are utilized in both current-based and voltage-based implementations, i) current mirror circuits, ii) circuits constructed with OTAs, and iii) switched-capacitor circuits. Linearity, accuracy and independency of operation point conditions on supply voltage and temperature of current mirror and OTA circuits are considerably poor. Since high gain amplifiers utilized in switched-capacitor circuits are generally used under feedback, and transfer characteristics of basic modules are determined by capacitor ratios, these circuits have more accurate characteristics and their supply voltage and

temperature independencies are better. Voltage-based implementations usually use more than one power supply. Rail-to-rail functionality can not be encountered in any reported voltage-based implementation. Their external and internal dynamic ranges are very limited.

Voltage-based switched-capacitor circuits we proposed uniquely have the rail-to-rail functionality and they use one power supply only. Accuracy and linearity characteristics of our modules are much better than most of both current-based and voltage-based implementations summarized in the Table 3.4. Additionally, supply voltage and temperature dependencies are very weak, because the operation point conditions of high gain amplifier we use in basic building blocks are almost totally independent of the fluctuations in supply voltage and temperature. Moreover, dimensional deviations in devices originating from the process can not affect the operation of this amplifier. The occupied area are smaller than most of the implemented controllers listed in the above mentioned table. The approach we proposed will be examined in the next chapters.

Table 3.3 Digital implementations

Implementation	Input space	Output space	Internal resolution	Rule Count	I/O Count	Area [mm ²] Technology	Speed [kFLIPS]	Power, Supply	Error %
Togai&Watanabe Programmable	31 quanta	31 quanta	4-b	16	1 in/1 out	10.4	80	-	-
Watanabe Programmable Reconfigurable	64 quanta	64 quanta	4-b	51 102	4 in/2 out 2 in/1 out	70.1 1.1 μ CMOS	580	1.2W, 3V	-
Jimenez Programmable	64 quanta	64 quanta	4-b	4	3 in/1 out	14.4 1 μ CMOS	3000	-	8
Jimenez Programmable	64 quanta	64 quanta	4-b	4	3 in/1 out	12.5 1 μ CMOS	2770	-	8

Table 3.4 Analog implementations

Implementation	Rule Count	I/O Count	Area [mm ²] Technology	Speed [kFLIPS]	Power, Supply	Error %
Lemaitre Current-based	9	2 in/1 out	0.4 1.2 μ CMOS	10000	10mW, 5V	-
Huertas Current-Based	9	2 in/1 out	1 2.4 μ CMOS	2000	-	1.5
Vidal-Verdu Current-Based	4	2 in/1 out	1 0.7 μ CMOS	3000	16mW	1
Manaresi Current-Based	15	3 in/1 out	32 (core 2.2) 0.7 μ CMOS	1600	45mW, 5V	-
Quigley Current-Based	4	2 in/1 out	4 2 μ CMOS	400	- 5V, 10V	-
Yamakawa Voltage-Based	4	3 in/1 out	130 2 μ BiCMOS	600	- 5V, 10V	
Solano Voltage-Based	4	1 in/1 out	3.4 2.4 μ CMOS	250	-	3
Fattaruso Voltage-Based	32	8 in/4 out	70 0.8 μ CMOS	500	-	-
Guo Voltage-Based	13	3 in/1 out	16.2 1.2 μ CMOS	6000	550mW, +5V, -5V	
Tsividis Current & Voltage-Based	5	3 in/1 out	4.1 0.7 μ CMOS	21	- +2.5V, -2.5V	8
Proposed sampled-analog Voltage-Based	16	4 in/2 out	1.76 1.2 μ CMOS	85	50mW, 5V	10

4. THE PROPOSED SAMPLED-ANALOG APPROACH

In this chapter, we introduce a new fully analog hardware implementation style for fuzzy controllers. The approach differs from continuous current or voltage based realizations presented in Section 3.2, in that, it suggests sampled-analog techniques for the basic building block circuits of a complete fuzzy controller instead of continuous time structures. Inputs and outputs are in the form of analog voltages which provide a natural compatibility to the voltage mode sensors and actuators, and internal data are processed also in voltage mode, thus, no type of external and/or internal conversion is not needed for the operation.

4.1 Fuzzy Controller Architecture

A typical fuzzy logic controller primarily consists of three basic building blocks: a fuzzifier, an inference engine and a defuzzifier. The architectural schematic of the proposed sampled-analog fuzzy logic controller is shown in Fig. 4.1.

In a sampled-analog system, continuously varying analog input data should be sampled and held before being processed. For that reason, Sample/Hold blocks are utilized prior to fuzzification in this realization. There is one S/H module for each input. A fuzzifier module converts the value of a crisp input (I) into a fuzzy membership class grade (M). There is one fuzzifier module for each membership class. An inference module accomplishes the “AND” operation, so finds the minimum (T) among the membership grades ($M_1, \dots, M_m$). Here, T is the truth value of a rule and $M_1, \dots, M_m$ are the grades on the fuzzy input membership classes associated with that rule. There is one inference module for each rule. A defuzzifier module calculates the weighted-average of singletons using the truth values of the rules ($T_1, \dots, T_n$) and the singleton output classes included by an output (O). The membership degree of each singleton output class is the truth value associated with

this class in a rule. There is one defuzzifier module for each output. Contents of these modules will be the subjects of the following sections.

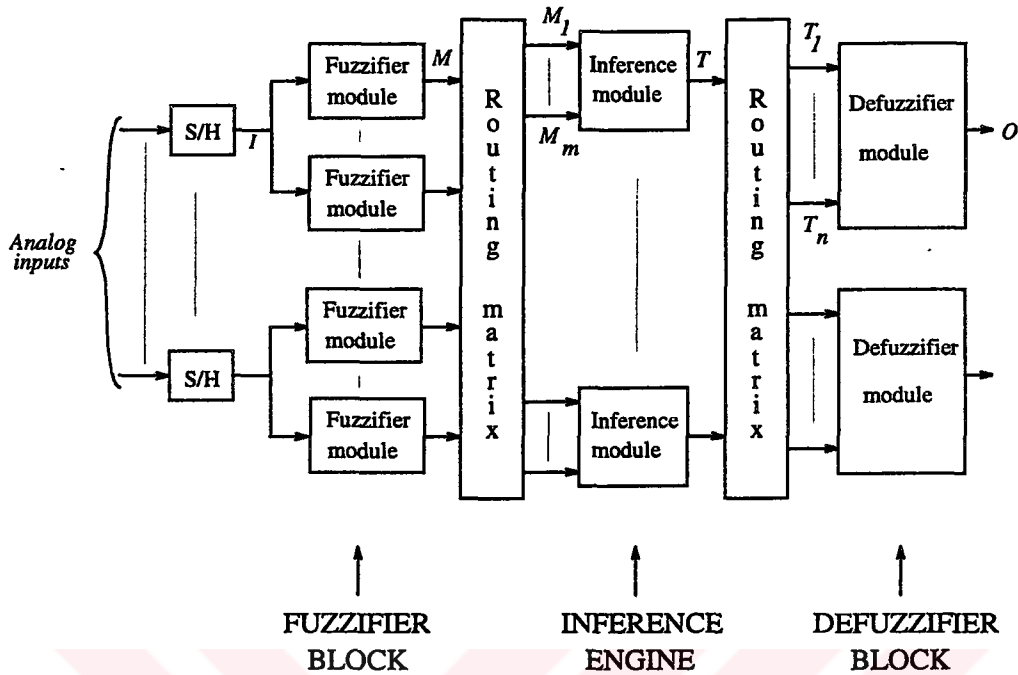


Figure 4.1 Block diagram of the proposed fuzzy logic controller.

Routing matrices, located between successive blocks are used for interconnection purposes. A data-path controller (phase generator) is also necessary for properly processing and shifting data from input to output in a sampled-analog implementation, although it is not included in the figure.

4.2 Fuzzifier

Input membership classes are commonly determined by the expertise on a specific controller. Choosing the shapes of these classes is still heuristic because there is not any fixed method developed up to today for optimally determining the class shapes. However, triangular, trapezoidal or ramp shaped membership classes have been used in almost all hardware-implemented analog fuzzifiers. The above piecewise linear functions are the compositions of the lines under some boundary conditions. For some rare conditions, there is also an option that a nonlinear function, such as Gaussian, can be synthesized with a good approximation by the superposition of the lines [101].

In this study, a fuzzifier module is expected to transform a crisp input value into a membership degree by performing a piecewise linear function. Generally three different functions should be realized. Namely, positive ramp, negative ramp, and trapezoid or triangle. However, it is not necessary to design different individual circuits to implement all these functions, because a triangular or a trapezoidal form can be generated by properly combining a pair of negative and positive ramp functions, as shown in Fig.4.2. In the figure; M_{PR} , M_{NR} , M_{TR} and I denote a positive ramp, a negative ramp, a triangular or a trapezoidal membership function and an input variable, respectively.

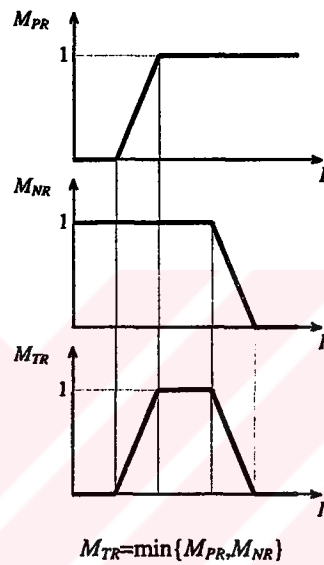


Figure 4.2 Generation of a trapezoid or a triangle by combining two types of ramp functions.

Quite obviously, creation of a triangular or trapezoidal function such as shown in Fig.4.2 necessitates a minimum (min) operation on ramp functions. Fortunately, min operation is available inherently in the inference mechanism. So, the generation of these functions is realized easily by assistance of the inference engine. Note that, any piecewise linear function can be generated by using only these two types of ramp functions, but, inference engine becomes more complicated with the increasing number of the piecewise lines in a membership function.

Fig.4.3 shows a fuzzifier block diagram for an input I . The fuzzifier is the combination of fuzzifier modules, one for each membership class. Every fuzzifier

module belongs to one of the input classes consisting of a pair of one positive ramp and one negative ramp ($V_{M(PR)}$ and $V_{M(NR)}$). Input I has k membership classes. In some specific cases, some of these ramps might be out of use if some classes are ramp-shaped instead of triangular or trapezoidal.

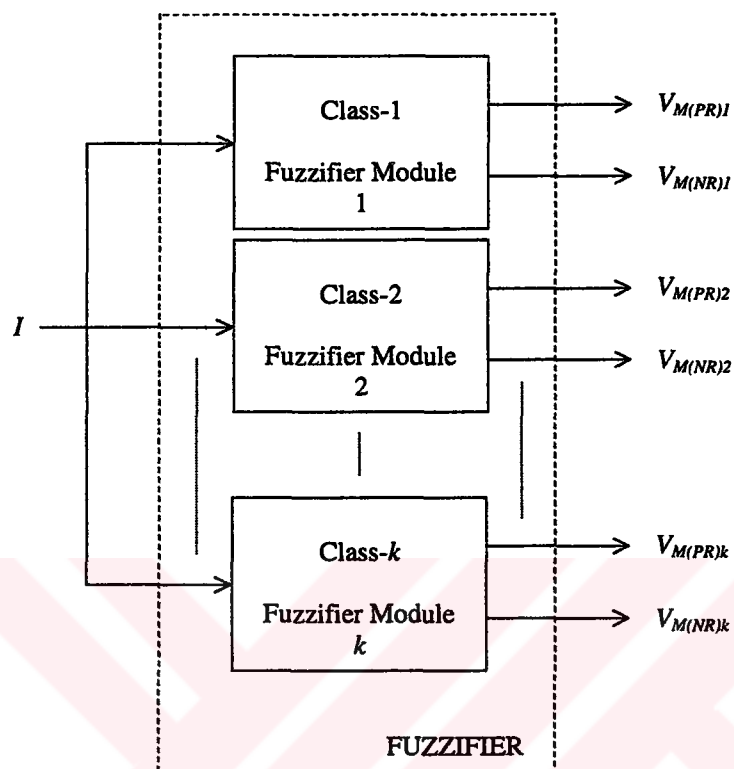


Figure 4.3 Fuzzifier block diagram for an input; I .

All piecewise linear membership functions can be realized solely with positive and negative ramp functions, which are implemented in the present study by using noninverting or inverting switched-capacitor voltage amplifiers. Next subsections will focus on these substructures.

4.2.1 Noninverting Amplifier

A positive ramp function can be implemented with a noninverting amplifier shown in Fig.4.4 (a). It is a derivative of the stray-insensitive switch-capacitor integrator proposed in [102]. With properly selected capacitor values, this configuration can generate an M_{PR} with any grade and any offset.

supply rail levels abruptly around this self-reference level. Fig.4.5 represents the dc transfer characteristic of OPI.

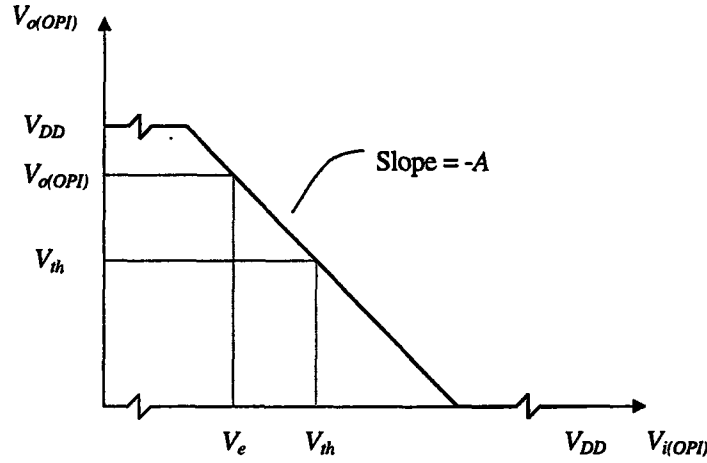


Figure 4.5 Representative dc transfer characteristics of OPI.

Noninverting amplification is achieved by using two-phase sequential nonoverlapping clock signals as depicted in Fig.4.4(b). The first phase is for resetting. During this phase input and output voltages of OPI are reset to its self-reference level V_{th} by a turned-on NMOS switch transistor depicted in the figure as S_R . Top plates of the capacitors are always connected to OPI's input node. In this phase, bottom plates of C_2 and C are tied to ground by NMOS switches while the bottom plate of C_1 receives the input (V_I) via an analog switch consisting of an NMOS/PMOS pair. Analog switch at the output isolates the output load from the circuit during resetting and it is turned on later during the final evaluation phase.

The charge, accumulated at the input node of OPI at the end of this resetting time interval, can be written as

$$Q_r = (V_r - V_I)C_1 + V_r C_2 + V_r C. \quad (4.1)$$

where V_r is the reset voltage at the input of OPI given as

$$V_r = V_{th}. \quad (4.2)$$

After the reset phase is over an evaluation phase begins. Since the resetting feedback from the output to the input of OPI is removed, the input node of OPI enters a high-

impedance state in the evaluation. For this reason, this node is unable to vary the value of the charge accumulated during resetting. In the evaluation mode of operation, the bottom plate of C_1 is connected to ground by an NMOS, that of C_2 is tied to V_{DD} by a PMOS switch, and that of C is connected to the output of the amplifier by an analog switch. A closed-loop operation is established via capacitor C . During this phase, the charge can be expressed as

$$Q_e = V_e C_1 + (V_e - V_{DD})C_2 + (V_e - V_{o(OPI)})C \quad (4.3)$$

which must be equal to Q_r . V_e denotes the new voltage which occurs at the input node in the evaluation phase. This voltage is assumed to be different from V_{th} (with the exception of the unique case; $V_{o(OPI)} = V_{th}$).

As a result of charge preservation, equality of Q_r and Q_e gives

$$(C_1 + C_2 + C)V_r - C_1 V_I = (C_1 + C_2 + C)V_e - C_2 V_{DD} - C V_{o(OPI)}. \quad (4.4)$$

Arrangement of the equation yields

$$V_{o(OPI)} = \frac{C_1}{C} V_I - \frac{C_2}{C} V_{DD} - \frac{(C_1 + C_2 + C)}{C} (V_{th} - V_e). \quad (4.5)$$

The perturbation $V_{th} - V_e$ at the input of OPI can be related to the perturbation $V_{o(OPI)} - V_{th}$ at the output via the transfer characteristic depicted in Fig.4.5:

$$V_{o(OPI)} - V_{th} = -A(V_e - V_{th}), \quad (4.6)$$

and, therefore,

$$V_e = -\frac{V_{o(OPI)} - V_{th}}{A} + V_{th}. \quad (4.7)$$

By substituting (4.7) into (4.5) we arrive at

$$V_{o(OPI)} = \frac{C_1}{C} V_I - \frac{C_2}{C} V_{DD} - \frac{(C_1 + C_2 + C)}{AC} (V_{o(OPI)} - V_{th}), \quad (4.8)$$

and by assuming that the gain $-A$ is sufficiently high, valid output of the noninverting amplifier at the end of the evaluation can be expressed as

$$V_{M(PR)} = \frac{C_1}{C}V_I - \frac{C_2}{C}V_{DD} \quad \text{for} \quad V^- \leq V_I \leq V^+, \quad (4.9)$$

where

$$V^- \equiv \frac{C_2}{C_1}V_{DD} \quad \text{and} \quad V^+ \equiv \frac{C+C_2}{C_1}V_{DD}. \quad (4.10)$$

It is obvious that for the rest of the input space the OPI saturates at the following levels:

$$V_{M(PR)} = GND \quad \text{for} \quad V_I \leq V^-, \quad (4.11a)$$

$$V_{M(PR)} = V_{DD} \quad \text{for} \quad V_I \geq V^+. \quad (4.11b)$$

Therefore, OPI remains nonsaturated for any input voltage in the range $V^- \leq V_I \leq V^+$. Equations (4.9-11) describe a positive ramp function and Fig.4.4(c) shows its characteristics. Note that, the grade and the offset (V^-) of the ramp are determined solely by the capacitor ratios C_1/C and C_2/C_1 , respectively, and saturation levels are determined by the supply voltages; ground and V_{DD} .

The result of an HSPICE transient response simulation for capacitances $C_1=250$ fF, $C_2=100$ fF and $C=100$ fF and supply voltage $V_{DD}=5$ V is given in Fig.4.6. V^- and V^+ , which correspond to these capacitor and supply voltage values, can be calculated as 2V and 4V, respectively. As can be seen from the figure, reset and evaluation phases are completed at the end of every $4\mu\text{s}$. Valid output values can be observed at the end of each period. Open-loop gain of OPI in the simulated configuration is sufficiently high for reliable operation (>80 dB).

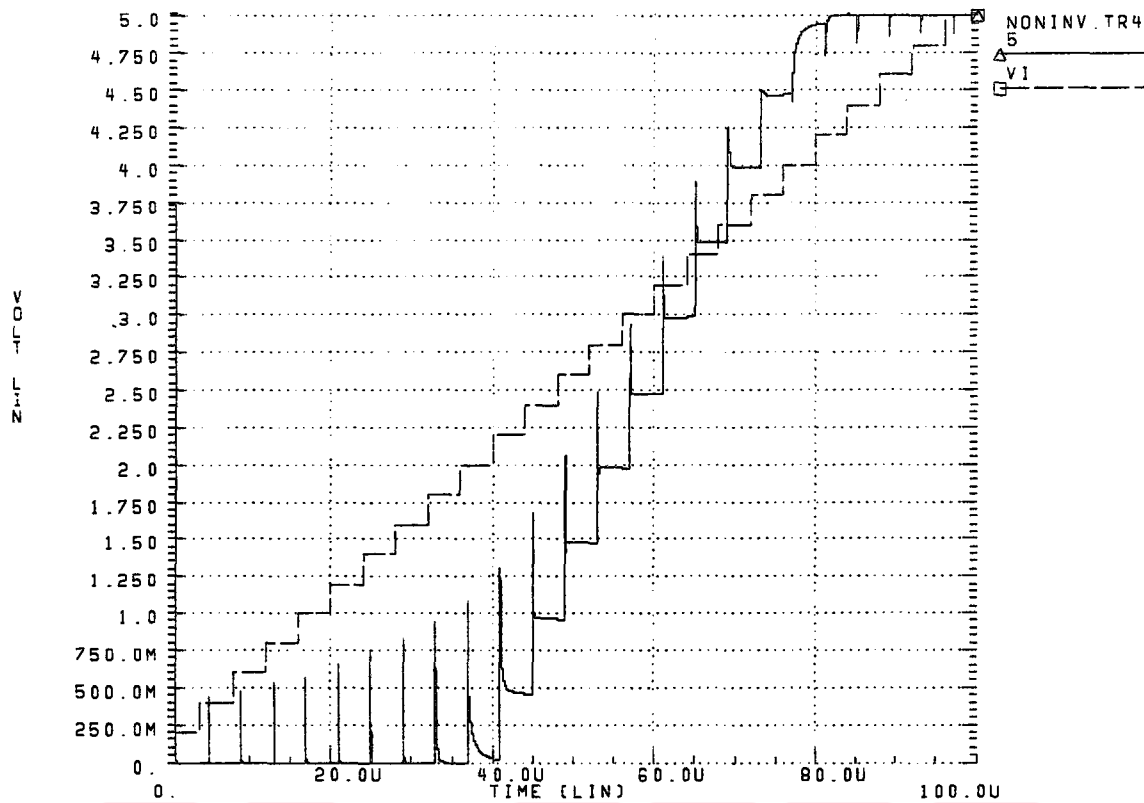


Figure 4.6 Staircase input and the output, transient analysis plots of a positive ramp generator with the capacitor values of $C_1=250\text{fF}$, $C_2=100\text{fF}$, $C=100\text{fF}$ corresponds to the gain boundaries of $V^- \approx 2\text{V}$ and $V^+ \approx 4\text{V}$.

4.2.2 Inverting Amplifier

A negative ramp function is implemented with an inverting amplifier. Configuration of an inverting amplifier is similar to the noninverting one and shown in Fig.4.7(a). It also uses two nonoverlapping clock phases as depicted in Fig.4.7(b).

The voltages, applied to C_1 and C_2 in reset and evaluation phases and the switch transistors are exchanged with respect to the noninverting amplifier schematic given in Fig.4.4(a). The voltage applied to the bottom plate of the capacitor C and its switch transistor are also changed. In the negative ramp generator, the bottom plate of C_1 is connected to ground by an NMOS switch, and those of C_2 and C are tied to V_{DD} by a PMOS switch for each capacitor during the interval of resetting. In the mode of evaluation C_1 receives an analog input via an analog switch, while C_2 is connected to ground by an NMOS transistor and C is tied to the output by an analog switch. The function of the output switch is already known. Very similar analysis given for the

noninverting amplifier can be done for the reset and evaluation phases for this configuration. The charge expressions in these phases can be written as

$$Q_r = V_r C_1 + (V_r - V_{DD})C_2 + (V_r - V_{DD})C \quad (4.12)$$

and

$$Q_e = (V_e - V_I)C_1 + V_e C_2 + (V_e - V_{o(OPI)})C. \quad (4.13)$$

Equality of these two gives

$$(C_1 + C_2 + C)V_r - (C_2 + C)V_{DD} = (C_1 + C_2 + C)V_e - V_I C_1 - V_{o(OPI)}C \quad (4.14)$$

and, hence,

$$V_{o(OPI)} = -\frac{C_1}{C}V_I + \frac{C_2 + C}{C}V_{DD} - \frac{(C_1 + C_2 + C)}{C}(V_{th} - V_e). \quad (4.15)$$

is obtained. By substituting (4.7) into (4.15) for V_e , and assuming OPI has a very high open-loop gain, the output voltage is expressed as

$$V_{M(NR)} = -\frac{C_1}{C}V_I + \frac{C_2 + C}{C}V_{DD} \quad \text{for} \quad V^- \leq V_I \leq V^+ \quad (4.16)$$

where V^- and V^+ are still defined by (4.10). $V_{M(NR)}$ versus V_I characteristics are depicted in Fig.4.7(c). Once again, the gain and the offset are determined by the capacitance ratios C_1/C and C_2/C_1 , respectively. Outside the gain region, the outputs are saturated at the following levels:

$$V_{M(NR)} = V_{DD} \quad \text{for} \quad V_I \leq V^-, \quad (4.17a)$$

$$V_{M(NR)} = GND \quad \text{for} \quad V_I \geq V^+. \quad (4.17b)$$

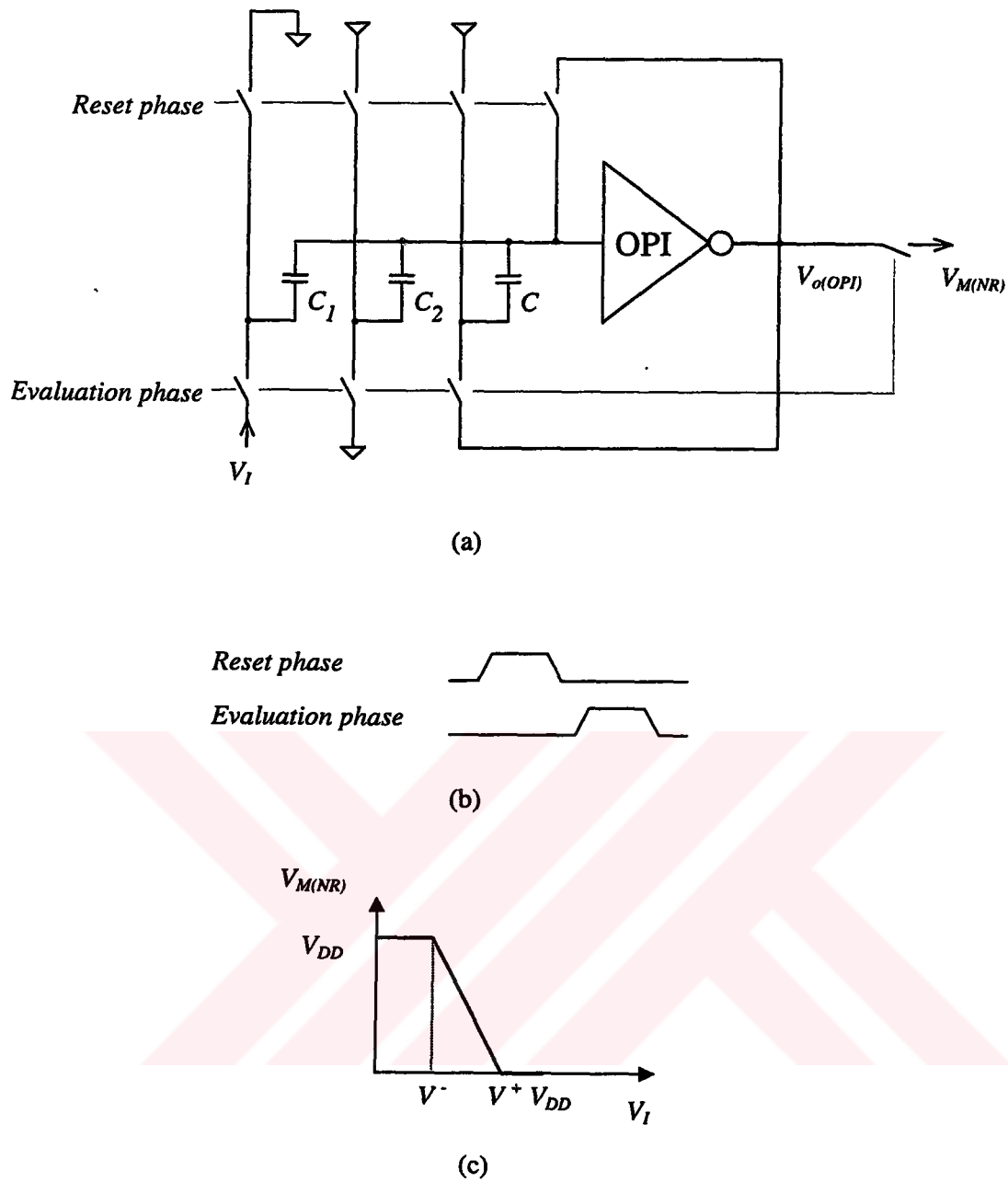


Figure 4.7(a) The circuit schematic of the inverting amplifier, (b) the phases it uses, and (c) the negative ramp that the amplifier generates.

An HSPICE transient response simulation for $C_1=200\text{fF}$, $C_2=50\text{fF}$ and $C=100\text{fF}$, and $V_{DD}=5\text{V}$ supply is depicted in Fig.4.8. The corresponding boundary voltages are $V^- \approx 1.25\text{V}$ and $V^+ \approx 3.75\text{V}$. As can be seen from the figure, reset and evaluation phases are completed at the end of every $4\mu\text{s}$.

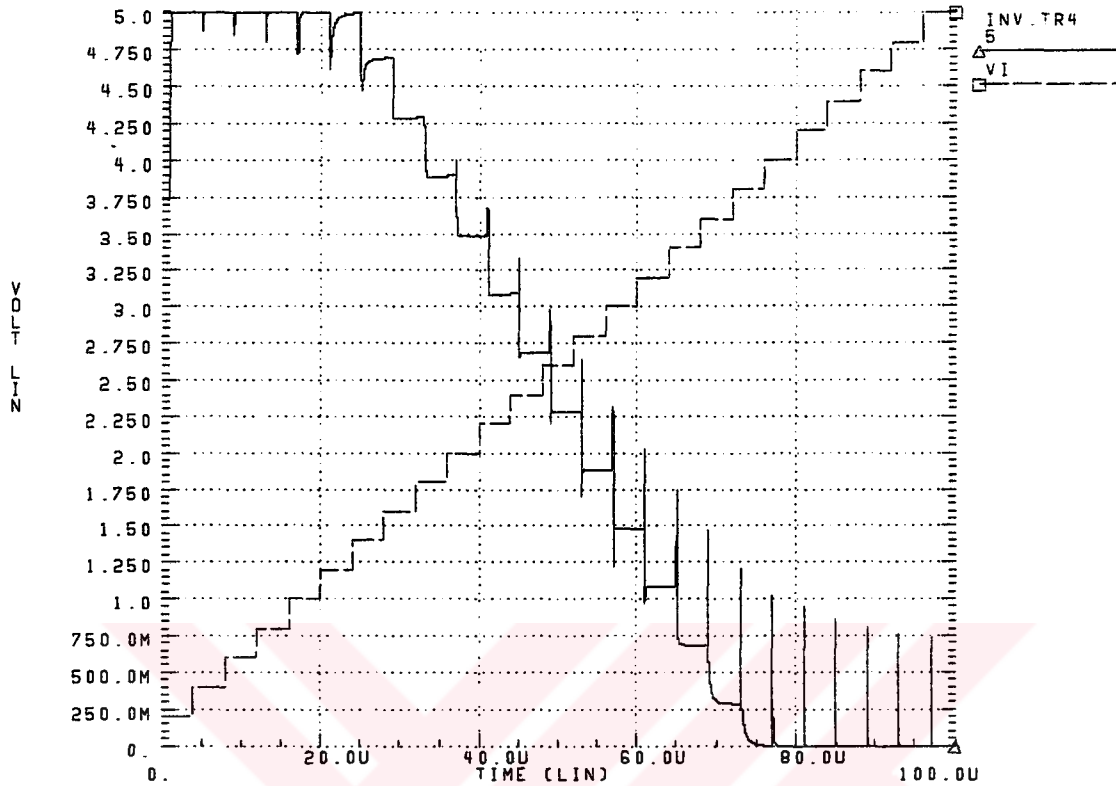


Figure 4.8 Staircase input and the output, transient analysis plots of a negative ramp generator with capacitor values of $C_1=200\text{fF}$, $C_2=50\text{fF}$ and $C=100\text{fF}$ corresponds the gain boundaries of $V^-=1,25\text{V}$ and $V^+=3,75\text{V}$.

4.2.3 Sample and Hold Circuit

Noninverting amplifier receives an input in the reset phase since it is also a sampling circuit, but the inverting one not only receives an input but also generates an output in the same evaluation phase. For this reason, fuzzy controller input variables (I) are sampled and held as V_I prior to fuzzification. Sampling and holding provides a synchronization for all the input voltages applied to the positive and negative ramp generators in both phases. Sample and hold units are constructed as a unity-gain zero-offset version of the noninverting amplifier. A S/H circuit is shown in Fig.4.9(a). It is constructed by cancelling one capacitor column in the noninverting amplifier configuration. Input variable is assumed to be a voltage and depicted in the figure as analog input, " V_{ai} ".

This circuit also has a rail-to-rail functionality. It uses two nonoverlapping resetting and evaluation phases for the operation like noninverting and inverting amplifier circuits do. During resetting, C_1 receives an input by an analog switch while C is connected to ground by an NMOS. In the evaluation phase, C_1 is connected to ground by an NMOS and C is connected to output via an analog switch. The charge registered at the input node of OPI in the reset phase is given by

$$Q_r = (V_r - V_{ai})C_1 + V_r C. \quad (4.18)$$

During evaluation, this amount of charge is preserved in this node because of the high-impedance state. This charge can be expressed as

$$Q_e = V_e C_1 + (V_e - V_{o(OPI)})C. \quad (4.19)$$

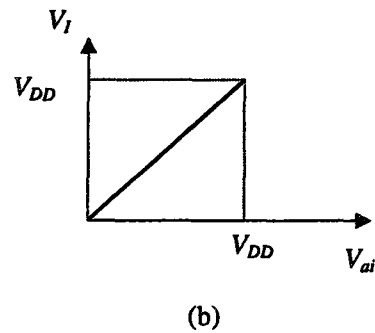
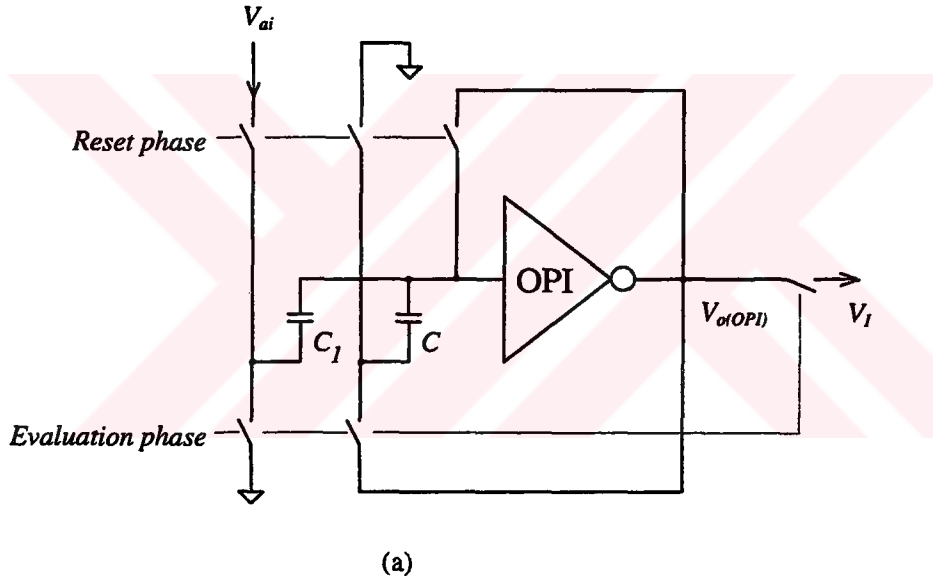


Figure 4.9(a) Sample and hold circuit, and (b) its transfer characteristics.

The output voltage can be derived with an analysis similar to that done before for the inverting and noninverting amplifiers. Thus, the output voltage expression is obtained as

$$V_{o(OP1)} = \frac{C_1}{C} V_{ai} - \frac{(C_1 + C)}{AC} (V_{o(OP1)} - V_{th}). \quad (4.20)$$

Since $-A$ is assumed to be very high, second term becomes negligible and

$$V_i = \frac{C_1}{C} V_{ai} \quad (4.21)$$

is obtained. If $C_1 = C$, the output voltage of the sample and hold circuit will be equal to the input voltage for the full range of ground- V_{DD} . This situation is drawn in Fig.4.9(b).

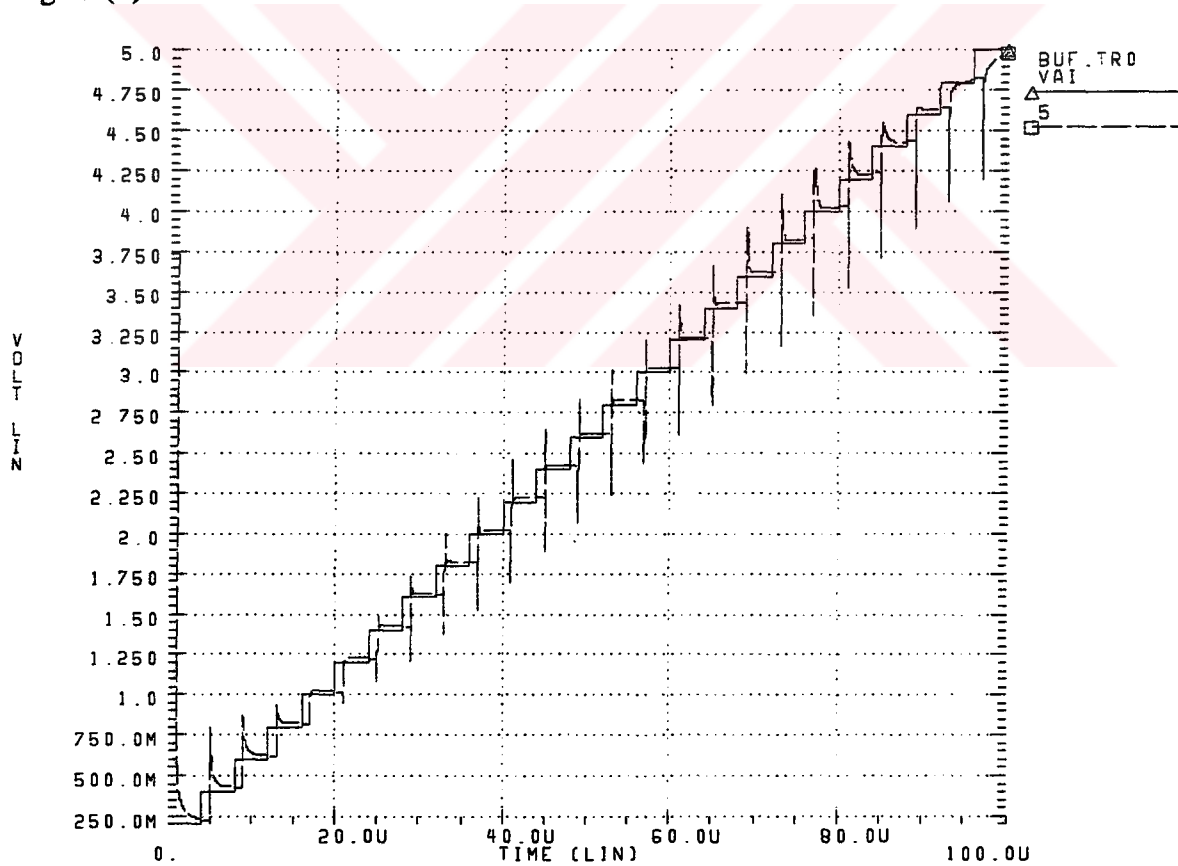


Figure 4.10 Staircase input and the output, transient analysis plots of a sample and hold circuit, $C_1 = C = 500\text{fF}$.

A simulation similar to those for the positive and negative ramps, was run for the sample and hold circuit for capacitances $C_1=C=500\text{fF}$. Fig.4.10 shows the input and output plots. $4\mu\text{s}$ depicts the period of sequential reset and evaluation phases.

4.2.4 Operational Inverter (OPI)

The proposed core amplifier, named “Operational Inverter”, is employed in fuzzifier subblocks and also in adder structures of the defuzzifier. Circuit schematic of OPI is depicted in Fig.4.11. Dimensions of the transistors are given in Table 4.1. The circuit is composed of three cascaded inverter stages and is a modified version of the amplifier proposed in [121]. The PSRR enhancement introduced to the first stage is one of the modifications. Enhancement of PSRR is obtained by the insertion of two source-follower transistors between the supplies and the inverter transistors. Gates of these additional transistors are tied to V_{GG1} and V_{GG2} . Second modification is done over the compensation scheme.

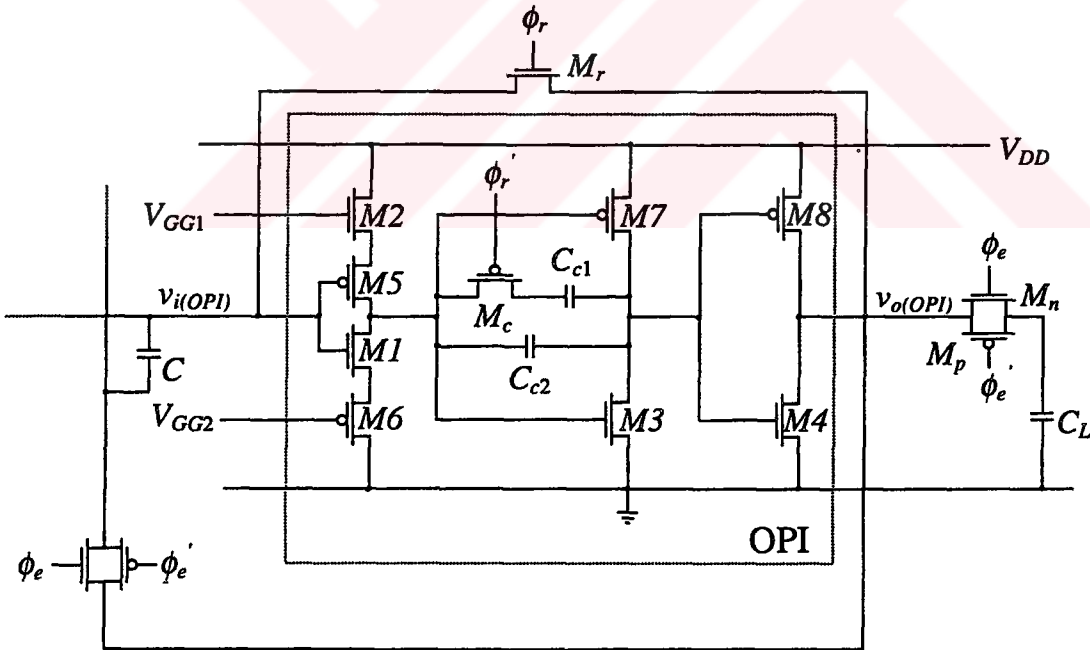


Figure 4.11 Circuit schematic of OPI.

Table 4.1 Dimensions of the transistors employed by OPI.

Transistor	W[μm]	L[μm]
M1	2	2,5
M2	2	2,5
M3	4	2,5
M4	12	2,5
M5	2	1,2
M6	2	1,2
M7	4	1,2
M8	12	1,2

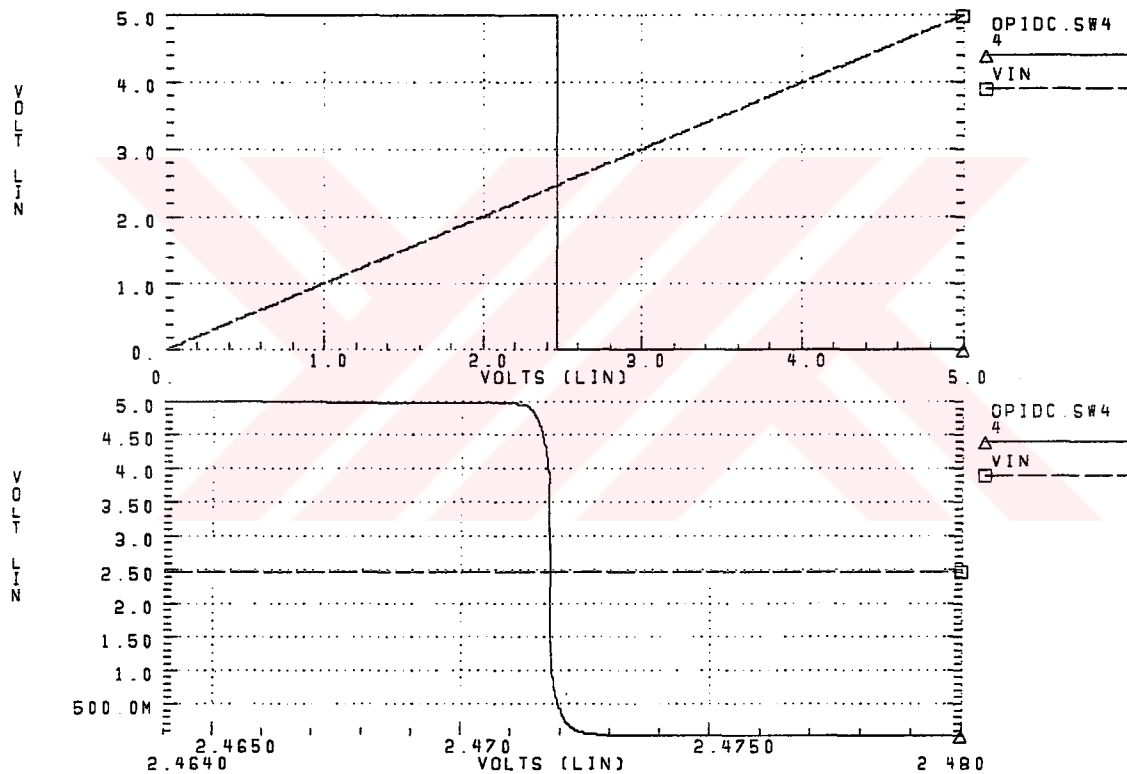


Figure 4.12 DC transfer characteristics of OPI. $V_{DD}=5\text{V}$, $V_{GG1}=5\text{V}$, $V_{GG2}=0\text{V}$. Simulation was run with the SPICE parameter set of AMS 1,2 μm CMOS technology. Dashed line is input, solid line is output.

As mentioned previously operational inverter has high gain around its logic threshold V_{th} and is used as an amplifier around this level. HSPICE dc simulation results of the transfer characteristic given in Fig.4.12. As can be clearly seen from the figure, very small variations in its input forces its output to reach to supply levels without any decay of linearity in a significantly wide region of full range.

As mentioned before, this sampled-analog amplifier uses two nonoverlapping clock signals for the operation. The first phase is for resetting while the second one is for the evaluation.

In the reset phase, input and output of OPI are shorted by the transistor M_r and voltages of these nodes settle to V_{th} . During this phase, the output load C_L is isolated from the output of the circuit because the analog switch M_n/M_p is cut off. Connection between the input and the output would result in an unstable condition because of the high gain and 180° phase difference between these two nodes, and, therefore, is prevented in this design. Stability is provided by the devices located between the input and the output of the second stage. Channel resistance of M_c and the capacitor C_{c1} stabilize the circuit (the effect of C_{c2} is insignificant in this phase).

In the second phase, M_r is turned off but another external feedback is applied to the amplifier via capacitor C . In this phase stability is assured by compensation with C_{c2} . M_c is not activated during this phase, hence, M_c and C_{c1} do not affect the circuit.

4.2.4.1 Small-Signal Analysis of Ramp Generators

Positive and negative ramp generators and the sample-and-hold circuit have similar small-signal equivalent schematics with the exception of differences in some component values. Given this circumstance, extracting of one small-signal equivalent circuit for each phase of two-phased operation is adequate. The small-signal equivalent circuit appropriate for the reset phase is given Fig.4.13. C_{o1} , C_{o2} and C_{o3}

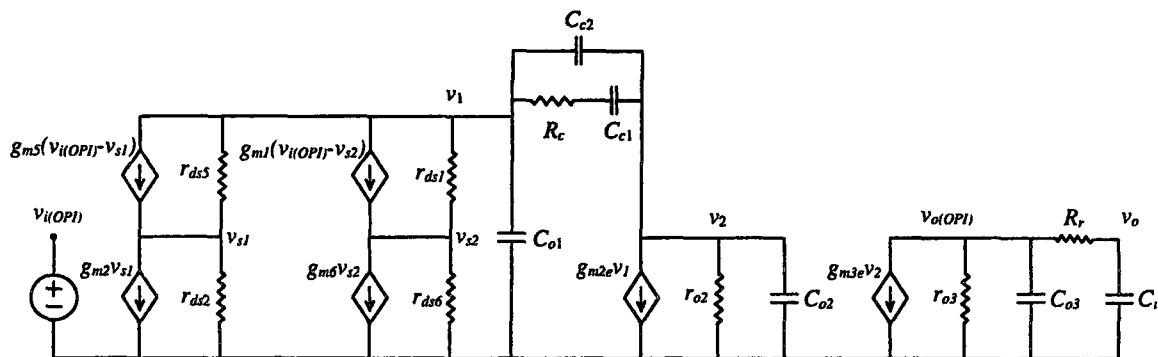


Figure 4.13 Small-signal equivalent of OPI in reset phase.

are placed for the equivalent output capacitances of the first, second and third stages, respectively, where r_{o2} , g_{m2e} and r_{o3} , g_{m3e} are the equivalent output resistances and the transconductances of related stages. Resistances of input switch transistors in series to the input capacitances are neglected and the capacitances located in parallel at the input node of OPI are lumped into an equivalent C_i for the sake of simplicity of the analysis. R_r and R_c represent the channel resistance of M_r and M_c , respectively. For analysing the open-loop behaviour of the circuit, the loop is opened from the input node of OPI [104] as depicted in the figure. Since the loading that is imposed on OPI are different in the first and second phases of the operation, analysis will be done separately for these two phases.

Some simplifications should be done on the first stage, before starting an entire analysis. First stage of OPI has four transistors including gain and PSRR enhancement parts. Because it is difficult to analyse the circuit in the form of this complex structure it is better to simplify it. Norton equivalent of the first stage will be derived in the next subsections and replaced with the purpose of simplification.

Dependent Current Source in Norton Equivalent of the First Stage

Small-signal equivalent of the first stage is shown in Fig.4.14 for extracting the value of the dependent current source. The value of this current source is described as i in Norton's which is short-circuit current

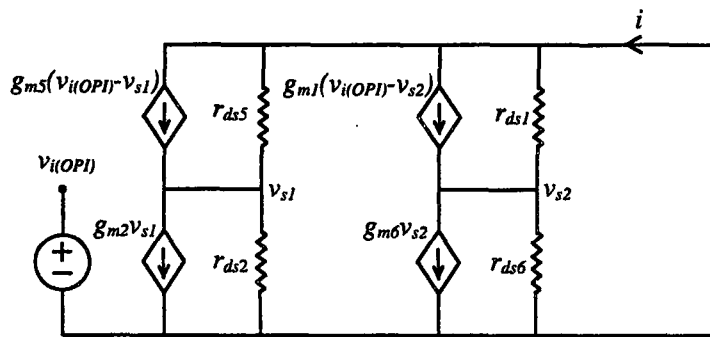


Figure 4.14 Circuit schematic in order to extract the dependent current source in Norton equivalent.

as depicted in the figure. Node equations can be written as follows

$$g_{m5}(v_{i(OPI)} - v_{s1}) - \frac{v_{s1}}{r_{ds5}} + g_{m1}(v_{i(OPI)} - v_{s2}) - \frac{v_{s2}}{r_{ds1}} = i, \quad (4.22)$$

$$g_{m5}(v_{i(OP1)} - v_{s1}) - \frac{v_{s1}}{r_{ds5}} - g_{m2}v_{s1} - \frac{v_{s1}}{r_{ds2}} = 0, \quad (4.23)$$

$$g_{m1}(v_{i(OP1)} - v_{s2}) - \frac{v_{s2}}{r_{ds1}} - g_{m6}v_{s2} - \frac{v_{s2}}{r_{ds6}} = 0. \quad (4.24)$$

Source voltages of transistors $M2$, $M5$ and $M6$, $M1$ can be extracted from the latter two as

$$v_{s1} = \frac{g_{m5}}{g_{m5} + \frac{1}{r_{ds5}} + g_{m2} + \frac{1}{r_{ds2}}} v_{i(OP1)}, \quad (4.25)$$

$$v_{s2} = \frac{g_{m1}}{g_{m6} + \frac{1}{r_{ds1}} + g_{m1} + \frac{1}{r_{ds6}}} v_{i(OP1)}. \quad (4.26)$$

Substitution of Eqs.(4.25) and (4.26) into Eq. (4.22) gives the current of the voltage-dependent source in Norton equivalent;

$$i = \left[g_{m1} + g_{m5} - \frac{g_{m1} \left(g_{m1} - \frac{1}{r_{ds1}} \right)}{g_{m1} + \frac{1}{r_{ds1}} + g_{m6} + \frac{1}{r_{ds6}}} - \frac{g_{m5} \left(g_{m5} - \frac{1}{r_{ds5}} \right)}{g_{m2} + \frac{1}{r_{ds2}} + g_{m5} + \frac{1}{r_{ds5}}} \right] v_{i(OP1)}. \quad (4.27)$$

Thus, the equivalent transconductance of the first stage is determined by the ratio of $i/v_{i(OP1)}$

$$g_{m1e} = g_{m1} + g_{m5} - \frac{g_{m1} \left(g_{m1} - \frac{1}{r_{ds1}} \right)}{g_{m1} + \frac{1}{r_{ds1}} + g_{m6} + \frac{1}{r_{ds6}}} - \frac{g_{m5} \left(g_{m5} - \frac{1}{r_{ds5}} \right)}{g_{m2} + \frac{1}{r_{ds2}} + g_{m5} + \frac{1}{r_{ds5}}}. \quad (4.28)$$

Output Resistance in Norton Equivalent of the First Stage

Fig.4.15 shows the configuration in order to derive the output resistance. Input independent voltage source; $v_{i(OPI)}$, is set to zero and a small-signal voltage source, v , is applied to the output. The ratio v/i gives the output resistance of the first stage.

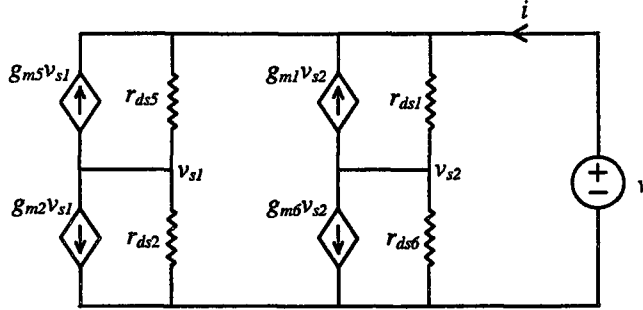


Figure 4.15 Circuit schematic in order to extract the output resistance of the first stage.

Node equations are

$$\frac{v - v_{s1}}{r_{ds5}} + \frac{v - v_{s2}}{r_{ds1}} - g_{m5}v_{s1} - g_{m1}v_{s2} = i, \quad (4.29)$$

$$g_{m5}v_{s1} + \frac{v_{s1} - v}{r_{ds5}} + g_{m2}v_{s1} + \frac{v_{s1}}{r_{ds2}} = 0, \quad (4.30)$$

$$g_{m1}v_{s2} + \frac{v_{s2} - v}{r_{ds1}} + g_{m6}v_{s2} + \frac{v_{s2}}{r_{ds6}} = 0. \quad (4.31)$$

The voltages of the source nodes can be derived in this situation as

$$v_{s1} = \frac{v}{r_{ds5} \left(g_{m5} + \frac{1}{r_{ds5}} + g_{m2} + \frac{1}{r_{ds2}} \right)} \quad (4.32)$$

$$v_{s2} = \frac{v}{r_{ds1} \left(g_{m1} + \frac{1}{r_{ds1}} + g_{m6} + \frac{1}{r_{ds6}} \right)}. \quad (4.33)$$

Substituting these two into the Eq.(4.29) we arrive at

$$i = \left[\frac{1}{r_{ds5}} + \frac{1}{r_{ds1}} - \frac{g_{m5} + \frac{1}{r_{ds5}}}{r_{ds5} \left(g_{m2} + \frac{1}{r_{ds2}} + g_{m5} + \frac{1}{r_{ds5}} \right)} - \frac{g_{m1} + \frac{1}{r_{ds1}}}{r_{ds1} \left(g_{m1} + \frac{1}{r_{ds1}} + g_{m6} + \frac{1}{r_{ds6}} \right)} \right] v. \quad (4.34)$$

The output resistance is described by the ratio v/i

$$r_{o1} = \frac{1}{\frac{1}{r_{ds5}} + \frac{1}{r_{ds1}} - \frac{g_{m5} + \frac{1}{r_{ds5}}}{r_{ds5} \left(g_{m2} + \frac{1}{r_{ds2}} + g_{m5} + \frac{1}{r_{ds5}} \right)} - \frac{g_{m1} + \frac{1}{r_{ds1}}}{r_{ds1} \left(g_{m1} + \frac{1}{r_{ds1}} + g_{m6} + \frac{1}{r_{ds6}} \right)}}. \quad (4.35)$$

Now, since the equivalent transconductance (g_{m1e}) and output resistance (r_{o1}) of the first stage are determined, this stage can be replaced with the equivalent circuit given in Fig.4.16 in the small-signal equivalent of OPI.

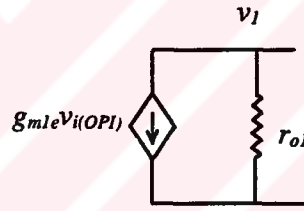


Figure 4.16 Norton equivalent of the first stage, g_{m1e} and r_{o1} are described by (4.28) and (4.35).

As a result of this replacement, the circuit is transformed into what is depicted in Fig.4.17.

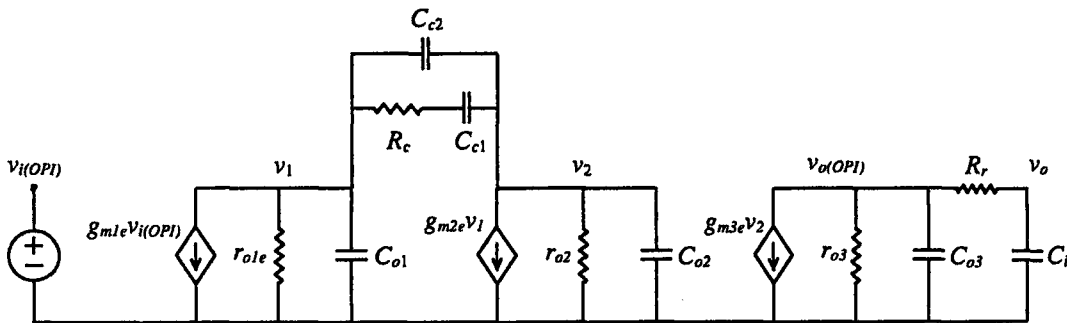


Figure 4.17 First stage is replaced by the Norton equivalent.

Defining admittances,

$$Y_{o1} = \frac{1}{r_{o1}} + sC_{o1} = \frac{1 + sr_{o1}C_{o1}}{r_{o1}},$$

$$Y_{o2} = \frac{1}{r_{o2}} + sC_{o2} = \frac{1 + sr_{o2}C_{o2}}{r_{o2}},$$

$$Y_c = sC_{c2} + \frac{1}{R_c + \frac{1}{sC_{c1}}} = \frac{s(C_{c1} + C_{c2}) + s^2 R_c C_{c1} C_{c2}}{1 + sR_c C_{c1}},$$

$$Y_L = \frac{1}{r_{o3}} + sC_{o3} + \frac{1}{R_r + \frac{1}{sC_i}} = \frac{1 + s[r_{o3}(C_{o3} + C_i) + R_r C_i] + s^2 r_{o3} R_r C_{o3} C_i}{r_{o3}(1 + sR_r C_i)}.$$

this circuit finally reduces to the configuration shown in Fig.4.18.

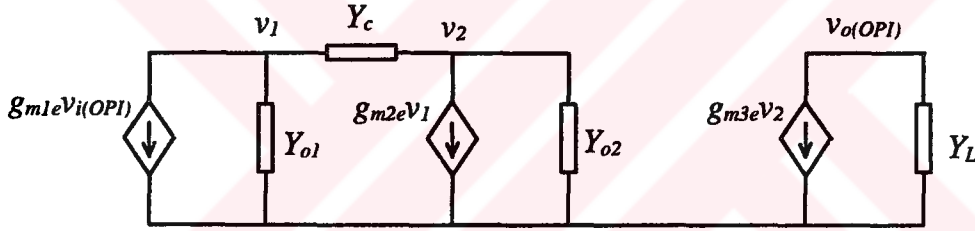


Figure 4.18 Admittance-based small-signal equivalent of a ramp generator.

This admittance-based equivalent schematic can be used for the analysis in both phases with simple changes in the descriptions of the admittances. From Fig. 4.18 node equations for both phases can be expressed as

$$Y_L v_{o(OPI)} + g_{m3e} v_2 = 0, \quad (4.36)$$

$$Y_{o2} v_2 + g_{m2e} v_1 + Y_c (v_2 - v_1) = 0, \quad (4.37)$$

$$g_{m1e} v_{i(OPI)} + Y_{o1} v_1 + Y_c (v_1 - v_2) = 0. \quad (4.38)$$

From (4.36)

$$v_2 = -\frac{Y_L}{g_{m3e}} v_{o(OPI)} \quad (4.39)$$

can be written, and arrangement of (4.37) gives

$$(Y_{o2} + Y_c)v_2 + (g_{m2e} - Y_c)v_1 = 0. \quad (4.40)$$

Hence, the relation between v_1 and v_2 can be expressed as

$$v_1 = \frac{Y_{o2} + Y_c}{Y_c - g_{m2e}} v_2. \quad (4.41)$$

If (4.39) and (4.41) are substituted into (4.38), and the resulting one is arranged,

$$\frac{v_{o(OPI)}}{v_{i(OPI)}} = -\frac{g_{m1e} g_{m3e}}{Y_L} \frac{g_{m2e} - Y_c}{Y_{o1}Y_{o2} + Y_{o2}Y_c + Y_{o1}Y_c + g_{m2e}Y_c} \quad (4.42)$$

can be obtained. This expression represents the transfer function of OPI.

4.2.4.2 Pole-Zero Analysis in Reset Phase

Output load and compensation circuits in reset phase are different from those in evaluation phase. These are represented by Y_L and Y_c in Fig.4.18. Descriptions of all the admittances in the circuit for the first phase are given as follows;

$$Y_{o1} = \frac{1}{r_{o1}} + sC_{o1} = \frac{1 + sr_{o1}C_{o1}}{r_{o1}}, \quad (4.43)$$

$$Y_{o2} = \frac{1}{r_{o2}} + sC_{o2} = \frac{1 + sr_{o2}C_{o2}}{r_{o2}}, \quad (4.44)$$

$$Y_c = sC_{c2} + \frac{1}{R_c + \frac{1}{sC_{c1}}} = \frac{s(C_{c1} + C_{c2}) + s^2 R_c C_{c1} C_{c2}}{1 + sR_c C_{c1}}, \quad (4.45)$$

$$Y_L = \frac{1}{r_{o3}} + sC_{o3} + \frac{1}{R_r + \frac{1}{sC_i}} = \frac{1 + s[r_{o3}(C_{o3} + C_i) + R_r C_i] + s^2 r_{o3} R_r C_{o3} C_i}{r_{o3}(1 + sR_r C_i)}. \quad (4.46)$$

Substituting the admittances given by (4.43-46) into (4.42), s -domain transfer function of OPI is expressed as

$$\frac{v_{o(OPI)}}{v_{i(OPI)}} = -\frac{g_{m1e}g_{m2e}g_{m3e}r_{o1}r_{o2}}{Y_L} \frac{1 + sR_cC_{c1} - \frac{s(C_{c1} + C_{c2})}{g_{m2e}} - \frac{s^2R_cC_{c1}C_{c2}}{g_{m2e}}}{1 + a_1s + a_2s^2 + a_3s^3} \quad (4.47)$$

where

$$a_1 = g_{m2e}r_{o1}r_{o2}(C_{c1} + C_{c2}) + (r_{o1} + r_{o2})(C_{c1} + C_{c2}) + r_{o1}C_{o1} + r_{o2}C_{o2} + R_cC_{c1}, \quad (4.48)$$

$$a_2 = g_{m2e}r_{o1}r_{o2}R_cC_{c1}C_{c2} + r_{o1}r_{o2}[(C_{c1} + C_{c2})(C_{o1} + C_{o2}) + C_{o1}C_{o2}] + R_cC_{c1}[r_{o1}(C_{o1} + C_{c2}) + r_{o2}(C_{o2} + C_{c2})] \quad (4.49)$$

and

$$a_3 = r_{o1}r_{o2}R_cC_{c1}[C_{o1}(C_{o2} + C_{c2}) + C_{o2}C_{c2}]. \quad (4.50)$$

After finding the transfer from the input to the output of OPI, open-loop transfer function should be found for pole-zero analysis. For this purpose, gain from the output of OPI to the output of the loop should be derived. From Fig.4.17 the transfer from $v_{o(OPI)}$ to v_o in s -domain is written as

$$\frac{v_o}{v_{o(OPI)}} = \frac{1}{1 + sR_rC_i}. \quad (4.51)$$

Equation for Y_L and (4.51) are substituted into (4.47) to arrive the loop transfer function in s -domain given below

$$\frac{v_o}{v_{i(OPI)}} = -\frac{A \left[1 + sR_cC_{c1} - \frac{s(C_{c1} + C_{c2})}{g_{m2e}} - \frac{s^2R_cC_{c1}C_{c2}}{g_{m2e}} \right]}{\left[1 + sr_{o3}(C_{o3} + C_i) + sR_rC_i + s^2sr_{o3}R_rC_{o3}C_i \right] (1 + a_1s + a_2s^2 + a_3s^3)} \quad (4.52)$$

where

$$A \equiv g_{m1e} g_{m2e} g_{m3e} r_{o1} r_{o2} r_{o3} . \quad (4.53)$$

As can be seen from the numerator of the equation above, the transfer function has two zeros which are introduced by the compensation components. The zeros can be extracted from this quadratic term by assuming that they are widely seperated, which means $|\omega_{z1}| \ll |\omega_{z2}|$. Therefore,

$$\begin{aligned} \left(1 + \frac{s}{\omega_{z1}}\right) \left(1 - \frac{s}{\omega_{z2}}\right) &= 1 + s \left(\frac{1}{\omega_{z1}} - \frac{1}{\omega_{z2}} \right) - s^2 \frac{1}{\omega_{z1} \omega_{z2}} \\ &\cong 1 + \frac{s}{\omega_{z1}} - \frac{s^2}{\omega_{z1} \omega_{z2}} \end{aligned} \quad (4.54)$$

can be written. In the equation, ω_{z1} denotes the zero in the left half-plane while ω_{z2} denotes that in the right half-plane. With the assumption given above, the zeros of the circuit can be determined as

$$\omega_{z1} = - \frac{g_{m2e}}{(g_{m2e} R_c - 1) C_{c1} - C_{c2}} \quad (4.55)$$

$$\omega_{z2} = \frac{(g_{m2e} R_c - 1) C_{c1} - C_{c2}}{R_c C_{c1} C_{c2}} . \quad (4.56)$$

Denominator of Eq.(4.52) indicates that the transfer function has five poles. The first multiplicand term of it is quadratic and two poles can be extracted form this term by using the similar assumption given above, hence,

$$\begin{aligned} \left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right) &= 1 + s \left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}} \right) + s^2 \frac{1}{\omega_{p1} \omega_{p2}} \\ &\cong 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1} \omega_{p2}} \end{aligned} \quad (4.57)$$

can be written for these two poles. Second term in the denominator of Eq.(4.52) is of third order and yields three poles. Once again, assuming that these are widely seperated in the order $|\omega_{p1}| \ll |\omega_{p2}| \ll |\omega_{p3}|$, the following can be written

$$\begin{aligned}
\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right) \left(1 + \frac{s}{\omega_{p3}}\right) &= 1 + s \left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}} + \frac{1}{\omega_{p3}} \right) \\
&+ s^2 \left(\frac{1}{\omega_{p1}\omega_{p2}} + \frac{1}{\omega_{p2}\omega_{p3}} + \frac{1}{\omega_{p1}\omega_{p3}} \right) \\
&+ s^3 \left(\frac{1}{\omega_{p1}\omega_{p2}\omega_{p3}} \right) \\
&\cong 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1}\omega_{p2}} + \frac{s^3}{\omega_{p1}\omega_{p2}\omega_{p3}}.
\end{aligned} \tag{4.58}$$

Under these conditions, five roots of the denominator in (4.52) can be derived as

$$\omega_{p1} = -\frac{1}{a_1}, \tag{4.59}$$

$$\omega_{p2} = -\frac{a_1}{a_2}, \tag{4.60}$$

$$\omega_{p3} = -\frac{a_2}{a_3}, \tag{4.61}$$

$$\omega_{p4} = -\frac{1}{r_{o3}(C_{o3} + C_i) + R_r C_i}, \tag{4.62}$$

$$\omega_{p5} = -\frac{r_{o3}(C_{o3} + C_i) + R_r C_i}{r_{o3} R_r C_{o3} C_i} \tag{4.63}$$

where a_1 , a_2 and a_3 were defined with the Eqs.(4.48-50).

Symbolic expressions for the zeroes and poles were obtained for the reset phase above and given with the (4.55,56) and (4.59-63). From these poles and zeros; f_{p1} , f_{p4} and f_{z1} are located in the unity-gain bandwidth while the others are at higher frequencies. f_{p1} is the dominant pole which is determined by the compensation components. f_{p4} is introduced by the input capacitors, channel resistance of the resetting transistor, output capacitor and resistance of the third stage. This pole is located very close to unity gain frequency for the different input capacitors used in noninverting and inverting amplifiers and the sample and hold circuit. This can cause a stability problem, thus, f_{z1} is introduced to compensate this effect.

Manual calculations and HSPICE pole-zero analysis results for a sample noninverting amplifier are compared in Table 4.2. Small-signal parameter values of the devices are taken from the output of the operating point analysis of HSPICE, input and output files can be found in App.A.

Table 4.2 AC analysis results for the first phase.

Loop gain, poles, zero	HSPICE Analysis results	Manual Analysis results
A	88 dB	87.5 dB
f_{p1}	246 Hz	280 Hz
f_{p4}	6.5 MHz	7.3 MHz
f_{z1}	18.2 MHz	19.2 MHz

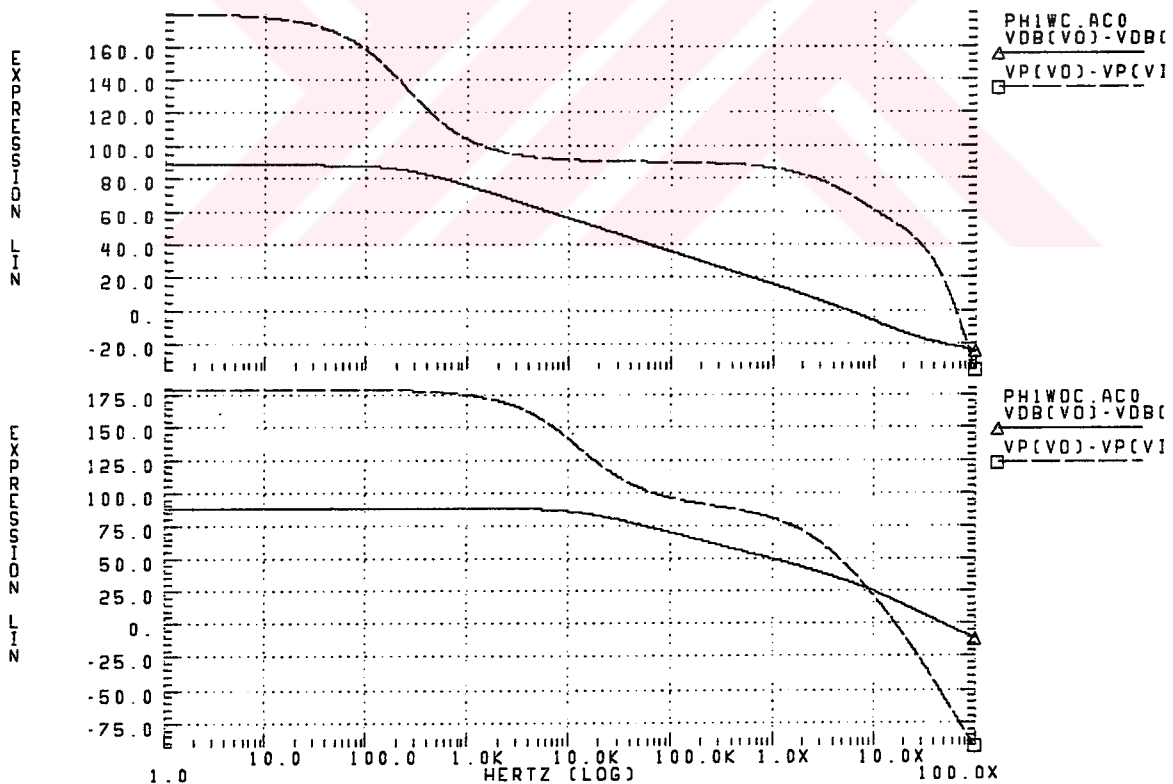


Figure 4.19 HSPICE ac analysis results for a sample noninverting amplifier in reset phase. Solid line is open-loop gain in [dB], dashed line show the change in phase. Upper plots depict the compensated situation while lower plots depict the situation without compensation. Transistor dimensions and capacitor values are given in App.A.

In the results of HSPICE pole-zero analysis it can be seen that two poles and two zeros appeared around 10 MHz. These poles and zeros are created by the parasitic capacitors between the source nodes of the source followers and ground which are driven by the clean supplies. Although they are very close to band width, they compensate for each other and never create a negative effect on stability, so, they have an insignificant effect on the transfer function. Fig.4.19 shows the loop gain and phase variations versus frequency in the reset phase of a sample noninverting amplifier.

4.2.4.3 Pole-Zero Analysis in Evaluation Phase

During the evaluation phase, M_c and C_{c1} are not functional. Stability is achieved in this phase only by C_{c2} existing across the second stage. It is obvious that Y_c and Y_L are different in this phase, but, as mentioned before, the small-signal equivalent circuit given in Fig.4.18 can also be used for pole-zero analysis of the configuration provided that appropriate modifications are made on these admittances for the evaluation phase. In the evaluation mode of operation the compensation admittance becomes

$$Y_c = sC_{c2}, \quad (4.64)$$

and the new load admittance shown in Fig.4.20 can be expressed as

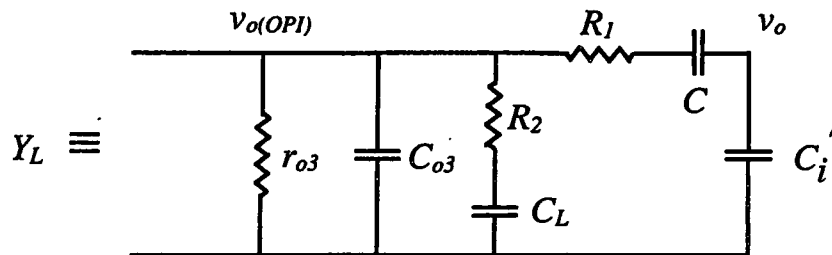


Figure 4.20 Load admittance equivalent imposed on OPI in the evaluation.

$$Y_L = \frac{1}{r_{o3}} + sC_{o3} + \frac{1}{R_2 + \frac{1}{sC_L}} + \frac{1}{R_1 + \frac{1}{sC'}} \quad (4.65)$$

where

$$C' = \frac{CC_i'}{C + C_i'} \quad (4.66a)$$

and

$$C_i' = C_i - C, \quad (4.66b)$$

where C_i' denotes the capacitance coming from the input circuitry of the ramp generator or sample and hold circuit, while C' is the equivalent of the feedback capacitor C in series with C_i' . In the figure, R_1 and R_2 represent the channel resistances of the transmission gates which connect the feedback capacitor C and the output load C_L , respectively. Arrangement of (4.65) gives,

$$Y_L = \frac{1 + b_1s + b_2s^2 + b_3s^3}{r_{o3}(1 + sR_2C_L)(1 + sR_1C')} \quad (4.67)$$

where

$$b_1 = r_{o3}(C_{o3} + C_L + C') + R_1C' + R_2C_L, \quad (4.68)$$

$$b_2 = R_2C_L(R_1C' + r_{o3}C_{o3} + r_{o3}C') + r_{o3}R_1C'(C_{o3} + C_L) \quad (4.69)$$

and

$$b_3 = r_{o3}R_1R_2C_{o3}C_LC'. \quad (4.70)$$

The transfer function below can be easily derived from Fig.4.20

$$\frac{v_o}{v_{o(OPI)}} = \frac{C'}{C_i'} \frac{1}{1 + sR_1C'}. \quad (4.71)$$

The relation between the input and the output of OPI in the evaluation was expressed in (4.42) in terms of admittances as

$$\frac{v_{o(OPI)}}{v_{i(OPI)}} = -\frac{g_{m1e}g_{m3e}}{Y_L} \frac{g_{m2e} - Y_c}{Y_{o1}Y_{o2} + Y_{o2}Y_c + Y_{o1}Y_c + g_{m2e}Y_c}.$$

By substituting (4.43), (4.44), (4.64), (4.67) into (4.42) and rearranging the result, open-loop transfer function is obtained as

$$\frac{v_o}{v_{i(OP1)}} = - \frac{A \frac{C'}{C_i} \left(1 - \frac{sC_{c2}}{g_{m2e}} \right) (1 + sR_2C_L)}{(1 + b_1s + b_2s^2 + b_3s^3)(1 + c_1s + c_2s^2)} \quad (4.72)$$

where

$$c_1 = g_{m2e}r_{o1}r_{o2}C_{c2} + r_{o1}(C_{o1} + C_{c2}) + r_{o2}(C_{o2} + C_{c2}) \quad (4.73)$$

and

$$c_2 = r_{o1}r_{o2}[C_{o1}(C_{o2} + C_{c2}) + C_{o2}C_{c2}] \quad (4.74)$$

with b_1 , b_2 , b_3 and A defined by the (4.68-70) and (4.53), respectively. The zeros are located at

$$\omega_{z1} = -\frac{1}{R_2C_L} \quad (4.75)$$

and

$$\omega_{z2} = \frac{g_{m2e}}{C_{c2}}. \quad (4.76)$$

The former one is created by the output load and output switch while the second one is created by the compensation capacitor and is located in the right half-plane. The latter one can cause a negative effect on the frequency response of the configuration. It is obvious that, the value of C_{c2} must be chosen as small as possible to eliminate this.

The poles of the s -domain open-loop transfer function can be extracted under the assumption of widely separation of the roots in the second and third order terms appearing in the denominator. By using the assumptions which were expressed by (4.57,58) in the reset phase analysis, the poles can be derived as follows

$$\omega_{p1} = -\frac{1}{b_1}, \quad (4.77)$$

$$\omega_{p2} = -\frac{b_1}{b_2}, \quad (4.78)$$

$$\omega_{p3} = -\frac{b_2}{b_3}, \quad (4.79)$$

$$\omega_{p4} = -\frac{1}{c_1}, \quad (4.80)$$

and

$$\omega_{p5} = -\frac{c_1}{c_2} \quad (4.81)$$

with b_1 , b_2 , b_3 , c_1 and c_2 defined by Eqs.(4.68-70) and Eqs.(4.73,74).

Stability problem in the evaluation phase is not as obvious as it is in the reset phase. Compensation is realized by a small capacitor (C_{c2}) which can cause a reasonable phase margin in the frequency response. C_{c2} creates a dominant pole which is given by (4.80). Another pole f_{p1} which is given by (4.77) is located within the bandwidth. The adverse effect of this pole on stability is compensated for by the zero expressed by (4.75). Both manual and HSPICE pole-zero analysis results are given in Table 4.3. Input and output files of the simulation are given in App.B. Fig.4.21 depicts the frequency response of the loop gain and phase in the evaluation for the sample noninverting amplifier.

For the inverting amplifier and sample and hold circuit, poles and zeros are given by the same expressions derived for the noninverting one, and therefore, stability conditions are identical for all three configurations.

Table 4.3 AC analysis results for the second phase.

Loop gain, poles, zero	HSPICE Analysis results	Manual Analysis results
$ A $	74 dB	73.5 dB
f_{p1}	2.9 MHz	3 MHz
f_{p4}	1.8 kHz	2.3 kHz
f_{z1}	8.1 MHz	8.1 MHz

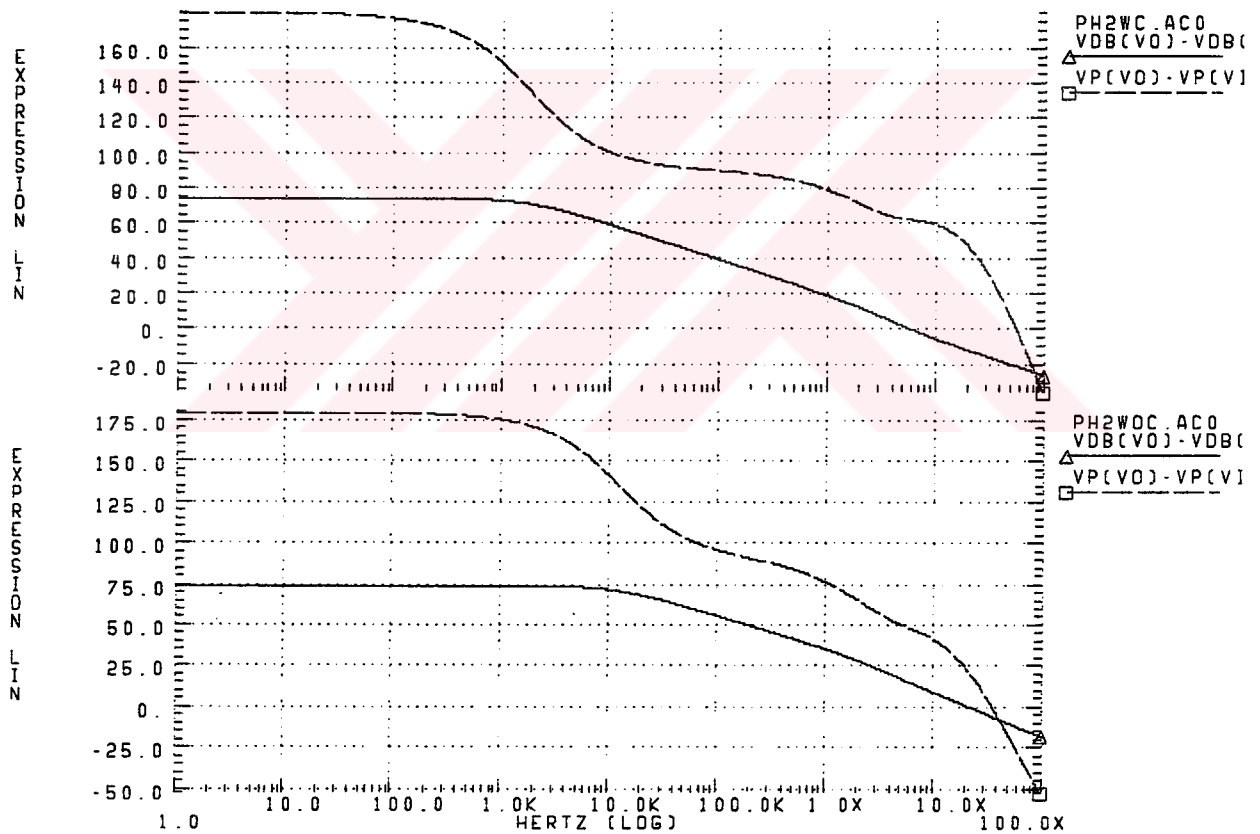


Figure 4.21 Results of HSPICE ac analysis for a sample noninverting amplifier in the evaluation phase. Solid line is open-loop gain in [dB], dashed line shows the change in phase. Upper plots depict the compensated situation while lower plots show the situation without compensation. Transistor dimensions and capacitor values are given in App.B.

4.2.4.4 PSRR Analysis of OPI

An important issue in analog circuit design is the prevention of noise coupling from supply rails. Especially in the mixed-mode integrated circuits, which consist of both analog and digital parts, the spikes generated by clocks can cause performance degradation in analog parts of the circuits. The measure of insensitivity to noise on the supply lines is known as Power Supply Rejection Ratio (PSRR).

The design of OPI includes a *PSRR* enhancement part as mentioned before. Two source follower transistors are inserted between the supply rails and the inverter in the first stage for this purpose. Gates of these transistors are driven by the "clean" supplies; V_{gg1} and V_{gg2} . These supplies give no dc current to the chip because they are terminated by the gates of the MOS transistors in all connection situations. PSRR enhancement is achieved by using the channel resistances of the source follower transistors as attenuators. Any small variation in V_{DD} is attenuated by the drain-source resistance of $M2$, and that in V_{SS} is attenuated by that of $M6$. By *PSRR* enhancement modification, source voltages of $M1$ and $M5$ (these transistors are used for the gain in the first stage) are offset from the supply levels, but, this situation does not cause a functional deterioration in the circuit. Because of open-loop gain of the overall circuit, which is determined by three stages collectively, the level of the output swing of the first stage is restored in the next stages and rail-to-rail swing is obtained at the output of OPI. Next, $PSRR_{dc}^+$ and $PSRR_{dc}^-$ which are described as the rejection ratios in low frequencies will be derived for OPI.

The small-signal equivalent of OPI that will be used for the *PSRR* analysis is depicted in Fig.4.22. Note that, bulk transconductances; g_{mb} s, are taken into account in this small-signal equivalent, they affect the PSRR behaviour of the circuit. Bulk transconductances of the transistors at the second and third stages are not effective, since their bulk-source voltages are zero.

From the figure, node equations can be written as

$$\frac{1}{r_{o8}}(v_o - v_{dd}) + g_{m8}(v_2 - v_{dd}) + \frac{1}{r_{o4}}(v_o - v_{ss}) + g_{m4}(v_2 - v_{ss}) = 0, \quad (4.82)$$

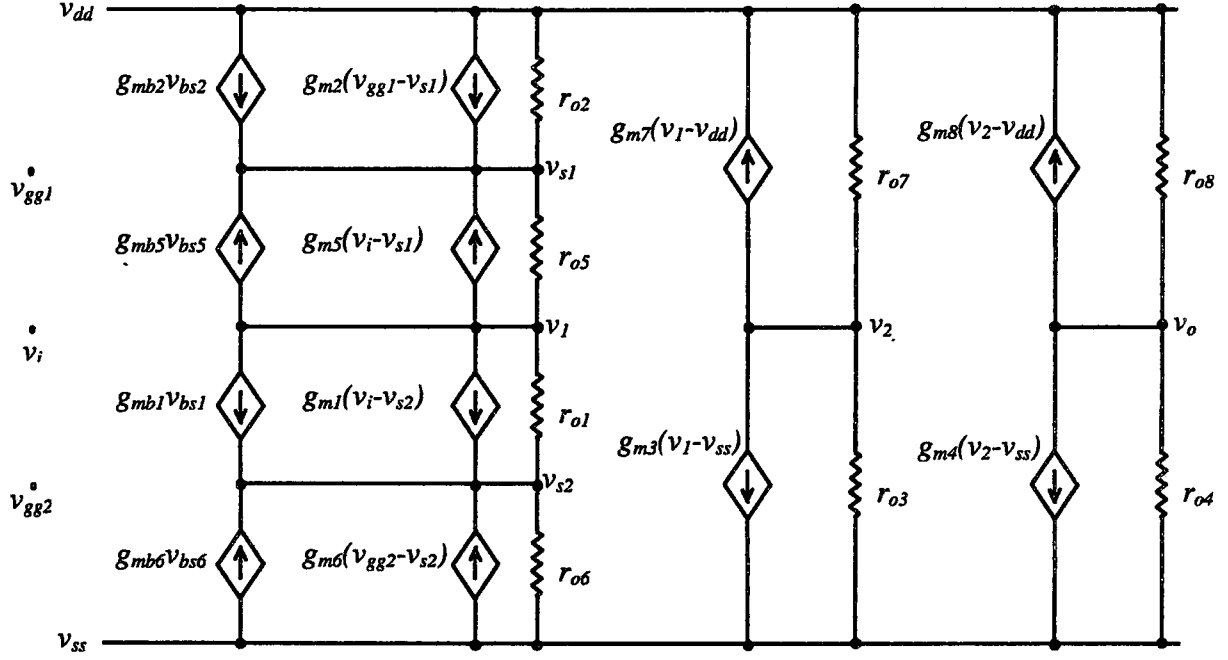


Figure 4.22 Small-signal equivalent circuit of OPI for *PSRR* analysis.

$$\frac{1}{r_{o7}}(v_2 - v_{dd}) + g_{m7}(v_1 - v_{dd}) + \frac{1}{r_{o3}}(v_2 - v_{ss}) + g_{m3}(v_1 - v_{ss}) = 0, \quad (4.83)$$

$$\begin{aligned} & \frac{1}{r_{o1}}(v_1 - v_{s2}) + g_{m1}(v_i - v_{s2}) + g_{mb1}(v_{ss} - v_{s2}) \\ & + \frac{1}{r_{o5}}(v_1 - v_{s1}) + g_{m5}(v_i - v_{s1}) + g_{mb5}(v_{dd} - v_{s1}) = 0, \end{aligned} \quad (4.84)$$

$$\begin{aligned} & \frac{1}{r_{o2}}(v_{s1} - v_{dd}) - g_{m2}(v_{gg1} - v_{s1}) - g_{mb2}(v_{ss} - v_{s1}) \\ & + \frac{1}{r_{o5}}(v_{s1} - v_1) - g_{m5}(v_i - v_{s1}) - g_{mb5}(v_{dd} - v_{s1}) = 0, \end{aligned} \quad (4.85)$$

$$\begin{aligned} & \frac{1}{r_{o1}}(v_{s2} - v_1) - g_{m1}(v_i - v_{s2}) - g_{mb1}(v_{ss} - v_{s2}) \\ & + \frac{1}{r_{o6}}(v_{s2} - v_{ss}) - g_{m6}(v_{gg2} - v_{s2}) - g_{mb6}(v_{dd} - v_{s2}) = 0. \end{aligned} \quad (4.86)$$

Arrangement of these equations yields

$$\begin{aligned}
v_o = & -|A_1||A_2||A_3|v_i \\
& + \left\{ -|A_3|\frac{r_{o2e}}{r_{77}} + |A_2||A_3|r_{ole} \left[\frac{r_{52}}{r_{55}} \left(g_{mb5} + \frac{1}{r_{o2}} \right) + \frac{r_{16}}{r_{11}} g_{mb6} - g_{mb5} \right] + \frac{r_{o3e}}{r_{88}} \right\} v_{dd} \\
& + \left\{ -|A_3|\frac{r_{o2e}}{r_{33}} + |A_2||A_3|r_{ole} \left[\frac{r_{16}}{r_{11}} \left(g_{mb1} + \frac{1}{r_{o6}} \right) + \frac{r_{52}}{r_{55}} g_{mb2} - g_{mb1} \right] + \frac{r_{o3e}}{r_{44}} \right\} v_{ss} \\
& + |A_2||A_3|\frac{r_{52}}{r_{55}} g_{m2} r_{ole} v_{gg1} \\
& + |A_2||A_3|\frac{r_{16}}{r_{11}} g_{m6} r_{ole} v_{gg2}
\end{aligned} \tag{4.87}$$

where

$$A_1 = g_{m1e} r_{ole}, \tag{4.88}$$

$$A_2 = g_{m2e} r_{o2e}, \tag{4.89}$$

$$A_3 = g_{m3e} r_{o3e}, \tag{4.90}$$

denote the voltage gains of related stages in OPI. Definitions of transconductances and conductances which appear in gain expressions are given below.

First stage:

$$g_{m1e} = \frac{r_{16}}{r_{11}} g_{m1} + \frac{r_{52}}{r_{55}} g_{m5} - g_{m15}, \tag{4.91}$$

$$\frac{1}{r_{ole}} = \frac{1}{r_{15}} - \frac{r_{16}}{r_{11}r_{ol}} - \frac{r_{52}}{r_{55}r_{os}}, \tag{4.92}$$

$$g_{m15} = g_{m1} + g_{m5}, \tag{4.93}$$

$$\frac{1}{r_{16}} = \frac{1}{r_{ol}} + g_{m1} + g_{mb1} + \frac{1}{r_{o6}} + g_{m6} + g_{mb6}, \tag{4.94}$$

$$\frac{1}{r_{52}} = \frac{1}{r_{os}} + g_{m5} + g_{m5} + \frac{1}{r_{o2}} + g_{m2} + g_{mb2}, \tag{4.95}$$

$$\frac{1}{r_{11}} = \frac{1}{r_{o1}} + g_{m1} + g_{mb1}, \quad (4.96)$$

$$\frac{1}{r_{55}} = \frac{1}{r_{o5}} + g_{m5} + g_{mb5}, \quad (4.97)$$

$$\frac{1}{r_{15}} = \frac{1}{r_{o1}} + \frac{1}{r_{o5}}. \quad (4.98)$$

Second stage:

$$g_{m2e} = g_{m7} + g_{m3}, \quad (4.99)$$

$$\frac{1}{r_{o2e}} = \frac{1}{r_{o7}} + \frac{1}{r_{o3}}, \quad (4.100)$$

$$\frac{1}{r_{33}} = \frac{1}{r_{o3}} + g_{m3}, \quad (4.101)$$

$$\frac{1}{r_{77}} = \frac{1}{r_{o7}} + g_{m7}. \quad (4.102)$$

Third stage:

$$g_{m3e} = g_{m4} + g_{m8}, \quad (4.103)$$

$$\frac{1}{r_{o3e}} = \frac{1}{r_{o4}} + \frac{1}{r_{o8}}, \quad (4.104)$$

$$\frac{1}{r_{88}} = \frac{1}{r_{o8}} + g_{m8}, \quad (4.105)$$

$$\frac{1}{r_{44}} = \frac{1}{r_{o4}} + g_{m4}. \quad (4.106)$$

Eq.(4.87) describes output voltage v_o , as a function of the small variations in V_{DD} , V_{SS} , V_{GG1} , V_{GG2} and V_I . Based on this function, we can express the sensitivity of v_o to small variations in supply voltages and input voltage as follows:

$$\frac{\partial v_o}{\partial v_i} = -|A_1||A_2||A_3| \quad (4.107)$$

is the low frequency gain of OPI,

$$\frac{\partial v_o}{\partial v_{dd}} = -|A_3|\frac{r_{o2e}}{r_{77}} + |A_2||A_3|r_{o1e}\left[\frac{r_{52}}{r_{55}}\left(g_{mb5} + \frac{1}{r_{o2}}\right) + \frac{r_{16}}{r_{11}}g_{mb6} - g_{mb5}\right] + \frac{r_{o3e}}{r_{88}} \quad (4.108)$$

and

$$\frac{\partial v_o}{\partial v_{ss}} = -|A_3|\frac{r_{o2e}}{r_{33}} + |A_2||A_3|r_{o1e}\left[\frac{r_{16}}{r_{11}}\left(g_{mb1} + \frac{1}{r_{o6}}\right) + \frac{r_{52}}{r_{55}}g_{mb2} - g_{mb1}\right] + \frac{r_{o3e}}{r_{44}} \quad (4.109)$$

are the small-signal gains from positive and negative supplies to the output, and

$$\frac{\partial v_o}{\partial v_{gg1}} = |A_2||A_3|\frac{r_{52}}{r_{55}}g_{m2}r_{o1e} \quad (4.110)$$

and

$$\frac{\partial v_o}{\partial v_{gg2}} = |A_2||A_3|\frac{r_{16}}{r_{11}}g_{m6}r_{o1e} \quad (4.111)$$

are those from the clean supplies to the output.

$PSRR_{dc}^+$ and $PSRR_{dc}^-$ are clearly defined in [105, 106] as

$$PSRR_{dc}^+ = 20 \log \frac{\left| \frac{\partial v_o}{\partial v_i} \right|}{\left| \frac{\partial v_o}{\partial v_{dd}} \right|} \quad (4.112)$$

and

$$PSRR_{dc}^- = 20 \log \frac{\left| \frac{\partial v_o}{\partial v_i} \right|}{\left| \frac{\partial v_o}{\partial v_{ss}} \right|}. \quad (4.113)$$

By taking the derivatives from (4.87), the following expressions can be found for rejection ratios;

$$PSRR_{dc}^+ = 20 \log \frac{|A_1||A_2||A_3|}{\left| -|A_3| \frac{r_{o2e}}{r_{77}} + |A_2||A_3| r_{o1e} \left[\frac{r_{52}}{r_{55}} \left(g_{mb5} + \frac{1}{r_{o2}} \right) + \frac{r_{16}}{r_{11}} g_{mb6} - g_{mb5} \right] + \frac{r_{o3e}}{r_{88}} \right|}, \quad (4.114)$$

$$PSRR_{dc}^- = 20 \log \frac{|A_1||A_2||A_3|}{\left| -|A_3| \frac{r_{o2e}}{r_{33}} + |A_2||A_3| r_{o1e} \left[\frac{r_{16}}{r_{11}} \left(g_{mb1} + \frac{1}{r_{o6}} \right) + \frac{r_{52}}{r_{55}} g_{mb2} - g_{mb1} \right] + \frac{r_{o3e}}{r_{44}} \right|}. \quad (4.115)$$

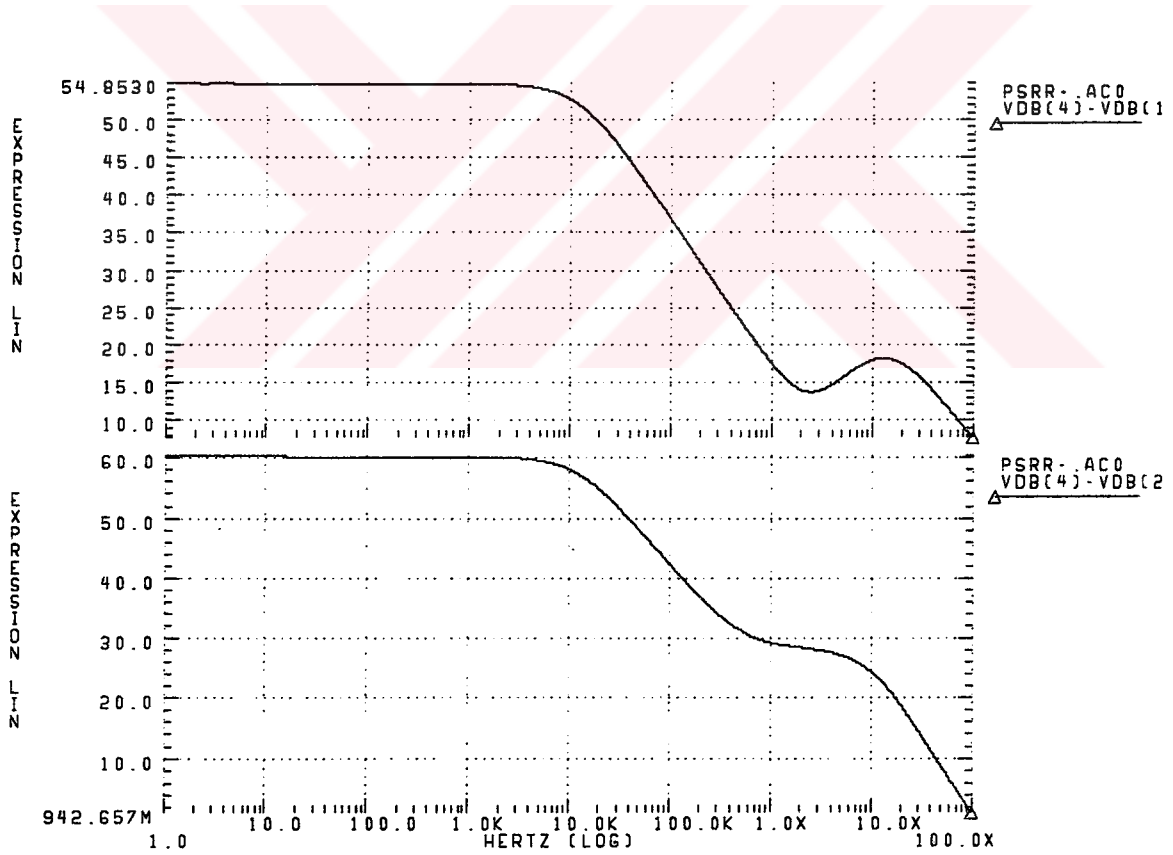


Figure 4.23 Frequency responses of $\partial v_o / \partial v_{dd}$ [dB] (upper trace) and $\partial v_o / \partial v_{ss}$ [dB] (lower trace).

In a switched-capacitor circuit some important nonlinear effects associated with MOS switches are due to their parasitic capacitances. A certain amount of parasitic charge is coupled onto the input node of OPI via drain/source-gate overlap capacitance. Since the gate of resetting transistor is switched to V_{DD} and ground during the two phases of operation, an offset is added to the input voltage depending on the amount of parasitic charge and associated capacitors. An additional charge, which is injected from the channel of resetting transistor to the input node, can be considered as another offset source in the circuit. At the end of the reset phase, this switch transistor turns off and some amount of its channel charge is injected into the input node. These phenomena are known as “clock feedthrough” [107].

Another nonideality which stems from capacitor mismatches is dominantly originated from the fabrication processes. Since systematic mismatch errors can be avoided by proper physical design practices, only the random component is considered in this work. In the physical design of the capacitors some important points should be taken into consideration; i) the capacitors appearing in the ramp generator characteristics ratios should be laid out as close as possible for preventing from the oxide thickness variation effects, ii) common-centroid geometry multiplication of a square-shaped unit capacitor should be adopted for the realization of bigger capacitors for minimizing the effect of the undercut mismatches may occur during the etching processes and parasitic fringing field effects. Since, in the fuzzifier circuits, gain and offset are determined solely by capacitor ratios, the influence of mismatch brought by physical implementation should be taken into nonideality accounts. In the worst case, depending on the capacitor implementation styles, relative capacitor mismatch error is smaller than 1% [108]. The effects of both clock feedthrough and mismatch on the gain and the offset for the proposed fuzzifier structures will be examined below.

By considering the parasitic effects and mismatch, the charges accumulated in the reset phase and preserved during evaluation can be rewritten for the noninverting amplifier as

$$Q_r = (V_r - V_l)(C_1 - \Delta C_1) + V_r(C_2 - \Delta C_2) + V_r C + (V_r - V_{DD})C_{ov} + V_r C_s, \quad (4.116a)$$

$$Q_e = V_e(C_1 - \Delta C_1) + (V_e - V_{DD})(C_2 - \Delta C_2) + (V_e - V_{out})C + V_e C_{ov} + V_e C_s, \quad (4.116b)$$

and

$$Q_e = Q_r + \Delta Q \quad (4.116c)$$

where ΔQ represents the injected channel charge and ΔC_i s stand for the deviations from intended capacitor values. Arrangement of (4.116a,b) according to (4.116c) yields

$$V_{M(PR)} = K \left[\left(\frac{C_1}{C} - \frac{\Delta C_1}{C} \right) V_I - \frac{C_2}{C} V_{DD} + \frac{\Delta C_2}{C} V_{DD} + \frac{C_1 - \Delta C_1 + C_2 - \Delta C_2 + C + C_s + C_{ov}}{AC} V_{th} + \frac{C_{ov}}{C} V_{DD} - \frac{\Delta Q}{C} \right] \quad (4.117)$$

where K is defined by

$$K \equiv \frac{AC}{(1+A)C + C_1 - \Delta C_1 + C_2 - \Delta C_2 + C_s + C_{ov}} \quad (4.118)$$

It is obvious that the ideal value of K is 1 and this condition is satisfied when open-loop gain of OPI approaches to infinity, however, a finite but very high A (88dB) sufficiently satisfies this condition that K differs from 1 by an error of 250 ppm with reasonable capacitor values. Thus, the error in the gain of the ramp function is reduced to

$$\Delta G = \frac{\Delta C_1}{C} \quad (4.119)$$

For the relative gain error

$$\frac{\Delta G}{G} = \frac{\Delta C_1}{C_1} \quad (4.120)$$

can be written. Quite clearly, relative gain error is no more than 1% for a positive ramp circuit.

Offset error in V^- can be derived from the Eq.(4.117) as

$$\Delta V^- = -\frac{\Delta C_2}{C_1} V_{DD} - \frac{C_{ov}}{C_1} V_{DD} + \frac{\Delta Q}{C_1} - \frac{C_1 - \Delta C_1 + C_2 - \Delta C_2 + C + C_s + C_{ov}}{AC_1} V_{th} \quad (4.121)$$

The last term in the equation can be neglected because of the very high A . The first term denotes the offset stemming from capacitor mismatch error, and the rest is introduced by clock feedthrough.

Assuming a) an injection of one half the channel charge of a typical minimum geometry $2\mu\text{m} \times 1,2\mu\text{m}$ NMOS reset switch, b) a gate-drain/source overlap capacitor of $0,6\text{fF}$, c) the reasonable capacitor values of $C_1=250\text{fF}$, $C_2=200\text{fF}$ and $C=100\text{fF}$, and d) an OPI of 88dB gain, 5V supply voltage and $V_{th}=2,5\text{V}$, (4.121) yields an offset error of approximately -60mV .

Another option is to choose the capacitors as large as possible which decreases the clock feedthrough offset, but, this can be considered as an handicap from the point of view of silicon area consumption. Another condition which should be satisfied for minimizing the offset is to use minimum-sized switch transistors. This minimizes not only the injected channel charge but also the gate-drain/source parasitic overlap capacitance.

Similar nonideality analysis can be carried out for the inverting amplifier and the sample and hold circuit. They yield the expressions

$$V_{M(NR)} = K \left[- \left(\frac{C_1}{C} + \frac{\Delta C_1}{C} \right) V_I + \frac{C + C_2}{C} V_{DD} + \frac{\Delta C_2}{C} V_{DD} + \frac{C_1 + \Delta C_1 + C_2 + \Delta C_2 + C + C_s + C_{ov}}{AC} V_{th} + \frac{C_{ov}}{C} V_{DD} - \frac{\Delta Q}{C} \right] \quad (4.122)$$

for the inverting amplifier, and

$$V_I = K \left[\left(\frac{C_1}{C} + \frac{\Delta C_1}{C} \right) V_I + \frac{C_1 + \Delta C_1 + C_2 + \Delta C_2 + C + C_s + C_{ov}}{AC} V_{th} + \frac{C_{ov}}{C} V_{DD} - \frac{\Delta Q}{C} \right] \quad (4.123)$$

for sample and hold circuit. K' is defined by

$$K' \equiv \frac{AC}{(1+A)C + C_1 + \Delta C_1 + C_s + C_{ov}}. \quad (4.124)$$

For both inverting amplifier and sample and hold circuit, relative gain error is 1% which is the same as in the case of the noninverting amplifier.

Offset error can be derived as

$$\Delta V^- = \frac{\Delta C_2}{C_1} V_{DD} + \frac{C_{ov}}{C_1} V_{DD} - \frac{\Delta Q}{C_1} + \frac{C_1 + \Delta C_1 + C_2 + \Delta C_1 + C + C_s + C_{ov}}{AC_1} V_{th} \quad (4.125)$$

for the inverting amplifier. In the sample and hold case, offset error can be expressed as

$$\Delta V^- = \frac{\Delta Q}{C_1} - \frac{C_{ov}}{C_1} V_{DD} - \frac{C_1 + \Delta C_1 + C + C_s + C_{ov}}{AC_1} V_{th} \quad (4.126)$$

which originates predominantly from clock feedthrough. The last term in the offset equations can be omitted because open-loop gain is very high.

Another structural nonideality that can be observed in OPI configurations is the curved transition at the break points in their transfer characteristics. Although ramp generators and the sample and hold circuit exhibit very good linearity in a considerably large region in their transfer characteristics, at the near vicinity of the upper and lower vertices where the gain region arrives at the supply levels, a linearity degradation is inevitably encountered. This situation can be explained by utilizing the dc transfer characteristics of OPI given in Fig.4.12. As can be clearly seen, in the narrow segments near the rail levels, where the transition reaches the supplies, A decreases rapidly. Consequently, K significantly reduces and becomes dominant on the gain error. At the same time, the terms containing A in (4.117), (4.122), and (4.123), which can be neglected for high gain region of OPI, cause additional errors in the output voltages of the ramp generators and S/H circuit. However, it can be seen in the HSPICE transient analysis, the error originating from the decreasing A does not exceed a couple of 10 millivolts.

4.3 Inference Engine

In a fuzzy controller, fuzzifier outputs are the inputs of the inference engine which executes the expert system rules. Generally, an inference engine should be able to realize both minimum and maximum selection operations, because the antecedent terms may be conjuncted by “AND” and/or “OR” operators in the rules.

As explained before, AND and OR operations correspond to minimum and maximum selections, respectively. In the present design, maximum selection is implemented with the maxnet configuration described in [109]. Minnet is a modified version of this configuration [110].

Usually, in the rules of physically implemented fuzzy controllers, antecedent terms are conjuncted by AND operator. Hence, inference is achieved by using only minimum operation. In the present study, only one min selection circuit is needed to execute a rule. This circuit is called as “inference module”. Therefore, the number of rules determines the number of inference modules, whereas the number of antecedent terms in a rule determines the number of inputs of the inference module.

Fig.4.25 shows an inference module block diagram. V_{Mi} depicts one of the fuzzifier module outputs. It can originate from a negative or a positive ramp generator. Since fuzzification is accomplished with the assistance of the inference mechanism, as explained in Section 4.2, construction of an input membership class is completed in the inference engine.

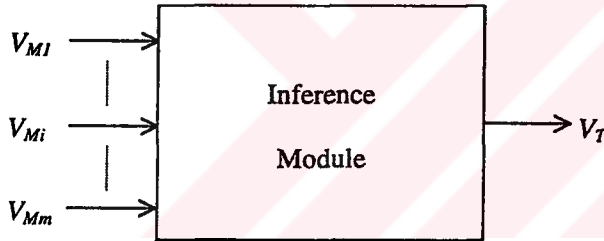


Figure 4.25 An inference module selects the minimum of V_{Mi} s.

Selection method is based on the assumption that there is only one winner which is the minimum among all inputs. It means that, there will exist a competition in the selection process. The circuit given in Fig.4.26 executes such a competition yielding only one winner. It comprises m identical cells, each assigned to one inference module input. This architecture comprises m^2+m transistors for m inputs. A cell is built around a competition node, for example, N_1 in Cell-1. This node has a pull-down path via NMOS M_D , and a pull-up path via a parallel network of $m-1$ PMOS devices placed in series with a PMOS M_U . The gate of each device in the parallel network is controlled by the competition node of another cell. A total of $m(m-1)$ such control paths establish mutually inhibitory connections among all cells,

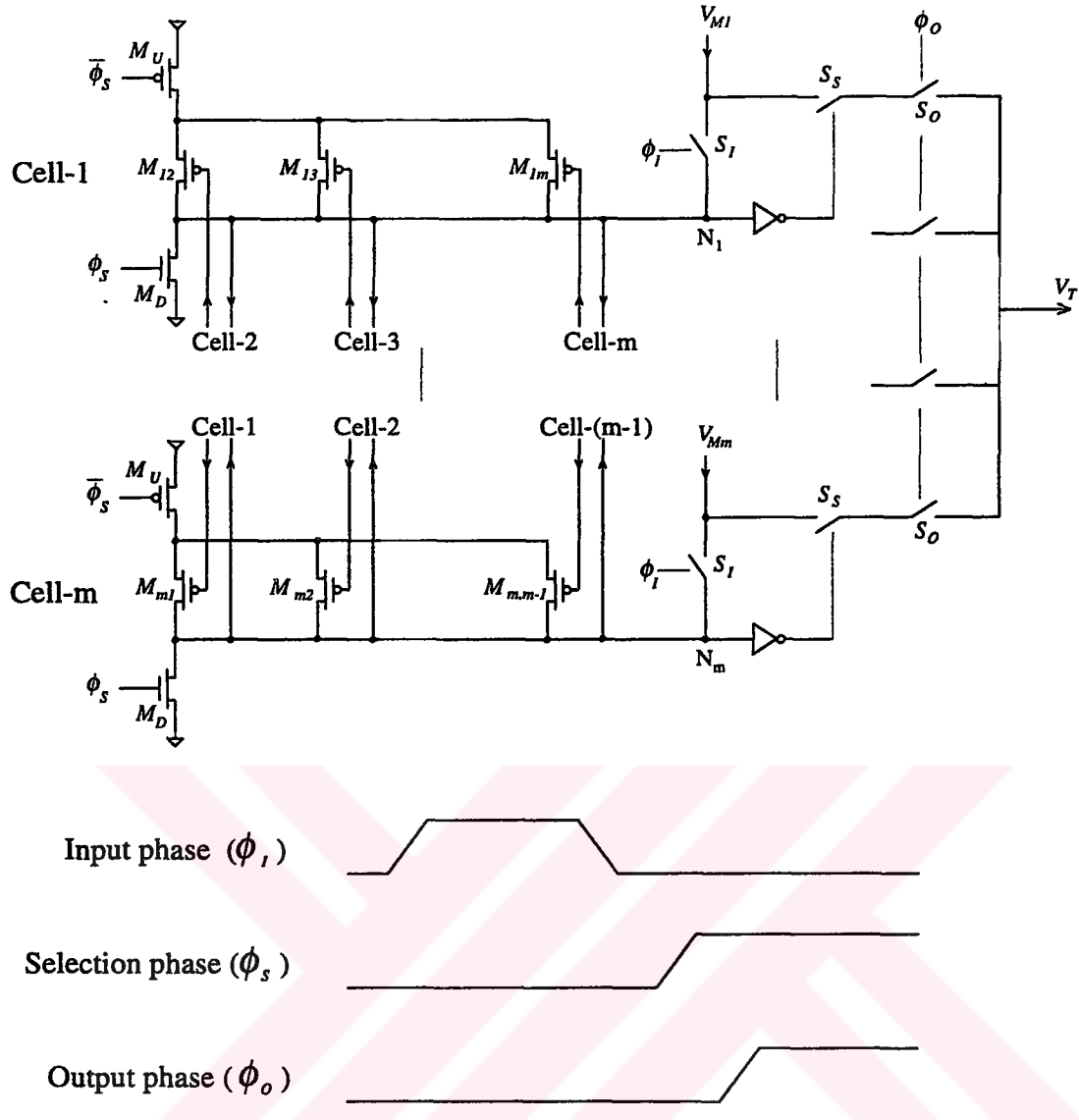


Figure 4.26 The inference module and clocking scheme.

so that when all M_D and M_U are on, the module converges to a stable state, in which one and only one competition node remains at 0V, and the others are pulled up to a voltage above $V_{DD} - |V_{TP}|$, where $|V_{TP}|$ is the absolute value of the PMOS device threshold voltage. This is guaranteed by ratioing M_D and M_U in such a way that, even if a single PMOS device in a parallel pull-up net receives 0V at its gate, the competition node voltage of that cell exceeds $V_{DD} - |V_{TP}|$. Analysis of this situation is given in the next subsection. Therefore, in a stable state, the parallel pull-up network of the cell of 0V node-voltage is completely cutoff, whereas all other cells' nodes are pulled up only by one device in each parallel pull-up net. Having described the stable state of interconnected competition nodes, we now attempt to explain the sequence of operations in the entire inference module.

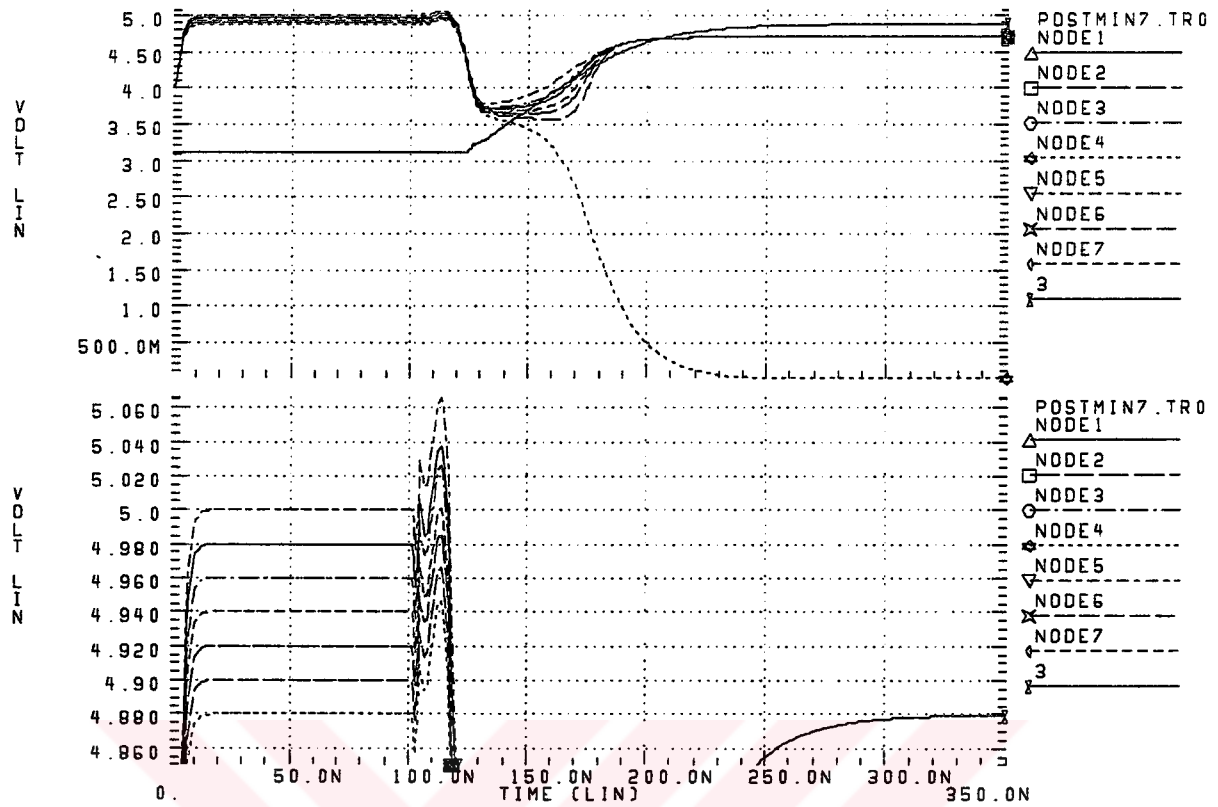


Figure 4.27 7-input inference module transient analysis results. Inputs, close to the upper extremity of the input range are transferred to the competition nodes 1 to 7 up to 100 nsec, winner node has 0V at the end of the competition.

The circuit operates with three clock signals shown in the figure. All inputs, V_{Mi} , $i=1,...,m$, are transferred onto the competition nodes of m separate cells via switches S_I during an input phase. Input voltages are registered as charges onto the identical parasitic node capacitors. Note that, since switches S_O and devices M_D and M_U are cut off, competition nodes are not interactive in this phase; they all appear as a purely capacitive load to the fuzzifier modules generating the inputs. In the following selection phase, all M_D and M_U are turned on to initiate interaction among competition nodes. At the beginning of competition, the node which has the minimum voltage initially, has a superiority over the others. Because the gate of the pull-up PMOS, which will try to raise the voltages of the other nodes to V_{DD} via M_U , has the lowest voltage, so, this transistor has the highest channel conductivity in the circuit. Competition starts under this condition and the node with the lowest voltage keeps its state during the competition. After a transient, a stable state is eventually reached, in which the cell that has initially received the lowest input survives with a grounded competition node. All other cells raise their node voltages above $V_{DD}-|V_{Th}|$.

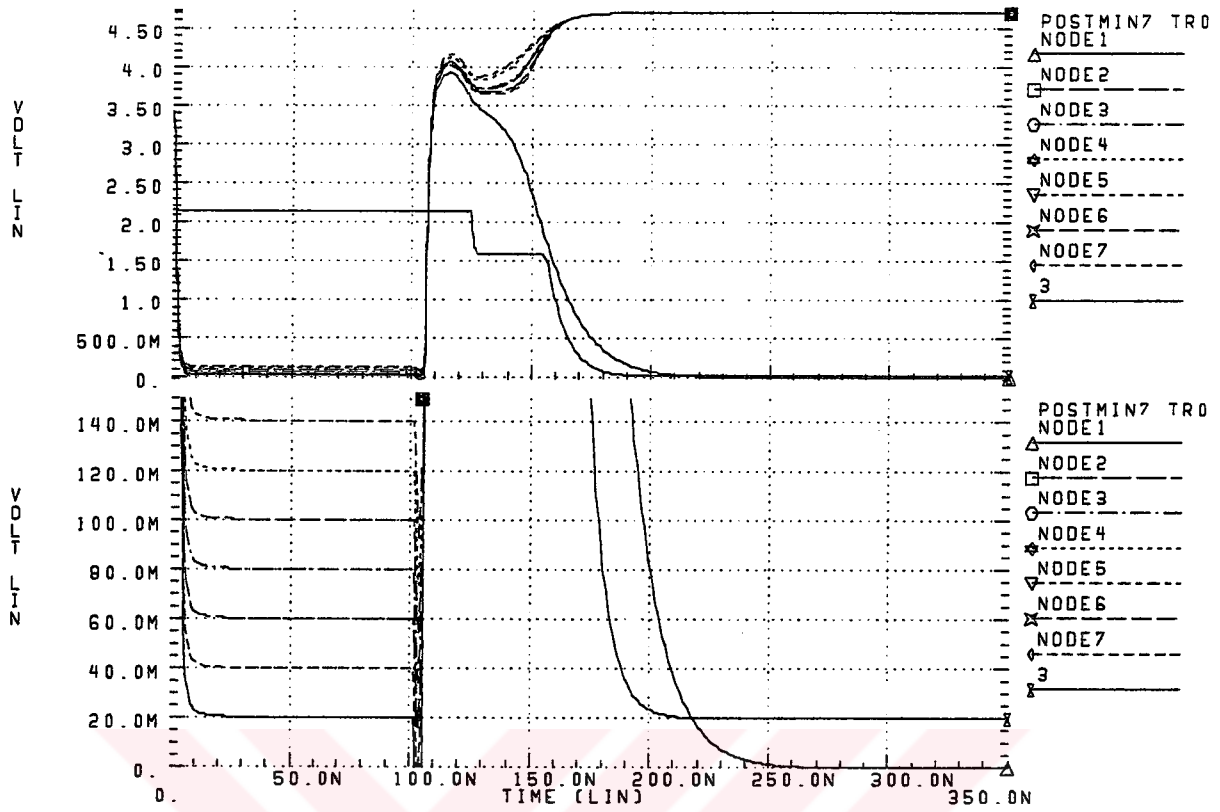


Figure 4.28 7-input inference module transient analysis results. Inputs, close to the lower extremity of the input range are transferred to the competition nodes 1 to 7 up to 100 nsec, winner node has 0V at the end of the competition.

As can be seen from Fig.4.26, switches S_S are controlled by competition nodes. Once competition-node voltages have reached a stable state with only one node having 0V, only the S_S controlled by that node remains connecting. Obviously, it connects the lowest input voltage among the set of m inputs to the output. This voltage is transferred to the output as switches S_O turn on in the final output phase. The output voltage V_T is, therefore, described by

$$V_T = \min\{V_{M1}, \dots, V_{Mm}\}. \quad (4.127)$$

As proven by the SPICE transient waveforms shown in Fig.4.27 and Fig.4.28 for two extreme input voltage vectors, the inference module is functional for the entire rail-to-rail input range, hence, fully compatible with the fuzzifier output range.

4.3.1 Analysis for Determining Transistor Dimensions in an Inference Cell

In an inference module, at the end of the competition, the voltages of the nodes except the grounded one should be somewhat bigger than $V_{DD} - |V_{TPl}|$. If not,

more than one S_S can be activated. Activation of more than one S_S can be prevented if the dimensions of the transistors are chosen properly. The following analysis leads to determining transistor dimensions for a guaranteed operation.

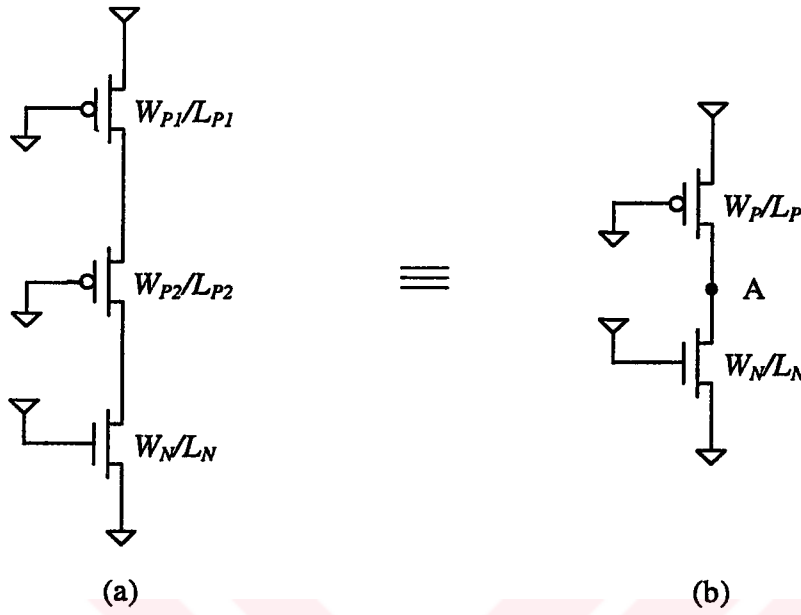


Figure 4.29 (a) Circuit of an inference module loser cell at the end of the selection, and (b) its equivalent.

At the end of the selection process, in the cells except the winner, gate of only one of the parallel connected PMOS transistors is grounded while the others are turned off, because the absolute value of their gate-source voltages can not reach $|V_{TP}|$. In other words, only one of the parallel connected PMOS transistors tries to pull-up the node. This condition is shown in Fig.4.29(a). As can be seen from the figure, it is possible to assume that the transistor located in the middle has negligible body effect on its threshold voltage since its source voltage is very close to V_{DD} . In this case, upper two PMOS transistors can be combined into one with the width/length ratio given below

$$\frac{W_P}{L_P} = \frac{W_{P1}W_{P2}}{W_{P1}L_{P2} + W_{P2}L_{P1}}. \quad (4.128)$$

The equivalent circuit is depicted in Fig.4.29(b). The condition for the reliable operation should be satisfied with the inequality given by

$$V_{DD} - V_A < |V_{TP}| \quad (4.129)$$

where V_A denotes the voltage of node A in Fig.4.29(b). In a typical 1.2 μm CMOS technology, it can be assumed that the absolute values of threshold voltages of PMOS and NMOS transistors are close to each other and smaller than 1V. Under this circumstance, NMOS works in the saturation region while PMOS is in the linear region. Equality of the currents of transistors yields the ratio

$$\frac{\beta_N}{\beta_P} = \frac{2(-V_{DD} - V_{TP})(V_A - V_{DD}) - (V_A - V_{DD})^2}{(V_{DD} - V_{TN})^2} \quad (4.130)$$

where β_N , V_{TN} and β_P , V_{TP} represent the conduction factor, the threshold voltage of NMOS and PMOS devices, respectively. This ratio can also be written as

$$\frac{\beta_N}{\beta_P} = \frac{\mu_n \frac{W_N}{L_N}}{\mu_p \frac{W_P}{L_P}}, \quad (4.131)$$

because of the identical gate oxide thickness. μ_n and μ_p denote the electron and hole mobilities. Dimensions of the transistors can be calculated by using the expression written below

$$\frac{W_N/L_N}{W_P/L_P} = \frac{\mu_p}{\mu_n} \frac{2(-V_{DD} - V_{TP})(V_A - V_{DD}) - (V_A - V_{DD})^2}{(V_{DD} - V_{TN})^2}. \quad (4.132)$$

If $V_{DD}=5\text{V}$, $V_A=4.5\text{V}$, $W_{P1}=20\mu\text{m}$, $W_{P2}=W_N=2\mu\text{m}$, $L_{P1}=L_{P2}=1.2\mu\text{m}$ are chosen $L_N=25.1\mu\text{m}$ is found for AMS 1.2 μm CMOS process parameters. It is clear that transistor dimensions are not influenced by the number of the inputs, but, strongly depend on the process parameters and the supply voltage.

4.3.1 Accuracy of an Inference Cell

Since the operation is based on the voltages registered onto the identical parasitic capacitors at the nodes, precision of this circuit is determined mainly by the mismatches of MOS transistors that may have occurred during the fabrication even if the cells are layed out exactly identical. The mismatch in transistor size affects the

current and parasitic capacitances, whereas the mismatch in the gate oxide thickness affects the threshold voltage and gate capacitances.

An analysis for selectivity of an m -input minnet can be done as follows. In Fig.4.26, assume that all the cells in an m -input minnet circuit are identical except one superior in which the matrix transistors along the cell; $M_{12}, \dots, M_{1m}$, do not match exactly the ones in the other cells but match each other, and pull-down transistor of this cell; M_{D1} , does not match the counterparts in the other cells. The mismatch of the pull-up transistor; M_{U1} , is not influential because it is very wide and its gate is connected to ground, thus, we can assume that its drain is pulled-up to V_{DD} during the selection process. Let us also assume that all the nodes have the same voltage except the superior one at the beginning of the selection. Because of its superiority, the cell including mismatches can be selected as minimum even if its voltage has a positive offset. Now, based on the offset analysis in [109]

$$\frac{I_{C1}}{C_1} = \frac{\beta_{D1}}{2C_1} [2(V_{DD} - V_{Tn1})(V + \Delta V) - (V + \Delta V)^2] - \frac{(m-1)\beta_{12}}{2C_1} (V_{DD} - V + V_{Tp1})^2 \quad (4.133a)$$

$$\frac{I_{C2}}{C_2} = \frac{\beta_{D2}}{2C_2} [2(V_{DD} - V_{Tn2})V - V^2] - \frac{(m-2)\beta_{21}}{2C_2} (V_{DD} - V + V_{Tp2})^2 - \frac{\beta_{21}}{2C_2} (V_{DD} - V - \Delta V + V_{Tp2})^2 \quad (4.133b)$$

can be written for the superior cell and one of the other exactly identical cells, respectively. Here, C_1 and C_2 stand for the lumped parasitic capacitances of the exclusive and ordinary nodes, respectively; I_{C1} and I_{C2} are the currents flowing through these capacitors, β_{D1} and β_{D2} denote the conduction factors of pull-down transistors, and β_{12} and β_{21} represent that of matrix transistors. This case indicates that all the cells in the circuit enter the selection process having equal initial conditions. In other words, the superiority originating from the mismatch can be significantly overcome by applying an additional offset voltage; ΔV , to the input node of exclusive cell. The right-hand sides of these equations should be equalized in order to find the maximum offset voltage. By doing this and arranging the resulting equality with the mismatch definitions given below;

$$\begin{aligned}
\beta_{D1} &= \beta_D + \Delta\beta_D & \beta_{D2} &= \beta_D, & C_1 &= C + \Delta C & C_2 &= C, \\
V_{Tn1} &= V_{Tn} - \Delta V_T & V_{Tn2} &= V_{Tn}, & V_{Tp1} &= V_{Tp} - \Delta V_T & V_{Tp2} &= V_{Tp}, \\
\beta_{12} &= \beta - \Delta\beta & \beta_{21} &= \beta
\end{aligned}$$

we can find the offset voltage as

$$\Delta V = \frac{\left\{ 2\beta_D \Delta V_T V + \Delta\beta_D [2(V_{DD} - V_{Tn})V - V^2] + 2(m-1)\beta \Delta V_T (V_{DD} - V + V_{Tp}) + (m-1)\Delta\beta (V_{DD} - V + V_{Tp})^2 - \frac{\Delta C}{C} \beta_D [2(V_{DD} - V_{Tn})V - V^2] + \frac{\Delta C}{C} (m-1)\beta (V_{DD} - V + V_{Tp})^2 \right\}}{2\beta(V_{DD} - V + V_{Tp}) - 2\beta_D(V_{DD} - V + V_{Tn})} \quad (4.134)$$

With the assumption of $|V_{Tp}| \sim |V_{Tn}| \sim |V_T|$ for a typical $1,2\mu\text{m}$ CMOS process, previously published device-mismatch data of

$$\frac{\Delta C}{C} = 1\%, \quad \frac{\Delta\beta}{\beta} = 1\%, \quad \frac{\Delta V_T}{V_T} = 2\%$$

[111, 112, 113], the device dimensions given in Section 4.3.1 and for $V_{DD}=5\text{V}$, $|V_T|=0,75\text{V}$ and $V=2,5\text{V}$ the offset voltage can be expressed as

$$\Delta V = 37\text{mV}(m-1) + 3\text{mV}. \quad (4.135)$$

For the described worst case above, HSPICE simulation and calculation results are given in Table 4.4 for 2, 4 and 7-input minnets.

Table 4.4 Offset analysis results for minnet circuits

Number of the inputs	ΔV calculated	ΔV simulated
2	40 mV	50 mV
4	115 mV	120 mV
7	225 mV	250 mV

4.4 Defuzzifier

Inference engine outputs denote the membership degrees on the classes of the output variables. Defuzzifier generates crisp output control signals from these output membership grades. Although there are several different defuzzification methodologies, a defuzzifier calculates the center of gravity of singleton output classes in almost all analog hardware-implemented fuzzy controllers. Proposed defuzzifier circuit here computes weighted-average of singletons which corresponds to the center of gravity of singleton output classes. Such a defuzzification involves simple addition, weighted addition, and division operations. Each of these is performed by a dedicated unit, as depicted by the block diagram in Fig.4.30.

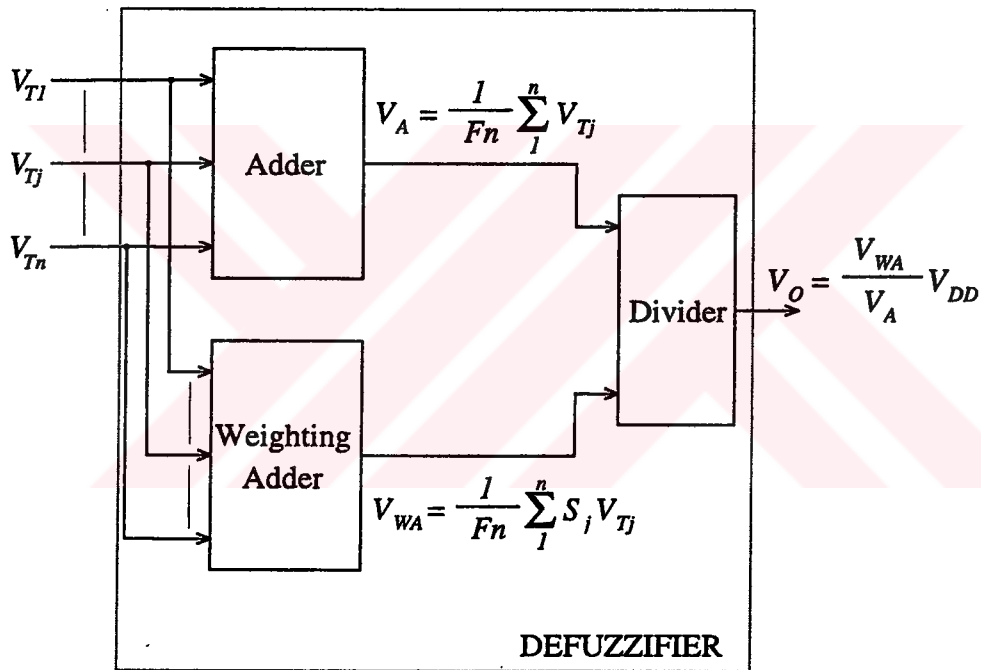


Figure 4.30 Block diagram of a defuzzifier that calculates the weighted-average of singletons.

Both adder and weighted-adder are fed by the same inference engine outputs, V_{Tj} , because defuzzification involves a division which contains weighted-average and average of inference engine outputs. Weighted-average is obtained by taking V_{Tj} s as membership grades on associated singleton output classes; S_j s. F is a multiplicand less than unity which will be described in Section 4.4.1. In the next sections, defuzzifier subblocks will be examined in detail.

4.4.1 Adders

The circuit schematic of both types of adders is given in Fig.4.31. It is a multiple input derivative of the sample-and-hold architecture shown in Fig.4.9. Note that the inputs, V_{Tj} , $j=1, \dots, n$, arriving from inference modules are received in a reset phase. Since, V_{Tj} can be in the range of ground- V_{DD} , analog switches are used for the inputs. Here again, resetting of OPI is obtained via an NMOS transistor. C is connected to ground by an NMOS switch. Input node charge of OPI can be expressed as

$$Q_r = (V_r - V_{T1})C_1 + \dots + (V_r - V_{Tj})C_j + \dots + (V_r - V_{Tn})C_n + V_r C \quad (4.136a)$$

in reset phase. In the evaluation phase, all input columns are connected to ground by an NMOS switch for each, and a feedback capacitance C is connected via an analog switch to the output. The charge at the input node can be written as

$$Q_e = V_e C_1 + \dots + V_e C_j + \dots + V_e C_n + (V_e - V_{output})C. \quad (4.136b)$$

Charge preservation is also valid here in this phase because of the high-impedance state. So, equality of two expressions describes

$$V_{output} = \sum_{j=1}^n \frac{C_j}{C} V_{Tj} \quad (4.137)$$

by utilizing $V_e - V_r$ relation given in (4.2), (4.7) and again by assuming that OPI has high gain around its logic threshold. If the capacitors on all input columns are identical, i.e., $C_j = C_I, \forall j$, the circuit implements simple addition, i.e.,

$$V_A = \frac{C_I}{C} \sum_{j=1}^n V_{Tj}. \quad (4.138)$$

In order to prevent the adder from saturation, however, this sum should never exceed V_{DD} . An obvious way to comply with this requirement is to select $C_I/C=1/n$. This would ensure nonsaturation even when all inputs to the adder are at V_{DD} . In a properly designed rule base, however, such an extreme input vector is impossible to occur because, it would imply a controller input condition that fits all rules with 100

percent truth value. Usually, the maximum possible value of the sum is a fraction of $n V_{DD}$, i.e.,

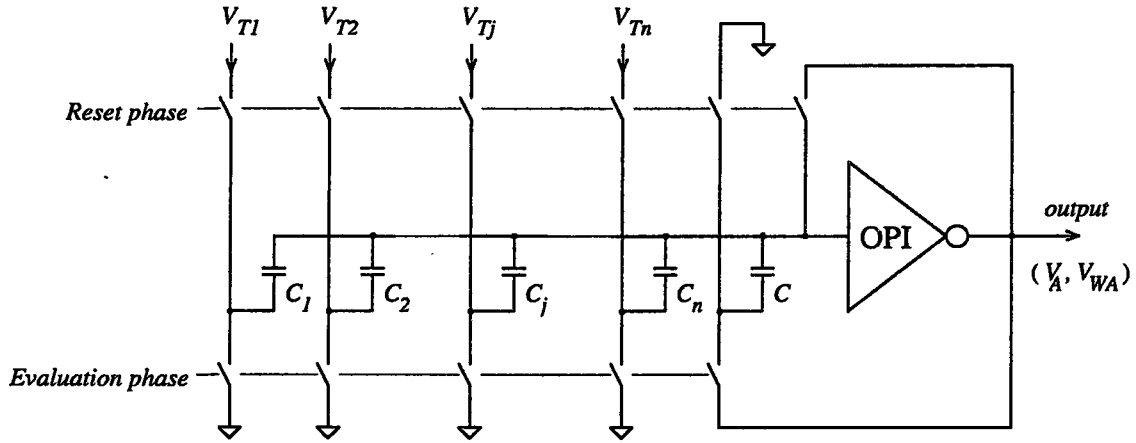


Figure 4.31 n -input adder/weighted-adder schematic.

$$\sum_{j=1}^n \frac{C_j}{C} V_{Tj} \Big|_{max} = Fn V_{DD}, \quad (4.139)$$

where, factor F is considerably less than unity. Assuming that F has been determined by analysing the control surface of the controller, it is more resonable to implement the capacitance ratio in accordance with $C_1/C=1/Fn$ because this not only results in smaller size for C , but also yields an amplified adder output as described by

$$V_A = \frac{1}{Fn} \sum_{j=1}^n V_{Tj}. \quad (4.140)$$

Provided that the weighted addition is also amplified by the same factor $1/F$, the quotient of the final division operation will not change. Only the precision of division will improve as a result of this amplification.

A weighted adder can be implemented by sizing input capacitors in accordance with

$$C_j = S_j C / Fn.$$

Thus, output voltage is obtained from (4.135) as

$$V_{WA} = \frac{1}{Fn} \sum_{j=1}^n S_j V_{Tj} . \quad (4.141)$$

Since singleton values S_j are not greater than unity, this output voltage cannot exceed the adder output voltage given by (4.140). This also ensures that the weighting adder cannot saturate.

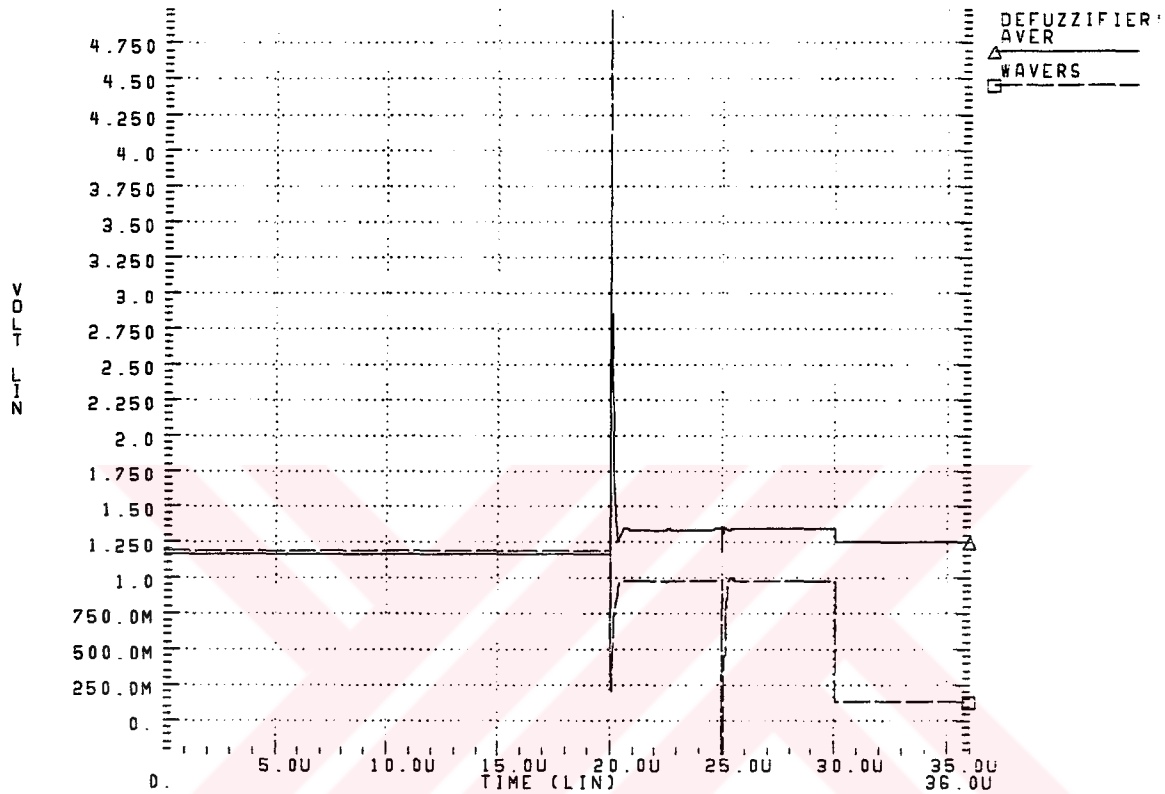


Figure 4.32 HSPICE simulation output plots of the average and the weighted-average circuits. Solid line shows the average and dashed line is the weighted-average. They are valid within 20-30 μ s.

Fig.4.32 shows the simulation output plots of an average and a weighted-average circuits. Both configurations have 16 inputs with $F=0.2$. The capacitor values and input voltages to these adders are in Table 4.5. Calculation and simulation results are given in Table 4.6.

Table 4.5 The capacitor and input voltage values simulated in adder circuits.

Capacitor Name	Value in Adder	Value in W-Adder	Input name	Input Voltage
C	160 fF	160 fF		
C_1	50 fF	20 fF	V_{T1}	0.5 V
C_2	50 fF	20 fF	V_{T2}	0.5 V
C_3	50 fF	30 fF	V_{T3}	0.0 V
C_4	50 fF	20 fF	V_{T4}	0.5 V
C_5	50 fF	30 fF	V_{T5}	0.2 V
C_6	50 fF	40 fF	V_{T6}	0.0 V
C_7	50 fF	20 fF	V_{T7}	0.0 V
C_8	50 fF	40 fF	V_{T8}	0.0 V
C_9	50 fF	40 fF	V_{T9}	0.0 V
C_{10}	50 fF	50 fF	V_{T10}	1.0 V
C_{11}	50 fF	50 fF	V_{T11}	1.0 V
C_{12}	50 fF	50 fF	V_{T12}	0.0 V
C_{13}	50 fF	20 fF	V_{T13}	0.0 V
C_{14}	50 fF	20 fF	V_{T14}	0.0 V
C_{15}	50 fF	30 fF	V_{T15}	0.5 V
C_{16}	50 fF	20 fF	V_{T16}	0.0 V

Table 4.6 Calculated and simulated values of adder outputs.

	Calculation	Simulation
Average	1.312 V	1.340 V
Weighted-average	0.944 V	0.970 V

4.4.2 Divider

A schematic of the divider unit is given in Fig.4.33. A current-based equivalent of the proposed division method can be found in [114]. It comprises a stack of q comparators, whose outputs, V_{Cp} , $p=1, \dots, q$, are fed into an output adder, which generates the crisp system output V_O . The adder configuration is exactly like

the one shown in Fig.4.31. Its input capacitors are sized in accordance with $C_p = C/q$, for every p , which yields from (4.137)

$$V_o = \frac{1}{q} \sum_{p=1}^q V_{Cp} . \quad (4.142)$$

Each comparator is built with two capacitors, C_{p1} and C_{p2} , and a cascade of two ordinary CMOS inverters, the first of which is resettable [115, 107]. In a reset phase, all these first inverter stages in the entire stack are reset to the logic threshold; V_{thC} , by an NMOS transistor for each. In the mean time, bottom plates of all C_{p1} receive the adder signal V_A via an analog switch, which is described by (4.138). In this phase, the bottom plates of C_{p2} are tied to ground by an NMOS device. Note that reset is removed slightly before the switches controlling capacitor bottom plates are turned off. This helps avoid a random offset that might otherwise result from charge injection onto the capacitor bottom-plate columns. In the following phase, the weighted-adder signal V_{WA} of (4.141) is imposed on all C_{p2} , while all C_{p1} are grounded.

The charge accumulated in the reset phase onto the input node of comparator p will be preserved in the following phase because of the high-impedance state, therefore,

$$(V_{rC} - V_A)C_{p1} + V_{rC}C_{p2} = V_{eC}C_{p1} + (V_{eC} - V_{WA})C_{p2} \quad (4.143)$$

can be written. V_{rC} , V_{eC} are respectively the reset and the evaluation voltages of the comparator input node. Here, V_{rC} corresponds to the logic threshold of the comparator; V_{thC} . Fig.4.34 shows a representative transfer characteristics of an inverter cascade.

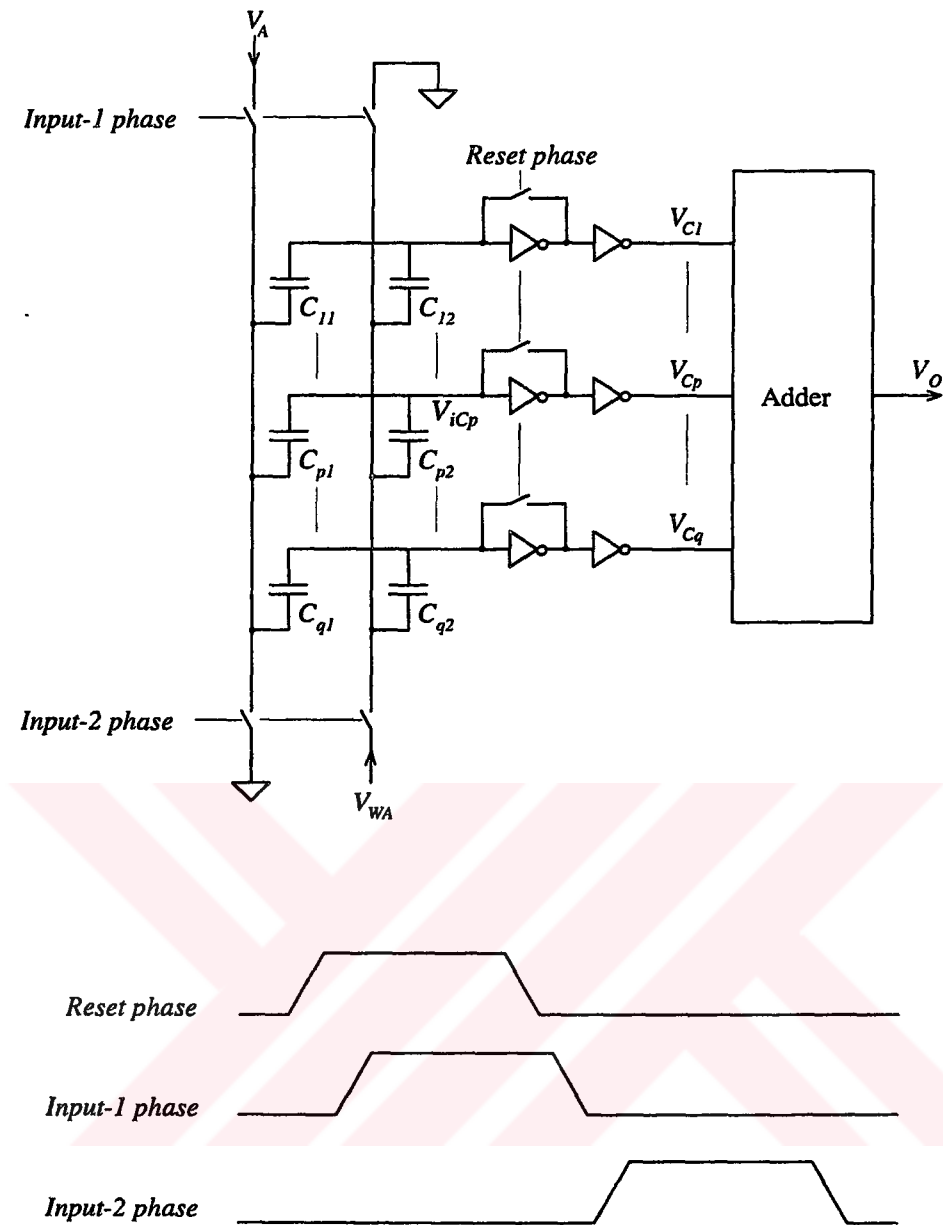


Figure 4.33 Schematic of divider and the phases it uses.

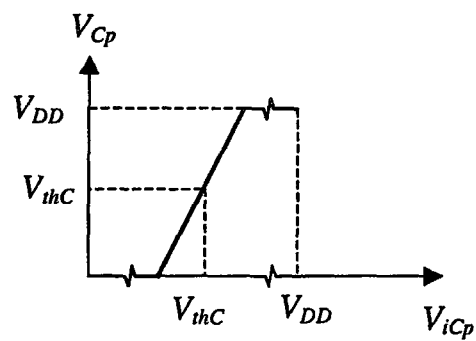


Figure 4.34 Representative transfer characteristics of inverter cascade in a comparator.

Arrangement of (4.143) gives

$$V_{eC} - V_{rC} = \frac{C_{p2}}{C_{p1} + C_{p2}} V_{WA} - \frac{C_{p1}}{C_{p1} + C_{p2}} V_A. \quad (4.144)$$

According to this equation, the resulting voltage perturbation at the input of an inverter cascade is positive if

$$\frac{V_{WA}}{V_A} = \frac{C_{p1}}{C_{p2}}; \quad (4.145)$$

otherwise, a negative perturbation occurs. Assuming that the inverter cascade has a sufficiently high gain, then, output from the cascade is described by

$$V_{Cp} = V_{DD} \quad \text{if} \quad \frac{V_{WA}}{V_A} > T_p, \quad (4.146a)$$

$$V_{Cp} = 0 \quad \text{if} \quad \frac{V_{WA}}{V_A} < T_p, \quad (4.146b)$$

where, the comparator threshold T_p is defined by

$$T_p \equiv \frac{C_{p1}}{C_{p2}}. \quad (4.147)$$

By selecting capacitance ratios in accordance with

$$\frac{C_{p1}}{C_{p2}} = \frac{2p-1}{2q}, \quad (4.148)$$

we create q equally spaced thresholds in the range 0 to 1. If V_{WA}/V_A exceeds a total of r thresholds, then, precisely r out of q comparators transfer a V_{DD} to output adder; and, according to (4.142), the adder responds by generating a system output of

$$V_o = \frac{r}{q} V_{DD}, \quad (4.149)$$

where, r/q is a quantized representation of V_{WA}/V_A . Fig.4.35 gives an idea about the quantization in the divider.

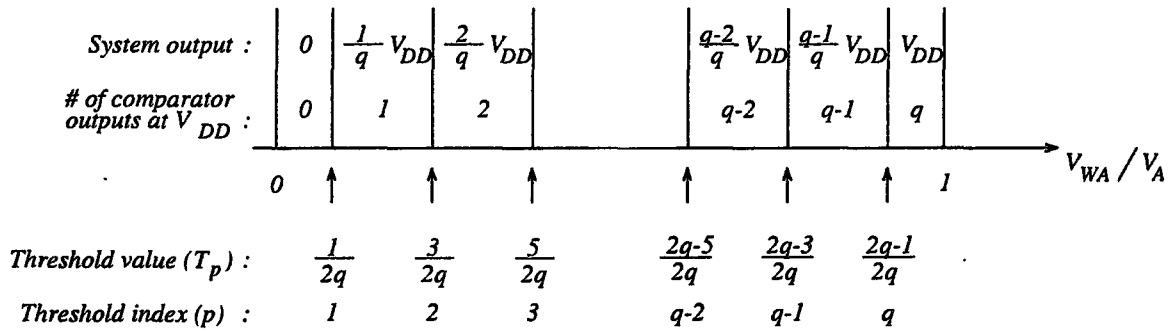
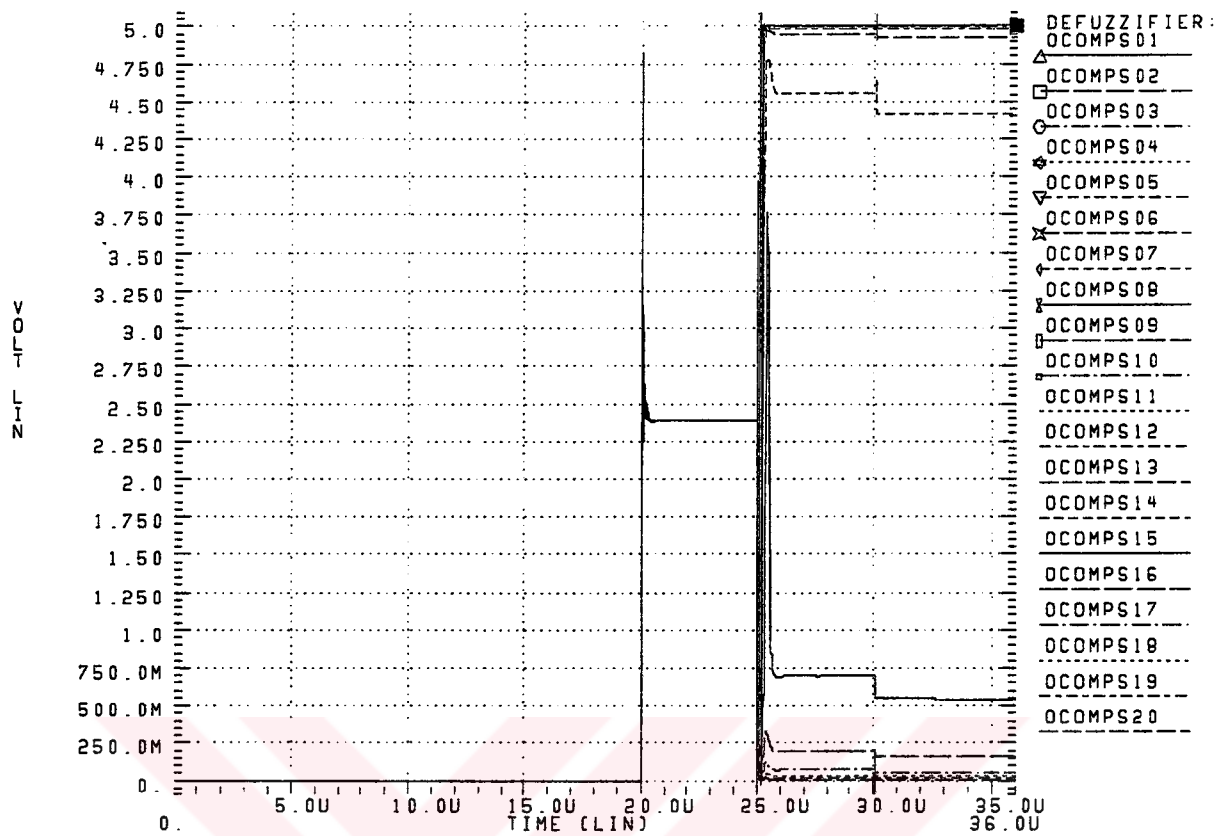


Figure 4.35 Quantization levels.

It is obvious that the defuzzifier module computes (4.142), and presents the outcome as a quantized system-output voltage in a full rail to rail range with a maximum quantization error $\pm V_{DD}/2q$.

Stability of the adder circuits including OPI is achieved by utilizing the same compensation scheme described in Section 4.2.4. Increase in the number of the inputs does not influence the symbolic analysis results given in Sections 4.2.4.2-3. By properly changing the value of C_i , required values of compensation components can be determined.

Fig.4.36(a) and (b) show the plots of a simulated divider. It has a stack of 20-comparators and a 20-input adder, it means that, 0V-5V range is separated by equally spaced 20 thresholds. The inputs are $V_A=1.340V$ and $V_{WA}=0.970V$, calculated divider output is $V_O=3.619V$. Expected and simulated comparator outputs are given in Table 4.7. By using the simulated comparator results, the output can be calculated as $V_O=3.525V$. Output adder simulation results in 3.530V for this value.



(a)

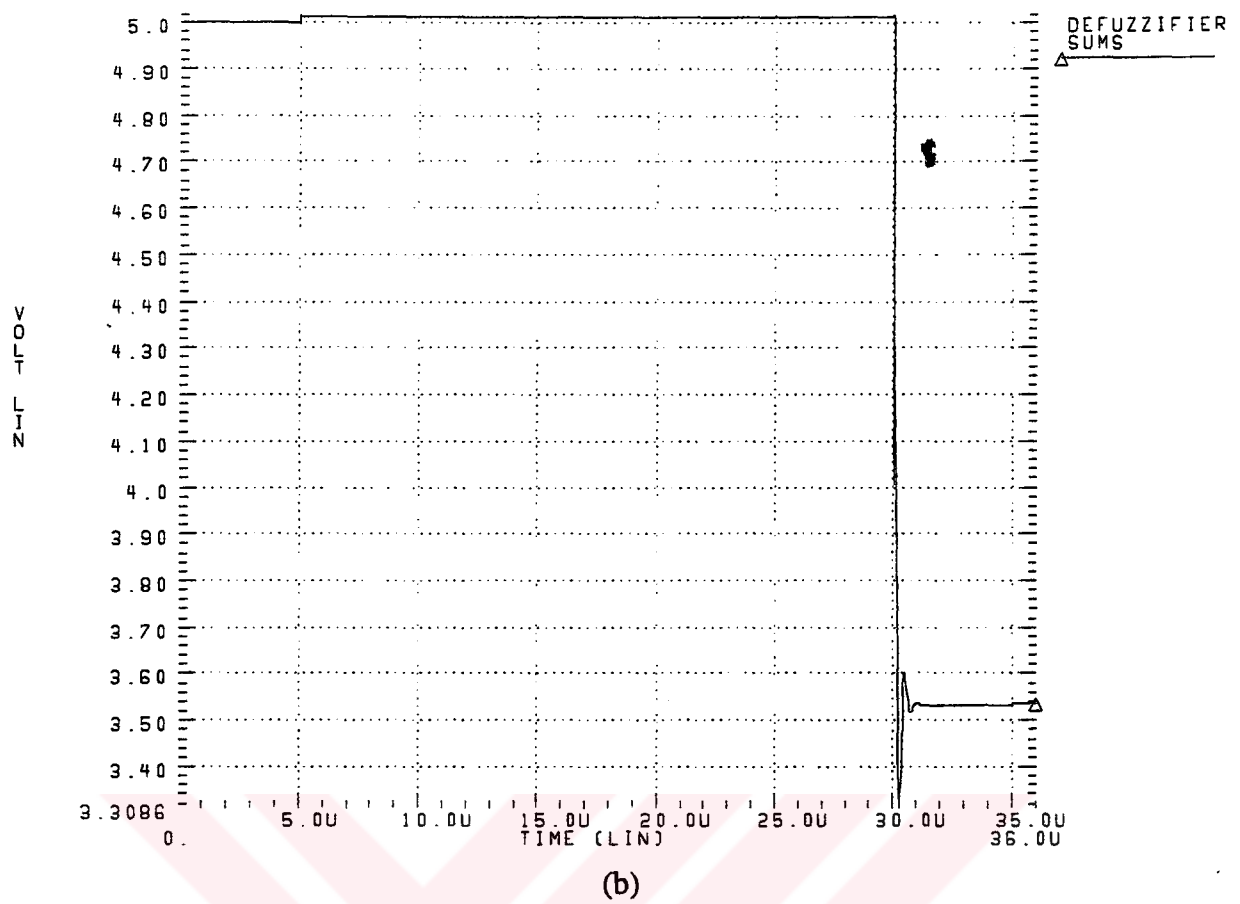


Figure 4.36 Divider simulation plots. (a) the outputs of 20 comparators are valid between 25-30 μ s, and (b) the output of adder in the divider is valid between 30-35 μ s.

Table 4.7 Simulation results and expected values for given inputs.

Comparator outputs	Expected value	Simulation result
V_{C1}	5.000 V	5.000 V
V_{C2}	5.000 V	5.000 V
V_{C3}	5.000 V	5.000 V
V_{C4}	5.000 V	5.000 V
V_{C5}	5.000 V	5.000 V
V_{C6}	5.000 V	5.000 V
V_{C7}	5.000 V	5.000 V
V_{C8}	5.000 V	5.000 V
V_{C9}	5.000 V	5.000 V
V_{C10}	5.000 V	5.000 V
V_{C11}	5.000 V	4.990 V
V_{C12}	5.000 V	4.980 V
V_{C13}	5.000 V	4.950 V
V_{C14}	5.000 V	4.560 V
V_{C15}	0.000 V	0.700 V
V_{C16}	0.000 V	0.197 V
V_{C17}	0.000 V	0.073 V
V_{C18}	0.000 V	0.033 V
V_{C19}	0.000 V	0.018 V
V_{C20}	0.000 V	0.011 V

4.4.3 Nonideality Analysis of the Defuzzifier Subblocks

Parasitic details and capacitor mismatch characteristics have already been given for a switched-capacitor OPI circuit. In an adder structure, their effect can be analyzed similarly to what has been done previously for a positive ramp generator in Section 4.2.5. Here again, let us depict the gate-drain/source overlap capacitance of the reset transistor with C_{ov} , lumped parasitic capacitance of OPI's input node with C_S and mismatch in capacitors with ΔC_i s. By rewriting reset and evaluation charges including these capacitors and by adding the injected channel charge, we can get a more realistic equation for an adder circuit;

$$\begin{aligned}
& \sum_{j=1}^n (V_r - V_{Tj})(C_j + \Delta C_j) + V_r C + (V_r - V_{DD})C_{ov} + V_r C_s + \Delta Q \\
& = \sum_{j=1}^n V_e (C_j + \Delta C_j) + (V_e - V_{output})C + V_e C_{ov} + V_e C_s.
\end{aligned} \tag{4.150}$$

By utilizing the relationships given by (4.2) and (4.7), rearrangement of this equation yields .

$$V_{output} = K_a \left[\sum_{j=1}^n \frac{C_j}{C} V_{Tj} + \sum_{j=1}^n \frac{\Delta C_j}{C} V_{Tj} + \frac{C_{ov}}{C} V_{DD} - \frac{\Delta Q}{C} + \frac{\sum_{j=1}^n (C_j + \Delta C_j) + C + C_{ov} + C_s}{AC} V_{th} \right] \tag{4.151}$$

where

$$K_a \equiv \frac{AC}{(1+A)C + \sum_{j=1}^n (C_j + \Delta C_j) + C_{ov} + C_s}.$$

It is assumed that K_a is equal to 1 with a good approximation and its influence can be neglected as explained in Section 4.2.5. The first term in the paranthesis in (4.151) is the ideal output and other terms show the deviation from the ideal output voltage. By neglecting the last term because of the open-loop gain

$$\Delta V_{output} = \sum_{j=1}^n \frac{\Delta C_j}{C} V_{Tj} + \frac{C_{ov}}{C} V_{DD} - \frac{\Delta Q}{C}. \tag{4.152}$$

can be written for the deviation. In a fuzzy controller only the active rules participate in the addition, meaning that, a few V_{Tj} s are different from zero.

As previously done for the ramp generators; assuming a) an injection of one half the channel charge of a typical minimum geometry $2 \mu\text{m} \times 1.2 \mu\text{m}$ NMOS reset switch, b) a gate-drain/source overlap capacitance of 0.6fF, c) a typical C of 160fF and C_j of 50fF, and d) full truthness percentage of 20 (corresponding to F); this equation yields an output voltage error of approximately 80mV. About 30mV excess stems from clock feedthrough and is evident in the simulation results given in Table

4.6. However, this error can be compensated for simply by adding a small-capacitor column into the inputs of the adder as shown in Fig.4.37.

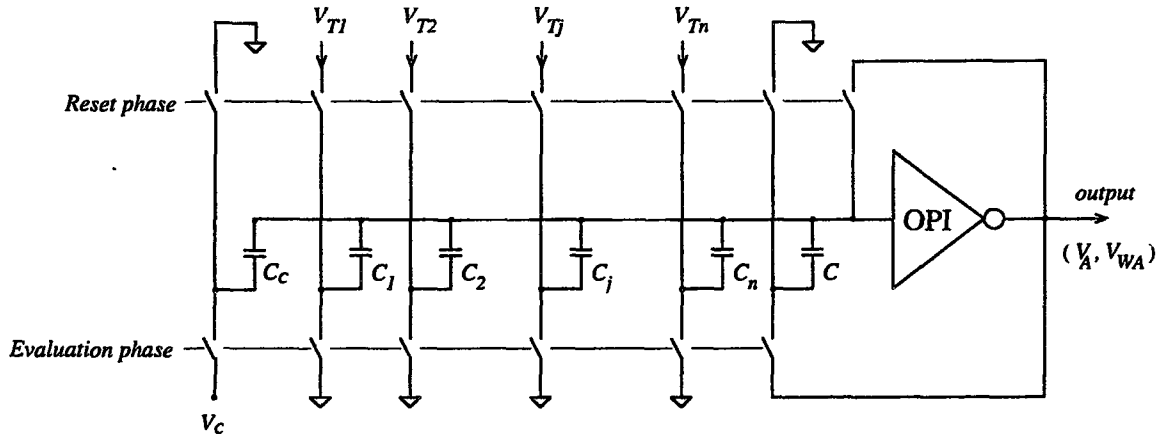


Figure 4.37 n -input adder/weighted-adder schematic with the output error compensation column. C_c is the compensation capacitor.

In this case, the output voltage equation can be expressed, excluding the capacitor mismatch, as

$$V_{output} = \sum_{j=1}^n \frac{C_j}{C} V_{Tj} + \frac{C_{ov}}{C} V_{DD} - \frac{\Delta Q}{C} - \frac{C_c}{C} V_c \quad (4.153)$$

where V_c denotes the compensation voltage. Cancelling the error in the output voltage can be achieved by selecting C_c and V_c in accordance with

$$C_c V_c = C_{ov} V_{DD} - \Delta Q. \quad (4.154)$$

For the typical values of $C_{ov}=0.6\text{fF}$, $V_{DD}=5\text{V}$ and $\Delta Q=-2\text{fC}$, total cancellation can be achieved by choosing $C_c=5\text{fF}$ and $V_c=1\text{V}$.

An adder output that is very close to supply voltages has an additional nonideality as due to the degrading gain of OPI near the rail levels as mentioned in the last paragraph of Section 4.2.5. This effect is not discussed here again, however, it can be said that the resulting deviation is very similar to the case discussed in that section because the configurations are the same.

Similar parasitics affect the operation of the comparators in the divider. By using the same representation for the overlap and the stray capacitors in a comparator

row, as depicted in Fig.4.24, in the reset and evaluation phases, input node charge equations can be rewritten as

$$Q_{rC} = (V_{rC} - V_A)C_{p1} + V_{rC}C_{p2} + (V_{rC} - V_{DD})C_{ov} + V_{rC}C_s, \quad (4.155a)$$

$$Q_{eC} = V_{eC}C_{p1} + (V_{eC} - V_{WA})C_{p2} + V_{eC}C_{ov} + V_{eC}C_s. \quad (4.155b)$$

Charge injection from the resetting transistor is again taken case of the expression

$$Q_{eC} = Q_{rC} + \Delta Q. \quad (4.155c)$$

Thus,

$$V_{eC} - V_{rC} = \frac{C_{p2}}{C_{p1} + C_{p2} + C_{ov} + C_s} V_{WA} - \frac{C_{p1}}{C_{p1} + C_{p2} + C_{ov} + C_s} V_A - \frac{C_{ov}}{C_{p1} + C_{p2} + C_{ov} + C_s} V_{DD} + \frac{\Delta Q}{C_{p1} + C_{p2} + C_{ov} + C_s}. \quad (4.156)$$

If the condition;

$$C_{p1} + C_{p2} \gg C_{ov} + C_s \quad (4.157)$$

is satisfied, last two terms in (4.156) denote the error in the voltage perturbation at the input node of a comparator. Compensation of this perturbation error originated from both channel charge and overlap capacitor is possible by using a dummy switch built with an NMOS transistor [107] with its drain shorted to source as depicted in Fig.4.38. Width of this transistor is one half of the resetting transistor, whereas the length is the same. Transistor is activated by a clock signal which should be the complementary of the reset phase. By this method, the feedthrough to the input node is reduced by having two feedthrough signals of nearly equal but opposite sign.

Another nonideality, originating from the comparators, can be observed in Fig.4.36(a); the transition from 0V to 5V in the values of comparator outputs does not occur abruptly because of the transfer characteristics of inverter cascades in comparators. The characteristics are shown in Fig.4.39. It is obvious that a finite gain exists and the large gain around V_{thC} can not be maintained near the rail levels, hence, a graded transition from 0V to 5V in neighbour comparator outputs is

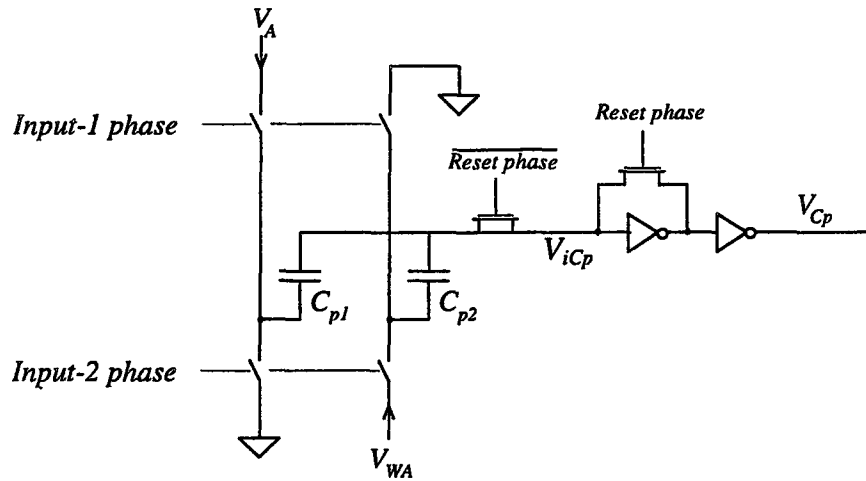


Figure 4.38 Schematic of a comparator row with compensation transistor.

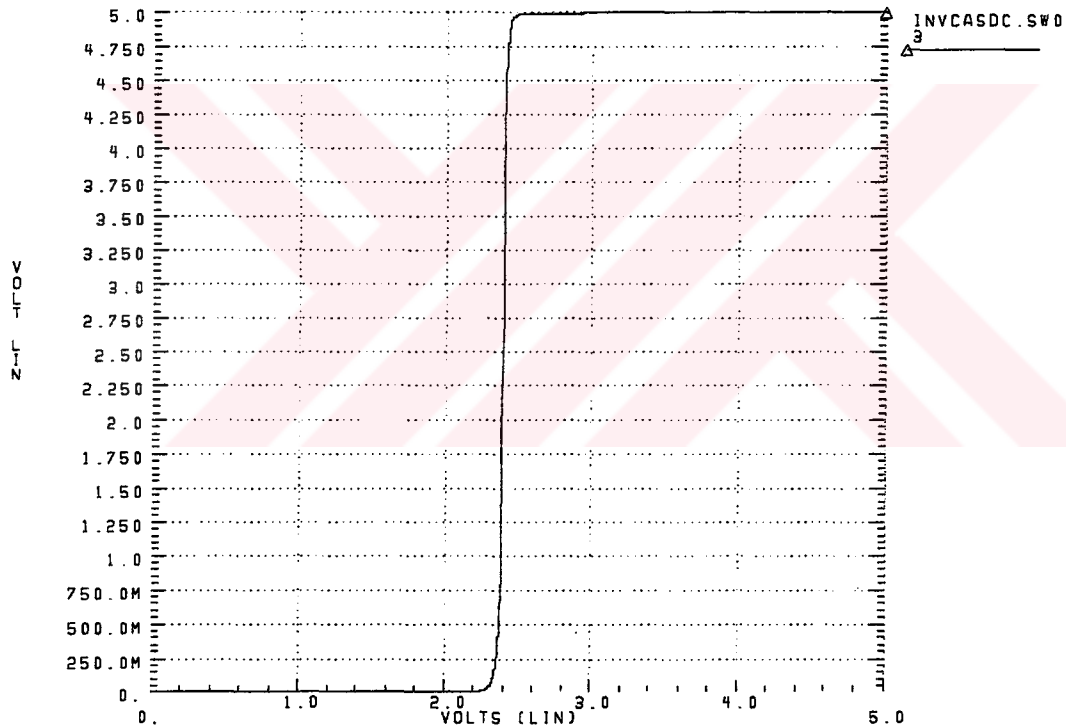


Figure 4.39 DC transition characteristics of the inverter cascade in the comparator.

inevitable. Sharpness may be provided by using 3 or more inverter stages instead of 2, but, for this type of dividing operation, cascading of 2 ordinary inverters is sufficient. Moreover, this graded transition may be useful for such a quantized system, since it can cause a partial correction in the value of analog divider output, if the quantization error is considered as the dominant weakness of this circuit.

1% relative mismatch in capacitor values originating from fabrication is not much influential on the comparator operation in the case of 20-level quantization, because, it brings 1% input perturbation error. Essentially, there is a $\pm 125\text{mV}$ quantization error for 20 quantization levels with a 5V supply voltage.



5. A FUZZY CONTROLLER PROTOTYPE IMPLEMENTED WITH THE PROPOSED APPROACH

In this chapter, a physically implemented fuzzy-controller designed with the proposed sampled-analog structures is presented. The prototype was designed to control a vacuum cleaner to be manufactured by Arcelik Inc.. Specifications were provided by Arcelik Inc. and are introduced in Section 5.1. The controller was laid out in Cadence Design Framework 4.2.1 and was fabricated by Austria Mikro Systeme in 1.2 μ m double-poly double-metal CMOS technology. The system has 4 inputs, 2 outputs and executes 16 rules.

5.1 Description of the Sample Controller

Inputs of the controller are; 1) Change Direction Switch, 2) Dust, 3) Vacuum and 4) Surface Type. They are respectively identified with subscripts *C*, *D*, *V* and *S* in the text. The chip is designed to take the analog information from the four input sensors as voltages and to generate two output control signals also as voltages. The outputs are; 1) Suction Power and 2) Brush Speed, associated with subscripts *SP* and *BS*, respectively. Analog input voltages can change in the range 0V-5V, which are the supply voltages, and generated output voltages vary in the same range as well. All the circuits in the system have rail-to-rail functionality, so, no voltage compression or expansion process is needed. Data is processed totally in analog mode by sampled-analog circuits in the entire controller without any A/D and/or D/A conversion. The only digital part of the chip is the phase generator which inevitably exists to control data flow from input to output.

5.1.1 Description of Input Membership Classes

Fig.5.1 shows all input membership functions in the prototype. Axes in the figure depict input voltages while ordinates show membership grades. Corresponding ramp function names are also depicted in the figure. Membership grade values between 0 and 1 linearly correspond to the voltages between 0V-5V, and $V_{DD}=5V$.

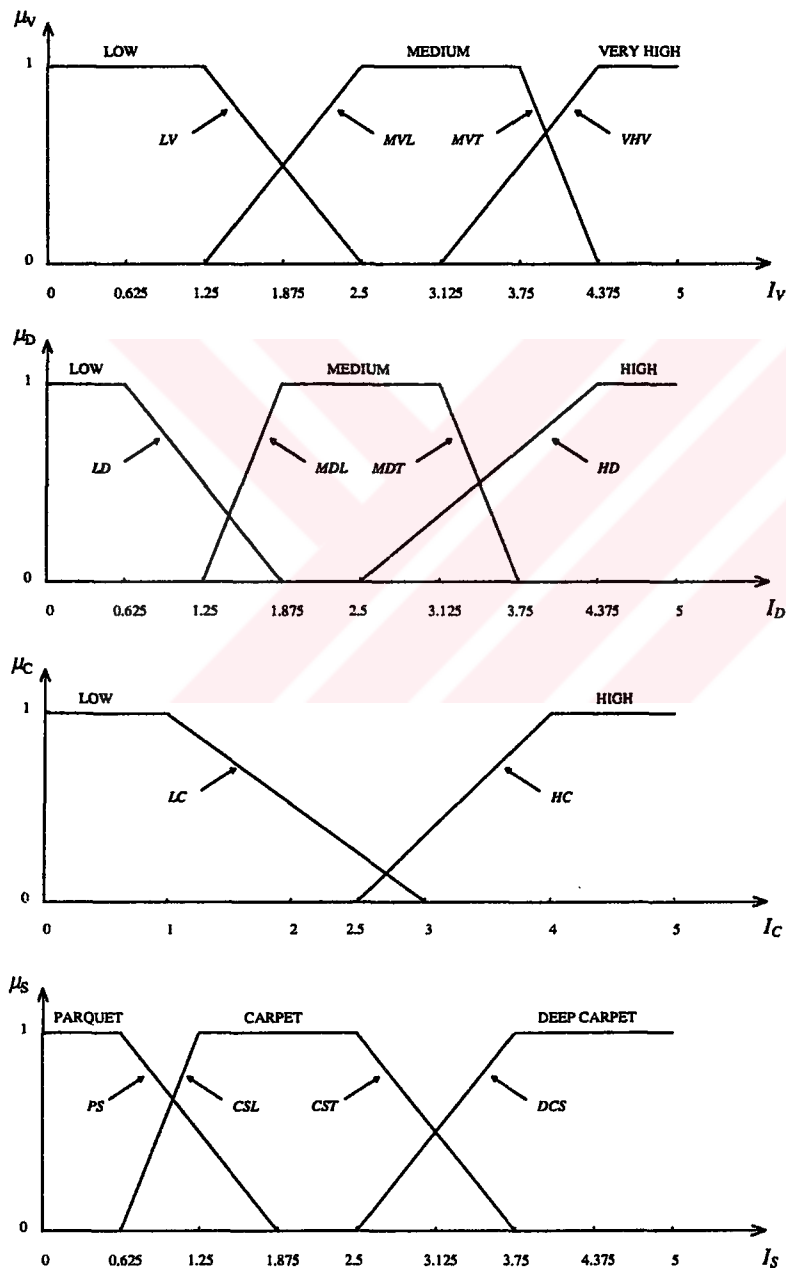


Figure 5.1 Input membership function descriptions of the prototype.

Descriptions of the ramp generators implemented in the fuzzifier are given in Table 5.1. As can be seen, for the membership functions containing leading and trailing edges such as ‘medium’ classes in the Fig.5.1, two ramp generators should be realized. For the functions with only one edge, only one ramp generator is sufficient. Given membership functions in the figure can be implemented with a total of 14 ramp generators.

Table 5.1 Descriptions of the ramp functions implemented in the prototype.

Ramp function	Piecewise linear functions constituting the membership functions		
<i>LC</i>	5 for $I_C < 1$,	$7.5 - 2.5I_C$ for $1 \leq I_C \leq 3$,	0 for $I_C > 3$
<i>HC</i>	0 for $I_C < 2.5$,	$-8.33 + 3.33I_C$ for $2.5 \leq I_C \leq 4$,	5 for $I_C > 4$
<i>LD</i>	5 for $I_D < 0.625$,	$7.5 - 4I_D$ for $0.625 \leq I_D \leq 1.875$,	0 for $I_D > 1.875$
<i>MDL</i>	0 for $I_D < 1.25$,	$-10 + 8I_D$ for $1.25 \leq I_D \leq 1.875$,	5 for $I_D > 1.875$
<i>MDT</i>	5 for $I_D < 3.125$,	$30 - 8I_D$ for $3.125 \leq I_D \leq 3.75$,	0 for $I_D > 3.75$
<i>HD</i>	0 for $I_D < 2.5$,	$-6.67 + 2.67I_D$ for $2.5 \leq I_D \leq 4.375$,	5 for $I_D > 4.375$
<i>LV</i>	5 for $I_V < 1.25$,	$10 - 4I_V$ for $1.25 \leq I_V \leq 2.5$,	0 for $I_V > 2.5$
<i>MVL</i>	0 for $I_V < 1.25$,	$-5 + 4I_V$ for $1.25 \leq I_V \leq 2.5$,	5 for $I_V > 2.5$
<i>MVT</i>	5 for $I_V < 3.75$,	$35 - 8I_V$ for $3.75 \leq I_V \leq 4.375$,	0 for $I_V > 4.375$
<i>VHV</i>	0 for $I_V < 3.125$,	$-12.5 + 4I_V$ for $3.125 \leq I_V \leq 4.375$,	5 for $I_V > 4.375$
<i>PS</i>	5 for $I_S < 0.625$,	$7.5 - 4I_S$ for $0.625 \leq I_S \leq 1.875$,	0 for $I_S > 1.875$
<i>CSL</i>	0 for $I_S < 0.625$,	$-5 + 8I_S$ for $0.625 \leq I_S \leq 1.25$,	5 for $I_S > 1.25$
<i>CST</i>	5 for $I_S < 2.5$,	$15 - 4I_S$ for $2.5 \leq I_S \leq 3.75$,	0 for $I_S > 3.75$
<i>DCS</i>	0 for $I_S < 2.5$,	$-10 + 4I_S$ for $2.5 \leq I_S \leq 3.75$,	5 for $I_S > 3.75$

5.1.2 Descriptions of the Output Membership Classes

In Fig.5.2 locations of the singleton output classes; $S_{j,s}$, are depicted. Here again, axes are the output voltages and the membership grade values [0,1] corresponding to the voltage range of 0V-5V.

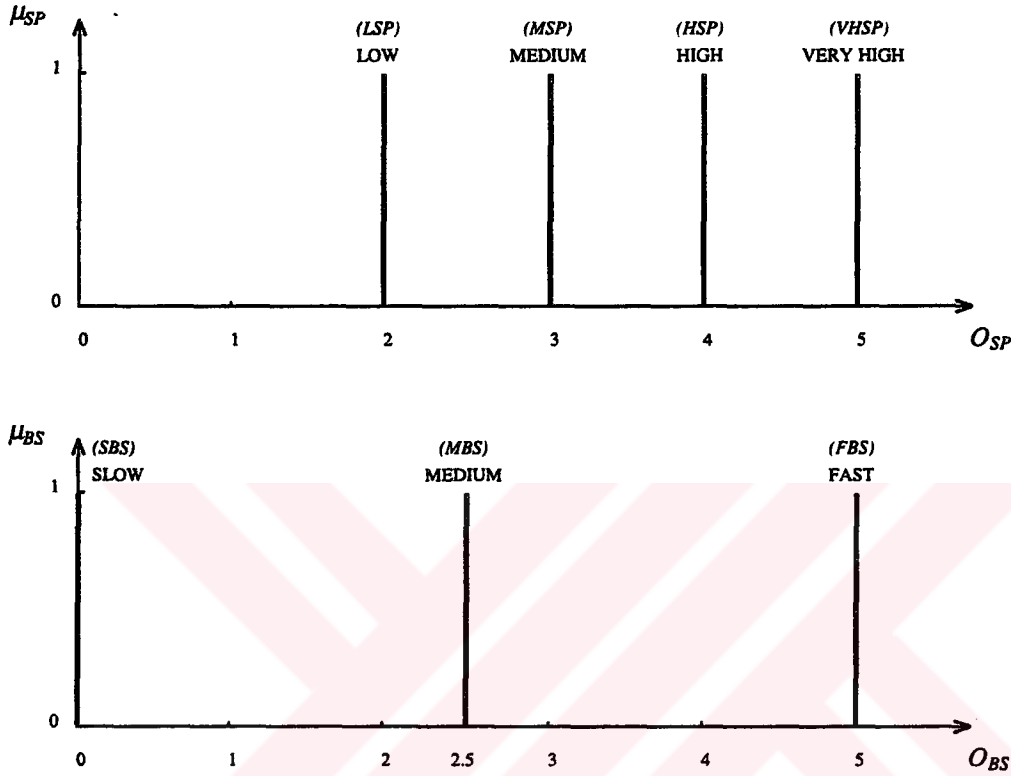


Figure 5.2 Output singleton classes.

5.1.3 Description of the Rules

16 rules with a total of 64 antecedent terms are described in Table 5.2. Antecedent and consequent terms, which are included in IF and THEN parts in a fuzzy rule, fill second and third columns of the table, respectively. Rule-1 may be given as an example;

IF $D=LOW$ AND $C=LOW$ AND $S=PARQUET$, THEN $SP=LOW$, $BS=SLOW$.

Execution of the rules is realized by minimum-selecting inference modules, one for each rule. The inference engine consists of 16 inference modules, and has 14 inputs/16 outputs. Nevertheless, maximum input number is 7 for the inference modules like in Rule-5, since the number of the inputs of a module is determined by

the number of the antecedent terms in a rule. Truth values of Rule- j , $j=1, \dots, 16$, were represented by V_{Tj} in chapter 4.

Table 5.2 The rules executed by the prototype.

Rules	Antecedents	Consequents
Rule-1	$LD \wedge LC \wedge PS$	LSP, SBS
Rule-2	$MDL \wedge MDT \wedge LC \wedge PS$	LSP, SBS
Rule-3	$HD \wedge LC \wedge PS$	MSP, SBS
Rule-4	$LD \wedge LC \wedge CSL \wedge CST$	LSP, SBS
Rule-5	$MVL \wedge MVT \wedge MDL \wedge MDT \wedge LC \wedge CSL \wedge CST$	MSP, MBS
Rule-6	$HD \wedge LC \wedge CSL \wedge CST$	HSP, FBS
Rule-7	$MVL \wedge MVT \wedge LD \wedge LC \wedge DCS$	LSP, MBS
Rule-8	$MDL \wedge MDT \wedge LC \wedge DCS$	HSP, FBS
Rule-9	$HD \wedge LC \wedge DCS$	HSP, FBS
Rule-10	$HC \wedge PS$	$VHSP, FBS$
Rule-11	$HC \wedge CSL \wedge CST$	$VHSP, FBS$
Rule-12	$HC \wedge DCS$	$VHSP, FBS$
Rule-13	$VHV \wedge LD \wedge LC \wedge DCS$	LSP, SBS
Rule-14	$VHV \wedge MDL \wedge MDT \wedge LC \wedge CSL \wedge CST$	LSP, SBS
Rule-15	$LV \wedge MDL \wedge MDT \wedge LC \wedge CSL \wedge CST$	MSP, MBS
Rule-16	$LV \wedge LD \wedge LC \wedge DCS$	LSP, MBS

5.1.4 Description of the Defuzzifier

Defuzzification is accomplished with the method of weighted-average of singletons as mentioned before. F is determined as 0.2 by using a BASIC program specifically written for this exemplar controller. Program input file is provided in App.D. The control surface was scanned by this program with properly selected

incremental steps for every input variable. Defuzzifier consists of two weighted adders, one adder, two 20-quanta dividers and two output adders since it generates two outputs. In the defuzzifier, the adder finds the average;

$$V_A = \frac{1}{0,2.16} \sum_{j=1}^n V_{Tj} ,$$

and the weighted-averages for Suction Power and Brush Speed are found in accordance with

$$V_{WASP} = \frac{1}{0,2.16} [0,4(V_{T1} + V_{T2} + V_{T4} + V_{T7} + V_{T13} + V_{T14} + V_{T16}) + 0,6(V_{T3} + V_{T5} + V_{T15}) + 0,8(V_{T6} + V_{T8} + V_{T9}) + 1(V_{T10} + V_{T11} + V_{T12})]$$

and

$$V_{WABS} = \frac{1}{0,2.16} [0,5(V_{T5} + V_{T7} + V_{T10} + V_{T15} + V_{T16} + V_{T14} + V_{T16}) + 1(V_{T6} + V_{T8} + V_{T9} + V_{T11} + V_{T12})]$$

Finally, we can get two crisp system outputs as the results of the dividing operations on the average and the weighted-averages;

$$O_{SP} = \frac{V_{WASP}}{V_A} .5$$

and

$$O_{BS} = \frac{V_{WABS}}{V_A} .5$$

5.2 Capacitor Values and Transistor Dimensions in the Prototype

5.2.1 In the Fuzzifier

Table 5.3 Transistor dimensions and capacitor values in OPI circuits.

Name	P/N ramp circuits; W:L	S/H circuits; W:L
$M1$	2 μm : 2,5 μm	2 μm : 2,5 μm
$M2$	2 μm : 2,5 μm	2 μm : 2,5 μm
$M3$	4 μm : 2,5 μm	4 μm : 2,5 μm
$M4$	12 μm : 2,5 μm	12 μm : 2,5 μm
$M5$	2 μm : 1,2 μm	2 μm : 1,2 μm
$M6$	2 μm : 1,2 μm	2 μm : 1,2 μm
$M7$	4 μm : 1,2 μm	4 μm : 1,2 μm
$M8$	12 μm : 1,2 μm	12 μm : 1,2 μm
M_r	2 μm : 1,2 μm	2 μm : 1,2 μm
M_c	2 μm : 2 μm	2 μm : 5 μm
M_n	2 μm : 3 μm	2 μm : 3 μm
M_p	2 μm : 3 μm	2 μm : 3 μm
C_{C1}	150 fF	100 fF
C_{C2}	20 fF	70 fF

Table 5.4 Values of C_1 , C_2 and C in ramp generator and S/H circuits.

S/H, Ramp function	C_1 [fF]	C_2 [fF]	C [fF]
S/H	500	---	500
<i>LC</i>	250	149	100
<i>HC</i>	333	174	100
<i>LD</i>	400	150	100
<i>MDL</i>	800	211	100
<i>MDT</i>	791	598	100
<i>HD</i>	266	140	100
<i>LV</i>	400	200	100
<i>MVL</i>	400	107	100
<i>MVT</i>	800	705	100
<i>VHV</i>	400	257	100
<i>PS</i>	400	150	100
<i>CSL</i>	800	111	100
<i>CST</i>	400	300	100
<i>DCS</i>	400	207	100

5.2.2 In the Inference Engine

Table 5.5 Transistor dimensions implemented in an inference module.

M_{matrix} ; W:L	M_U ; W:L	M_D ; W:L	Other
2 μm : 1.2 μm	20 μm : 1.2 μm	2 μm : 25 μm	2 μm : 1.2 μm

5.2.3 In the Defuzzifier

Table 5.6 Transistor dimensions and capacitor values of OPI circuits implemented in the adders.

Name	Average	Weighed-average	Output adder
$M1$	$2\ \mu\text{m} : 2,5\ \mu\text{m}$	$2\ \mu\text{m} : 2,5\ \mu\text{m}$	$2\ \mu\text{m} : 2,5\ \mu\text{m}$
$M2$	$2\ \mu\text{m} : 2,5\ \mu\text{m}$	$2\ \mu\text{m} : 2,5\ \mu\text{m}$	$2\ \mu\text{m} : 2,5\ \mu\text{m}$
$M3$	$4\ \mu\text{m} : 2,5\ \mu\text{m}$	$4\ \mu\text{m} : 2,5\ \mu\text{m}$	$4\ \mu\text{m} : 2,5\ \mu\text{m}$
$M4$	$12\ \mu\text{m} : 2,5\ \mu\text{m}$	$12\ \mu\text{m} : 2,5\ \mu\text{m}$	$12\ \mu\text{m} : 2,5\ \mu\text{m}$
$M5$	$2\ \mu\text{m} : 1,2\ \mu\text{m}$	$2\ \mu\text{m} : 1,2\ \mu\text{m}$	$2\ \mu\text{m} : 1,2\ \mu\text{m}$
$M6$	$2\ \mu\text{m} : 1,2\ \mu\text{m}$	$2\ \mu\text{m} : 1,2\ \mu\text{m}$	$2\ \mu\text{m} : 1,2\ \mu\text{m}$
$M7$	$4\ \mu\text{m} : 1,2\ \mu\text{m}$	$4\ \mu\text{m} : 1,2\ \mu\text{m}$	$4\ \mu\text{m} : 1,2\ \mu\text{m}$
$M8$	$12\ \mu\text{m} : 1,2\ \mu\text{m}$	$12\ \mu\text{m} : 1,2\ \mu\text{m}$	$12\ \mu\text{m} : 1,2\ \mu\text{m}$
M_r	$2\ \mu\text{m} : 1,2\ \mu\text{m}$	$2\ \mu\text{m} : 1,2\ \mu\text{m}$	$2\ \mu\text{m} : 1,2\ \mu\text{m}$
M_c	$2\ \mu\text{m} : 30\ \mu\text{m}$	$2\ \mu\text{m} : 20\ \mu\text{m}$	$2\ \mu\text{m} : 30\ \mu\text{m}$
M_n	$2\ \mu\text{m} : 6\ \mu\text{m}$	$2\ \mu\text{m} : 6\ \mu\text{m}$	$2\ \mu\text{m} : 6\ \mu\text{m}$
M_p	$2\ \mu\text{m} : 6\ \mu\text{m}$	$2\ \mu\text{m} : 6\ \mu\text{m}$	$2\ \mu\text{m} : 6\ \mu\text{m}$
C_{C1}	150 fF	150 fF	150 fF
C_{C2}	35 fF	35 fF	100 fF

Table 5.7 Capacitor values implemented in adder circuits.

Capacitor	Adder	W-adder (SP)	W-adder (BS)	Output adder
C	160 fF	160 fF	160 fF	500 fF
C_1	50 fF	20 fF	0 fF	25 fF
C_2	50 fF	20 fF	0 fF	25 fF
C_3	50 fF	30 fF	0 fF	25 fF
C_4	50 fF	20 fF	0 fF	25 fF
C_5	50 fF	30 fF	25 fF	25 fF
C_6	50 fF	40 fF	50 fF	25 fF
C_7	50 fF	20 fF	25 fF	25 fF
C_8	50 fF	40 fF	50 fF	25 fF
C_9	50 fF	40 fF	50 fF	25 fF
C_{10}	50 fF	50 fF	25 fF	25 fF
C_{11}	50 fF	50 fF	50 fF	25 fF
C_{12}	50 fF	50 fF	50 fF	25 fF
C_{13}	50 fF	20 fF	0 fF	25 fF
C_{14}	50 fF	20 fF	0 fF	25 fF
C_{15}	50 fF	30 fF	25 fF	25 fF
C_{16}	50 fF	20 fF	25 fF	25 fF
C_{17}	---	---	---	25 fF
C_{18}	---	---	---	25 fF
C_{19}	---	---	---	25 fF
C_{20}	---	---	---	25 fF

Table 5.8 Transistor dimensions in a comparator.

Transistor	W [μm]	L [μm]
Inverter PMOS	2	1.2
Inverter NMOS	2	2.5
Reset	2.2	1.2
Compensation	2	1.2

Table 5.9 Capacitor values implemented in comparator stack.

Quantum	T_p	C_{p1}	C_{p2}
1	0.05	20 fF	400 fF
2	0.10	38 fF	382 fF
3	0.15	55 fF	365 fF
4	0.20	70 fF	350 fF
5	0.25	84 fF	336 fF
6	0.30	97 fF	323 fF
7	0.35	109 fF	311 fF
8	0.40	120 fF	300 fF
9	0.45	130 fF	290 fF
10	0.50	140 fF	280 fF
11	0.55	149 fF	271 fF
12	0.60	158 fF	262 fF
13	0.65	165 fF	255 fF
14	0.70	173 fF	247 fF
15	0.75	180 fF	240 fF
16	0.80	187 fF	233 fF
17	0.85	193 fF	227 fF
18	0.90	199 fF	221 fF
19	0.95	205 fF	215 fF
20	1.00	210 fF	210 fF

Note that the sum of the input capacitor values for each comparator is the same since that ensures the parasitic input capacitance of each comparator to be equal.

5.3 Implementation and Test Results

Pre-layout and post-layout simulations were run on HSPICE for the entire controller. The data of these simulations are given in Table 5.10 and 5.11.

Table 5.10 Pre-layout simulation data of the prototype.

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] simulated	O_{BS} [V] calculated	O_{BS} [V] simulated
1.000	1.250	0.625	0.625	2.000	2.000	0.000	0.035
1.000	1.250	0.625	2.500	2.000	2.000	0.000	0.030
1.000	1.250	0.625	3.750	2.000	2.000	2.500	2.490
1.000	1.250	1.875	0.625	2.000	2.000	0.000	0.035
1.000	1.250	1.875	2.500	3.000	2.990	2.500	2.500
1.000	1.250	1.875	3.750	4.000	3.980	5.000	4.930
1.000	1.250	4.375	0.625	3.000	2.990	0.000	0.036
1.000	1.250	4.375	2.500	4.000	3.980	5.000	4.930
1.000	1.250	4.375	3.750	4.000	3.980	5.000	4.930
1.000	2.500	0.625	0.625	2.000	2.000	0.000	0.029
1.000	2.500	0.625	2.500	2.000	2.000	0.000	0.028
1.000	2.500	0.625	3.750	2.000	2.000	2.500	2.490
1.000	2.500	1.875	0.625	2.000	2.000	0.000	0.028
1.000	2.500	1.875	2.500	3.000	2.990	2.500	2.490
1.000	2.500	1.875	3.750	4.000	3.980	5.000	4.930
1.000	2.500	4.375	0.625	3.000	2.990	0.000	0.038
1.000	2.500	4.375	2.500	4.000	3.980	5.000	4.930
1.000	2.500	4.375	3.750	4.000	3.980	5.000	4.930
1.000	4.375	0.625	0.625	2.000	1.990	0.000	0.014
1.000	4.375	0.625	2.500	2.000	2.000	0.000	0.034
1.000	4.375	0.625	3.750	2.000	2.000	0.000	0.037
1.000	4.375	1.875	0.625	2.000	2.000	0.000	0.035
1.000	4.375	1.875	2.500	2.000	2.000	0.000	0.034
1.000	4.375	1.875	3.750	4.000	3.980	5.000	4.930
1.000	4.375	4.375	0.625	3.000	2.990	0.000	0.036
1.000	4.375	4.375	2.500	4.000	3.980	5.000	4.930
1.000	4.375	4.375	3.750	4.000	3.980	5.000	4.930
2.700	1.500	1.500	1.250	3.078	3.030	1.717	1.740
2.700	1.500	1.500	3.125	3.196	3.220	3.068	3.020
2.700	1.500	3.250	1.250	3.521	3.500	2.456	2.480
2.700	1.500	3.250	3.125	3.965	3.950	4.260	4.250
2.700	1.500	3.750	1.250	4.203	4.190	3.086	3.050
2.700	1.500	3.750	3.125	4.468	4.420	5.000	4.840
2.700	3.125	1.500	1.250	3.091	3.050	1.581	1.560
2.700	3.125	1.500	3.125	3.438	3.460	3.265	3.260
2.700	3.125	3.250	1.250	3.612	3.550	2.449	2.480
2.700	3.125	3.250	3.125	4.132	4.050	4.566	4.510
2.700	3.125	3.750	1.250	4.202	4.190	3.086	3.080
2.700	3.125	3.750	3.125	4.468	4.420	5.000	4.840
2.700	3.750	1.500	1.250	2.930	2.920	1.347	1.300
2.700	3.750	1.500	3.125	3.068	3.020	2.424	2.440
2.700	3.750	3.250	1.250	3.373	3.300	2.086	2.040
2.700	3.750	3.250	3.125	3.817	3.770	3.891	3.800
2.700	3.750	3.750	1.250	4.203	4.190	3.086	3.060
2.700	3.750	3.750	3.125	4.468	4.420	5.000	4.840

Table 5.10 Continued.

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] simulated	O_{BS} [V] calculated	O_{BS} [V] simulated
3.100	1.500	1.500	1.250	5.000	4.920	3.750	3.740
3.100	1.500	1.500	3.125	5.000	4.920	5.000	4.920
3.100	1.500	3.250	1.250	5.000	4.920	3.750	3.740
3.100	1.500	3.250	3.125	5.000	4.920	5.000	4.920
3.100	1.500	3.750	1.250	5.000	4.920	3.750	3.740
3.100	1.500	3.750	3.125	5.000	4.920	5.000	4.920
3.100	3.125	1.500	1.250	5.000	4.920	3.750	3.740
3.100	3.125	1.500	3.125	5.000	4.920	5.000	4.920
3.100	3.125	3.250	1.250	5.000	4.920	3.750	3.740
3.100	3.125	3.250	3.125	5.000	4.920	5.000	4.920
3.100	3.125	3.750	1.250	5.000	4.920	3.750	3.740
3.100	3.125	3.750	3.125	5.000	4.910	5.000	4.910
3.100	3.750	1.500	1.250	5.000	4.920	3.750	3.740
3.100	3.750	1.500	3.125	5.000	4.920	5.000	4.920
3.100	3.750	3.250	1.250	5.000	4.920	3.750	3.740
3.100	3.750	3.250	3.125	5.000	4.920	5.000	4.920
3.100	3.750	3.750	1.250	5.000	4.930	3.750	3.740
3.100	3.750	3.750	3.125	5.000	4.920	5.000	4.920
4.000	1.250	0.625	0.625	5.000	4.930	2.500	2.490
4.000	1.250	0.625	2.500	5.000	4.930	5.000	4.930
4.000	1.250	0.625	3.750	5.000	4.930	5.000	4.930
4.000	1.250	1.875	0.625	5.000	4.930	2.500	2.490
4.000	1.250	1.875	2.500	5.000	4.930	5.000	4.930
4.000	1.250	1.875	3.750	5.000	4.930	5.000	4.930
4.000	1.250	4.375	0.625	5.000	4.930	2.500	2.490
4.000	1.250	4.375	2.500	5.000	4.930	5.000	4.930
4.000	1.250	4.375	3.750	5.000	4.930	5.000	4.930
4.000	2.500	0.625	0.625	5.000	4.930	2.500	2.490
4.000	2.500	0.625	2.500	5.000	4.930	5.000	4.930
4.000	2.500	0.625	3.750	5.000	4.930	5.000	4.930
4.000	2.500	1.875	0.625	5.000	4.930	2.500	2.500
4.000	2.500	1.875	2.500	5.000	4.930	5.000	4.930
4.000	2.500	1.875	3.750	5.000	4.930	5.000	4.930
4.000	2.500	4.375	0.625	5.000	4.930	2.500	2.490
4.000	2.500	4.375	2.500	5.000	4.930	5.000	4.930
4.000	2.500	4.375	3.750	5.000	4.930	5.000	4.930
4.000	4.375	0.625	0.625	5.000	4.930	2.500	2.490
4.000	4.375	0.625	2.500	5.000	4.930	5.000	4.930
4.000	4.375	0.625	3.750	5.000	4.930	5.000	4.930
4.000	4.375	1.875	0.625	5.000	4.930	2.500	2.500
4.000	4.375	1.875	2.500	5.000	4.930	5.000	4.930
4.000	4.375	1.875	3.750	5.000	4.930	5.000	4.930
4.000	4.375	4.375	0.625	5.000	4.930	2.500	2.490
4.000	4.375	4.375	2.500	5.000	4.930	5.000	4.930
4.000	4.375	4.375	3.750	5.000	4.930	5.000	4.930

Table 5.11 Post-layout simulation data of the prototype.

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculation	O_{SP} [V] simulation	O_{BS} [V] calculation	O_{BS} [V] simulation
0.000	5.000	0.000	0.000	2.000	2.000	0.000	0.288
1.000	1.250	1.250	0.625	2.000	2.140	0.000	0.291
2.000	0.000	5.000	1.500	3.625	3.730	3.125	3.260
2.500	2.500	1.500	2.000	2.500	2.800	1.250	1.690
2.800	1.300	1.700	0.850	3.610	3.760	2.210	2.500
3.500	3.500	1.000	1.000	5.000	4.770	3.680	3.650
3.500	3.850	3.200	3.500	5.000	4.760	5.000	4.760
4.000	1.000	3.500	3.500	5.000	4.760	5.000	4.760
5.000	4.000	1.000	5.000	5.000	4.770	5.000	4.770

The integrated controller together with the phase generator contains 2004 MOS transistors and 263 poly-to-poly capacitors, and occupies an area of 1,76mm². Fig.5.3 shows the photomicrographs of fundamental blocks in the controller prototype. Fig 5.4 shows the photomicrograph of the entire test chip.

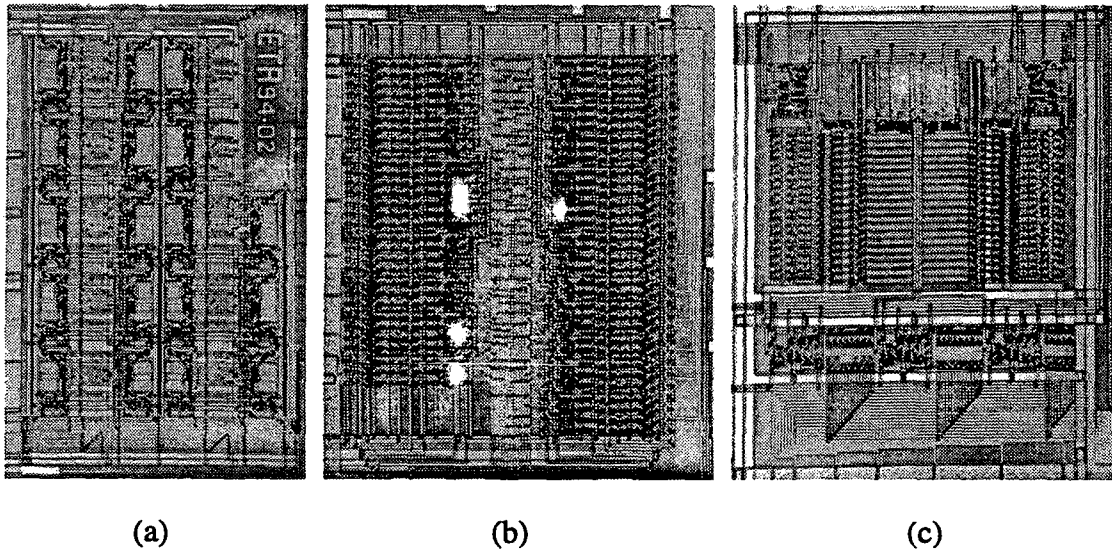


Figure 5.3 The photomicrograph of (a) fuzzifier block including 14 ramp generators and 4 sample and hold units, (b) inference engine block executing 16 rules, and (c) defuzzifier block generating 2 outputs.

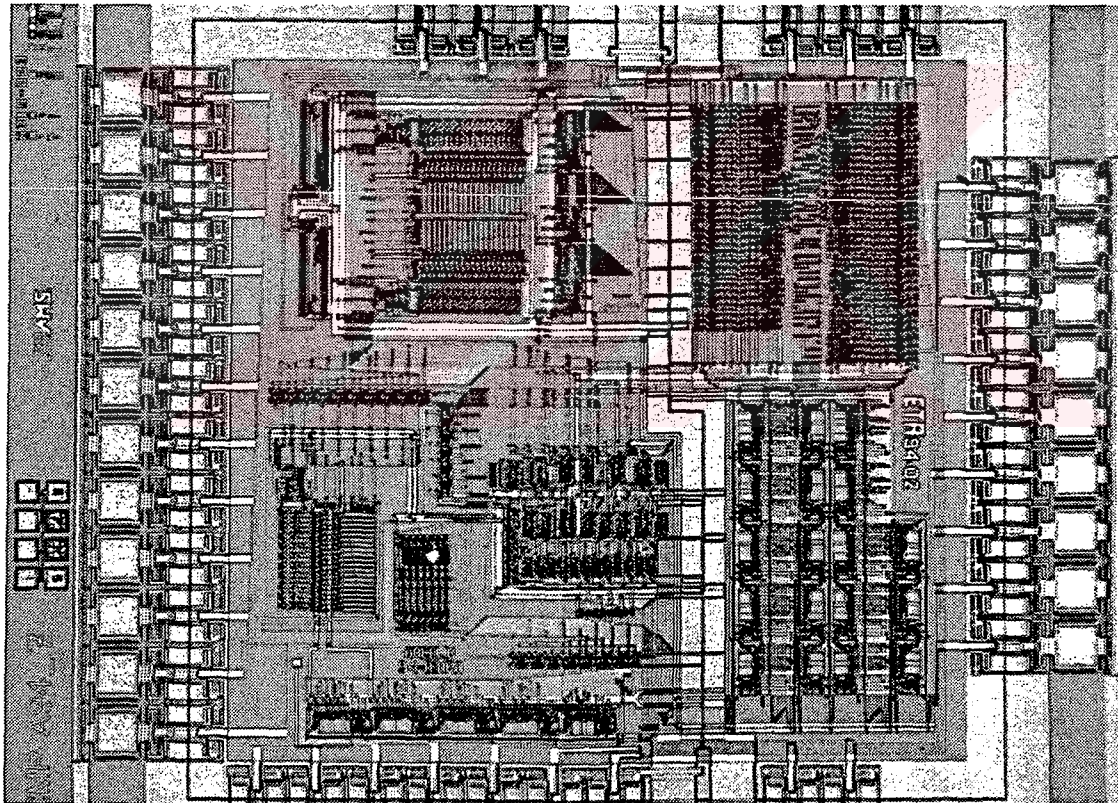


Figure 5.4 The chip photomicrograph. The fuzzifier, inference engine and defuzzifier are distinguishable, the block in the middle is phase generator and some stand-alone modules for characterization are located around the phase generator.

Fig.5.5 shows the measured transfer characteristics of four stand-alone fuzzifier modules. These four ramp outputs correspond to three labels (one trapezoidal and two ramp membership functions) of one input variable. The traces were obtained by applying a ramp to the input from 0V to 5V. Sampling frequency is 80k per second (corresponding to a master clock frequency of 480kHz). Targeted corner voltages V^- and V^+ are 0,625V and 1,875V for Fig.5.5(a), 1,250V and 1,875V for Fig.5.5(b), 3,125V and 3,750V for Fig.5.5(c) and 2,500V and 4,375V for Fig.5.5(d). Measured characteristics are very close to intended ones showing very good linearity in almost full rail-to-rail range.

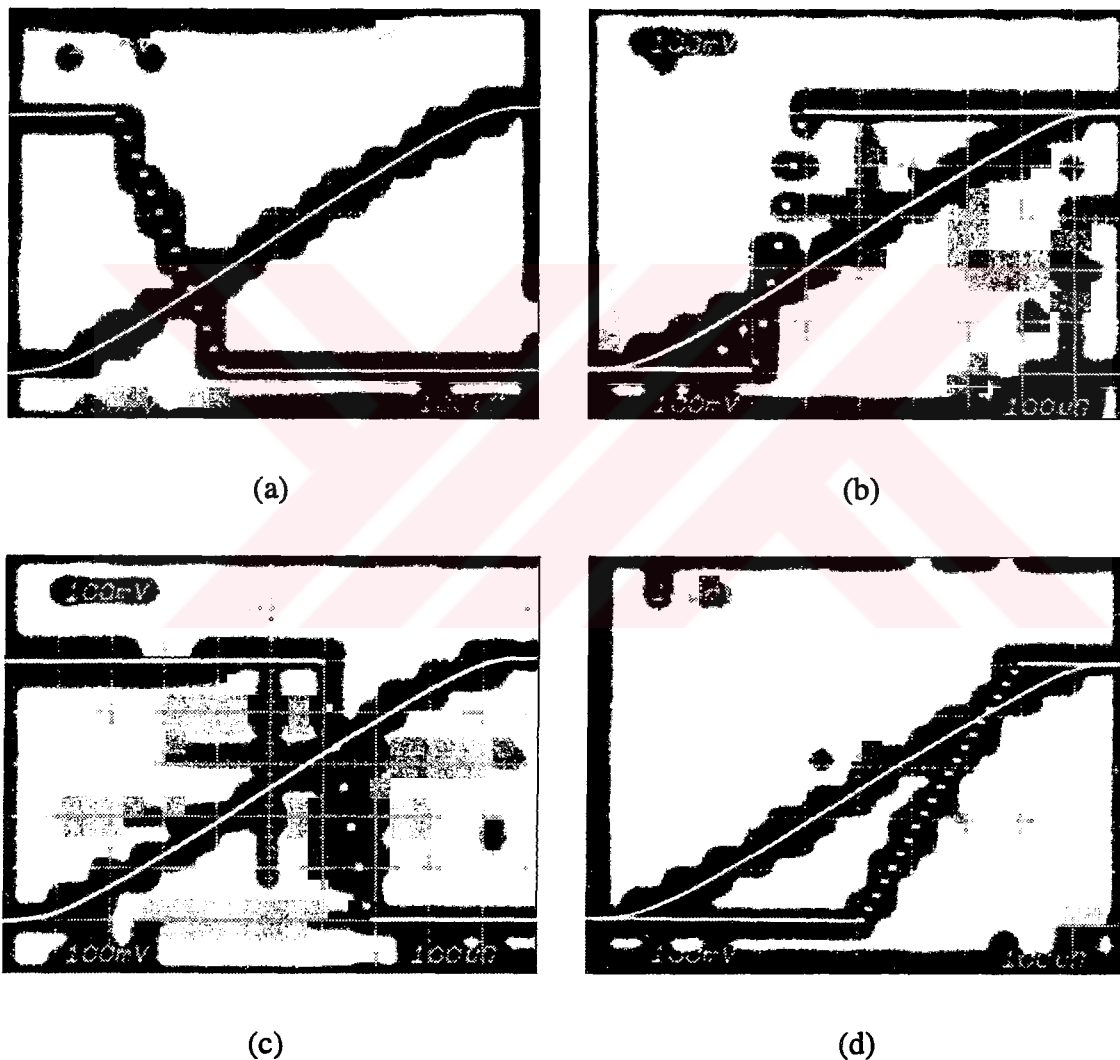


Figure 5.5 Measured transfer characteristics of four ramp generators.

Seven-input minimum selection module measurements are shown in Fig.5.6. The uppermost trace in all three photograph depict the output voltage. Other traces are of the three input voltages. Remaining four inputs are hold at 5V and not shown

in the photographs. In Fig.5.6(a) three inputs were set initially to 0V, 0.4V and 0.8V, and sequentially switched to 5V beginning with the smallest, so each can be the minimum in a sequence. Initially, input voltages were set to 2.1V, 2.5V and 2.9V for the case of Fig.5.6(b) and 3.8V, 4.2V and 4.6V that of Fig.5.6(c). As can be clearly observed from the photographs, minimum selection ability of the inference module in complete rail-to-rail range is verified.

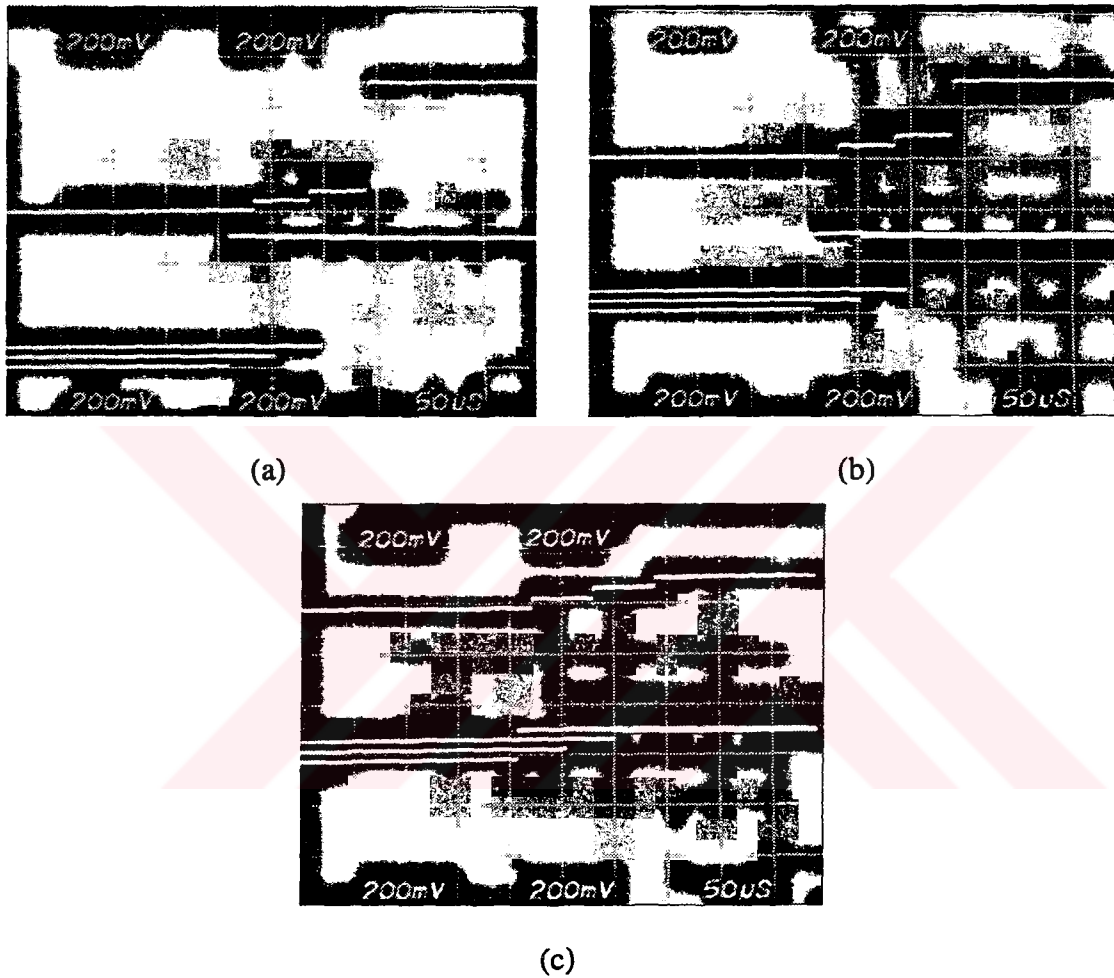


Figure 5.6 Measurements on seven-input minimum selection test circuit.

In Fig.5.7 a stand-alone divider response is depicted. The dividend is kept constant at 0.45V while the divisor is ramped from 0V to 5V. The output follows the expected hyperbolic characteristics of a divider. As especially observed in the small values of the quotient, nonsaturated comparator outputs cause the divider output voltages to take values in between two neighboring quanta as explained in Section 4.4.3. Due to a mistake in the calculation of capacitance ratios, however, all threshold voltages in the entire comparator stack were realized with an additional 125mV offset error, as a result of which, not only the maximum quantization error

became -250mV instead of $\pm 125\text{mV}$, but also the maximum output voltage was limited to 4.75V , because the comparator of the highest index could not be activated at all.

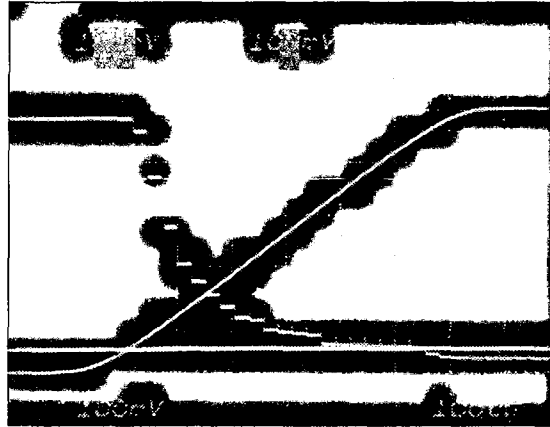


Figure 5.7 Divider response for a ramp input.

An exhaustive functional test was performed at room temperature by scanning the entire two-dimensional input space with 250mV increments at a rate of 85k sample per second while the other inputs were kept at constant values. Difference between the measured and targeted values of the output voltage remained between -150mV ~ 500mV for the entire input space. The calculation and measurement results can be found in App.E. The experimentally obtained control-surface graph is shown in Fig.5.8(a). I_D and I_S are the scanned inputs, I_C and I_V are hold at 1V and 1.25V , respectively, and O_{SP} is the output variable, all measured in volts. Targeted control surface is depicted in Fig.5.8(b) and difference between the two surfaces ΔO_{SP} , which we call “error surface” is shown in Fig.5.8(c). Two prominent systematic errors can be clearly observed in this graph. First one appears as a plateau in the error surface for the large values of both I_D and I_S , which stems from the quantization in the divider. In this region of the error surface, only the quantization error is dominant by the reason that the ramp generators cannot contribute an error, since all of them are in their deep-saturation modes of operation. Second, some peaks can be seen in the rest of the surface due to the output voltage deviations of the ramp generators. As mentioned before, in the regions where the amplifiers are biased at the near vicinity of ground-rail vertex, an additional error occurs originating from the degradation in the open-loop gain. As can be observed from the data given in App.E, a maximum error of 502mV (10% of the full scale)

occurs for the case of $I_C=1V$, $I_V=1.25V$, $I_D=1.25V$ and $I_S=3.5V$. Accumulated error can be calculated approximately by considering the nonideality analysis results given in Sections 4.2.5, 4.3.1 and 4.4.3, but, an accurate error model cannot be developed for the proposed fuzzy controller architecture due to the number of the subcircuits contained and the complexity of the interconnections involved. For given input values above the approximate error calculation for the integrated controller yields $\Delta O_{SP}=536mV$ which is consistent with the measured value of 502mV.

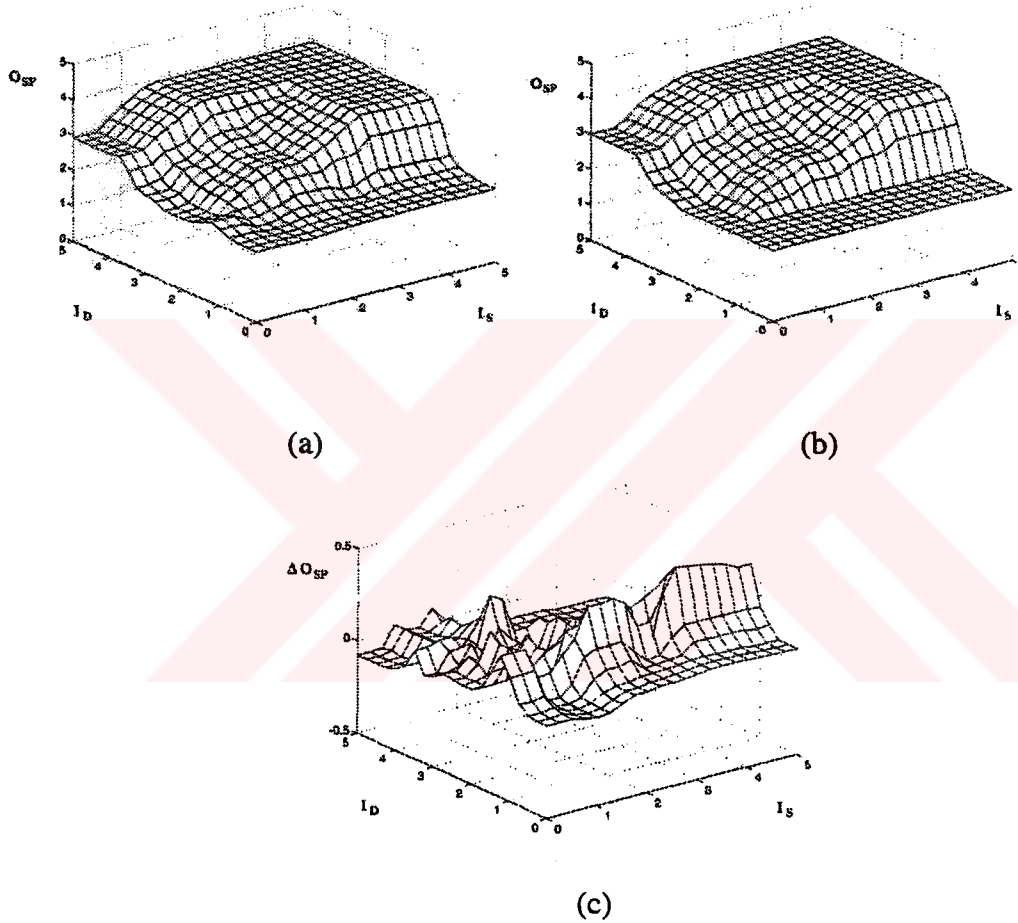


Figure 5.8 Partial control surface of the integrated controller. (a) Measured control surface, (b) targeted control surface, and (c) error surface defined as different between these two.

High temperature performance of the controller was tested by reextracting the control-surface at 70°C. The maximum absolute deviation in the output voltage with respect to room temperature operation was observed to be less than 35mV over the entire control-surface. The measurement data are given in Table 5.12.

Table 5.12 Temperature dependency measurement results.

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] T=23.5 °C	O_{SP} [V] T=70 °C
1.000	1.250	0.000	0.000	2.025	2.030
1.000	1.250	0.000	5.000	2.099	2.100
1.000	1.250	0.250	0.000	2.026	2.032
1.000	1.250	0.250	5.000	2.100	2.099
1.000	1.250	0.500	0.000	2.026	2.031
1.000	1.250	0.500	5.000	2.104	2.100
1.000	1.250	0.750	0.000	2.061	2.064
1.000	1.250	0.750	5.000	2.157	2.148
1.000	1.250	1.000	0.000	2.198	2.183
1.000	1.250	1.000	5.000	2.236	2.236
1.000	1.250	1.250	0.000	2.294	2.290
1.000	1.250	1.250	5.000	2.416	2.421
1.000	1.250	1.500	0.000	2.195	2.192
1.000	1.250	1.500	5.000	3.259	3.265
1.000	1.250	1.750	0.000	2.071	2.072
1.000	1.250	1.750	5.000	3.760	3.760
1.000	1.250	2.000	0.000	2.036	2.041
1.000	1.250	2.000	5.000	3.930	3.900
1.000	1.250	2.250	0.000	2.034	2.041
1.000	1.250	2.250	5.000	3.930	3.910
1.000	1.250	2.500	0.000	2.040	2.038
1.000	1.250	2.500	5.000	3.930	3.900
1.000	1.250	2.750	0.000	2.161	2.144
1.000	1.250	2.750	5.000	3.920	3.900
1.000	1.250	3.000	0.000	2.222	2.220
1.000	1.250	3.000	5.000	3.910	3.890
1.000	1.250	3.250	0.000	2.286	2.300
1.000	1.250	3.250	5.000	3.920	3.890
1.000	1.250	3.500	0.000	2.646	2.612
1.000	1.250	3.500	5.000	3.940	3.910
1.000	1.250	3.750	0.000	3.015	3.010
1.000	1.250	3.750	5.000	3.980	3.960
1.000	1.250	4.000	0.000	2.982	2.981
1.000	1.250	4.000	5.000	3.950	3.940
1.000	1.250	4.250	0.000	2.963	2.953
1.000	1.250	4.250	5.000	3.940	3.930
1.000	1.250	4.500	0.000	2.955	2.950
1.000	1.250	4.500	5.000	3.940	3.930
1.000	1.250	4.750	0.000	2.958	2.943
1.000	1.250	4.750	5.000	3.940	3.930
1.000	1.250	5.000	0.000	2.956	2.953
1.000	1.250	5.000	5.000	3.940	3.930

6. CONCLUSIONS

In this work, a novel approach based on sampled-analog circuit techniques has been proposed for the implementation of application-specific fuzzy controllers. A set of seven subcircuits comprising a sample-and-hold amplifier, positive and negative ramp amplifiers, an inference cell, adder and weighted-adder amplifiers, and a divider unit has been explored. These subcircuits form a complete library. By using the proposed library, any fuzzy controller expert system with piecewise linear input membership functions, conjunctive rules, and singleton output classes can be implemented on silicon.

All the proposed circuits have been designed to function from one rail to the other excluding any compression and/or expansion loss and/or distortion. Rail-to-rail functionality was verified by measurements on either stand-alone subcircuits or completely integrated fuzzy controller. As also verified by testing, all cells exhibit very good linearity over the entire rail-to-rail range. This leads to an accurate representation of the expert system. Furthermore, the chip operates with a single 5V supply, accepts fully analog voltage inputs, and generates quantized analog voltage outputs. These interfaces operate over the same rail-to-rail range as internal nodes. Since the inputs and outputs are analog voltages and data are processed in analog voltage mode along the entire controller, no type of conversion is necessary as well. This protects the implementation style from additional error sources such as A/D and/or D/A or I/V and/or V/I conversions. Natural compatibility with the analog voltage-mode sensors and actuators is also an advantage of this implementation method. Voltage mode processing of the data in the controller provides the subblocks in it with large fan-out within reasonable limits, which is not the case in current mode implementations.

Sampled-analog data are processed in parallel in the controller. In a system containing sampled-analog circuits, existence of a digital data path controller is a

must. Such a controller consists of appropriately designed phase generator circuits and manages the data flow from input to output. The area occupied by data path controller can be considered as a loss of silicon for analog hardware implementations, however, its size is about 0.15mm^2 for $1.2\text{-}\mu\text{m}$ double-poly double-metal CMOS technology.

Independent of the fabrication technology, the proposed circuits in this study can be implemented with ordinary CMOS processes including double-poly for the capacitors. In most of continuous voltage and current mode realizations presented in Chapter 3, device dimensions should be determined carefully for specific processes, and besides, some biasing currents and voltages should be supplied externally for reliable operation. In contrast, the proposed style does not demand any size adjustment and/or topology variation in the frames of the circuits (because they are self-biased circuits), however, compensation devices and capacitors might be resized for different technologies. Furthermore, since the functionalities of ramp generators, sample-and-hold units and adder circuits are provided by a high gain amplifier constructed by cascaded three inverter stages in which the virtual-ground level of the amplifier is determined by its logic threshold, typical process-dependent variations in device parameters and dimensions are not influential on the operations of these structures.

The programmability can be adapted to the proposed architecture via additional RAM, switching matrices and capacitors, since characteristics of the input and output membership functions are defined by the capacitor ratios and a standard inference cell can easily be created to execute each rule. It is also worth noting that the offset in the inputs of the ramp generators can be soft programmed by tying C_2 to a programming voltage instead of V_{DD} .

Since capacitor ratios determine the transfer characteristics of the ramp generator circuits, parasitics and process originated deviations cannot be much effective on the transfer functions as can be inferred from the given nonideality analysis.

The sensitivity of fuzzy controller operation with respect to temperature is very weak as verified by testing. Almost zero temperature dependency of the

response of entire controller can be seen with the maximum measured value of 35mV within full range.

It is not possible to derive an accurate error model due to the complexity of the controller architecture, but a maximum 10% full scale error was measured during testing which mostly originated from quantization. Still, it is inside the acceptable typical fuzzy controller error limit of 20% reported in the literature.

The measured speed of the proposed controller is 85kFLIPS. It seems to be adequate for the industrial applications since recovering times of almost all physical systems under fuzzy controlling are much longer.

The chip size of a fully integrated controller including the data path controller (but excluding the pads) can be estimated in mm^2 for a typical 1.2- μm double-poly double-metal CMOS technology from

$$\text{Size} \sim 1.7(0.15 + 0.11X + 0.03Y + 0.01Z)$$

where X is the number of outputs, Y is the number of input classes, and Z is the number of all antecedent terms in the rule base. The fuzzy controller prototype built with these units for $X=2$, $Y=11$, and $Z=64$ measures approximately 2mm^2 . The comparison with the programmable implementations presented in Chapter 3 cannot yield realistic results, because the programming facility can be achieved only at the expense of a quite large silicon area, but, let us examine the case for two programmable fuzzy controller chips which are characterized with $(X=2, Y=64, Z=51)$ [24, 25] and $(X=4, Y=56, Z=256)$ [85]. If they had been implemented with the circuits given in this work, the corresponding chip size would have been 4.5mm^2 and 8mm^2 , respectively. The fact that each of these two chips actually measures about 70mm^2 clearly shows the magnitude of compaction achievable with the ASIC approach. Moreover, it can be seen by applying the above area estimation formula to most of application specific controller implementations presented in the same chapter, that they would occupy smaller or similar areas were they implemented by the modules proposed in this manuscript.

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APPENDIX

A. HSPICE Input and Output Files AC Analysis of Noninverting Amplifier in Reset Phase

noninverting amplifier ph1

* reading file: /soft/hspice/96/hspice.ini

```
.model nmos nmos level=2 uo=515 vto=.736 nfs=.452e12 tox=23.8e-9
+ nsub=3.33e16 ucrit=28.7e4 uexp=0.251 vmax=77.3e3 rsh=25.5 xj=175e-9
+ ld=-50e-9 delta=0 pb=.96 js=10e-6 neff=5.25 cj=360e-6
+ mj=430e-3 cjsw=2.5e-10 mjsw=.190 cgso=290e-12 cgdo=290e-12 cgbo=170e-12
+ kf=0.101e-25 af=1.33 wd=0.398e-6
```

```
.model pmos pmos level=2 uo=175 vto=-.751 nfs=1.3e12 tox=23.8e-9
+ nsub=1.8e16 ucrit=21.6e4 uexp=0.268 vmax=54e3 rsh=46 xj=56e-9
+ ld=43e-9 delta=0.798 pb=.97 js=20e-6 neff=3.09 cj=340e-6
+ mj=0.530 cjsw=2.2e-10 mjsw=.2 cgso=290e-12 cgdo=290e-12 cgbo=170e-12
+ kf=0.390e-27 af=1.29 wd=0.448e-6
```

```
m0 vo vp1 4 0 nmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m1 1 vin 7 0 nmos w=2u l=2.5u ad=9p as=9p pd=12.5u ps=12.5u
m2 100 vgg1 6 0 nmos w=2u l=2.5u ad=9p as=9p pd=12.5u ps=12.5u
m3 3 1 0 0 nmos w=4u l=2.5u ad=18p as=18p pd=16.5u ps=16.5u
m4 4 3 0 0 nmos w=12u l=2.5u ad=50p as=50p pd=32.5u ps=32.5u
m5 1 vin 6 100 pmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m6 7 vgg2 0 100 pmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m7 3 1 100 100 pmos w=4u l=1.2u ad=18p as=18p pd=16.5u ps=16.5u
m8 4 3 100 100 pmos w=12u l=1.2u ad=50p as=50p pd=32.5u ps=32.5u
m9 vgg2 vp1 10 0 nmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m10 vgg2 vp1 9 0 nmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m11 vi vp1 8 0 nmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m12 vi vp1c 8 100 pmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m13 8 vp2 vgg2 0 nmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m14 9 vp2c vgg1 100 pmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m15 10 vp2c 4 100 pmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m16 10 vp2 4 0 nmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m17 4 vp2 5 0 nmos w=2u l=3u ad=9p as=9p pd=12.5u ps=12.5u
m18 4 vp2c 5 100 pmos w=2u l=3u ad=9p as=9p pd=12.5u ps=12.5u
mf 1 vp1c 2 100 pmos w=2u l=2u ad=9p as=9p pd=12.5u ps=12.5u
```

```
c0 vo 10 100f
c1 vo 8 250f
c2 vo 9 150f
cp vo 0 10f
cl 5 0 1p
cf1 2 3 150f
cf2 1 3 20f
```

```

vdd 100 0 5
vgg1 vgg1 0 5
vgg2 vgg2 0 0
vp1 vp1 0 5
vp1c vp1c 0 0
vp2 vp2 0 0
vp2c vp2c 0 5
vi vi 0 5

```

```

vin vin 0 dc 2.471811 ac 1u
.ac dec 500 1 100meg
.pz v(vo) vin
.op
.options post delmax=2.5n
.end

```

```

***** H S P I C E --      96.3.1 (961009) 10:10:08  98/10/03      sun4
*****

```

```

noninverting amplifier ph1

```

```

***** operating point information      tnom= 25.000 temp= 25.000
*****

```

```

***** operating point status is all      simulation time is      0.

```

node	=voltage	node	=voltage	node	=voltage
+0:1	= 2.4287	0:2	= 2.4287	0:3	= 2.4457
+0:4	= 2.4752	0:5	= 2.4876	0:6	= 3.5198
+0:7	= 1.3686	0:8	= 5.0000	0:9	= 43.8984n
+0:10	= 40.0844n	0:100	= 5.0000	0:vgg1	= 5.0000
+0:vgg2	= 0.	0:vi	= 5.0000	0:vin	= 2.4718
+0:vo	= 2.4752	0:vp1	= 5.0000	0:vp1c	= 0.
+0:vp2	= 0.	0:vp2c	= 5.0000		

```

**** voltage sources

```

```

subckt

```

element	0:vdd	0:vgg1	0:vgg2	0:vp1	0:vp1c	0:vp2
volts	5.0000	5.0000	0.	5.0000	0.	0.
current	-484.4002u	-5.9226p	25.9281p	0.	0.	0.
power	2.4220m	29.6132p	0.	0.	0.	0.

```

subckt

```

element	0:vp2c	0:vi	0:vin
volts	5.0000	5.0000	2.4718
current	0.	-20.0315p	0.
power	0.	100.1574p	0.

```

total voltage source power dissipation=      2.4220m      watts

```

```

**** mosfets

```

```

subckt

```

element	0:m0	0:m1	0:m2	0:m3	0:m4	0:m5
model	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:pmos
id	-2.4757p	17.8873n	17.8836n	106.0625u	378.3197u	-17.8820n
ibs	-2.228e-16	-1.232e-16	-3.168e-16	0.	0.	2.664e-16
ibd	-2.228e-16	-2.186e-16	-4.500e-16	-4.402e-16	-1.2376f	4.628e-16
vgs	2.5248	1.1032	1.4802	2.4287	2.4457	-1.0479
vds	-26.7766n	1.0600	1.4802	2.4457	2.4752	-1.0911
vbs	-2.4752	-1.3686	-3.5198	0.	0.	1.4802
vth	1.1888	1.0793	1.4566	694.2306m	694.1431m	-1.0544
vdsat	838.5836m	35.7452m	36.3735m	1.1136	1.1229	-55.9099m
beta	69.2035u	35.7239u	35.9562u	95.5287u	334.1518u	28.2963u

gam eff	602.9620m	668.2828m	653.6843m	676.7301m	676.6298m	449.8748m
gm	1.3117p	409.3037n	426.6427n	120.2395u	424.4837u	270.6617n
gds	92.4571u	6.4041n	6.1914n	1.9884u	7.0291u	6.2252n
gmb	198.5460f	88.0416n	62.8973n	33.6519u	118.5402u	47.5478n
cdtot	6.0409f	4.9292f	4.2755f	8.2016f	20.4004f	4.2450f
cgtot	3.6576f	5.0480f	4.9490f	10.8996f	35.8586f	2.5273f
cstot	6.0409f	8.4622f	7.6107f	19.8228f	57.7820f	5.6361f
cbtot	8.8774f	10.0507f	8.4414f	18.0896f	43.4880f	8.2868f
cgs	1.7155f	3.6079f	3.6079f	9.2178f	31.6570f	1.4788f
cgd	1.7155f	5.864e-16	5.890e-16	1.1994f	3.6195f	5.820e-16

subckt						
element	0:m6	0:m7	0:m8	0:m9	0:m10	0:m11
model	0:pmos	0:pmos	0:pmos	0:nmos	0:nmos	0:nmos
id	17.8893n	-106.0625u	-378.3198u	-9.9745p	-10.9235p	0.
ibs	9.000e-16	0.	0.	-3.608e-24	-3.951e-24	-4.500e-16
ibd	6.536e-16	9.195e-16	2.5248f	0.	0.	-4.500e-16
vgs	0.	-2.5713	-2.5543	5.0000	5.0000	183.1083n
vds	1.3686	-2.5543	-2.5248	-40.0844n	-43.8984n	183.1083n
vbs	5.0000	0.	0.	-40.0844n	-43.8984n	-5.0000
vth	-1.3766	-700.8034m	-693.3422m	674.6502m	674.6502m	1.4850
vdsat	-57.1751m	-1.2219	-1.2247	1.6226	1.6226	36.3071m
beta	28.8505u	77.8248u	278.2047u	57.5298u	57.5298u	69.2035u
gam eff	432.7232m	461.6481m	461.7701m	654.2694m	654.2694m	575.3137m
gm	275.7515n	90.8676u	325.5546u	1.1180p	1.2244p	8.965e-28
gds	5.8640n	7.5041u	27.0300u	248.8365u	248.8365u	2.009e-22
gmb	36.3296n	16.5741u	55.6233u	599.3093f	656.3328f	0.
cdtot	4.7868f	7.0704f	17.6919f	8.0805f	8.0805f	4.2689f
cgtot	2.4094f	5.8838f	19.2202f	3.6550f	3.6550f	1.7288f
cstot	3.6624f	14.2547f	39.5950f	8.0805f	8.0805f	4.2699f
cbtot	6.8304f	15.8453f	38.5363f	12.9541f	12.9541f	7.9362f
cgs	5.823e-16	4.5047f	15.4450f	1.7155f	1.7155f	5.834e-16
cgd	1.4317f	1.1771f	3.5404f	1.7155f	1.7155f	5.824e-16

subckt						
element	0:m12	0:m13	0:m14	0:m15	0:m16	0:m17
model	0:pmos	0:nmos	0:pmos	0:pmos	0:nmos	0:nmos
id	15.0310p	30.1286f	-922.6306f	0.	-23.2152f	0.
ibs	3.296e-23	0.	0.	4.545e-16	-2.228e-16	-2.239e-16
ibd	0.	-4.500e-16	9.000e-16	9.000e-16	-3.608e-24	-2.228e-16
vgs	-5.0000	0.	0.	2.5248	-2.4752	-2.4876
vds	183.1083n	5.0000	-5.0000	-2.4752	-2.4752	-12.4667m
vbs	183.1083n	0.	0.	2.5248	-2.4752	-2.4876
vth	-734.1667m	640.2349m	-712.8898m	-1.2161	652.2863m	1.3158
vdsat	-2.2992	34.5841m	-53.4455m	-56.7171m	34.4964m	36.1459m
beta	19.2432u	80.7709u	34.6557u	30.8022u	76.8223u	29.0208u
gam eff	478.4512m	614.7915m	453.5205m	436.8394m	628.6157m	673.5805m
gm	1.4734p	651.4432f	13.3626p	0.	500.3158f	0.
gds	82.0882u	8.7317f	137.8253f	0.	10.0303f	0.
gmb	601.5614f	147.2715f	3.0054p	0.	113.6650f	0.
cdtot	7.2822f	4.2670f	3.6603f	3.6601f	6.9900f	4.9089f
cgtot	3.1358f	2.3548f	2.0730f	2.1360f	2.3538f	3.9048f
cstot	7.2822f	6.9909f	6.4225f	4.2658f	4.9056f	4.9033f
cbtot	11.8114f	11.2001f	9.7702f	7.7291f	11.8389f	11.3850f
cgs	1.4722f	6.259e-16	6.125e-16	5.863e-16	5.802e-16	5.825e-16
cgd	1.4722f	5.805e-16	5.803e-16	5.800e-16	6.250e-16	5.835e-16

subckt		
element	0:m18	0:mf
model	0:pmos	0:pmos
id	0.	-2.5718p

```

ibs      4.522e-16  4.628e-16
ibd      4.545e-16  4.628e-16
vgs      2.5124     -2.4287
vds      -12.4667m -156.2433n
vbs      2.5124     2.5713
vth      -1.3265    -1.3047
vdsat    -56.6932m -886.4634m
beta     9.6196u    14.6455u
gam eff  499.2693m  481.5128m
gm        0.        1.9724p
gds      0.        16.4603u
gmb      0.        323.0258f
cdtot    4.2616f    5.7759f
cgtot    3.7001f    4.5581f
cstot    4.2669f    5.7759f
cbtot    9.8983f    7.6582f
cgs      5.830e-16  2.1129f
cgd      5.821e-16  2.1129f

```

```

***** H S P I C E  --      96.3.1 (961009) 10:10:08  98/10/03      sun4
*****

```

```

noninverting amplifier ph1

```

```

***** pole/zero analysis          tnom= 25.000 temp= 25.000
*****

```

```

input = 0:vin          output = v(vo)

```

```

node=vp2      real= -2.2091E-18 imaginary= -1.3096E-25

```

```

**warning** underflow 1 time(s) in pole/zero analysis

```

```

poles (rad/sec)          poles ( hertz)

```

```

*****

```

real	imag	real	imag
0.	0.	0.	0.
-1.5442k	0.	-245.7603	0.
-40.9745x	0.	-6.5213x	0.
-61.9143x	0.	-9.8540x	0.
-62.0192x	0.	-9.8707x	0.
-511.2381x	0.	-81.3661x	0.
-627.2301x	-386.8008x	-99.8268x	-61.5613x
-627.2301x	386.8008x	-99.8268x	61.5613x
-1.8453g	0.	-293.6882x	0.
-3.3803g	0.	-537.9963x	0.
-11.2690g	0.	-1.7935g	0.

```

node=vi      real= -3.0928E-19 imaginary= 0.

```

```

**warning** underflow 1 time(s) in pole/zero analysis

```

```

zeros (rad/sec)          zeros ( hertz)

```

```

*****

```

real	imag	real	imag
0.	0.	0.	0.
-41.3604x	0.	-6.5827x	0.
-61.9549x	0.	-9.8604x	0.
-114.1331x	0.	-18.1648x	0.
-308.8121x	0.	-49.1490x	0.
412.9448x	0.	65.7222x	0.
-1.5385g	0.	-244.8582x	0.
-2.0958g	0.	-333.5583x	0.
8.7345g	0.	1.3901g	0.
104.7553g	0.	16.6723g	0.

B. HSPICE Input and Output Files

AC Analysis of Noninverting Amplifier in Evaluation Phase

noninverting amplifier ph2

* reading file: /soft/hspice/96/hspice.ini

```
.model nmos nmos level=2 uo=515 vto=.736 nfs=.452e12 tox=23.8e-9
+ nsub=3.33e16 ucrit=28.7e4 uexp=0.251 vmax=77.3e3 rsh=25.5 xj=175e-9
+ ld=-50e-9 delta=0 pb=.96 js=10e-6 neff=5.25 cj=360e-6
+ mj=430e-3 cjsw=2.5e-10 mjsw=.190 cgso=290e-12 cgdo=290e-12 cgbo=170e-12
+ kf=0.101e-25 af=1.33 wd=0.398e-6
```

```
.model pmos pmos level=2 uo=175 vto=-.751 nfs=1.3e12 tox=23.8e-9
+ nsub=1.8e16 ucrit=21.6e4 uexp=0.268 vmax=54e3 rsh=46 xj=56e-9
+ ld=43e-9 delta=0.798 pb=.97 js=20e-6 neff=3.09 cj=340e-6
+ mj=0.530 cjsw=2.2e-10 mjsw=.2 cgso=290e-12 cgdo=290e-12 cgbo=170e-12
+ kf=0.390e-27 af=1.29 wd=0.448e-6
```

```
m0 vo vp1 4 0 nmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m1 1 vin 7 0 nmos w=2u l=2.5u ad=9p as=9p pd=12.5u ps=12.5u
m2 100 vgg1 6 0 nmos w=2u l=2.5u ad=9p as=9p pd=12.5u ps=12.5u
m3 3 1 0 0 nmos w=4u l=2.5u ad=18p as=18p pd=16.5u ps=16.5u
m4 4 3 0 0 nmos w=12u l=2.5u ad=50p as=50p pd=32.5u ps=32.5u
m5 1 vin 6 100 pmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m6 7 vgg2 0 100 pmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m7 3 1 100 100 pmos w=4u l=1.2u ad=18p as=18p pd=16.5u ps=16.5u
m8 4 3 100 100 pmos w=12u l=1.2u ad=50p as=50p pd=32.5u ps=32.5u
m9 vgg2 vp1 10 0 nmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m10 vgg2 vp1 9 0 nmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m11 vi vp1 8 0 nmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m12 vi vp1c 8 100 pmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m13 8 vp2 vgg2 0 nmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m14 9 vp2c vgg1 100 pmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m15 10 vp2c 4 100 pmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m16 10 vp2 4 0 nmos w=2u l=1.2u ad=9p as=9p pd=12.5u ps=12.5u
m17 4 vp2 5 0 nmos w=2u l=3u ad=9p as=9p pd=12.5u ps=12.5u
m18 4 vp2c 5 100 pmos w=2u l=3u ad=9p as=9p pd=12.5u ps=12.5u
mf 1 vp1c 2 100 pmos w=2u l=2u ad=9p as=9p pd=12.5u ps=12.5u
```

```
c0 vo 10 100f
c1 vo 8 250f
c2 vo 9 150f
cp vo 0 10f
cl 5 0 1p
cf1 2 3 150f
cf2 1 3 20f
```

```

vdd 100 0 5
vgg1 vgg1 0 5
vgg2 vgg2 0 0
vp1 vp1 0 0
vp1c vp1c 0 5
vp2 vp2 0 5
vp2c vp2c 0 0
vi vi 0 5
*v vo vin 0
vin vin 0 dc 2.471811 ac 1u

```

```

.ac dec 500 1 100meg
.pz v(vo) vin
.op
.options post delmax=2.5n
.end

```

```

***** H S P I C E --      96.3.1 (961009) 10:18:11  98/10/03      sun4
*****

```

noninverting amplifier ph2

```

***** operating point information          tnom= 25.000 temp= 25.000
*****

```

```

***** operating point status is all      simulation time is      0.

```

node	=voltage	node	=voltage	node	=voltage
+0:1	= 2.4282	0:2	= 3.7142	0:3	= 2.4562
+0:4	= 2.2418	0:5	= 2.2418	0:6	= 3.5198
+0:7	= 1.3686	0:8	= 64.1130n	0:9	= 5.0000
+0:10	= 2.2418	0:100	= 5.0000	0:vgg1	= 5.0000
+0:vgg2	= 0.	0:vi	= 5.0000	0:vin	= 2.4718
+0:vo	= 1.1208	0:vp1	= 0.	0:vp1c	= 5.0000
+0:vp2	= 5.0000	0:vp2c	= 0.		

**** voltage sources

subckt

element	0:vdd	0:vgg1	0:vgg2	0:vp1	0:vp1c	0:vp2
volts	5.0000	5.0000	0.	0.	5.0000	5.0000
current	-487.0460u	-10.0306p	23.2480p	0.	0.	0.
power	2.4352m	50.1529p	0.	0.	0.	0.

subckt

element	0:vp2c	0:vi	0:vin
volts	0.	5.0000	2.4718
current	0.	-15.9532p	0.
power	0.	79.7660p	0.

total voltage source power dissipation= 2.4352m watts

**** mosfets

subckt

element	0:m0	0:m1	0:m2	0:m3	0:m4	0:m5
model	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:pmos
id	0.	17.8869n	17.8845n	106.0269u	381.0011u	-17.8828n
ibs	-2.018e-16	-1.232e-16	-3.168e-16	0.	0.	2.664e-16
ibd	-1.009e-16	-2.185e-16	-4.500e-16	-4.421e-16	-1.1209f	4.629e-16
vgs	-2.2418	1.1032	1.4802	2.4282	2.4562	-1.0479

vds	-1.1209	1.0596	1.4802	2.4562	2.2418	-1.0916
vbs	-2.2418	-1.3686	-3.5198	0.	0.	1.4802
vth	948.5043m	1.0793	1.4566	694.1994m	694.8526m	-1.0544
vdsat	35.3779m	35.7452m	36.3735m	1.1134	1.1279	-55.9099m
beta	73.9979u	35.7236u	35.9562u	95.5439u	332.9254u	28.2973u
gam eff	615.5816m	668.2844m	653.6843m	676.6943m	677.4436m	449.8728m
gm	1.318e-27	409.2939n	426.6631n	120.2347u	424.7106u	270.6746n
gds	0.	6.4046n	6.1917n	1.9809u	7.6965u	6.2247n
gmb	1.431e-28	88.0395n	62.9004n	33.6512u	118.5530u	47.5501n
cdtot	5.6155f	4.9294f	4.2755f	8.1949f	20.7927f	4.2448f
cgtot	2.3230f	5.0480f	4.9490f	10.8998f	35.8447f	2.5273f
cstot	4.9960f	8.4622f	7.6107f	19.8228f	57.7820f	5.6361f
cbtot	10.5855f	10.0508f	8.4414f	18.0828f	43.8927f	8.2867f
cgs	5.800e-16	3.6079f	3.6079f	9.2178f	31.6570f	1.4788f
cgd	5.945e-16	5.864e-16	5.890e-16	1.1996f	3.6063f	5.820e-16

subckt

element	0:m6	0:m7	0:m8	0:m9	0:m10	0:m11
model	0:pmos	0:pmos	0:pmos	0:nmos	0:nmos	0:nmos
id	17.8888n	-106.0269u	-381.0012u	-22.5058f	-30.1286f	30.1286f
ibs	9.000e-16	0.	0.	-2.018e-16	-4.500e-16	-5.770e-24
ibd	6.536e-16	9.158e-16	2.7582f	0.	0.	-4.500e-16
vgs	0.	-2.5718	-2.5438	-2.2418	-5.0000	-64.1130n
vds	1.3686	-2.5438	-2.7582	-2.2418	-5.0000	5.0000
vbs	5.0000	0.	0.	-2.2418	-5.0000	-64.1130n
vth	-1.3766	-700.8404m	-692.5351m	653.7051m	640.2349m	640.2349m
vdsat	-57.1751m	-1.2221	-1.2196	34.4845m	34.5841m	34.5841m
beta	28.8505u	77.7640u	282.9710u	76.3930u	80.7709u	80.7709u
gam eff	432.7232m	461.6915m	460.8243m	630.2433m	614.7915m	614.7915m
gm	275.7449n	90.8029u	330.5331u	484.8617f	651.4432f	651.4419f
gds	5.8639n	7.5248u	25.5326u	10.2406f	8.7317f	8.7317f
gmb	36.3287n	16.5621u	56.4846u	110.1400f	147.2715f	147.2712f
cdtot	4.7867f	7.0769f	17.3361f	6.9899f	6.9909f	4.2670f
cgtot	2.4093f	5.8837f	19.2260f	2.3537f	2.3548f	2.3548f
cstot	3.6624f	14.2547f	39.5950f	4.9962f	4.2670f	6.9909f
cbtot	6.8304f	15.8518f	38.1751f	11.9295f	11.2001f	11.2001f
cgs	5.823e-16	4.5047f	15.4450f	5.802e-16	5.805e-16	6.259e-16
cgd	1.4317f	1.1770f	3.5460f	6.249e-16	6.259e-16	5.805e-16

subckt

element	0:m12	0:m13	0:m14	0:m15	0:m16	0:m17
model	0:pmos	0:nmos	0:pmos	0:pmos	0:nmos	0:nmos
id	922.6306f	15.9537p	-10.0306p	-723.2464f	-3.2664p	-432.4912f
ibs	9.000e-16	0.	0.	4.965e-16	-2.018e-16	-2.018e-16
ibd	0.	-5.770e-24	2.199e-23	4.965e-16	-2.018e-16	-2.018e-16
vgs	5.0000	5.0000	-5.0000	-2.2418	2.7582	2.7582
vds	5.0000	64.1130n	-122.1927n	-29.4327n	-29.4327n	-10.0387n
vbs	5.0000	0.	0.	2.7582	-2.2418	-2.2418
vth	-712.8898m	674.6502m	-734.1667m	-1.2652	1.1546	1.2737
vdsat	-53.4455m	1.6226	-2.2992	-744.0186m	941.4281m	1.0917
beta	34.6557u	57.5298u	19.2432u	25.1628u	69.2035u	29.0208u
gam eff	453.5205m	654.2694m	478.4512m	443.1973m	606.2171m	674.9810m
gm	13.3626p	1.7882p	983.2037f	600.4619f	1.4239p	232.4930f
gds	137.8253f	248.8365u	82.0882u	24.5728u	110.9792u	43.0822u
gmb	3.0054p	958.5646f	401.4369f	84.6590f	233.4281f	44.3410f
cdtot	6.4225f	8.0805f	7.2822f	5.0720f	6.1314f	7.7036f
cgtot	2.0730f	3.6550f	3.1358f	3.1383f	3.6568f	7.1148f
cstot	3.6603f	8.0805f	7.2822f	5.0720f	6.1314f	7.7036f
cbtot	9.7702f	12.9541f	11.8114f	7.3935f	9.0578f	9.3714f
cgs	5.803e-16	1.7155f	1.4722f	1.4722f	1.7155f	3.2877f
cgd	6.125e-16	1.7155f	1.4722f	1.4722f	1.7155f	3.2877f

```

subckt
element 0:m18      0:mf
model    0:pmos    0:pmos
id       -84.3273f -9.395e-24
ibs      4.965e-16 2.314e-16
ibd      4.965e-16 4.629e-16
vgs      -2.2418   1.2858
vds      -10.0387n -1.2860
vbs      2.7582    1.2858
vth      -1.3685   -1.0665
vdsat    -716.7796m -55.7489m
beta     9.6196u   15.7747u
gam eff  498.5263m 485.1678m
gm        89.1692f 1.399e-22
gds       8.4002u  1.879e-24
gmb       15.0032f 2.210e-23
cdtot     6.5137f  4.2429f
cgtot     6.3361f  2.7608f
cstot     6.5137f  4.8765f
cbtot     7.7081f  9.5256f
cgs       2.9138f  5.972e-16
cgd       2.9138f  5.800e-16

```

```

      poles (rad/sec)                poles ( hertz)
*****
      real      imag      real      imag
      0.         0.         0.         0.
      0.         0.         0.         0.
      -11.4036k   0.        -1.8149k   0.
      -18.3678x   0.        -2.9233x   0.
      -61.9185x   0.        -9.8546x   0.
      -62.0203x   0.        -9.8708x   0.
      -332.8398x   0.       -52.9731x   0.
      -603.5185x   0.       -96.0530x   0.
      -1.1671g    0.       -185.7449x   0.
      -3.9789g    0.       -633.2650x   0.
      -8.6531g    0.       -1.3772g    0.
node=vp2      real= -2.1779E-19 imaginary= -3.6232E-27
**warning** underflow 1 time(s) in pole/zero analysis
      zeros (rad/sec)                zeros ( hertz)
*****
      real      imag      real      imag
      0.         0.         0.         0.
      0.         0.         0.         0.
      -41.3609x   0.        -6.5828x   0.
      -50.7607x   0.        -8.0788x   0.
      -61.9561x   0.        -9.8606x   0.
      412.9486x    0.        65.7228x   0.
      -508.1309x   0.       -80.8715x   0.
      -925.9665x   0.      -147.3721x   0.
       9.4312g     0.         1.5010g    0.
      105.5940g    0.        16.8058g    0.

```

C. HSPICE Input File for PSRR Analysis

PSRR

```
.MODEL NMOS NMOS LEVEL=2 UO=515 VTO=.736 NFS=.452E12 TOX=23.8E-9
+ NSUB=3.33E16 UCRIT=28.7E4 UEXP=0.251 VMAX=77.3E3 RSH=25.5 XJ=175E-9
+ LD=-50E-9 DELTA=0 PB=.96 JS=10E-6 NEFF=5.25 CJ=360E-6
+ MJ=430E-3 CJSW=2.5E-10 MJSW=.190 CGSO=290E-12 CGDO=290E-12 CGBO=170E-12
+ KF=0.101E-25 AF=1.33 WD=0.398E-6
```

```
.MODEL PMOS PMOS LEVEL=2 UO=175 VTO=-.751 NFS=1.3E12 TOX=23.8E-9
+ NSUB=1.8E16 UCRIT=21.6E4 UEXP=0.268 VMAX=54E3 RSH=46 XJ=56E-9
+ LD=43E-9 DELTA=0.798 PB=.97 JS=20E-6 NEFF=3.09 CJ=340E-6
+ MJ=0.530 CJSW=2.2E-10 MJSW=.2 CGSO=290E-12 CGDO=290E-12 CGBO=170E-12
+ KF=0.390E-27 AF=1.29 WD=0.448E-6
```

```
M1 1 VIN 7 0 NMOS W=2U L=2.5U AD=9P AS=9P PD=12.5U PS=12.5U
M2 100 VGG1 6 0 NMOS W=2U L=2.5U AD=9P AS=9P PD=12.5U PS=12.5U
M3 3 1 0 0 NMOS W=4U L=2.5U AD=18P AS=18P PD=16.5U PS=16.5U
M4 4 3 0 0 NMOS W=12U L=2.5U AD=50P AS=50P PD=32.5U PS=32.5U
M5 1 VIN 6 100 PMOS W=2U L=1.2U AD=9P AS=9P PD=12.5U PS=12.5U
M6 7 VGG2 0 100 PMOS W=2U L=1.2U AD=9P AS=9P PD=12.5U PS=12.5U
M7 3 1 100 100 PMOS W=4U L=1.2U AD=18P AS=18P PD=16.5U PS=16.5U
M8 4 3 100 100 PMOS W=12U L=1.2U AD=50P AS=50P PD=32.5U PS=32.5U
```

```
VGG1 VGG1 0 5
VGG2 VGG2 0 0
VIN VIN 0 2.471811
vdd 100 0 dc 5 ac 1u
```

```
.AC DEC 500 1 100MEG
.PRINT VP(100) VP(4) VDB(100) VDB(4)
.PZ V(4) Vdd
.OP
.OPTIONS POST DELMAX=2.5N
.END
```

D. Control Surface Scanning Program of the Sample Controller

```
1 REM MIN OF AVERAGE (ARCELIK YENI)
5 CLS: CLEAR
11 REM C: CDS SENSOR; LC, HC
12 REM D: DUST SENSOR; LD, MDL, MDT, HD
13 REM V: VACUUM SENSOR; LV, MVL, MVT, VHV
14 REM S: SURFACE SENSOR; PS, CSL, CST, DCS
15 XC=0: XD=0: XV=0: XS=0: XAV=10: XWAVS=10: XWAVB=10: I=0: Z=0
20 DIM XXC(2500): DIM XXD(2500): DIM XXV(2500): DIM XXS(2500)
30 FOR XV=0 TO 5 STEP .25
31 FOR XD=0 TO 5 STEP .25
32 FOR XC=0 TO 5 STEP .25
33 FOR XS=0 TO 5 STEP .25
75 GOTO 170
80 IF XC=5 AND XD=5 AND XV=5 AND XS=5 THEN 2000
85 I=I+1
90 NEXT XS
110 NEXT XC
130 NEXT XD
140 NEXT XV
150 REM CLASS FUNCTIONS DESCRIPTIONS
170 REM FIRST INPUT: XC
180 IF XC<1 THEN LC=5: GOTO 200
190 IF XC>3 THEN LC=0: GOTO 200
195 LC=7.5-(2.5*XC)
200 IF XC<2.5 THEN HC=0: GOTO 230
210 IF XC>4 THEN HC=5: GOTO 230
220 HC=-8.33+(3.33*XC)
230 REM SECOND INPUT: XD
235 IF XD<.625 THEN LD=5: GOTO 270
240 IF XD>1.875 THEN LD=0: GOTO 270
250 LD=7.5-(4*XD)
270 IF XD<1.25 THEN MDL=0: GOTO 300
280 IF XD>1.875 THEN MDL=5: GOTO 300
290 MDL=-10+(8*XD)
300 IF XD<3.125 THEN MDT=5: GOTO 330
310 IF XD>3.75 THEN MDT=0: GOTO 330
320 MDT=30-(8*XD)
330 IF XD<2.5 THEN HD=0: GOTO 360
340 IF XD>4.375 THEN HD=5: GOTO 360
350 HD=-6.67+(2.67*XD)
360 REM THIRD INPUT: XV
370 IF XV<1.25 THEN LV=5: GOTO 400
380 IF XV>2.5 THEN LV=0: GOTO 400
390 LV=10-(4*XV)
400 IF XV<1.25 THEN MVL=0: GOTO 430
410 IF XV>2.5 THEN MVL=5: GOTO 430
420 MVL=-5+(4*XV)
430 IF XV<3.75 THEN MVT=5: GOTO 470
440 IF XV>4.375 THEN MVT=0: GOTO 470
450 MVT=35-(8*XV)
470 IF XV<3.125 THEN VHV=0: GOTO 500
480 IF XV>4.375 THEN VHV=5: GOTO 500
490 VHV=-12.5+(4*XV)
```

```

495 REM FOURTH INPUT: XS
500 IF XS<.625 THEN PS=5:GOTO 530
510 IF XS>1.875 THEN PS=0:GOTO 530
520 PS=7.5-(4*XS)
530 IF XS<.625 THEN CSL=0:GOTO 551
540 IF XS>1.25 THEN CSL=5:GOTO 551
550 CSL=-5+(8*XS)
551 IF XS<2.5 THEN CST=5:GOTO 555
552 IF XS>3.75 THEN CST=0:GOTO 555
553 CST=15-(4*XS)
555 IF XS<2.5 THEN DCS=0:GOTO 560
556 IF XS>3.75 THEN DCS=5:GOTO 560
557 DCS=-10+(4*XS)
560 REM END OF CLASS FUNCTIONS DESCRIPTIONS
570 REM RULE DESCRIPTIONS
575 REM RULE 1
580 IF LD>LC THEN R1=LC:GOTO 586
585 R1=LD
586 IF R1<PS THEN 588
587 R1=PS
588 REM RULE 2
589 IF MDL>MDT THEN R2=MDT:GOTO 591
590 R2=MDL
591 IF R2<LC THEN 593
592 R2=LC
593 IF R2<PS THEN 596
594 R2=PS
596 REM RULE 3
600 IF HD>LC THEN R3=LC:GOTO 605
603 R3=HD
605 IF R3<PS THEN 615
610 R3=PS
615 REM RULE 4
620 IF LD<LC THEN R4=LD:GOTO 627
624 R4=LC
627 IF R4<CSL THEN 640
630 R4=CSL
640 IF R4<CST THEN 660
650 R4=CST
655 REM RULE 5
660 IF MVL<MVT THEN R5=MVL:GOTO 671
670 R5=MVT
671 IF R5<MDL THEN 673
672 R5=MDL
673 IF R5<MDT THEN 675
674 R5=MDT
675 IF R5<LC THEN 680
676 R5=LC
680 IF R5<CSL THEN 700
690 R5=CSL
700 IF R5<CST THEN 711
705 R5=CST
710 REM RULE 6
711 IF HD<LC THEN R6=HD:GOTO 713
712 R6=LC
713 IF R6<CSL THEN 715
714 R6=CSL
715 IF R6<CST THEN 717
716 R6=CST
717 REM RULE 7
718 IF MVL<MVT THEN R7=MVL:GOTO 720
719 R7=MVT
720 IF R7<LD THEN 735
730 R7=LD
735 IF R7<LC THEN 740
736 R7=LC
740 IF R7<DCS THEN 755

```

```

750 R7=DCS
755 REM RULE 8
760 IF MDL<MDT THEN R8=MDL:GOTO 775
770 R8=MDT
775 IF R8<LC THEN 780
776 R8=LC
780 IF R8<DCS THEN 791
785 R8=DCS
790 REM RULE 9
791 IF HD<LC THEN R9=HD:GOTO 793
792 R9=LC
793 IF R9<DCS THEN 796
795 R9=DCS
796 REM RULE 10
797 IF HC<PS THEN R10=HC:GOTO 800
798 R10=PS
799 REM RULE 11
800 IF HC<CSL THEN R11=HC:GOTO 820
810 R11=CSL
820 IF R11<CST THEN 840
830 R11=CST
835 REM RULE 12
840 IF HC<DCS THEN R12=HC:GOTO 860
850 R12=DCS
855 REM RULE 13
860 IF VH<LD THEN R13=VH:GOTO 862
861 R13=LD
862 IF R13<LC THEN 864
863 R13=LC
864 IF R13<DCS THEN 866
865 R13=DCS
866 REM RULE 14
867 IF VH<MDL THEN R14=VH:GOTO 869
868 R14=MDL
869 IF R14<MDT THEN 871
870 R14=MDT
871 IF R14<LC THEN 873
872 R14=LC
873 IF R14<CSL THEN 875
874 R14=CSL
875 IF R14<CST THEN 879
876 R14=CST
879 REM RULE 15
880 IF LV<MDL THEN R15=LV:GOTO 900
890 R15=MDL
900 IF R15<MDT THEN 920
910 R15=MDT
920 IF R15<LC THEN 940
930 R15=LC
940 IF R15<CSL THEN 960
950 R15=CSL
960 IF R15<CST THEN 980
970 R15=CST
980 REM RULE 16
990 IF LV<LD THEN R16=LV:GOTO 1010
1000 R16=LD
1010 IF R16<LC THEN 1030
1020 R16=LC
1030 IF R16<DCS THEN 1720
1040 R16=DCS
1720 REM END OF RULE DESCRIPTIONS
1750 REM AVERAGE/WEIGHTED AVERAGE CALCULATIONS
1760 AV=(R1+R2+R3+R4+R5+R6+R7+R8+R9+R10+R11+R12+R13+R14+R15+R16)/16
1770 WAVS1=2*(R1+R2+R4+R7+R13+R14+R16)+3*(R3+R5+R15)+4*(R6+R8+R9)
1780 WAVS2=5*(R10+R11+R12)
1790 WAVS=(WAVS1+WAVS2)/16
1800 WAVB=(2.5*(R5+R7+R10+R15+R16)+5*(R6+R8+R9+R11+R12))/16

```

```

1830 REM END OF A/WA CALCULATIONS
1840 REM COMPARISON OF THE VOLTAGES
1850 IF XAV<AV THEN 1900
1855 IF XAV<AV OR XWAVS<WAVS OR XWAVB<WAVB THEN 4000
1860 XAV=AV:XWAVS=WAVS:XWAVB=WAVB:XXS(Z)=XS:XXV(Z)=XV:XXD(Z)=XD:XXC(Z)=XC
1865 Z=Z+1
1870 CLS:PRINT I
1900 GOTO 80
2000 REM END SECTION
2010 CLS
2020 PRINT"AVER = ";XAV:PRINT"WAVERS = ";XWAVS:PRINT"WAVRB = ";XWAVB
2030 PRINT:PRINT
2042 Y=Z+1
2045 PRINT:PRINT:PRINT:PRINT"AYNI SONUC SAYISI = ";Y
2046 PRINT:PRINT:PRINT:PRINT"GIRIS DEGISKENI KOMBINEZONU SAYISI = ";I
2050 LPRINT:LPRINT TAB(6)"XV"TAB(21)"XD"TAB(36)"XC"TAB(51)"XS":LPRINT:LPRINT
2060 FOR K=0 TO Z
2070 LPRINT XXV(K) TAB(15) XXD(K) TAB(30) XXC(K) TAB(45) XXS(K)
2080 NEXT K
2900 REM DIM SIFIRLAMA
3500 END
4000 FOR K=0 TO Z
4020 NEXT K:Z=0
4030 GOTO 1860

```



E. Calculation and Measurement Results of the Entire Controller

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] measured
1.000	1.250	0.000	0.000	2.000	2.000
1.000	1.250	0.000	0.250	2.000	2.000
1.000	1.250	0.000	0.500	2.000	2.000
1.000	1.250	0.000	0.750	2.000	1.984
1.000	1.250	0.000	1.000	2.000	1.974
1.000	1.250	0.000	1.250	2.000	1.984
1.000	1.250	0.000	1.500	2.000	2.017
1.000	1.250	0.000	1.750	2.000	2.045
1.000	1.250	0.000	2.000	2.000	2.045
1.000	1.250	0.000	2.250	2.000	2.058
1.000	1.250	0.000	2.500	2.000	2.059
1.000	1.250	0.000	2.750	2.000	2.065
1.000	1.250	0.000	3.000	2.000	2.073
1.000	1.250	0.000	3.250	2.000	2.082
1.000	1.250	0.000	3.500	2.000	2.083
1.000	1.250	0.000	3.750	2.000	2.083
1.000	1.250	0.000	4.000	2.000	2.082
1.000	1.250	0.000	4.250	2.000	2.080
1.000	1.250	0.000	4.500	2.000	2.077
1.000	1.250	0.000	4.750	2.000	2.075
1.000	1.250	0.000	5.000	2.000	2.073
1.000	1.250	0.250	0.000	2.000	2.000
1.000	1.250	0.250	0.250	2.000	2.000
1.000	1.250	0.250	0.500	2.000	2.006
1.000	1.250	0.250	0.750	2.000	1.984
1.000	1.250	0.250	1.000	2.000	1.973
1.000	1.250	0.250	1.250	2.000	1.984
1.000	1.250	0.250	1.500	2.000	2.014
1.000	1.250	0.250	1.750	2.000	2.044
1.000	1.250	0.250	2.000	2.000	2.044
1.000	1.250	0.250	2.250	2.000	2.057
1.000	1.250	0.250	2.500	2.000	2.057
1.000	1.250	0.250	2.750	2.000	2.067
1.000	1.250	0.250	3.000	2.000	2.073
1.000	1.250	0.250	3.250	2.000	2.082
1.000	1.250	0.250	3.500	2.000	2.084
1.000	1.250	0.250	3.750	2.000	2.083
1.000	1.250	0.250	4.000	2.000	2.081
1.000	1.250	0.250	4.250	2.000	2.080
1.000	1.250	0.250	4.500	2.000	2.077
1.000	1.250	0.250	4.750	2.000	2.074
1.000	1.250	0.250	5.000	2.000	2.073

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] measured
1.000	1.250	0.500	0.000	2.000	2.007
1.000	1.250	0.500	0.250	2.000	2.007
1.000	1.250	0.500	0.500	2.000	2.018
1.000	1.250	0.500	0.750	2.000	1.984
1.000	1.250	0.500	1.000	2.000	1.975
1.000	1.250	0.500	1.250	2.000	1.987
1.000	1.250	0.500	1.500	2.000	2.028
1.000	1.250	0.500	1.750	2.000	2.048
1.000	1.250	0.500	2.000	2.000	2.051
1.000	1.250	0.500	2.250	2.000	2.064
1.000	1.250	0.500	2.500	2.000	2.065
1.000	1.250	0.500	2.750	2.000	2.069
1.000	1.250	0.500	3.000	2.000	2.076
1.000	1.250	0.500	3.250	2.000	2.086
1.000	1.250	0.500	3.500	2.000	2.089
1.000	1.250	0.500	3.750	2.000	2.084
1.000	1.250	0.500	4.000	2.000	2.083
1.000	1.250	0.500	4.250	2.000	2.083
1.000	1.250	0.500	4.500	2.000	2.077
1.000	1.250	0.500	4.750	2.000	2.075
1.000	1.250	0.500	5.000	2.000	2.074
1.000	1.250	0.750	0.000	2.000	2.042
1.000	1.250	0.750	0.250	2.000	2.045
1.000	1.250	0.750	0.500	2.000	2.055
1.000	1.250	0.750	0.750	2.000	1.985
1.000	1.250	0.750	1.000	2.000	1.977
1.000	1.250	0.750	1.250	2.000	1.995
1.000	1.250	0.750	1.500	2.000	2.077
1.000	1.250	0.750	1.750	2.000	2.114
1.000	1.250	0.750	2.000	2.000	2.112
1.000	1.250	0.750	2.250	2.000	2.130
1.000	1.250	0.750	2.500	2.000	2.067
1.000	1.250	0.750	2.750	2.000	2.072
1.000	1.250	0.750	3.000	2.000	2.080
1.000	1.250	0.750	3.250	2.000	2.090
1.000	1.250	0.750	3.500	2.000	2.143
1.000	1.250	0.750	3.750	2.000	2.142
1.000	1.250	0.750	4.000	2.000	2.140
1.000	1.250	0.750	4.250	2.000	2.140
1.000	1.250	0.750	4.500	2.000	2.136
1.000	1.250	0.750	4.750	2.000	2.127
1.000	1.250	0.750	5.000	2.000	2.134

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] measured
1.000	1.250	1.000	0.000	2.000	2.164
1.000	1.250	1.000	0.250	2.000	2.165
1.000	1.250	1.000	0.500	2.000	2.176
1.000	1.250	1.000	0.750	2.000	1.991
1.000	1.250	1.000	1.000	2.000	1.990
1.000	1.250	1.000	1.250	2.000	2.043
1.000	1.250	1.000	1.500	2.000	2.175
1.000	1.250	1.000	1.750	2.000	2.205
1.000	1.250	1.000	2.000	2.000	2.204
1.000	1.250	1.000	2.250	2.000	2.209
1.000	1.250	1.000	2.500	2.000	2.135
1.000	1.250	1.000	2.750	2.000	2.071
1.000	1.250	1.000	3.000	2.000	2.081
1.000	1.250	1.000	3.250	2.000	2.161
1.000	1.250	1.000	3.500	2.000	2.214
1.000	1.250	1.000	3.750	2.000	2.212
1.000	1.250	1.000	4.000	2.000	2.212
1.000	1.250	1.000	4.250	2.000	2.210
1.000	1.250	1.000	4.500	2.000	2.210
1.000	1.250	1.000	4.750	2.000	2.209
1.000	1.250	1.000	5.000	2.000	2.108
1.000	1.250	1.250	0.000	2.000	2.262
1.000	1.250	1.250	0.250	2.000	2.263
1.000	1.250	1.250	0.500	2.000	2.260
1.000	1.250	1.250	0.750	2.000	2.093
1.000	1.250	1.250	1.000	2.000	2.100
1.000	1.250	1.250	1.250	2.000	2.183
1.000	1.250	1.250	1.500	2.000	2.250
1.000	1.250	1.250	1.750	2.000	2.405
1.000	1.250	1.250	2.000	2.000	2.407
1.000	1.250	1.250	2.250	2.000	2.419
1.000	1.250	1.250	2.500	2.000	2.374
1.000	1.250	1.250	2.750	2.000	2.233
1.000	1.250	1.250	3.000	2.000	2.239
1.000	1.250	1.250	3.250	2.000	2.377
1.000	1.250	1.250	3.500	2.000	2.502
1.000	1.250	1.250	3.750	2.000	2.490
1.000	1.250	1.250	4.000	2.000	2.480
1.000	1.250	1.250	4.250	2.000	2.466
1.000	1.250	1.250	4.500	2.000	2.447
1.000	1.250	1.250	4.750	2.000	2.413
1.000	1.250	1.250	5.000	2.000	2.417

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] measured
1.000	1.250	1.500	0.000	2.000	2.152
1.000	1.250	1.500	0.250	2.000	2.154
1.000	1.250	1.500	0.500	2.000	2.169
1.000	1.250	1.500	0.750	2.182	2.236
1.000	1.250	1.500	1.000	2.286	2.237
1.000	1.250	1.500	1.250	2.286	2.342
1.000	1.250	1.500	1.500	2.307	2.577
1.000	1.250	1.500	1.750	2.444	2.723
1.000	1.250	1.500	2.000	2.571	2.723
1.000	1.250	1.500	2.250	2.571	2.723
1.000	1.250	1.500	2.500	2.571	2.722
1.000	1.250	1.500	2.750	2.727	2.904
1.000	1.250	1.500	3.000	2.857	2.936
1.000	1.250	1.500	3.250	2.857	2.975
1.000	1.250	1.500	3.500	2.909	3.335
1.000	1.250	1.500	3.750	3.143	3.336
1.000	1.250	1.500	4.000	3.143	3.328
1.000	1.250	1.500	4.250	3.143	3.317
1.000	1.250	1.500	4.500	3.143	3.298
1.000	1.250	1.500	4.750	3.143	3.275
1.000	1.250	1.500	5.000	3.143	3.276
1.000	1.250	1.750	0.000	2.000	2.044
1.000	1.250	1.750	0.250	2.000	2.044
1.000	1.250	1.750	0.500	2.000	2.049
1.000	1.250	1.750	0.750	2.166	2.301
1.000	1.250	1.750	1.000	2.400	2.481
1.000	1.250	1.750	1.250	2.533	2.670
1.000	1.250	1.750	1.500	2.615	2.790
1.000	1.250	1.750	1.750	2.727	2.926
1.000	1.250	1.750	2.000	2.888	2.925
1.000	1.250	1.750	2.250	2.888	2.923
1.000	1.250	1.750	2.500	2.888	3.084
1.000	1.250	1.750	2.750	3.000	3.227
1.000	1.250	1.750	3.000	3.166	3.436
1.000	1.250	1.750	3.250	3.333	3.639
1.000	1.250	1.750	3.500	3.500	3.845
1.000	1.250	1.750	3.750	3.770	3.828
1.000	1.250	1.750	4.000	3.770	3.810
1.000	1.250	1.750	4.250	3.770	3.800
1.000	1.250	1.750	4.500	3.770	3.804
1.000	1.250	1.750	4.750	3.770	3.785
1.000	1.250	1.750	5.000	3.770	3.792

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] measured
1.000	1.250	2.000	0.000	2.000	2.012
1.000	1.250	2.000	0.250	2.000	2.014
1.000	1.250	2.000	0.500	2.000	2.030
1.000	1.250	2.000	0.750	2.182	2.365
1.000	1.250	2.000	1.000	2.461	2.530
1.000	1.250	2.000	1.250	2.666	2.696
1.000	1.250	2.000	1.500	2.769	2.891
1.000	1.250	2.000	1.750	2.909	2.948
1.000	1.250	2.000	2.000	3.000	2.946
1.000	1.250	2.000	2.250	3.000	2.950
1.000	1.250	2.000	2.500	3.000	3.155
1.000	1.250	2.000	2.750	3.200	3.323
1.000	1.250	2.000	3.000	3.400	3.506
1.000	1.250	2.000	3.250	3.600	3.686
1.000	1.250	2.000	3.500	3.800	3.892
1.000	1.250	2.000	3.750	4.000	3.892
1.000	1.250	2.000	4.000	4.000	3.880
1.000	1.250	2.000	4.250	4.000	3.880
1.000	1.250	2.000	4.500	4.000	3.880
1.000	1.250	2.000	4.750	4.000	3.880
1.000	1.250	2.000	5.000	4.000	3.880
1.000	1.250	2.250	0.000	2.000	2.011
1.000	1.250	2.250	0.250	2.000	2.015
1.000	1.250	2.250	0.500	2.000	2.030
1.000	1.250	2.250	0.750	2.182	2.365
1.000	1.250	2.250	1.000	2.461	2.528
1.000	1.250	2.250	1.250	2.666	2.697
1.000	1.250	2.250	1.500	2.769	2.884
1.000	1.250	2.250	1.750	2.909	2.947
1.000	1.250	2.250	2.000	3.000	2.946
1.000	1.250	2.250	2.250	3.000	2.949
1.000	1.250	2.250	2.500	3.000	3.154
1.000	1.250	2.250	2.750	3.200	3.334
1.000	1.250	2.250	3.000	3.400	3.500
1.000	1.250	2.250	3.250	3.600	3.688
1.000	1.250	2.250	3.500	3.800	3.889
1.000	1.250	2.250	3.750	4.000	3.892
1.000	1.250	2.250	4.000	4.000	3.870
1.000	1.250	2.250	4.250	4.000	3.880
1.000	1.250	2.250	4.500	4.000	3.880
1.000	1.250	2.250	4.750	4.000	3.870
1.000	1.250	2.250	5.000	4.000	3.880

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] measured
1.000	1.250	2.500	0.000	2.000	2.018
1.000	1.250	2.500	0.250	2.000	2.013
1.000	1.250	2.500	0.500	2.000	2.070
1.000	1.250	2.500	0.750	2.182	2.410
1.000	1.250	2.500	1.000	2.461	2.568
1.000	1.250	2.500	1.250	2.666	2.702
1.000	1.250	2.500	1.500	2.769	2.925
1.000	1.250	2.500	1.750	2.909	2.954
1.000	1.250	2.500	2.000	3.000	2.954
1.000	1.250	2.500	2.250	3.000	2.959
1.000	1.250	2.500	2.500	3.000	3.179
1.000	1.250	2.500	2.750	3.200	3.354
1.000	1.250	2.500	3.000	3.400	3.518
1.000	1.250	2.500	3.250	3.600	3.685
1.000	1.250	2.500	3.500	3.800	3.894
1.000	1.250	2.500	3.750	4.000	3.894
1.000	1.250	2.500	4.000	4.000	3.870
1.000	1.250	2.500	4.250	4.000	3.870
1.000	1.250	2.500	4.500	4.000	3.880
1.000	1.250	2.500	4.750	4.000	3.870
1.000	1.250	2.500	5.000	4.000	3.880
1.000	1.250	2.750	0.000	2.117	2.141
1.000	1.250	2.750	0.250	2.117	2.143
1.000	1.250	2.750	0.500	2.439	2.205
1.000	1.250	2.750	0.750	2.638	2.477
1.000	1.250	2.750	1.000	2.792	2.688
1.000	1.250	2.750	1.250	2.893	2.739
1.000	1.250	2.750	1.500	3.025	2.948
1.000	1.250	2.750	1.750	3.117	3.036
1.000	1.250	2.750	2.000	3.117	3.037
1.000	1.250	2.750	2.250	3.117	3.053
1.000	1.250	2.750	2.500	3.368	3.244
1.000	1.250	2.750	2.750	3.526	3.426
1.000	1.250	2.750	3.000	3.684	3.580
1.000	1.250	2.750	3.250	3.842	3.686
1.000	1.250	2.750	3.500	4.000	3.886
1.000	1.250	2.750	3.750	4.000	3.886
1.000	1.250	2.750	4.000	4.000	3.860
1.000	1.250	2.750	4.250	4.000	3.870
1.000	1.250	2.750	4.500	4.000	3.870
1.000	1.250	2.750	4.750	4.000	3.870
1.000	1.250	2.750	5.000	4.000	3.870

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] measured
1.000	1.250	3.000	0.000	2.210	2.199
1.000	1.250	3.000	0.250	2.210	2.199
1.000	1.250	3.000	0.500	2.210	2.223
1.000	1.250	3.000	0.750	2.553	2.671
1.000	1.250	3.000	1.000	2.760	2.710
1.000	1.250	3.000	1.250	2.880	2.888
1.000	1.250	3.000	1.500	2.980	3.019
1.000	1.250	3.000	1.750	3.110	3.157
1.000	1.250	3.000	2.000	3.210	3.156
1.000	1.250	3.000	2.250	3.210	3.158
1.000	1.250	3.000	2.500	3.210	3.346
1.000	1.250	3.000	2.750	3.450	3.450
1.000	1.250	3.000	3.000	3.600	3.636
1.000	1.250	3.000	3.250	3.739	3.687
1.000	1.250	3.000	3.500	3.863	3.875
1.000	1.250	3.000	3.750	4.000	3.876
1.000	1.250	3.000	4.000	4.000	3.860
1.000	1.250	3.000	4.250	4.000	3.860
1.000	1.250	3.000	4.500	4.000	3.860
1.000	1.250	3.000	4.750	4.000	3.860
1.000	1.250	3.000	5.000	4.000	3.860
1.000	1.250	3.250	0.000	2.333	2.303
1.000	1.250	3.250	0.250	2.333	2.297
1.000	1.250	3.250	0.500	2.333	2.400
1.000	1.250	3.250	0.750	2.625	2.702
1.000	1.250	3.250	1.000	2.857	2.757
1.000	1.250	3.250	1.250	2.952	2.937
1.000	1.250	3.250	1.500	3.055	3.178
1.000	1.250	3.250	1.750	3.214	3.264
1.000	1.250	3.250	2.000	3.333	3.255
1.000	1.250	3.250	2.250	3.333	3.264
1.000	1.250	3.250	2.500	3.333	3.419
1.000	1.250	3.250	2.750	3.500	3.470
1.000	1.250	3.250	3.000	3.660	3.647
1.000	1.250	3.250	3.250	3.770	3.686
1.000	1.250	3.250	3.500	3.875	3.880
1.000	1.250	3.250	3.750	4.000	3.886
1.000	1.250	3.250	4.000	4.000	3.860
1.000	1.250	3.250	4.250	4.000	3.870
1.000	1.250	3.250	4.500	4.000	3.870
1.000	1.250	3.250	4.750	4.000	3.870
1.000	1.250	3.250	5.000	4.000	3.870

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] measured
1.000	1.250	3.500	0.000	2.571	2.657
1.000	1.250	3.500	0.250	2.571	2.657
1.000	1.250	3.500	0.500	2.571	2.676
1.000	1.250	3.500	0.750	2.850	2.956
1.000	1.250	3.500	1.000	3.071	3.000
1.000	1.250	3.500	1.250	3.072	3.100
1.000	1.250	3.500	1.500	3.152	3.430
1.000	1.250	3.500	1.750	3.382	3.623
1.000	1.250	3.500	2.000	3.571	3.620
1.000	1.250	3.500	2.250	3.571	3.625
1.000	1.250	3.500	2.500	3.571	3.660
1.000	1.250	3.500	2.750	3.700	3.667
1.000	1.250	3.500	3.000	3.769	3.666
1.000	1.250	3.500	3.250	3.769	3.690
1.000	1.250	3.500	3.500	3.850	3.907
1.000	1.250	3.500	3.750	4.000	3.910
1.000	1.250	3.500	4.000	4.000	3.890
1.000	1.250	3.500	4.250	4.000	3.890
1.000	1.250	3.500	4.500	4.000	3.890
1.000	1.250	3.500	4.750	4.000	3.890
1.000	1.250	3.500	5.000	4.000	3.890
1.000	1.250	3.750	0.000	3.000	2.980
1.000	1.250	3.750	0.250	3.000	2.976
1.000	1.250	3.750	0.500	3.000	2.979
1.000	1.250	3.750	0.750	3.230	3.233
1.000	1.250	3.750	1.000	3.473	3.432
1.000	1.250	3.750	1.250	3.571	3.608
1.000	1.250	3.750	1.500	3.689	3.820
1.000	1.250	3.750	1.750	3.869	3.930
1.000	1.250	3.750	2.000	4.000	3.927
1.000	1.250	3.750	2.250	4.000	3.925
1.000	1.250	3.750	2.500	4.000	3.904
1.000	1.250	3.750	2.750	4.000	3.897
1.000	1.250	3.750	3.000	4.000	3.900
1.000	1.250	3.750	3.250	4.000	3.910
1.000	1.250	3.750	3.500	4.000	3.920
1.000	1.250	3.750	3.750	4.000	3.934
1.000	1.250	3.750	4.000	4.000	3.920
1.000	1.250	3.750	4.250	4.000	3.920
1.000	1.250	3.750	4.500	4.000	3.920
1.000	1.250	3.750	4.750	4.000	3.920
1.000	1.250	3.750	5.000	4.000	3.920

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] measured
1.000	1.250	4.000	0.000	3.000	2.942
1.000	1.250	4.000	0.250	3.000	2.942
1.000	1.250	4.000	0.500	3.000	2.946
1.000	1.250	4.000	0.750	3.200	3.232
1.000	1.250	4.000	1.000	3.461	3.445
1.000	1.250	4.000	1.250	3.615	3.636
1.000	1.250	4.000	1.500	3.727	3.810
1.000	1.250	4.000	1.750	3.888	3.911
1.000	1.250	4.000	2.000	4.000	3.912
1.000	1.250	4.000	2.250	4.000	3.909
1.000	1.250	4.000	2.500	4.000	3.900
1.000	1.250	4.000	2.750	4.000	3.899
1.000	1.250	4.000	3.000	4.000	3.900
1.000	1.250	4.000	3.250	4.000	3.904
1.000	1.250	4.000	3.500	4.000	3.915
1.000	1.250	4.000	3.750	4.000	3.914
1.000	1.250	4.000	4.000	4.000	3.900
1.000	1.250	4.000	4.250	4.000	3.900
1.000	1.250	4.000	4.500	4.000	3.900
1.000	1.250	4.000	4.750	4.000	3.900
1.000	1.250	4.000	5.000	4.000	3.900
1.000	1.250	4.250	0.000	3.000	2.926
1.000	1.250	4.250	0.250	3.000	2.926
1.000	1.250	4.250	0.500	3.000	2.929
1.000	1.250	4.250	0.750	3.182	3.216
1.000	1.250	4.250	1.000	3.461	3.452
1.000	1.250	4.250	1.250	3.651	3.650
1.000	1.250	4.250	1.500	3.756	3.801
1.000	1.250	4.250	1.750	3.903	3.903
1.000	1.250	4.250	2.000	4.000	3.900
1.000	1.250	4.250	2.250	4.000	3.898
1.000	1.250	4.250	2.500	4.000	3.896
1.000	1.250	4.250	2.750	4.000	3.899
1.000	1.250	4.250	3.000	4.000	3.900
1.000	1.250	4.250	3.250	4.000	3.902
1.000	1.250	4.250	3.500	4.000	3.904
1.000	1.250	4.250	3.750	4.000	3.907
1.000	1.250	4.250	4.000	4.000	3.890
1.000	1.250	4.250	4.250	4.000	3.890
1.000	1.250	4.250	4.500	4.000	3.890
1.000	1.250	4.250	4.750	4.000	3.890
1.000	1.250	4.250	5.000	4.000	3.890

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] measured
1.000	1.250	4.500	0.000	3.000	2.922
1.000	1.250	4.500	0.250	3.000	2.923
1.000	1.250	4.500	0.500	3.000	2.926
1.000	1.250	4.500	0.750	3.182	3.214
1.000	1.250	4.500	1.000	3.461	3.456
1.000	1.250	4.500	1.250	3.666	3.650
1.000	1.250	4.500	1.500	3.769	3.832
1.000	1.250	4.500	1.750	3.909	3.901
1.000	1.250	4.500	2.000	4.000	3.902
1.000	1.250	4.500	2.250	4.000	3.900
1.000	1.250	4.500	2.500	4.000	3.900
1.000	1.250	4.500	2.750	4.000	3.899
1.000	1.250	4.500	3.000	4.000	3.899
1.000	1.250	4.500	3.250	4.000	3.903
1.000	1.250	4.500	3.500	4.000	3.903
1.000	1.250	4.500	3.750	4.000	3.904
1.000	1.250	4.500	4.000	4.000	3.890
1.000	1.250	4.500	4.250	4.000	3.890
1.000	1.250	4.500	4.500	4.000	3.890
1.000	1.250	4.500	4.750	4.000	3.890
1.000	1.250	4.500	5.000	4.000	3.890
1.000	1.250	4.750	0.000	3.000	2.922
1.000	1.250	4.750	0.250	3.000	2.922
1.000	1.250	4.750	0.500	3.000	2.937
1.000	1.250	4.750	0.750	3.182	3.217
1.000	1.250	4.750	1.000	3.461	3.451
1.000	1.250	4.750	1.250	3.666	3.648
1.000	1.250	4.750	1.500	3.769	3.790
1.000	1.250	4.750	1.750	3.909	3.901
1.000	1.250	4.750	2.000	4.000	3.900
1.000	1.250	4.750	2.250	4.000	3.900
1.000	1.250	4.750	2.500	4.000	3.899
1.000	1.250	4.750	2.750	4.000	3.900
1.000	1.250	4.750	3.000	4.000	3.900
1.000	1.250	4.750	3.250	4.000	3.901
1.000	1.250	4.750	3.500	4.000	3.905
1.000	1.250	4.750	3.750	4.000	3.905
1.000	1.250	4.750	4.000	4.000	3.890
1.000	1.250	4.750	4.250	4.000	3.890
1.000	1.250	4.750	4.500	4.000	3.890
1.000	1.250	4.750	4.750	4.000	3.890
1.000	1.250	4.750	5.000	4.000	3.890

I_C [V]	I_V [V]	I_D [V]	I_S [V]	O_{SP} [V] calculated	O_{SP} [V] measured
1.000	1.250	5.000	0.000	3.000	2.922
1.000	1.250	5.000	0.250	3.000	2.922
1.000	1.250	5.000	0.500	3.000	2.928
1.000	1.250	5.000	0.750	3.182	3.216
1.000	1.250	5.000	1.000	3.461	3.451
1.000	1.250	5.000	1.250	3.666	3.650
1.000	1.250	5.000	1.500	3.769	3.840
1.000	1.250	5.000	1.750	3.909	3.900
1.000	1.250	5.000	2.000	4.000	3.900
1.000	1.250	5.000	2.250	4.000	3.901
1.000	1.250	5.000	2.500	4.000	3.898
1.000	1.250	5.000	2.750	4.000	3.899
1.000	1.250	5.000	3.000	4.000	3.900
1.000	1.250	5.000	3.250	4.000	3.903
1.000	1.250	5.000	3.500	4.000	3.904
1.000	1.250	5.000	3.750	4.000	3.905
1.000	1.250	5.000	4.000	4.000	3.890
1.000	1.250	5.000	4.250	4.000	3.890
1.000	1.250	5.000	4.500	4.000	3.890
1.000	1.250	5.000	4.750	4.000	3.890
1.000	1.250	5.000	5.000	4.000	3.890

BIOGRAPHY

Banu Pamir received the B.S. and M.S. degrees in electronics from Istanbul Technical University, Istanbul, Turkey, in 1988 and 1991, respectively. Since 1988, she has been working as a Research Assistant at the Electronics and Communication Engineering Department of Istanbul Technical University. From 1992-1994 she was also with ETA ASIC Design Center, Istanbul, developing full-custom mixed-mode industrial ASIC's. Her research interests are in the area of analog electronics.

