ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

TEMPERATURE TO DIGITAL CONVERTER DESIGN AND MEASUREMENT

M.Sc. THESIS

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

SICAKLIK - SAYISAL DÖNÜŞTÜRÜCÜ TASARIMI VE ÖLÇÜMÜ

YÜKSEK LİSANS TEZİ

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ARALIK 2016

Ahmet Mert Ozdemir, a M.Sc. student of ITU Graduate School of Science Engineering and Technology 504131202 successfully defended the thesis entitled **"TEMPERATURE TO DIGITAL CONVERTER DESIGN AND MEASUREMENT"**, which he/she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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To my love, friends and family,

FOREWORD

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December 2016 Ahmet Mert Ozdemir

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ABBREVIATIONS

DC : Direct Current
AC : Alternating Current
ADC : Analog to Digital Converter
DAC : Digital to Analog Converter
IC : Integrated Circuit
LSB : Least Significant Bit
MSB : Most Significant Bit
OPAMP : Operational Amplifier
I2C : Inter-Integrated Circuit
SoC : System on Chip
PTAT : Proportional to Absolute Temperature
PSD : Power Spectral Density
MOS : Metal Oxide Semiconductor
MOSFET : Metal Oxide Semiconductor Field Effect Transistor
CMOS : Complementary Metal Oxide Semiconductor
NMOS : N Channel Type Complementary Metal Oxide Semiconductor
PMOS : P Channel Complementary Metal Oxide Semiconductor
POR : Power On Reset
ESD : Electrostatic Discharge
VCO : Voltage Controlled Oscillator
TDC : Temperature to Digital Converter
PCB : Printed Cicuit Board
BJT : Bipolar Junction Transistor
NPN : N Type Bipolar Junction Transistor
PNP : P Type Bipolar Junction Transistor
ppm : Parts Per Million
STF : Signal Transfer Function
NTF : Noise Transfer Function
ENOB : Effective Number of Bits
SNR : Signal to Noise Ratio
SFDR : Spurious Free Dynamic Range
DR : Dynamic Range
MPW : Multi Project Wafer
JLCC : J-Leaded Ceramic Chip Carrier
LDO : Low Dropout Regulator
PSRR : Power Supply Rejection Ratio
SMD : Surface Mount Device
SMA : SubMiniature version A
SOT : Small Outline Transistor
WSON : Very Very Thin Small Outline Non-Leaded
LFCSP : Lead Frame Chip Scale Package
GSa/s : Giga Sample per Second

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TEMPERATURE TO DIGITAL CONVERTER DESIGN AND MEASUREMENT

SUMMARY

Integrated circuits (ICs) dominates modern electronic and today ICs have penetrated in people's everyday life. It had begun with personal computers, continued with cell phones and evolved to smart phones. With Internet of Things (IoT) every devices (cars, buildings, cities etc.) will be connected through wifi.

The most important aspects of these ICs and applications are performance and power consumption. These two metric is strongly depended each other. Performance requires more power consumption where power consumption leads to heat dissipation.

The heat dissipation raises the temperature of both the IC and the device contains that particular IC. This leads to two major problems. First of all high temperature may burn the IC and the device. The second aspect is ICs performance metrics change with temperature varitaion regardless of hot or cold.

To protect ICs and devices, temperature must be controlled. The control mechanism can be cooling down the IC/Device with a cooling system (fan or liquid) or turn of the IC/Device.

To stabilize performance of ICs over temperature change is essential to have reliable and robust devices. To accomplish this it is needed to adjust parameters, current or voltage, of the IC with drifting temperature.

To accomplish these goals first temperature must be sensed and monitored. Temperature sensing can be performed in the IC itself or in a device with separate IC dedicated to temperature sensing. When temperature is sensed, it need to be turn into a digital code to process.

In this thesis, a temperature sensing IC, based on Sigma Delta modulator is measured and characterized. The results matche to simulation results of the designed IC and show that designed temperature sensor is working and it can be used as an IP in other ICs or as a separate IC in systems which requires temperature sensing.

Temperature to digital converter is designed and taped-out using AMS035HB4 process. The dimension of the IC core is 1024um X 600um while full chip with esd and pad rings occupying 1024um X 1395um. The simulation results show that 12 bits temperature to digital conversion is achieved with 0.25C resolution while measurement verifies 10 bits temperature to digital conversion with 1 C resolution.

SICAKLIK - SAYISAL DÖNÜŞTÜRÜCÜ TASARIMI VE ÖLÇÜMÜ

ÖZET

Tümleşik devreler modern elektroniği domine etmekte ve günümüzde insanların yaşamlarının her alanına girmiş bulunaktadır. Bu gelişme kişisel bilgisayarlar ile başladı ve en son akıllı telefon olarak adlandırılan cep telefonları ile devam etti. Son zamanlarda gelşmekte olan Nesnelerin İnterneti teknolojisi isminden de anlaşılacağı üzere tüm nesnelerin, özellikle arabalar ve hatta şehirlerin internet üzerinden birbiriyle bağlanması planlanmaktadır. Tüm bu gelişmeler, tümleşik devrelerin icat edilmesi ve bu teknolojinin sürekli olarak geliştirilmesi sayesinde yaşanabilmektedir.

Tümleşik devrelerin ve bu develeri içeren sistemlerin en önemli iki parametresi güç tüketimi ve performans olmakla beraber güç tüketiminin düşük, performansın yüksek olması istenmektedir. Ancak bu iki parametre birbirine son derece bağımlıdır ve genellikle yüksek performans yüksek güç tüketimi anlamına gelmektedir.

Bir tümleşik devre veya sistemin güç tüketiminin yüksek olması iki temel sorun ortaya çıkarır. Bunlardan ilki tümleşik devre veya sistem, cep telefonu ve dizüstü bilgisayarlarda olduğu gibi pil ile çalıştırılıyorsa daha kısa pil ömrü ve dolayısıyla daha kısa kullanım süresi anlamına gelir. İkinci olarak da güç tüketimi arttıkça ısı yayılması da doğru oranda artarak tümleşik devre ve sistemin sıcaklığının yükselmesine sebep olur.

Bir tümleşik devre ve sistemin sıcaklığının çok yükselmesi devre ve sistemin yanması veya bozulmasıyla sonuçlanabilir. Sistemin yanması gibi sonuçlar doğurmayacak sıcaklık değişimleri de tümleşik devre ve sistemin performans metriklerini olumsuz etkiler. Bu nedenle çok yüksek sıcaklıklarda sitemin yanmasını engelleyecek soğutma veya kapama önlemleri almak ve sistemin her sıcaklıkta aynı performansı verecek şekilde konfigüre edilerek daha güvenilir ve dayanıklı bir sistem elde etmek gerekmektedir. Bu işlemleri gerçekleştirebilmek için öncelikle sıcaklık bilgisinin ölçülmesi ve monitör edilmesi gerekir. Sıcaklık ölçümü tümleşik devre içerisnde yapılabileceği gibi sistemde ayrı bir sıcaklık sensör tümleşik devresi ile de yapılabilir. Sıcaklık bilgisinin sayısal işarete dönüştürülmesi ile de sıcaklık bilgisi günümzde yaygın olan sayısal sistemlerde daha kolay işlenebilir.

Küçük alanda düşük güç tüketimli karmaşık devreler elde edebilmek için CMOS teknolojisinin gelişmesi ve eleman boyutlarının küçülmesi gerekmetedir. Moore yasası olarak bilinen ilke, eleman boyutlarının küçülmesi ile bir tümleşik devre içerisindeki transistör sayısının her iki senede bir iki katına çıkacagını öngörmektedir. Küçük alanda yüksek performans trendi tümleşik devre içerisinde yüksek integrasyon ve güç yoğunlukları ve buna bağlı olarak yüksek ısıl değişimleri ile yüksek çalışma sıcaklıkları anlamına gelmektedir. Yüksek performanslı ve uzun dönemde güvenilir tümleşik devreler elde edebilmek için hassas sıcaklık sensörlere ihtiyaç duyulmaktadır.

Hassas sıcaklık sensörlerinin tümleşik devrelerin performans ve güvenirliğinin iyileştirlmesi için kritik bir parçası olarak görülmektedir. Bu nedenle birçok araştırmacı sıcaklık sensörlerinden yararlanarak kalibrasyon devreleri veya sıcaklık geribildirimli sistemler kurarak tasarladıkları tümleşik devrelerin performansını arttıracak tasarım teknikleri üzerinde çalışmaktadır. Bu çalışmada tasarlanan sıcaklık sensorü ile bir gerilim kontrollü osilatörün frekansının sıcaklık ile değişimini azaltmak amaçlanmaktadır.

Tümleşik devre içerisine konulacak bir sıcaklık sensörü için gerekli kriterler oldukça zorlayıcıdır. Sensörün, sıcaklık ölçümü yapılacak yere yakın konulabilmesi için boyutunun küçük olması gerekmektedir. Ayrıca sensör düşük güç tüketmeli ki kendi ürettiği ısı ile fazladan bir hata getirmesin. Bunlarla beraber sensörün çalışma sıcaklık aralağının geniş ve çözünürlüğünün yüksek olması gerekmektedir. Toplam sıcaklık hatası, tümleşik devre sıcaklığının ölçülmesindedeki hata ve sıcaklık sensörünün kendi hatasının toplamından oluşur. Ölçüm test ortamının sıcaklığının belirsizliği tipik olarak $\pm 0.5C$ seviyesında olduğu düşünülürse sıcaklık sensörünün çözünürlüğünün minimum $\pm 0.9C$ olması gerekir. Bu nedenle bu çalışmada tasarlanan sıcaklık sayısal dönüştürücünün -40C 85C aralığında minumum çözünürlüğünün $\pm 0.5C$ olması hedeflenmiştir.

Sıcaklık ölçmek için farklı topolojiler öneren pek çok araştırma bulunmaktadır. Sıcaklık sensörünün en önemli iki özelliği kapladığı alan ve güç tüketimi olduğundan, çalışmalar bu iki parametreden en az biri ya da ikisini birden optimize ederek gerekli çözünürlüğü elde etmek üzerine yoğunlaşmaktadır. Referanslarda belirtilen çalışmada (Wang, 2016) alan ve güç optimize edilmesine rağmen $\pm 0.9C$ çözünürlük sadece 60C 90C aralığında elde eilmiştir. Diğer bir çalışmada ise (Anand, Makinwa, & Hanumolu, 2016) gerilim kontrollü osilatörün frekansının sıcaklık ile değişimi ile bir sıcaklık sensörü önerilmiştir. Ancak bu çalışmada da sıcaklık aralığığ 0C ile 100C arasında sınırlı kalmış ve iki kalibrasyon sonucunda $\pm 0.9C$ çözünürlük elde edilebilmiştir. Elektro-ısıl süzgeç ile sıcaklık ölçümü öneren bir çalışma (Kashmiri, Xia, & Makinwa, 2009), -55C 125C askeri sıcaklık aralığında $\pm 0.7C$ çözünürlük elde edebilmiş ancak devre $2.3mm^2$ alan kaplamaktadır. Çalışmada ayrıca offset gerilimi ve düşük freakans flicker gürültüsünü module etmek için chopper tekniği kullanılmıştır. Bu calışmada kullanılan yapıyla benzerlik gösteren bir calışmada (Pu et al., 2015) -40C 130C aralığında 0.4C çözünürlük $0.2mm^2$ alanda elde edilmişitr. Fakat calışma 65nm CMOS teknolojisinde tasarlanmakla beraber PN jonksiyon olarak ayrık BJT transistorleri kullanılmış ve iki kalibrasyon metodu kullanılmıştır.

Bugune kadar önerilen çalışmalarda alan ve güç tüketimi optimize edilirken istenilen çözünürlük seviyeleri kısıtlı bir sıcaklık aralığında elde edildiği gözlemlenmiştir. Sıcaklık aralığının yüksek ve çözünürlüğün iyi olduğu çalışmalarda ise alanın büyüdüğü görülmüştür. Bu nedenle düşük alan ve güç tüketimiyle geniş sıcaklık aralığında minimum kalibrasyon ile yüksek çözünürlük elde etmek oldukça önemlidir.

Bu çalışmada AMS 0.35u CMOS teknolojisinde 12 bitlik bir sıcaklık sayısal dönüştürücü tasalarlandı ve serimi yapıldı. Tasarlanan dönüştürücü Euro Practice aracılığıyla İTÜ VLSI Labs finans desteği ile üretildi. Sıcaklık sayısal dönüştürücü sıcaklık ölçümü için bir P-N jonksiyonu kullanırken, sayısal dönüşüm için ikinci derece sigma delta modulatör kullanmaktadır. Offset ve düşük frekans flicker gürültüsünü azaltmak ve modüle etmek için iki farklı teknik uygulanmıştır. Dönüştürücünün yonga boyutları 1024um X 600um $0.6144mm^2$ iken giriş çıkış padleri

ve ESD elamanlar ile birlikte toplamda 1.43mm^2 alan kaplamaktadır. Simulasyon sonuçları ile -40C 85C sıcaklık aralığıda 12 bitlik 0.25C çözünürlük gösterilmiş ve ölçüm sonuçları ile yine aynı sıcaklık aralığında 10 bitlik 1C çözünürlük doğrulanmıştır.

Sonuçlar bölümünde çalışmanın geliştirilmesi için yapılması gerekenler belirtilmiş ve çalışmanın geliştirilmesi ile bir doktora çalışmasına dönüşme ihtimali gösterilmiştir. İTÜ bünyesinde bulunacak olan endüstrü seviyesinde bir sıcaklık sayısal dönüştürücü, ilerdeki sıcaklık sensörü ihtiyaç duyan akademik çalışmalarda bir IP ya da sistemlerde ayrı bir tümleşik devre olarak kullanılabilir.

1. INTRODUCTION

1.1 Introduction

With the dramatic rising in the demand for smart phones, tablets and even smart cars nowadays CMOS technology is forced to scale down device dimensions in order to achieve complex functionality in a small area with low power consumption. As a generalization of Moore's law, the downward scaling of feature sizes in semiconductor processes has been paralleled with a doubling of the number of components in an integrated circuit about every two years. Demand for high performance in a small area has led to higher integration density, increased power density, larger thermal gradients, highly localized hotspots, and higher operating temperatures in the integrated circuits. In order to achieve high performance and long-term reliability for ICs, accurate temperature sensors with low-power consumption and small-chip area are needed to provide sensory input to the thermal management units.

Since accurate temperature measurement has become recognized as a critical part of the power and thermal management of an integrated circuit that is needed to prevent performance and reliability degradation, most researcher have focused on pursuing better performance by incorporating elaborate circuit design techniques such as digitally-assisted feedback loops to enhance performance of ICs such as low dropout regulators, slew-rate enhancement to improve the high-frequency performance of amplifiers, and oscillators to improve the frequency drift over temperature. This work focuses on the temperature sensor to minimize temperature drift of voltage controlled oscillator (VCO).

The requirements for an on-die temperature sensor are quite strict. The sensor need to be occupy small area in order to place them close to critical transistors or blocks in IC. The temperature sensor also should consume less power as possıble as to prevent extra errors from self heating. Finally the sensor need to have high resolution, accuracy to achieve targeted goals with thermal algorithms without degrading system performance. The total temperature error is the sum of the error in measuring the

actual die temperature at trim plus the error in the temperature sensor itself. A typical uncertainty of the trim temperature in a production testing environment is $\pm 0.5C$. If the trim temperature error is $\pm 0.5C$, the accuracy required for the temperature sensor itself is $\pm 0.9C$ (Wang, 2016). Thus, for this work, the target accuracy of the on-chip temperature sensors for thermal management has been set at $\pm 0.25C$ in the range of -40C to 85C.

There are several studies which proposes different architectures to sense temperature. Since the area and power consumption is the most critical part of the temperature sensors, the studies focus on optimize at least one of these performance metric while having needed temperature resolution. The area and power optimized in (Wang, 2016), but it does have temperature accuracy of $\pm 0.9C$ throughout the 60C, 90C temperature range. Also in (Anand et al., 2016) vco frequency drift over temperature is used as temperature sensor, but the work has range of 0C to 100C with a resolution of $\pm 0.9C$ after 2 points calibration while having good area and power performance. Another paper is proposed to sense temperature with an electrothermal filter (Kashmiri et al., 2009). It has temperature accuracy of $\pm 0.7C$ over the range from -55C to 125C which is military range. However it has a huge area of $2.3mm^2$. The work also has chopper stabilization method to eliminate offset and the low frequency flicker noise. Another study (Pu et al., 2015) which is using a similar architecture as in this work, a PN junction to create temperature information and a sigma delta ADC to converting digital, achieve 0.4C resolution in the temperature range -40C to 130C with $0.2mm^2$. However the study is using external BJTs and two external calibration methods and manufactured in 65nm CMOS process.

As seen from proposed papers up-to today, they focused on the power and area performance where they have limited temperature range and accuracy and moving the low frequency noise to higher frequency with chopper stabilization technique. Therefore it is important to have maximum temperature resolution while having small area and less power consumption in a wide temperature range while reducing the low frequency flicker noise beside moving it out of the band.

In this work, a 12 bit temperature to digital converter with a resolution of 0.25C is designed, presented with simulation results and laid out. Then designed TDC is manufactured through Euro Practice with financial support of ITU VLSI LAbs. The temperature to digital converter are using a P-N junction to sense the temperature and

a sigma delta modulator for digital conversion. Two technique are implemented to reduce and modulate the low frequency noise to higher frequencies. The dimension of the core is 1024um X 600um which is $0.6144mm^2$ while full chip with esd occupies $1.43mm^2$. TDC is measured in a temperature chamber and measurement results verify 10 bit temperature to digital conversion with a 1C resolution.

1.2 Organization of Thesis

This thesis is organized in 6 chapters.

In this chapter, a brief summary of the thesis is introduced.

In chapter 2, selected temperature to digital converter architecture is given. Schematic design of each blocks in the architecture and full system are explained. Simulation results of sub blocks and top level are presented.

In chapter 3, layout design of temperature to digital converter is explained in detailed for both sub-blocks and top level.

In chapter 4, package selection for the temperature to digital converter is given. Printed circuit board (PCB) design is explained in detailed for both schematic and layout design.

In chapter 5, measurement method and setup of evaluation board of temperature to digital converter are presented. Then measurement results are given with a comparison to simulation results.

Finally, chapter 6 concludes the thesis and discuss the future works.

2. SCHEMATIC DESIGN OF THE TEMPERATURE TO DIGITAL CONVERTER

2.1 Architecture

The architecture given in the Figure 2.1 is constructed to convert temperature information to digital signal. As seen in the Figure 2.1 first a proportional to absolute temperature (PTAT) current is generated and PTAT current can be scaled by a current DAC. Then it is followed by a voltage buffer which translate PTAT current into a PTAT voltage to drive sigma delta modulator to convert analog voltage into single bit digital stream. At the end, a digital counter performs filtering at DC by counting number of logic 1 and dividing result by counter value.

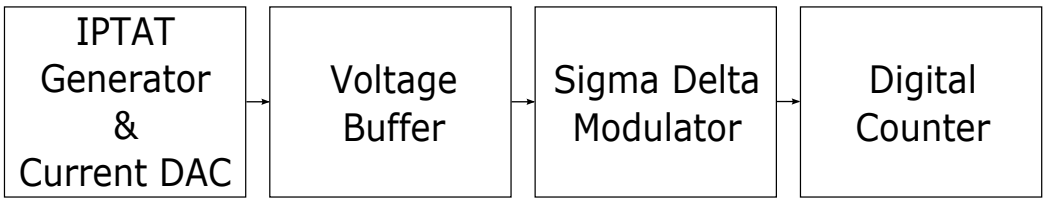

Figure 2.1 : Temperature to Digital Converter Architecture

In the following sections each block in the architecture will be analysed and their performance will be shown.

2.1.1 PTAT current generator

To generate a proportional to absolute temperature (PTAT) current, firstly a voltage difference between two p-n junctions (e.g. diodes), operated at different current densities must be generated. Then this voltage is translated into current by simply applying it to a resistor. A generic PTAT current generator can be seen in the Figure 2.2 (Razavi, 2001).

Diode connected Q_1 and Q_2 PNP type bipolar junction transistors realise p-n junctions while different current density is created by selecting Q_2, n times bigger than Q_1. This creates a voltage difference ΔV_{BE} between base-emitter voltage of Q_1 V_{BE1} and Q_2 V_{BE2}. Then ΔV_{BE} is translated into current on R_1 resistor which is called PTAT

current and it is copied to output by a current mirror consist of M_4 and M_5 PMOS transistors. To derive the equation for PTAT current and its temperature coefficient, following equation set is solved.

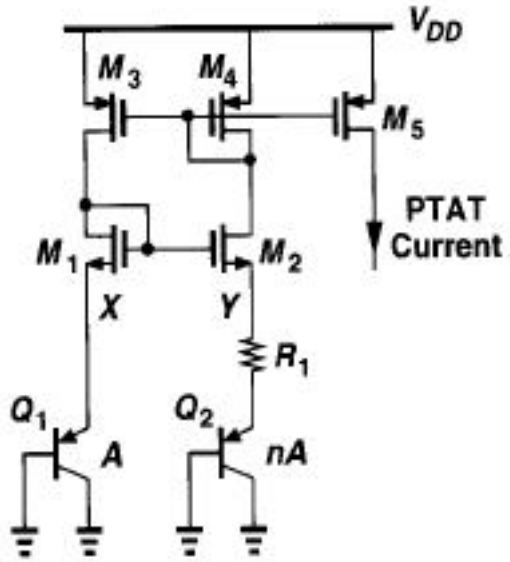

Figure 2.2 : A Generic PTAT Current Generator

Firstly lets write V_{BE} voltages for Q_1 and Q_2 and ΔV_{BE} voltage.

$$\begin{aligned} V_{BEQ1} &= V_t \cdot ln(\frac{I_{cQ1}}{I_{sQ1}}) \\ V_{BEQ2} &= V_t \cdot ln(\frac{I_{cQ2}}{I_{sQ2}}) \end{aligned} \tag{2.1}$$

$$\Delta V_{BE} = V_{BEQ2} - V_{BEQ2} = V_t \cdot ln(\frac{I_{CQ2}}{I_{SQ2}} \cdot \frac{I_{SQ1}}{I_{CQ1}}) \tag{2.2}$$

Due to Q_2 is n times bigger than Q_1;

$$I_{SQ1} = n \cdot I_{SQ2} \tag{2.3}$$

$$\Delta V_{BE} = V_t \cdot ln(\frac{I_{CQ2}}{I_{SQ2}} \cdot \frac{n \cdot I_{SQ2}}{I_{CQ1}}) \tag{2.4}$$

and since $I_{CQ1} = I_{CQ2}$;

$$\Delta V_{BE} = V_t \cdot ln(n) \tag{2.5}$$

In this case I_{PTAT} is given as in the Equation (2.6).

$$I_{PTAT} = \frac{V_t \cdot ln(n)}{R_1} \tag{2.6}$$

V_t is the thermal voltage given in the formula below.

$$V_t = \frac{k \cdot T}{q} \tag{2.7}$$

where k is Boltzman constant, $1.38 \cdot 10^{-24} J/K$, T is the absolute temperature in Fahrenheit $300F$ at room temperature and q is the magnitude of the electrical charge on electron $1.6 \cdot 10^{-19} C$, the value of the thermal voltage V_t is approximately $26mV$ at room temperature.

$$V_t = \frac{1.38 \cdot 10^{-23} \cdot 300}{1.60 \cdot 10^{-19}} = 25.875 \tag{2.8}$$

To obtain temperature coefficient of I_{PTAT} derivative of I_{PTAT} respect to the temperature is calculated as below.

$$\frac{d}{dT} I_{PTAT} = \frac{d}{dT} \frac{V_t \cdot ln(n)}{R_1} \tag{2.9}$$

$$\frac{d}{dT} I_{PTAT} = \frac{d}{dT} V_t \cdot \frac{d}{dT} \frac{ln(n)}{R_1} \tag{2.10}$$

If temperature dependency of resistor R_1 is neglected;

$$\frac{d}{dT} I_{PTAT} = \frac{d}{dT} V_t \cdot \frac{ln(n)}{R_1} \tag{2.11}$$

Temperature coefficient of V_t is approximately $+0.085mV/C$ and Equation (2.11) shows that temperature coefficient of PTAT current is positive which means it is proportional to temperature and the value of the temperature coefficient is determined by the ratio of sizes of two bipolar transistor n and resistor R_1.

In this work a bandgap reference circuit, which is previously designed in the same process and also characterized with measurement, is used to generate I_{PTAT}. PTAT core of reference circuit is shown in the Figure 2.3 (Ozkaya, 2010).

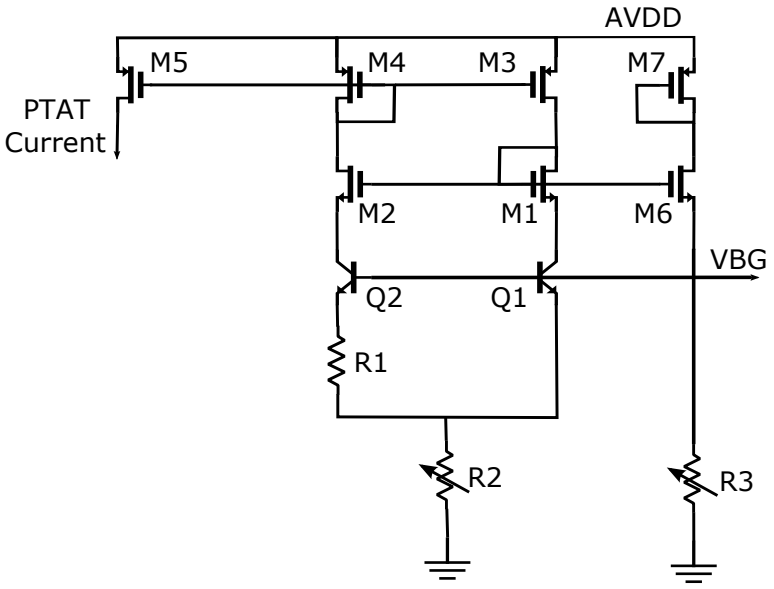

Figure 2.3 : Designed PTAT Current Generator

PTAT current generator core slightly differs from traditional PTAT core but the principle is still the same. Q_1 and Q_2 bipolar transistors are NPN type rather than PNP type and their base terminals are biased with V_{BG} voltage which is approximately $1.2V$ rather than diode connected. Q_2 is 8 times bigger than Q_1 to create voltage difference on R_1 to obtain PTAT current. There are 2 PTAT current outputs available in bandgap reference circuit. There are also several voltage and current outputs of bandgap reference circuit including V_{BG} which can be adjusted by changing value of resistor R_2 and bandgap currents in 1uA, 2.5uA, 5uA and 10uA units which again can be adjusted by changing value of resistor R_3 with an I2C controlled memory. I2C controlled memory will be explained in the following chapters.

In this work V_{BG} reference voltage is not used while 5uA and 10uA bandgap current outputs are used for biasing analog circuits and PTAT current outputs are used for converting temperature information into current.

The ratio between bipolar transistors n and R1 of the PTAT core are 8 and 20Kohm respectively. If Equation (2.6) is solved for the scheme shown in the Figure 2.3 for these values PTAT current at $27C$ can be found as approximetley $2.7uA$.

$$Iptat = 26 \cdot 10^{-3} \cdot \frac{ln(8)}{20000} = 2.7uA \tag{2.12}$$

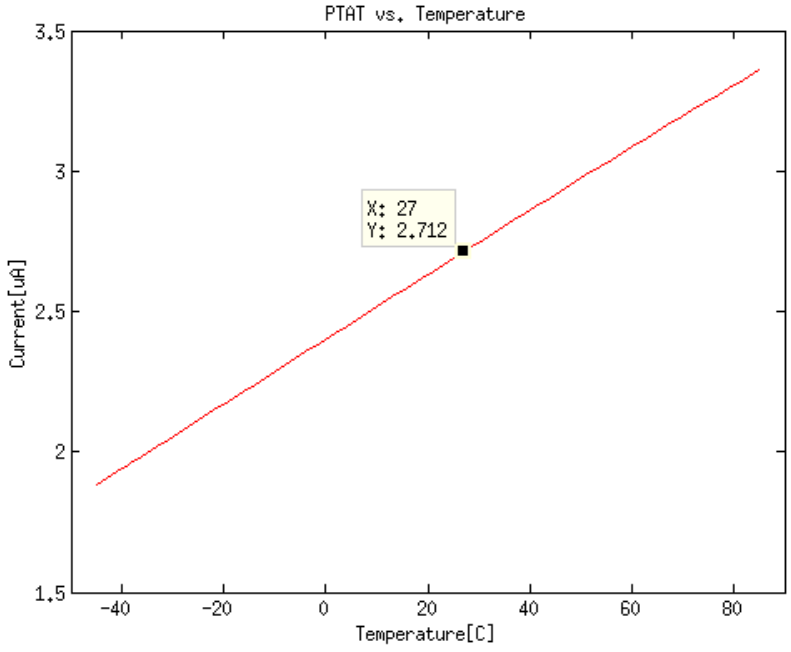

Figure 2.4 : PTAT Current vs. Temperature

Simulation results of PTAT current generator is given in the Figure 2.4 showing that generated PTAT current is $2.712uA$ at $27C$ matching with hand calculation and increasing with temperature as expected.

The value of temperature coefficient of the PTAT current is calculated as $8.838nA$ solving Equation (2.11) with design parameters $n = 8$ and $R_1 = 20000$.

$$\frac{d}{dT}Iptat \approx +0.085mV/C \cdot \frac{ln(8)}{20000} = 8.838 \cdot 10^{-9} \tag{2.13}$$

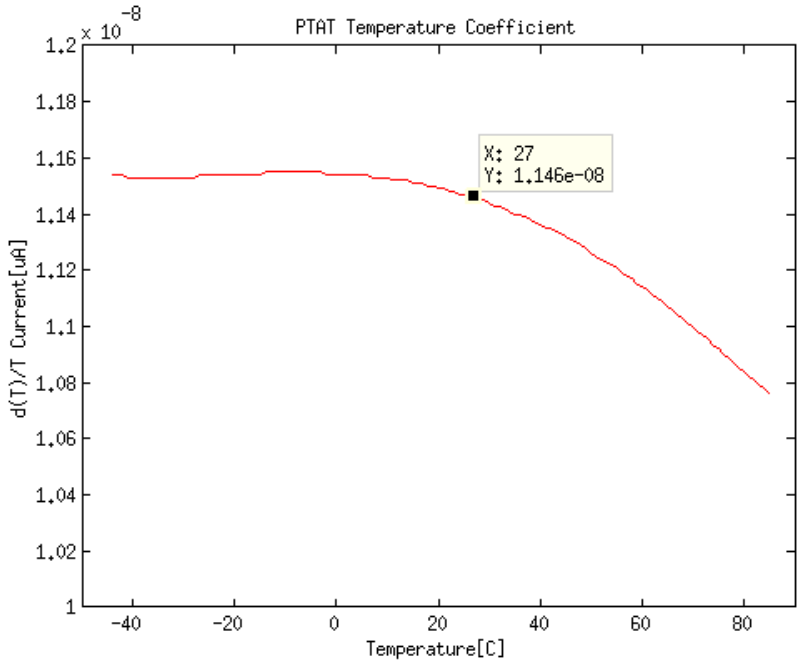

Figure 2.5 : PTAT Current Derivative vs. Temperature

Simulation results of PTAT current generator is given in the Figure 2.5 showing that the slope of current which is derivative of current respect to the temperature is about $11.46nA$. This value is higher than calculated value in Equation (2.13). and it is decreasing with temperature.

The difference between calculation and simulation result for temperature coefficient of PTAT current is the temperature coefficient of resistor and temperature coefficient of MOS devices which are neglected in calculation. It is expected that mismatch between calculation and simulation due to temperature coefficient of resistor will be eliminated by converting current into to the voltage in the following section.

2.1.2 PTAT current DAC and single to differential Circuit

Generated PTAT current is planned to be scaled by a DAC to have ability to change both value and temperature coefficient of PTAT current. In this work a current DAC, which is previously designed in the same process and also characterized with measurement, is used to scale I_{PTAT}. The schematic of the DAC is given in the Figure 2.6 (Ates, 2010).

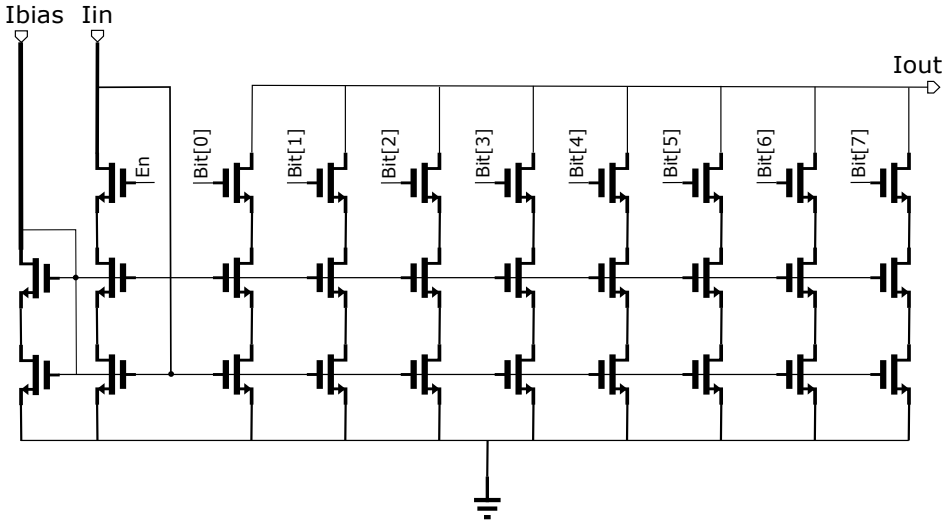

Figure 2.6 : PTAT Current DAC

DAC has 2 current inputs, Ibias and Iin, and 1 current output Iout. There are 8 bit binary control to scale Iout while a control signal En enables or disables the DAC. The relation between Iout and Iin is given in the Equation (2.14). Ibias is used for biasing the gate of cascode transistor of the current mirrors in each branch.

$$Iout = Iin \cdot K_{DAC} \tag{2.14}$$

where K_{DAC} is the gain of the DAC and given as the formula below.

$$K_{DAC} = \left(2^0 \cdot b_0 + 2^1 \cdot b_1 + 2^2 \cdot b_2 + 2^3 \cdot b_3 + 2^4 \cdot b_4 + 2^5 \cdot b_5 + 2^6 \cdot b_6 + 2^7 \cdot b_7\right) \tag{2.15}$$

PTAT current generated by the reference circuit is applied to the Iin while second PTAT current output of the reference circuit is applied to Ibias. If I_{PTAT} is replaced as Iin in the Equation (2.14), the new PTAT current $I_{PTATout}$ is defined as in the equation below.

$$I_{PTATout} = I_{PTAT} \cdot K_{DAC} \tag{2.16}$$

Gain of the current DAC K_{DAC} can take a value from 1 to 255. However only values in the range of 1 to 15 is used in the design due to higer values overload the voltage at the input of the sigma delta modulator which will be explained following sections. In the Figure 2.7 simulation result of the DAC is shown. $IPTAT_{out}$ is changing between 2.712uA and 40.77uA by 2.712uA steps.

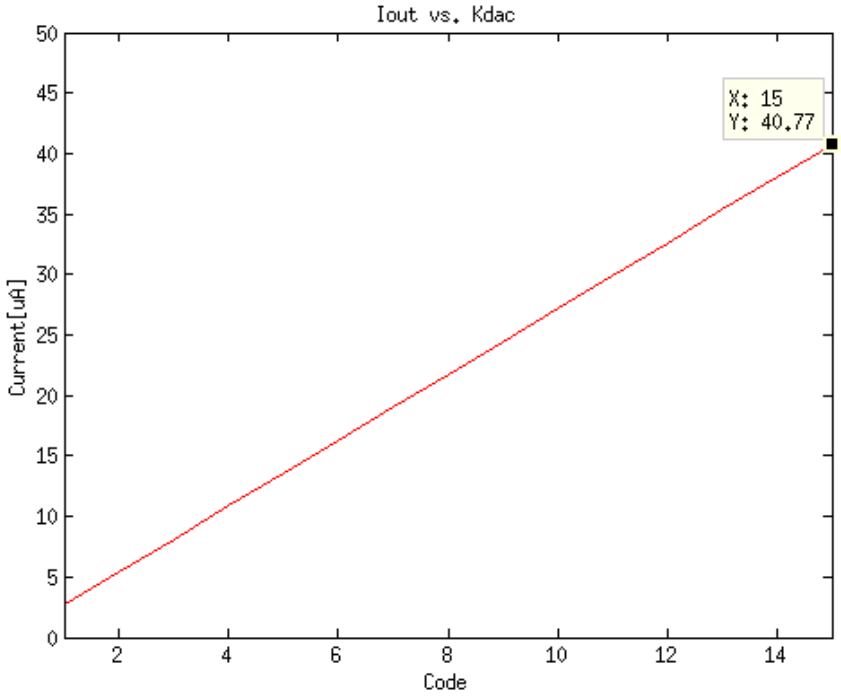

Figure 2.7 : Simulation Result of PTAT Current DAC

Finally $I_{PTATout}$ is converted to differential current to drive sigma delta modulator differentially. Differential conversion is done by cascode circuit mirrors where NMOS current mirror provide sink current while PMOS current mirror provide source current as shown in the Figure 2.8. The transistor size of the circuit is given in the Table 2.1.

Table 2.1 : Transistor Size of Single to Differential Circuit

MP1	20u/2u	MP2	20u/2u
MP3	20u/2u	MP4	20u/2u
MP5	20u/2u	MP6	20u/2u
MN1	10u/2u	MN2	10u/2u
MN3	10u/2u	MN4	10u/2u

The most critical performance metric of the single to differential circuit is the mismatch between Iout_p and Iout_n currents. Simulation result is given given in the Figure 2.9 while sweeping K_{DAC} value.

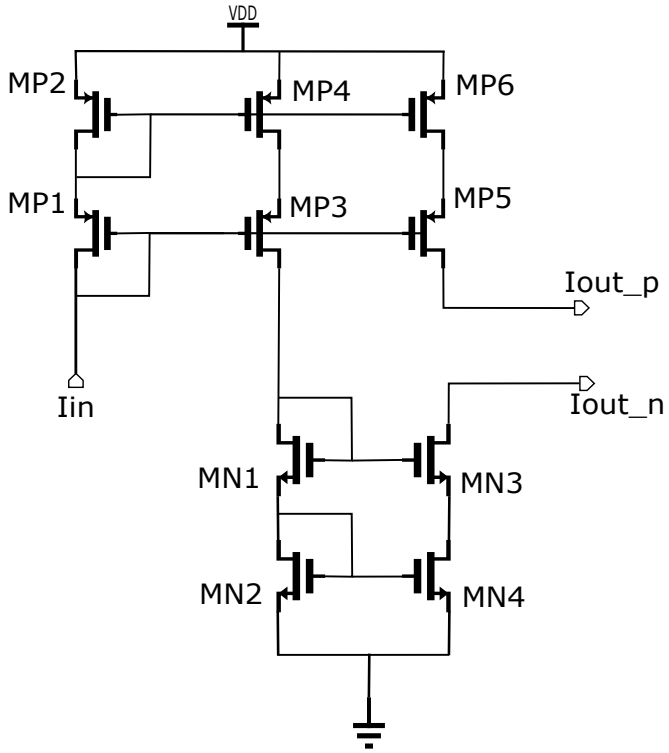

Figure 2.8 : Single to Differential Circuit

It is seen that error is in the pA range until $K_{DAC} = 10$ value and after this point error is increasing with K_{DAC} code value. However K_{DAC} value also increases the current absolute value so it would be better to examine the error as percentage error. Percentage error is given in the Figure 2.10 as ppm.

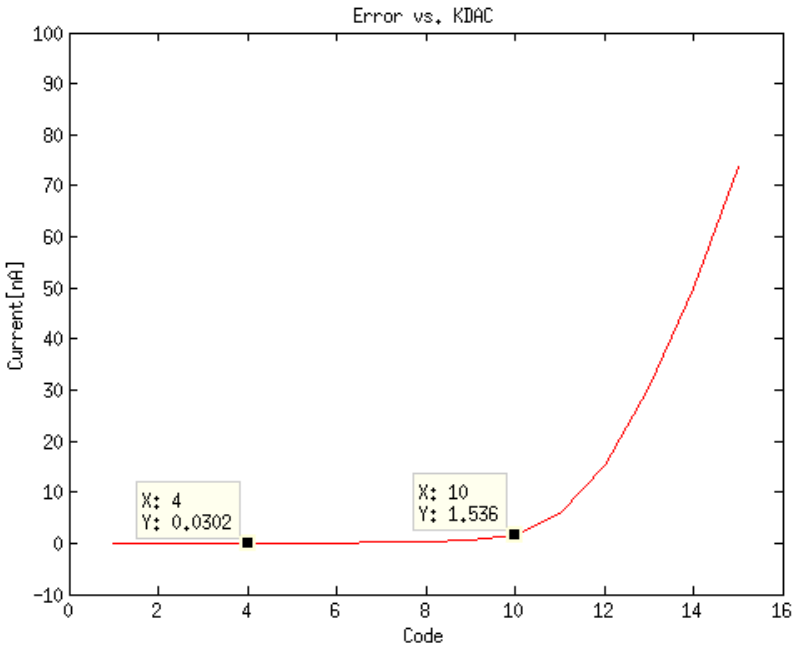

Figure 2.9 : Simulation Result of Single to Differential Circuit

Figure 2.10 shows that ppm error of the signal to differential circuit is in the range of a few ten ppm while it is increasing exponentially after value of $K_{DAC} = 10$.

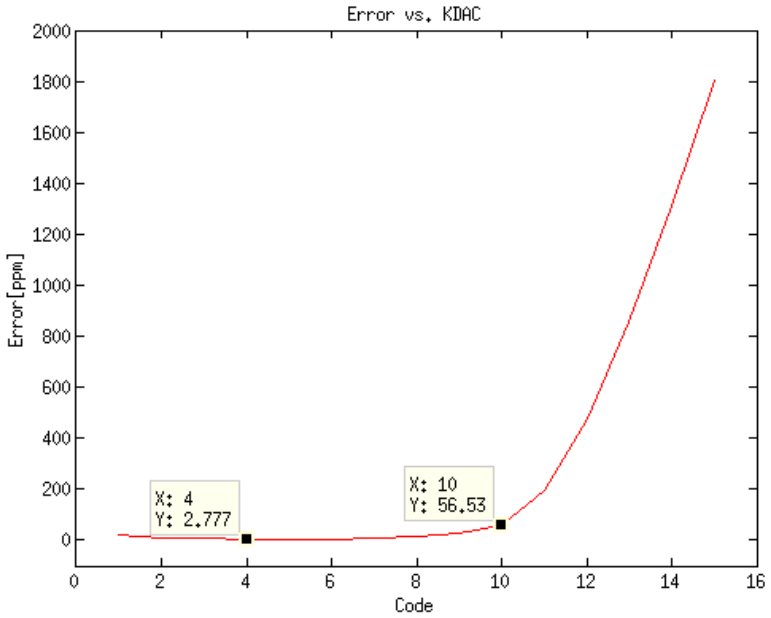

Figure 2.10 : Error vs K_{DAC} of Single to Differential Circuit

The other important simulation result is given in the Figure 2.11 which gives the ppm error of the signal to differential circuit respect to the absolute temperature. It is seen that ppm error is relatively stable over temperature and varies between 8ppm to 12 ppm in the temperature range of -40C to 85C.

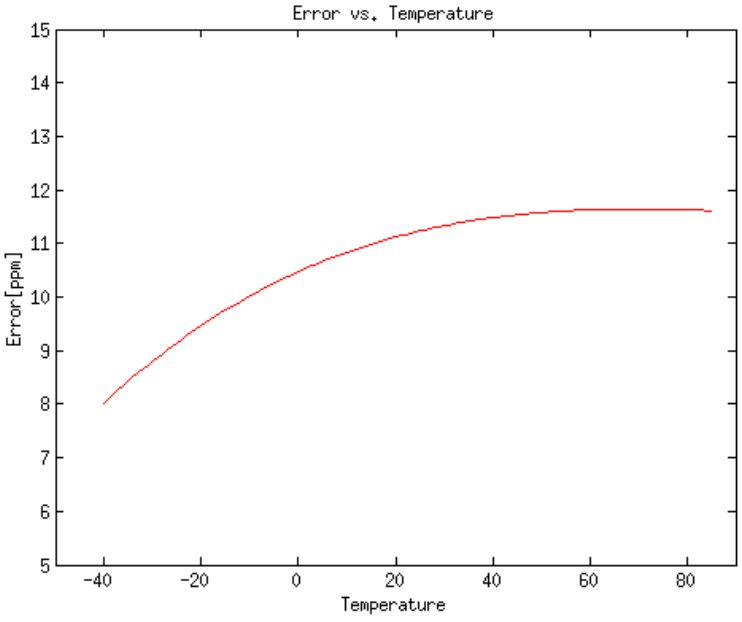

Figure 2.11 : Error vs Temperature of Single to Differential Circuit

2.1.3 PTAT voltage and modulator driver

In this section differential PTAT current is converted to PTAT voltage in order to drive sigma delta modulator The scheme seen in the Figure 2.12, modulator driver is used for this purpose. It is a fully differential operational amplifier in resistive negative feedback configuration. Driver has two inputs, positive IN_P and negative IN_M where differential current is applied and two outputs, positive VOUT_P and VOUT_M which drive modulator eventually.

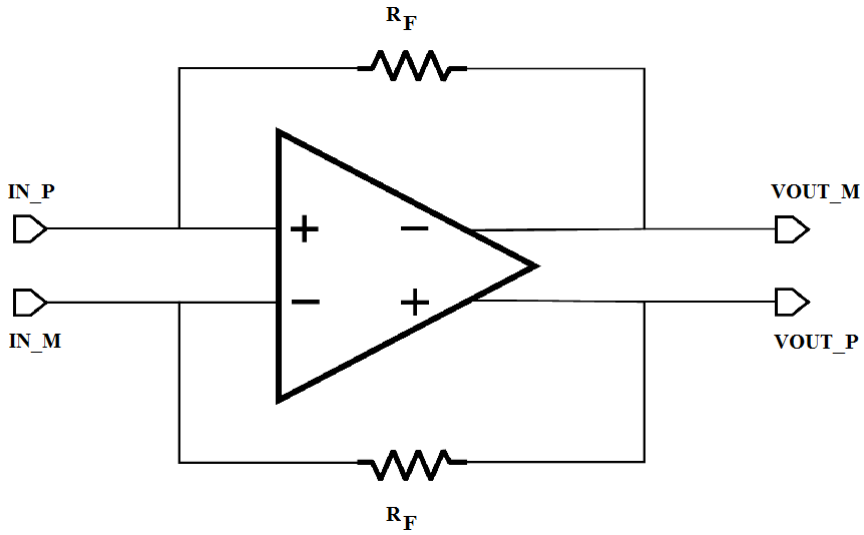

Figure 2.12 : Modulator Driver

Before giving schematic design details and simulation results it would be proper to give the function and the equation of the modulator. Transfer function of the circuit is expressed as the equation below where $V_{OUT} = VOUT\_P - VOUT\_M$ and $I_{IN} = IN\_P - IN\_M$.

$$V_{OUT} = I_{IN} \cdot R_F \tag{2.17}$$

If V_{OUT} is called V_{PTAT} and $I_{PTATout}$ is replaced as I_{IN};

$$V_{PTAT} = 2 \cdot I_{PTATout} \cdot R_F \tag{2.18}$$

voltage which is proportional to absolute temperature is expressed as in the Equation (2.18). Multiplier of 2 in the equation represents the single to differential circuit. To derive temperature coefficient of V_{PTAT}, Equation (2.18) is re-written using Equation (2.16) and Equation (2.6) to express the equation with design parameters.

$$V_{PTAT} = 2 \cdot \frac{V_t \cdot ln(n)}{R_1} \cdot K_{DAC} \cdot R_F \tag{2.19}$$

If R_F is chosen es equal to R_1;

$$V_{PTAT} = 2 \cdot \frac{V_t \cdot ln(n)}{R_1} \cdot K_{DAC} \cdot R_1 = 2 \cdot V_t \cdot ln(n) \cdot K_{DAC} \tag{2.20}$$

Finally if the derivative of V_{PTAT} is taken respect to the temperature, the temperature coefficient of the PTAT voltage is found as below.

$$\frac{d}{dT} V_{PTAT} = \frac{d}{dT} \left[2 \cdot \frac{V_t \cdot ln(n)}{R_1} \cdot K_{DAC} \cdot R_F \right] \tag{2.21}$$

The temperature coefficient of resistors cancel out each other regardless of their values. The ratio of resistors only contribute as a constant multiplier which is 1 in this case due to they are chosen as equal. As a result the only variable which changes with temperature is V_t and all other terms are just constant which scales the temperature coefficient of V_{PTAT}.

$$\frac{d}{dT} V_{PTAT} = \frac{d}{dT} V_t \left[2 \cdot ln(n) \cdot K_{DAC} \right] \tag{2.22}$$

It is clearly seen that temperature coefficient of resistor which is neglected in PTAT current equations is eliminated by converting current into voltage as previously mentioned.

The offset and low frequency noise of the opamp used in the modulator must be eliminated due to desired signal is at DC and any offset or noise at low frequency may distort the signal and degrade the performance of the system. In order to minimize eliminate low frequency flicker noise switched bias technique is implemented and chopper stabilization technique is used for move the offset and low frequency noise to higher frequency band.

In the following section switched bias and chopper stabilization technique is explained and simulation results of the modulator driver with and without chopper stabilization ar given.

2.1.3.1 1/f noise

Flicker noise, or 1/f noise is a noise whose power spectral density has the form in the Equation (2.23), where x typically is around 1. In most circuits, this means that white noise dominates above a certain frequency, and noise spectrum is obtained as in the Figure 2.13 (Schmid, 2008).

$$S(f) = S(1) \cdot \frac{1}{f^x} \tag{2.23}$$

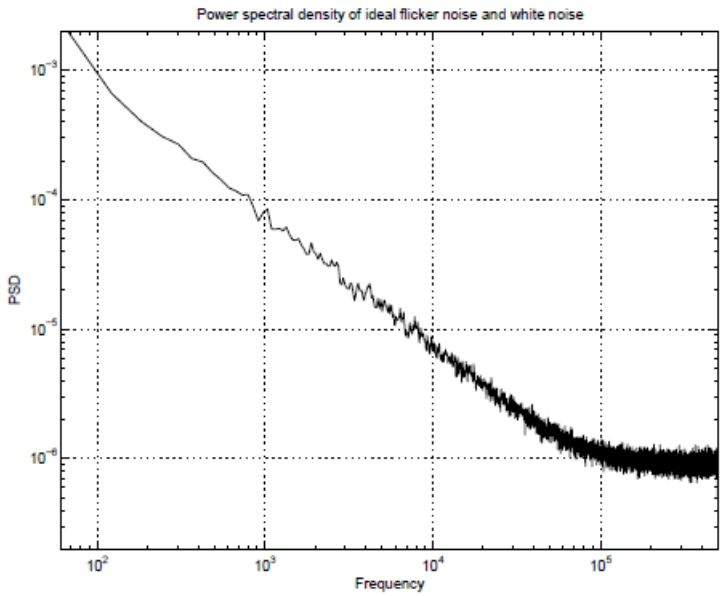

Figure 2.13 : Power Spectral Density of White Noise Overlaid by Flicker Noise

Almost every electronic device, vacuum tubes, resistors, diodes, BJTs and MOSFETs, has some flicker noise where the magnitude of flicker noise in MOSFETs is the largest due to there are several different effects causing flicker noise in electronic devices in general case with $1/f^x$ and $x \approx 1$. These effects can be divided into two which are volume effects and surface effects.

Volume effects are mainly Bremsstrahlung and carrier scattering. Bremsstrahlung is a German term used in quantum mechanics that roughly means deceleration radiation. Whenever an electron is accelerated, it will emit low-frequency Bremsstrahlung, and will be slowed down by its own Bremsstrahlung, as will other electrons in its vicinity. Thus it results haveing low-frequency energy and a cascade that remembers it, giving 1/f noise (Schmid, 2008).

The second volume effect is scattering, when electrons are scattered at the silicon lattice, or at impurities in the material, or by acoustical or optical phonons. In all cases, the scattering will interact with the lattice, generating phonons, which will later cause more scattering, and again it leads to have 1/f noise. This is the dominant source in most solid-state devices (Schmid, 2008).

The effect that dominates in MOSFETs, is something quite different which in MOSFETs, electrons tunnel from traps in the oxide to the gate and the conducting channel, and vice versa. If there is only one single trap which may happen in minimum size deep sub-micron transistors, then this causes a power spectral density of the drain current with a certain trap time constant τ (Schmid, 2008).

$$S(f) \approx \frac{\tau}{1+\omega^2\tau^2} \tag{2.24}$$

This is $1/f^2$ behaviour, as white noise fed through a one-pole low-pass filter would give, but due to the quantum nature of the electron trapping, this noise signal will only have two current levels. Such noise is called random telegraph noise. If there are several traps, it can be shown that the time constant for a trap at a distance z from the interface is for some process-dependent time constant τ_0, so if traps are uniformly distributed over z = 0. . .zg (Schmid, 2008).

$$\tau = \tau_0 \cdot exp\left(\frac{10^{10}}{m} \cdot z\right) \tag{2.25}$$

Equation (2.25) shows memories with time constants that are uniformly distributed over a logarithmic scale. Experiments with large scale excitation of MOSFETs, where part of the memory is deleted and therefore flicker noise is reduced intrinsically, show that flickering occurs even when the transistor is switched off completely. It can not be measured directly, however the effects caused by electron trapping: electrons tunnelling in and out of traps will cause both carrier number fluctuations and also fluctuations of the carrier mobility μ which in turn make the drain current of the MOSFET flicker can be measured. This is also reflected in one of the widely used simple flicker noise models of the MOSFET,

$$V_g^2 = \frac{K}{WLC_{ox}f} \tag{2.26}$$

where K and C_{ox} are technology parameters, and W and L the transistor dimensions: this formula does not depend on the bias conditions of the device, meaning it does not

depend on whether any current flows through the MOSFET (Schmid, 2008).

Considering all these information about flicker noise, three techniques can be implemented to minimize or eliminate flicker noise.

- Flicker noise which is caused by memory can be minimized by resetting memory. This is known as large signal excitation (LSE).
- Flicker noise has a flat auto correlation function, and it can be removed by subtracting two correlated samples. This is known as correlated double sampling (CDS).
- Flicker noise is dominant in the low frequencies, so it can be modulated into a frequency band outside the signal band. This technique is known as chopping.

In this work two of these three techniques, LSE and chopping are implemented to minimize and eliminate flicker noise and offset.

2.1.3.2 Bias switching and large-scale excitation (LSE)

Figure 2.14 shows a switched current source. If this circuit is operated with a variable-duty-cycle clock CLK and its inverse CLKB, then the current can be tuned by a factor of two. It has been observed that for duty cycles between 0% and 100%, this circuit is much less noisy than the circuit simulator predicts. The reason for this is that switching a transistor off deletes some of its flickering memory by kicking some of the trapped electrons out of their traps (Schmid, 2008).

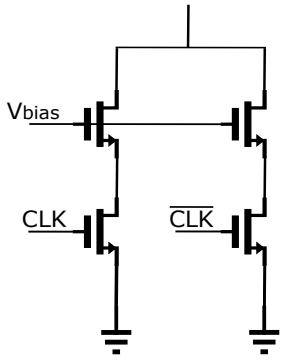

Figure 2.14 : Switched Current Source

Figure 2.15 shows another Matlab simulation in which the memory of the flicker noise is deleted almost completely once every 10 us. The flicker noise disappears almost completely in this example; normally, some flicker noise remains at low frequencies because it is not possible to delete all of the memory. This effect can be calculated, but not simulated; there is as yet no circuit simulator that takes flicker noise memory effects into account (Schmid, 2008).

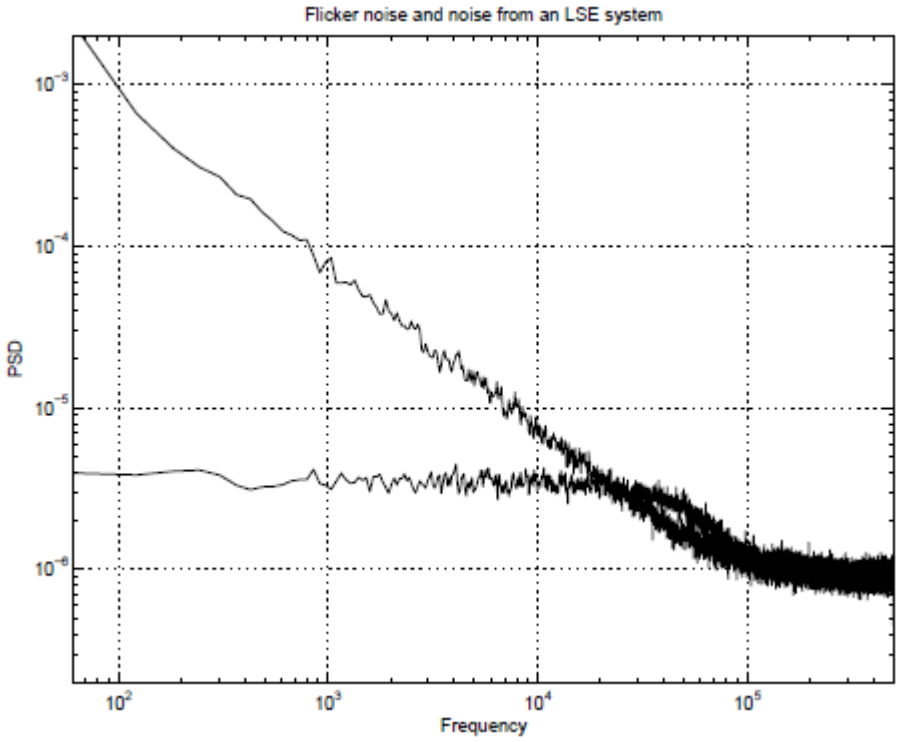

Figure 2.15 : PSD of Switched Current Source

In this work bias transistors are switched with a 500KHz clock which has a 50% duty cycle. This means flicker noise memory is deleted every 2us and PSD is expected to be flat until 500KHz.

2.1.3.3 Chopper amplifier

A chopper amplifier system is shown in the Figure 2.16 (Toth & Tsividis, 2003). As seen in the scheme on one phase of the clock signal, input signals VIN_P and VIN_M are applied to positive input and negative input of the amplifier respectively while output signals VOUT_M and VOUT_P are connected negative and positive output of the amplifier. On the other phase of the clock signal both input and output signals are inverted. VIN_P signal is applied to negative input of the amplifier and VIN_M signal is applied to positive input amplifier. To keep polarity the same, positive output of the amplifier is connected to VOUT_M and negative output of the amplifier is connected to VOUT_P signal.

This operation means modulation on the input and the output signals with chopper frequency. The input is modulated by a square wave before the amplifier which move the signal spectrum across the chopper frequency. The spectrum at the output of the amplifier contains the both offset and low frequency noise especially $1/f$ noise.

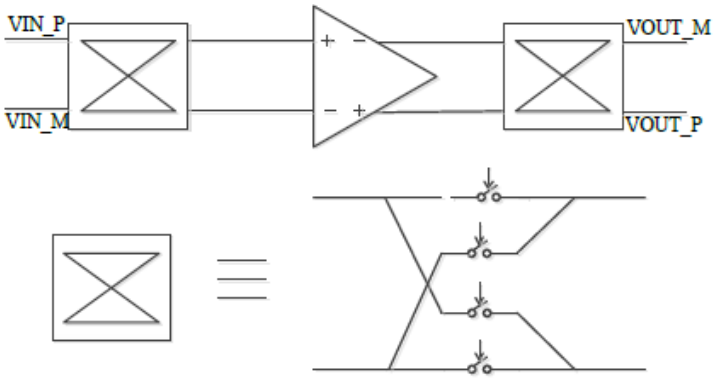

Figure 2.16 : Chopper Amplifier

Second modulation at the output brings the signal spectrum back to the original position and moves the offset and the noise to a chopper frequency (Maloberti, 2007). Frequency response of a chopper amplifier is given in the Figure 2.17.

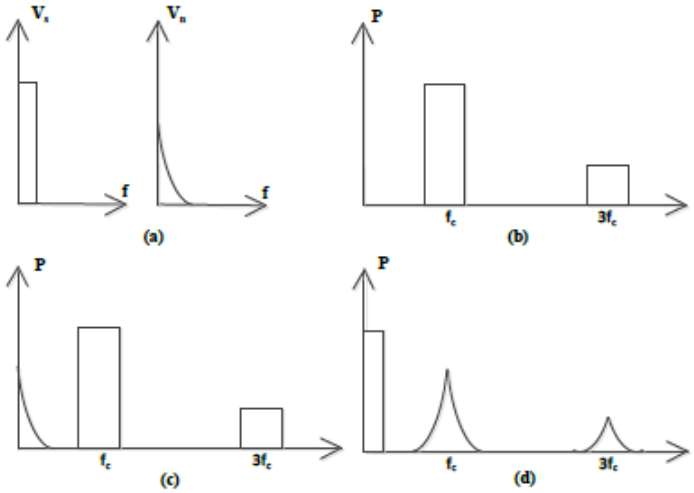

Figure 2.17 : Frequency Response of a Chopper Amplifier

The designed chopper amplifier schematic is given in the Figure 2.18 and the values of the components are given in the Table 2.2.

Table 2.2 : Transistor Size of Chopper Amplifier

MN1	10u/1u	MP10	120u/1u	MN19	10u/0.35u	MP28	240u/1u
MN2	10u/1u	MN11	30u/1u	MN20	10u/0.35u	MP29	240u/1u
MN3	10u/1u	MN12	30u/1u	MN21	10u/0.35u	MP30	240u/1u
MN4	10u/1u	MN13	30u/1u	MN22	10u/0.35u	R1	30K
MP5	20u/1u	MN14	30u/1u	MN23	120u/1u	R2	30K
MP6	20u/1u	MN15	30u/1u	MN24	120u/1u	R3	100K
MP7	50u/1u	MN16	30u/1u	MN25	120u/1u	R4	100K
MP8	50u/1u	MN17	30u/1u	MN26	120u/1u	Rc	1K
MP9	120u/1u	MN18	30u/1u	MP27	240u/1u	Cc	1p

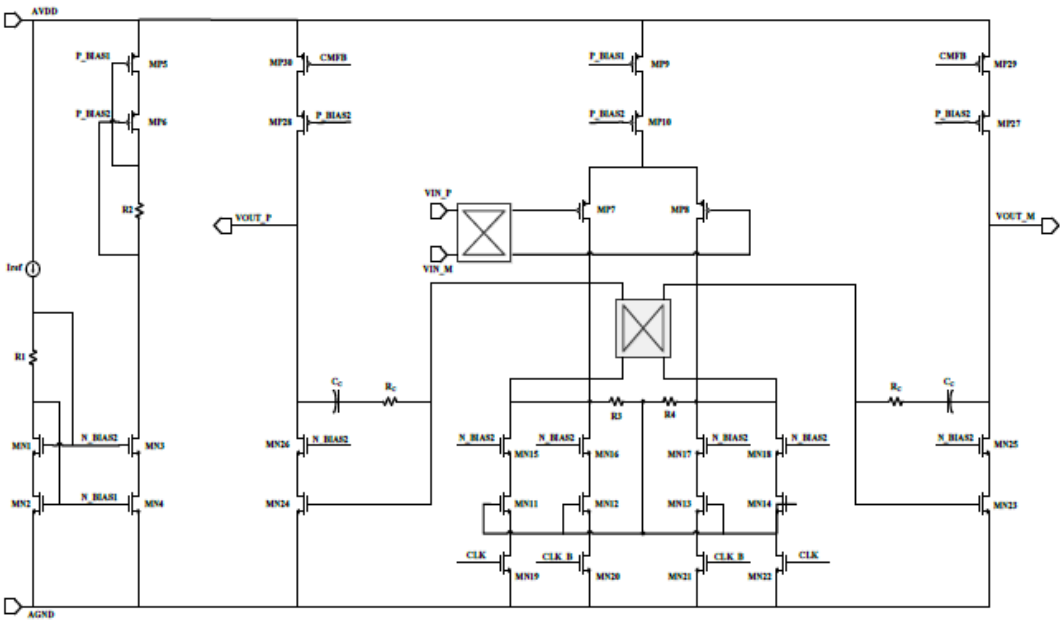

Figure 2.18 : Designed Chopper Amplifier

Common mode feedback is done by a switched capacitor common mode feedback circuit which is given in the Figure 2.19 where $C_S = 200fF$ and $C_F = 100fF$. Switches are designed as a transmission gate which is shown in the Figure 2.20 where the size of NMOS transistor is 2u/0.5u and size of PMOS transistor is 5u/0.5u.

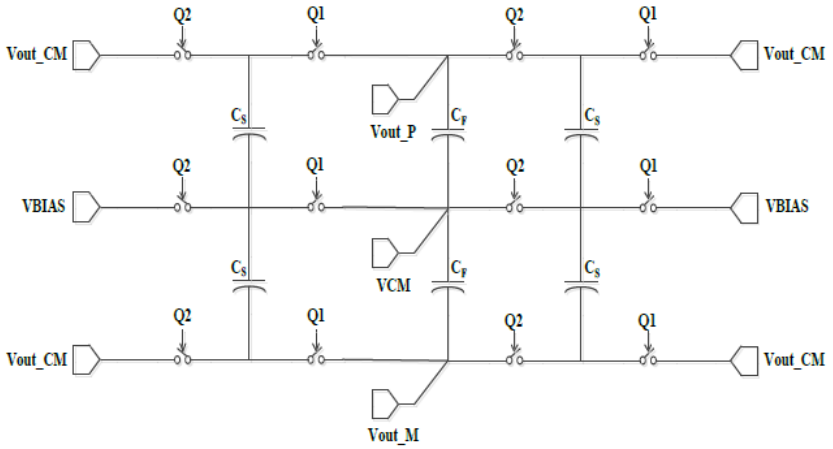

Figure 2.19 : Switched Capacitor Common Mode Feedback Circuit

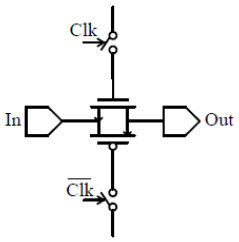

Figure 2.20 : Transmission Gate

Frequency response of chopper amplifier is shown in the Figure 2.21 when 10mV DC offset is applied with 750 Hz sinusoidal signal to the input of the amplifier. As seen in the PSD results, when chopper is disable there is a DC content with a power of -40dB which is 10mV. When chopper is enabled power of DC offset is scaled down by 60dB to -100dB which verifies the chopper stabilization technique is working.

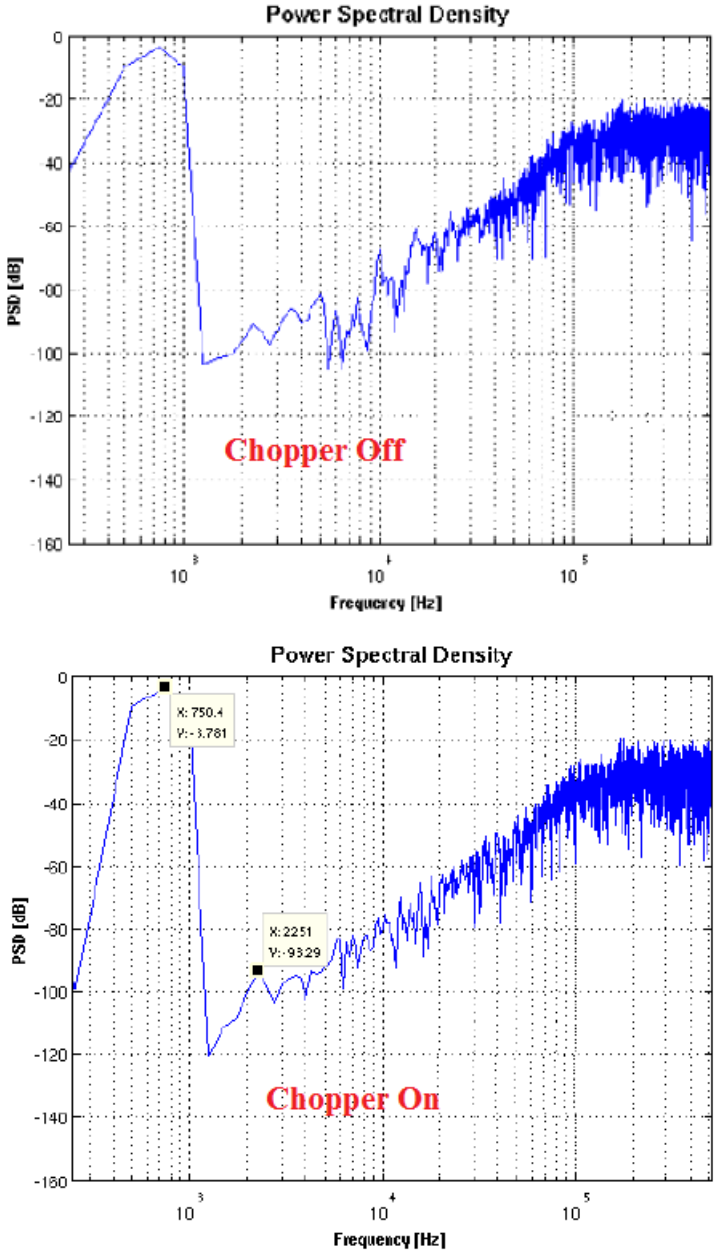

Figure 2.21 : PSD with Chopper Off and On

In the Figure 2.22 simulation result of V_{PTAT} voltage is given respect to temperature for the values of $K_{DAC} = 4$ and $K_{DAC} = 10$ when chopper stabilization is disabled.
In the Figure 2.23 simulation result of V_{PTAT} voltage is given respect to temperature

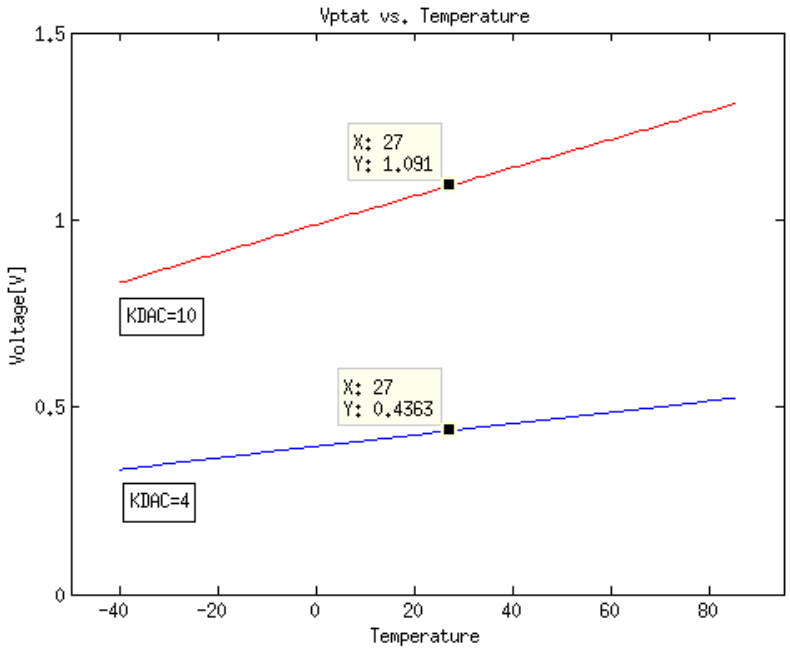

Figure 2.22 : V_{PTAT} vs. Temperature (Chopper Disabled)

for the values of $K_{DAC} = 4$ and $K_{DAC} = 10$ when chopper stabilization is disabled.

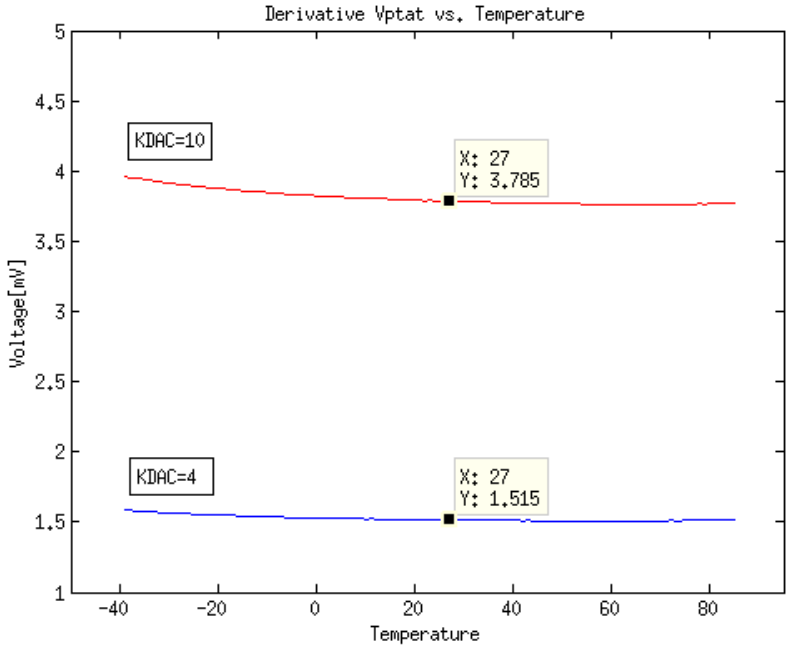

Figure 2.23 : Derivative V_{PTAT} vs. Temperature (Chopper Disabled)

Simulation results verify successful conversion from temperature to analog voltage. In the following section method and design of digital presentation of temperature information is given and explained.

2.1.4 Analog switched capacitor sigma delta modulator

Temperature information is converted to analog voltage in previous sections. In this section analog voltage is converted to digital signal by using a second order switched capacitor sigma delta modulator which is designed in the work (Ozdemir, 2012).
In the following subsections a brief introduction will be given about sigma delta modulators. Then chosen sigma delta modulator type will be explained and finally simulation results of sigma delta modulator will be presented.

2.1.4.1 Introduction to sigma delta modulators

The Figure 2.24(a) performs integration (sigma) of the difference (delta) the modulator. Thus it is named sigma delta $(\Sigma\Delta)$ modulator. Due to it uses only one integrator in the loop the modulator shown in the Figure 2.24(b) is a first order $\Sigma\Delta$ modulator (Maloberti, 2007).

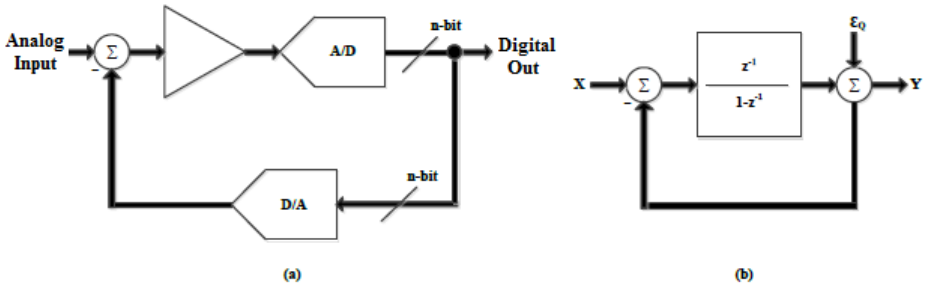

Figure 2.24 : Sigma Delta Modulator a) Block Diagram b) Linear Model

2.1.4.2 First order sigma delta modulator and noise shaping

If the quantizer is put in a feedback loop as shown in the Figure 2.25, the noise reduction in the desired band is enhanced which also called noise shaping. The linear model represents the quantization error with the additive noise ε_Q that is a second input of the circuit (Maloberti, 2007).
The transfer function of the block diagram in the Figure 2.25 is given below.

$$Y = [X - Y \cdot B(z)]A(z) + \varepsilon_Q \tag{2.27}$$

If the equation is rearranged it leads to;

$$Y = \frac{X \cdot A(z)}{1 + A(z)B(z)} + \frac{\varepsilon_Q}{1 + A(z)B(z)} \tag{2.28}$$

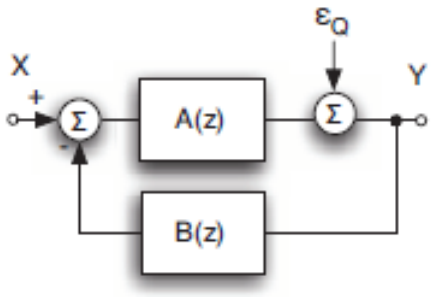

Figure 2.25 : Feedback

Equation (2.28) shows that signal and quantization noise pass through two different transfer functions which are signal transfer $(S(z))$ function and noise transfer function $(N(z))$. To obtain noise shaping, S(z) must be low pass and N(z) must be high pass (Maloberti, 2007).

$$Y = X \cdot S(z) + \varepsilon_Q \cdot N(z) \tag{2.29}$$

As seen in the Figure 2.24(b) in the forward path, first order sigma delta modulator has the transfer function which is given below.

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.30}$$

In the feedback path modulator has transfer function of 1 due to it is in unity feedback configuration. If the Equation (2.30) is rewritten for $A(z) = H(z)$ and $B(z) = 1$;

$$Y(z) = [X(z) - Y(z)] \frac{z^{-1}}{1 - z^{-1}} + \varepsilon_Q(z) \tag{2.31}$$

If the Equation (2.31) is rearranged;

$$Y(z) = X(z) \cdot z^{-1} + \varepsilon_Q(z) \left(1 - z^{-1}\right) \tag{2.32}$$

The Equation (2.32) shows that the signal is just delayed by one clock period and the noise is passed through $\left(1 - z^{-1}\right)$. This means that the signal and the quantization noise are processed differently, signal passes through the signal transfer function $STF(z)$ and the quantization noise through the the noise transfer function $NTF(z)$, by the modulator (Maloberti, 2007).

$$Y(z) = X \cdot STF(z) + \varepsilon_Q(z) \cdot NTF(z) \tag{2.33}$$

The noise transfer function of the first order ΣΔ is high-pass as is evident by its estimation on the unity circle: $z \rightarrow e^{j\omega T}$ (Maloberti, 2007).

$$NTF(\omega) = 1 - e^{j\omega T} = 2je^{-j\omega T/2}\frac{e^{j\omega T/2} - e^{-j\omega T/2}}{2j} \qquad \textbf{(2.34)}$$
$$NTF(\omega) = 2je^{-j\omega T/2}sin(\omega T/2)$$

The result shows that the white spectrum of the quantization noise is amplified by 4 but is shaped by $sin^2(\omega T/2)$ giving rise to a significant attenuation of the low-frequency components of the spectrum. This results to first order ΣΔ modulator to have the signal to noise ratio (SNR) equation given below (Maloberti, 2007).

$$SNR_{\Sigma\Delta,1} = 6.02 \cdot n' - 3.39 + 9.03 \cdot log_2(OSR) \qquad \textbf{(2.35)}$$

First order ΣΔ modulator benefits an SNR improvement of 9.03 dB for every doubling of the oversampling ratio which means every doubling of the sampling frequency improves the ENOB by 1.5-bit (Maloberti, 2007). PSD result of a ideal first order sigma delta modulator is shown in the Figure 2.26 (Malcovati et al., 2003).

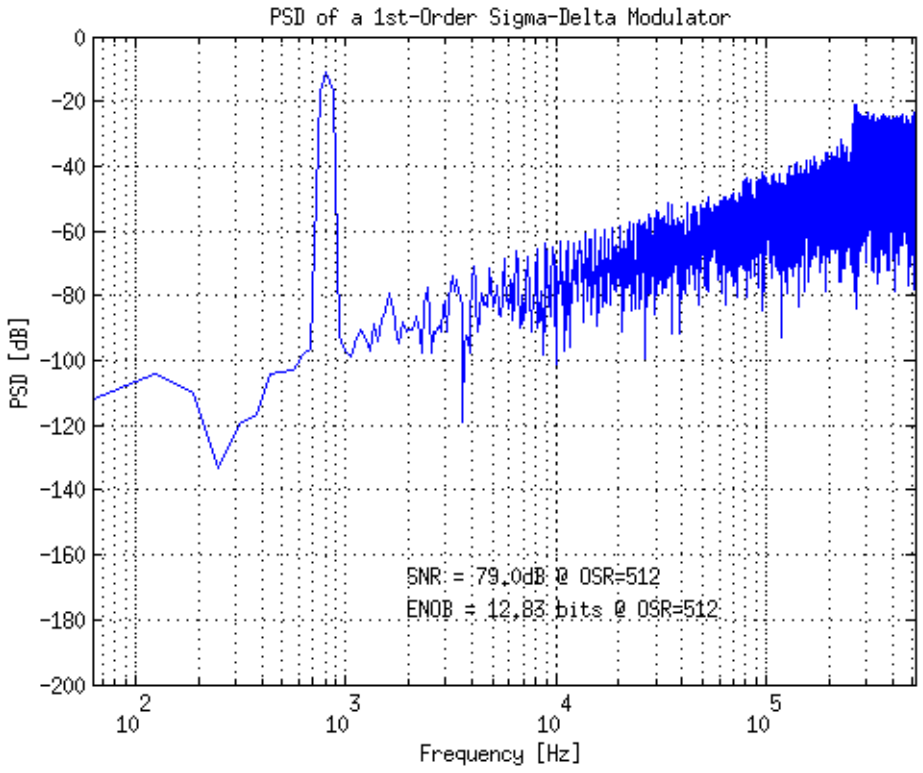

Figure 2.26 : PSD Result of First Order Sigma Delta

As seen in the figure noise shaping is $20dB/Decade$ indicating first order behaviour. Example uses OSR as 512 and the extra bit n' as 0 which means single bit quantizer. If Equation (2.35) is solved for these values, SNR is calculated as 77.88 dB.

$$SNR_{\Sigma\Delta,1} = 6.02 \cdot 0 - 3.39 + 9.03 \cdot log_2(512) = 77.88 \quad \textbf{(2.36)}$$

In the next section second order $\Sigma\Delta$ is examined as examined in this section by its noise shaping behaviour and SNR improvements.

2.1.4.3 Second order sigma delta modulator and noise shaping

Additional second integrator to the loop forms a second order modulator as shown in the Figure 2.27 to ac hive better performance and features (Maloberti, 2007).

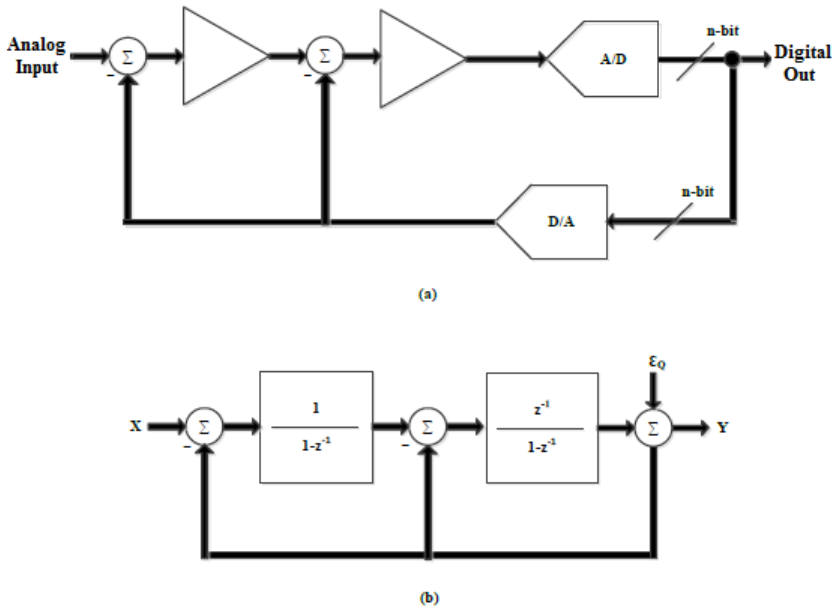

Figure 2.27 : Second Order Sigma Delta Modulator a) Block Diagram b) Linear Model

The transfer function of the linear model of second order $\Sigma\Delta$ shown in the Figure 2.27 is given in the Equation (2.37).

$$Y(z) = \left\{ [X(z) - Y(z)] \frac{1}{1 - z^{-1}} - Y(z) \right\} \frac{z^{-1}}{1 - z^{-1}} + \varepsilon_Q(z) \quad \textbf{(2.37)}$$

If the equation is rearranged;

$$Y(z) = X(z) \cdot z^{-1} + \varepsilon_Q(z) \left(1 - z^{-1}\right)^2 \quad \textbf{(2.38)}$$

The Equation (2.38) shows that the signal transfer function again is just a delay line in the first order ΣΔ modulator and the noise transfer function is $(1-z^{-1})^2$, the square of the result of first order ΣΔ modulator. If noise transfer function S(z) and SNR equation is written for second order ΣΔ modulator, Equation (2.39) and (2.40) are obtained (Maloberti, 2007).

$$NTF(\omega) = (1-e^{j\omega T})^2 = -4e^{-j\omega T}\{sin(\omega T/2)\}^2 \quad \textbf{(2.39)}$$

$$SNR_{\Sigma\Delta,2} = 6.02 \cdot n' - 11.12 + 15.05 \cdot log_2(OSR) \quad \textbf{(2.40)}$$

Second order ΣΔ benefits an SNR improvement of 15.05 dB for every doubling of the oversampling ratio which means every doubling of the sampling frequency improves the ENOB by 2.5-bit (Maloberti, 2007). PSD result of a ideal second order sigma delta modulator is shown in the Figure 2.28 (Malcovati et al., 2003).

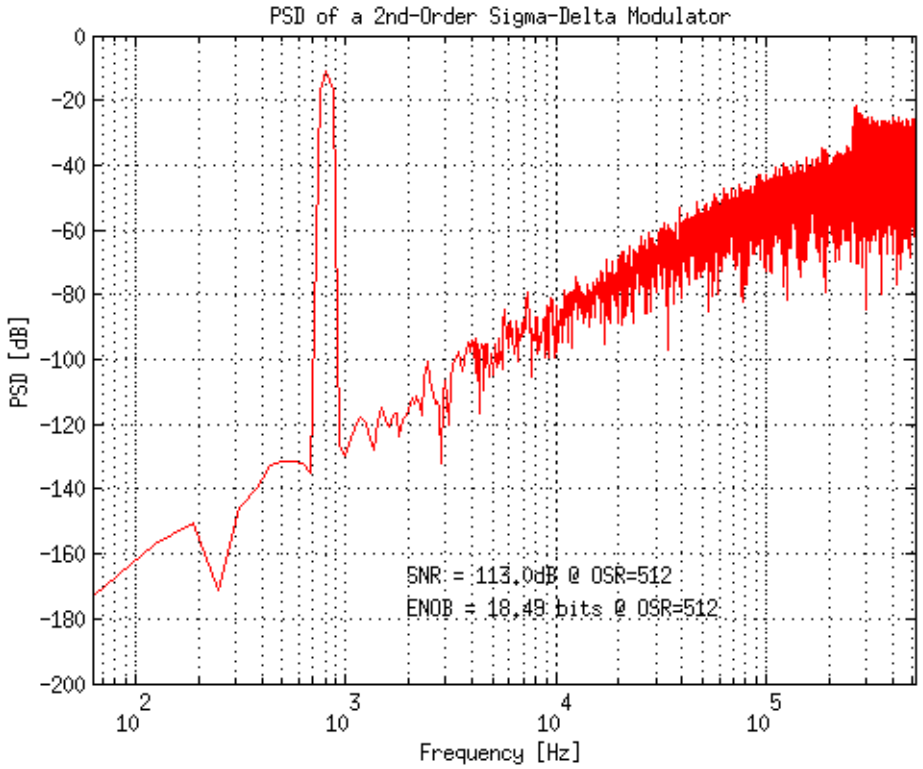

Figure 2.28 : PSD Result of Second Order Sigma Delta

As seen in the figure noise shaping is $40dB/Decade$ indicating second order behaviour. In the example OSR value is 512 and the extra bit n' is 0. Equation (2.40) is solved for these values.

$$SNR_{\Sigma\Delta,2} = 6.02 \cdot 0 - 11.12 + 15.05 \cdot log_2(512) = 124.33 \quad \textbf{(2.41)}$$

Ideal simulation results SNR value as 113.0 while calculation results SNR value as 124.33. The SNR mismatch of 11.33 dB between calculation and simulation is amplitude of the input signal and system non-idelaities where calculation assumes signal is 1V (full scale) while simulation use half of it which leads 6 dB difference. Th remaining part of the mismatch is coming from the system non-idealities including in the Matlab-Simulink model(Malcovati et al., 2003).

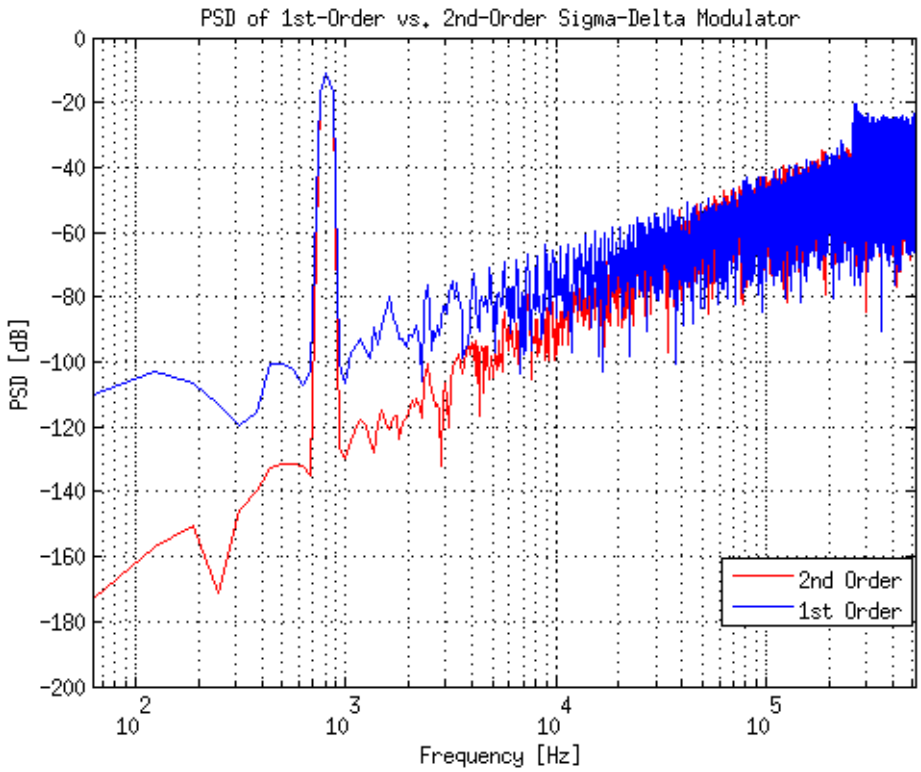

Figure 2.29 : PSD Result of First vs. Second Order Sigma Delta

As seen in the Figure 2.29 second order sigma delta modulator has much stronger noise shaping feature than first order sigma delta modulator which enables high SNR and ENOB values with the same operating frequency but with power and area penalty. In this work second order sigma delta modulator is chosen in order to achieve high SNR value which also leads higher resolution. In the following section chosen second order sigma delta topology is presented and explained.

2.1.4.4 Boser-Wooley type second order sigma delta modulator

The signal range required at the outputs of the two integrators is several times the full scale analog input range. This requirement creates a serious problem in circuit topologies, especially CMOS technology, where the dynamic range is limited (Wooley, 1988).

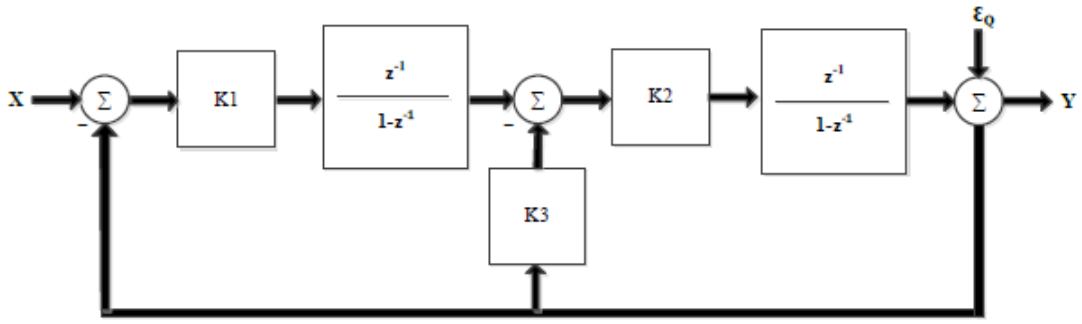

Figure 2.30 : Boser-Wooley Type Second Order Sigma Delta Modulator

The architecture shown in the Figure 2.30 requires smaller signal range within integrators. The architecture also differs from conventional configuration with two delay is included in both integrators, thus simplifying the implementation with straightforward sampled-data analog circuits (Wooley, 1988). The transfer function of the modulator seen in the Figure 2.30 is given in the equation (2.42).

$$Y(z) = \left\{ [X(z) - Y(z)]K1 \left(\frac{z^{-1}}{1-z^{-1}} \right) - Y(z)K3 \right\} K2 \left(\frac{z^{-1}}{1-z^{-1}} \right) + \varepsilon_Q(z) \qquad \textbf{(2.42)}$$

If the coefficients K1, K2 and K3 are chosen as 0.5, 2 and 1 respectively the transfer function becomes as indicated in the Equation (2.43). This means there is an attenuation of 0.5 at the input of first integrator and gain of 2 at the input of the second integrator. However gain of 2 at the input of the second integrator is not a problem due to it is followed by a single bit quantizer (Wooley, 1988).

$$Y(z) \left[1 + \left(\frac{z^{-1}}{1-z^{-1}} \right)^2 + 2 \left(\frac{z^{-1}}{1-z^{-1}} \right) \right] = \varepsilon_Q(z) + X(z) \left(\frac{z^{-1}}{1-z^{-1}} \right)^2 \qquad \textbf{(2.43)}$$

since

$$1 + \left(\frac{z^{-1}}{1-z^{-1}} \right)^2 + 2 \left(\frac{z^{-1}}{1-z^{-1}} \right) = \left(\frac{1}{1-z^{-1}} \right)^2 \qquad \textbf{(2.44)}$$

transfer function of the Booser - Wooley type second order ΣΔ modulator is found as equation below.

$$Y(z) = X(z) \cdot z^{-2} + \varepsilon_Q(z)\left(1 - z^{-1}\right)^2 \tag{2.45}$$

Booser - Wooley type second order ΣΔ modulator has the same transfer function except the signal is delayed two clock cycles compare to one clock cycle in the traditional second order ΣΔ modulator.

Implemented design (Ozdemir, 2012) is shown in the Figure 2.31. The design differs from the architecture in the Figure 2.30 by no attenuation at the input of second integrator. The first integrator is also chopper stabilized with chopper frequency of $500KHz$ which is half of the system clock $1MHz$.

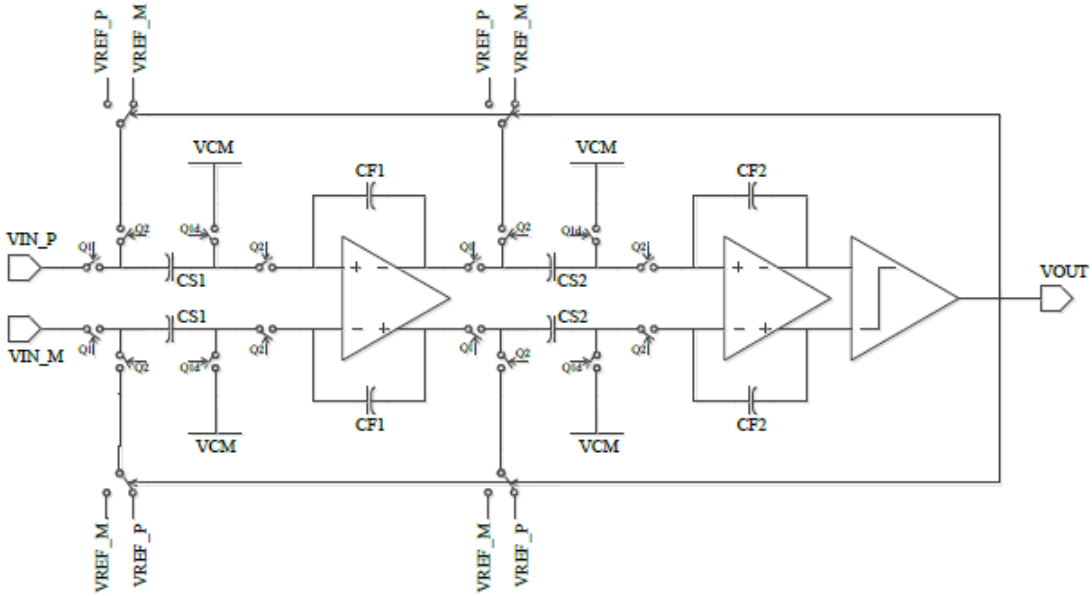

Figure 2.31 : Designed Second Order Sigma Delta Modulator

Table 2.3 : Sigma Delta Modulator Performance Metrics

Performance Metric	Value
Supply Voltage	3.3V
Power Consumption	5mW
SNR	107.6dB
SFDR	92.5dB
DR	1.5V

In the thesis (Ozdemir, 2012) there can be found more detailed design consideration and simulation results for both sub blocks and sigma delta modulator itself while Table

2.4 and Table 2.3 summarizes system parameters and performance metrics of designed second order ΣΔ modulator.

Table 2.4 : Sigma Delta Modulator System Parameters

Parameter	Value	Description
VCM	1.65V	Common Mode Voltage Reference
VREF_P	2.4V	Positive Reference Voltage
VREF_M	0.9V	Negative Reference Voltage
VIN_P	(0.9V,2.4V)	Positive Analog Input Voltage
VIN_M	(0.9V,2.4V)	Negative Analog Input Voltage
CS1	250fF	Sampling Capacitor of First Integrator
CF1	500fF	Feedback Capacitor of First Integrator
CS2	250fF	Sampling Capacitor of Second Integrator
CF2	250fF	Feedback Capacitor of Second Integrator
CLK	1MHz	Modulator Operating Clock Frequency

Figure 2.32 shows the PSD of the designed ΣΔ modulator for 750.4Hz sinusoidal input signal which has an amplitude of 1V. SNDR and ENOB are found as 107.6dB and 17.59 respectively for 2KHz bandwidth at 1.024MHz clock frequency means $OSR = 512$ (Ozdemir, 2012).

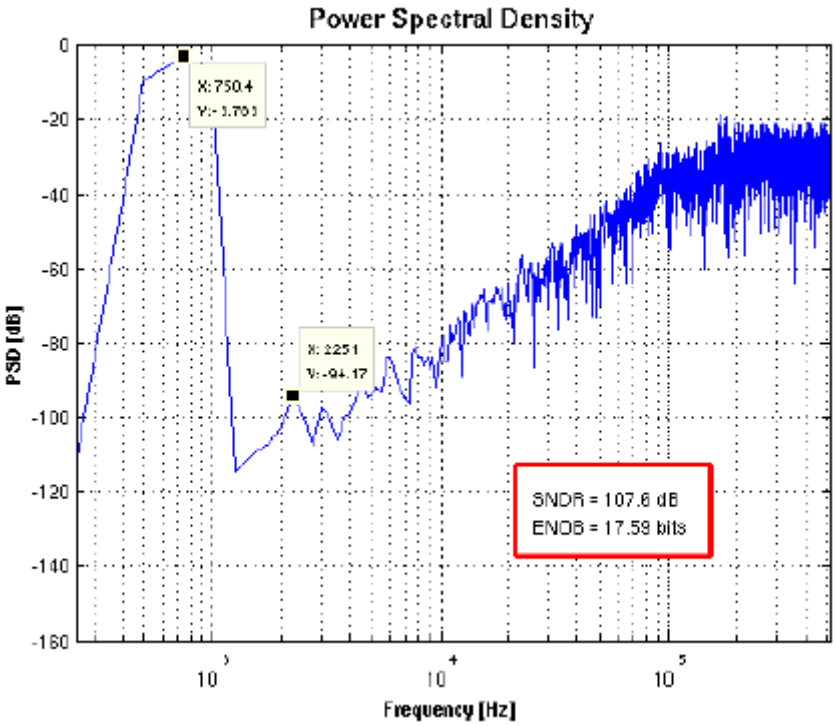

Figure 2.32 : PSD Result of Sigma Delta Modulator

2.1.5 Digital core

Main purpose of the digital core is to set internal bits. It has a 48 bit memory made of 48 D type flip flops. The data stored in the memory can be read and written with I2C protocol or 8 bit standard parallel input/output pins controlled with 3 bit address bus. The memory has also a preset value given in the Table 2.6. The memory can be read and written by I2C bus, the data input, address input and clock input is determined by I2C. Detailed representation of the digital core is shown in the Figure 2.33.

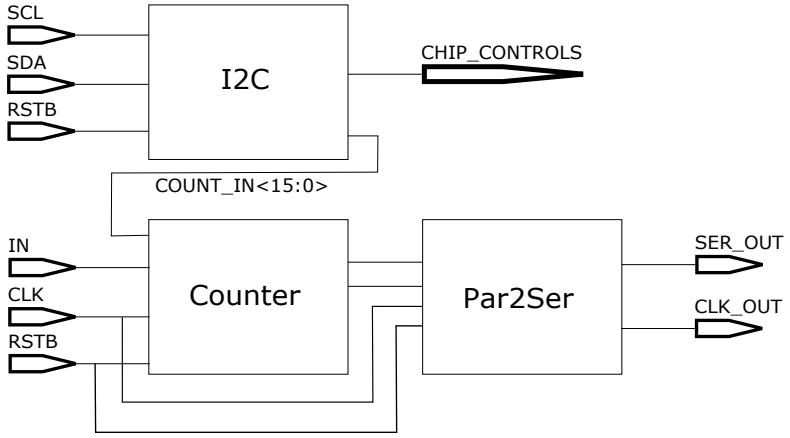

Figure 2.33 : Digital Core

In the following sections a brief summary of I2C protocol is given along with a typical I2C controlled memory.

2.1.5.1 I2C protocol

I2C is a serial data interface developed by Philips. Its main purpose is to reduce the pin count for communications between ICs. It has two pins, one for data and one for clock, namely SDA and SCL. Since there is only one data line, communication is half duplex, with a master telling a slave what to do. For this purpose, there are four possible roles in an I2C communication (Philips, 1995).

- 1. Master Transmitter: Transmit unique chip address, data, read or write command
- 2. Master Receiver: Receives data requested from slave
- 3. Slave Transmitter: Transmit data requested by master
- 4. Slave Receiver: Receives unique chip address, data, read or write command

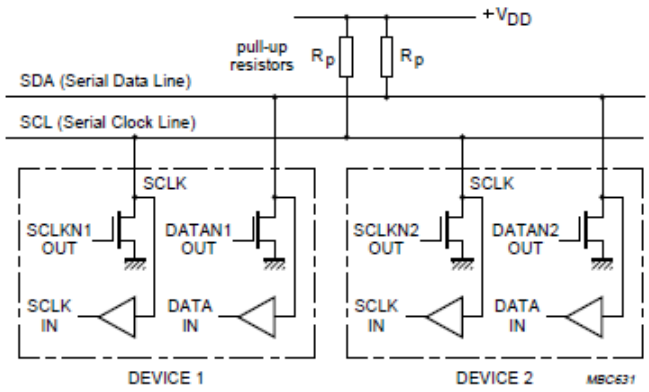

Figure 2.34 : CMOS I2C I/O Schematics

As shown in the Figure 2.34, SDA line is a pull-up line, driven by pull-down outputs of chips connected. When one chip is transferring the data, all other chips should release the data line for proper operation (Philips, 1995).

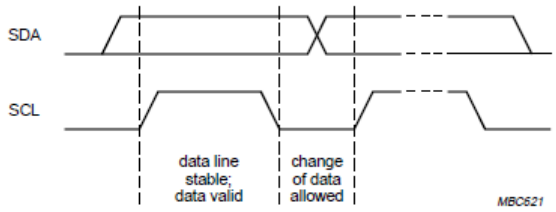

Figure 2.35 : Bit Transfer on I2C Bus

For a data to be valid, SDA should be constant during high phase of SCL as shown in the Figure 2.35. Falling edge of SDA during high phase of SCL corresponds to START condition, whereas rising edge corresponds to STOP condition. START condition can occur more than once before a STOP condition, which is called a REPEATED START condition. All data transfer occurs between a START and a STOP condition as seen in the Figure 2.36 (Philips, 1995).

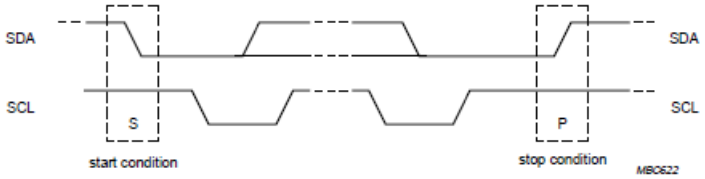

Figure 2.36 : START and STOP Condition

Every byte in I2C protocol is 8 bits, each followed by an ACK bit (SDA = 0) sent from receiver. If the receiver does not pull down the SDA line it is called NACK (SDA=1) which means not acknowledge as descried in the Figure 2.37 and Figure 2.38 (Philips, 1995).

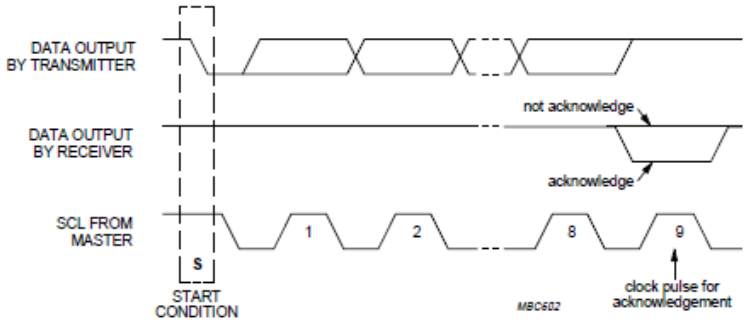

Figure 2.37 : Acknowledge on I2C Bus

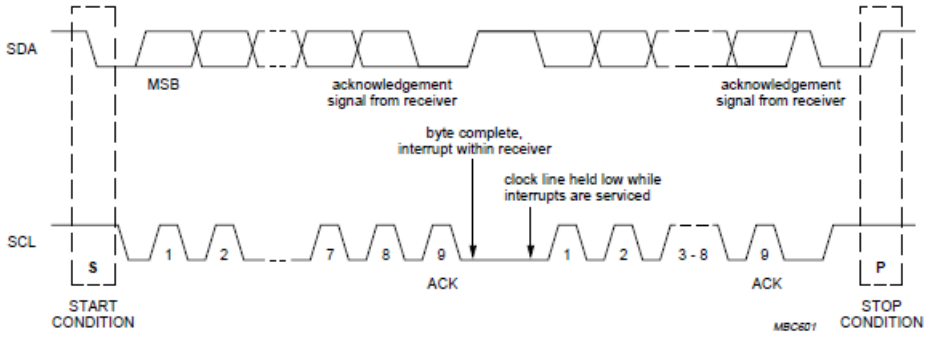

Figure 2.38 : Data Transfer on I2C Bus

Every chip connected to the I2C bus has a unique 7 bit address so that the master can tell which slave it wants to communicate with. This 7 bit address is followed by a R/!W bit, determining whether the master wants to write or read. A complete data transfer is shown in the Figure 2.39 (Philips, 1995).

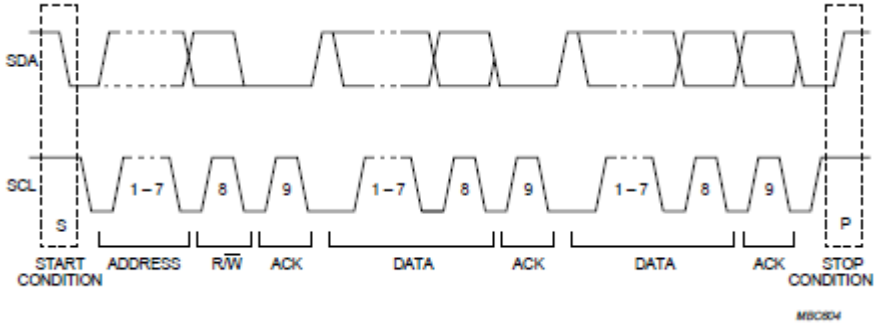

Figure 2.39 : Complete Data Transfer on I2C Bus

2.1.5.2 I2C controlled memory

There are 48 D flip-flops in the memory which represents 6 8 bits register which are addressed by 3 bits address control signal ADDR[2:0]. Value of each register can be set from 0 to 255 if needed. Write and read operation is explained below.

Write sequence:

In the write sequence, each byte is written one by one, simply by sending the address and data after the control byte as seen in the Figure 2.40 (*128-Bit I2C Bus Serial EEPROM*, 2011).

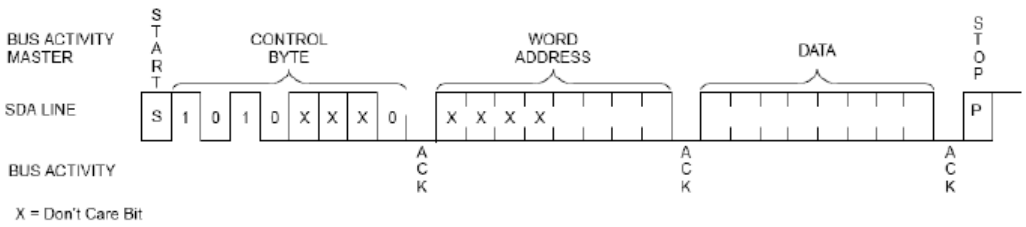

Figure 2.40 : Write Sequence

The I2C device address of the temperature to digital converter is 0x57 which is 101 0111 in binary code. So the XXX in the control byte must be 111 in the Figure 2.40. Word address can be 0 to 5 and data can be 0 to 255.

Read sequence:

Current address read sequence enables the master to read the data of the current address. Since the address bus is incremented after read operation, if the last read address was n, current address read returns the data at the address of n+1. The sequence is simply a control byte with read enabled, followed with data sent from slave transmitter. After the read operation is completed, the master does not send an ACK bit, telling the slave that the communication will be stopped. If master sends an ACK bit, the operation continues as sequential read. The sequence of current address read is shown in the Figure 2.41 (*128-Bit I2C Bus Serial EEPROM*, 2011).

Random read sequence enables the master to read the data of the arbitrary address. In order to do this, master sends a control byte with write enabled, followed by one byte which contains the word address. After that, the master sends a REPEATED START, followed by a control byte with read enabled, thus the slave becomes transmitter and sends the data of the address transmitted by master as seen in the Figure 2.42 (*128-Bit*

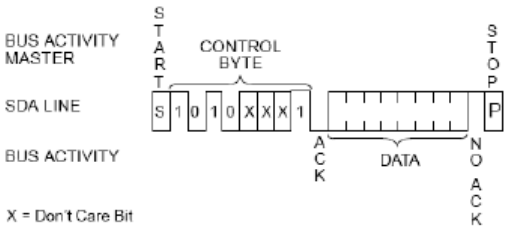

Figure 2.41 : Current Address Read

I2C Bus Serial EEPROM, 2011). After the read operation is completed, the master does not send an ACK bit, telling the slave that the communication will be stopped. If master sends an ACK bit, the operation continues as sequential read (*128-Bit I2C Bus Serial EEPROM*, 2011).

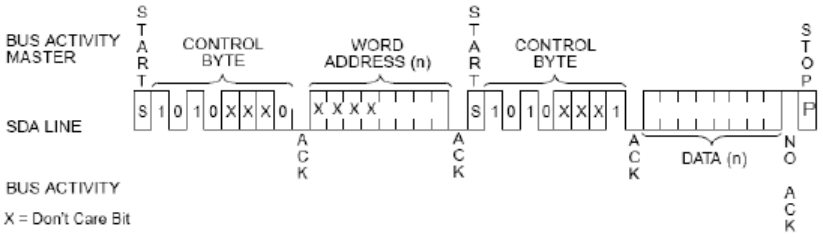

Figure 2.42 : Random Address Read

If the master sends ACK after the read operation in random read, the address is incremented by one, and the data transfer of the incremented address starts. This procedure goes on until master does not send ACK after read operation as seen in the Figure 2.43 (*128-Bit I2C Bus Serial EEPROM*, 2011).

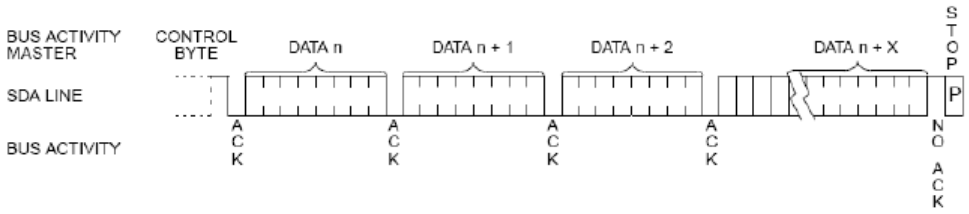

Figure 2.43 : Sequential Read

In the Figure 2.44 I2C memory controller of the temperature to digital converter is shown. It has two main blocks called I2C Main which is I2C slave core and Register Block which contains configuration bits of the chip.

In the Table 2.5 pins and their descriptions of the I2C memory controller is given. There are three inputs and two outputs of the I2C memory controller. There are also five intermediate input/output pins.

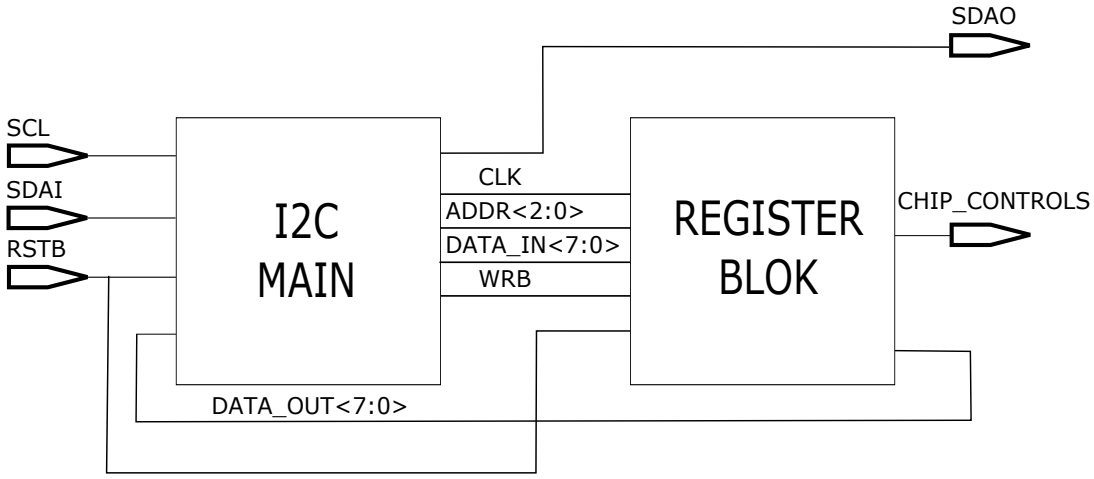

Figure 2.44 : I2C Memory Controller

Table 2.5 : Pins of I2C Memory Control

Name	Purpose	Description
SCL	Input	I2C Clock Input
SDAI	Input	I2C Data Input
RSTB	Input	Power-On Reset Input
SDAO	Output	I2C Data Output
DATA_IN[7:0]	Input-Output	Data Input of Register Array
DATA_OUT [7:0]	Input-Output	Data Output of Register Array
ADDR[2:0]	Input-Output	Address Input of Register Array
CLK	Input-Output	Clock Input of Register Array
WRB	Input-Output	Write-Read Input of Register Array
CHIP_CONTROLS[47:0]	Output	Chip Control Outputs

In the Table 2.6 chip control registers are explained and their width and default values are given.

Table 2.6 : Register

Name	Width	Default	Description
TCTRIM[7:0]	8	4	DAC Trim Bits for PTAT Current
TST[2:0]	3	2	Bandgap Test Bits
VIBTRIM[5:0]	6	32	Bandgap Current Trim Bits
VBGTRIM[3:0]	4	8	Bandgap Voltage Trim Bits
ENDAC	1	1	Enable PTAT Current DAC
COUNTIN	16	65535	Counter Value
ENMODP	1	0	Enable Modulator Positive Inuput
ENMODM	1	0	Enable Modulator Negative Inuput
ENCHOPMOD	1	1	Enable Chopper for SDM
ENCHOPDRI	1	1	Enable Chopper for SDM Driver
DUMMY[5:0]	6	0	Spare Bits

2.1.5.3 Digital counter

In the previous sections, temperature information is translated into current, voltage and a single digital bit stream by a second order sigma delta modulator respectively. In this section temperature information will be extracted as a digital code from this single digital bit stream by a digital counter.

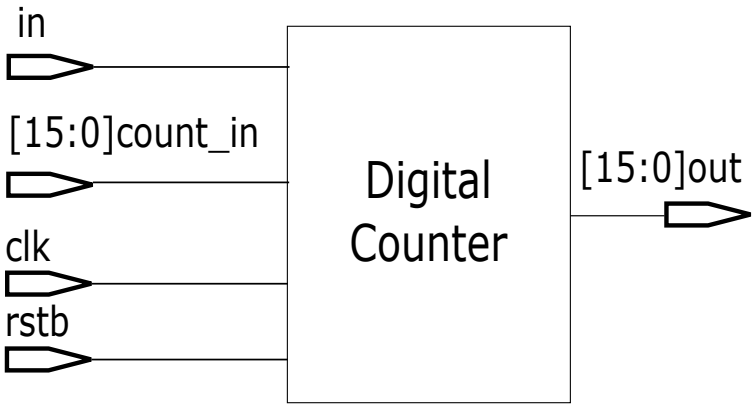

Figure 2.45 : Digital Counter Inputs and Outputs

Inputs and outputs of digital counter block are shown in the Figure 2.45. Counter has 4 inputs and 1 output which is given below with their descriptions.

- in: is the input signal which is driven by modulator output.
- 15:0]count_in: determines the counter value and is 2^{16} by default.
- clk: is the clock input. Counter counts up or keep its value depending on the input signal on every rising edge of clock.
- rstb: is the asynchronous active low reset. Counter is reset when rstb signal is logic 0.
- [15:0]out: is the 16 bit parallel output which gives the digital code representation of the temperature by parallel 16 bit.

Digital counter counts every logic 1 and logic 0 and increases counter value 1 up for logic 1, keeps current value for logic 0. When the counter register is 0 the result is loaded to out and counter register is restarted. Verilog code of the digital counter block is given in the Appendix A1.

2.1.5.4 Parallel to serial converter

Parallel to serial converter takes 16 bits output of integrator and converts 16 bits parallel signal into one bit serial data in order to simplify temperature to digital conversion and reduce number of pins. It has 4 inputs and 2 outputs as seen in the Figure 2.46. Verilog code of the parallel to serial converter digital block is given in the Appendix A1.

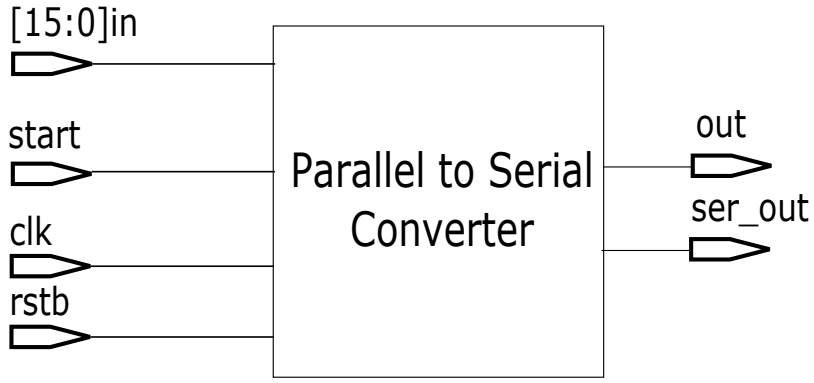

Figure 2.46 : Inputs and Outputs of Parallel to Serial Converter

- [15:0]in: is the 16 bits parallel input signal which is generated by counter.
- start: start signal which is generated by counter when counter register is 0.
- clk: is the clock input.
- rstb: is the asynchronous active low reset. Block is reset when rstb signal is logic 0.
- out: is the serial output which gives the digital code representation of the temperature by serial single 16 bit.
- clk_out: is the clock output.

The clock and the output of the parallel to serial converter block is directly routed to the pads CLK_OUT and SER_OUT. The result of temperature to digital conversion will be measured at these two pins.

2.1.6 Power on reset

Digital circuits especially which contains memory block needs a reset after power up to be settled to known state. A silicon proved POR circuit which is designed in the same process is used to reset digital circuit. Block diagram of the circuit is given in the Figure 2.47.

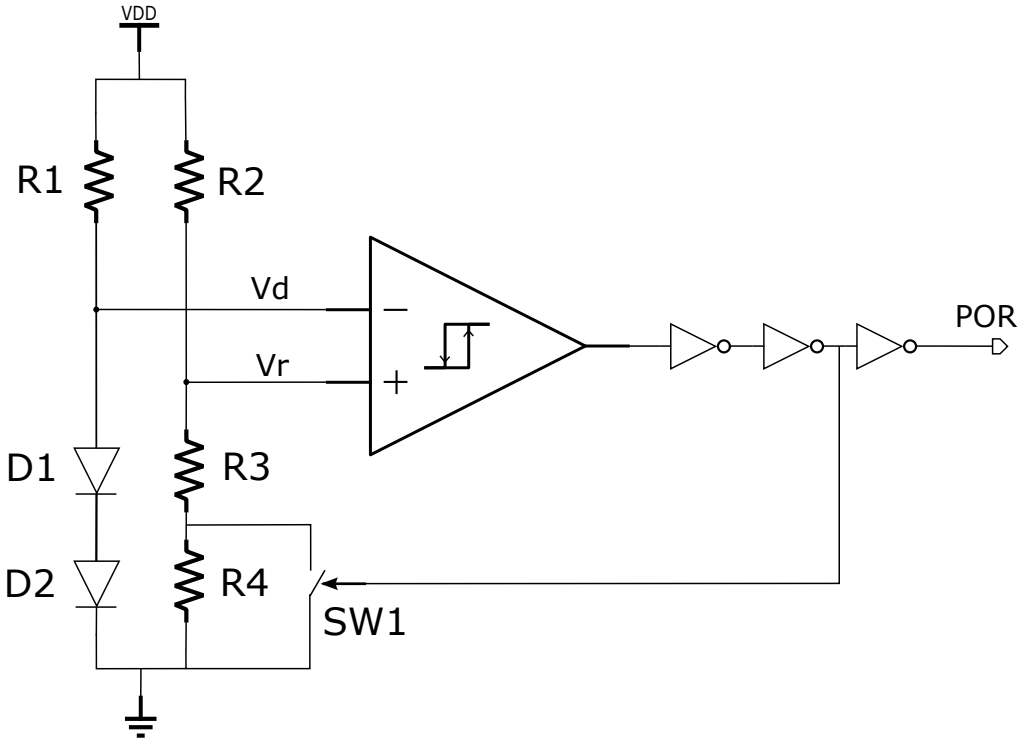

Figure 2.47 : Power on Reset Circuit

POR circuit creates a reset signal by comparing the voltage of resistor and voltage of diode. Negative input of the comparator is connected to V_d which is 2 times of a diode voltage while positive input of the comparator is connected to V_r which is a resistor divider formed by R_2 and R_3. V_d and V_r voltage equations are given below.

$$\begin{aligned} V_d &= V_{D1} + V_{D2} \\ V_r &= VDD\left(\frac{R3}{R_2 + R_3}\right) \end{aligned} \tag{2.46}$$

If diode voltage is taken as 0.75V approximately and V_r is calculated for the values $R_2 = 50K$ and $R_3 = 100K$.

$$\begin{aligned} V_d &= 0.75 + 0.75 = 1.5V \\ V_r &= 3.3\left(\frac{100K}{50K + 100K}\right) = 2.2V \end{aligned} \tag{2.47}$$

V_d and V_r are found as 1.5V and 2.2V respectively. Simulation result of the POR circuit gives V_d and V_r values as 1.46V and 2.27 as expected. Transient simulation results of the POR circuit are given in the Figure 2.48 and 2.49.

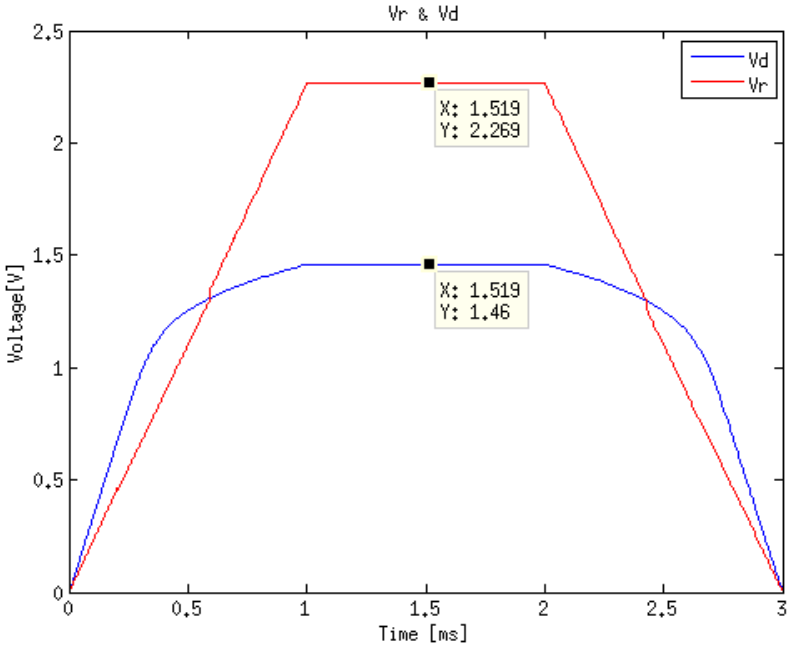

Figure 2.48 : Simulation Result V_r and V_d

As seen in the Figure 2.49 reset signal is removed after VDD is reached 1.964V and re-applied after VDD drops down 1.889V which gives a 75mV hysteresis.

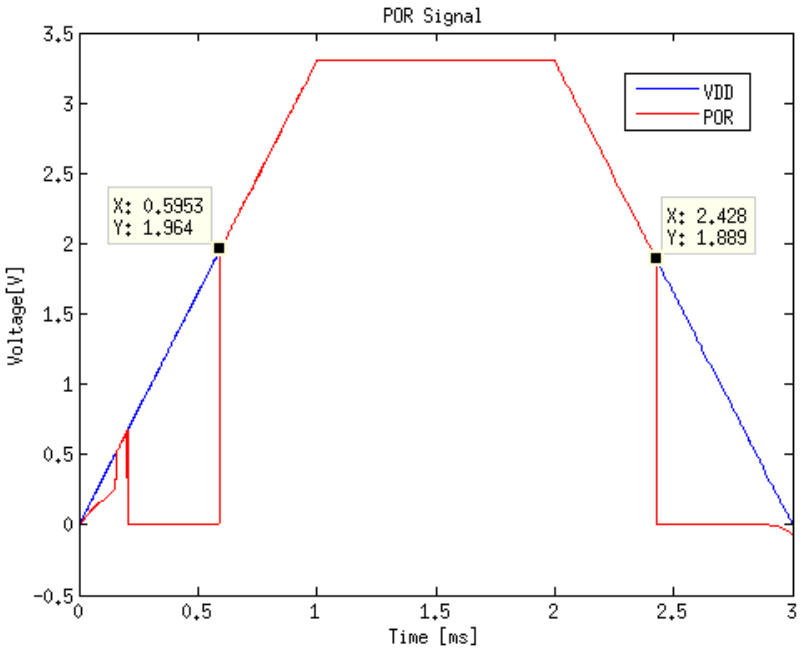

Figure 2.49 : Simulation Result of POR Circuit

2.2 Top Level Schematic

In section Architecture architecture is given in a system manner by a block diagram. In the Figure 2.50 system is given more detailed. Top level schematic of temperature to digital converter is given in section APPENDIX A.2.

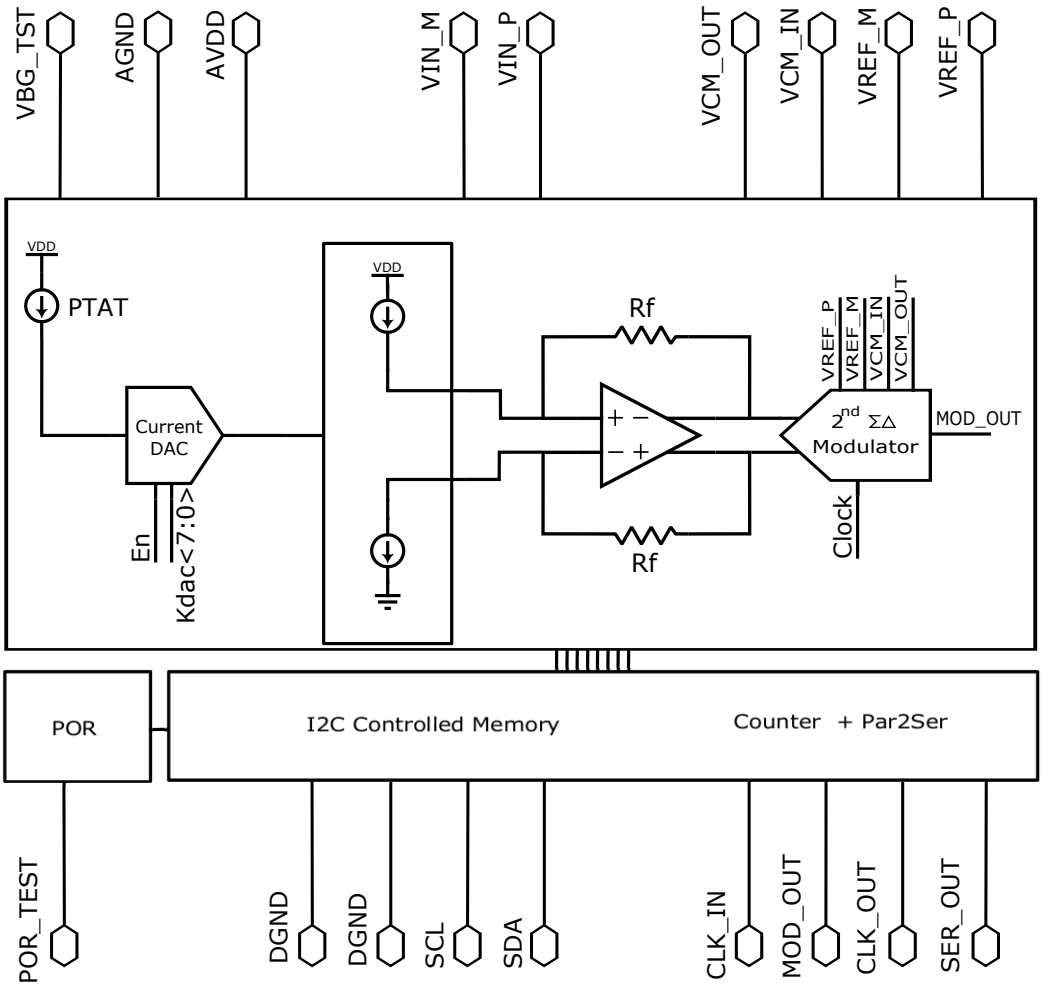

Figure 2.50 : Temperature to Digital Block Diagram

As seen in the Figure 2.50 there are total of 18 pins including analog and digital supply voltages, reference voltages, test pins and digital I/Os in the system. These pins can be grouped as analog and digital as in the Table 2.7 which also gives purpose and description of related pins.

Table 2.7 : Pin Name and Description

Pin Name	Description
Analog Pins	
AVDD	Analog Supply Voltage
AGND	Analog Ground
VSUB	Guard-ring Bias
VCM_IN	Common Mode Reference Voltage In
VCM_OUT	Common Mode Reference Voltage Out
VREF_P	Positive Reference Voltage Input
VREF_M	Negative Reference Voltage Input
VIN_P	Positive Analog Input Voltage
VIN_M	Negative Analog Input Voltage
TST_PAD	Bandgap Reference Voltage Test Output
Digital Pins	
DVDD	Digital Supply Voltage
DGND	Digital Ground
SCL	I2C Clock Input
SDA	I2C Data Input
CLK	Clock Input
MOD_OUT	Modulator Output
CLK_OUT	Clock Output
SER_OUT	Serial Data Output
POR_TEST	Power on Reset Signal Test Output

Temperature to digital converter represent temperature as digital code as the following equation.

$$code = \frac{V_{PTAT}}{V_{lsb}} + \frac{counter_{max}+1}{2} \tag{2.48}$$

where

$$V_{lsb} = \frac{VREF\_P - VREF\_N}{counter_{max}} \tag{2.49}$$

In the Figure 2.51 a simulation result of temperature to digital converter is shown at room temperature 27C where $K_{DAC} = 4$, $VREF\_P = 2.4V$, and $VREF\_M = 0.9V$. Simulation results *code* as $(0000001010010100)_{binary}$ which is decimal 660. The Equation (2.48) also gives the *code* as 658.8 which proves the temperature to digital converter works as expected.

$$V_{lsb} = \frac{2.4-0.9}{1023} = 1.466mV \tag{2.50}$$

$$code = \frac{25.875 \cdot 10^{-3} \cdot ln(8) \cdot 4}{1.466 \cdot 10^{-3}} + \frac{1024}{2} = 658.8 \tag{2.51}$$

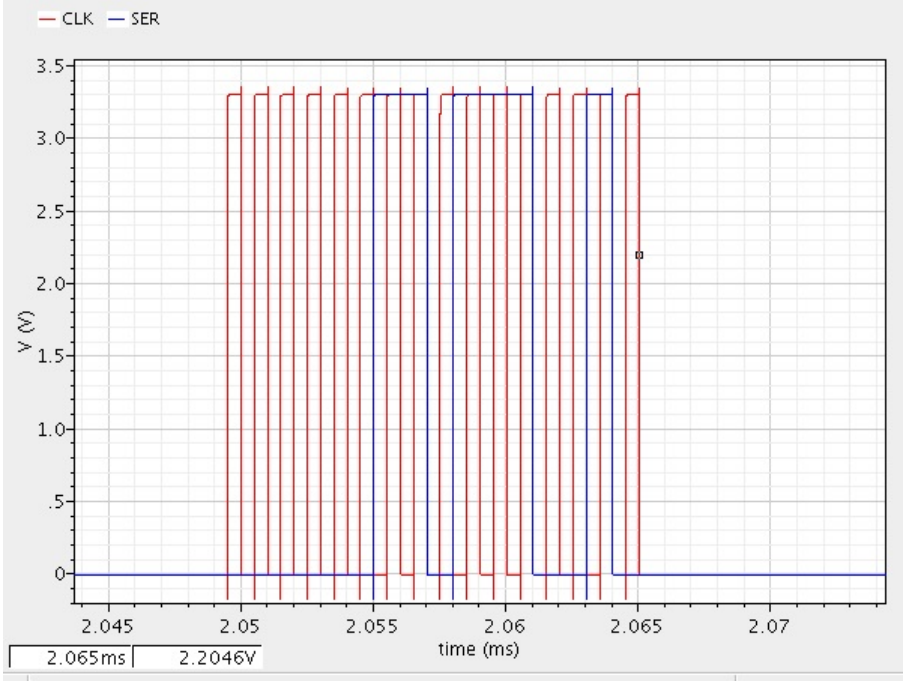

Figure 2.51 : Top Level Simulation Result

The simulation is repeated in the same conditions for the temperature -40C and 85C and code is found as 625 and 690 respectively. To compare simulation results, the Equation (2.48) is solved at -40C and 85C.

$$code = \frac{20.096 \cdot 10^{-3} \cdot ln(8) \cdot 4}{1.466} + \frac{1024}{2} = 626.020 \tag{2.52}$$

$$code = \frac{30.878 \cdot 10^{-3} \cdot ln(8) \cdot 4}{1.466} + \frac{1024}{2} = 687.195 \tag{2.53}$$

There is a strong relation between K_{DAC} value and temperature resolution. K_{DAC} determines the voltage difference for every 1C temperature step according to equation (2.21). To obtain 1C temperature resolution , V_{lsb} of the sigma delta modulator must be equal or less than temperature coefficient of V_{PTAT} voltage. For example when $K_{DAC} = 4$ which is default value, the required counter value is calculated as below.

$$\frac{\Delta}{dT} V_{PTAT} = 2 \cdot 0.085 \cdot 10^{-3} \cdot 2.079 \cdot 4 = 1.414mV \tag{2.54}$$

So the counter value must be 1061.

$$\begin{aligned} V_{lsb} &= \frac{2.4 - 0.9}{N} \leq 1.414mV \\ N &\geq 1060.822 \end{aligned} \tag{2.55}$$

In the Table 2.8 minimum required counter values are given for values 4,8 and 10 of K_{DAC} along width ΔV voltage for every 1C temperature step.

Table 2.8 : K_{DAC} vs Counter Value

K_{DAC}	ΔV	Min Counter Value
4	0.707 mV	2121
8	1.414 mV	1061
10	1.768 mV	849

In the Figure 2.52 and Figure 2.53 simulation results of temperature to digital converter is given where counter value $N = 1023$, the $K_{DAC} = 4$ and $K_{DAC} = 8$ respectively. Simulation is done by 5C temperature steps. More resolution step is not convenient due to long simulation time.

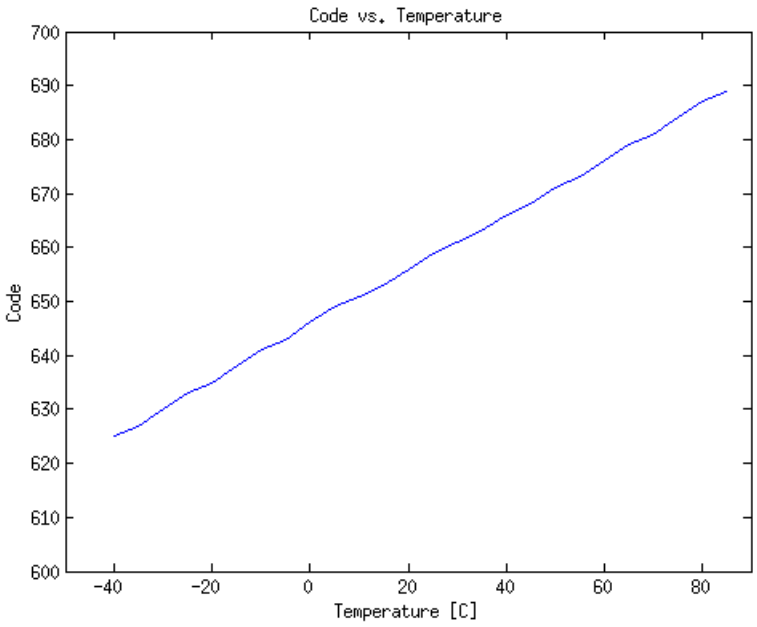

Figure 2.52 : Top Level Simulation Result with $N = 10$, $K_{DAC} = 4$

Both graphs are showing increasing code vs increasing temperature as expected. But the slope of each graph which is shown in the Figure 2.54 gives the resolution of the conversion. Blue trace belongs to $K_{DAC} = 4$ and the red one is $K_{DAC} = 8$. It is clearly seen that counter value of 1024 is not enough for correct results while $K_{DAC} = 4$. 5C temperature steps corresponds the 3.535mV changes and the V_{lsb} is 1.466mV. So code must be change by 2.5 for every 5C temperature change which is not possible. But code is changing randomly between 2 and 3 values which still indicates the correct temperature for bigger temperature changes.

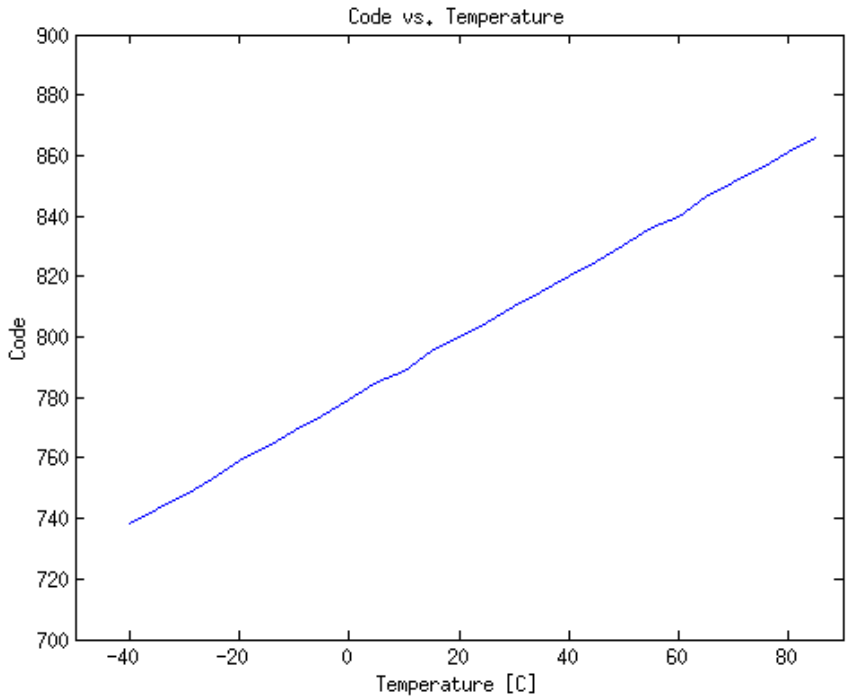

Figure 2.53 : Top Level Simulation Result with $N = 10$, $K_{DAC} = 8$

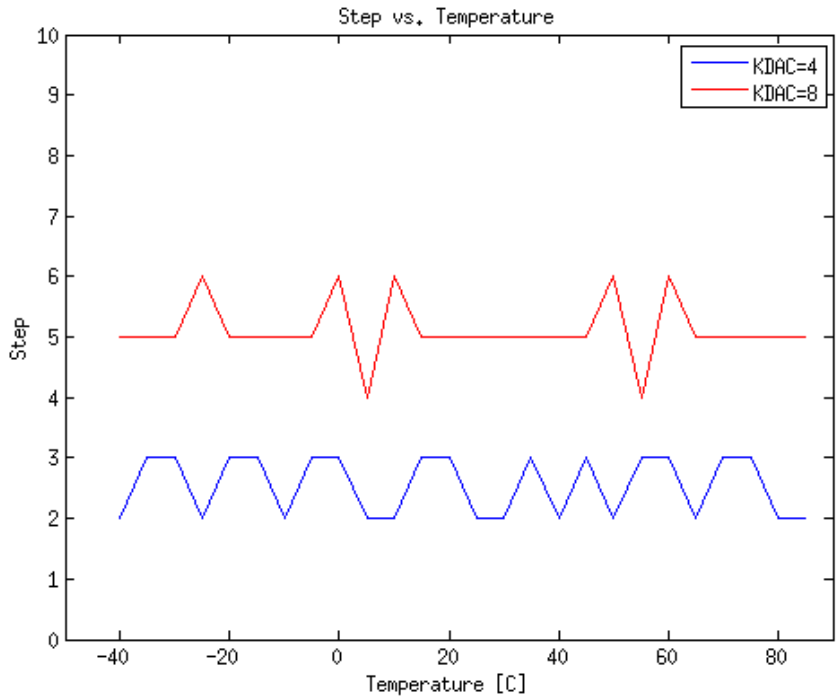

Figure 2.54 : Top Level Simulation Result with $K_{DAC} = 4, 8$

If K_{DAC} is chosen as 8, every 5C temperature step corresponds the 7.07mV changes and since V_{lsb} is 1.466mV code must be changed by 5 for every 5C temperature change. There are some 4 and 6 steps which corresponds to simulation fault due to first conversion includes settling time and error of amplifier and integrators.

In the Figure 2.55 code is represented with voltage and shown with ideal voltage transfer curve.

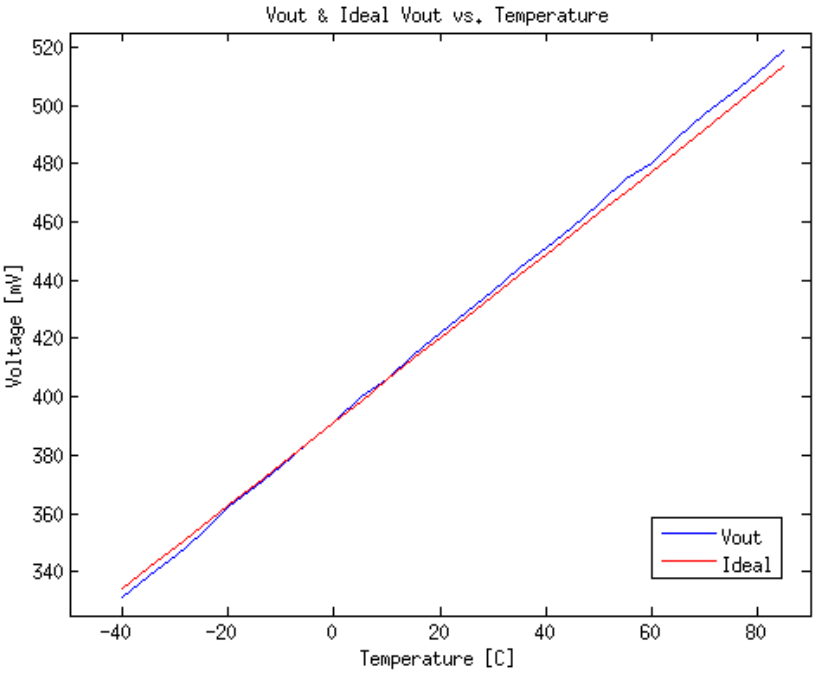

Figure 2.55 : Vout vs. Ideal for $K_{DAC} = 8$

As seen in the figure there is a gain error at the output. Gain error can be easily eliminated with first order equation fit as shown in the Figure 2.56.

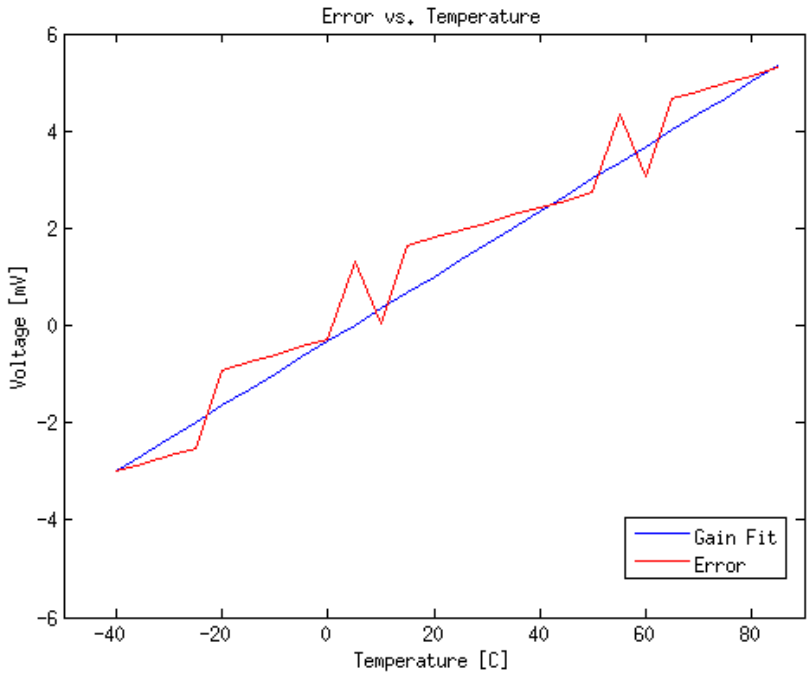

Figure 2.56 : Error for $K_{DAC} = 8$

Error of the system after first order gain fit is given in the Figure 2.57. Gain correction fix the error and keep in the range of ± 0.5 LSB.

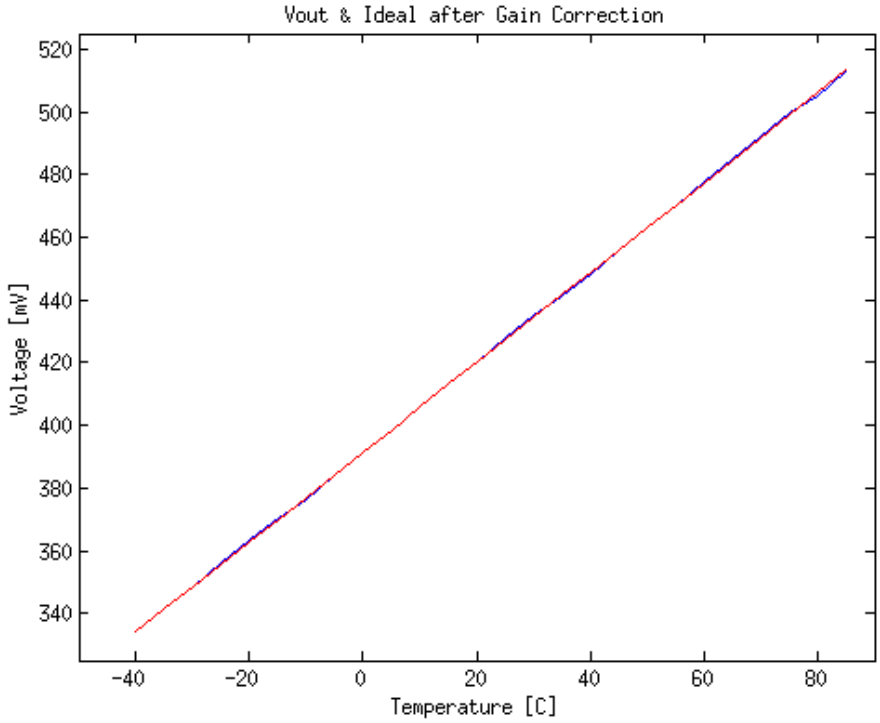

Figure 2.57 : Vout vs. Ideal after Gain Calib $K_{DAC} = 8$

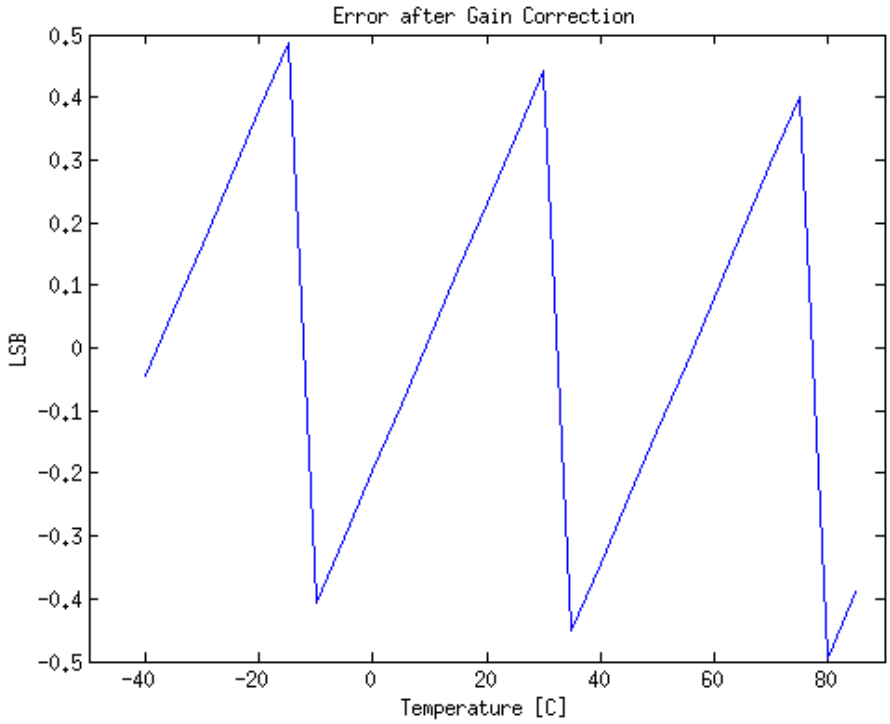

Figure 2.58 : Error after Gain Calib $K_{DAC} = 8$

Additionally due to chopper stabilization technique there need to be several results at every temperature value to make an average operation and see the chopper effect. But this means a lot of simulation times. So chopper stabilization technique is disabled and the simulation is repeated with $K_{DAC} = 10$ and 10 bit counter. Simulation result is given in the Figure 2.59

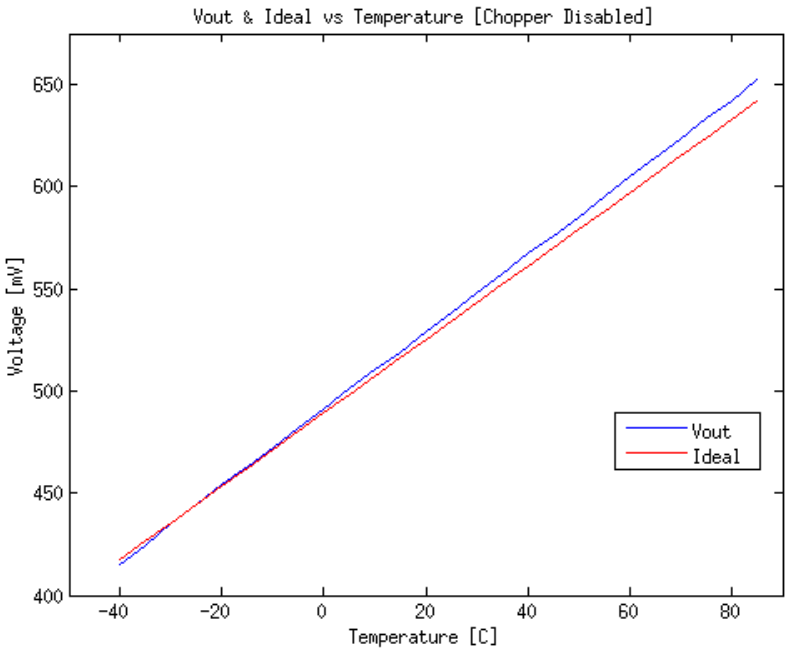

Figure 2.59 : Top Level Simulation Result with Chopper Disabled

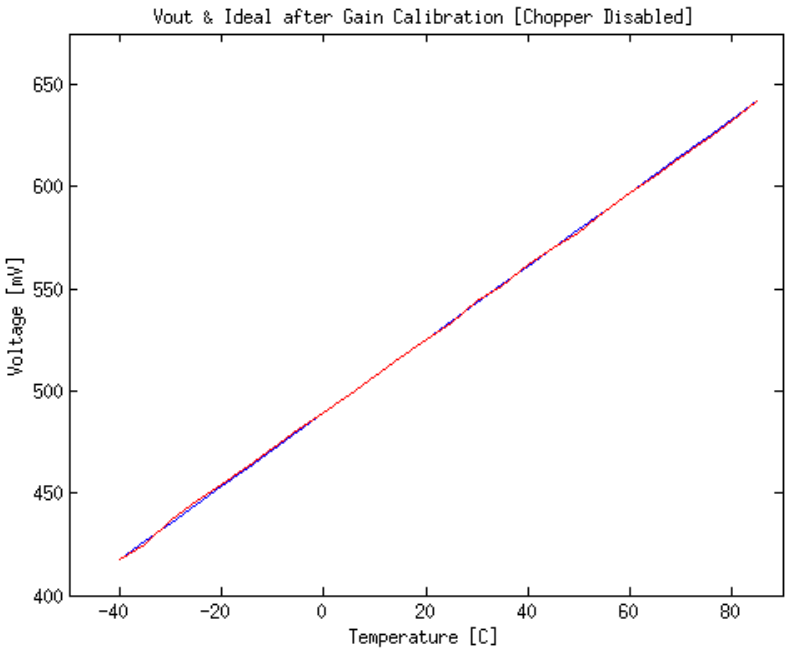

Figure 2.60 : Top Level Simulation Result with Chopper Disabled After Calibration

Second simulation confirms the relation between K_{DAC} and counter value N and successful conversion.

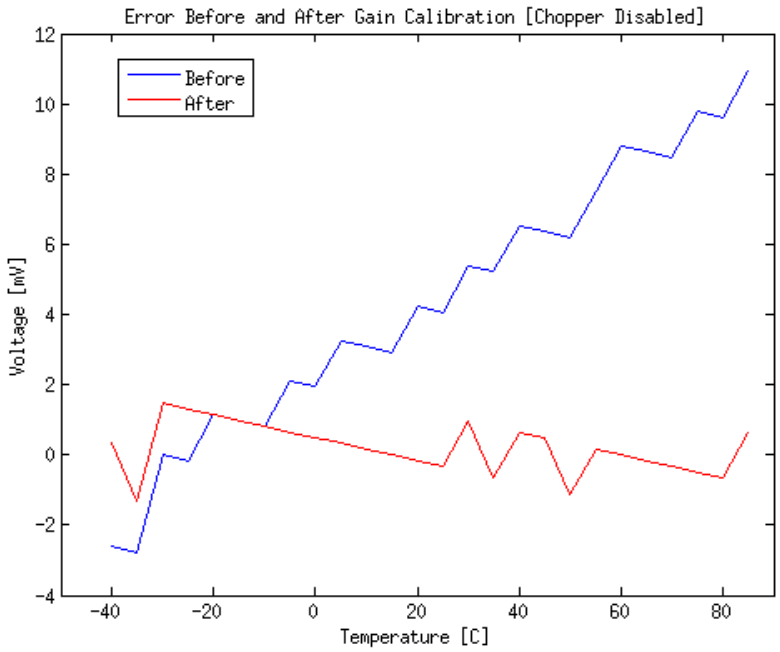

Figure 2.61 : Error with Chopper Disabled Before and After Calibration

As seen in the results with $K_{DAC} = 10$ and 10 bit counter 1C resolution is confirmed in the range of -40C to 85C. Respectively 0.5C resolution is achieved with 11 bit counter and 0.25C resolution is achieved with 12 bit counter when$K_{DAC} = 10$. Due to long simulation times this resolutions are obtained with less temperature points around room temperature 27C.

In the following section layout design of the temperetautre to digital converter will be explained.

3. LAYOUT DESIGN OF THE TEMPERATURE TO DIGITAL CONVERTER

3.1 Process Layout Overview

AMSH35B4 is a high voltage 0.35um CMOS process from Austria Micro Systems (AMS). Process has option for isolated NMOS and PMOS which is also called triple well. General information about the process is listed below.

- 2 Layers Poly-silicon
- 4 Layers Metal, Thick 4^{th} Metal
- High Resistive Poly
- 50 Volts Maximum operating voltage
- 3.3V / 5.0V / 20V Maximum gate voltage

In this work MOS transistors are isolated 3.3V gate voltage devices. 2 poly-silicon layers are used to generate poly-poly capacitor while high resistive poly layer is used for high value resistors. Three metal layers are used interconnections in blocks and routing between blocks where 4^{th} thick metal is used for routing supply voltages and ground connections due to its low square resistance which comes from thickness.
In the following sections layout design of sub blocks and finally layout design of full chip will be explained.

3.2 PTAT Current Generator

As indicated in chapter 2, PTAT current generator is used from previously designed and measured silicon proved work. The layout of reference circuit which is shown in the Figure 3.1 (Ozkaya, 2010) which contains PTAT core is directly imported from .gdsII file.

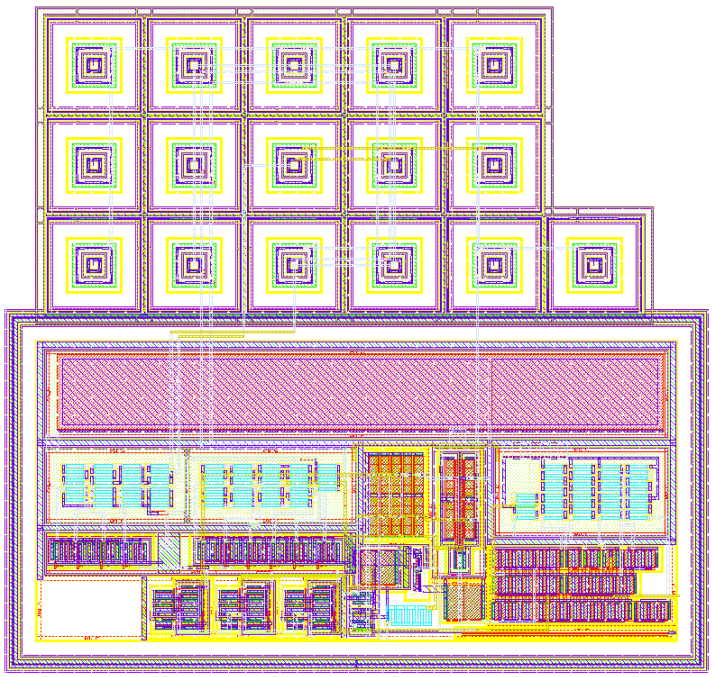

Figure 3.1 : Layout of PTAT Current Generator

The BJT devices are placed in a separate guard ring while MOS devices with passive devices, resistors and capacitors, are placed in the same guard ring.

3.3 PTAT DAC and Differential Circuit

As indicated in chapter 2, PTAT DAC is used from previously designed and measured silicon proved work. The layout of PTAT DAC circuit which is shown in the Figure 3.2 (Ates, 2010) is directly imported from .gdsII file.

The layout of the single to differential circuit is given in the Figure 3.3. PMOS current mirror network is located at the top of the layout while NMOS network is located at the bottom. This approach is tried to be kept for all following blocks to make easier power and ground routing where supply lines are planned to be routed from top and ground lines to be roted from bottom side of each block.

To improve matching main current mirror transistor is put in the middle of the transistor array and the transistors which is mirroring the current is placed right and left side of the main transistor. The same approach is followed for the cascode devices. As seen in the Figure 3.3 main current mirror network is located at the left side of the layout while cascode transistors are located at the right side of the layout.

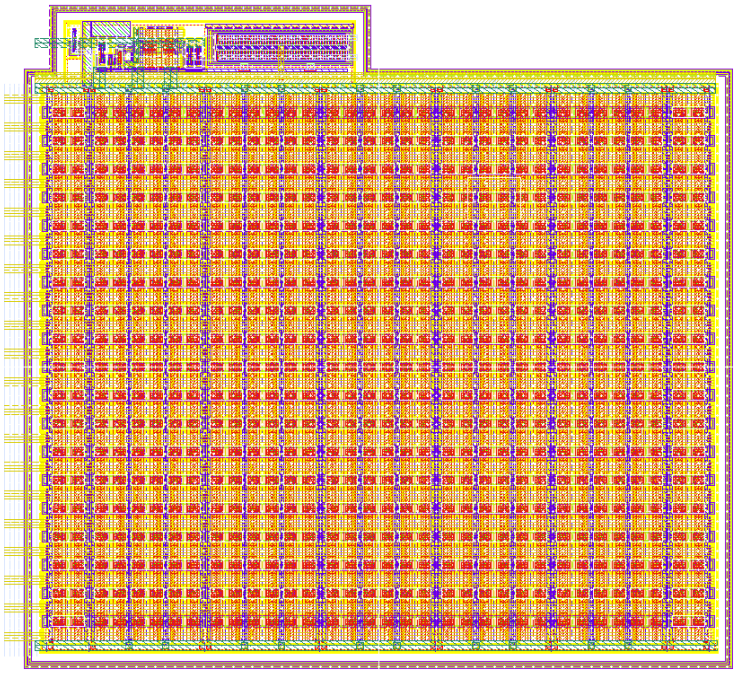

Figure 3.2 : Layout of PTAT Current DAC

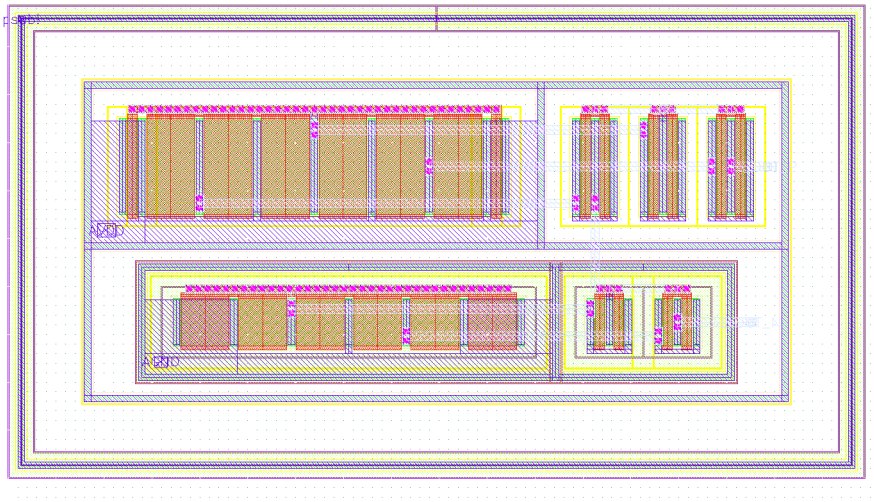

Figure 3.3 : Layout of Single to Differential Circuit

3.4 PTAT Voltage and Modulator Driver

Layout of modulator driver is consist of two main parts where the first one is an operational amplifier and the second part is feedback resistors and bypass switches. Layout design of the operational amplifier is explained in detail in the subsection 3.5.4 due to operational amplifier which is used for modulator driver is exactly the same as the operational amplifier which is used as a first integrator in the sigma delta modulator. Feedback resistors and bypass switches are placed at the top of the operational amplifier in a seperate guard ring.

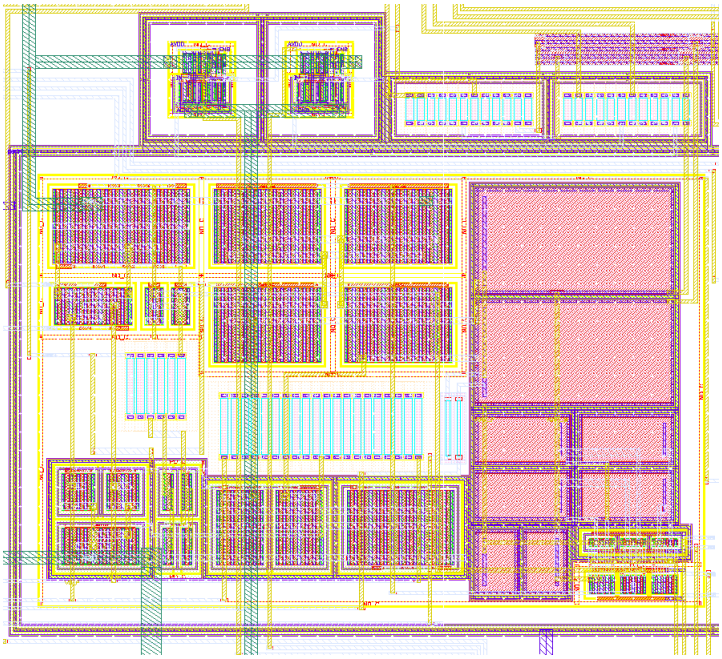

Figure 3.4 : Layout of PTAT Voltage Generator - Modulator Driver

3.5 Analog Switched Capacitor Sigma Delta Modulator

The most critical block in the temperature to digital converter is the sigma delta modulator due to performance of the modulator determines the system performance. Therefore layout of the modulator need to be drawn very carefully. In the Figure 3.5 layout plan scheme is given. In the following sections the layout consideration and design is presented for each fraction of this plan.

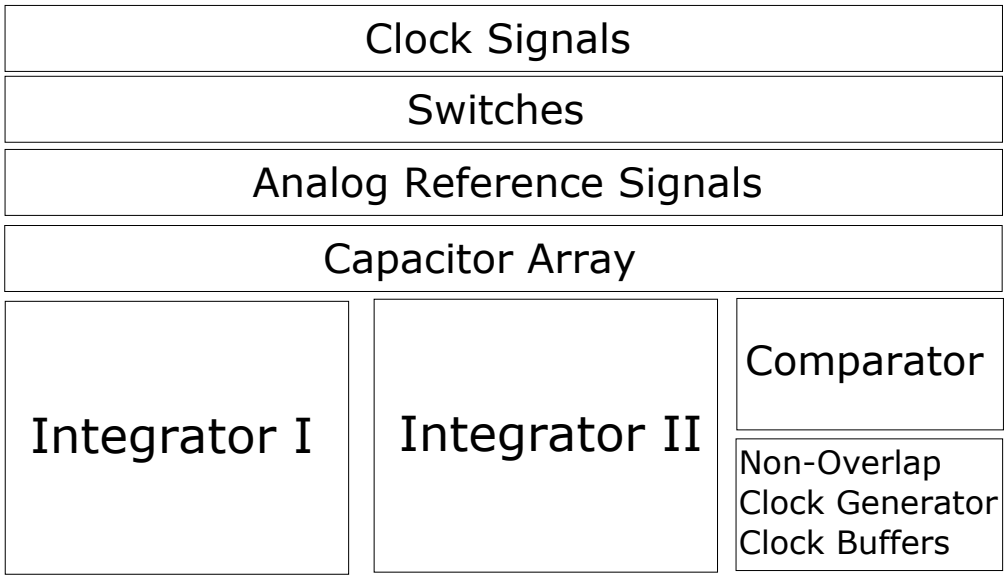

Figure 3.5 : Layout Plan of Sigma Delta Modulator

3.5.1 Unit capacitor and capacitor array

Matching of the sampling and feedback capacitors in the sigma delta modulator design is very important to achieve good resolution. Any mismatch on capacitors can be lead to gain error or worse, saturation at the output of integrators which decrease system performance. Therefore layout of capacitor array is very critical.

In this section, first a brief introduction and performance metrics are given about poly-poly capacitor. Then designed unit capacitor and capacitor array is explained in detailed.

In the Figure 3.6 cross section and the equivalent circuit of a poly-poly capacitor is shown (Maloberti, 2001).

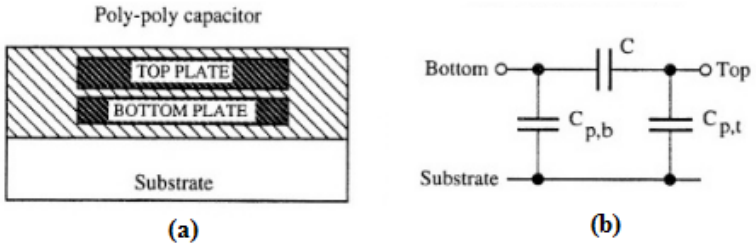

Figure 3.6 : Poly-Poly Capacitor a) Cross Section b) Equivalent Circuit

The capacitance, neglecting fringing and parasitic effects, is given by

$$C = \left(\frac{\varepsilon_0 \cdot \varepsilon_r}{t_{ox}} \right) WL \tag{3.1}$$

where ε_r is the relative dielectric constant and t_{ox} is the oxide thickness, W and L are the geometrical dimensions of the plates,assumed as being rectangular (Maloberti, 2001).

The oxide thickness of typical technology today is around 10 nm. Assuming the relative dielectric constant ε_r as equal to 3.8 (the nominal value for SiO_2) the capacitance of the thin oxide per unit area results $3.36 fF/um^2$.

The bottom plate made with poly-silicon, the parasitic $C_{p,b}$ is normally smaller, as the bottom plate sits upon relatively thick oxide; its value holds a fraction of a percent of the integrated capacitor. For both structures, the top plate parasitic, $C_{p,t}$ is clearly smaller than the bottom plate parasitic; it is around one order of magnitude less than the value of $C_{p,b}$.

The accuracy of an integrated capacitor is determined by the accuracy of the parameters in Equation (3.1). Since the all parameters derive from different technological steps, all the parameters can be assumed as being statistically independent (Maloberti, 2001).

$$(\frac{\Delta C}{C})^2 = (\frac{\Delta \varepsilon_r}{\varepsilon_r})^2 + (\frac{\Delta t_{ox}}{t_{ox}})^2 + (\frac{\Delta L}{L})^2 + (\frac{\Delta W}{W})^2 \qquad \textbf{(3.2)}$$

In the Figure 3.7 general performance metrics are given for different capacitor types (Maloberti, 2001). It is clearly seen that poly-poly capacitor has the optimum performance if the absolute accuracy, temperature coefficient and voltage coefficient are considered at the same time.

Type	t_{ox} nm	Absolute Accuracy %	Temperature Coefficient ppm/°C	Voltage Coefficient ppm/V
poly-diff.	6-20	7-14	20-50	60-300
poly I-poly II	8-25	6-12	20-50	40-200
metal-poly	500-700	6-12	50-100	40-200
metal-diff.	1200-1400	6-12	50-100	60-300
metal I-metal II	800-1200	6-12	50-100	40-200

Figure 3.7 : The Performance of Different Types of Integrated Capacitors

Designed unit capacitor is shown in the Figure 3.8. Capacitor value is determined by square poly2 area over poly1 which is 7.5 X 7.5 um for this work. The top plate poly2 is accessible at metal1 layer from all sides while bottom plate poly1 is accessible at metal2 layer.

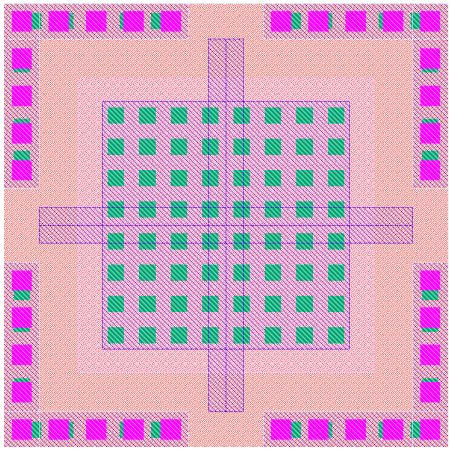

Figure 3.8 : Layout of Unit Capacitor

50 unit capacitors is aligned and a capacitor array is constructed shown in the Figure 3.9. There are dummy poly-poly capacitors at the edge of each side of capacitor array to prevent any edging related mismatches.

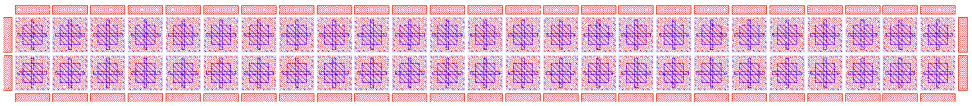

Figure 3.9 : Layout of Capacitor Array

3.5.2 Reference and clock signals

To minimize the parasitic coupling between analog reference signal and digital clock signals, the signals are shielded with ground signal shown in the Figure 3.10 and Figure 3.11.

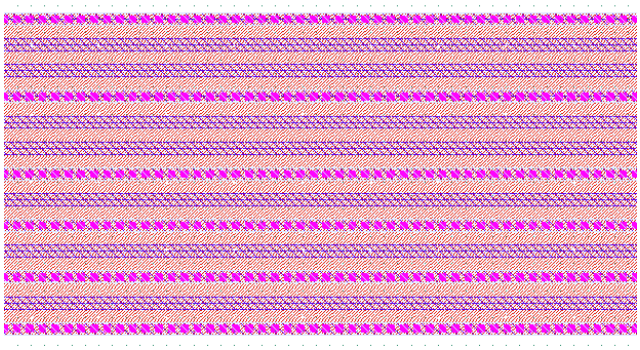

Figure 3.10 : Ground Shielded Clock Signals

The bottom plate is poly1 layer and the top plate is metal2 layer where these two layers are shorted with contact (poly1 to metal1) and via1 (metal1 to metal2) layers and connected to the ground. In the middle metal1 is used to route reference or clock signals. For more critical signals on metal1, additional ground is added between critical signals to improve isolation more.

Figure 3.11 : Ground Shielded Refernce Signals

3.5.3 Switches

A switch is a critical element in analog processing systems. It is typically used to transfer packets of charge from one analog node to another, but it is also controlled by a digital clock applied to the gate of MOS transistors. Analog function with a digital control, is on the border between the analog world and the digital world and can become a source of possibly undesired coupling that should be avoided (Maloberti, 2001).

The layout of the switch is given in the Figure 3.12 which consist of three inverters for generating inverted clock signals to drive gate of NMOS and PMOS transistor formed as a transmission gate. As seen in the Figure 3.5 it is planed to have switches in the between clock and analog reference signals and have isolation by clock signals coming from top while analog reference signals are coming from bottom side.

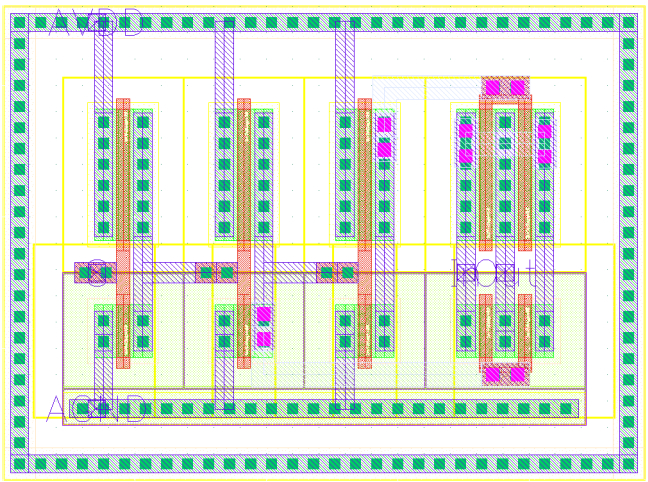

Figure 3.12 : Layout of Transmission Gate

In the Figure 3.13 constructed switch array is shown and the layout of the clock signals, switch array, analog reference voltages and capacitor array is given in the Figure 3.14 which also matches with the plan in the Figure 3.5.

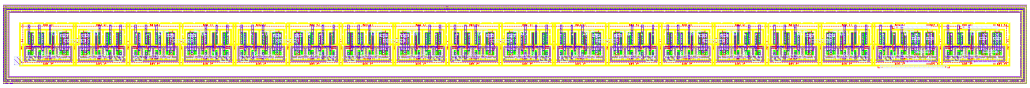

Figure 3.13 : Layout of Transmission Gate Array

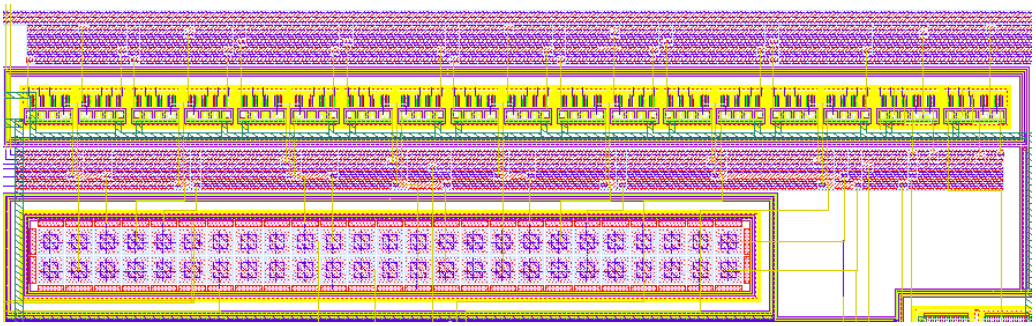

Figure 3.14 : Signal Flow Layout

3.5.4 Integrator

Amplifier consist of a PMOS differential input pair, NMOS and PMOS current mirrors with bias circuit, compensation capacitor and resistor and switched capacitor common mode feedback.

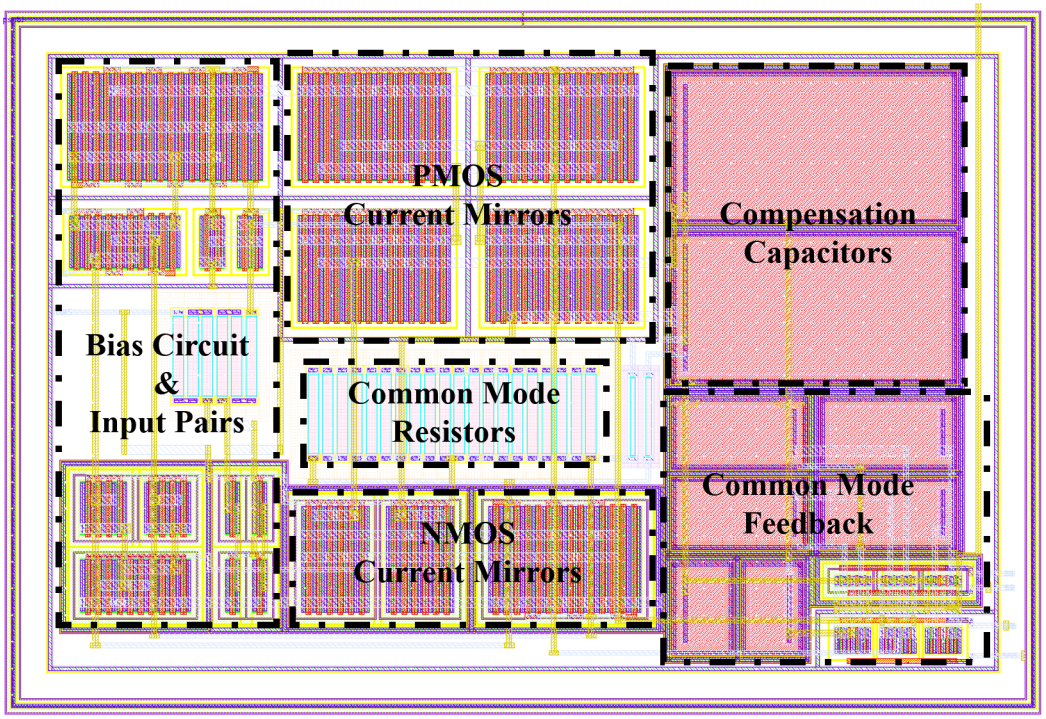

Figure 3.15 : Layout of Integrator

As seen in the Figure 3.15 input PMOS pair and tail current with bias circuit is located in the left side of layout. NMOS and PMOS current mirrors is placed in the middle of layout where NMOS network is at bottom side and PMOS network is at the top side respectively. Common mode resistor is placed in the middle of NMOS and PMOS network. Finally compensation capacitor and resitor with common mode circuit is located at the right side of the layout.

In the scheme seen in the Figure 3.15 signal flows from left side to right side and common mode circuit with clock signal is isolated from input pairs to make sure there will be less clock coupling to the input pair. It is important because any coupling to the input may cause amplified noise at the output.

3.5.5 Comparator

Comparator layout is given in the Figure 3.16. PMOS and NMOS networks are again placed at the top and bottom accordingly and the biasing resistor is located at the middle right side of the layout.

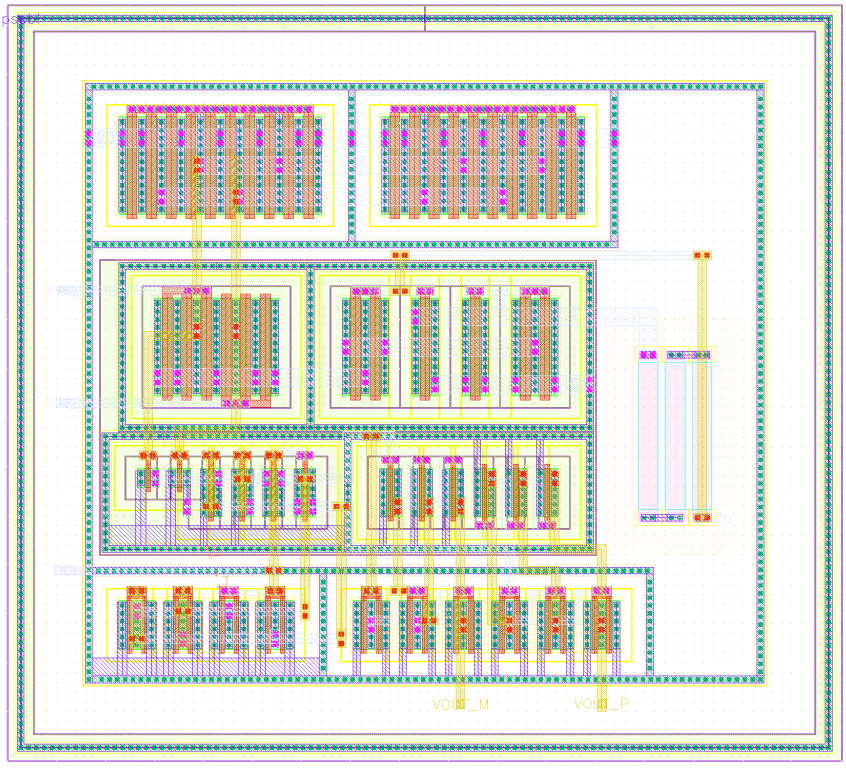

Figure 3.16 : Layout of Comparator

3.5.6 Clock generation and clock buffer

Clock generation circuit has standard logic cells and three capacitors to generate delay for non overlapping clocks. As seen in the Figure 3.17 logic cells are placed at the top side of layout while capacitors are at the bottom. The reason of the capacitors are located at the bottom is bottom plates of capacitors is connected to ground line and it is planned to have global ground line at the bottom.

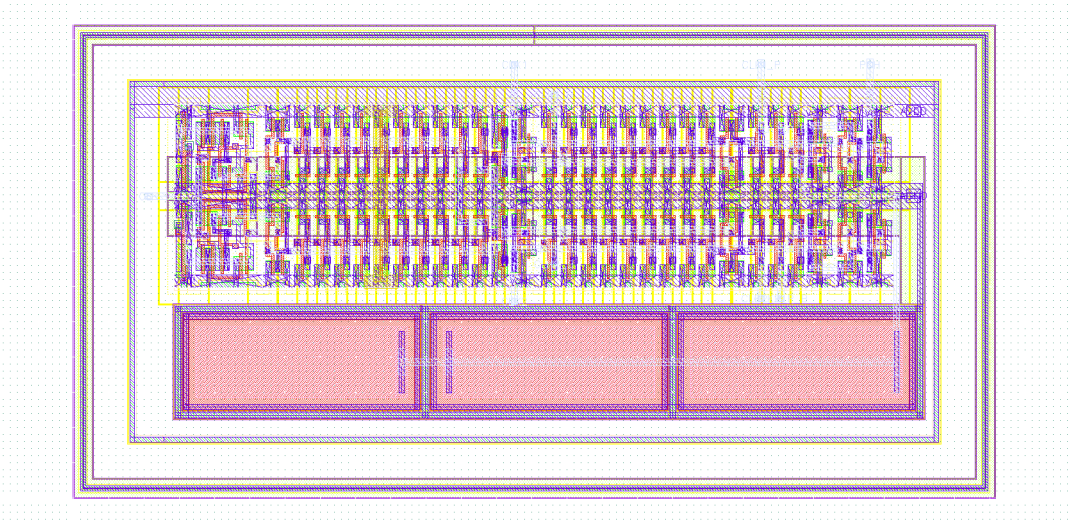

Figure 3.17 : Layout of Clock Generator

Final layout of the sigma delta modulator is given in the Figure 3.18 which matches well with the initial layout plan of the sigma delta modulator given in the Figure 3.5.

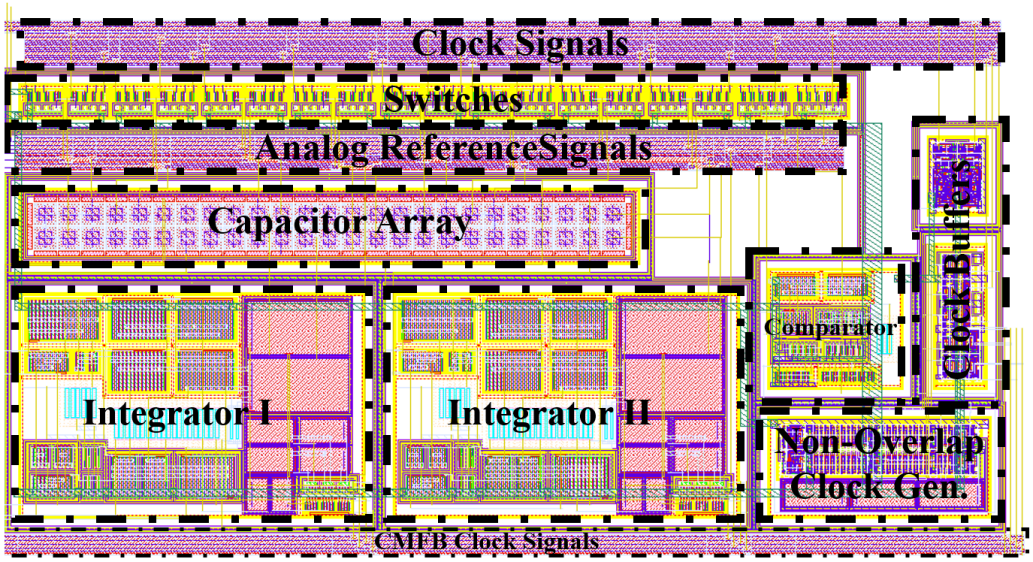

Figure 3.18 : Layout of Sigma Delta Modulator

3.6 Digital Core

Layout of digital block which contains counter, parallel to serial converter, I2C slave and control registers is automatically generated by using Cadence Encounter place and route tool. The script of place and route routine is given while the output layout of the script is shown in the Figure 3.19

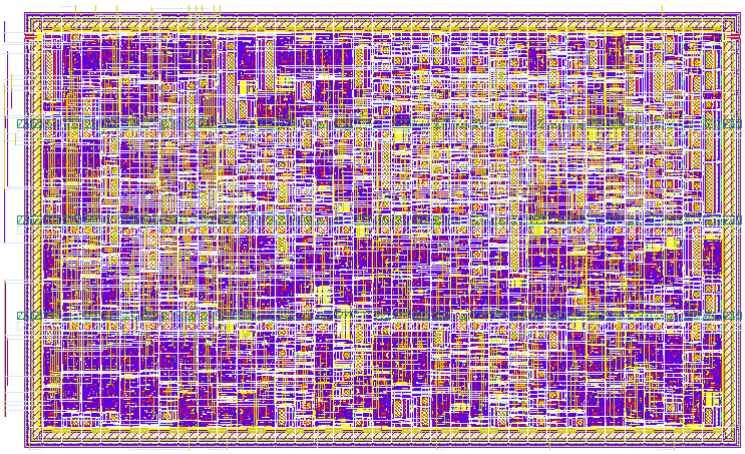

Figure 3.19 : Layout of Digital Block

3.7 Core Level

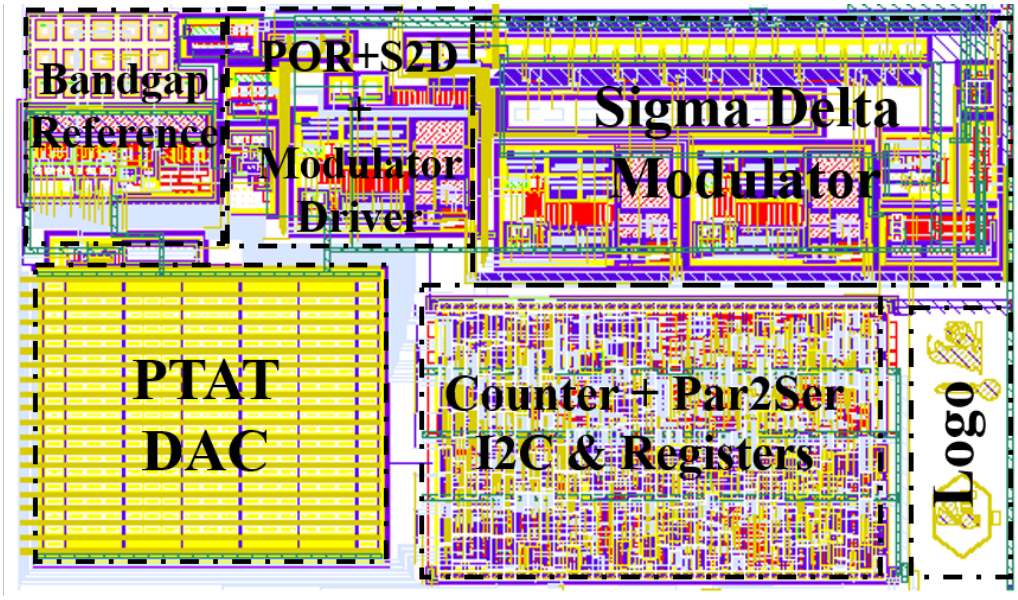

Figure 3.20 : Layout of Core

3.8 Pad Frame and Top Level

In the Figure 3.21 the top level layout of temperature to digital converter is given. The core of die is located in the middle while analog pads are at the top and digital pads are at the bottom side of the die. ITU VLSI LABs logo and a thermometer logo with tape-out date are also inserted to identify chip.

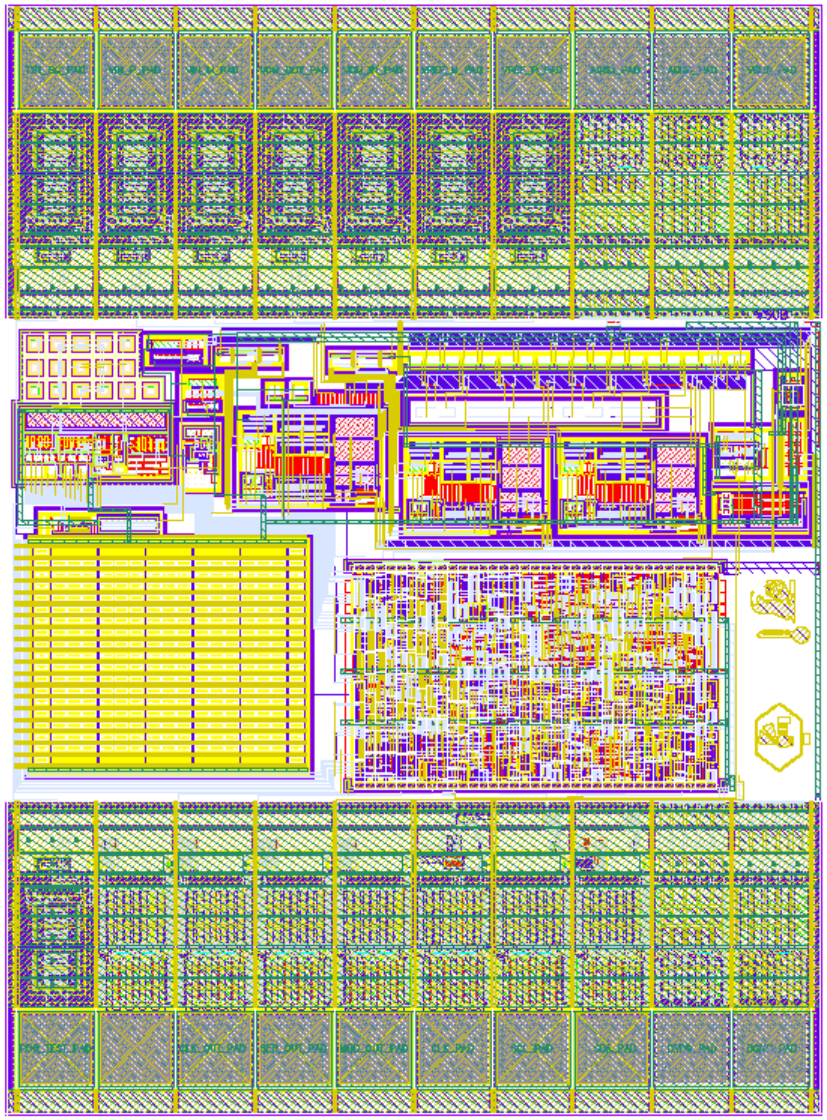

Figure 3.21 : Layout of Temperature to Digital Converter

The pads are inserted from standard analog and digital IO library of process AMSH35B4. ESD rating of each pad is 2kV. Supply and ground pads have the reverse ESD diodes and back to back diodes as well.

4. PACKAGING AND PCB BOARD DESIGN

4.1 Package Selection and Overview

The temperature to the digital converter chip is manufactured as Multi-Project Wafer (MPW) through Euro Practice IC Service with financial support of ITU VLSI Labs. The design is packaged with a 44 pins J-Leaded Ceramic Chip Carrier (JLCC) which is a square or rectangular surface-mount ceramic package that has J-formed leads around its periphery. JLCC is also common package type for A/D converters. Although typical JLCC's have lead counts that range from 20 to 84, Euro Practice offers JLCC package with a minimum 44 leads. The top and bottom views of a 44 pins JLCC IC package is shown in the Figure 4.1 (EESemi.com).

Figure 4.1 : The Bottom View of a 44 Pins JLCC IC Package

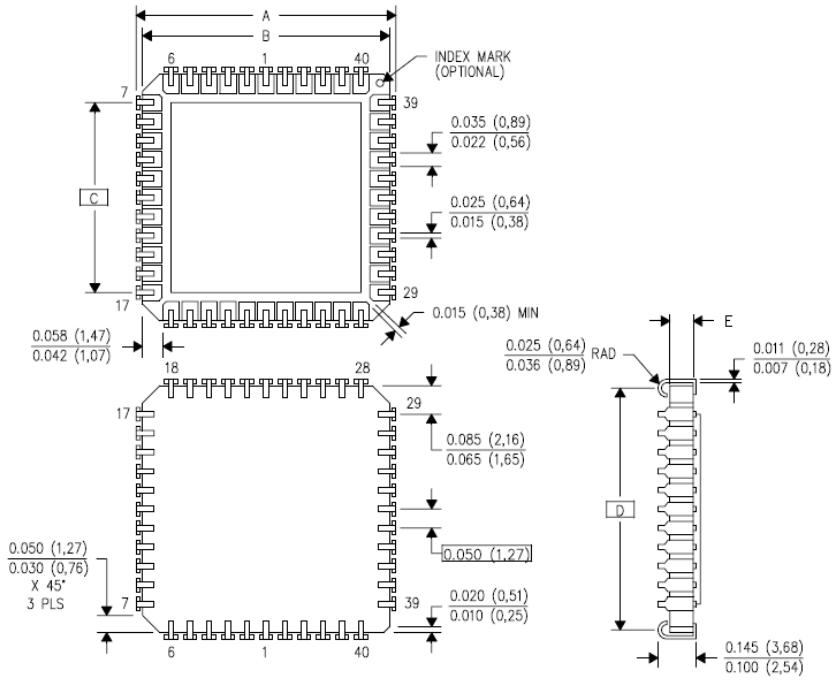

Figure 4.2 : The Footprint of a 44 Pins JLCC IC Package

A JLCC's lead pitch, distance between leads is typically 50 mils which is 1.27 mm. The JLCC can either be directly soldered onto the PCB or operated using a socket. In this work it is planned to have direct soldering method. The footprint of a 44 pins JLCC IC package which summarize dimension of the package is given in the Figure 4.2 (Instruments, 2003). All the dimensions are in inches while the values in the parenthesis are in millimeters.

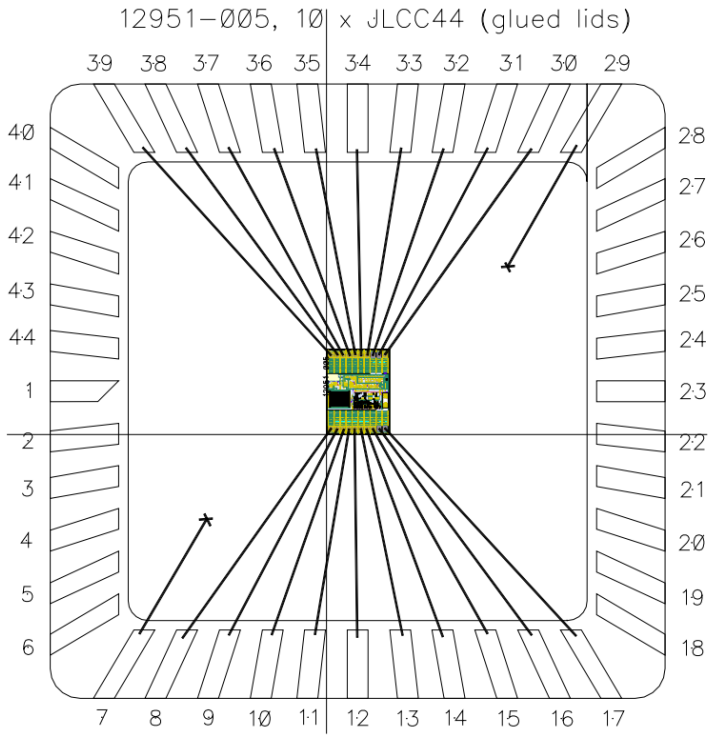

Figure 4.3 : Bonding Diagram of Temperature to Digital Converter

Table 4.1 : Pin Number and Pin Name

Pin Number	Pin Name	Pin Number	Pin Name
1-6	No Connect	29	Down Bond
7	Down Bond	30	VSUB
8	POR_TEST	31	AGND
9	Reserved	32	AVDD
10	CLK_OUT	33	VREF_P
11	SER_OUT	34	VREF_M
12	MOD_OUT	35	VCM_IN
13	CLK	36	VCM_OUT
14	SCL	37	VIN_M
15	SDA	38	VIN_P
16	DVDD	39	TST_BG
17	DGND	40 - 44	No Connect
18 - 28	No Connect	-	-

Bonding diagram for temperature to digital converter is shown in the Figure 4.3 while the pin numbers and names is given in the Table 4.1.

Temperature to digital converter is also delivered as die form without package. The die photo shown in the Figure 4.4 is taken in the ITU Nanotechnology Laboratory. Sub-blocks of the system are also noted in the photo.

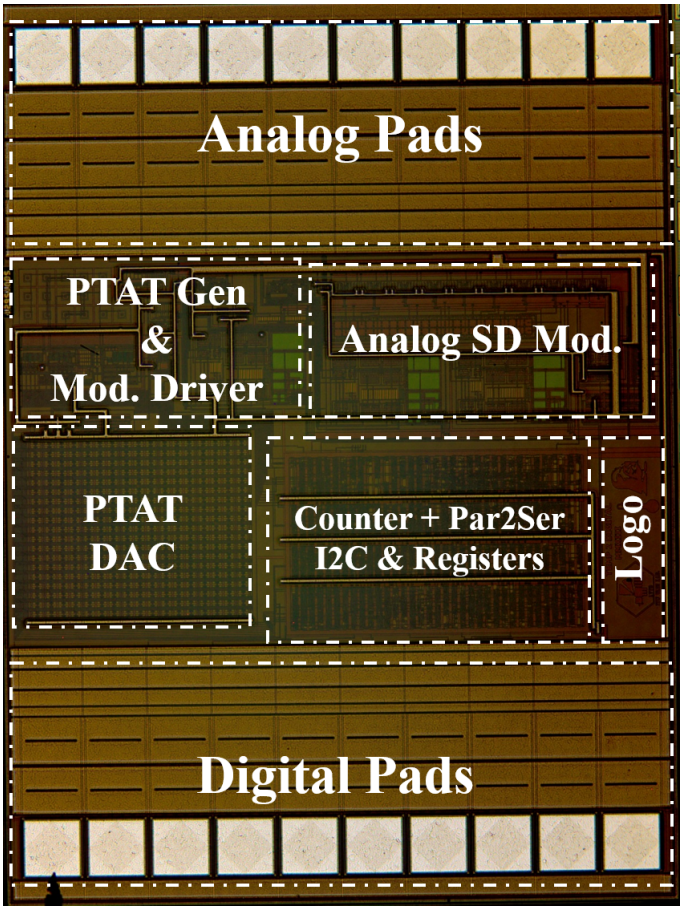

Figure 4.4 : Die Photo of Temperature to Digital Converter

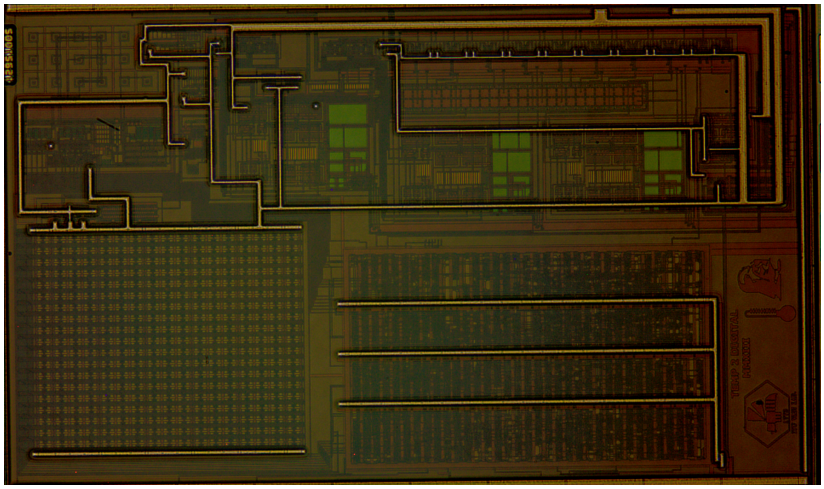

Figure 4.5 : Core Die Photo

4.2 PCB Board Design

In this section schematic and layout design of the evaluation board of the temperature to digital converter is explained in detailed. Firstly selected ICs and passive components for board design along side with connectors and headers are examined for their purpose and performance.

4.2.1 Component selection

In this section choice of component of the test PCB board is explained with design consideration and performance of components.

First consideration is supply voltages. There are two supply need to be provide for the temperature to digital converter. First one is AVDD which is 3.3V supply voltage for analog blocks in where the second is DVDD which is again 3.3V supply voltage for digital block in the die. To minimize coupling between AVDD and DVDD they need to be supplied separately. It is planned to have both supplies can be provided to board directly via a test point from a power supply instrument. In that case supply voltages would be noisy which is not a problem for digital supply DVDD but serious problem for analog supply AVDD

It is decided to use two different low dropout regulators (LDOs) for supply voltages. In this way both supply voltages would be clean by using generally good PSRR performance of LDOs and analog supply and digital supply can be isolated. This method also provide to use a single power supply instrument and minimize the effort of measurement setup.

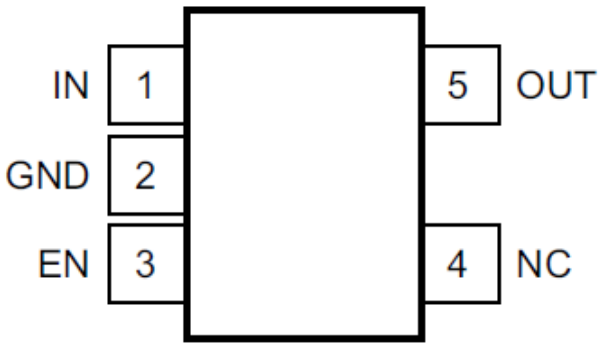

Figure 4.6 : Pin Configuration of TLV713

The LDO for analog supply AVDD is chosen as TLV713 from Texas Instruments. TLV713 offers stable operation with or without input and output capacitors while has an output voltage of 3.3V with %1 accuracy and input voltage range 1.4V to 5.5V and high PSSR, 65dB at 1Khz. In the Figure 4.6 the pin configuration of TLV713 is shown while pin description is given below.(*Capacitor-Free, 150-mA, Low-Dropout Regulator with Foldback Current Limit for Portable Devices*, 2015).

- Pin 1 - IN: Input pin.
- Pin 2 - GND: Ground pin.
- Pin 3 - EN: Enable pin.
- Pin 4 - NC: No connection.
- Pin 5 - OUT: Regulated output voltage pin.
- Thermal Pad : Need to be connected to GND pin for improved thermal performance.

Before choosing the LDO for digital supply DVDD, there is one more IC needs to be supplied which is an oscillator for the system clock of 1 MHz. To drive CLK input of the temperature to digital converter it is decided to use a square wave oscillator to eliminate frequency generator instrument and simplify measurement setup. But to be safe CLK input of the die can be also driven through a pin header. Two options is reconfigurable and this method is explained in detailed in the following section.

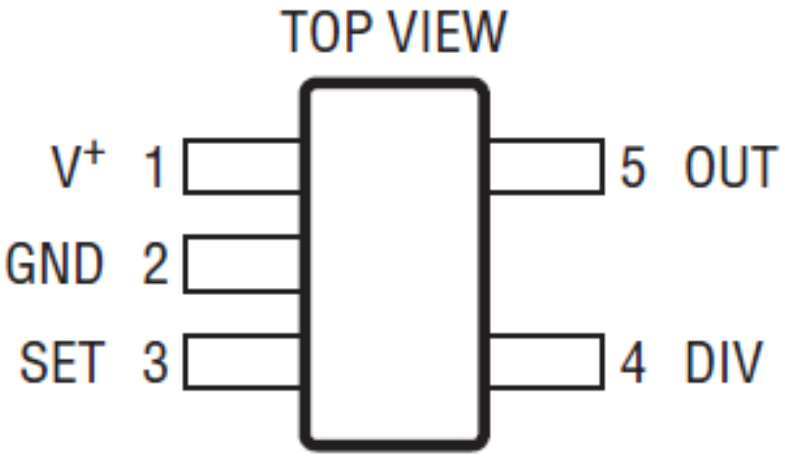

Figure 4.7 : Pin Configuration of LTC6900

The oscillator is chosen as LTC6900 from Linear Technology which is low power, 1kHz to 20Mhz resistor set oscillator. In the Figure 4.7 the pin configuration of LTC6900 is shown while pin descriptions are given below (*Low Power, 1kHz to 20MHz Resistor Set SOT-23 Oscillator*, 2002).

LTC6900 has following features; frequency error $\leq 2\%$ Max, 5kHz to 10MHz in the temperature range of 0C to 70C, $\pm 40 ppm/C$ temperature stability, $0.04\%/V$ supply stability, $50\% \pm 1\%$ duty cycle 1kHz to 2MHz and $50\% \pm 5\%$ duty cycle 2MHz to 10MHz and it operates from a single 2.7V to 5.5V supply.

- Pin 1 - V^+ : Supply Voltage $(2.7V \leq V^+ \leq 5.5V)$.
- Pin 2 - GND: Ground.
- Pin 3 - SET: Frequency-Setting Resistor Input.
- Pin 4 - DIV: Divider-Setting Input
- Pin 5 - OUT: Oscillator Output.

Oscillator also needs a clean supply in the range of 2.7V - 5.5V in order to generate clean clock signal. Supply voltage of the oscillator needs to be 3.3V due to temperature converter die needs a clock signal which has a 3.3V rail.

As a result there need to be two separate 3.3V supplies for DVDD where one for the temperature to digital converter and the oscillator. To minimize the number of components on the board and keep the size of the board as small as possible it is decided to chose an LDO which has two 3.3V outputs.

The LDO for digital supply DVDD and supply voltage V^+ is chosen as TLV711 from Texas Instruments which is a dual, low power and low dropout regulator.

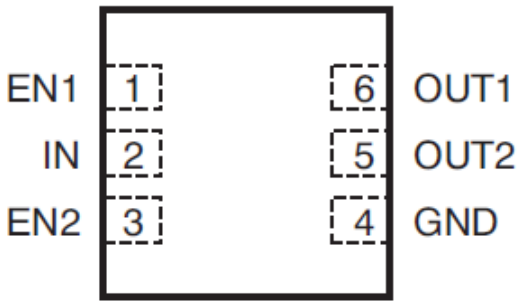

Figure 4.8 : Pin Configuration of TLV711

TLV711 offers stable operation with effective capacitance of 0.1uF while has two output voltages of 3.3V with %2 accuracy over temperature and input voltage range of 2V to 5.5V and high PSSR, 70dB at 1Khz. In the Figure 4.8 the pin configuration of TLV711 is shown while pin descriptions are given below. (*Dual, 200mA, Low-Iq, Low-Dropout Regulator for Portable Devices*, 2010).

- Pin 1 - EN1: Enable pin for regulator 1.
- Pin 2 - IN: Input pin.
- Pin 3 - EN2: Enable pin for regulator 2.
- Pin 4 - GND: Ground pin.
- Pin 5 - OUT2: Regulated output voltage pin
- Pin 6 - OUT1: Regulated output voltage pin

Board needs three analog reference voltages VREF_P, VREF_M and VCM which are critical for the performance of the system. Therefore they need to be noiseless as possible which is not possible with standard power supply instruments. They need to be supplied from a high end noiseless power supply generator or from a regulator. It is planned to have both option on the board which is configurable and LDO mode is default on the board. VREF_P and VREF_M are generated again with a dual LDO ADP225 from Analog Devices which is low noise, high PSRR voltage regulator.

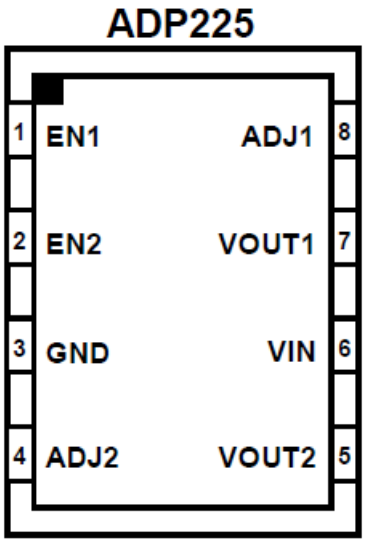

Figure 4.9 : Pin Configuration of ADP225

ADP225 offers two adjustable output voltages in the range of 0.5V to 5.0V, %1 accuracy and input voltage range of 2.5V to 5.5V. ADP225 has high PSSR values of 70dB, 60dB and 40 dB at 10Khz, 100kHz and 1Mhz respectively while having low noise performance; 27 uV rms at VOUT = 1.2V, 50 uV rms at VOUT = 2.8 V. In the Figure 4.9 the pin configuration of ADP225 is shown while pin descriptions are given below (*Dual, 300 mA Output, Low Noise, High PSRR Voltage Regulators*, 2014).

- Pin 1 - EN1: Enable input for the first regulator.
- Pin 2 - EN2: Enable input for the second regulator.
- Pin 3 - GND: Ground pin.
- Pin 4 - ADJ2: Adjust pin for VOUT2.
- Pin 5 - VOUT2: Regulated output voltage.
- Pin 6 - IN: Regulator input supply.
- Pin 7 - ADJ1: Adjust pin for VOUT1.
- Pin 8 - VOUT1: Regulated output voltage.

There are also need of passive components such as resistors and capacitors needed for functionality and performance of selected integrated circuit components. For example to set frequency of oscillator the precise thin film metal resistor is needed. Additionally set the correct output voltage for LDO generating analog reference voltages, resistor dividers are needed. Finally capacitors are needed at the both input and output of LDOs for a stable operation or bypassing LDOs to achieve better noise performance. All passive components are chosen as 0603 (1608 metric) surface mount device (SMD) packaged. Their values are determined in the following section.

4.2.2 Schematic design

In this section schematic design of PCB board is explained with considering to achieve best performance with most simplicity and instructions at the datasheets of chosen IC components. Schematic design of LDOs for supply voltages and reference voltages and oscillator are described with their interaction with related pins of temperature to digital converter. The system monitor test points, header pins and SMA connector pins are also included. The schematic design of the PCB is done at Eagle PCB Design with the version of 7.6.0 from CadSoft.

For the analog supply LDO TLV713, datasheet states there is no need for capacitor at the both input and output pins for stability. However it is recommended that a 0.1uF or larger 1uF X5R X7R type ceramic capacitor at the input improves dynamic response. It also indicates that it is good analog design practice to connect a 0.1uF to 1uF capacitor from IN pin to GND pin of TLV713. This input capacitor enhances transient response, input ripple and PSRR (*Capacitor-Free, 150-mA, Low-Dropout Regulator with Foldback Current Limit for Portable Devices*, 2015). So two X5R 1uF capacitors are connected from IN to GND and OUT to GND pins of TLV713.

In the datasheet of TLV711 which is a dual LDO for DVDD and supply of oscillator, it states that minimum 0.1uF capacitor is needed for stability. However it is also recommended that to have a 1uF X5R or X7R type ceramic capacitor at the input to be safe after consideration of variation in value of capacitor. It is again recommended to connect a 0.1uF to 1uF capacitor from IN pin to GND pin to enhances transient response, input ripple and PSRR (*Dual, 200mA, Low-Iq, Low-Dropout Regulator for Portable Devices*, 2010). So three X5R 1uF capacitors are connected from IN to GND, OUT1 to GND and OUT2 to GND pins of TLV711.

In the datasheet of ADP225 which is a dual LDO for reference voltages $VREF\_P$ and $VREF\_P$, it states that minimum 0.7uF capacitor with en ESR of 1 ohm or less is needed for stability. It is also recommended to connect a 1uF capacitor from VIN pin to GND pin. So three X5R 1uF capacitors are connected from VIN to GND, VOUT1 to GND and VOUT2 to GND pins of TLV711.

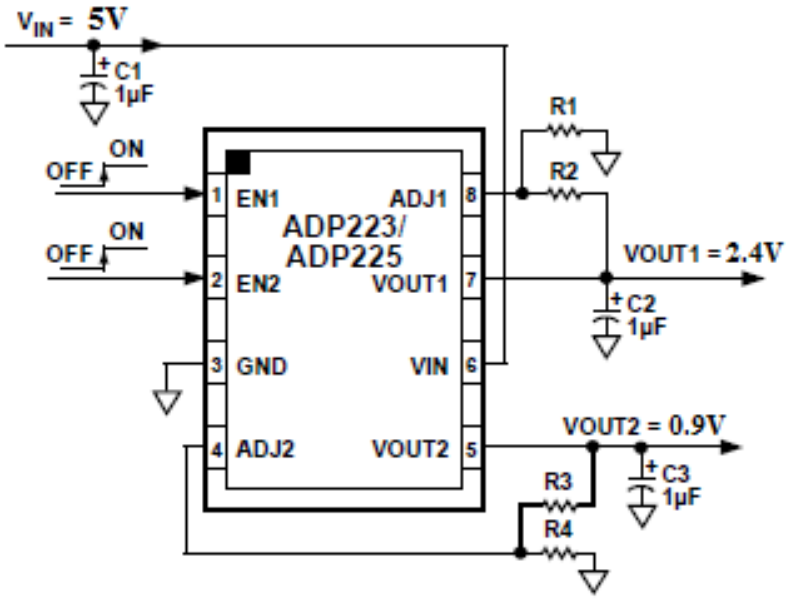

Figure 4.10 : Reference Voltage LDO ADP225 Adjustable Operation

The two output voltages are adjustable in the range of 0.5V and 5V as indicated earlier and these two output voltages can be set according to following equations.

$$\begin{aligned} V_{OUT1} &= 0.5V(1+R2/R1) \\ V_{OUT2} &= 0.5V(1+R3/R4) \end{aligned} \tag{4.1}$$

The value of R1 and R4 should be less than 200 kohm to minimize errors in the output voltage caused by the ADJx pin input current. For example, when R1 and R2 each equal 200 kohm, the output voltage is 1.0 V. The output voltage error introduced by the ADJx pin input current is 2 mV or 0.20%, assuming a typical ADJx pin input current of 10 nA at 25C (*Dual, 300 mA Output, Low Noise, High PSRR Voltage Regulators*, 2014).

Temperature to digital converter needs VREF_P = 2.4V and VREF_M = 0.9V. VOUT1 pin of ADP225 is used for generating VREF_P = 2.4V while VOUT2 pin is used for VREF_M = 0.9V. To calculate required resistors equation (4.1) need to be solved for the required voltages.

$$\begin{aligned} 0.9V &= 0.5V(1+R2/R1) \rightarrow R2/R1 = 0.8 \\ 2.4V &= 0.5V(1+R3/R4) \rightarrow R3/R4 = 3.8 \end{aligned} \tag{4.2}$$

To have non fractional number values for resistors R1 and R4 are chosen as 50kohm. In this case R3 is 190kohm and R2 is 40kohm.

Common mode voltage VCM is generated from VREF_P and VREF_M voltages by connecting two high value 200k ohm resistors between these two voltages. Common node of resistors is used for VCM_IN and VCM_OUT pins. VCM voltage can be expressed in equation (4.3). It is also decoupled with 10uF capacitor to ground.

$$VCM = (VREF\_P + VREF\_M)/2 \tag{4.3}$$

For VREF_P = 2.4V and VREF_M = 0.9V, VCM is found as 1.65V which is AVDD/2.

$$VCM = (2.4 + 0.9)/2 = 1.65V \tag{4.4}$$

For the oscillator LTC6900 which is used for system clock datasheet states that supply pin V^+ should be bypassed by 0.1uF capacitor to ground plane. It also indicates that a precision thin metal film resistor with a value between 10kohm to 2Mohm for best performance. DIV pin is a three state pin and determines the N value in the equation (4.5). This pin should be tied to ground for divider value of 1 or tied to V^+ pin fir divider value of 100. Floating DIV pin divides the oscillator by 10 (*Low Power, 1kHz to 20MHz Resistor Set SOT-23 Oscillator*, 2002).

$$f_{osc} = 10MHz \cdot \left(\frac{20k}{N \cdot R_{SET}} \right) \tag{4.5}$$

System needs 1MHz clock input. It is planned to have a jumper for DIV pin to control divider value with a default value of ground means divider is 1. If the equation (4.5) is solved for $N = 1$, R_{SET} is found as 200kohm.

$$1MHz = 10MHz \cdot \left(\frac{20k}{1 \cdot R_{SET}} \right) \rightarrow R_{SET} = 200kohm \tag{4.6}$$

A zero ohm resistor is also placed between CLK_IN pin of the temperature to digital converter and output pin of the oscillator. CLK_IN is also connected to a pin header to monitor clock signal and apply external clock with removed zero ohm at the output pin of the oscillator.

I2C data and clock signals SDA and SCL are routed to pin headers with 3.3k pull-up resistors to DVDD. These pin headers are used for i2c communication to reconfigure registers in the temperature to digital converter.

MOD_OUT pin is connected to pin header to monitor modulator output directly. CLK_OUT and SER_OUT pins are connected both pin headers and SMA connectors. Temperature to digital conversion is measured by these two pins, it is planned to measure these signals by an oscilloscope via SMA cables.

POR_OUT pin and VBG_TST pin are again connected to two pin headers. These pin headers are used for monitoring internal POR signal indicating that digital is reset and VBG voltage which gives the information that reference circuit is up and running.

The full schematic of the designed PCB board is given in the Figure 4.11

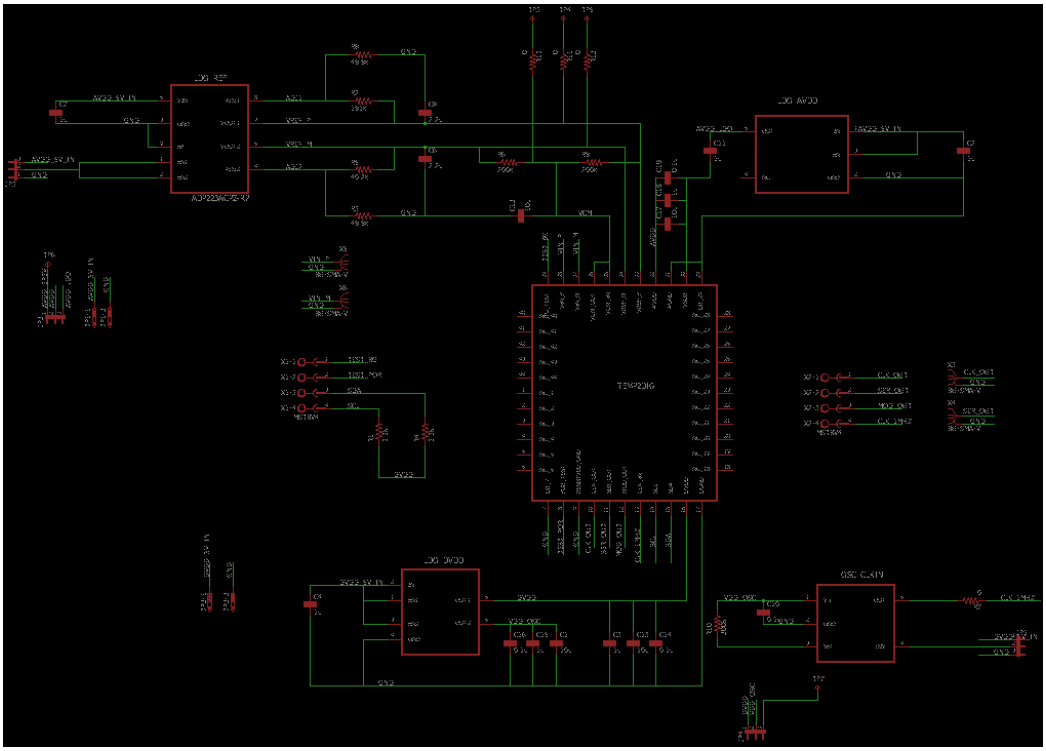

Figure 4.11 : PCB Schematic of Temperature to Digital Converter

In this section schematic design of PCB, considering performance and component datasheet recommendation, is explained in detailed. In the next section layout design of PCB is presented.

4.2.3 Layout design

Careful PCB layout design is important to minimize coupling between lines and enhance isolation in order to achieve best performance. There are five integrated circuit and several passive components on the board. In this section footprint of ICs and passive components are given. Then layout design of the board is explained with consideration of layout instruction indicated in datasheets of both ICs and passive components.

It would be convenient to start with analog supply LDO TLV713. The package type of TLV713 is 5 pins small outline transistor package (SOT23-5) which is shown in the Figure 4.12.

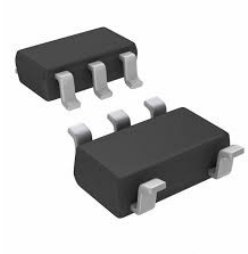

Figure 4.12 : Top and Bottom View of SOT23-5 Package

Footprint of SOT23-5 package is given in te Figure 4.13. All the lengths are in millimeters.

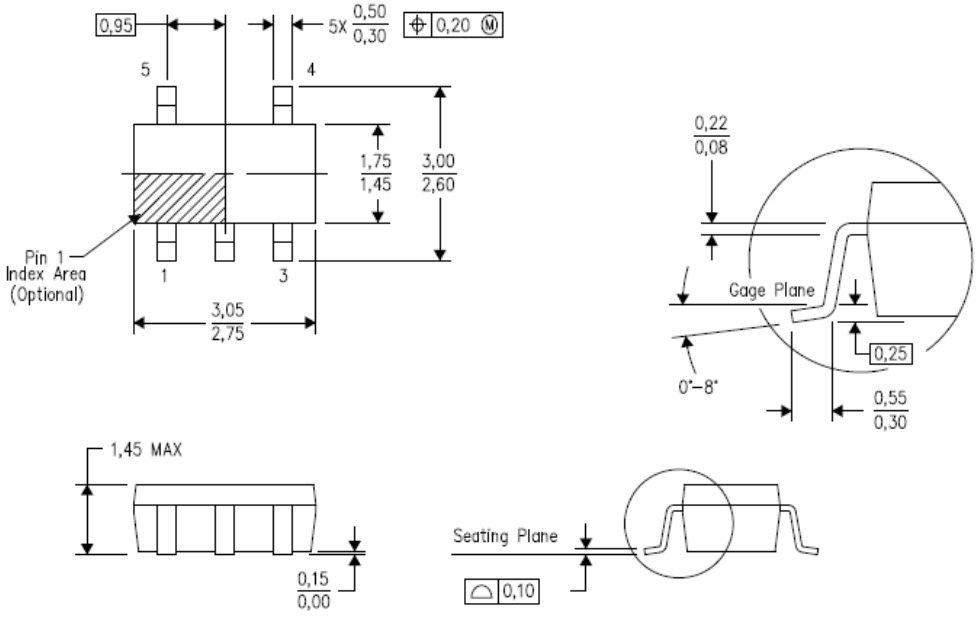

Figure 4.13 : Footprint of SOT23-5 Package

The package type of LDO TLV711 for DVDD and V_+ is 6 pins small outline non-leaded WSON-6 which is shown in the figure 4.14. W in the prefix stands for very very thin.

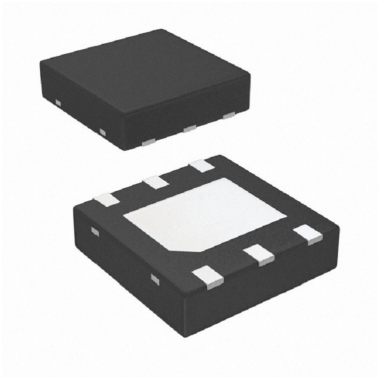

Figure 4.14 : Bottom and Top View of WSON-6 Package

Footprint of WSON-6 package is given in te Figure 4.13. All the lengths are in millimeters.

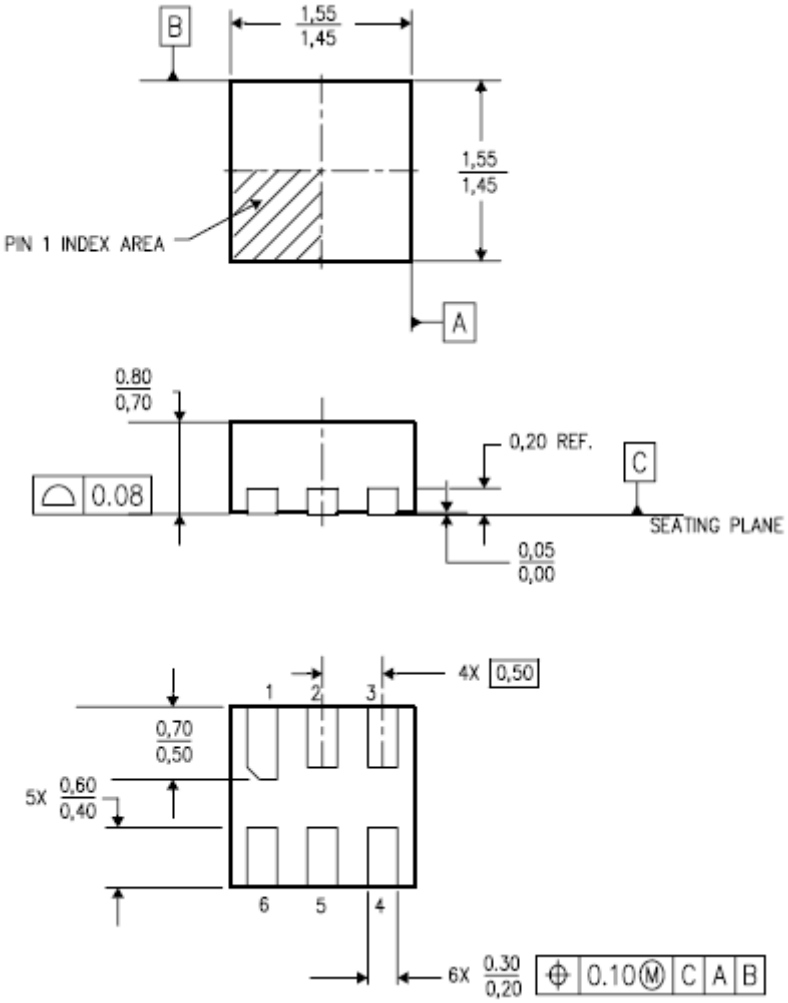

Figure 4.15 : Footprint of WSON-6 Package

The package type of LDO ADP225 for voltage reference signals is 8 pins lead frame chip scale package LFCSP-8 which is shown in the figure 4.16.

Figure 4.16 : Bottom and Top View of LFCSP-8 Package

Footprint of LFCSP-8 package is given in te Figure 4.15. All the lengths are in millimeters.

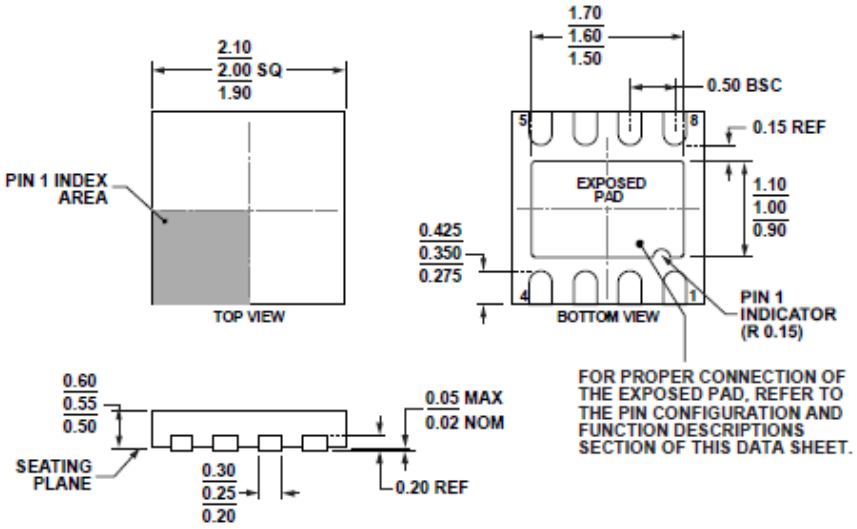

Figure 4.17 : Footprint of LFCSP-8 Package

The package type of oscilator LTC6900 for clock signal is again 5 pins small outline transistor package (SOT23-5) which is shown in the Figure 4.12 and the footprint in the Figure 4.13.

All the passive components capacitors and resistors are 0603 (1608 metric) surface mount device SMD packaged. Dimension of a 0603 SMD package is shown in the Figure 4.18.

Temperature to digital converter is placed at the center of layout. Analog domain parts such as AVDD LDO, reference LDO and passive components are placed at the top of board due to all analog inputs of the temperature to digital converter are located there.

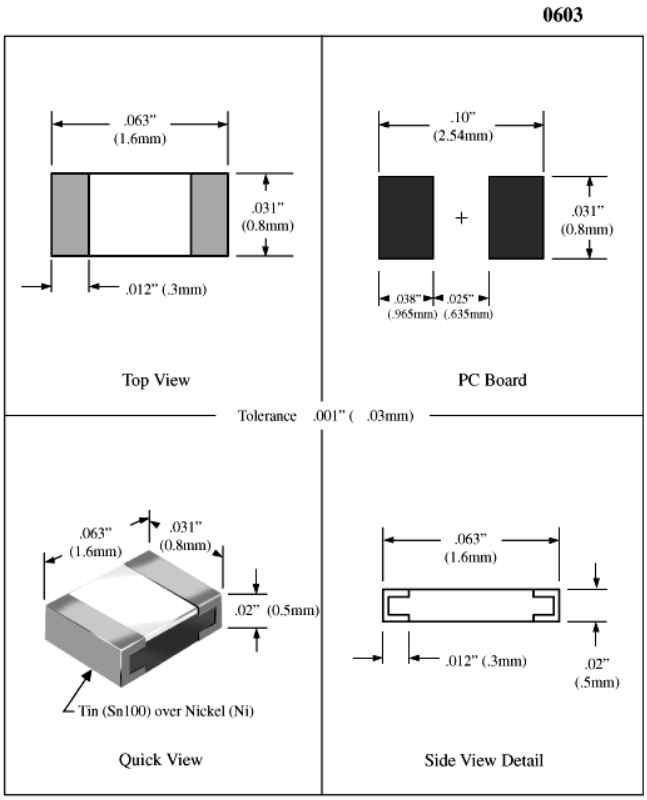

Figure 4.18 : Foot Print of 0603 SMD Package

Digital domain parts such as DVDD LDO and oscilsator are placed at the bottom of the layout again due to digital input of the temperature to digital converter are at the bottom.

AVDD LDO is placed very closed to AVDD pin. 1uF Xr5 ceramic capacitor is placed right at the output of AVDD LDO. Input pin and input capacitor of AVDD LDO is located at the upper right corner of the board and connected to the AVDD_5V test point where analog supply is applied to the board. Three decoupling capacitors 0.1uF, 1uF and 10uF are placed very close to AVDD pin of the temperature to digital converter. AVDD can be supplied either by LDO or test point AVDD_3p3V through a three point jumper which is located at the upper right corner.

VREF_P and VREF_M inputs are connected to VOUT1 and VOUT2 of reference LDO which is located at the upper center of the board. Resistor networks which adjust reference voltage levels and output capacitors are placed around the reference LDO and close as possible to the related pins. The both outputs of reference LDO can be disabled by a three point jumper at the upper center. In this case VREF_M and VREF_P reference voltages can be supplied to the chip by test points VREFM and VREFP which are located upper left side of the board.

VCM_IN and VCM_OUT pins are shorted. Common mode voltage is generated by connecting two high resistor, 200k ohm, between VREF_M and VREF_P. Common node of these resistor is common mode voltage and this voltage is decoupled to ground by 10uF X5R ceramic capacitor. It is again two resistors and one capacitor are placed near of the VCM pins. Common mode voltage pins of the temperature to digital converter can be driven from external supply through a test point at the upper left side of the layout.

VIN_M and VREF_P input pins of the temperature to digital converter are directly routed to the two SMA connector which are located at the upper left corner of the board. These two SMA connectors can be used to apply input signal directly to the input of the modulator to check performance of modulator itself. But there must be performed an i2c communication first to re-arrange inputs of the modulator.

TEST_BG pin is directly route to an header pin which is located middle right of the board to check the health of reference circuitry.

DVDD LDO is placed very closed to DVDD pin. 1uF X5R ceramic capacitor is placed right at the output of AVDD LDO. Input pin and input capacitor of DVDD LDO is located at the lower left corner of the board and connected to the DVDD_5V test point where digital supply is applied to the board. Three decoupling capacitors 0.1uF, 1uF and 10uF are placed very close to DVDD pin of the temperature to digital converter. DVDD can be supplied either by LDO or test point DVDD_3p3V through a three point jumper which is located at the lower right corner.

I2C clock and data signals SCL and SDA are routed to the header pins which are located middle left of the board with 3.3k pull-up resistors.

CLK_IN pin is connected to oscillator output with 0 ohm SMD resistor which is located at the lower right corner of the board to minimize clock coupling to other signals. CLK_IN signal also is routed to the pin header located at the bottom middle of the board. This header can bu used for monitoring input clock signal or applying external clock with removing 0 ohm resistor at the output of the oscillator.

MOD_OUT pin is routed to the header pin located at the bottom middle of the board. This pin can be used for observe the output of the modulator directly.

SER_OUT pin is routed to both the header pin located at the bottom middle and the SMA connector located at the lower left corner of the board. SMA connector is used to measure serial digital data with an oscilloscope or logic analyzer.

CLK_OUT pin is routed to both the header pin located at the bottom middle and the SMA connector located at the lower left corner of the board. SMA connector is used to measure clock of the serial to parallel conversion digital block with an oscilloscope or logic analyzer.

POR_OUT pin is directly routed to header pin which is placed middle left side of the board. This header pin can be used to monitor the POR signal which indicates digital circuit is reset successfully.

After placing all components and routing all signals rest of the board is filled by copper to form a ground plane. Both top plate and bottom plate of the board are formed as ground planes. To strengthen ground connection via arrays are placed all over the board where there is no signal routing. In the figure 4.19 final board layout is shown. After completing layout of the board it is need to be converted gerber files. The gerber

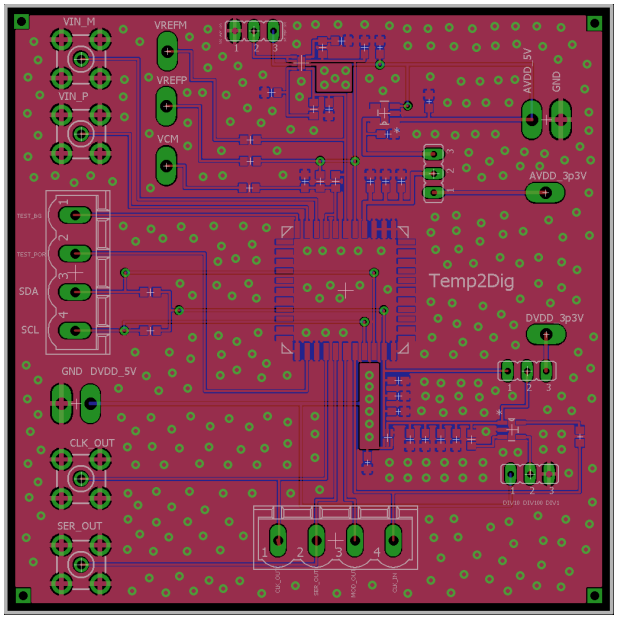

Figure 4.19 : Layout of PCB Board

format is an open ASCII vector format for 2D binary images. Gerber files are global file which are used in PCB manufacturing. There are a lot of drawing tools and each tool has its own file type which is unmanageable by manufacturers. That is why global gerber files are used.

To manufacture a PCB there need to be several gerber files according PCB design. The temperature to digital board is designed as two sided PCB. So the following files are needed for manufacturing.

- Solder Mask: is a thin lacquer-like layer of polymer that is usually applied to the copper traces of a printed circuit board (PCB) for protection against oxidation and to prevent solder bridges from forming between closely spaced solder pads.
- Copper: is the layer indicating all the copper area on the board including component pads, traces, vias, pads and ground planes.
- Silkscreen: is the print layer on soldermask includes component names, values, texts or logos.
- Drill file: is the file contains diameter, x and y coordinates of vias and pads on the PCB.
- Paste: defines the area of solder paste for soldering the components

In the Figure 4.20 top solder mask layer is shown of designed board. As seen in the figure at this layer only pads of ICs and components. This layer shows where copper is left open on the board.

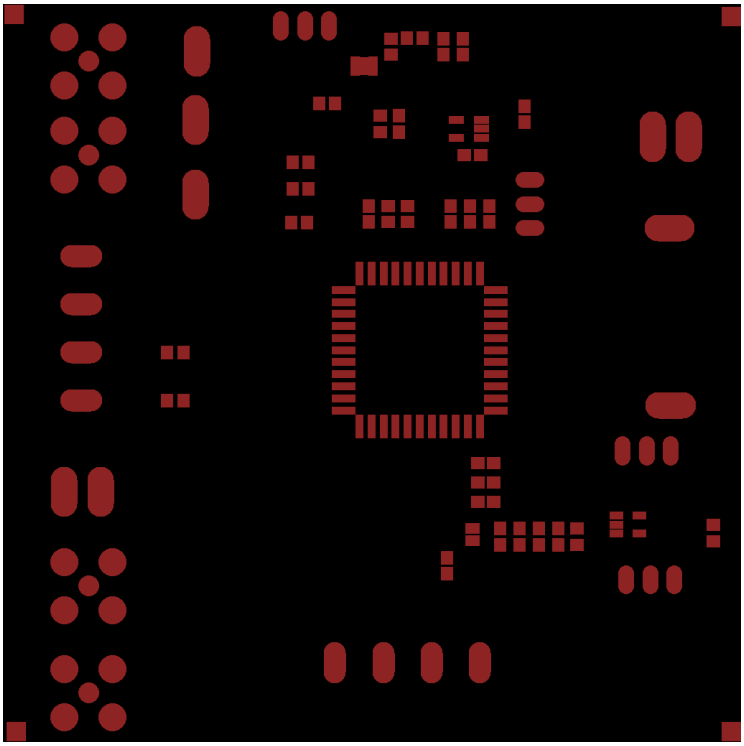

Figure 4.20 : Top Soldermask Layer of PCB Board

In the Figure 4.21 top copper layer is shown of designed board. As seen in the figure at this layer all the copper areas including pads of ICs and components, traces and ground planes.

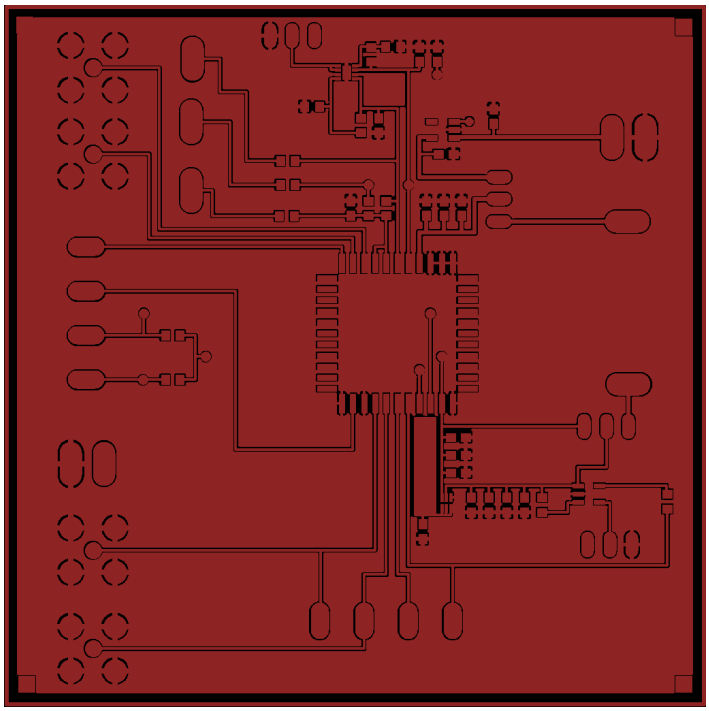

Figure 4.21 : Top Copper Layer of PCB Board

In the Figure 4.22 top silkscreen layer is shown of designed board. As seen in the figure at this layer texts and some indicator of components are presented.

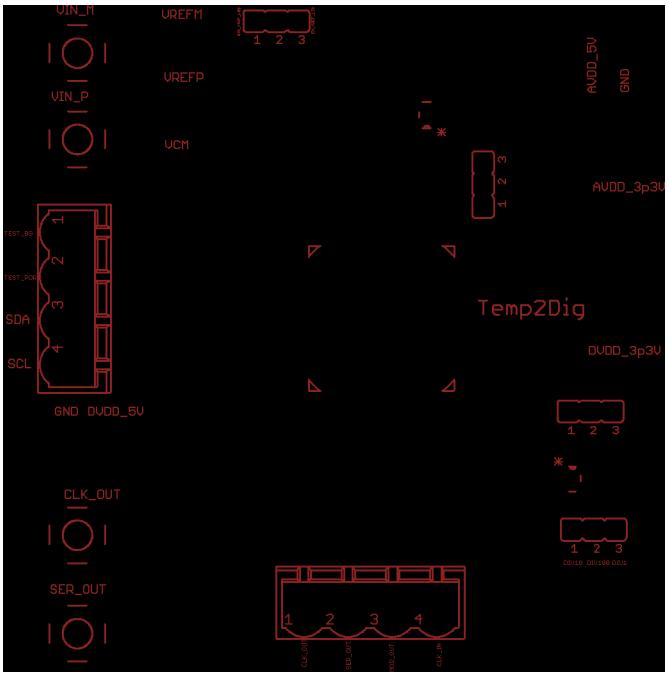

Figure 4.22 : Silkscreen Layer of PCB Board

In the Figure 4.23 bottom solder mask layer is shown of designed board. As seen in the figure at this there are only pads of test points, headers and SMA connectors due to there is no component at the bottom side.

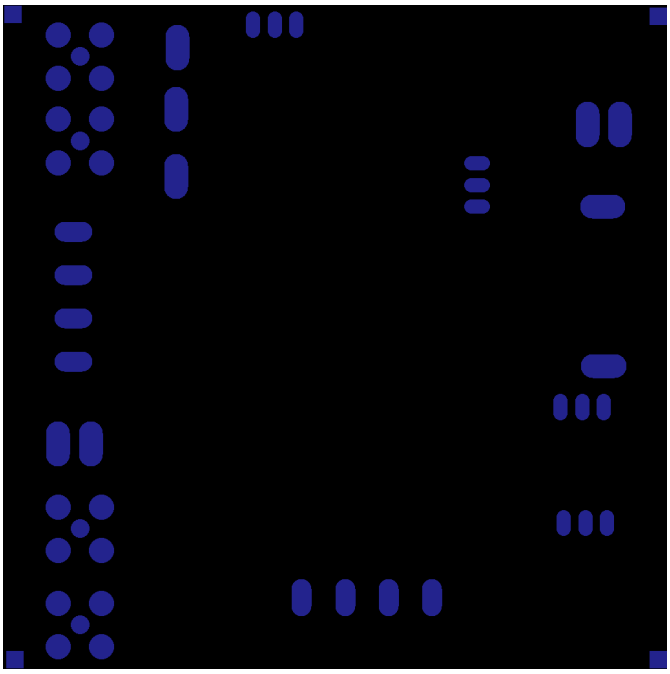

Figure 4.23 : Bottom Soldermask Layer of PCB Board

In the Figure 4.24 bottom copper layer is shown of designed board. As seen in the figure, there are only two VDD planes and three traces at the bottom copper. The rest is ground plane.

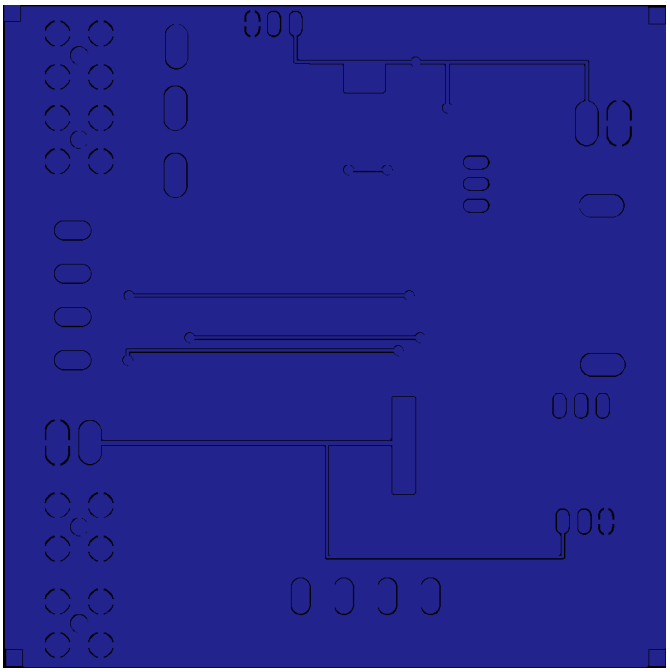

Figure 4.24 : Bottom Copper Layer of PCB Board

There are no texts or component indicators at the bottom, so there is no need for bottom silkscreen layer.

In the Figure 4.25 manufactured PCB board is shown while final PCB after placing components is given in the Figure 4.26.

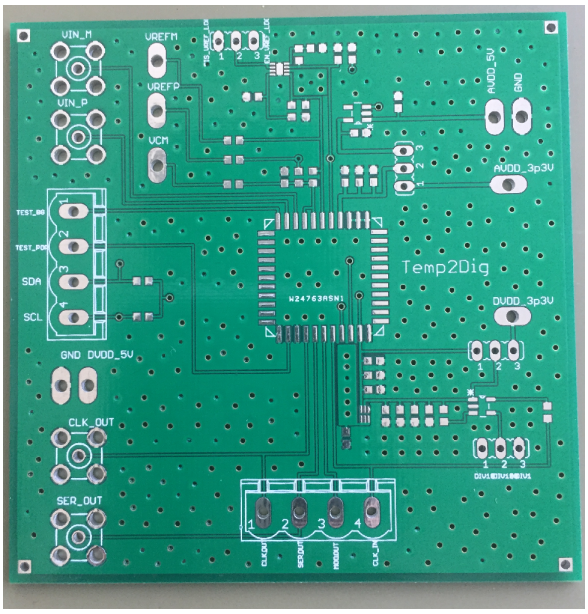

Figure 4.25 : Manufactured PCB

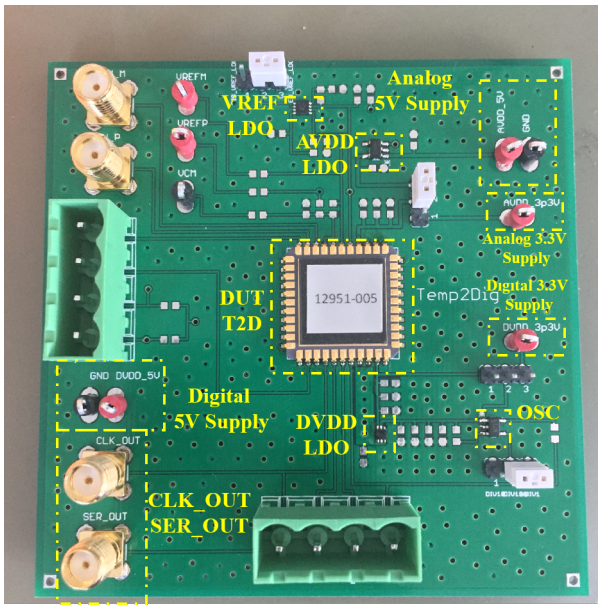

Figure 4.26 : PCB with Components

In the following section measurement setup and measurement results which are using this PCB board will be given.

5. MEASUREMENT OF TEMPERATURE TO DIGITAL CONVERTER

5.1 Measurement Setup

In this section measurement setup is explained with instruments in the setup. Planned setup is shown in the Figure 5.1. E3648A which is a dual output power supply from Keysight Technologies is used for supply voltages AVDD and DVDD while MSO9404A mixed signal oscilloscope which has 4GHz bandwidth and 20GSa/s sample rate from Agilent Technologies is used for monitoring CLK_OUT and SER_OUT pins. Arduino Mega 2560 Rev2 board is used for I2C communication with commands sent from a computer through serial port. Finally for temperature sweeping an Espec temperature chamber is used.

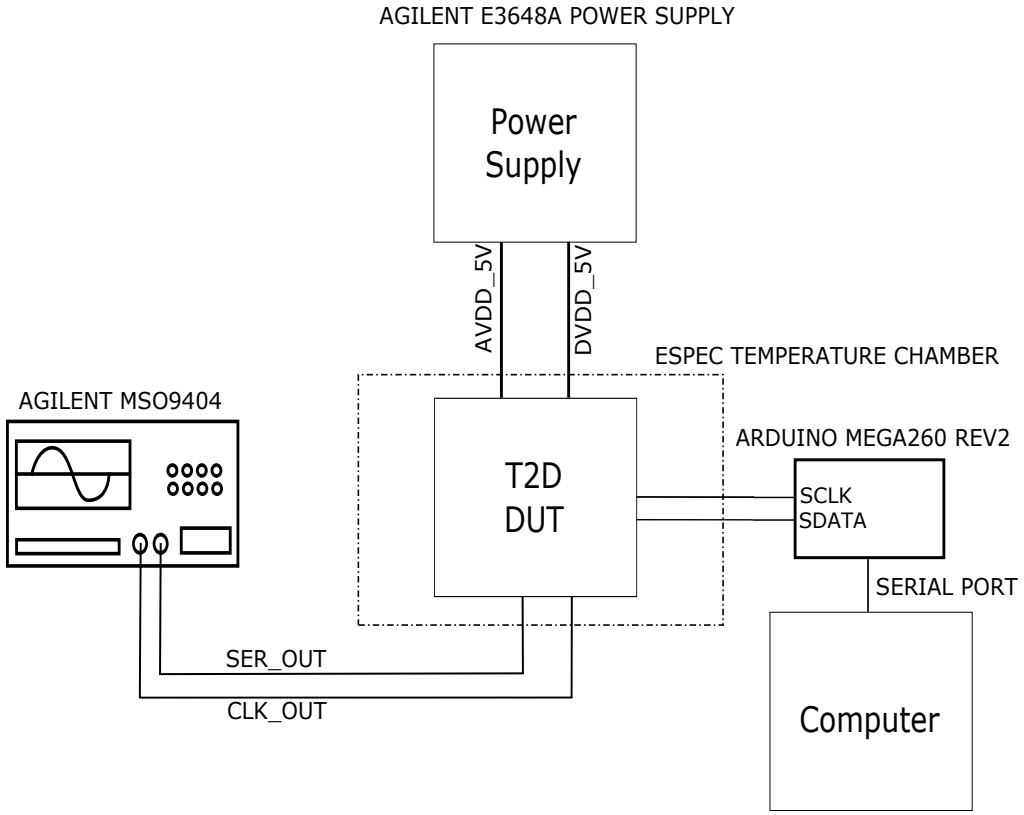

Figure 5.1 : Measurement Setup Block Diagram

5.2 DC Measurements and I2C Communication

Before starting temperature sweeping, DC voltages such as supply voltages AVDD and DVDD, analog reference voltages VREF_P, VREF_M and VCM are measured with a multimeter along with test points such as VBG_TST and POR_TST to ensure the health of the board. Measured DC voltages are given in the Table 5.1.

Table 5.1 : DC Measurement Results

Parameter	Value [V]	Parameter	Value [V]
AVDD	3.3	DVDD	3.3
VREF_P	2.4	VREF_M	0.9
VCM_IN	1.65	VCM_OUT	1.65
VBG_TST	1.2	POR_TST	3.3

Secondly default register values are read from chip to check the registers are settled to correct values after POR. I2C communication setup is given in the Figure 5.2.

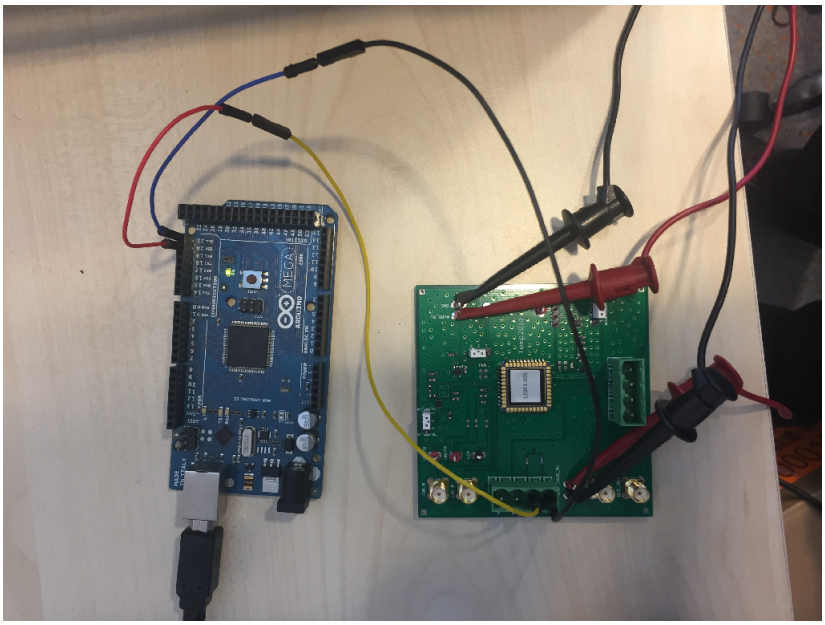

Figure 5.2 : I2C Communication Setup

Default values are read correctly as given in the Figure 5.2.

Table 5.2 : Default Register Values

Address	Value [Hex]	Address	Value [Hex]
0	0x04	1	0x02
2	0xF1	3	0xFF
4	0x3F	5	0x03

5.3 Transient Measurements Over Temperature

After verifying DC operation points and I2C communication measurement setup shown in the Figure 5.3 is constructed according to block diagram in the Figure 5.1.

Figure 5.3 : Measurement Setup

Measurements are taken for every 5C steps in the range of -40C to 85C. First temperature is set to desired value and wait for 5 minutes for settling. Then 10 measurements are taken at every temperature value. This process is repeated for every 5C up to 85C.

In the Figure 5.4 measurement result for $K_{DAC} = 10$ and 12 bit counter is given with ideal voltage curve. It is seen that there is an offset between measured and ideal curves. There is also some fluctuation on measured curve. In the Figure 5.5 error between measured and ideal curve is given which shows offset error and fluctuation.

Fluctuation on the measurement is a result of chopper operation at the modulator driver. To eliminate this behaviour more samples must be taken at every temperature value. But this means a lot of measurement time. So the chopper stabilization at the modulator driver is turned off and measurement is repeated.

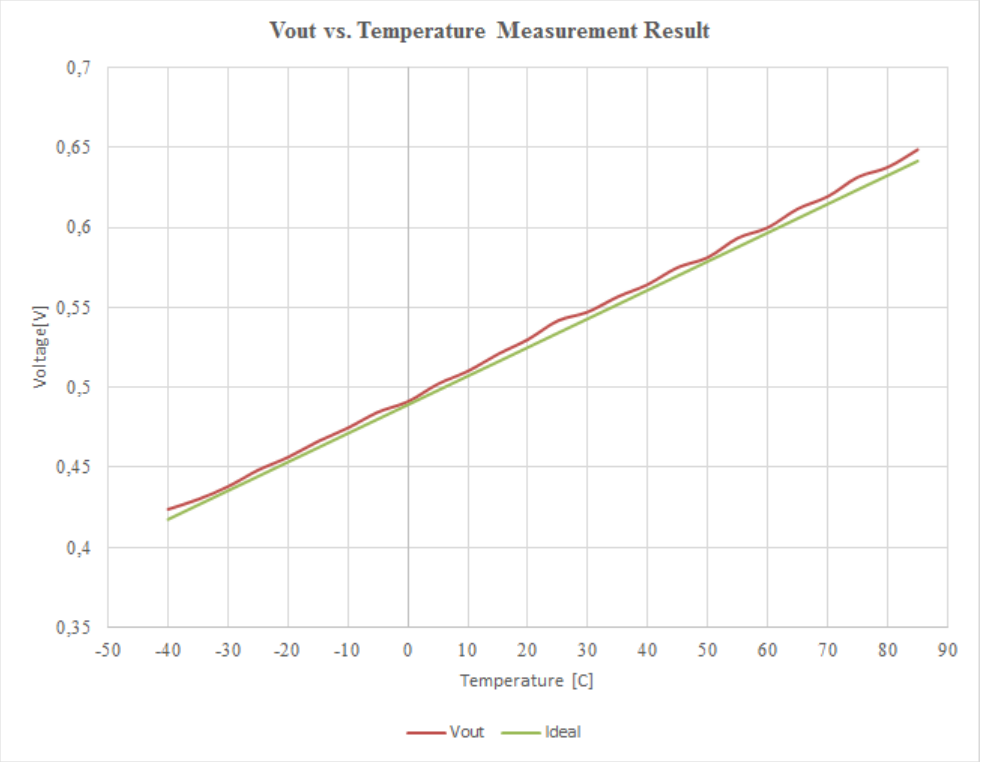

Figure 5.4 : Measurement Result for $K_{DAC} = 10$

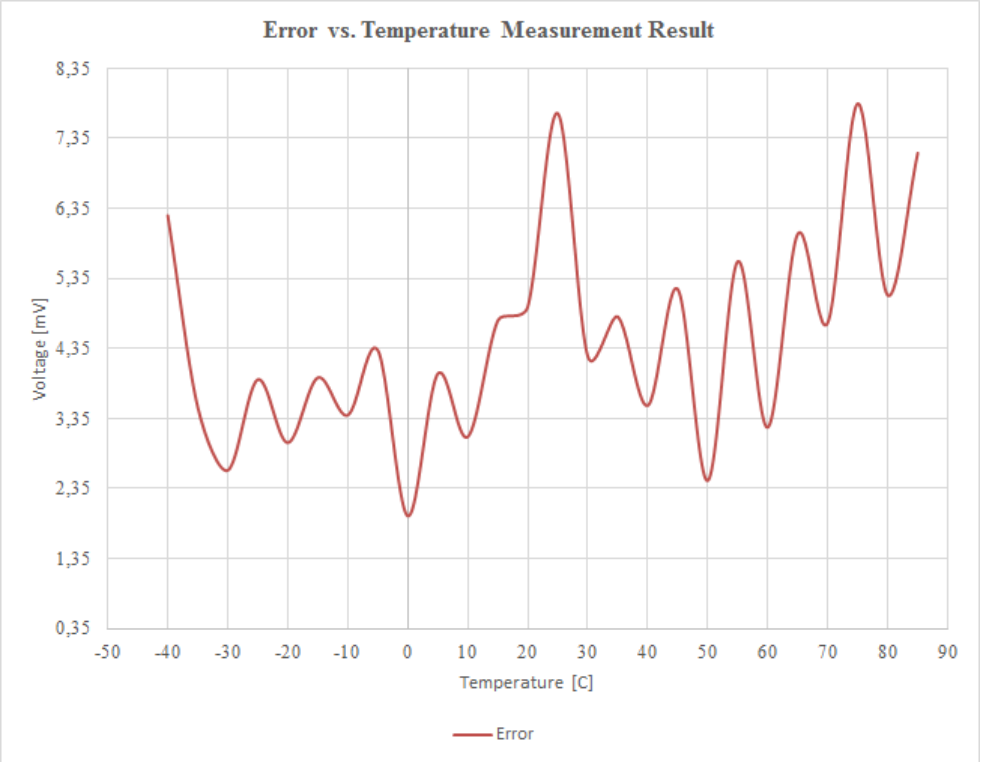

Figure 5.5 : Measurement Error for $K_{DAC} = 10$

Measurement results and error for disable chopper stabilization is given in the Figure 5.6 and Figure 5.7. It is clearly seen that fluctuation is gone away and only the offset error is presence.

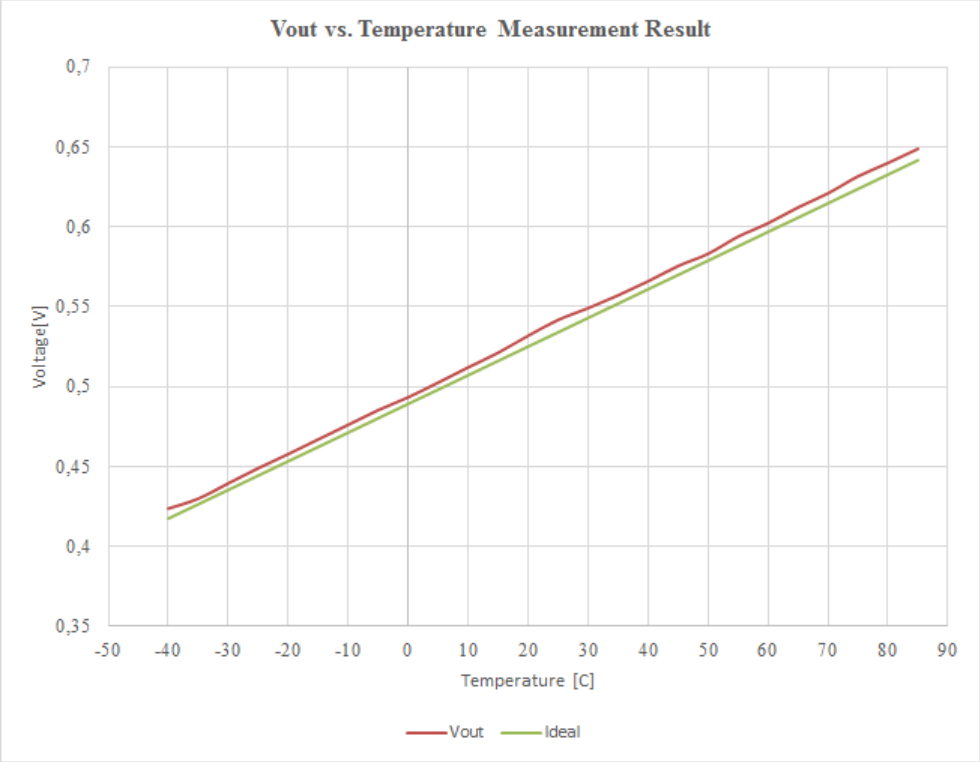

Figure 5.6 : Measurement Result for $K_{DAC} = 10$ (Chopper Disabled)

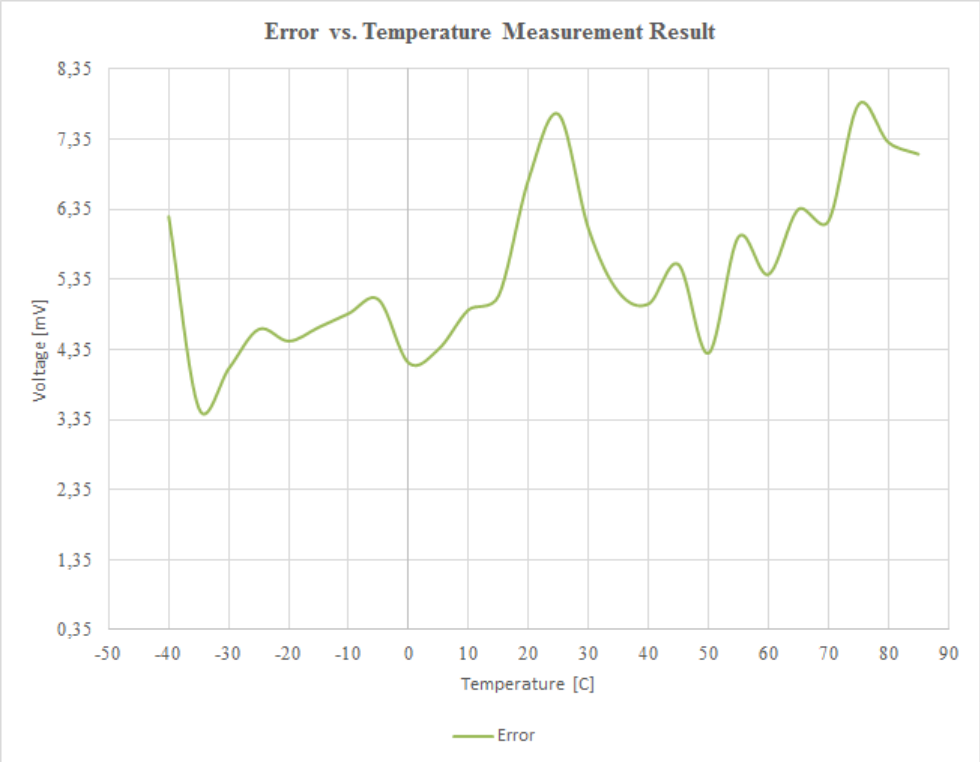

Figure 5.7 : Measurement Error for $K_{DAC} = 10$ (Chopper Disabled)

After offset and gain calibration output voltage of temperature to digital converter is given in the Figure 5.8 with ideal voltage cureve while error after calibration is given in the Figure 5.9.

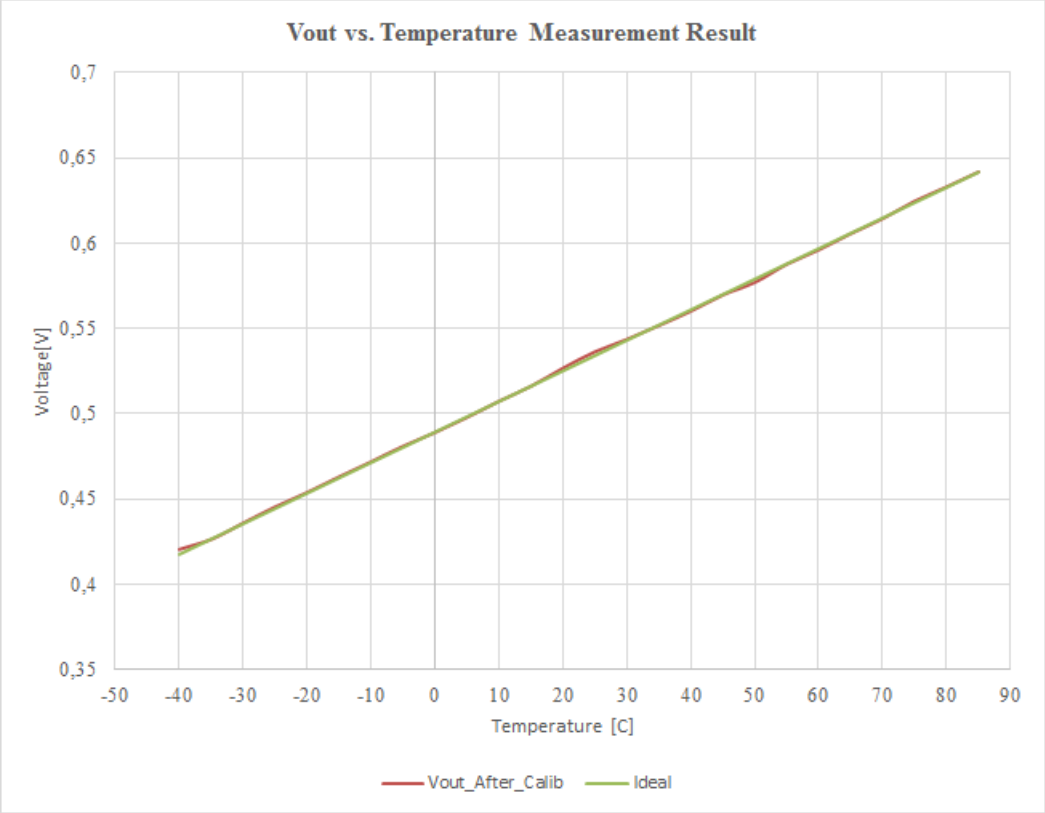

Figure 5.8 : Calib Result for $K_{DAC} = 10$ (Chopper Disabled)

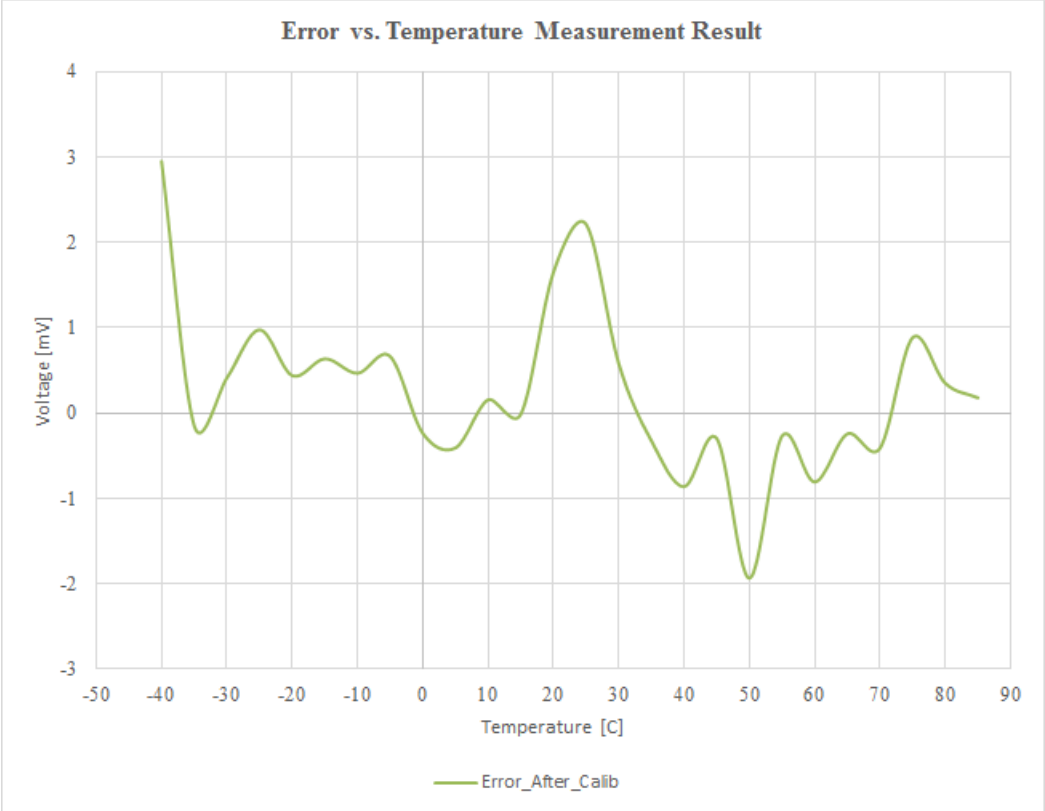

Figure 5.9 : Calib Error for $K_{DAC} = 10$ (Chopper Disabled)

Measurement results show successful temperature to digital conversion in the range of -40C to 85C with a resolution of 1C. However measurement setup is not advance to derive maximum resolution of the designed temperature sensor. Temperature chamber has a resolution of 0.1C but the temperature value is changing constantly over time. There are also error in reference voltages while sweeping temperature which cause error in conversion.

In order to ac have maximum resolution the measurement setup must be enhanced by using temperature chamber which is more stable or feedback systems contains thermocouple devices. Additionally reference voltages must be fixed or less varying over the temperature. De-embed method can be applied for both oven related errors and reference voltages related errors. Possible improvements for both design and measurement are given in the next section.

6. CONCLUSIONS

In this study, a temperature to digital converter is designed using a P-N junction to generate temperature information and a second order sigma delta modulator to convert temperature to digital.

In order to minimize flicker noise, switched tail current operational amplifier is proposed and simulation results are given with comparison to the standard tail current operational amplifier. Additionally to move the offset and low frequency noise chopper stabilization technique is used in both modulator driver and first integrator of sigma delta modulator.

Digital conversion of the temperature and resolution of the designed converter are given for different configuration of the chip such as gain of current and counter values with and without chopper technique. To obtain maximum resolution in the temperature range of -40C to 85C, gain and offset correction methods are presented.

Layout design of the temperature to digital converter is explained in detailed, layout matching techniques such as common centroid, inter-digitized and shielded clock and analog signals are employed in order to achieve good matching and less coupling.

Evaluation board schematic and layout design is presented. General PCB board design considerations and datasheet recommendations are followed to achieve best performance.

Temperature to digital conversion and resolution are verified with simple measurement setup which includes a power supply generator, an oscilloscope and a temperature chamber.

For future work temperature to digital converter must be fully characterized with more samples. To derive full resolution of the converter more advance measurement setup must be constructed including thermocouple devices and de-embeded setup related errors. To achieve less complex evaluation board and performance, reference voltages which are needed for sigma delta modulator can be generated internally with internal

LDOs. The same for the clock, clock can be generated with an internal oscillator. VPTAT voltage can be buffered to pin to measure temperature sensor and ADC separately. To minimize the area current DAC and I2C core can be eliminated after finding optimum configuration values for the registers. An enable/disable control for temperature conversion may be also added to system to be able to turn on/off the converter.

As a consequence in this work a 12 bit temperature to digital converter with a resolution of 0.25C is designed and manufactured. Temperature to digital conversion and 10 bit 1C resolution is verified with measurement. Future work and possible improvements are presented. As a result designed temperature to digital converter can be used as an IP in an IC which need a temperature sensor designed in the same process or in a system as a separate IC. This work provides a good solution for systems need a fine calibration over temperature and future academic works can benefit this work.

References

128-bit i2c bus serial eeprom (No. DS21178H). (2011). (Rev. E)

Anand, T., Makinwa, K. A. A., & Hanumolu, P. K. (2016, Nov). A vco based highly digital temperature sensor with 0.034 c/mv supply sensitivity. *IEEE Journal of Solid-State Circuits*, *51*(11), 2651-2663. doi: 10.1109/JSSC.2016.2598765

Ates, O. (2010). *Fully integrated 50mhz frequency reference with 1ppm absolute accuracy within 0-80c* (PhD Thesis). Istanbul Technical University.

Capacitor-free, 150-ma, low-dropout regulator with foldback current limit for portable devices (No. SBVS195E). (2015, 3). (Rev. E)

Dual, 200ma, low-iq, low-dropout regulator for portable devices (No. SBVS142A). (2010, 8). (Rev. A)

Dual, 300 ma output, low noise, high psrr voltage regulators (No. D09376-0-5/14(E)). (2014, 5). (Rev. E)

Instruments, T. (2003). *Fj (s-cqcc-j**) 4040139 (rev. b)* (AN). United States: Author.

Kashmiri, S. M., Xia, S., & Makinwa, K. A. A. (2009, July). A temperature-to-digital converter based on an optimized electrothermal filter. *IEEE Journal of Solid-State Circuits*, *44*(7), 2026-2035. doi: 10.1109/JSSC .2009.2020248

Low power, 1khz to 20mhz resistor set sot-23 oscillator (No. 6900fa). (2002). (Rev. A)

Malcovati, P., Brigati, S., Francesconi, F., Maloberti, F., Cusinato, P., & Baschirotto, A. (2003, Mar). Behavioral modeling of switched-capacitor sigma-delta modulators. *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, *50*(3), 352-364. doi: 10.1109/TCSI.2003 .808892

Maloberti, F. (2001). *Analog design for cmos vlsi systems*. NewYork, Boston, Dordrecht, London, Moscow: Kluwer Academic Publishers.

Maloberti, F. (2007). *Data converters*. Dordrecht, The Netherlands: Springer.

Ozdemir, M. (2012). *Ikinci derece sigma-delta a/d donusturucu tasarimi* (B. Sc. Thesis). Istanbul Technical University.

Ozkaya, I. (2010). *Wide input signal range 14 bits 1msps sar adc in 0.35um high voltage cmos process* (Master Thesis). Istanbul Technical University.

Philips. (1995). *The i2c-bus and how to use it*. Philips Semiconductor.

Pu, X., Ash, M., Nagaraj, K., Park, J., Vu, S., Kimelman, P., & de la Haye, S. (2015, Sept). An embedded 65 nm cmos remote temperature sensor with digital beta correction and series resistance cancellation achieving an inaccuracy of 0.4c (3 σ) from -40c to 130c. *IEEE Journal of Solid-State Circuits*, *50*(9), 2127-2137. doi: 10.1109/JSSC.2015.2434845

Razavi, B. (2001). *Design of analog cmos integrated circuits* (1st ed.). New York, NY, USA: McGraw-Hill, Inc.

Schmid, H. (2008, Nov). *Offset, flicker noise, and ways to deal with them.*

Toth, L., & Tsividis, Y. P. (2003, Aug). Generalization of the principle of chopper stabilization. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, *50*(8), 975-983. doi: 10.1109/TCSI.2003.815188

Wang, Y.-T. (2016). *Ultra-small low power temperature-to-digital converter and verification methods of analog circuit with trojan states* (PhD Thesis). Iowa State University.

Wooley, B. A. (1988). The design of sigma-delta modulation analog-to-digital converters. *IEEE Journal of Solid-State Circuits*, *12*(6).

APPENDICES

APPENDIX A.1 : Digital Verilog Codes
APPENDIX A.2 : Temperature to Digital Converter Top Level Schematic

APPENDIX A.1

```
module DIGITAL_TOP(SCL, RSTB, SDAI, SDAO, LOGIC_ZERO, CLK_TOP, IN, SER_OUT, CLK_OUT, TCTRIM, TST, VIBTRIM, VBGTRIM,
EN_DAC, EN_MOD_P, EN_MOD_M, EN_CHOP_MOD, EN_CHOP_DRIVER, DUMMY);

  input SCL, RSTB;
  input SDAI;

  input CLK_TOP;
  input IN;


  output [7:0] TCTRIM;
  output [2:0] TST;
  output [5:0] VIBTRIM;
  output [3:0] VBGTRIM;
  output EN_DAC;
  output EN_MOD_P;
  output EN_MOD_M;
  output EN_CHOP_MOD;
  output EN_CHOP_DRIVER;
  output [5:0] DUMMY;

  output SDAO;
  output LOGIC_ZERO;

  output SER_OUT;
  output CLK_OUT;

  wire [15:0] COUNT_IN;
  wire START_PAR2SER;
  wire [15:0] PAR_OUT;

  I2C_TOP U_I2C(.SCL(SCL), .RSTB(RSTB), .SDAI(SDAI), .SDAO(SDAO), .LOGIC_ZERO(LOGIC_ZERO), .TCTRIM(TCTRIM),
  .TST(TST), .VIBTRIM(VIBTRIM), .VBGTRIM(VBGTRIM), .EN_DAC(EN_DAC), .COUNT_IN(COUNT_IN), .EN_MOD_P(EN_MOD_P),
  .EN_MOD_M(EN_MOD_M), .EN_CHOP_MOD(EN_CHOP_MOD), .EN_CHOP_DRIVER(EN_CHOP_DRIVER), .DUMMY(DUMMY));

  integrator U_INT(.in(IN),.clk(CLK_TOP),.rstb(RSTB),.count_in(COUNT_IN), .start_par2ser(START_PAR2SER),
  .out(PAR_OUT));

  PAR2SER U_PAR2SER(.clk(CLK_TOP), .rstb(RSTB), .start(START_PAR2SER),
  .in(PAR_OUT), .out(SER_OUT), .clk_out(CLK_OUT));

endmodule
```

APPENDIX A.1

```
//Verilog HDL for "ITUVLSIREFLIB", "I2C_TOP" "behavioral"

/*
TOP Module connects all I2C blocks. Interfacing should be as follows:
1. SDAO and SCL should be connected to open drain output buffers.
2. The input of SDAI buffer and the output of SDAO buffer should be
   short circuited for bidirectional operation. Single pad with both
   input buffer and open drain output buffer can be used if such I/O
   Pad is available.
*/

module I2C_TOP (SCL, RSTB, SDAI, SDAO, LOGIC_ZERO, TCTRIM, TST, VIBTRIM,
     VBGTRIM, EN_DAC, COUNT_IN,
     EN_MOD_P, EN_MOD_M, EN_CHOP_MOD,
     EN_CHOP_DRIVER, DUMMY);

   input SCL, RSTB;
   input SDAI;


   output [7:0] TCTRIM;
   output [2:0] TST;
   output [5:0] VIBTRIM;
   output [3:0] VBGTRIM;
   output EN_DAC;
   output [15:0] COUNT_IN;
   output EN_MOD_P;
   output EN_MOD_M;
   output EN_CHOP_MOD;
   output EN_CHOP_DRIVER;
   output [5:0] DUMMY;

   output SDAO;


   output LOGIC_ZERO;

   wire [47:0] DATA_OUT_CHIP;

   wire WRB, CLK;
   wire [7:0] DATA_IN;
   wire [7:0] DATA_OUT;
   wire [2:0] ADR;


   assign LOGIC_ZERO = 1'b0;

   assign TCTRIM[7:0] = DATA_OUT_CHIP[7:0];
   assign TST[2:0] = DATA_OUT_CHIP[10:8];
   assign VIBTRIM[5:0] = DATA_OUT_CHIP[16:11];
   assign VBGTRIM[3:0] = DATA_OUT_CHIP[20:17];
   assign EN_DAC = DATA_OUT_CHIP[21];
   assign COUNT_IN[15:0] = DATA_OUT_CHIP[37:22];
   assign EN_MOD_P = DATA_OUT_CHIP[38];
   assign EN_MOD_M = DATA_OUT_CHIP[39];
   assign EN_CHOP_MOD = DATA_OUT_CHIP[40];
   assign EN_CHOP_DRIVER = DATA_OUT_CHIP[41];
   assign DUMMY[5:0] = DATA_OUT_CHIP[47:42];
   I2C_MAIN U1(SCL, RSTB, SDAI, SDAO, DATA_IN, CLK, ADR, WRB, DATA_OUT);
   REG_BLOCK U2(CLK, RSTB, ADR, WRB, DATA_IN, DATA_OUT, DATA_OUT_CHIP);

endmodule
```

APPENDIX A.1

```
module PAR2SER(clk, rstb, in, start, out, clk_out);

input clk, rstb;
input [15:0] in;
input start;
output reg out;
output reg clk_out;

reg [3:0] cnt;

reg clk_en;

always@(*) begin
  if(clk_en) begin
    clk_out = ~clk;
  end
  else begin
    clk_out = 0;
  end
end

always@(posedge clk or negedge rstb) begin
  if(!rstb) begin
    clk_en <= 0;
    out <= 0;
    cnt <= 15;
  end
  else if(start || cnt != 15) begin
    cnt <= cnt - 1;
    out <= in[cnt];
    clk_en <= 1;
  end
  else begin
    out <= 0;
    clk_en <= 0;
  end
end

endmodule
```

APPENDIX A.1

```
//Verilog HDL for "ITUVLSIREFLIB", "I2C_MAIN" "behavioral"

// I2C Main Module communicates through the I2C protocol, writes to and reads from REG BLOCK.

module I2C_MAIN (SCL, RSTB, SDAI, SDAO, DATA_IN, CLK_OUT, ADR, WRB, DATA_OUT);

input SCL, RSTB, SDAI;
input [7:0] DATA_OUT;

output [7:0] DATA_IN;
output [2:0] ADR;
output CLK_OUT, SDAO;
output WRB;

reg [5:0] STATE;
reg [2:0] ADR;
reg [7:0] DATA_IN;
reg CLK_OUT, SDAO;
reg WRB;

parameter CHIP_ADR = 7'b1010111;
wire START, REP_START;

I2C_START U1(SCL, SDAI, RSTB, START, REP_START);

parameter BEGIN    = 6'h00;
parameter CTRL_ADR6    = 6'h01;
parameter CTRL_ADR5    = 6'h02;
parameter CTRL_ADR4    = 6'h03;
parameter CTRL_ADR3    = 6'h04;
parameter CTRL_ADR2    = 6'h05;
parameter CTRL_ADR1    = 6'h06;
parameter CTRL_ADR0    = 6'h07;
parameter READ_WRITE    = 6'h08;
parameter W_ACK    = 6'h09;
parameter ADR_IN7    = 6'h0A;
parameter ADR_IN6    = 6'h0B;
parameter ADR_IN5    = 6'h0C;
parameter ADR_IN4    = 6'h0D;
parameter ADR_IN3    = 6'h0E;
parameter ADR_IN2    = 6'h0F;
parameter ADR_IN1    = 6'h10;
parameter ADR_IN0    = 6'h11;
parameter ADR_ACK    = 6'h12;
parameter DATA_OUT7_OR_STOP = 6'h13;
parameter DATA_OUT6    = 6'h14;
parameter DATA_OUT5    = 6'h15;
parameter DATA_OUT4    = 6'h16;
parameter DATA_OUT3    = 6'h17;
parameter DATA_OUT2    = 6'h18;
parameter DATA_OUT1    = 6'h19;
parameter DATA_OUT0    = 6'h1A;
parameter DATA_OUT_ACK    = 6'h1B;
parameter DATA_IN7_OR_READ  = 6'h1C;
parameter DATA_IN6    = 6'h1D;
parameter DATA_IN5    = 6'h1E;
parameter DATA_IN4    = 6'h1F;
parameter DATA_IN3    = 6'h20;
parameter DATA_IN2    = 6'h21;
parameter DATA_IN1    = 6'h22;
parameter DATA_IN0    = 6'h23;
parameter DATA_IN_ACK    = 6'h24;
parameter HLT    = 6'h25;

wire RSTB_INT;

assign RSTB_INT = START && RSTB;

always@(negedge SCL or negedge RSTB_INT) begin
  if(!RSTB_INT) begin
    STATE <= BEGIN;
    DATA_IN <= 0;
    CLK_OUT <= 1;
    SDAO <= 1;
    WRB <= 0;
    if(!RSTB) begin
      ADR <= 0;
    end
  end
  else begin
    case (STATE)
      BEGIN: begin
        SDAO <= 1;
        STATE <= CTRL_ADR6;
        CLK_OUT <= 1;
        WRB <= 0;
      end
      CTRL_ADR6: begin
        SDAO <= 1;
        if(SDAI==CHIP_ADR[6]) begin
          STATE <= CTRL_ADR5;
        end
        else begin
          STATE <= HLT;
```

```
    end
    CLK_OUT <= 1;
    WRB <= 0;
  end
  CTRL_ADR5: begin
    SDAO <= 1;
    if(SDAI==CHIP_ADR[5]) begin
      STATE <= CTRL_ADR4;
    end
    else begin
      STATE <= HLT;
    end
    CLK_OUT <= 1;
    WRB <= 0;
  end
  CTRL_ADR4: begin
    SDAO <= 1;
    if(SDAI==CHIP_ADR[4]) begin
      STATE <= CTRL_ADR3;
    end
    else begin
      STATE <= HLT;
    end
    CLK_OUT <= 1;
    WRB <= 0;
  end
  CTRL_ADR3: begin
    SDAO <= 1;
    if(SDAI==CHIP_ADR[3]) begin
      STATE <= CTRL_ADR2;
    end
    else begin
      STATE <= HLT;
    end
    CLK_OUT <= 1;
    WRB <= 0;
  end
  CTRL_ADR2: begin
    SDAO <= 1;
    if(SDAI==CHIP_ADR[2]) begin
      STATE <= CTRL_ADR1;
    end
    else begin
      STATE <= HLT;
    end
    CLK_OUT <= 1;
    WRB <= 0;
  end
  CTRL_ADR1: begin
    SDAO <= 1;
    if(SDAI==CHIP_ADR[1]) begin
      STATE <= CTRL_ADR0;
    end
    else begin
      STATE <= HLT;
    end
    CLK_OUT <= 0;
    WRB <= 0;
  end
  CTRL_ADR0: begin
    SDAO <= 1;
    if(SDAI==CHIP_ADR[0]) begin
      STATE <= READ_WRITE;
    end
    else begin
      STATE <= HLT;
    end
    CLK_OUT <= 1;
    WRB <= 0;
  end
  READ_WRITE: begin
    SDAO <= 0;
    if(SDAI) begin
      STATE <= DATA_OUT7_OR_STOP;
    end
    else begin
      STATE <= W_ACK;
    end
    CLK_OUT <= 1;
    WRB <= 0;
  end
  W_ACK: begin
    SDAO <= 1;
    STATE <= ADR_IN7;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  ADR_IN7: begin
    SDAO <= 1;
    STATE <= ADR_IN6;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  ADR_IN6: begin
    SDAO <= 1;
    STATE <= ADR_IN5;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  ADR_IN5: begin
    SDAO <= 1;
```

```
    STATE <= ADR_IN4;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  ADR_IN4: begin
    SDAO <= 1;
    STATE <= ADR_IN3;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  ADR_IN3: begin
    SDAO <= 1;
    STATE <= ADR_IN2;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  ADR_IN2: begin
    SDAO <= 1;
    ADR[2] <= SDAI;
    STATE <= ADR_IN1;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  ADR_IN1: begin
    SDAO <= 1;
    ADR[1] <= SDAI;
    STATE <= ADR_IN0;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  ADR_IN0: begin
    ADR[0] <= SDAI;
    STATE <= ADR_ACK;
    SDAO <= 0;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  ADR_ACK: begin
    SDAO <= 1;
    STATE <= DATA_IN7_OR_READ;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  DATA_OUT7_OR_STOP: begin
    if (SDAI) begin
      SDAO <= 1;
      STATE <= HLT;
    end
    else begin
      SDAO <= DATA_OUT[7];
      STATE <= DATA_OUT6;
    end
    CLK_OUT <= 1;
    WRB <= 0;
  end
  DATA_OUT6: begin
    SDAO <= DATA_OUT[6];
    STATE <= DATA_OUT5;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  DATA_OUT5: begin
    SDAO <= DATA_OUT[5];
    STATE <= DATA_OUT4;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  DATA_OUT4: begin
    SDAO <= DATA_OUT[4];
    STATE <= DATA_OUT3;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  DATA_OUT3: begin
    SDAO <= DATA_OUT[3];
    STATE <= DATA_OUT2;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  DATA_OUT2: begin
    SDAO <= DATA_OUT[2];
    STATE <= DATA_OUT1;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  DATA_OUT1: begin
    SDAO <= DATA_OUT[1];
    STATE <= DATA_OUT0;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  DATA_OUT0: begin
    SDAO <= DATA_OUT[0];
    ADR <= ADR + 1;
    STATE <= DATA_OUT_ACK;
    CLK_OUT <= 1;
    WRB <= 0;
  end
  DATA_OUT_ACK: begin
    SDAO <= 1;
    CLK_OUT <= 1;
```

```
        STATE <= DATA_OUT7_OR_STOP;
        WRB <= 0;
      end
      DATA_IN7_OR_READ: begin
        SDAO <= 1;
        CLK_OUT <= 1;
        WRB <= 0;
        if(REP_START) begin
          STATE <= CTRL_ADR6;
        end
        else begin
          STATE <= DATA_IN6;
          DATA_IN[7] <= SDAI;
        end
      end
      DATA_IN6: begin
        SDAO <= 1;
        CLK_OUT <= 1;
        WRB <= 0;
        STATE <= DATA_IN5;
        DATA_IN[6] <= SDAI;
      end
      DATA_IN5: begin
        SDAO <= 1;
        CLK_OUT <= 1;
        WRB <= 0;
        STATE <= DATA_IN4;
        DATA_IN[5] <= SDAI;
      end
      DATA_IN4: begin
        SDAO <= 1;
        CLK_OUT <= 1;
        WRB <= 0;
        STATE <= DATA_IN3;
        DATA_IN[4] <= SDAI;
      end
      DATA_IN3: begin
        SDAO <= 1;
        CLK_OUT <= 1;
        WRB <= 0;
        STATE <= DATA_IN2;
        DATA_IN[3] <= SDAI;
      end
      DATA_IN2: begin
        SDAO <= 1;
        CLK_OUT <= 1;
        WRB <= 0;
        STATE <= DATA_IN1;
        DATA_IN[2] <= SDAI;
      end
      DATA_IN1: begin
        SDAO <= 1;
        CLK_OUT <= 1;
        WRB <= 0;
        STATE <= DATA_IN0;
        DATA_IN[1] <= SDAI;
      end
      DATA_IN0: begin
        STATE <= DATA_IN_ACK;
        SDAO <= 0;
        DATA_IN[0] <= SDAI;
        CLK_OUT <= 0;
        WRB <= 1;
      end
      DATA_IN_ACK: begin
        SDAO <= 1;
        STATE <= HLT;
        CLK_OUT <= 1;
        WRB <= 1;
      end
      HLT: begin
        SDAO <= 1;
        STATE <= HLT;
        CLK_OUT <= 1;
        WRB <= 0;
      end
      default: begin
        SDAO <= 1;
        STATE <= HLT;
        CLK_OUT <= 1;
        WRB <= 0;
      end
    endcase
  end
end

endmodule
```

APPENDIX A.1

```
//Verilog HDL for "ITUVLSIREFLIB", "REG_BLOCK" "behavioral"

// REG BLOCK is a standard 8 bit word block with hard wired default values.


module REG_BLOCK (CLK, RSTB, ADR, WRB, DATA_IN, DATA_OUT, DATA_OUT_CHIP);

parameter DATA_OUT_CHIP_WIDTH = 48;
parameter ADD_WIDTH = 3;

input CLK, RSTB, WRB;
input [ADD_WIDTH-1:0] ADR;
input [7:0] DATA_IN;
output [7:0] DATA_OUT;
output [DATA_OUT_CHIP_WIDTH-1:0] DATA_OUT_CHIP;

reg [7:0] DATA_OUT;
reg [7:0] DATA_OUT_REG_ARRAY [5:0];

assign DATA_OUT_CHIP[7:0] = DATA_OUT_REG_ARRAY[0];
assign DATA_OUT_CHIP[15:8] = DATA_OUT_REG_ARRAY[1];
assign DATA_OUT_CHIP[23:16] = DATA_OUT_REG_ARRAY[2];
assign DATA_OUT_CHIP[31:24] = DATA_OUT_REG_ARRAY[3];
assign DATA_OUT_CHIP[39:32] = DATA_OUT_REG_ARRAY[4];
assign DATA_OUT_CHIP[47:40] = DATA_OUT_REG_ARRAY[5];


always@(posedge CLK or negedge RSTB) begin
  if(!RSTB) begin
    DATA_OUT_REG_ARRAY[0] <= 8'b00000100;
    DATA_OUT_REG_ARRAY[1] <= 8'b00000010;
    DATA_OUT_REG_ARRAY[2] <= 8'b11110001;
    DATA_OUT_REG_ARRAY[3] <= 8'b11111111;
    DATA_OUT_REG_ARRAY[4] <= 8'b00111111;
    DATA_OUT_REG_ARRAY[5] <= 8'b00000011;
  end
  else begin
    if(WRB == 1 && ADR <= 5) begin
      DATA_OUT_REG_ARRAY[ADR] <= DATA_IN;
    end
  end
end

always@(*) begin
  if(ADR <= 5) begin
    DATA_OUT = DATA_OUT_REG_ARRAY[ADR];
  end
  else begin
    DATA_OUT = 0;
  end
end

endmodule
```

APPENDIX A.1

```
`timescale 1ns/1ps
//`include "/vlsi/kits/ams/HK400/verilog/h35b4/h35_CORELIB_HV.v"
//`include "/vlsi/kits/ams/HK400/verilog/h35b4/h35_UDP.v"

module TEST_DIGITAL_TOP;

  `include "I2C_numbers.v"

  parameter SDA_WRITE0 = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER00,TX_ACK,NUMBERAA,TX_ACK,STOP};
  parameter SDA_WRITE1 = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER01,TX_ACK,NUMBER55,TX_ACK,STOP};
  parameter SDA_WRITE2 = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER02,TX_ACK,NUMBERAA,TX_ACK,STOP};
  parameter SDA_WRITE3 = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER03,TX_ACK,NUMBER55,TX_ACK,STOP};
  parameter SDA_WRITE4 = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER04,TX_ACK,NUMBERAA,TX_ACK,STOP};
  parameter SDA_WRITE5 = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER05,TX_ACK,NUMBER55,TX_ACK,STOP};
  parameter SDA_WRITE6 = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER06,TX_ACK,NUMBERAA,TX_ACK,STOP};
  parameter SDA_WRITE7 = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER07,TX_ACK,NUMBER55,TX_ACK,STOP};
  parameter SDA_WRITE8 = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER08,TX_ACK,NUMBERAA,TX_ACK,STOP};
  parameter SDA_WRITE9 = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER09,TX_ACK,NUMBER55,TX_ACK,STOP};
  parameter SDA_WRITEA = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER0A,TX_ACK,NUMBERAA,TX_ACK,STOP};
  parameter SDA_WRITEB = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER0B,TX_ACK,NUMBER55,TX_ACK,STOP};
  parameter SDA_WRITEC = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER0C,TX_ACK,NUMBERAA,TX_ACK,STOP};
  parameter SDA_WRITED = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER0D,TX_ACK,NUMBER55,TX_ACK,STOP};
  parameter SDA_WRITEE = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER0E,TX_ACK,NUMBERAA,TX_ACK,STOP};
  parameter SDA_WRITEF = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER0F,TX_ACK,NUMBER55,TX_ACK,STOP};

  parameter SDA_WRITE3a = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER03,TX_ACK,NUMBER07,TX_ACK,STOP};
  parameter SDA_WRITE4a = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER04,TX_ACK,NUMBER00,TX_ACK,STOP};

  parameter SDA_READ_ALL = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER00,TX_ACK,REP_START,CHIP_ADR_ARRAY,R,TX_ACK,
    {8{IDLE}},RX_ACK,
    {8{IDLE}},RX_ACK,
    {8{IDLE}},RX_ACK,
    {8{IDLE}},RX_ACK,
    {8{IDLE}},RX_ACK,
    {8{IDLE}},IDLE,STOP};
  parameter SDA_READ9 = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER09,TX_ACK,REP_START,CHIP_ADR_ARRAY,R,TX_ACK,{8{IDLE}},IDLE,STOP};
  parameter SDA_WRITE_ALL = {START,CHIP_ADR_ARRAY,W,TX_ACK,NUMBER00,TX_ACK,
    NUMBERAA,TX_ACK,
    NUMBER55,TX_ACK,
    NUMBERAA,TX_ACK,
    NUMBER55,TX_ACK,
    NUMBERAA,TX_ACK,
    NUMBER55,TX_ACK,
    NUMBERAA,TX_ACK,
    NUMBER55,TX_ACK,STOP};
  /*parameter SDA_ARRAY = {{10{IDLE}},SDA_READ_ALL,
    {10{IDLE}},SDA_WRITE0,
    {10{IDLE}},SDA_WRITE1,
    {10{IDLE}},SDA_WRITE2,
    {10{IDLE}},SDA_WRITE3,
    {100000{IDLE}},
    {10{IDLE}},SDA_WRITE4,
    {10{IDLE}},SDA_READ_ALL,
    {10{IDLE}}};
  */
  parameter SDA_ARRAY = {{10{IDLE}},SDA_READ_ALL,
    {10{IDLE}},SDA_WRITE0,
    {10{IDLE}},SDA_WRITE1,
    {10{IDLE}},SDA_WRITE2,
    {10{IDLE}},SDA_WRITE3,
    {10{IDLE}},SDA_WRITE4,
    {10{IDLE}},SDA_WRITE5,
    {10{IDLE}},SDA_READ_ALL,
    {10{IDLE}},SDA_WRITE0,
    {10{IDLE}},SDA_WRITE1,
    {10{IDLE}},SDA_WRITE2,
    {10{IDLE}},SDA_WRITE3a,
    {10{IDLE}},SDA_WRITE4a,
    {10{IDLE}},SDA_WRITE5,
    {10{IDLE}},SDA_READ_ALL,
    {10{IDLE}}};
  //Final MEM Contents: 55 00 07 55 AA
  //parameter SDA_ARRAY = {{10{IDLE}},SDA_READ_ALL,{10{IDLE}},SDA_WRITE_ALL,{10{IDLE}},SDA_READ_ALL,{10{IDLE}}};

  reg SDA;
  //This CLK is for timing purposes only!!
  reg CLK;
  reg SCL_RUN = 0;
  reg ISSTART = 0;
  reg ISREPSTART = 0;
  reg ISSTOP = 0;
  reg [2:0] COND;
  integer i = 10;
  integer imax = 0;

  reg SCL;
  reg RSTB;
  reg SDAI;
  wire SDAO;
  wire LOGIC_ZERO;
  reg CLK_TOP;
  reg IN;
  wire SER_OUT;
  wire CLK_OUT;
```

```
  wire [7:0] TCTRIM;
  wire [2:0] TST;
  wire [5:0] VIBTRIM;
  wire [3:0] VBGTRIM;
  wire EN_DAC;
  wire EN_MOD_P;
  wire EN_MOD_M;
  wire EN_CHOP_MOD;
  wire EN_CHOP_DRIVER;
  wire [5:0] DUMMY;

DIGITAL_TOP UUT(
  SCL,
  RSTB,
  SDAI,
  SDAO,
  LOGIC_ZERO,
  CLK_TOP,
  IN,
  SER_OUT,
  CLK_OUT,
  TCTRIM,
  TST,
  VIBTRIM,
  VBGTRIM,
  EN_DAC,
  EN_MOD_P,
  EN_MOD_M,
  EN_CHOP_MOD,
  EN_CHOP_DRIVER,
  DUMMY);

  always@(*) begin
    if(SDA == 0 || SDAO == 0) begin
      SDAI = 0;
    end
    else begin
      #52 SDAI = 1;
    end
  end

  initial begin
    while (SDA_ARRAY[imax] !== 1'bx) begin
      imax = imax + 1;
    end
    i = imax - 1;
  end

  //For Trim Testing
  always@(negedge CLK) begin
      ISSTART = 0;
      ISSTOP = 0;
      ISREPSTART = 0;
      if(i>=2) begin
        COND[0] = SDA_ARRAY[i-2];
        COND[1] = SDA_ARRAY[i-1];
        COND[2] = SDA_ARRAY[i];
        if(COND == START) begin
          if(SCL_RUN == 0) begin
            SCL_RUN = 1;
            ISSTART = 1;
          end
          else begin
            ISREPSTART = 1;
          end
        end
        else if(COND == STOP) begin
          SCL_RUN = 0;
          ISSTOP = 1;
        end
      end
        if(ISSTART) begin SCL = 1; end
        else if(ISREPSTART) begin SCL = 0; end
        else if(ISSTOP) begin SCL = 0; end
          else if(SCL_RUN) begin SCL = 0; end
        else begin SCL = 1; end
      #62.5 if(i == 0) begin
        SDA = 1;
          end
          else begin
            SDA = SDA_ARRAY[i];
        i = i - 1;
          end
         if(ISSTART) begin SCL = 1; end
         else if(ISREPSTART) begin SCL = 0; end
        else if(ISSTOP) begin SCL = 0; end
          else if(SCL_RUN) begin SCL = 0; end
        else begin SCL = 1; end
      #62.5 if(i == 0) begin
        SDA = 1;
          end
          else begin
            SDA = SDA_ARRAY[i];
        i = i - 1;
          end
         if(ISSTART) begin SCL = 1; end
         else if(ISREPSTART) begin SCL = 1; end
        else if(ISSTOP) begin SCL = 1; end
          else if(SCL_RUN) begin SCL = 1; end
        else begin SCL = 1; end
      #62.5 if(i == 0) begin
```

```
          SDA = 1;
            end
            else begin
               SDA = SDA_ARRAY[i];
          i = i - 1;
            end
  end


  initial begin
    // Initialize Inputs
    SCL = 1;
    RSTB = 0;
    CLK = 0;

    #100 RSTB = 1;

  end

  always@(negedge CLK) begin
    if(i == 0) begin
//     #100 $stop;
       #100000000 $stop;
    end
  end

  always #125 CLK = ~CLK;

// initial $sdf_annotate("DIGITAL_TOP_all.sdf",UUT, , , "maximum");

initial CLK_TOP = 0;

always #450 CLK_TOP = ~CLK_TOP;

always@(posedge CLK_TOP) begin
  #100 IN = {$random};
end

initial IN = 0;

endmodule
```

APPENDIX A.1

```
module integrator(in,clk,rstb,count_in,out,start_par2ser);
  input in;
  input clk;
  input rstb;
  input [15:0] count_in;
  output [15:0] out;
  output reg start_par2ser;
  reg [15:0] count_out;
  reg [15:0] tmp;
  reg [15:0] out;
  reg set;

  always @ (posedge clk or negedge rstb) begin
    if(!rstb) begin
      tmp <= 0;
    end
    else begin
      if(count_out == 0) begin
        tmp <= in;
      end
      else if(in) begin
        tmp <= tmp+1;
      end
    end
  end

  always @ (posedge clk or negedge rstb) begin
    if(!rstb) begin
      set <= 1;
      count_out <= 0;
    end
    else begin
      if(set) begin
        count_out <= count_in;
        set <= 0;
      end
      else begin
        count_out <= count_out-1;
        if(count_out==1) begin
          set <= 1;
        end
        else begin
          set <= 0;
        end
      end
    end
  end

  always @ (posedge clk or negedge rstb) begin
    if(!rstb) begin
      out <= 0;
      start_par2ser <= 0;
    end
    else begin
      if(count_out==0) begin
        out <= tmp;
        start_par2ser <= 1;
      end
      else begin
        start_par2ser <= 0;
      end
    end
  end

endmodule
```

APPENDIX A.1

```
# Cadence Encounter(r) RTL Compiler
#  version v06.20-s027_1 (32-bit) built Apr 25 2007
#

set_attribute lib_search_path /work/kits/ams/HK400/liberty/h35_3.3V
set_attribute library {h35_CORELIB_HV.lib}
read_hdl -v2001 ../verilog/I2C_MAIN.v
read_hdl -v2001 ../verilog/I2C_REG_BLOCK.v
read_hdl -v2001 ../verilog/I2C_START.v
read_hdl -v2001 ../verilog/I2C_TOP.v
read_hdl -v2001 ../verilog/integrator.v
read_hdl -v2001 ../verilog/PAR2SER.v
 read_hdl -v2001 ../verilog/DIGITAL_TOP.v
elaborate DIGITAL_TOP
define_clock -period 100000 -fall 80 -rise 80 -name clkin /designs/DIGITAL_TOP/ports_in/SCL
define_clock -period 100000 -fall 80 -rise 80 -name clkin2 /designs/DIGITAL_TOP/ports_in/CLK_TOP
set_attribute slew {100 100 200 200} [find -clock clkin]
set_attribute slew {100 100 200 200} [find -clock clkin2]
external_delay -input 1000 -clock [find -clock clkin] -edge_fall [find /des* -port ports_in/SDAI]
external_delay -output 1000 -clock [find -clock clkin] -edge_fall [find /des* -port ports_out/*]
external_delay -input 1000 -clock [find -clock clkin2] -edge_rise [find /des* -port ports_in/IN]
external_delay -output 1000 -clock [find -clock clkin2] -edge_rise [find /des* -port ports_out/SER_OUT]
external_delay -output 1000 -clock [find -clock clkin2] -edge_rise [find /des* -port ports_out/CLK_OUT]
synthesize -to_mapped
write -mapped > DIGITAL_TOP_syn.v
write_sdc > DIGITAL_TOP.sdc
```

APPENDIX A.2

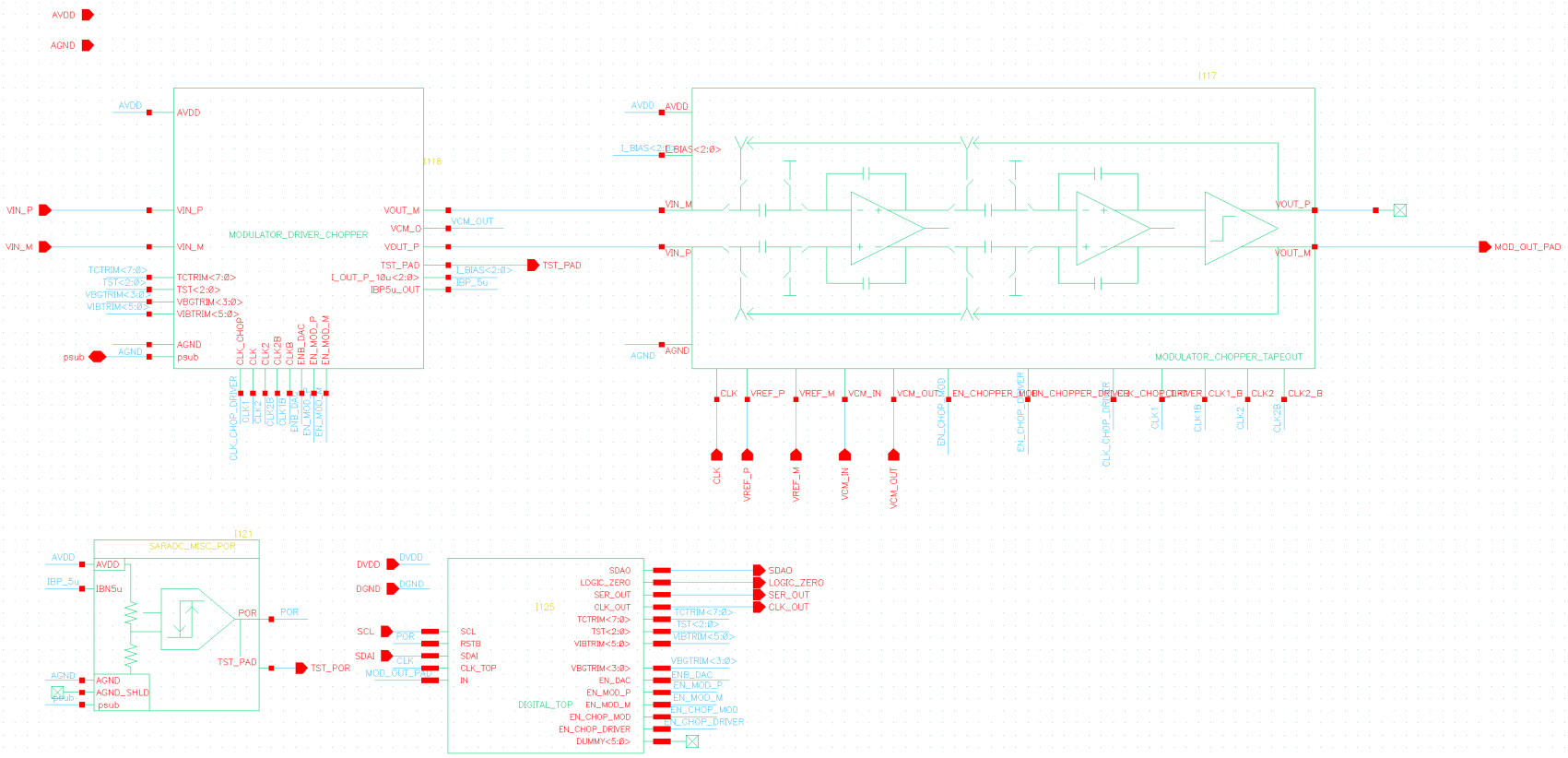

Figure B.1 : Top Level Schematic

CURRICULUM VITAE

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