ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

MODELING AND IMPLEMENTATION OF BIOLOGICAL NEURAL SYSTEMS

Ph.D. THESIS

Özgür ERDENER

Department of Electronics and Communications Engineering

Electronics Engineering Programme

SEPTEMBER 2016

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To my family,

FOREWORD

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June 2016 Özgür ERDENER

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ABBREVIATIONS

2-D : Two Dimensional
AdEx : Adaptive Exponential
AMS : Austria Micro Systems
BiCMOS : Bipolar CMOS
BMI : Brain-Machine Interface
CLM : Channel Length Modulation
CM : Current Mirror
CMOS : Complementary MOS
CPG : Central Pattern Generator
FET : Field Effect Transistor
FF : Fast-Fast
FS : Fast Spiking/Fast-Slow (for corners)
FN : Fitzhugh-Nagumo
GUI : Graphical User Interface
HH : Hodgkin-Huxley
HR : Hindmars-Rose
I&F : Integrate and Fire
ICFM : Iterative Curve Fitting Methodology
LTD : Long Term Depression
LTP : Lonp Term Plasticity
LTS : Low Threshold Spiking
MOS : Metal Oxide Semiconductor
PRC : Phase Response Curve
RMSE : Root Mean Squared Error
RS : Regular Spiking
SF : Slow-Fast
SiGe : Silicon Germanium
SNN : Spiking Neural Network
SS : Slow-Slow
STD : Short Term Depression
STP : Short Term Potentation
THB : Tanget Hyperbolic Block
tm : typical mean
TSMC : Taiwan Semiconductor Manufacturing Company
TT : Typical-Typical
VLSI : Very Large Scale Integration
ws : worstcase speed
wp : worstcase power
wo : worstcase one
wz : worstcase zero

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MODELING AND IMPLEMENTATION OF BIOLOGICAL NEURAL SYSTEMS

SUMMARY

The elementary processing units of brain are the nerve cells, or neurons. Neurons are believed to be the key elements in signal processing. Those cells are analog units that work together to carry out the highly sophisticated computations in cognition and control. In traditional artificial neural networks, the neuron behavior is described only in terms of firing rate, but most of the real neurons, commonly known as spiking neurons, transmit information by pulses called action potentials or spikes. Spiking neuron models vary from the computationally simple Integrate and Fire (I&F) model to biologically meaningful Hodgkin-Huxley (HH) model. The network constructed with those models are called Spiking Neural Network (SNN). According to accuracy requirements and electronically easeness of implementation the appropriate model is selected for implementing the network. Today, SNN's has become essential to study the brain functions for Artificial Network Community.

In this thesis, a new dynamical neuron model suitable for low power and compact VLSI implementation is presented. This model can operate in biological time and voltage scale. When designing the model, geometrical nullcline approach is used. In operational area, model has similar nullclines with $I_{Na,p}$+I_K model resulting to equivalency in dynamic behaviour at subthreshold region. Offered model has two state variables such that one represents the membrane voltage while the other one represents the recovery variable. Also it has after spike reset mechanism as in hybrid models. Unlike Izhikevich and AdEx I&F model, only the membrane voltage is reset to a constant reset value after the spike reaches its apex. This is a big advantage of the model since implementing the hard reset of recovery variable requires large number of transistors which is a limiting factor for design of large-scale neuromorphic hardware. Recovery variable grows to the desired 'after-spike' value on its own in our model. Tangent hyperbolic characteristic of nullcline slows down the growth speed of state variable while approaching to the positive (or negative) saturation region of tangent hyperbolic. So this mechanism limits the growth speed as it will result to realistic spike timing.

Even the new neuron model seems to have ten different parameters when it is scaled to obtain the minimum numbers of parameters it is seen that it has only four independent parameters and an input current. One can obtain nearly all of the major spiking templates of real biological neurons by only modifiying two of this parameters and input current. A software application in MATLAB to examine the neuro computational features of new neuron model with numerical simulations is developed, also. This application has a GUI for accepting the inputs from user and displaying the calculated outputs. By using this application it is shown that the model is capable of generating the most of the spiking patterns exhibited by the known types of neocortical and thalamic neurons when the proper parameter set is selected.

New neuron model is constructed with tangent hyperbolic functions since it is odd symetric and easily implementable as VLSI circuit by using subthreshold CMOS technique. Judicious use of this technique leads to a very effective low power CMOS neuron. Implemented neuron circuit consist of a single first-order log domain filter, hyperbolic function generators, linear voltage dividers, compare & reset block and a voltage tunable current reference. In design phase, the simulation results are fitted to analytic expressions by using linear least squares curve fitting method. Accuracy metric of fitting is Root Mean Squared Error (RMSE) value. The design parameters is iterated until RMSE value stays below a spesific value. This technique is named as Iterative Curve Fitting Method (ICFM).

Long tailed circuit topology with cascode output stage is used for implementing the tangent hyperbolic function generators (THB). To minimize the effect of process parameters deviation, a core THB with minimum tail current supplied from matched 100pA current source is designed, then the output is multiplied by a constant value for obtaining the real output of different THB's.

Linear voltage divider circuit consist of two layered ladder type diode connected NMOS transistors. Dividing ratio of this block is determined as 8.8. When compared with the conventional MOS voltage dividers offered configuration has the advantage of having less number of transistors for the same divider value and of reduced body effect. Source shifting or offset voltage is applied to this circuit since it operates at very low currents.

Log domain filter is a current mode circuit such that it is completely suitable for the implementation of recovery variable of our neuron model. Source shifting is applied to this circuit, also.

A comparator circuit which drives a discharge switch is designed. Comparator circuit is implemented by connecting the input of two stage inverter to the output of a simple long tailed circuit that acts as differential amplifier. Tail current of differential amplifier should be high enough to drive output inverter stage as fast as possible. Thus this current is selected $\approx$2.3 nA. Discharge switch is implemented with big sized NMOS transistor since it should have high current sink capacity.

Process parameter deviation and temperature dependency are the two most critical problems effective on the circuit operation. Especially for the circuits based on subthreshold operation, temperature dependency is a very common problem. Therefore, a wide temperature range voltage tunable current reference circuit is implemented. Voltage tuning is needed for minimizing the effect of process parameters deviation. The tuning voltage values that guarantees the proper operation of neuron circuit at all process corners are obtained.

Initial design and simulations are carried out with TSMC 0.18μm technology by using LTSpice design tools. Then all the blocks of neuron circuit is designed again with AMS 0.35μm SiGe-BiCMOS process by using Cadence® Virtuoso® tools for both verifying the previous design and implementing the Layout of the neuron. The circuit topology and transistor sizes are kept same as in TSMC design and obtained the same results by only modifiying the value of voltage, currents sources and capacitors. The operating and supply voltages is shifted to higher values since the transistor transconductance of AMS technology is quite lower than TSMC technology. Minimum channel width to length ratio is selected as 2μm/2μm at both

designs for minimizing the effect of the absolute parameter deviation in sizing caused by the VLSI manufacturing process.

AMS design occupies 0.0128 mm^2 chip area. Power consumption is 277.5 nW for AMS design and 241 nW for TSMC design. Supply and offset voltages are 2.5 V and 0.5 V for AMS circuit, 1.5 V and 0.2 V for TSMC circuit, respectively. Spiking patterns obtained from circuit simulations perfectly matches with numerical results.

In most of the synapse models, temporal dynamics are neglected and synapses are assumed as an instantaneous multiplier operator. A realistic model should take into consideration the spatial and temporal summation of synaptic currents. In the light of these observations, a new dynamical synapse model for coupling the neurons to create the realistic SNNs is offered. This model consist of similar terms as new neuron model that makes it also suitable for compact and low power VLSI implementation. The model allows to make a synapse excitatory or inhibitory by only altering the reversal potential parameter.

Synchronized activity of neurons take role in a wide range from cognitive functions to rhythmic movements of animals. The phase response curve (PRC), i.e. the neurons's response to weak perturbations, is a useful tool to understand the collective dynamical properties of a neuron in a network. Therefore the PRC of new neuron with VLSI implemented parameters is extracted and shown that it has Type II PRC. Based on complete neuron and synapse models, synchronization behavior of different number of reciprocally connected neurons that form a ring coupled network with excitatory and inhibitory synapses is studied. Numerical simulations are accomplished and inphase, antiphase and N-phase synchronization behaviour for networks with 2, 3 and 4 neurons are observed.

VLSI circuit of two reciprocally coupled neuron and a ring coupled network with 3 neurons is designed by using TSMC 0.18μm technology. Because of weak coupling synaptic currents are so small to implement as VLSI circuit. So some scaling operations are made to shift the synapse circuit output current value in a VLSI implementable range. At circuit simulations the expected inphase, antiphase and N-phase synchronization patterns is successfully observed. Power consumption is 282 nW for two reciprocally coupled neuron and 320 nW for three ring coupled neuron network.

BİYOLOJİK SİNİR SİSTEMLERİNİN MODELLENMESİ VE GERÇEKLENMESİ

ÖZET

Beynimizin temel işlem birimi sinir hücreleri veya kısaca nöronlardır. Bir memeli beynindeki sinir hücreleri, birbirleri ile koordine bir şekilde çalışıp görüntü işleme, karar verme, idrak etme, motor kontrol gibi yüksek karmaşıklıktaki hesaplamaları çok kısa sürede, çok az enerji tüketerek yerine getiren analog birimlerdir. İnsan sinir sisteminde yaklaşık olarak 100 milyar nöron olduğu tahmin edilmektedir. Bununla beraber normal bir sinir hücresi 50.000-250.000 kadar başka nöronla bağlantılıdır. Beynin tamamının nasıl çalıştığı konusunda günümüzde halen yeterli bilgiye sahip değiliz fakat bazı küçük bölümlerinin çalışması ile ilgili ayrıntılı bilgiler mevcuttur. Dinamik nöron modelleri, hesaplama kolaylığı olan I&F modelinden biyolojik olarak anlamlı olan karmaşık Hodgkin-Huxley modeline kadar çeşitlilik göstermektedir. Uygulamadaki hassasiyete ve tasarım kolaylığına bağlı olarak VLSI devre olarak gerçekleme için uygun olan model seçimi değişebilir.

Bu tez çalışmasında, düşük güç tüketen ve az alan kaplayan VLSI devresi olarak gerçeklemeye uygun, biyolojik zaman ve biyolojik işaret ölçeğinde çalıştırılabilen dinamik bir nöron modeli önerilmiştir. Bu model geometrik yaklaşımla, denge eğrilerinden hareket ederek tasarlanmıştır. Önerilen model işlevsel olduğu çalışma bölgesinde $I_{Na,p}+I_K$ modeli ile benzer denge eğrilerine sahiptir. Bu durum, eşik altı bölgede, her iki modelin de eş davranış göstermesine neden olur. Model, biri hücre zarı potansiyelini diğeri tazmin akımını temsil eden iki durum değişkeninden oluşmaktadır. Ayrıca, hibrit modellerde olduğu gibi aksiyon potansiyeli sonrası reset mekanizmasına sahiptir. Ancak, Izhikevich ve AdEx I&F modellerinden farklı olarak, aksiyon potansiyeli tepe değerine ulaştığında sadece hücre zarı gerilimi sabit bir değere resetlenir. Tazmin değişkeninin resetlenmesi donanımsal olarak çok sayıda tranzistor gerektirdiği için çok geniş ölçekli nöromorfik devre gerçeklemede sınırlayıcı bir etkendir. Dolayısıyla, yeni modelde bu reset parametresinin olmaması devre gerçekleme açısından büyük bir avantaj sağlamaktadır . Önerilen modelin denge eğrilerinin tanjant hiperbolik karakteristiklerinden ötürü tazmin değişkeni, hücre zarı potansiyelinin resetlendiği noktada, olması gereken değere kendi kendine ulaşır.

Yeni nöron modelinde on farklı parametre varmış gibi gözükse de, denklemler minumum sayıda parametre elde edecek şekilde normalize edildiğinde, sadece dört bağımsız parametreye sahip olduğu görülür. Bu parametrelerden sadece iki tanesine değişik değerler vererek gerçek bir biyolojik sinir hücresinin gösterdiği aksiyon potansiyeli örüntülerinin birçoğu elde edilebilir. Modelin gösterdiği aksiyon potansiyeli davranışlarını incelemek amacıyla kullanıcıdan girdileri alıp sayısal benzetim sonuçlarını kullanıcıya sergileyen bir MATLAB uygulaması geliştirilmiştir. Bu uygulama sayesinde, uygun parametreler seçildiğinde, önerilen

modelin beynin neokorteks ve talamus bölgesinde bulunan sinir hücrelerinin gösterdiği farklı davranışların birçoğunu gerçekleştirebildiği kanıtlanmıştır.

Tek simetrik olması ve eşik altı CMOS tekniği ile VLSI gerçekleme kolaylığı nedeniyle yeni model tanjant hiperbolik fonksiyonlar ile oluşturulmuştur. Bu da nöron devresinin kısmen kolay ve hızlı gerçeklenmesini sağlamıştır. Gerçeklenen nöron devresi bir adet birinci derece logaritmik süzgeç, tanjant hiperbolik fonksiyon üreteçleri, doğrusal gerilim bölücüler, karşılaştırma ve resetleme bloğu ve bir adet de gerilim kontrollü akım referansından oluşmaktadır. Tasarım aşamasında, ayrı ayrı tüm bloklar için devre benzetim sonucunu analitik ifadesinin eğrisine, minumum kareler yöntemi kullanarak, uydurma yöntemi uygulanmıştır. Akım ve tranzistor boyutları gibi tasarım parametreleri belli bir karesel hatanın altında kalana kadar yinelenmiş ve bu yöntem Yinelemeli Eğri Uydurma Yöntemi olarak (Iterative Curve Fitting Method-ICFM) olarak isimlendirilmiştir.

Tanjant hiperbolik fonksiyon üreteci (THB) olarak eşik altı çalışan, koskod çıkış katlı, uzun kuyruklu devre yapısı kullanılmıştır. Proses parametrelerinin sapmasından kaynaklanacak hatanın minimize edilebilmesi için kuyruk akımı 100 pA olan bir çekirdek THB tasarlanmıştır. Daha sonra, farklı değerli THB blokları bu çekirdek bloğun çıkışındaki akım, kaskod akım aynası kullanılarak, gerekli sabit katsayılar ile çarpılarak elde edilmiştir.

Doğrusal gerilim bölücü devresi iki katmanlı merdiven tipi diyot bağlı NMOS tranzistorlardan oluşmaktadır. Bu bloğun bölme değeri geniş bi gerilim aralığında 8.8 olarak elde edilmiştir. Klasik MOS gerilim bölücüye göre bu tasarımda daha az sayıda tranzistor ile daha büyük bölme değeri elde edilir ve gövde etkisi de diğerine göre daha düşüktür. Bu devre çok küçük akımlarla çalıştığı için devreye kaynak öteleme gerilimi uygulanmıştır.

Birinci derece logaritmik süzgeç devresi akım modlu olması nedeni ile tazmin akımını temsil eden değişkenin gerçeklenmesi için tamamı ile uygundur. Çok küçük akımlarla çalışıldığı için bu bloğa da kaynak öteleme gerilimi uygulanmıştır.

Karşılaştırma devresi, iki adet kaskod bağlı eviriciden oluşan yapının girişi fark kuvvetlendiricisi olarak çalışan uzun kuyruklu bir devrenin çıkışına bağlanarak gerçeklenmiştir. Bu devre akım boşaltma anahtarı görevi yapan büyük boyutlu bir NMOS tranzistoru sürmektedir. Uzun kuyruklu devrenin kuyruk akımı çıkıştaki evirici katlarını çok hızlı sürmesi için yeterince yüksek olmalıdır. Bu koşuldan yola çıkılarak kuyruk akımı ≈ 2.3 nA olarak belirlenmiştir.

Proses parametrelerindeki sapma ve sıcaklık bağımlılığı VLSI devrelerin çalışmasını etkileyen en kritik iki sorundur. Özellikle eşik altı çalışan devrelerde sıcaklık bağımlılığı hayati önem arz etmektedir. Bu nedenle geniş sıcaklık aralığında çalışan gerilimle kontrol edilebilir bir akım referansı devresi tasarlanmıştır. Gerilim kontrolü, proses parametrelerinden kaynaklı değişimlerin etkilerini minimize etmek için kullanılmış ve bu çerçevede devrenin bütün proses köşelerinde çalışmasını garanti edecek kontrol gerilimleri ayrı ayrı tespit edilmiştir.

Devre tasarımı ve benzetimleri ilk olarak TSMC 0.18μm teknolojisi ile LTSpice tasarım araçları kullanılarak yapılmıştır. Daha sonra, hem bu tasarımı doğrulamak hem de devrenin serimini oluşturabilmek için AMS 0.35μm SiGe-BiCMOS teknolojisi ile Cadence® Virtuoso® araçları kullanılarak bütün bloklar tekrar tasarlanmıştır. Bu tasarımda, devre yapısı ve tranzistor boyutları TSMC'deki ile aynı tutulup sadece akım, gerilim kaynakları ve kapasite değerleri değiştirilerek aynı sonuçlara ulaşılmıştır. AMS teknolojisinin geçiş iletkenliği TSMC'ye göre oldukça düşük olduğu için AMS ile yapılan tasarımda besleme ve çalışma gerilimlerini daha

yüksek değerlere ötelemek zorunluluğu ortaya çıkmıştır. Her iki tasarımda da VLSI üretim prosesinden kaynaklı mutlak boyut sapmalarının etkisini azaltmak için minimum tranzistor boyutu 2μm/2μm olarak seçilmiştir.

AMS teknolojisi ile gerçeklenen nöron devresi 0.0128 mm^2 alan kaplamakta ve 277.5 nW güç tüketmektedir. TSMC teknolojisi ile gerçeklenen nöron ise 241 nW güç tüketmektedir. Besleme ve kaynak öteleme gerilimleri sırasıyla AMS için 2.5 V ve 0.5 V, TSMC için 1.5 V ve 0.2 V'tur. Sayısal analizlerden elde edilen sonuçlarla devre benzetimlerinden elde edilen sonuçların mükemmel bir şekilde uyuştuğu gösterilmiştir.

Literatürdeki bir çok model, sinapsları anlık çarpma operatörleri farzedip dinamik bir yapı olduğunu göz ardı eder. Gerçek bir sinaps modeli sinaps akımlarının zaman ve uzamda toplanabilmesi özelliğini göz önünde bulundurmalıdır. Bu bilgiler çerçevesinde, nöronları birbirine bağlayıp gerçekçi sinir ağları oluşturabilmek amacıyla yeni bir dinamik sinaps modeli önerilmiştir. Modelde kullanılan ifadeler yeni nöron modelindekine benzer yapıda olması nedeniyle sinaps modeli de kompakt ve düşük güçlü VLSI gerçeklemeye uygundur. Yeni modelle, sadece ters gerilim potansiyeline karşı düşen terimin değiştirilmesi ile sinapsların uyarıcı veya kısıtlayıcı davranış göstermesi sağlanmıştır.

Nöronların senkronize davranışı canlıların kavramsal işlevlerini yerine getirmesi ve ritmik hareketlerinin oluşması gibi çok geniş bir çerçevede önemli bir role sahiptir. Bir nöronun zayıf uyarımlara cevabını gösteren Faz Yanıt Eğrileri (PRC), bir ağdaki nöronların ortak dinamik davranışını anlamak açısından çok önemli bir araçtır. Bu nedenle VLSI devre olarak gerçeklenen nöronun faz yanıt eğrisi çıkartılıp bunun Tip II PRC özelliğine sahip olduğu gösterilmiştir. Tip II PRC'ye sahip olması nedeniyle bir ağ içerisinde senkronize olabileceği sonucuna ulaşılmıştır. Daha sonra, yeni önerilen sinaps ve nöron modelleri kullanılarak, senkronizasyon davranışlarının incelenmesi amacıyla çeşitli sayılardaki nöronlar zincir bağlı bir ağ yapısı oluşturacak şekilde karşılıklı olarak uyarıcı ve kısıtlayıcı sinapslerle birbirlerine bağlanmıştır. Sayısal hesaplamalar sonucunda 2, 3 ve 4 nörondan oluşan ağda eş faz, zıt faz ve N-faz senkronizasyon davranışlarının oluşturulabileceği gösterilmiştir.

TSMC 0.18μm teknolojisi kullanılarak 2 ve 3 nöronlu zincir bağlı ağ yapısının devresi gerçekleştirilmiştir. Zayıf kuplajdan dolayı sinaptik akımlar VLSI devre olarak gerçeklemek için çok düşük kalırlar. Bu nedenle akımları VLSI olarak gerçeklenebilir sınırlara çekmek için birtakım ölçekleme işlemleri gerçekleştirilmiştir. Devre simülasyonlarında, beklenen eş faz, zıt faz ve N-faz senkronizasyon davranışları başarıyla gözlemlenmiştir. Güç tüketimi 2 nörondan oluşan ağ için 282 nW, 3 nörondan oluşan ağ içinse 320 nW olarak bulunmuştur.

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1. INTRODUCTION

1.1 Motivation

We constantly receive sensory input from our environment. We process this information and recognize food, environment or danger and take the appropriate actions. Animals show this behaviour spontaneously with apparent ease. The reason of this performance lies in our neural structure or brain [1]. The elementary processing units of brain are the nerve cells, or neurons. Neurons are believed to be the key elements in signal processing. Those cells are analog units that work together to carry out the highly sophisticated computations in cognition and control [2]. There are approximately 10^{11} neurons in the human brain, and each can have more than 10^4 synaptic connections with neighbouring neurons.

Today we still do not have sufficient knowledge about how the whole brain works but there is detailed knowledge about the structure and functionality of small portions of the brain. Studying the brain functionality and operation give us hope to design biological neural systems for brain-like performing systems, Brain Machine Interfaces (BMI) or intelligent machines in future. Thus, modeling of biological neural systems have been an attractive research area for engineers from past to date.

In traditional artificial neural networks, the neuron behavior is described only in terms of firing rate, but most of the real neurons, commonly known as spiking neurons, transmit information by pulses called action potentials or spikes. Spiking neuron models vary from the computationally simple Integrate and Fire (I&F) model to biologically meaningful Hodgkin-Huxley (HH) model. The network constructed with those models are called Spiking Neural Network (SNN). According to accuracy requirements and electronically easeness of implementation the appropriate model is selected for implementing the network.

Neurons communicate with each other through the units called synapses. Synapses play a crucial role in information transfer between the neurons. Due to synaptic dynamics, important properties exist in a network such as cognition, learning,

synchronization, memory etc. Thus far, many neuron models were proposed [3-12] for explaining the behaviour of a neuron but, until now, none of these models has considered the function of the synapses. So the modeling of synaptic transmission has crucial importance for understanding the neuronal activitiy of brain.

Today, SNNs has become essential to study the brain functions for Artificial Network Community. From literature research we extracted that the basic units and mechanisms, given below, should be appropriately modeled for investigating the real behaviour of a brain as SNN:

- Dynamics of single neuron cell.
- Axonal delay.
- Dynamics of synapses.
- Coupling model of neuron cells.
- Connection topology of neuron cells.
- Permanent modification in synaptic efficacy (i.e Long Term Plasticity - LTP or Long Term Depression - LTD)
- Temporary modification in synaptic efficacy (i.e Shot Term Plasticity - STP or Term Depression - STD)
- Effect of neromodulators to network dynamics.

First, third and fourth issues are the most curicial topics for realistic brain modeling as we mentioned in previous pharagraphs. In this work, we especially focused on those topics and offered a new dynamical neuron and synapse model completely appropriate for VLSI (Very Large Scale Integration) implementation.

Analog controllers are more attractive than the digital ones because of the increasing demand for real-time adaptability to environment. It is very diffucult to process large amounts of sensory input from natural environment with digital circuits [13]. This systems are still designed by digital approach that causes to speed, area and power limitations. Recently, by inspiring from the living organisms, to deal with mentioned problems signal processing neural system (i.e brain) has been investigated and the analog processing has get great importance. Design of the circuits that mimics the behaviour of the single neuron has been commenced while signal processing

mechanism of the brain is still trying to be understood by the researchers. Emergence of neurocomputer notion has increased the interest to design of the electronic neuron cell, also.

Neural networks consist of electronic neuron cell have the below advantages when compared with the digital systems:

- High processing capacity.
- Area efficient.
- Consumes Low power so more appropriate for biomedical applications.

1.2 Purpose of Thesis

There are many mathematical models that mimic the electrical activity of a neuron membrane in literature. Some of those models are too simple to show a real biological neuron dynamics but effective to use in numerical simulations and have the advantage of implementation easiness as an electronic circuit. Others mimic real neuron behaviour succesfuly but electronic circuit implementation is so diffucult and it takes so much time to integrate those models in numerical simulations. Electronic implementability is not an design constraint for most of them since they are not offered with engineering point of view. Another insufficiency of those models is that none of them has considered the function of the synapses. Synapses are dynamic units as neurons but in most of the synapse models, in literature, temporal dynamics are neglected and synapses are assumed as an instantaneous multiplier operators.

In this thesis, based upon the discussions mentioned above we determined a roadmap that aims to implement the below requirements:

- A new neuron model suitable for low power and compact VLSI implementation should be offered. Model should operate at biological timescale and biological voltage scale. With offered model, one should obtain nearly all of the major spiking templates of real biological neurons by only modifiying a few parameters.
- A new synapse model and coupling method suitable for low power and compact VLSI implementation should be offered. Coupling method should

support the summation property of the synaptic currents and temporal dynamics property of synapses should be included in synapse model.

- By using offered models, synchronization behaviour of coupled neurons with ring topology should be studied as an application. At this step, in phase, anti phase and N phase synchronizations should be observed.
- VLSI circuit of offered neuron and synapse model and ring coupled network should be implemented.

Numerical analysis and other calculations are planned to perform with MATLAB program and VLSI circuit design and simulations with Cadence and LTSpice Tools, in this work.

1.3 Thesis Structure

In section 2. the biological neuron dynamics and mechanism behind its electrophysiological behavior is introduced. Brief explanations about some important mathematical neuron models are mentioned.

In section 3. real chemical synapse behaviour is introduced and synaptic transmission flow is explained in detail. Brief explanations about some important mathematical synapse models in literature is introduced.

In section 4. synchronization phenomena is introduced. As an application, synchronization analysis is performed for ring coupled neural network. In this analysis we used Adaptive Exponential Integrate and Fire (AdEx I&F) model for neurons and the modified version of model given in [14] for synaptic connection and coupling rule.

In section 5. a new biological neuron model suitable for low power and compact VLSI implementation is introduced. Derivation of the model equations and neurocomputational features of the model are explained in detail. Also, it is shown that the most of the spiking patterns exhibited by real neurons are obtained with offered model.

In section 6. low power and compact VLSI implementation of offered neuron model is explained. Detailed design of the sub-blocks are mentioned. Tonic spiking and bursting patterns obtained from circuit simulations are shown in this section.

Verification and Layout implementation of designed circuit is expressed. This section is concluded by making a comparison between our design and other similar works in the literature.

In section 7. a new dynamic synapse model and a synaptic connection rule is explained. Phase Response Curve (PRC) of offered neuron model is extracted for determining the synchronization capability of neuron under the influence of synaptic inputs. Then synchronization behaviour of a ring coupled neural network composed of offered neuron and synapse model is investigated by numerical simulations and as a result, in phase, anti phase and N phase synchronization patterns are obtained.

In section 8. low power and compact VLSI circuit implementation of offered synapse model is also introduced. Circuit simulations are performed for ring coupled network with 2 and 3 neuron by connecting the previously designed neuron circuit with this synapse circuit. Then synchronization behaviour of network circuit is investigated.

In section 9. thesis is concluded with a brief explanation of the things had done in this work.

2. NEURON AND ITS DYNAMICS

If we carry out the voltage measurements across the membrane using an intracellular electrode in any cell it is seen that there is a voltage difference between inside and outside of cell membrane. That voltage difference called membrane potential. This potential is used to transmit signals in neurons. Neurons communicate with each other via this electrical signals which are called action potentials or spikes. The spike signal is an essential measurument of a neuron's activity [15].

2.1 Mechanism Behind the Action Potentials or Spikes

Action potentials play a crucial role among the many mechanisms for communication between neurons. Action potentials are generated and sustained by ionic currents through the cell membrane. The ions that are mostly contributed to this mechanism are sodium, Na^+, calcium, Ca^{++}, potassium, K^+, and Cl^-, chloride. Basic mechanisms and elements resulting to firing of spikes in neurons is shown in Figure 2.1. In the simplest case an increase in the membrane potential activates Na^+ and/or Ca^{++} channels, resulting in rapid inflow of the ions and further increase in the membrane potential. Such positive feedback leads to sudden growth of the potential. This triggers a relatively slower process of inactivation of the channels and/or activation of K^+ channels, which leads to increased K^+ current and eventually reduces the membrane potential. These simplified positive and negative feedback mechanisms are responsible for the generation of action potentials [2].

Positive and negative feedback loops resulted in excited behaviour in neurons is shown in Figure 2.2. According to this figure we can summarize the simple chemical and electrical process of spike generation as:

1. Na^+ channels are opened and Na^+ ions begin to enter inside the cell. This inward current depolarizes the membrane voltage. This voltage increase (i.e. depolarization) causes the activation of more channels resulting in further depolarization. This positive feedback loop results in the sudden upstroke of membrane potential.

2. K^+ channels are opened K^+ ions begin to leave the cell. This causes slow outward current. Na^+ current continues to enter inside the cell. So depolarization phase goes on.

3. Na^+ channels becomes refractory no more Na^+ ions enter into the cell. Inactivation of Na^+ current begins.

4. Inactivation of Na^+ current continues. K^+ continues to leave the cell. Total current repolarize the membrane voltage. This voltage decrease (i.e. repolarization) causes the inactivation of more Na^+ channels and activation of less K^+ resulting in further repolarization. This negative feedback loop results in the sudden downstroke of membrane potential.

5. K^+ channels close and Na^+ channels reset. This forces the membrane potential to return the resting potential. So repolarization phase goes on.

6. Extra K^+ diffuses away outside of neuron. This outward current results membrane voltage to go below resting potential. This phase is called after hyperpolarization.

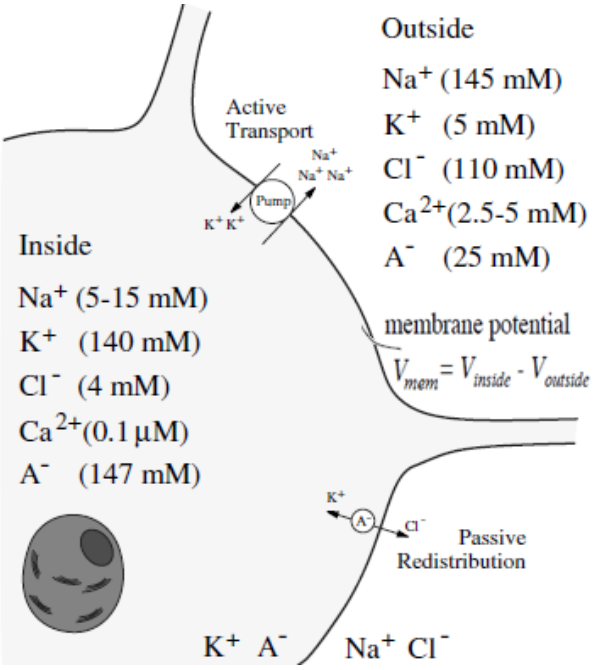


Figure 2.1 : Basic elements resulting to action potential in a neuron [19].

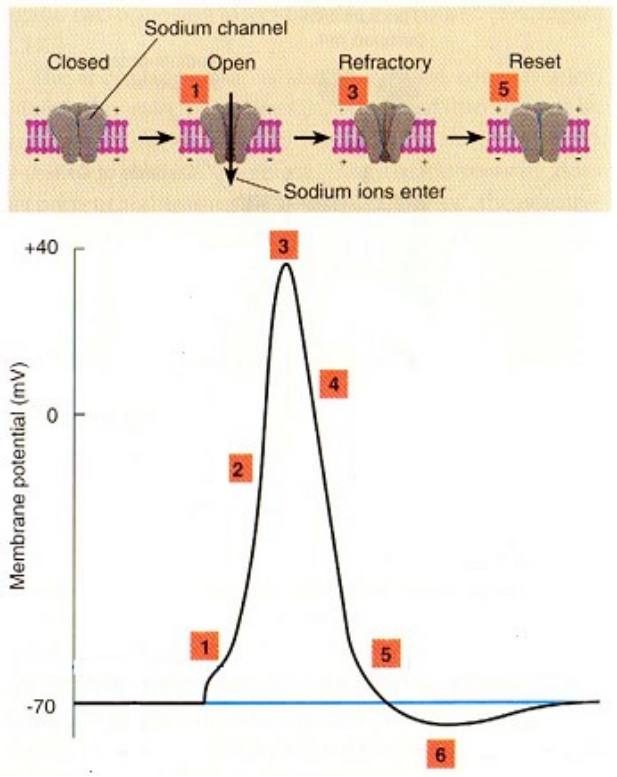


Figure 2.2 : Positive and negative feedback loops resulting in action potential in neurons.

Functional parts and electrical properties of neurons is shown in Figure 2.3 [16]. The nonlinear ionic conductances in Figure 2.3(b) are voltage dependent and correspond to different ion channels. Amplitue of typical spike is on the order of 100 mV and has 1-2 ms duration, and is followed by a longer after-hyperpolarization period called refractory period during which the neuron is less likely to generate another spike [16]. Simple signal flow mechanism between the neighbouring neurons can be summarized as:

- The neuron receives inputs through synapses on its dendritic tree.
- These inputs cause to generation of a spike at the spike generation zone of the cell body.
- Generated spike travels down to the axon and triggers the chemical transmitter release in the synapses of the axonal tree.
- Released transmitters activates the postsynaptic neuron and the process is repeated.

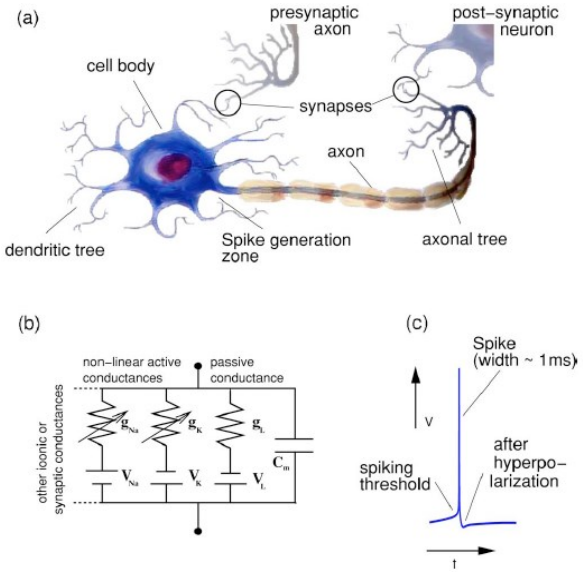


Figure 2.3 : Illustration of the functional parts and electrical properties of neurons. (a) Simple neuron and its connections to other neurons. (b) Electrical circuit equivalent for a membrane patch of a neuron. (c) typical spike shape [16].

2.2 Modeling of Neuron Dynamics

Classical (i.e. artificial) neuron model offered by Mc. Cullach and Pitts [12] in 1943 has been a fundamental work for latter models. This model was too simple to model the real behaviour since it has many assumptions like the neuron activity is based on all-or-none principle, synapses can be represented with constant weights etc. Today's understanding and methods of modeling the neural excitability have been signicantly influenced by the work of Hodgkin and Huxley in a series of five articles published in 1952. These investigators explained the key properties of the ionic conductances underlying the nerve action potential [9, 17]. This model's parameters are biophysically meaningful and measurable but extremely expensive to implement. Because of the complexity of the Hodgkin-Huxley model (HH), reduced models has been proposed. In 1961 FitzHugh has investigated the phase portraits of HH by using bifurcation parameters and proposed a simpler model called FitzHugh-Nagumo Model [3]. In 1981, conductance based Morris–Lecar model [11] that has a two-dimensional system of nonlinear differential equations is offered. It is considered a simplified model compared to the four-dimensional Hodgkin-Huxley model. In 1984 Hindmarsh and Rose reinvestigate the FitzHugh-Nagumo model and proposed 3th degree Hindmarsh-Rose equations by resolving the insufficiencies of this model [8]. Several different models have been proposed until the beginning of the year 2000 but

these models have not obtained the popularity. New models and circuit implementations have occured in last decade because of the better understanding of neuron behaviour and devolopment in technology that leads to realization of the highly integrated neural networks. There are also models offered especially after year 2000, that combine continuous spike-generation and a discontinuous 'after-spike' reset of state variables [18]. These are called hybrid neuron models[6, 7]. While the goal of Hodgkin-Huxley type conductance based models are matching the neuronal electrophysiology with biophysically meaningful and measurable parameters, hybrid models aim to match the neuronal dynamics with mathematically meaningful state equations.

2.2.1 Present neuron models

In this work, proposed model should have the below properties

- Should mimic the behaviour of the real neurons
- Should be appropriate for electronic implementation
- Should have the controlable parameters.
- Should have simple numeric calculations since the simulation phase takes long time because of the many neurons and connections in a network.

In any study of network dynamics, there are two crucial issues which are the model that describes the spiking dynamics of each neuron and the connection rule of neurons [4]. An important result of the Hodgkin-Huxley studies is that "neurons are dynamical systems". A dynamical system consists of a set of variables that describe its state and a law that describes the evolution of the state variables with time. So, the state of the system in the next instant of time depends on the input and its state at the previous instant of time. Typically, all state variables describing neuronal dynamics can be classified into four classes, according to their function and the time scale [19].

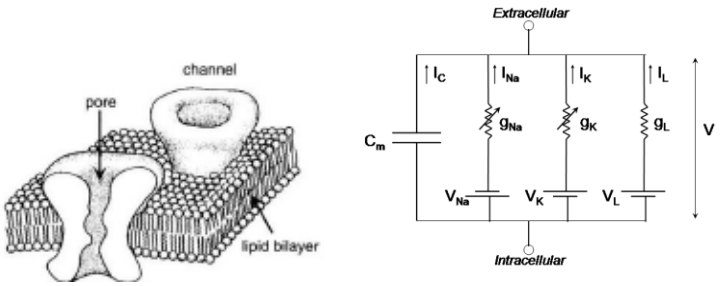
- Membrane potential.
- Excitation variables, such as activation of a Na^+ current. These variables are responsible for the upstroke of the spike.

- Recovery variables, such as inactivation of a Na^+ current and activation of a fast K^+ current. These variables are responsible for the repolarization (downstroke) of the spike.
- Adaptation variables, such as activation of slow voltage- or Ca^{++} dependent currents. These variables build up during prolonged spiking and can affect excitability in the long run.

As we stated in section 2.2 there are many neuron models in literature, we only summarized most important of them at the following sections. Comparison between the computational efficiency of most of those models are explained in [4].

2.2.1.1 Hodgkin-Huxley model (HH)

One of the most important model in computational neuroscience is the Hodgkin-Huxley model [9] of the squid giant axon. Using pioneering experimental techniques of their time, they determined the squid axon's electrical activity with four dimensional equation system [19]. This model is biophysicaly meaningful and have measurable parameters but not easily implementable as an electronic circuit because of its complexity as can be seen from equation (2.1). In this model each component of an excitable cell is assumed to be an electrical element as can be seen in Figure 2.4. All the conductance based models have similar equivalent circuit that only differs from each other with the ionic channels used in model. The lipid bilayer corresponds to capacitance (C), voltage-gated ion channels correspond to electrical conductances (g_{Na}, g_K), leak channels maps to linear conductances (g_L) and electrochemical gradients correspond to constant voltage sources (V_{NA}, V_K, V_L). Ratio of the inside and outside concentration of the related ions determine the value of those constant voltage sources called reversal potentials.



(a) (b)

Figure 2.4 : Membrane structure (a) Channel structure (b) Equivalent circuit representation of a patch of cell membrane of Hodgkin Huxley model.

$$C\frac{dv(t)}{dt} = I - g_K[n(t)]^4(v(t)-E_K) - g_{Na}[m(t)]^3 h(t)(v(t)-E_{Na}) - g_L(v(t)-E_L)$$

$$\frac{dn(t)}{dt} = 0.01\frac{(10-v(t))}{\left(e^{\left(\frac{10-v(t)}{10}\right)}-1\right)}(1-n(t)) - 0.01e^{\left(\frac{-v(t)}{80}\right)}n(t)$$

$$\frac{dm(t)}{dt} = 0.1\frac{(25-v(t))}{\left(e^{\left(\frac{25-v(t)}{10}\right)}-1\right)}(1-m(t)) - 4e^{\left(\frac{-v(t)}{18}\right)}m(t) \qquad (2.1)$$

$$\frac{dh(t)}{dt} = 0.07e^{\left(\frac{-v(t)}{20}\right)}(1-h(t)) - \frac{1}{e^{\left(\frac{30-v(t)}{10}\right)}+1}h(t)$$

We can rewrite the above activation functions in standart form as in equation (2.2). Voltage dependent steady-state values and time constants of the functions in this equation shown in Figure 2.5.

$$\frac{dn}{dt} = \frac{n_\infty(V)-n}{\tau_n} \;;\; \frac{dm}{dt} = \frac{m_\infty(V)-m}{\tau_m} \;;\; \frac{dh}{dt} = \frac{h_\infty(V)-h}{\tau_h}$$

$$n_\infty = \frac{\alpha_n}{\alpha_n+\beta_n} \;;\; m_\infty = \frac{\alpha_m}{\alpha_m+\beta_m} \;;\; h_\infty = \frac{\alpha_h}{\alpha_h+\beta_h} \qquad (2.2)$$

$$\tau_n = \frac{1}{\alpha_n+\beta_n} \;;\; \tau_m = \frac{1}{\alpha_m+\beta_m} \;;\; \tau_h = \frac{1}{\alpha_h+\beta_h}$$

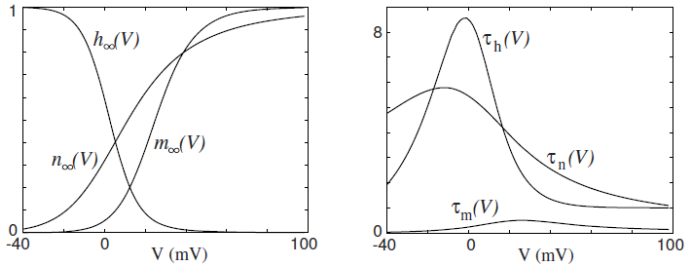


Figure 2.5 : Voltage dependent steady-state values and time constants of the functions in Hodgkin-Huxley model [19].

2.2.1.2 Moris-Lecar model

The Morris-Lecar model [11] is a conductance based, reduced and two-dimensional model. This model has biophysicaly meaningful parameters and a few fitting parameters. The model describes neurons as units with Ca^{++} and K^+ voltage gated ion channels and a constant leak current. Morris and Lecar used calcium and potassium channels because they found that the oscillatory behavior of the barnacle muscle

fiber's are depended on calcium and potassium concentration inside and outside of cell. The Morris-Lecar model can be represented with below equations**.**

$$C\frac{dv(t)}{dt} = I_{in} - g_K n(t)\left(v(t) - E_K\right) - g_{Ca}\left(\frac{1}{2}\left[1 + \tanh\left(\frac{v(t) - V_1}{V_2}\right)\right]\right)\left(v(t) - E_{Na}\right) - g_L\left(v(t) - E_L\right)$$
$$\frac{dn(t)}{dt} = \phi\cosh\left(\frac{v(t) - V_3}{2V_4}\right)\left(\frac{1}{2}\left[1 + \tanh\left(\frac{v(t) - V_3}{V_4}\right)\right] - n(t)\right) \tag{2.3}$$

where *v(t)*, membrane potential, *n(t)*, recovery variable, *C*, membrane capacitance, I_{in}, input sitimuli current, g_K, g_{Ca} and g_L are potassium, calcium and leak conductances respectively, E_K, E_{Na} and E_L are potassium, calcium and leak resting potentials respectively, $(1/\phi)$, timescale for recovery, V_1, V_2, V_3 and V_4 are voltage clamp data fitting parameters.

2.2.1.3 Fitzhugh-Nagumo model (FN)

Fitzhugh-Naguma model [3] is a two-dimensional model that can be derived from HH model via reduction of variables. This model is offered by investigating the geometrical represantation of dynamical behaviour of HH model. It is a typical example of relaxation oscillator. If the external input exceeds a certain threshold value, the system will follow a characteristic trajectory at phase space before variables *v(t)* and *w(t)* relax back to their resting values as can be seen in Figure 2.6. The model is not biophysically meaningful but appropriate for electronic implementations [20, 21]. Main drawback of this model is lack of modeling of bursting behaviour. Generic form of model equation is given by:

$$\frac{dv(t)}{dt} = f(v(t)) - w(t) + I_{in} = p_1 v(t) + p_2\left[v(t)\right]^2 + p_3\left[v(t)\right]^3 - w + I_{in}$$
$$\tau\frac{dw(t)}{dt} = p_4 v(t) - w(t) + p_5 \tag{2.4}$$

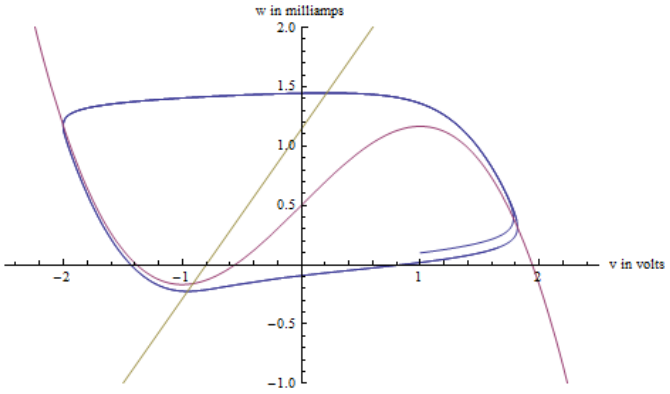


Figure 2.6 : Trajectory of FitzHugh-Nagumo Model in phase space and nullclines for $p_1=1$, $p_2=0$, $p_3=-(1/3)$, $p_4=(5/4)$, $p_5=(7/8)$, $\tau=(125/8)$.

2.2.1.4 Hindmarsh-Rose model (HR)

The Hindmarsh-Rose [8] model solves some of the deficiencies offered by the FN model, but adds complexity which makes the analysis more difficult. So this is an enhanced case of Fitzhugh-Nagumo model. It is preferred because of having rich membrane dynamics including bursting behaviour. This model is not biophysically meaningful but not too complex as HH model for circuit implementation. An important implementation of this model is presented in [13]. And also, in [22] circuit is designed by using subthreshold technique and used in a robot design. General form of the model equations can be written by:

$$\begin{aligned} \frac{dx(t)}{dt} &= y(t) - F(x(t)) + I - z(t) \\ \frac{dy(t)}{dt} &= G(x(t)) - y(t) \\ \frac{dz(t)}{dt} &= \frac{H(x(t)) - z(t)}{\tau} \end{aligned} \tag{2.5}$$

where F, G and H are some functions. Depending on their choice, the model can, in principle, exhibit all of the neuro-computational properties. In the best case that functions are polynamials of the third degree [23] as:

$$\frac{dx(t)}{dt} = y(t) - x^3(t) + 3x(t) + I - z(t)$$
$$\frac{dy(t)}{dt} = 1 - 5x^2(t) - y(t) \qquad (2.6)$$
$$\frac{dz(t)}{dt} = \frac{s(x(t) - x_1) - z(t)}{\tau}$$

where τ controls the speed of variation of the slow variable *z(t)* it governs the spiking frequency, whereas in the case of bursting, it affects the number of spikes per burst, *s* governs the adaptation capability of neuron and x_{rest} sets the resting potential of the system [24].

2.2.1.5 Integrate and fire model (I&F)

Because of the simplicity this is one of the most widely used and best known model of spiking neurons in computational neuroscience [25, 26]. As it can be seen from equation (2.7) this model has only one variable. It lacks an intrinsic spike-generation mechanism so it is called a threshold model. If *v(t)* goes beyond a certain threshold V_{thres}, a spike is said to be fired. Despite its simplicity, it is one of the worst models to use in simulations [4].

$$\frac{dv(t)}{dt} = I + a - bv(t), \qquad if \quad v \geq V_{thresh}\, then \leftarrow c \qquad (2.7)$$

This model is based on, and most easily explained by, principles of electronics. Spike travels down the axon and is transformed by a low-pass filter, then this filter converts the short input into a current pulse that charges the integrate and fire circuit. Once the voltage goes above threshold value the neuron sends out a pulse itself [27].

2.2.1.6 Resonate and fire model (R&F)

The resonate-and-fire neuron [5] is a two-dimensional (2-D) analogue of the I&F neuron. Minimal modificaions is made to I&F model to exhibit the damped oscillations. A circuit implementation of this model is explained in [28]. Model equations are given by:

$$\begin{aligned} \frac{dx(t)}{dt} &= bx(t) - \omega y(t) \\ \frac{dy(t)}{dt} &= \omega x(t) + by(t) \\ \frac{dz(t)}{dt} &= (b + i\omega)z(t) \rightarrow z(t) = x(t) + iy(t) \\ if\ \mathrm{Im}\{z(t)\} &= a_{thresh}\ \ then\ \ z \leftarrow z_0(z) \end{aligned} \tag{2.8}$$

Here, *z(t),* is a complex-valued variable that describes oscillatory activity of the neuron. The real part, *x(t),* is the current like variable. It describes dynamics of voltage-gated and synaptic curents. The imaginary part, *y(t),* is the voltage-like variable [5].

2.2.1.7 Exponential integrate and fire model (Ex I&F)

This model [29] is the most realistic one among the one dimensional models but it has no analytic solution and exponential term makes the calculations difficult. A circuit implementation of this model is explained in [30]. Model equation is given by:

$$C\frac{dv(t)}{dt} = -g_L(v(t) - V_L) + g_L\Delta_T e^{\left(\frac{v(t)-V_T}{\Delta_T}\right)} \tag{2.9}$$

2.2.1.8 Izhikevich model

Izhikevich has investigated the phase portraits and equilibrium graph of neuron cells and show that all dynamic behaviour of this cells can be explained by 4 different bifurcation. By using the results of this investigation he proposed his own model [6]. This model is not biophsicaly meaningful but is simple for numeric calculations and can exhibit firing patterns of all known types of cortical neurons, as can be seen in Figure 2.7, with the choice of appropriate parameters. This is the most widely used realistic neuron model. There are many circuit implementation of this model [31-34].

$$\frac{dv(t)}{dt} = 0.04v^2(t) + 5v(t) + 140 + I - u(t)$$
$$\frac{du(t)}{dt} = a(bv(t) - u(t)) \qquad (2.10)$$
$$if \;\; v \geq +30mV, \quad then \;\; \begin{cases} v \leftarrow c \\ u \leftarrow u + d \end{cases}$$

where *v(t)* corrresponds to the membrane potential, *u(t)* corresponds to a slow membrane recovery variable, *I* corresponds to the stimuli input current, *a* represents the time constant of slow variable, *b* represents the sensitivity of slow variable to the subthreshold oscillations, *c* and *d* after spike reset value of membrane potential and slow variable, respectively.

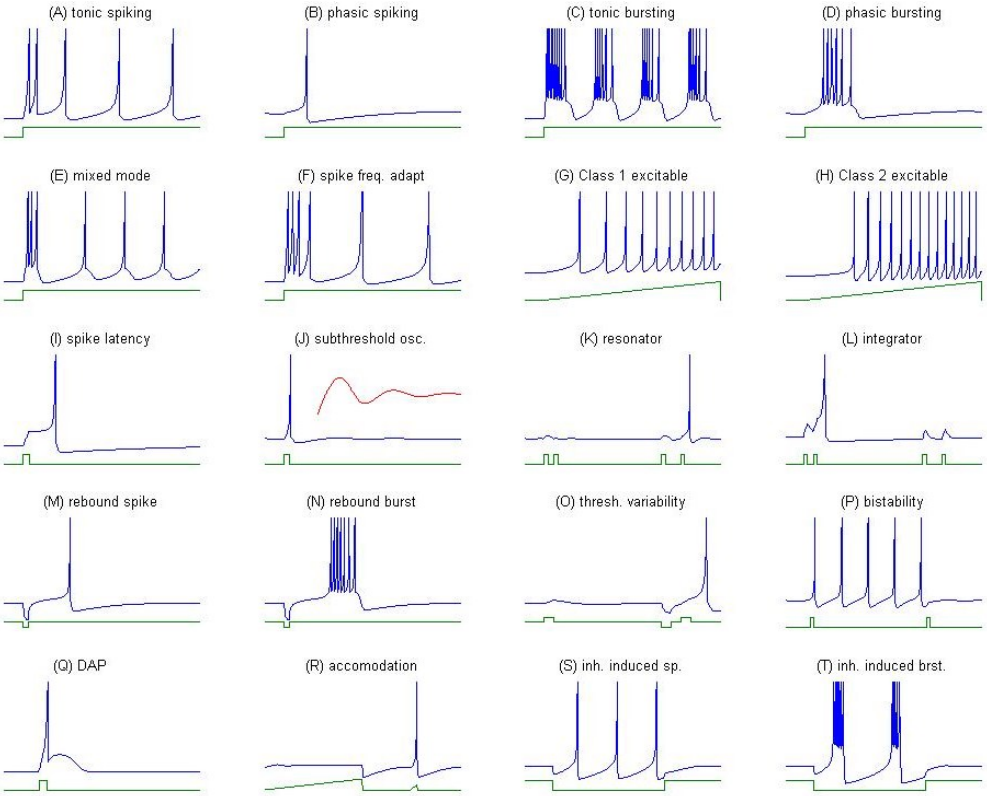


Figure 2.7 : Summary of the neuro-computational properties of biological neurons obtained by Izhikevich Model [4].

2.2.1.9 Adaptive exponential integrate and fire model (AdEx I&F)

This model [7] is the combination of Exponential Integrate&Fire [29] and Izhikevich [6] model. Dynamics of the model has been investigated detailed in [35, 36]. This model is biophysically meaningful. A low power circuit implementation of the model is explained in [37, 38]. This model is described by two variables, the membrane

potential *v(t)* and an adaptation current *w(t)*, whose dynamics are governed by the following differential equations [35]:

$$C\frac{dv(t)}{dt} = -g_L(v(t) - V_L) + g_L\Delta_T e^{\left(\frac{v(t)-V_T}{\Delta_T}\right)} - w(t) + I$$
$$\tau_w \frac{dw(t)}{dt} = a(v(t) - E_L) - \omega(t) \tag{2.11}$$
$$if\ v \geq 0mV, \quad then \quad \begin{cases} v \to V_r \\ w \to w_r = w + b \end{cases}$$

where *v(t)* represents the membrane potential, *w(t),* adaptation variable, *C,* membrane capacitance, *I,* synaptic current, g_L, leak conductance, V_L, resting potential, Δ_T, slope factor, V_T, threshold potential, τ_w, time constant of the adaptation variable. Also *a* parameter represents the level of subthreshold adaptation, V_r is after spike reset value and *b* is increment value of adaptation variable applied at instant of spike formation.

3. SYNAPSES AND SYNAPTIC DYNAMICS

Charles Sherrington introduced the term synapse in 1897. He used this term for describing the specialized structure at the contact zone between neurons as the point in which they communicates with each other. If we consider a neuron as a signal processing device, its inputs are the frequency of pulses received at the synapses, and its output is the frequency of action potentials generated on axon. If an incoming spike from a presynaptic neuron causes an increase/decrease in membrane potential of postsynaptic neuron then this kind of synapse is called excitatory/inhibitory. Thus far, many neuron models were proposed for explaining the activitiy of a neuron as it is discussed in section 2. However, until now, none of these models has considered the function of the synapses. Therefore, those models cannot explain the basic signal processing characteristics of the neuron in principle [39]. So the modeling of synaptic transmission has crucial importance for understanding the neuronal activitiy of human.

3.1 Synaptic Transmission

There are two types of synapses, one is called chemical and the other is electrical. Electrical synapses conduct action potentials faster than chemical synapses but they don't have gain or loss which means they transfer the incoming signal directly. Electrical synapses are important for neural systems that require the fastest possible response and for arranging the synchronous behaviour in some specific networks. Chemical synapses are primary units for synaptic transmission between neurons. Most neuron cells communicate via chemical synapses. Those are separated by a space called a synaptic cleft that have the avarage length of 20 to 30 nanometers. Because of synaptic cleft, presynaptic neuron can not transmit action potentials directly to the postsynaptic neuron. At this point, chemicals called neurotransmitters are utilized to transfer the signal from presynaptic to postsynaptic cells. Some neurotransmitters depolarize the postsynaptic cell and called excitatory while the others hyperpolarize the postsynaptic cell and called inhibitory. Excitatory/Inhibitory

synapses increase/decrease the probability of firing of postsynaptic neuron. The summary of sequence of steps in synaptic transmission is shown in Figure 3.1. From this figure step by step explanation of transmission can be summarized as:

1. Depolarization of the presynaptic neuron's cell membrane.
2. Calcium entry into presynaptic neuron through voltage-gated calcium channels.
3. Calcium transport and merging with synaptic vesicle. Synaptic vesicles are synthesized in the cell body (A) and transported to the terminal (B), where they are filled with transmitter.
4. Priming of synaptic vesicle.
5. Docking of synaptic vesicle.
6. Fusion of the vesicle with the membrane, releasing neurotransmitter.
7. Diffusion of the neurotransmitter across the synaptic cleft
9. Binding of transmitter to the postsynaptic neuron's receptor.
10. Change in the conductance of postsynaptic neuron cell membrane
11. To terminate the synaptic action, transmitter is metabolized (8) or removed from the cleft by reuptake (8a) or recycled by uptake (8b) and refilled with transmitter.

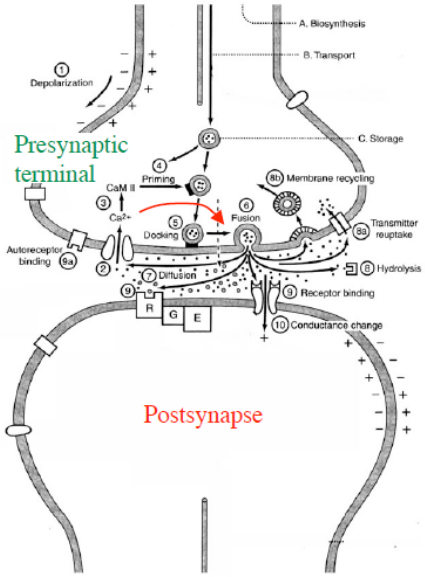


Figure 3.1 : The sequence of steps in synaptic transmission. Modified from [40].

3.1.1 Synapse models

Synaptic transmission is highly dynamic and stochastic process since many biophysiological phenomena contribute to this activity, as can be clearly seen from Figure 3.1. This makes the modeling of synapses so challenging task that require numerous simplifications and abstractions. Furthermore, synaptic transmission is believed to be an important source of noise in the nervous system [41]. A few simple models of synaptic transmission is given in [41] in detail.

A good synapse model based on physiology is given in [39]. In this work, a synaptic current model that well matches with the previously mentioned synapse behaviour is given by equation (3.1). The relationship between membrane potential and ion currents across the membrane is shown in Figure 3.2. The synaptic current onto neuron j is the linear sum of the currents of all incoming synapses $I_{in,j} = \sum I_{in,ji}$ where the individual currents are:

$$\begin{aligned} I_{in,ji} &= g_{ij} S_i (V_j - V_{rev}) \\ \tau \frac{dS_i}{dt} &= (R_i - \kappa S_i) \frac{S_{\max} - S_i}{S_{\max}} \\ \tau \frac{dR_i}{dt} &= \Theta(V_i - V_{th}) - R_i \end{aligned} \tag{3.1}$$

where the threshold potential for transmitter release is V_{th}= *-20 mV*, the synaptic time scale τ=*50 ms*, the maximal fraction of postsynaptically bound transmitter S_{max} = 0.045, the relative rate of transmitter binding and unbinding κ= 1/2, and Θ denotes the Heaviside step function. R_i is a measure of the amount of neurotransmitter released presynaptically and S_i the fraction of postsynaptically bound neurotransmitter [39].

In many neural network applications, pulse coupling method has great importance as synaptic connection rule. In this approach, each firing of pre-synaptic neuron produces a pulse with the amplitude of real valued constant g_{ij} that contributes to post-synaptic neuron's stimulation. But pulse-coupled neural networks are to simple models. They are based on abstractions of important properties of biological neurons but stil far away from the reality. Consequently, all results obtained by using pulse-coupled mechanism might not be truly model the brain.

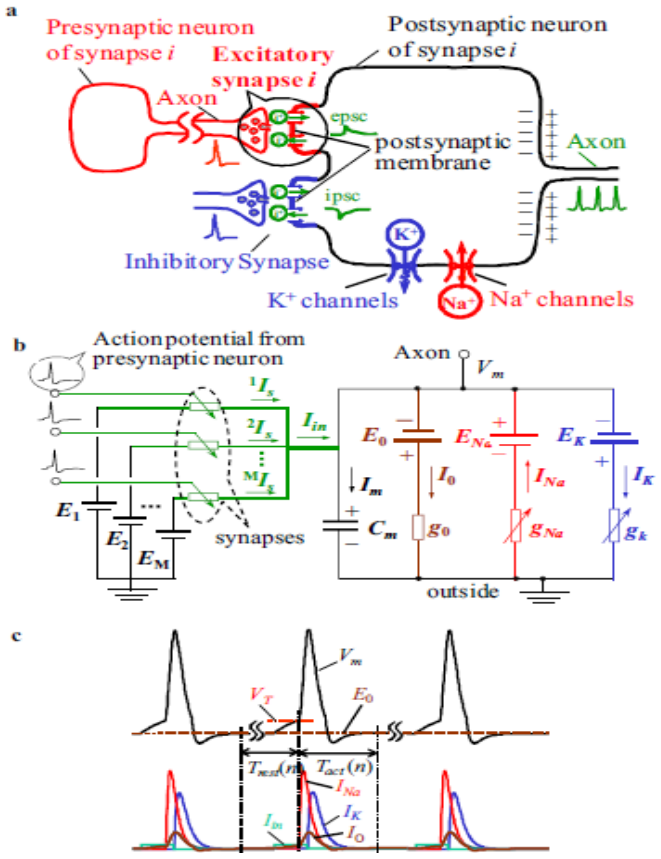


Figure 3.2 : The relationship between membrane potential and ion currents across the membrane. a) Illustration of the electrical mechanism of a neuron. b) Equivalent circuit of a neuron c) The membrane potential caused by the ion currents across the membrane [39].

For I&F neurons pulse coupling method can be de defined as in equation (3.2). Here, g_{ij} is synaptic coefficient, δ is the Dirac delta function and t_j^* is the nearest moment of firing of the j^{th} neuron.

$$\frac{dV_i}{dt} = a_i - b_i V_i + \sum_{j=1}^{n} g_{ij}\delta(t - t_j^*) \tag{3.2}$$

Another important concept for synapses is synaptic plasticity. It was first proposed as a mechanism for learning and memory on the basis of theoretical analysis [42]. The plasticity rule, proposed by Hebb, claim that when one neuron drives the activity of another neuron the connection between these neurons is potentiated. Effect of this mechanism causes the changing of synaptic efficacy. Theoretical analysis indicates that not only potentiation is necessary but also depression can occur between two neurons that are not sufficiently coactive. Synaptic plasticity is not in the scope of this thesis.

4. SYNCHRONIZATION AND AN APPLICATION

Synchronization phenomena in coupled systems are very important models to describe various higher dimensional nonlinear phonomena in the field of natural science [43]. We can briefly describe the synchronization as an adjustment of rhythms of oscillating systems due to their weak interaction. Neural networks have the ability of producing some kinds of phase patterns, and thought to be utilized for associative memory, image processing etc. [44-46]. Synchronized activity of neurons takes role in a wide range from cognitive functions to rhythmic movements of animals. Coupled neurons (in general oscillators) can show inphase synchronization behaviour if the phase difference is zero, antiphase if the phase difference is close to 180° and N-phase if the phase difference is arbitrary.

There is a good application of this phonemena in [47]. In this work Central Pattern Generator (CPG) is modeled by coupling the oscillators to generate the swimming and walking motion of a salamender as can be seen from Figure 4.1.

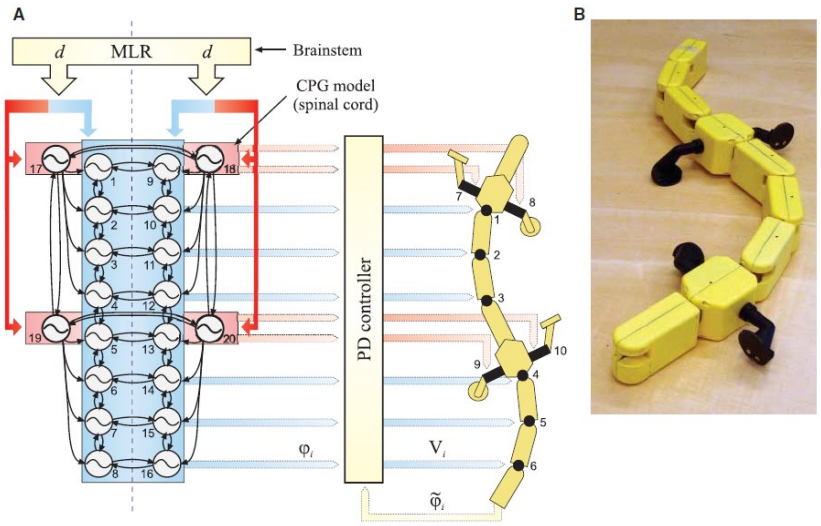


Figure 4.1 : Configuration of the CPG model B Salamander Robot [47].

4.1 An Example Synchronization Analysis

As a combination of issues discussed until now, for studying the synchronization behavior, we constructed a ring coupled neural network, as shown in Figure 4.2, by

using the previously mentioned AdEx I&F model for neurons and a modified version of connection rule given in [14] for coupling between the neurons. The state equations of this system for *N* neurons is given by equation (4. 1).

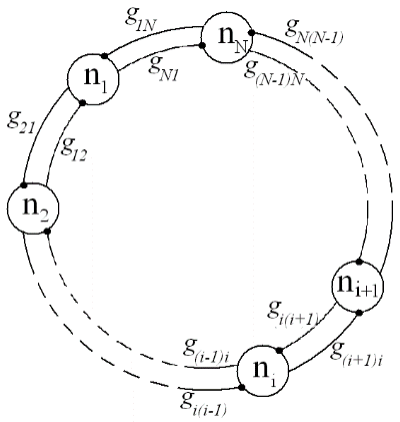


Figure 4.2 : Neural network topology with ring of neuron cells.

$$
\begin{aligned}
C\frac{dV_i}{dt} &= -g_L(V_i - V_L) + g_L\Delta_T e^{\left(\frac{V_i - V_T}{\Delta_T}\right)} + z_i(V_i - V_{re}) - w_i + I \\
\tau_w \frac{dw_i}{dt} &= a(V_i - E_L) - w \\
\tau_z \frac{dz_i}{dt} &= g_{i(i+1)} \frac{1}{\left(1 + \exp\left(\frac{0.5 - V_{i+1}}{20}\right)\right)} + g_{i(i-1)} \frac{1}{\left(1 + \exp\left(\frac{0.5 - V_{i-1}}{20}\right)\right)} + z_i \qquad (4.\ 1) \\
\text{if } V_i \geq 0mV, \quad \text{then } &\begin{cases} V_i \to V_r \\ w_i \to w_r = w_i + b \end{cases}, \quad i = 1,2,3,....,N
\end{aligned}
$$

The Phase Response Curves (PRC), i.e. the neuron's response to weak perturbations, usually suffices to understand the collective dynamical properties of a neuronal sytem or network. This curve is extracted for given neuron model. If the curve takes positive and negative values (type II) that means that the model can synchronize in a network. PRC extraction method will be explained in detail at section 7. In the light of mentioned issues we extracted the PRC of AdEx model used in example and defined the neuron parameters as the model will have the synchronization capability. Result of this extraction is shown in Figure 4.3.

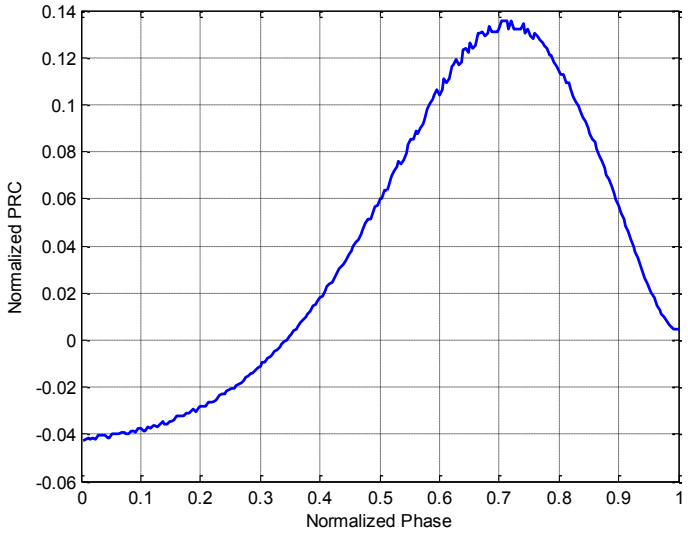


Figure 4.3 : PRC (type II) of AdEx neuron used in example.

In our design example model parameters (C, g_L, V_T, D_T, V_{re}, I, a, τ_ω, E_L, τ_z, V_r, b) are the same for each neuron in network. The coupling parameters (c_{ij}) are chosen as the network will show the N-phase synchronization behaviour. An example snapshot of the output of MATLAB analysis from the example work is given in Figure 4.4. Design parameters are given on the left column of the snapshot.

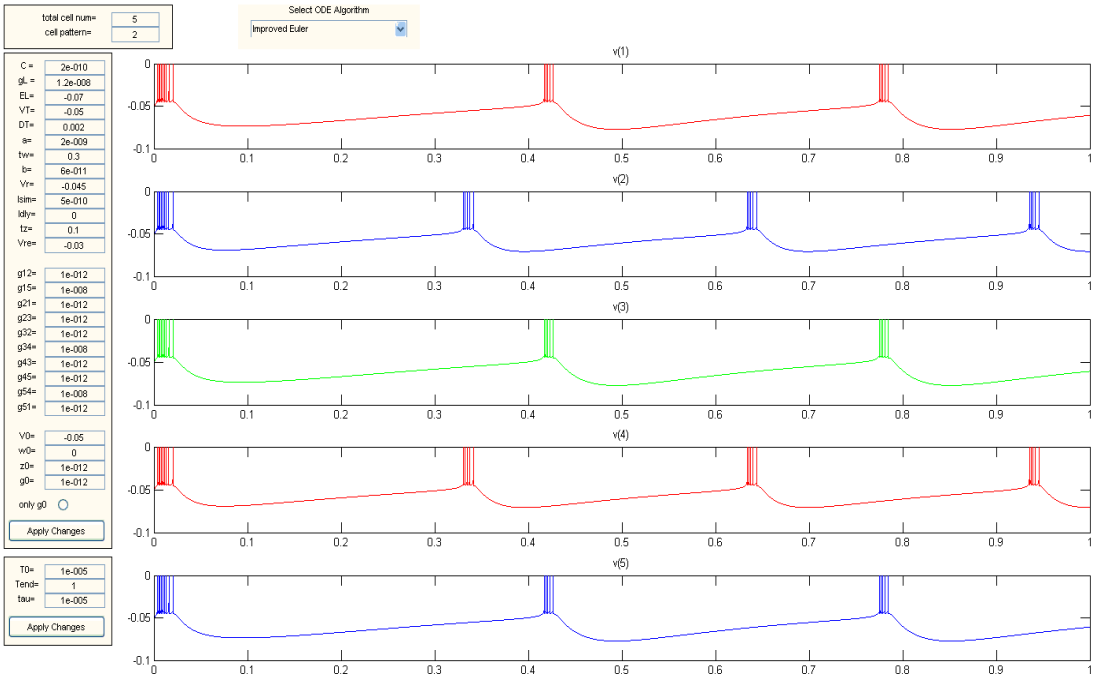


Figure 4.4 : N-phase synchronization of the five AdEx neurons in a ring coupled network.

5. NEW NEURON MODEL

Many spiking neuron models have similar dynamic features. When we have examined the geometrical phase plane analysis of various two-dimensional neuron models, we saw that the common feature of these models are having a fast membrane voltage variable and a slower adaptation current variable. Typically, the fast variable has an N-shaped nullcline and the slower variable has a sigmoid or linear shaped nullcline [19]. Morris-Lecar [11] and FitzHugh-Nagumo [3] is the two most important examples to these models. And also we observed that combining the after spike reset mechanism with these features results to obtain rich dynamic behaviour and spiking repertoir. Furthermore, after spike reset mechanism allows us to mimic the real spike timing.

By using the above facts we offered a new neuron model that can be included to the class of hybrid models as Izhikevich and AdEx I&F models. The main motivation was to construct a realistic neuron model which is completely appropriate for low power and compact VLSI circuit implementation. We know that the odd symetrical functions are more suitable for circuit implementation. So, new model is constructed with tangent hyperbolic functions since it is odd symetric and easily implementable as VLSI circuit by using subthreshold CMOS technique.

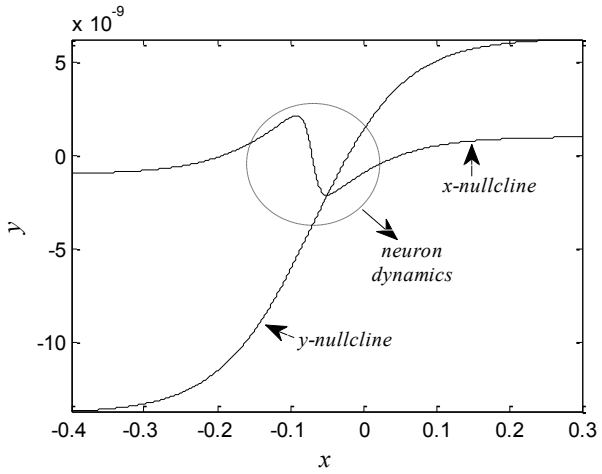


Figure 5.1 : Nullcline derivation of new neuron model. Neuron dynamics takes place in the N-shaped area marked with dotted circle.

When designing the new neuron model we used geometrical nullcline approach as shown in Figure 5.1. For N-Shaped nullcline we scaled two tangent hyperbolic functions (i.e. *[p_1*tanh(p_2*x) – p_3*tanh(p_4*x)]*) and for sigmoid(linear)-shaped nullcline we scaled one tangent hyperbolic function (i.e. p_5*tanh(p_2*x)). Scaling parameters, p_1, p_2, p_3, p_4 and p_5 are responsible for the scaling of the state variables. Then we included the bifurcation parameters and after spike reset mechanism to tangent hyperbolic constructed nullclines. Those bifurcation parameters cause to qualitative changes in the behavior of the system. Finally we arrived the 2-D dynamical system in (5.1) for modeling a real neuronal activity.

$$\tau_x \frac{dx(t)}{dt} = X_1 \tanh\left[\left(x(t)+X_o\right)X_{sy}\right] - X_2 \tanh\left[\left(x(t)+X_o\right)X_{sx}\right] - y(t) + I_{in}(t)$$

$$\tau_y \frac{dy(t)}{dt} = Y_1 \tanh\left[\left(x(t)+X_o\right)X_{sy}\right] - y(t) + Y_2 \qquad (5.1)$$

$$x(t) > X_{\max} \Rightarrow x(t) \leftarrow X_r$$

Offered model in (5.1) has ten parameters for defining the evolution of the state variables *x(t)* and *y(t)*. Parameter names are generic since they are not biophysically meaningfull. Offered model can operate in biological time scale and biological voltage scale by selecting the appropriate parameters. Model has similar nullclines, in operational area, with $I_{Na,p}$+I_K model resulting to equivalency in dynamic behaviour at the subthreshold ($x < X_{max}$) region. Model also includes the after spike reset mechanism as in hybrid models [6, 35]. Unlike Izhikevich and AdEx I&F model, only the membrane voltage *x(t)* is reset to constant reset value (X_r) after the spike reaches its maximum value (X_{max}) in our model. This is another big advantage of our model since implementing the hard reset of recovery variable *y(t)* requires large number of transistors which is a limiting factor for design of large-scale neuromorphic hardware[18]. Slow(recovery) variable grows to the desired 'after-spike' value on its own in our model as can be seen in Figure 5.3 and Figure 5.4. This growth comes from tangent hyperbolic characteristic of nullcline. This characteristic slows down the growth speed of state variable while approaching to the positive (or negative) saturation region of tangent hyperbolic. So this mechanism limits the growth speed as it will result to realistic spike timing by selecting appropriate parameters.

X_1, X_2, Y_1, Y_2, X_o, X_{sx} and X_{sy} are scaling parameters that helps to extend and offset the state variables. τ_x, τ_y and X_r are bifurcation parameters that brings qualitative changes to the state variables. Explanation of the model paramaters and variables are:

- ***x(t)*** **:** State variable that mimics the membrane potential.
- ***y(t)*** **:** State variable that mimics the recovery of membrane potential. It corresponds to activation of K^+ ionic currents in $I_{Na,p}+I_K$ model.
- $\boldsymbol{X_o}$**:** Offset value for membrane potential *x*. It corresponds to resting potential in $I_{Na,p}+I_K$ model.
- $\boldsymbol{X_{sx}}$**,** $\boldsymbol{X_{sy}}$**:** Scaling factors for *x* variable. Ratio of these parameters are crucial for proper operation and defines the shape of *x* nullcline. (X_{sx} /X_{sy}) is selected *10* in our application since it is adequate for obtaining the extensive firing patterns exhibited by real biological neurons.
- $\boldsymbol{X_1}$**,** $\boldsymbol{X_2}$**:** Shape factors for N-shaped *x* nullcline. These parameters correspond to effect of ohmic leak current, I_L plus instantenous $I_{Na,p}$ ionic currents in $I_{Na,p}+I_K$ model. These parameters is affected especially on period of spikes since they establish the curvature of N-Shaped nullcline.
- $\boldsymbol{\tau_x}$**:** Timescale for membrane potential *x*. Coarsely, It defines the upstroke speed of the spike. Upstroke time increases/decreases when this parameters decreases/increases.
- $\boldsymbol{\tau_y}$**:** Timescale for recovery current *y*. Coarsely, It defines the time between the consecutive spikes. Spiking period increases/decreases when this parameters decreases/increases.
- $\boldsymbol{I_{in}}$**:** Input current that mimics the sum of synaptic and injected currents.
- $\boldsymbol{Y_1}$**:** Coupling strenght between membrane potential *x* and recovery current *y*. It corresponds to the coefficient of K^+ steady-state activation function in $I_{Na,p}+I_K$ model.
- $\boldsymbol{Y_2}$**:** Offset value for recovery current *y*. This constant current holds the membrane voltage close to the spiking state. So input current I_{in} would be scaled as it will be in the range of real synaptic currents.

- ***X_r*:** After spike reset value. This parameter strongly defines the spiking behaviour of model.
- ***X_{max}*:** Maximum value for membrane potential *x*. After the spike reaches this value membrane voltage resets to X_r.

Even the new model seems to have ten different parameters, when we rescale it to obtain the minimum numbers of parameters as in (5.2), we see that it has only four independent parameters and an input current as in Izhikevich [6] and AdEx I&F [35] models. As we will see at oncoming sections, one can obtain nearly all of the major spiking templates of real biological neurons by only modifiying two of this parameters (i.e. p_3 and p_4) and input current I_{in}.

$$\tilde{t} = \frac{t}{\tau_x} X_2 X_{sx} \quad ; \quad \tilde{x}(\tilde{t}) := \left[(x(t) + X_o) X_{sx} \right] \quad ; \quad \tilde{y}(\tilde{t}) := \frac{y(t) - Y_2}{Y_1}$$

$$X_{sy} = \frac{X_{sx}}{10} \quad ; \quad p_1 = \frac{X_1}{X_2} \quad ; \quad p_2 = \frac{Y_1}{X_2}$$

$$p_3 = \frac{\tau_y}{\tau_x} X_2 X_{sx} \quad ; \quad p_4 = \left[(X_r + X_o) X_{sx} \right]$$

$$\tilde{Y}_{in} = \frac{Y_{in} - Y_2}{X_2} \quad ; \quad \tilde{X}_{\max} = \left[(X_{\max} + X_o) X_{sx} \right] \tag{5.2}$$

$$\frac{d\tilde{x}(\tilde{t})}{d\tilde{t}} = p_1 \tanh\left[\frac{\tilde{x}(\tilde{t})}{10} \right] - \tanh\left[\tilde{x}(\tilde{t}) \right] - p_2 \tilde{y}(\tilde{t}) + \tilde{Y}_{in}$$

$$p_3 \frac{d\tilde{y}(\tilde{t})}{d\tilde{t}} = \tanh\left[\frac{\tilde{x}(\tilde{t})}{10} \right] - \tilde{y}(\tilde{t})$$

$$\tilde{x}(\tilde{t}) > \tilde{X}_{\max} \Rightarrow \tilde{x}(\tilde{t}) \leftarrow p_4$$

By using local linear analysis method we can determine the bifurcation and stability regions of new neuron model. This method informs us about the behaviour of the neuron for different parameter sets. It is based on obtaining the eigen values of Jacobian Matrix of model at the specific equilibrium point as can be seen from equation (5.3), (5.4) and (5.5). Since the model may have many equilibrium points X_e and Y_e are vectors in equation (5.3).

$$\frac{dx(t)}{dt} = f(x,y) \;;\; \frac{dy(t)}{dt} = g(x,y) \;\Rightarrow\; f(\vec{X}_e,\vec{Y}_e) = g(\vec{X}_e,\vec{Y}_e)$$

$$\Rightarrow J = \begin{bmatrix} \dfrac{\partial f(x,y)}{\partial x} & \dfrac{\partial f(x,y)}{\partial y} \\ \dfrac{\partial g(x,y)}{\partial x} & \dfrac{\partial g(x,y)}{\partial y} \end{bmatrix}_{x=\vec{X}_e \;,\; y=\vec{Y}_e} \tag{5.3}$$

$$\det(J-\lambda I) = 0 \;\Rightarrow\; \lambda^2 - \tau\lambda + \Delta = 0 \;\Rightarrow\; \lambda_{1,2} = \frac{\tau \pm \sqrt{\tau^2 - 4\Delta}}{2}$$

$$\tau = \left.\frac{\partial f}{\partial x}\right|_{x=X_e \;,\; y=Y_e} + \left.\frac{\partial g}{\partial y}\right|_{x=X_e \;,\; y=Y_e}$$

$$\Rightarrow \tau = \frac{X_1 X_{sy}}{\tau_x}\sec h^2\left[(X_e + X_o)X_{sy}\right] - \frac{X_2 X_{sx}}{\tau_x}\sec h^2\left[(X_e + X_o)X_{sx}\right] - \frac{1}{\tau_y} \tag{5.4}$$

$$\Delta = \left.\frac{\partial f}{\partial x}\frac{\partial g}{\partial y}\right|_{x=X_e \;,\; y=Y_e} - \left.\frac{\partial f}{\partial y}\frac{\partial g}{\partial x}\right|_{x=X_e \;,\; y=Y_e}$$

$$\Rightarrow \Delta = -\frac{X_1 X_{sy}}{\tau_y \tau_x}\sec h^2\left[(X_e + X_o)X_{sy}\right] + \frac{X_2 X_{sx}}{\tau_y \tau_x}\sec h^2\left[(X_e + X_o)X_{sx}\right] \tag{5.5}$$

$$+ \frac{Y_1 X_{sy}}{\tau_y \tau_x}\sec h^2\left[(X_e + X_o)X_{sy}\right]$$

The eigenvalues found in equation (5.3), (5.4) and (5.5) shows stability of an equilibrium and also define geometry of the vector field near the equilibrium as can be seen from Figure 5.2. From equations (5.4) and (5.5) it can be deduced that by changing only X_1 (or X_2) and τ_x (or τ_y) one can cover all the bifurcation regions in Figure 5.2 which means all the possible spiking behaviours are also been obtained.

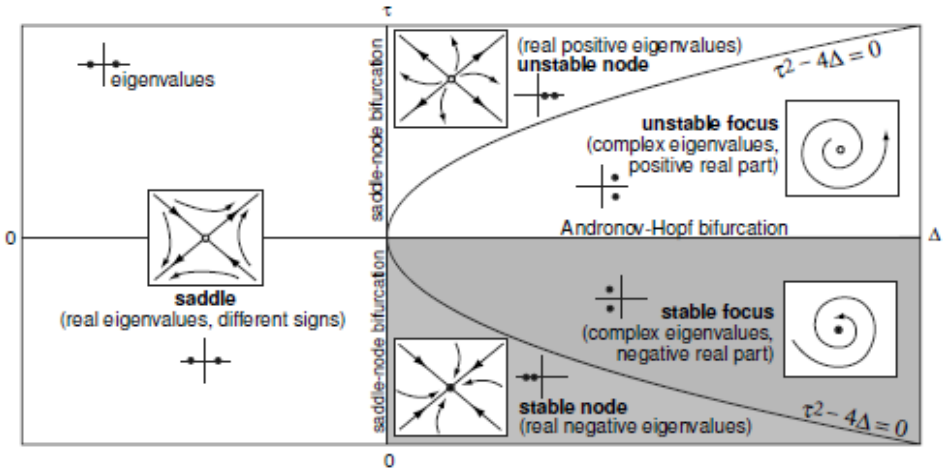


Figure 5.2 : Equilibrium points and Bifurcation regions of model [19].

5.1 Neuro Computational Features

We designed a software application in MATLAB to examine the neuro computational features of new neuron model. This application has a Graphical User Interface (GUI) , shown in Figure 5.3, for accepting the inputs from user and displaying the calculated outputs. By using this GUI one can enter the neuron parameter values, simulation time parameters and stimulation current parameters and run the numerical simulations. Heun's method (also called Improved Euler method) is used to solve the differential equations of new neuron model. The Heun's procedure for calculating the numerical solution for $y'(t) = f(t, y(t))$; $y(t_0) = y_0$ kind of initial value problem is to find the intermediate value $\tilde{y}_{i+1}$ at the first step and then to obtain the final approximation y_{i+1} at the next integration step as can be given by:

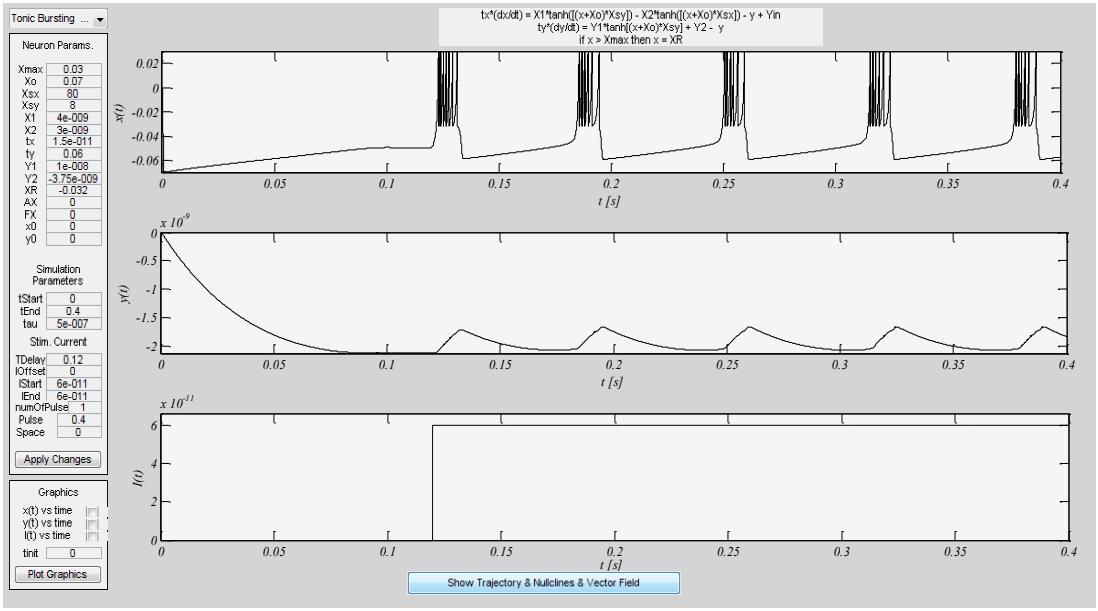
$$\begin{aligned} \tilde{y}_{i+1} &= y_i + hf(t_i, y_i) \\ y_{i+1} &= y_i + \frac{h}{2}\left[f(t_i, y_i) + f(t_{i+1}, \tilde{y}_{i+1})\right] \end{aligned} \tag{5.6}$$

where h is the integration step size (i.e. $h = t_{i+1} - t_i$).

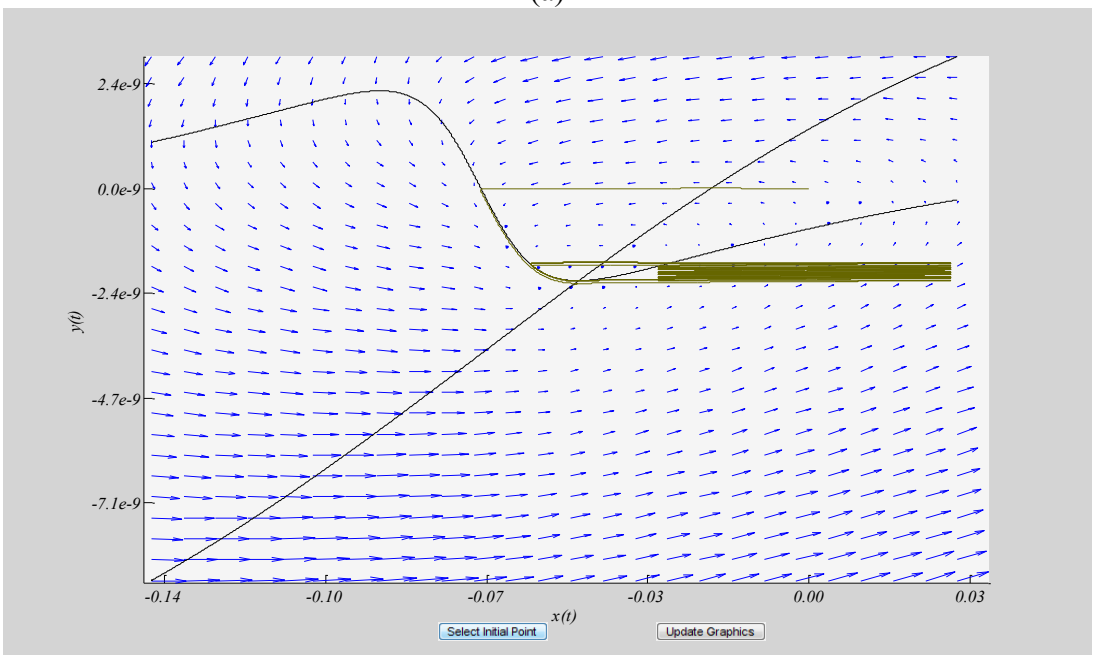
In designed GUI, simulation duration and simulation time step can be determined by user. x, y and I_{in} vs. time graphics are displayed on main window or can be displayed on seperate window for detailed analysis. For phase plane analysis user can display the vector field, trajectory of system and nullclines on the same window as can be seen from Figure 5.3(b). From this window user can also select an initial point for state variables by clicking the desired point on graphic plane and can update the output of the system (i.e. x, y and I_{in} vs. time) initialized with selected initial values. Some pre-defined spiking patterns with the parameters given in Table 5.1 is implemented in a combo box on main window. So the users can use those patterns as starting point for their analysis.

Table 5.1 : Parameter values of various spiking behaivours obtained with offered neuron model. X_2=3e-9, X_{sx}=80, X_{sy}=8, X_o=0.07, Y_1=1e-8, Y_2=-3,75e-9 and X_{max}=0.03(Not applicable for Limit Cycle Oscillation) same for all behaviours.

	Figure No	τ_x	X_1	τ_y	X_r	I_{in}
Limit Cycle Osc.	Figure 5.4	1.5e-11	3.5e-9	0.025	-	3e-10
Tonic Spiking	Figure 5.5	1.5e-11	4e-9	0.060	-0.045	6e-11
Tonic Bursting	Figure 5.6	1.5e-11	4e-9	0.060	-0.032	6e-11
Class I Excitability	Figure 5.8(a)	1.5e-11	4e-9	10.00	-0.050	Figure 5.8(a)
Class II Excitability	Figure 5.8(b)	1.5e-11	4e-9	0.040	-0.046	Figure 5.8(b)
Integrator	Figure 5.9(a)	1.5e-11	4e-9	0.035	-0.050	Figure 5.9(a)
Resonator	Figure 5.9(b)	1.5e-11	5e-9	0.003	-0.050	Figure 5.9(b)
Phasic Spiking	Figure 5.7(a)	1.5e-11	4e-9	0.020	-0.050	4e-11
Phasic Bursting	Figure 5.7(b)	1.5e-11	4e-9	0.050	-0.032	4e-11
Rebound Spike	Figure 5.10(a)	1.5e-11	4e-9	0.060	-0.045	Figure
Rebound Burst	Figure 5.10(b)	1.5e-11	4e-9	0.060	-0.032	Figure
Spike Latency	Figure 5.11	3.0e-11	4e-9	0.055	-0.045	Figure 5.11
Spike Frequency Adaptation	Figure 5.12	2.0e-11	4e-9	3.00	-0.050	10e-11
Suspensions	Figure 5.13	1.5e-11	4e-9	0.060	-0.048	5.4e-11



(a)



(b)

Figure 5.3 : GUI of Software application designed in MATLAB to examine the neuro computational features of new neuron model (a) main output window (b) phase plane analysis window.

5.1.1 Limit cycle oscillations

We determined the value of scaling parameters by taking into consideration that these functions represent the ionic currents through the cell membrane. The value of this current changes from a few hundred pico to nano amperes [7, 9, 19, 36]. Bifurcation parameters are determined by considering that they (i.e. τ_x , τ_y) represents the scaled membrane capacitance and time constant of recovery current [36] respectively. Reset parameters (e.i. X_{max}, X_r) are determined by accounting that they

corresponds to maximum membrane potential (~*30 mV* for real neurons) and a reset value less than maximum but greater than minimum membrane potential (~ *-60 mV* for real neurons). Reset parameter X_r is also a bifurcation parameter since its value defines the spiking behaviour.

By considering above facts our initial goal was to find a limit cycle attractor since it causes to spike like oscillations even without reset mechanism as shown in Figure 5.4. The parameters found at this step is taken as a starting point for obtaining the various real time spiking patterns. Most of the spiking patterns exhibited by the known types of neocortical and thalamic neurons given in [6] and [4] can be obtained by selecting the proper parameters. Parameter set for the most important of them are given in Table 5.1. For these parameters resting potential of neurons is about *-50 mV* and well matched with real biological neuron values.

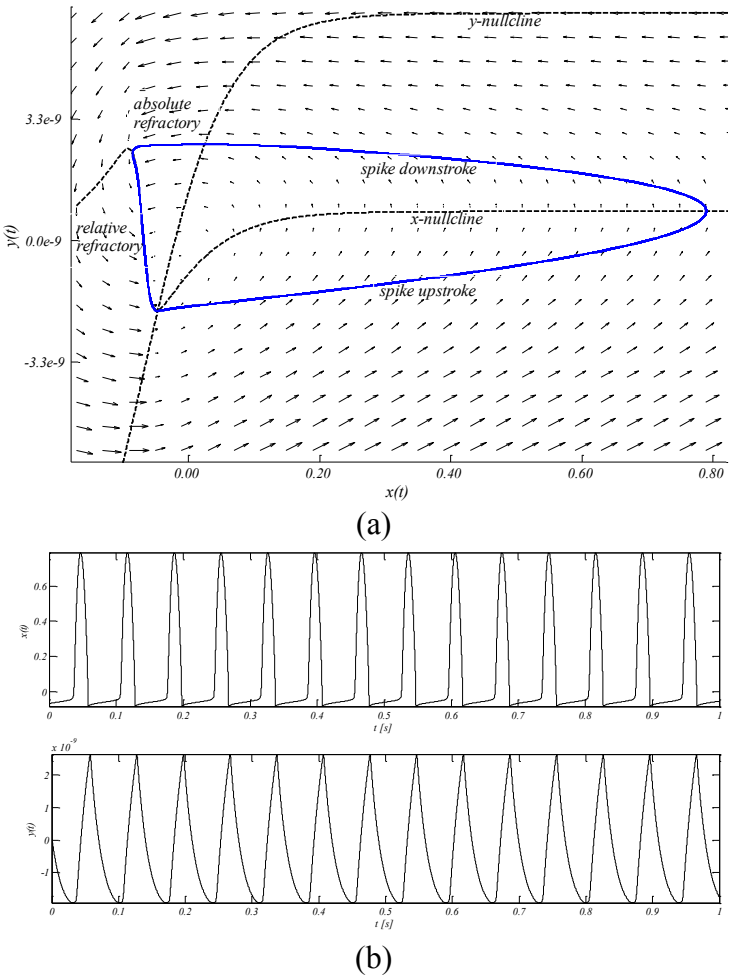
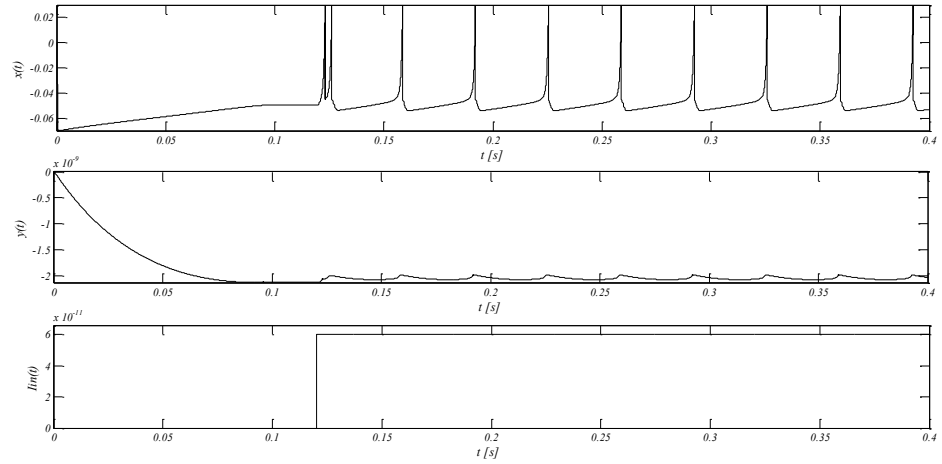


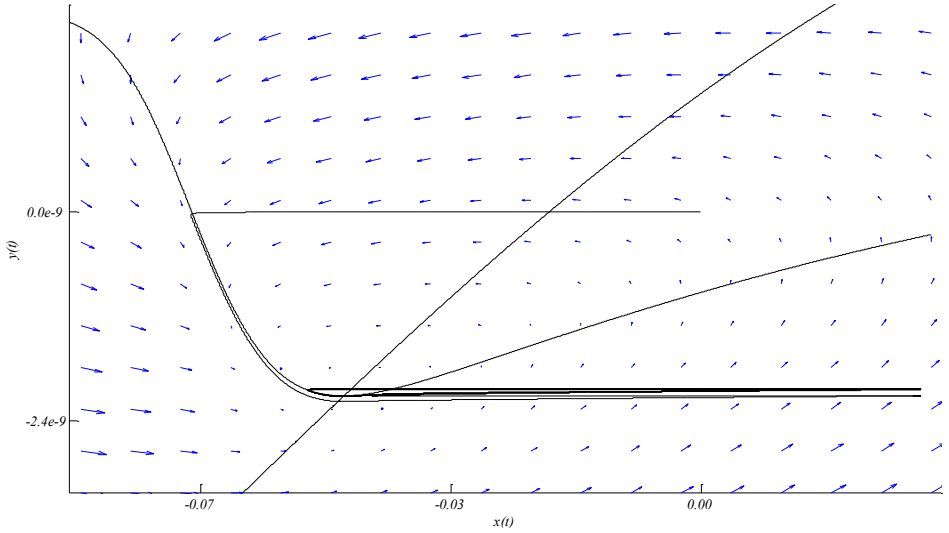
Figure 5.4 : Spike like oscilations for obtaining the starting point parameters in new neuron model (a) phase plane and vector field for limit cycle attractor (b) evolution of state variables in time.

5.1.2 Tonic spiking

When the neurons stimulated with a proper current they fire spikes. Neurophysiologists inject this current into the neuron and records its membrane potential. Some types of cortical neurons like low threshold spiking (LTS) or fast spiking (FS) inhibitory neurons and regular spiking (RS) excitatory neurons generates continuous train of spikes as long as the input current exist. Continous firing indicate that there is a persistent input [4]. This kind of spiking is called tonic spiking. It has been thought that this firing type is seen awake, alert animal. Thalamic relay cells are good example to this kind of neurons [48]. By choosing proper parameters as seen in Table 5.1 our model can easily imitate the tonic spiking behaviour of real neurons as shown in Figure 5.5.



(a)

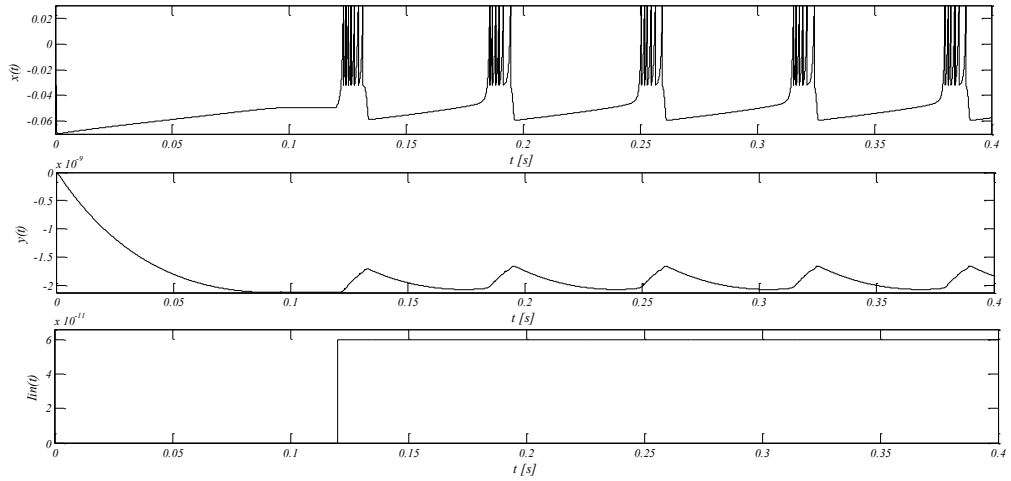


(b)

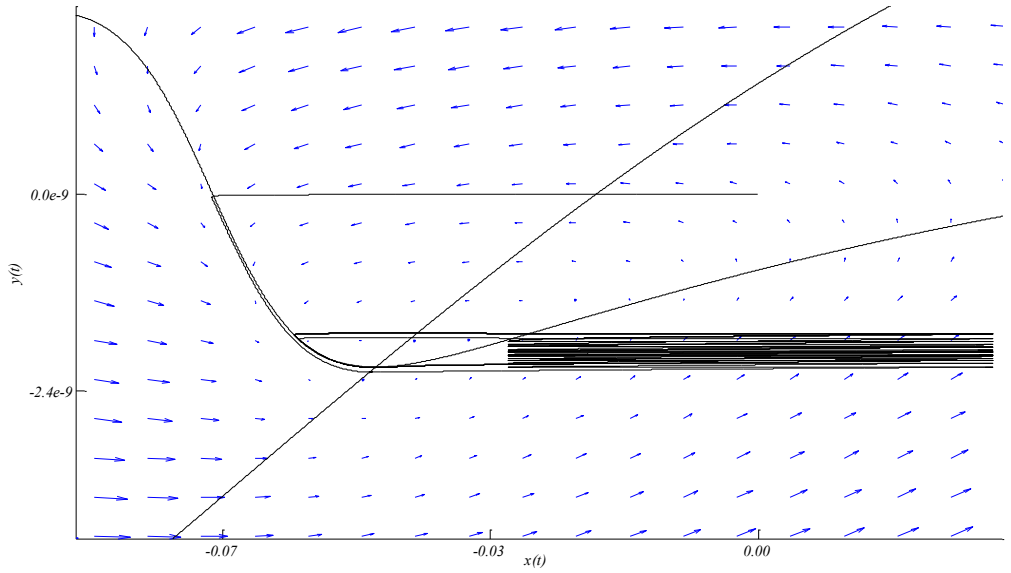
Figure 5.5 : Tonic spiking behaviour of novel neuron model (a) Time evolution of state variables and injected current (b) Phase plane demonstration of vector field, trajectory and nullclines.

5.1.3 Tonic bursting

Some neurons generate periods of rapid spikes that are followed by a quiescent period before the next period. So neuron fires discrete group of spikes as long as the input exist. This kind of behaviour is called tonic bursting and is thought to be important in the operation of CPGs [49], gamma-frequency oscillations in the brain and reduction of neuronal noise and synaptic transmission failures. Tonic spiking and bursting are primary behaviours of many neuron types. By choosing proper parameters as seen in Table 5.1 our model can easily imitate the tonic bursting behaviour of real neurons as shown in Figure 5.6.



(a)

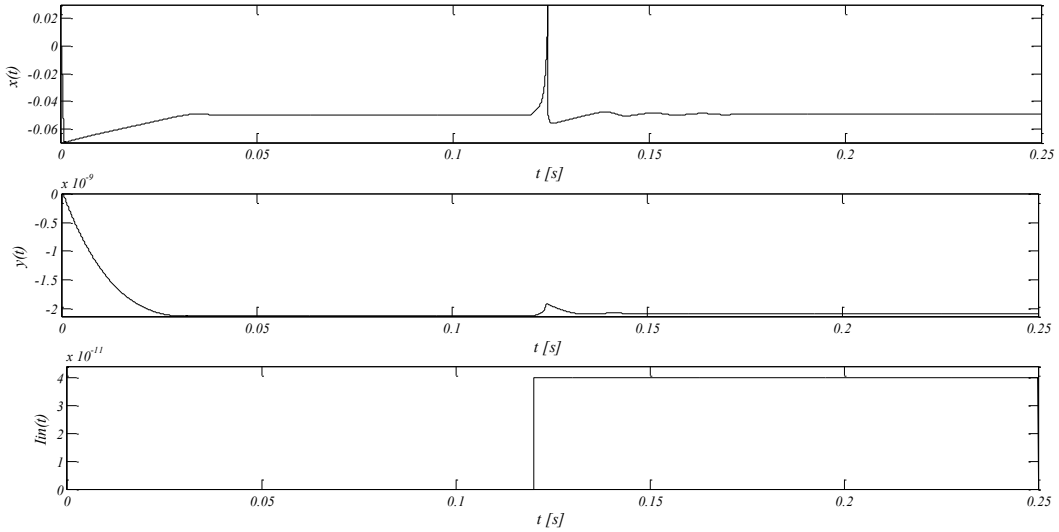


(b)

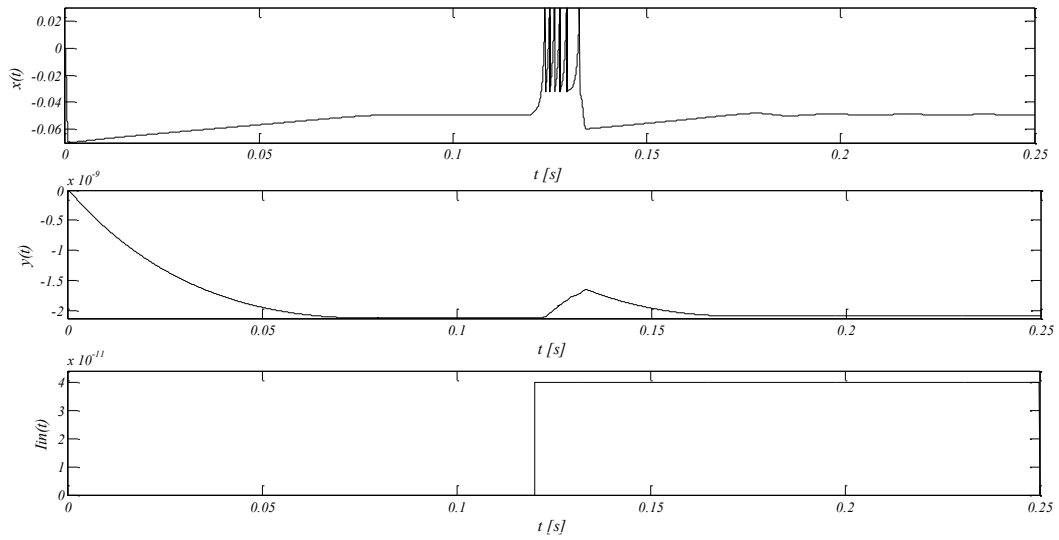
Figure 5.6 : Tonic bursting behaviour of novel neuron model (a) Time evolution of state variables and injected current (b) Phase plane demonstration of vector field, trajectory and nullclines.

5.1.4 Phasic spiking and phasic bursting

Some neurons emit one shot spike or burst at the onset of the input current. Such patterns are called phasic spiking and bursting. This behaviour is indicator for the beginning of the stimuli. By choosing proper parameters as seen in Table 5.1 our model can easily imitate this behaviour of real neurons as shown in Figure 5.7.



(a)



(b)

Figure 5.7 : Time evolution of state variables and injected current for (a) Phasic spiking (b) Phasic bursting.

5.1.5 Excitability types

Works of Hodgkin on squid axons about the bifurcation in neural dynamics showed that neurons can be classified into two main groups with regard to the response to

various amplitudes of input stimulu. If spikes can be generated with low frequency and firing rate can be increased sharply depending on the strength of the applied current this neuron is called Class I excitable. Class I excitable neurons have continuous current-frequency curve as can be seen in Figure 5.8(a). If spikes can be generated above a certain frequency this neuron is called Class II excitable. Class II excitable neurons have discontinuous current-frequency curve as can be seen in Figure 5.8(b). Used neuron parameters for obtaining the graphics in Figure 5.8 is given in Table 5.1.

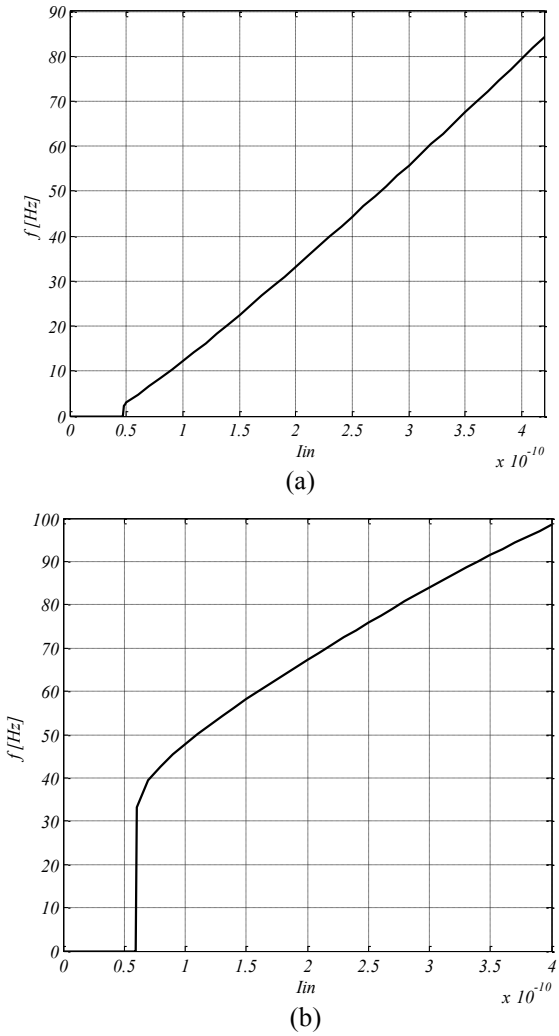
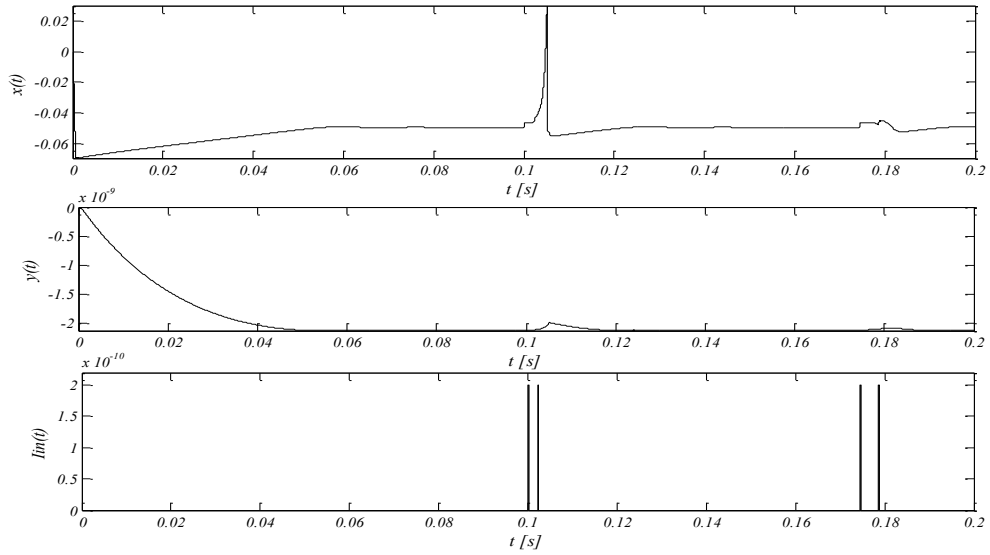


Figure 5.8 : Representation of excitability types of new neuron model (a) Class I (b) Class II.

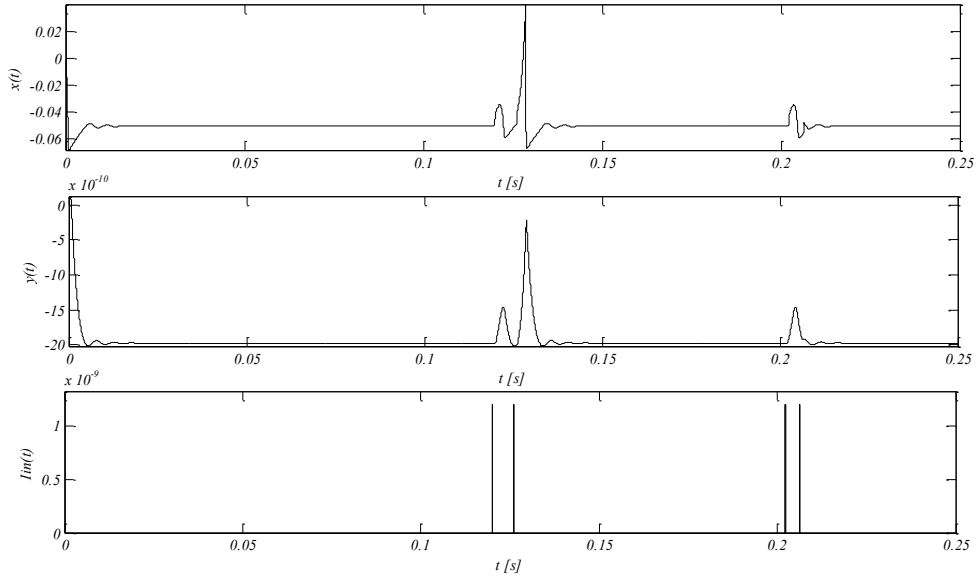
5.1.6 Resonator and integrator behaviour

Neurons with damped subthreshold ($x < X_{max}$) oscillations referred as resonator. Those neurons responds only to the inputs whose frequency matches with the frequency of subthreshold oscillations. As it can be seen in Figure 5.9(b), even the

second pair of spikes are more close to each other they do not cause to neuron to fire since their timing do not match the frequency of subthreshold oscillations of resonator neuron. Neurons that do not have oscillatory potentials referred as integrators. They integrates their input so the higher the input frequency the more likely they fire as in Figure 5.9(a).



(a)



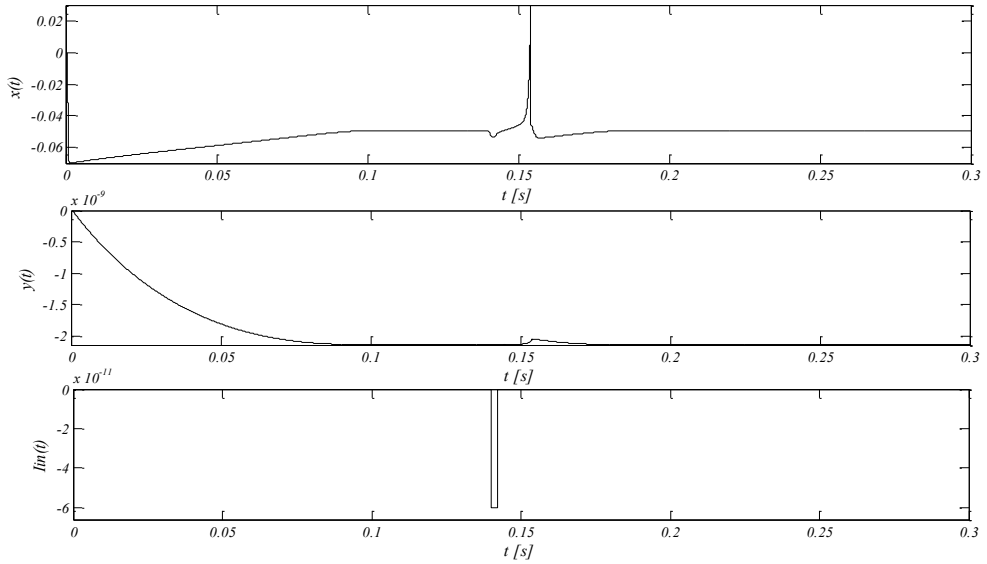
(b)

Figure 5.9 : Demonstration of (a) Integrator (b) Resonator behaviour of novel neuron model.

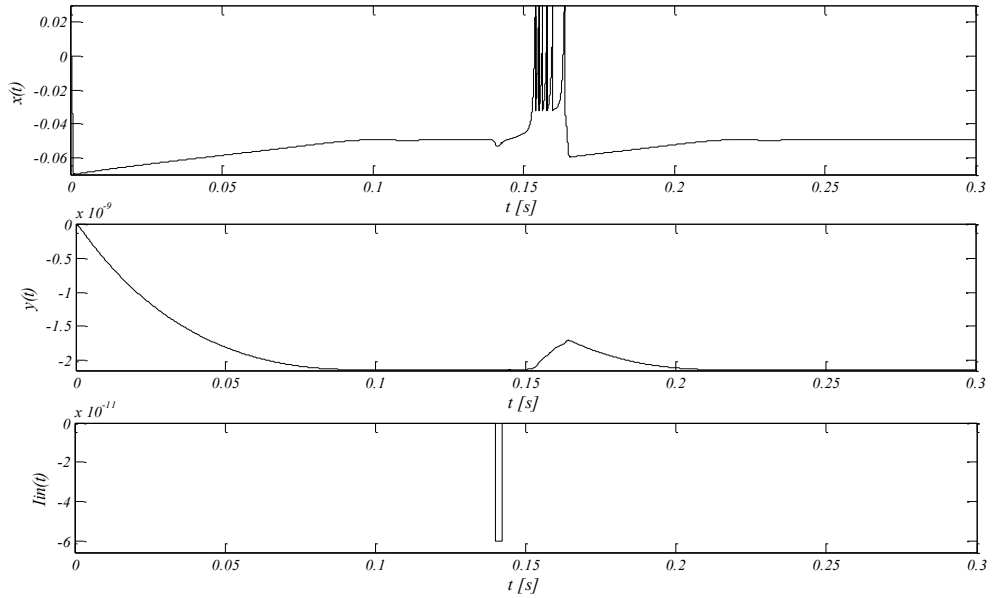
5.1.7 Rebound bursting and rebound spiking

When we apply an inhibitory input to a neuron, it may elicits a spike or burst of spikes quick after the inhibitory input is released. This kind of post-inhibitory

response is called rebound spike/burst. Rebound spikes are charecteristics of some neuron types and brain regions including cerebellar Purkinje cells, thalamic relay cells, olfactory mitral cells etc. [50]. Rebound spikes is believed to serve to the oscillatory dynamics like central pattern generation in a neuronal network. Rebound spikes are believed to be the main contributer of the sleep oscillations. So a good neuron model should mimic those behaivours successfuly as our model do as can be seen from the Figure 5.10. Used neuron parameters for obtaining the graphics in figure is given in Table 5.1.



(a)



(b)

Figure 5.10 : Demonstration of rebound (a) spike (b) burst behaviour of novel neuron model.

5.1.8 Spike latency behaviour

In some type of neurons like the RS cells in mammalian cortex there is a time delay between the input stimuli and response of neuron to this input. This behaviour is called spike latency. Decreasing the input current causes increasing of the delay. This delay can be quite large as tens of milliseconds. This mechanism is believed to have a role in propagation/transmission of information in several sensory systems like auditory and visual systems. By using the parameters given in Table 5.1 we obtained the spike latency property as shown in Figure 5.11.

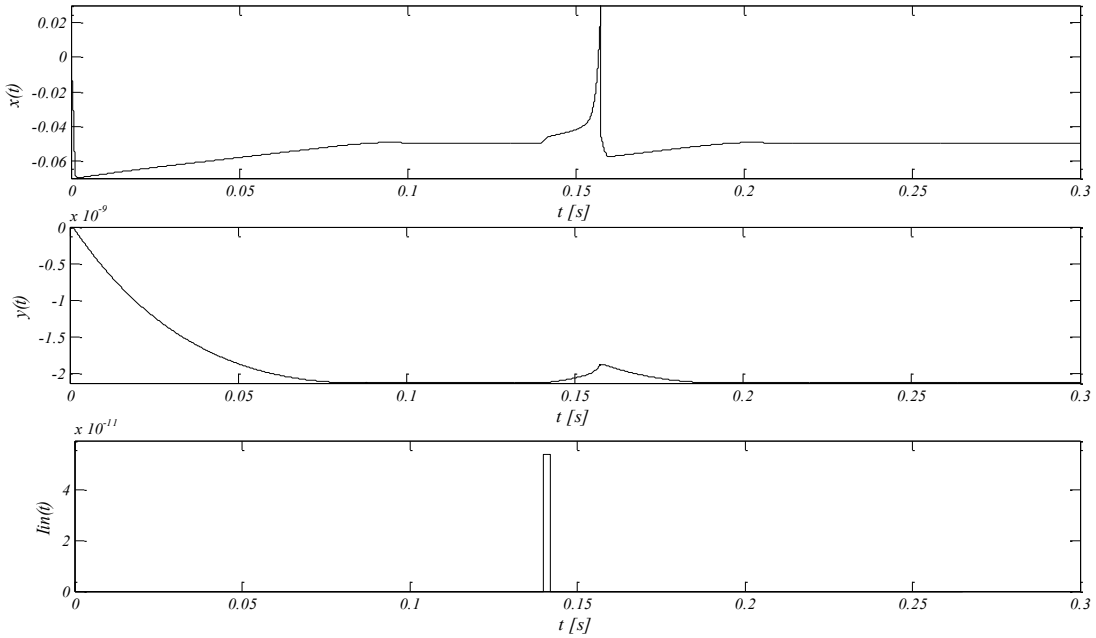


Figure 5.11 : Demonstration of Spike Latency behaviour of new model.

5.1.9 Spike frequency adaptation

Many neurons responds the constant input current with high spike frequency at the onset of stimuli then the frequency decays down to a lower steady-state value in time. This phenomenon is called spike-frequency adaptation. Process of this phenomenon is slower than the dynamics of spike generation. Excitatory neurons in mammalian neocortex, namely the regular spiking (RS) cell, and Low-threshold spiking (LTS) inhibitory neurons have this property [4]. Spike-frequency adaptation behaviour is obtained for offered model with the parameters given in Table 5.1 and pattern shown in Figure 5.12.

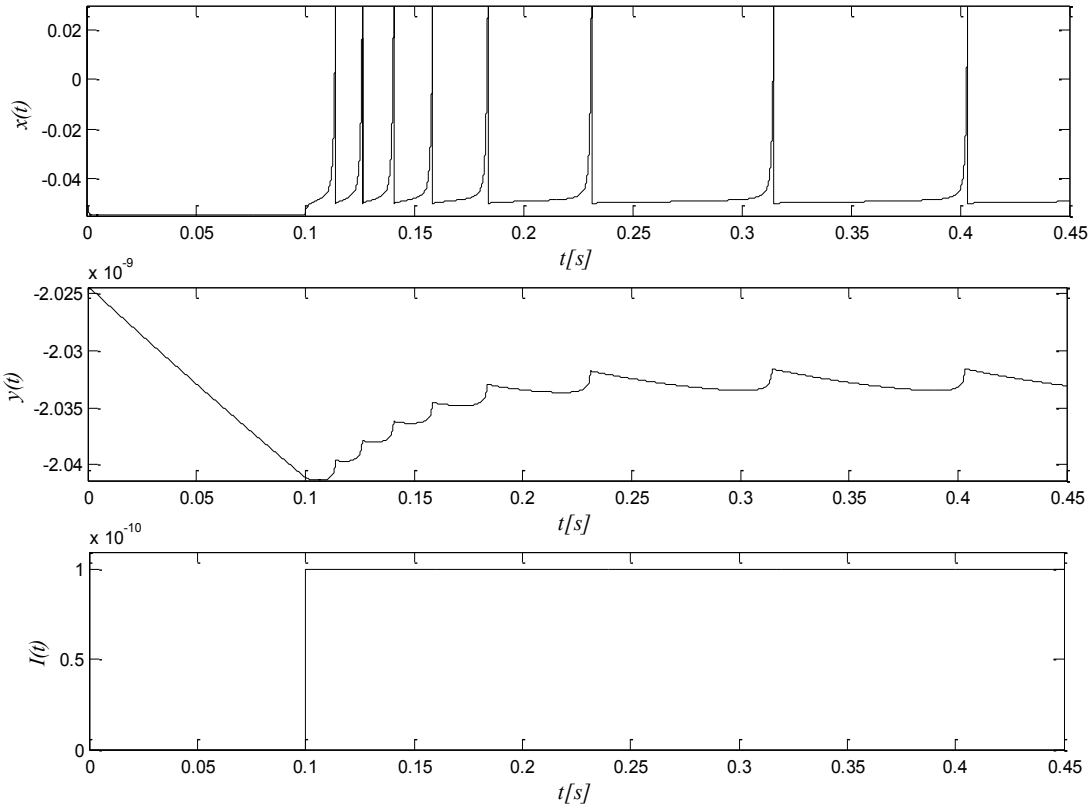


Figure 5.12 : Demonstration of Spike Frequency Adaptation behaviour.

5.1.10 Suspensions

Some type of neurons in mammalian cortex, a sharp spike is followed by small amplitude limit cycle oscillations as a response to a input stimuli. The pattern that represents this behaviour is called suspensions. By using the parameters in Table 5.1 we can obtain this pattern for offered neuron model as shown in Figure 5.13.

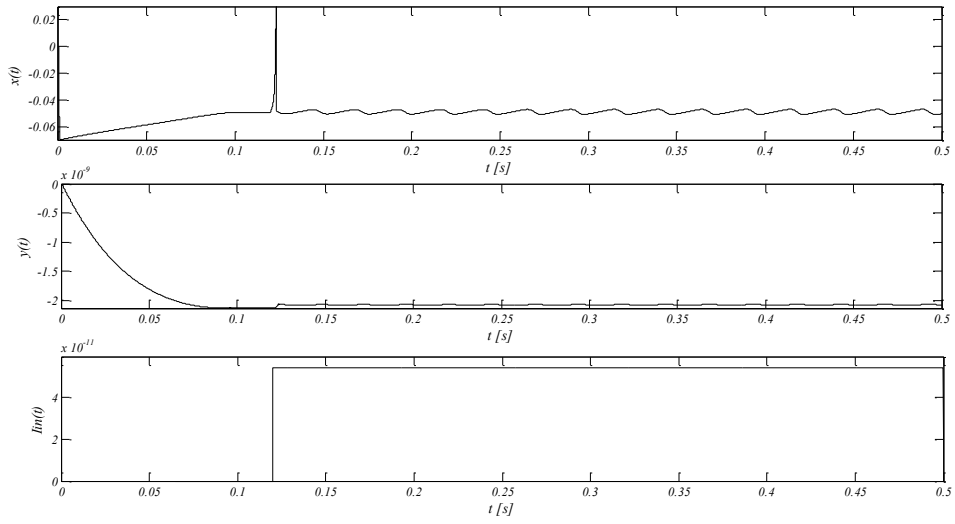


Figure 5.13 : Demonstration of Suspension behaviour of neuron model.

6. NEURON CIRCUIT DESIGN

Digital circuits dominate today's integrated circuit technology, which employ MOSFETs as switching elements. Analog circuits comprise a small part of those designs and even a smaller part of those designs employs MOSFETs in subthreshold domain where neuromorphic circuits are among these examples. It is very difficult to process large amounts of data with digital circuits. Thus, analog VLSI circuits has become more attractive than digital circuits since the demand for real time processing has become crucial for huge neuromorphic systems. Designers had great progress in implementing VLSI neurons that mimic the behavior of real biological neurons using analog circuits from the beginning of neuromorphic engineering starting with the pioneering work of Mead [51]. Those systems include thousands of coupled neurons on a single silicon chip [52, 55]. Such systems are used for investigating the neurocomputational features of real biological neural systems and may be useful for understanding and mimicing the working mechanism of human brain. Thousands of neurons and coupling circuits means huge silicon area and high power consumption that cause to adversity in designing those kind of systems. Another difficulty comes from the low amplitude and low frequency range (i.e. 2 Hz-120 Hz) property of real spikes. Low frequency means large time constants, so circuits operating at this range should employ large value capacitors which results in larger silicon area. If we decrease the capacitor value, spiking frequency increases and goes out of biological timescale and this kind of design may only be used for simulation purposes not for creating a real neuromorphic systems like Man Machine Interfaces (MMI). The only way to use small value capacitors is to work with small currents. This makes the small currents key factor for low power and compact design.

VLSI implementations of biological neurons varies in complexity and accuracy. There is a trade of between the accuracy and complexity. Many low power and compact designs have been proposed recently [34, 37, 38, 56]. However, in [56] and [37] the spike shapes are not compatible with real neuron's spike shape which results

in restricted dynamical behaviour. Circuits in [13, 34, 38] consumes much power and large chip area as they will not be suitable for a large neuromorphic network design.

Restrictions mentioned above should be kept in mind when designing the low power and compact neuron circuits for massively large networks. By considering above facts we designed a low power VLSI neuron relying on our new model by using subthreshold CMOS design technique as explained at following sections. Subthreshold design allows to work with the very small currents at level of pico amperes.

6.1 Design Parameters and Blocks

As we explained in previous sections the main advantage of our neuron model is suitability for low power and compact electronic implementation. In our VLSI design of new neuron model $x(t)$ variable is represented with voltage and $y(t)$ variable is represented with current. All the transistors except that a few transistors in current reference circuit operates in subthreshold region to satisfy the low power condition. Linear Technology's LTSpice is used in circuit simulations. For obtaining the accurate results we set the SPICE option G_{min} to 10^{-16} since the circuit operates at low currents.

We designed the circuit by using TSMC $0.18\mu m$ technology. Base terminal of all NMOS transistors are tied to lowest potential (GND) and base terminal of all PMOS transistors are tied to highest potential (VDD) since the used process technology is n-well. Because the circuit operates at picoamperes range we selected the minimum channel width to length ratio (i.e. W/L) as $2\mu m/2\mu m$ for minimizing the effect of the absolute parameter deviation in sizing caused by the VLSI manufacturing process. So all the transistors in circuit is thought to be sized as $2\mu m/2\mu m$ unless otherwise specified. We selected supply voltage V_{DD} as $1.5V$ for being compatible with the equipments work with battery.

When the gate-source voltage of a MOS transistor is below the threshold voltage, it is said to operate in subthreshold region or in weak inversion. In this region, the relationship between drain current and gate voltage has an exponential form since the diffusion mechanism dominant for current calculation. Additionally, the current flowing through the MOS transistor varies from picoamperes to a few nanoamperes.

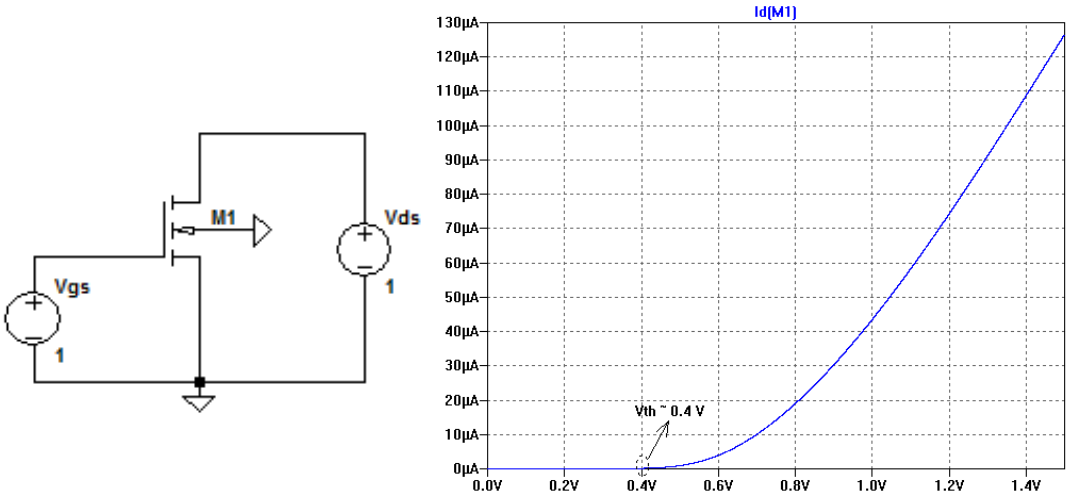
Reverse diode leakage current is the bottom limit of this current. Typical values are on the order of *0.1 fA~0.5 fA*. However, ion implantation applied for lowering the threshold value increases the leakage current seriously, up to a few pA for the worst case. The relationship between the subthreshold current and terminal voltages for a NMOS transistor is given by equation (6.1)[57].

$$I_{ds} = \mu_n C_{ox}(1-n)V_{TH}^2\left(\frac{W}{L}\right)e^{\left[\frac{(1-n)V_{bs}}{nU_T}\right]}e^{\left[\frac{V_{gs}}{nU_T}\right]}\left(1-e^{-\left[\frac{V_{ds}}{U_T}\right]}+\frac{V_{ds}}{V_o}\right) \tag{6.1}$$

where μ is the carrier mobility, C_{ox} is the gate-oxide capacitance, n is the subthreshold slope factor, V_{TH} is the threshold voltage, (W/L) is the aspect ratio of transistor, $U_T=(kT/q)$ is the thermal voltage (26 mV for room temperature), V_o is Early voltage. For $V_{ds} > 4U_T=0.1V$ transistor is said to operate in saturation. By ignoring body effect, Early Effect and assuming transistor operates in saturation we can simplfy the equation in form that enables hand analysis. This simple equation is given by:

$$I_{ds} = I_S\left(\frac{W}{L}\right)e^{\left[\frac{V_{gs}}{nU_T}\right]} \tag{6.2}$$

Simulation results of input-output characteristics of NMOS transistor for model parameter extraction is given at Figure 6.1 to Figure 6.3. Figure 6.1(a) shows the configuration used in simulations for parameter extraction. Dimension of this transistor is selected *1μm/1μm*. Figure 6.1(b) shows the gate source voltage to drain current relation for all operation regions including subthreshold, moderate and strong inversion. In this simulation drain source voltage is held constant at *1 V*. We found threshold voltage of transistor *~0.4V* which means below this value NMOS is operating in subthreshold.

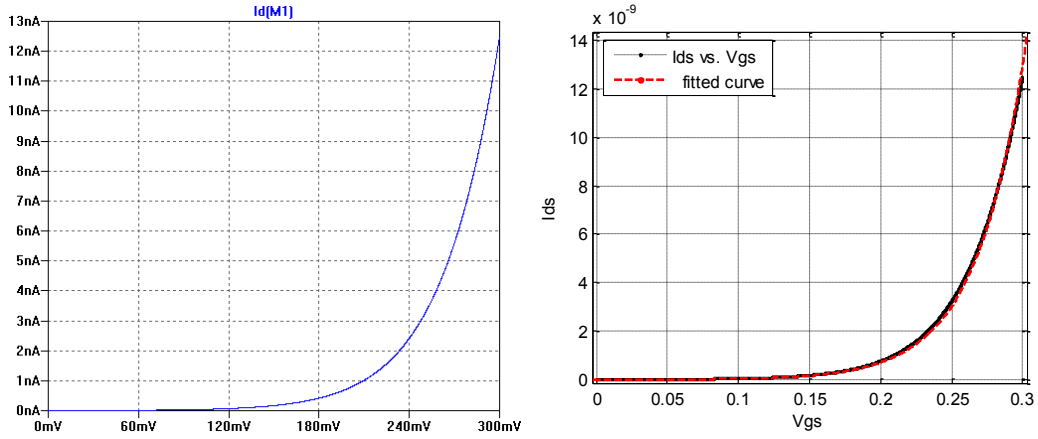


(a) (b)

Figure 6.1 : Extraction of model parameters (a) Configuration used for NMOS parameters extraction (b) I_{ds} vs. V_{gs} (V_{ds}=*1 V*).

Figure 6.2(a) shows the gate-source voltage to drain current relation at subthreshold region for *1V* constant drain to source voltage. The curve obtained in this step is used for determining the α and I_s parameters by using curve fitting method. Fitted curve is shown in Figure 6.2(b). Simulation result is fitted the simple expression given in equation (6.2) as described below:

$$I_{ds} = \left(\frac{1}{1}\right) 2.021 * 10^{-12} e^{(29.24 * V_{gs})} \rightarrow I_s = 2.021\ pA \text{ then } \alpha = \left(\frac{1}{nU_T}\right) = 29.24$$



(a) (b)

Figure 6.2 : (a) I_{ds} vs. V_{gs} *(V_{ds}=1 V)* of NMOS in subthreshold (b) fitted curve.

Figure 6.3 shows the drain-source voltage to drain current relation at subthreshold region for *0.25V* constant gate to source voltage. The curve obtained in this step is used for determining the Early Voltage V_o given in equation (6.1). Early Voltage represents the effect of Channel Length Modulation (CLM) at saturation. This

parameter is also obtained by curve fitting of simulation data. Consequently V_o is found *17V*.

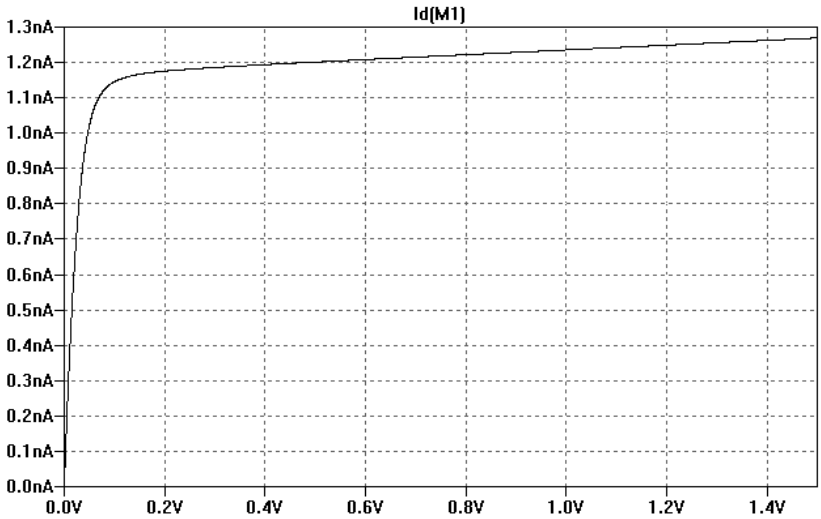


Figure 6.3 : I_{ds} vs. V_{ds} $(V_{gs}=250\ mV)$ of NMOS in subthreshold region.

Parameter values of implemented neuron are given at Table 6.1. As it can be seen from the values in this table, spiking to bursting behaviour transition is made by changing only reset voltage (i.e. X_R) parameter.

Table 6.1 : Parameter values of VLSI implemented neuron with TSMC $0.18\mu m$ technology ($X_{max} = 1.1\ V$).

	Fig. No	τ_x	X_1	X_2	X_{sx}	X_{sy}	X_o	τ_y	Y_1	Y_2	X_r	I_{in}
Tonic Spiking	Fig 2.4a	3e-12	4e-9	3e-9	16.5	1.5	-0.6	0.023	1e-8	-3.75e-9	0.70	22e-12
Tonic Bursting	Fig 2.4b	3e-12	4e-9	3e-9	16.5	1.5	-0.6	0.023	1e-8	-3.75e-9	0.82	12e-11

We analysed the neuron model numericaly by using the values given in Table 6.1. Numerical simulation results are given in Figure 6.4. We are expecting to obtain the similar results from circuit simulations carried out in section 6.6.

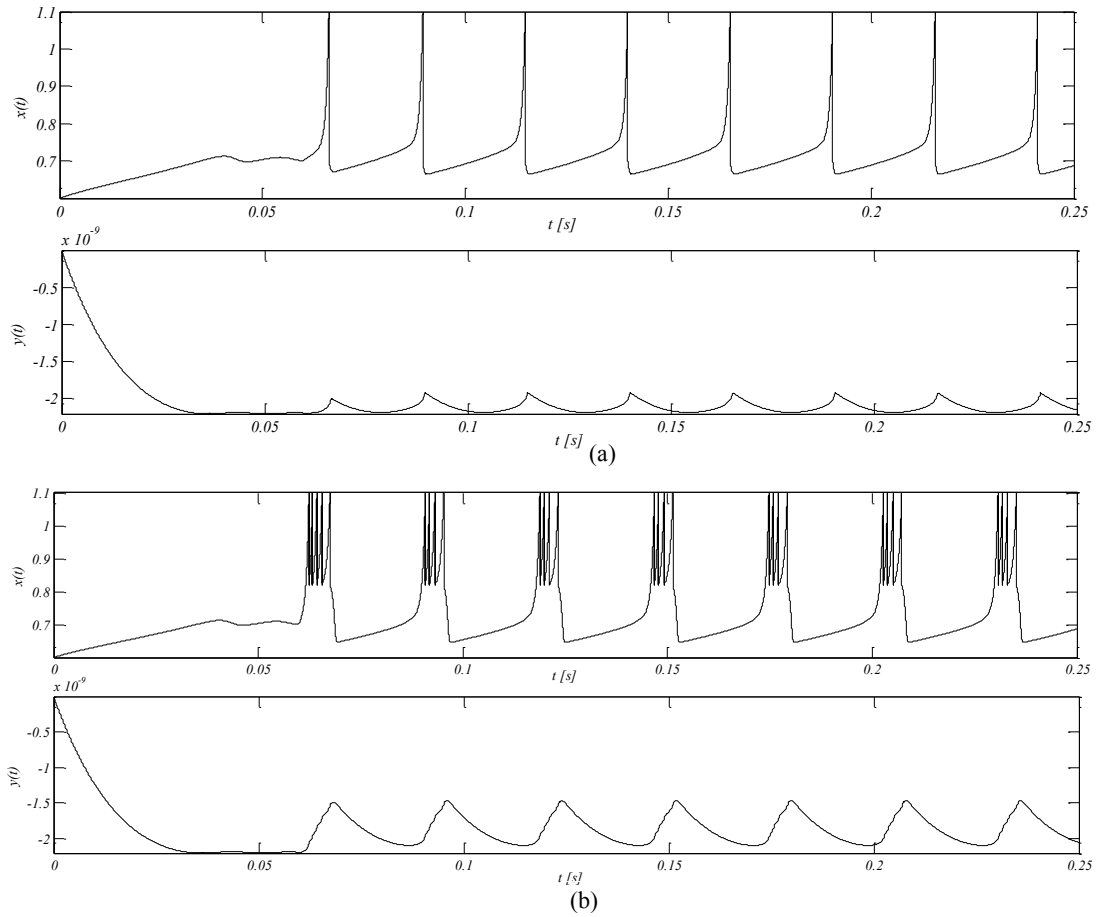


Figure 6.4 : Numerical Analysis result of new neuron model with the VLSI implementation values given in Table 6.1 for (a) tonic spiking (b) tonic bursting.

For making the model suitable for circuit implemantation firstly we wrote down the model equations by using given values in Table 6.1 and subtract $8.75*10^{-9}$ value from $y(t)$ then multiplied first state equation by 10^{-1} and second one by $(\alpha*10^{-12})$. After subtractions and multiplications, we made $x(t) \rightarrow v(t)$ and $y(t) \rightarrow [10*i(t)]$ transformation and broke the final expressions into the corresponding subthreshold CMOS blocks and elements as can be seen from equation (6.3). In this equation THB is an abbreviation for Tangent Hyperbolic Block (THB) explained at next section.

$$
\begin{aligned}
\underbrace{300*10^{-15}}_{C=300fF}\frac{dv(t)}{dt} &= \Bigg\{ \underbrace{4*100*10^{-12}*\tanh\left[\left(\underbrace{\frac{v(t)}{8.8}}_{\substack{voltage\\ divider}}-\underbrace{\frac{0.6}{8.8}}_{\substack{voltage\\ divider}}\right)*\frac{\alpha}{2}\right]}_{\substack{output\ current\ of\ Long-tailed\ circuit\ with\\ 100pA\ tail\ current\ multiplied\ by\ 4\ (THB2)}} - \underbrace{3*100*10^{-12}\tanh\left[(x(t)-0.6)*\frac{\alpha}{2}\right]}_{\substack{output\ current\ of\ Long-tailed\ circuit\ with\\ 100pA\ tail\ current\ multiplied\ by\ 3\ (THB3)}} \\
&\quad -i(t)+\underbrace{I_c}_{875*10^{-12}A}+\underbrace{I_{in}}_{stimuli\ current} \Bigg\} \\
\underbrace{\alpha*23*10^{-14}}_{C=\alpha*230fF}\frac{di(t)}{dt} &= \underbrace{\left(\alpha*\underbrace{50*10^{-12}}_{\substack{I_b\to constant\\ current\ source}}\right)\underbrace{(2)}\left(\frac{R_2R_4}{R_1R_3}\right)}_{C\frac{di(t)}{dt}=(\alpha I_b)\left(\frac{R_2R_4}{R_1R_3}\right)i_{in}(t)-(\alpha I_d)i(t)\ (\log Domain\ Filter)} \Bigg[\underbrace{100*10^{-12}\tanh\left[\left(\underbrace{\frac{v(t)}{8.8}}_{\substack{voltage\\ divider}}-\underbrace{\frac{0.6}{8.8}}_{\substack{1\ voltage\\ divider}}\right)*\frac{\alpha}{2}\right]}_{Long-tailed\ circuit\ with\ 100pA\ tail\ current(THB1)} + \underbrace{100*10^{-12}}_{\substack{100pA\ constant\\ current\ source}} \Bigg]}_{i_{in}(t)} \\
&\quad -(\alpha*\underbrace{10*10^{-12}}_{\substack{I_d\to constatnt\\ current\ source}})i(t) \\
&\underbrace{v(t)>1.1\ \Rightarrow v(t)=V_R=0.70\,(Tonic\ \ Spiking),0.82\,(Tonic\ \ Bursting)}_{voltage\ comparator\ and\ resetter}
\end{aligned}
\tag{6.3}
$$

Conceptual block diagram of VLSI circuit derived from equation (6.3) is shown in Figure 6.5. Spiking and bursting behaviours are switched by only modifiying V_r voltage and I_{in} current. Some constant current sources are added for offsetting purposes. Efect of those currents are compensated in current I_c for not to change the over all behaviour of circuit. Internal design of all blocks will be explained at following sections. As can be seen from Figure 6.5 there are four main blocks in design:

- Tangent Hyperbolic Block
- Log Domain Filter Block
- Compare & Reset Block
- Current Reference Block (Current Sources)

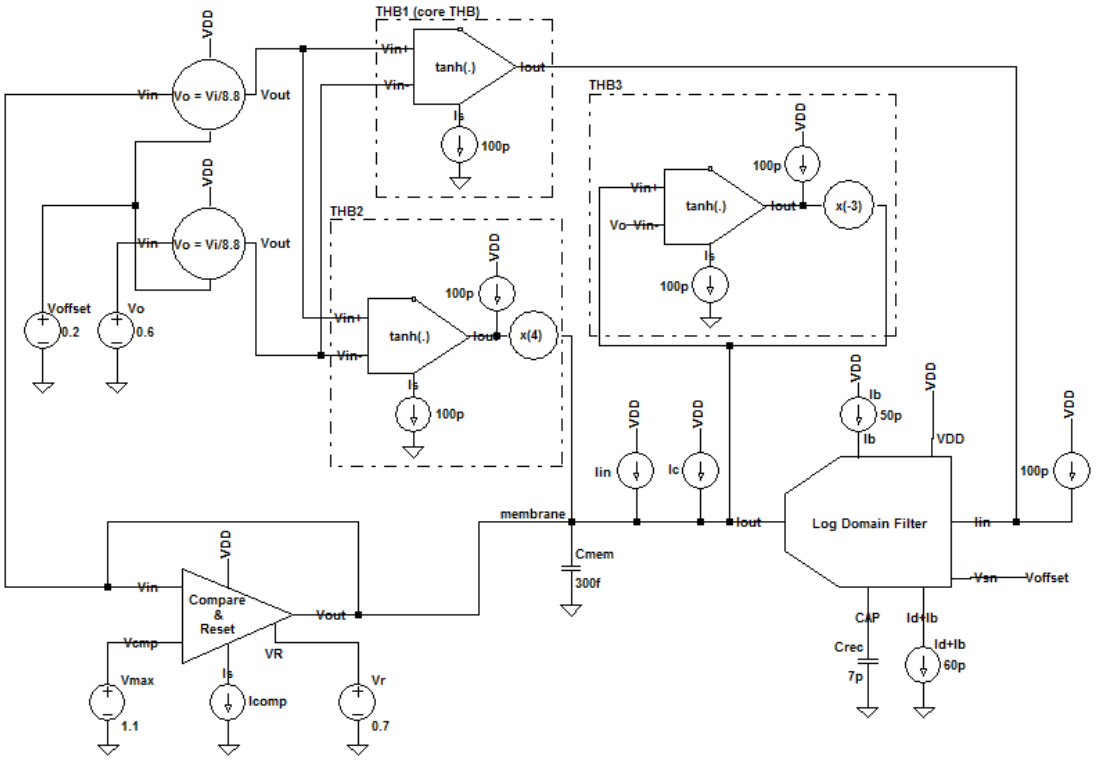


Figure 6.5 : Conceptual block diagram of the designed neuron circuit.

6.2 Tangent Hyperbolic Block (THB)

We used long tailed circuit topology with cascode output stage for implementing the tangent hyperbolic function as shown in Figure 6.6(a). Long tailed pair (or source coupled pair) is input stage of an operational amplifier. It consists of two matched transistors operating in subthreshold and a constant tail current source. By using subthreshold drain current equation in saturation given in equation (6.2), output current can be written as the function of the differantial input voltage as:

$$I_{out} = I_S \tanh\left[\frac{\alpha}{2}\left(V_{in+} - V_{in-}\right)\right] \tag{6.4}$$

When we change the polarity of the input voltages, output current is reversed since *tanh(-x) = -tanh(x).* So current direction can be changed by changing the place of the input voltages. We used the 2-layered cascode Current Mirror (CM) at the output for obtaining the high output resistance as given in equation (6.5) since the output resistance of the basic long tailed circuit is too low. Cascode output CM's does not limit the output voltage swing since the transistors are operating at subthreshold region. Also tail current is drived by using a cascode CM.

$$R_{out}=[r_{o6}(1+g_{m6}r_{o5})]//[r_{o16}(1+g_{m16}r_{o15})] \quad (6.5)$$

We designed a voltage tunable current reference explained in section 6.4 for eliminating the effect of process parameters variation on circuit function. Theoretically tunning voltage varies for different current values since there is no linear dependency with process parameter deviation. That means, different tail current values in THB blocks- which is the case for our design- may need different tunning voltages and so different current references. It is not applicable to use different current references for all seperate current sources since most of the power is consumed by current reference circuit in our design. So we used only one current reference and to optimize the effect of mentioned problems we designed a core THB with minimum tail current and then multiplied the output by a constant value for obtaining the real output of different THB's as shown in Figure 6.5. Tail currents are supplied from matched 100pA current sources. So THB2 and THB3 are implemented by using the core THB plus current multiplier at the outputs as it can be seen in Figure 6.5. Current multipliers are simple 3-layered cascode current mirrors as shown in Figure 6.6(b). Coscode current mirror did not limit the operation of circuit since transistors work at subthreshold region. Theoretically, operation of current mirrors are not affected from the process parameters variations and temperature variations, it is only affected from sizing variations that made us to take precautions for minimizing this effect by choosing minimum size $2\mu m/2\mu m$ even the technology is $0.18\mu m$. Also for proper opeation of THB2 and THB3 we applied a offset current to the junction point of core THB output and multiplier current mirror input. Offset currents effect on model equation is compensated in constant current I_c. Offset currents are also supplied from matched *100pA* current sources. Value of those offset currents are not critical since they are compensated at the output node (i.e. positive pin of membrane capacitance).

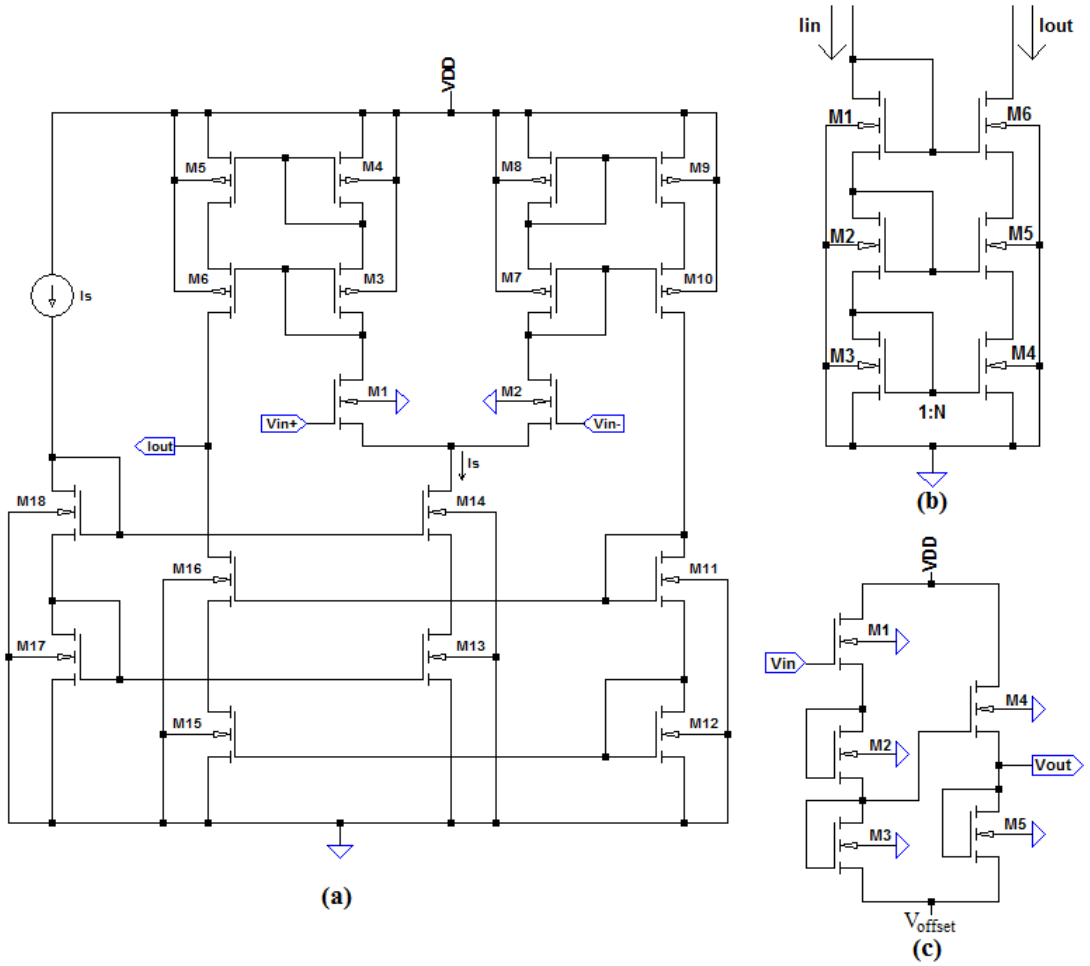


Figure 6.6 : Circuit parts that form the Tangent Hyperbolic Function Generators (a) Long tailed circuit topology with cascode output stage (b) N Multiplier Cascode Current Mirror $\left[\left(\frac{W}{L}\right)_4 = R_4 = N*\left(\frac{2\mu m}{2\mu m}\right) \rightarrow \begin{Bmatrix} N = 3.1 \; in \; THD2 \\ N = 4 \; in \; THD3 \end{Bmatrix}\right]$ (c) 2-layered ladder type diode connected linear voltage divider with offset *(V_{offset}=0.2 V)*.

As it can be seen from equation (6.4) intrinsic architecture of the circuit dictates the value of X_{sx} as $\alpha/2$. As we stated previously X_{sy} should be nearly 10 times smaller than X_{sx}. Since α (or 2*X_{sx}) is intrinsic parameter it is not possible to divide it but we can divide the input voltage to create the same effect. For this purpose we designed a two layered ladder type diode connected linear voltage divider with offset as shown in Figure 6.6(c). If we ignore the body effect and CLM, input to output relation of circuit is given as:

$$v_{out}(t) = \frac{v_{in}(t) + 5V_{offset} + \frac{2}{\alpha}\ln\left[\left(\frac{R_1}{R_2}\right)^2\left(\frac{R_2}{R_3}\right)\right]}{6} \tag{6.6}$$

When compared with the conventional MOS voltage dividers two layered configuration has the advantage of having less number of transistors for the same divider value and of reduced body effect. Offset voltage is needed to hold the output voltage above a certain value which should be high enough for proper operation of THB even at lower input voltages. Because the same ofsett voltage is applied to the both inputs of THB its effect is eliminated in overall function as it can be seen from equation (6.4). Theoretically, for matched transistors voltage divider gives input to output division factor of *6* as it can be found from equation (6.6). But, because of the body and CLM effects this factor is obtained *~8.8* by using curve fitted simulation results as shown in Figure 6.7. Offset voltage is selected *0.2 V*.

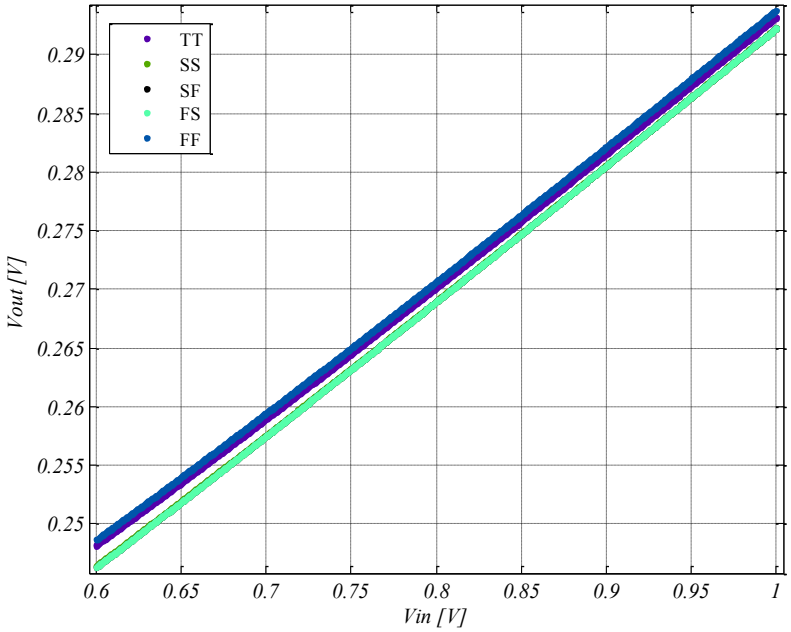
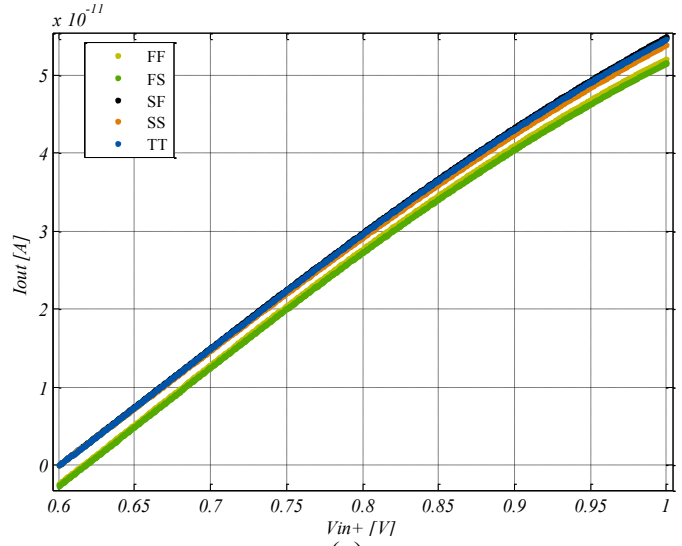


Figure 6.7 : Simulation results of voltage divider circuit for all corners.

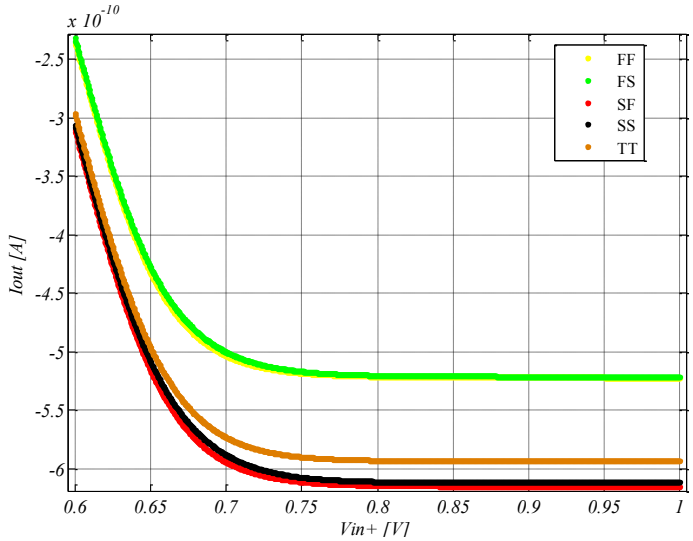
Corner analysis is an important method of analysing the effect of process parameter deviation on operation of VLSI circuits. Process corners represent the extremes of process parameter deviations within which a circuit that has been implemented onto the wafer must function correctly. As a naming convention the first letter refers to the NMOS transistor corner, and the second letter refers to the PMOS transistor corner. There are three corners named as typical, fast and slow. Fast and slow corners exhibit carrier mobilities that are higher and lower than normal. Typical corner is not really a corner, it is an avarage value but called a corner, anyway. There are therefore five possible corners: typical-typical (TT), fast-fast (FF), slow-slow (SS), fast-slow (FS), and slow-fast (SF).

We should design the neuron circuit such that it will show the same behaviour at all four corners (i.e FF, FS, SF, SS) plus typical (TT) to ensure the robustness of implementation. This condition is accomplished by obtaining the appropriate value of tunning voltage in current reference circuit for all corners seperately. So tunning voltage values and transistor sizes in current multipliers should be determined to complete the THB design.

We know that the simulation result of input to output relation for a THB circuit should match to analytic equation (6.4), theoretically. In practice, this means that we can fit the simulation results to analytic expressions by using a proper curve fitting method. For this purpose we used linear least squares method in our design. Accuracy metric of fitting was Root Mean Squared Error (RMSE) value. We iterate the design parameters until RMSE value stays below *%0.15* of maximum current value for THB1 (i.e. $RMSE_{THB1} < 0.15\ pA$), THB2 (i.e. $RMSE_{THB2} < 0.60\ pA$) and *%0.3* of maximum current value for THB3 (i.e. $RMSE_{THB3} < 0.9\ pA$). Expected RMSE is higher for THB3 since its output dynamic range broader than other THB's as it can be seen from Figure 6.8. THB1 and THB2 have input voltage dividers, thus real voltage swing at input for those blocks are about dividing ratio (i.e. *~8.8* for our design) times less than THB3's voltage swing.



(a)



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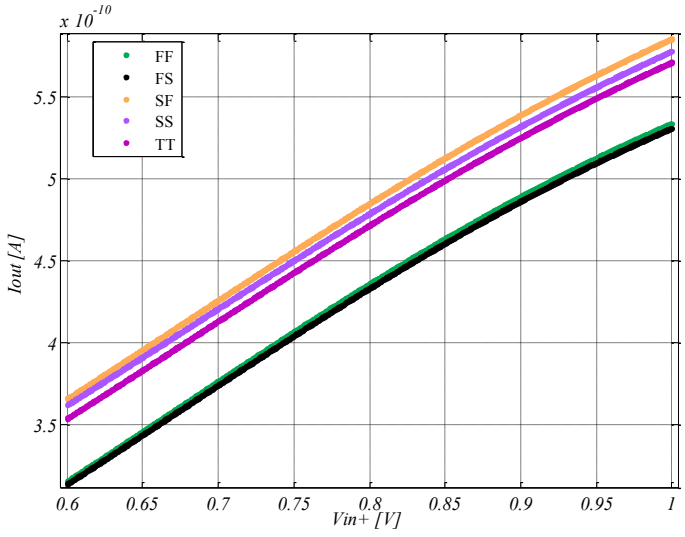


(c)

Figure 6.8 : Simulation results of THB circuits for all corners (a) THB1 (including voltage divider) (b) THB3 (c) THB2 (including voltage divider).

6.2.1 Iterative design methodology

We named design method mentioned in section 6.2 as Iterative Curve Fitting Methodology (ICFM). For design and optimisation of THB's we used this iterative approach. Curve fitting is applied *0.6V* to *1V* voltage interval since our design's dynamic takes place in this range as it can be seen from Figure 6.8. By rewriting the equation (6.4) such that it will be appropriate for curve fitting we obtain:

$$I_{out,THB} = I_s * tanh[X_{sx/y} * (V_{mem} - 0.6)] + I_o \quad (6.7)$$

Step by step explanation of our design process is given as:

1. Simulate THB1 for TT parameter set by connecting ideal *100 pA* current source to tail.
2. Fit the simulation result to equation (6.7) by changing X_{sy} (i.e. [(α/2)/8.8]) and I_s until the fitting error stays below $RMSE_{THB1}$. I_s should be around *100pA*. We know the value of $\alpha \approx 31$ for single transistor (see section 6.1) and dividing factor 8.8 for voltage divider so, by using those values as an initial value we can easily find X_{sy} parameter as *~1.5* after a few trial.
3. Simulate THB1 for TT parameter set by connecting real current source to tail.
4. Fit the simulation result to equation (6.7) by using the value of X_{sy} obtained at step 2 and iterate this step by altering the tunning voltage in Figure 6.11 until the fitting error stays below $RMSE_{THB1}$.
5. Repeat step 3 to 4 for all corners (i.e. FF, FS, SF, SS). At the end of this step X_{sy} and tunning voltage values for all corners has been obtained as can be seen in Table 6.2. Obtained tunning voltage values that fix the circuit operation for all corners are given in Table 6.5. Simulated core THB tail currents correspond to these voltages are given in Table 6.5, also. These currents fit to $I_s = 100pA$ in analytic expression (6.4).
6. Simulate THB2 for TT parameter set by connecting real current source to tail.
7. Fit the simulation result to equation (6.7) by using the value of X_{sy} obtained at step 2 and iterate this step by modifying the size of 4 multiplier CM's current multiplier transistor (i.e. M_4 in Figure 6.6(b)) until the fitting error stays below $RMSE_{THB2}$. X_{sy} and tunning voltage values has been obtained at step 5,

at the end of this step transistor sizes of THB2's output current multiplier has been obtained, also.

8. Simulate THB3 for TT parameter set by connecting real current source to tail.
9. Fit the simulation result to equation (6.7) by changing X_{sx} (i.e. $\alpha/2$) until the fitting error stays below $RMSE_{THB3}$. We know the value of $\alpha \approx 31$ for single transistor (see section 6.1) so, by using this value as an initial value we can easily find X_{sx} parameter as *~1.65* after a few trial.
10. Fit the simulation result to equation (6.7) by using the value of X_{sx} obtained at step 9 and iterate this step by modifying the size of 3 multiplier CM's current multiplier transistor (i.e. M_4 in Figure 6.6(b)) until the fitting error stays below $RMSE_{THB3}$. Tunning voltage values has been obtained at step 4, at the end of this step transistor sizes of THB3's output current multiplier has been obtained, also.

Table 6.2 : Parameter values of fitted equation for core THB (THB1).

Corner	Fitted Equation for THB1
TT	$I_{out} = 102*10^{-12}*\tanh[(V_{in+}-0.6)*1.5] - 0.276*10^{-12} \rightarrow RMSE= 7.797*10^{-14}$
SS	$I_{out} = 101*10^{-12}*\tanh[(V_{in+}-0.6)*1.5] - 0.247*10^{-12} \rightarrow RMSE= 7.054*10^{-14}$
SF	$I_{out} = 103*10^{-12}*\tanh[(V_{in+}-0.6)*1.5] - 0.233*10^{-12} \rightarrow RMSE= 6.979*10^{-14}$
FS	$I_{out} = 102*10^{-12}*\tanh[(V_{in+}-0.6)*1.5] - 2.596*10^{-12} \rightarrow RMSE= 1.68*10^{-13}$
FF	$I_{out} = 102.5*10^{-12}*\tanh[(V_{in+}-0.6)*1.5] - 2.372*10^{-12} \rightarrow RMSE= 1.828*10^{-}$

Table 6.3 : Parameter values of fitted equation for core THB2.

Corner	Fitted Equation for THB2
TT	$I_{out} = 408*10^{-12}*\tanh[(V_{in+}-0.6)*1.5] + 352.8*10^{-12} \rightarrow RMSE= 3.101*10^{-13}$
SS	$I_{out} = 405*10^{-12}*\tanh[(V_{in+}-0.6)*1.5] + 361.0*10^{-12} \rightarrow RMSE= 2.895*10^{-13}$
SF	$I_{out} = 412.4*10^{-12}*\tanh[(V_{in+}-0.6)*1.5] + 364.9*10^{-12} \rightarrow RMSE= 2.812*10^{-13}$
FS	$I_{out} = 408.6*10^{-12}*\tanh[(V_{in+}-0.6)*1.5] + 313.6*10^{-12} \rightarrow RMSE= 6.113*10^{-13}$
FF	$I_{out} = 410.9*10^{-12}*\tanh[(V_{in+}-0.6)*1.5] + 315.5*10^{-12} \rightarrow RMSE= 6.833*10^{-13}$

Table 6.4 : Parameter values of fitted equation for core THB3.

Corner	Fitted Equation for THB3
TT	$I_{out} = -299.3*10^{-12}*\tanh[(V_{in+}-0.6)*16.5] - 294.6*10^{-12} \rightarrow RMSE= 4.326*10^{-13}$
SS	$I_{out} = -308.5*10^{-12}*\tanh[(V_{in+}-0.6)*16.2] - 303.4*10^{-12} \rightarrow RMSE= 6.044*10^{-13}$
SF	$I_{out} = -306.8*10^{-12}*\tanh[(V_{in+}-0.6)*16.5] - 308.6*10^{-12} \rightarrow RMSE= 4.193*10^{-13}$
FS	$I_{out} = -290.5*10^{-12}*\tanh[(V_{in+}-0.6)*16.5] - 231.1*10^{-12} \rightarrow RMSE= 1.377*10^{-13}$
FF	$I_{out} = -286*10^{-12}*\tanh[(V_{in+}-0.6)*16.5] - 237.4*10^{-12} \rightarrow RMSE= 9.658*10^{-13}$

Table 6.5 : Tunning voltage values and corresponding simulated tail current.

	Typical (TT)	FF	FS	SF	SS
Tunning Voltage Value (mV)	470	396	404	538	545
Core THB Tail Current (pA)	90.1	93.2	93.1	92	90.8

6.3 Current Mode Log Domain Filter

If we get $y(t)$ as output and $Y_1*\tanh[(x(t)-X_o)*X_{sy}]$ as input at second state equation in neuron model we see that this expression correponds to a typical first order low pass filter. This is the expected characteristic since the second equation models the slow variable. Input and output variables was represented with current in our design which means that the filter should be current based as seen in equation (6.3). We implemented this block with log domain filter topology which is a useful block employed in neuromorphic circuits. For this purpose subthreshold operating MOS alternative of the circuit given in [58] has used. Circuit schematic is shown in Figure 6.9. Here M_1-M_4 transistors and I_b and I_{b+d} constant current sources are core structure that form the filter function while the others are cascode current mirrors for providing the high impedance paths for output current and constant current sources. Because of the subthreshold operation cascode layer does not limit the output voltage swing. Using translinear principle on core structure, we can easily show that the state equation of the log domain filter is given by:

$$C\frac{dI_{out}}{dt} = I_{in}(\alpha I_b)\left(\frac{R_2R_4}{R_1R_3}\right) - I_{out}(\alpha I_d) \tag{6.8}$$

Here α is intrinsic parameter that we can not manipulate it in design phase. We can only manipulate I_b and I_b+I_d current sources, C capacitor value and the aspect ratios

given as R_1, R_2, R_3, and R_4. Theoretical values of these parameters has given in equation (6.3). We know that $\alpha \approx 31$ so we selected $C = \alpha * 23 * 10^{-14} \approx 7\ pF$ in our design. C capacitance that corresponds to τ_y in our neuron model is mainly effective on time period of spikes which means the process originated variations on capacitor value have small effect on spiking behaviour. Thus, critical parameters for this block are constant current sources I_b and I_b+I_d since they are effective on spiking behaviour. Absolute variation is smaller for lower currents. For lowering the I_b current to a reasonable value we selected the $\left(\frac{R_2 R_4}{R_1 R_3}\right)$ ratio as *2*. To ensure the symmetry of the circuit this is done by setting $R_2 = R_4 = \frac{2.8\mu m}{2\mu m} \approx \frac{\sqrt{2} * 2\mu m}{2\mu m}$. So theoretically I_b=*50pA* and I_b+I_d=*60pA* is the case for our design as seen in equation (6.3). Analytic expressions of gain and phase functions of equation (6.8) can be given by:

$$A(f) = 20\log\left(\frac{I_{out}(f)}{I_{in}(f)}\right) = 20\log\left[\left(\frac{I_b}{I_d}\right)\left(\frac{R_2 R_4}{R_1 R_3}\right)\right] - 10\log\left[1 + f^2\left(2\Pi\frac{C}{\alpha I_d}\right)^2\right]$$
$$\varphi(f) = \Pi - arctg\left[\left(\frac{2\Pi C}{\alpha I_d}\right) f\right] \qquad (6.9)$$

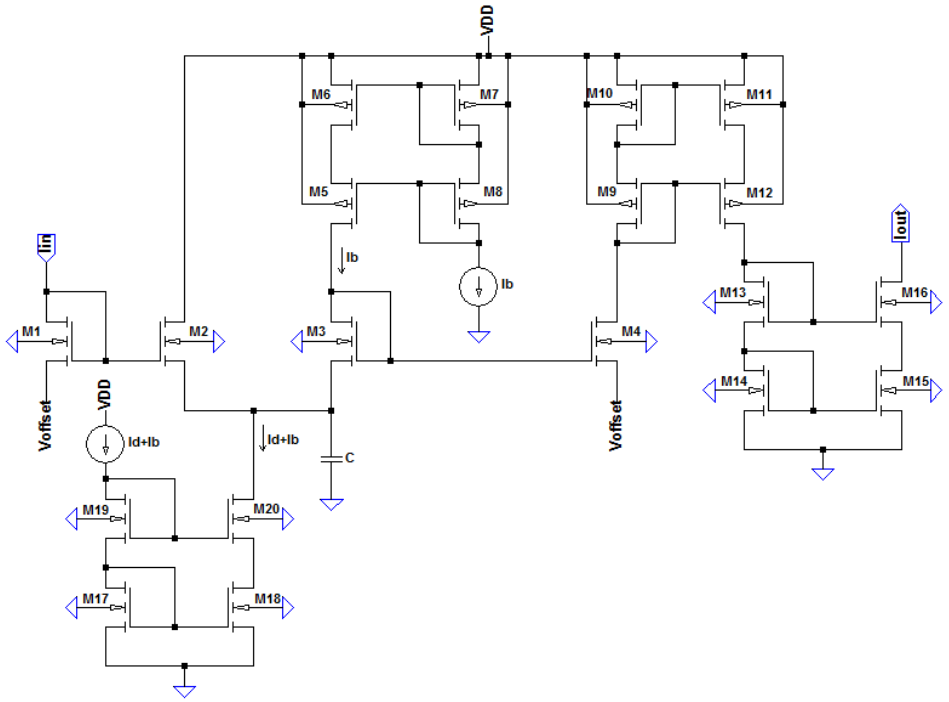


Figure 6.9 : Schematics of the current based Log Domain Filter Circuit.

For determining the real current values for I_b and I_b+I_d we fitted the AC analyses simulation result shown in Figure 6.10 to the analytical equation (6.9). Fitting parameters were the size of the divisor transistors of current mirrors used to adjust the real currents extracted from the current reference shown in Figure 6.11. Tunning voltages for all corners had been determined previously as in Table 6.6. The result of the simulations has shown that the current variation at the corners stay in reasonable range such that it will not change the behaviour of the neuron circuit.

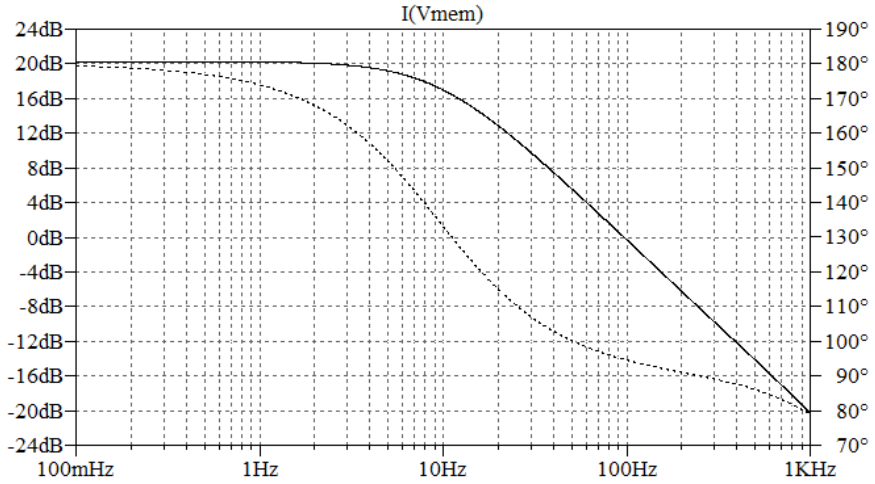


Figure 6.10 : Gain and Phase response of Current based Log Domain Filter Circuit for simulation with typical process parameters set.

Table 6.6 : Theoretical and simulated current values of log domain filter for all corners.

	Theoretical Value	Typical (TT)	FF	FS	SF	SS
I_b *(pA)*	*50*	49.6	51.5	51.3	50.7	49.8
I_b+I_d *(pA)*	60	59.7	61.8	61.5	61	60

6.4 Current Reference Circuit

Process parameter deviation and temperature dependency are the two most critical problems effective on the circuit operation. Especially for the circuits based on subthreshold operation, temperature dependency is a very common problem. To minimize the effect of process parameter deviation we designed the current reference circuit voltage tunable as it is explained in section 6.2.1 . Two main blocks of our design, explained in section 6.2 and 6.3 has intrinsic dependency to the temperature because of $\alpha \propto \frac{1}{T}$ as can be seen in equations (6.4) and (6.8). For current mirrors there is no temperature dependency theoretically if we ignore the CLM and body

effects. Those issues mean that for temperature optimisation we could only manipulate the constant currents which are generated from current reference circuit. So the dependence of constant currents I_S (i.e. tail current of core THB), I_b and I_b+I_d to temperature should be as low as possible in a reasonable temperature range for our design. Also, the most of the power drawn by the neuron circuit is consumed by this block. Those issues makes the current reference circuit the most critical part of neuron circuit design.

In the light of above issues we simplified and modified the circuit in [59] as shown in Figure 6.11. In this schematic M_1-M_7 constitutes the core current reference circuit, while the others are only for current division. In core circuit M_1 and M_2 operates in strong inversion while M_1 in triode and M_2 in saturation region. For proper operation aspect ratios of M_4 and M_3 and also M_6 and M_7 should be selected different. In our design we selected (R_3/R_4) and current mirror gain $M=(R_7/R_6)$ as $6\mu m/2\mu m$. For obtaining the low current value the aspect ratios of M_1 and M_2 should be selected as small as possible since they operate in strong inversion. So we selected R_1 and R_2 as $2\mu m/10\mu m$.

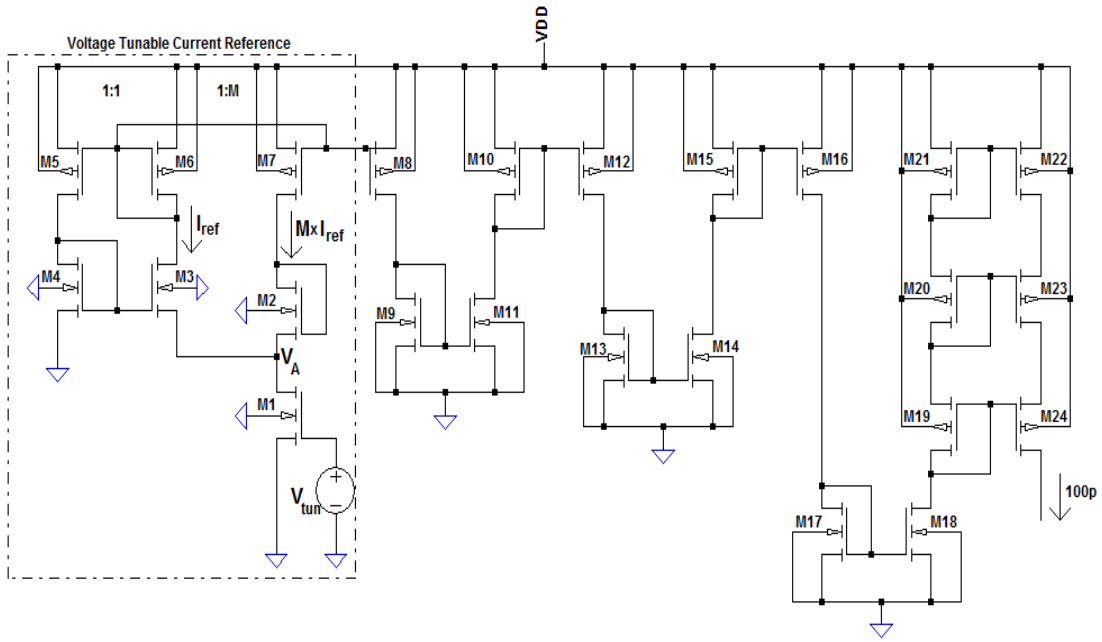


Figure 6.11 : Voltage tunable current reference and divisor current mirror circuits.

If we analyse the circuit in Figure 6.11 we can easily obtain the reference current equation as:

$$I_{ref} = \mu_n C_{ox} \frac{R_1}{M+1}(V_{tun} - V_{th})V_A = \mu_n C_{ox} \frac{R_1}{\left(\frac{R_7}{R_6}+1\right)}(V_{tun} - V_{th})nU_T \ln\left(\frac{R_3}{R_4}\right) \tag{6.10}$$

where μ_n is the carrier mobility, C_{ox} is the gate-oxide capacitance and V_{th} is the threshold voltage. The first order definition of temperature dependent parameters in equation (6.10) are:

$$U_T = \frac{k}{q}T \quad ; \quad V_{th} = V_{th0} - \kappa T \quad ; \quad \mu_n = \mu_{n0}\left(\frac{T}{T_0}\right)^{-m} \tag{6.11}$$

where, V_{th0} is the *0* Kelvin (K) threshold voltage, κ is the temperature coefficient (TC) of V_{th0}, k is the Boltzmann constant, q is the electron charge, μ_{n0} is the mobility at T_0 K and m is the mobility temperature exponent with an approximate value of *1.5*. By substituting the expressions in equation (6.11) to equation (6.10) we obtained TC of I_{ref} as:

$$TC_{I_{ref}} = \frac{1}{I_{ref}}\frac{dI_{ref}}{dT} = \frac{2-m}{T} \tag{6.12}$$

Temperature dependency curves of three main critical currents are shown in Figure 6.12. From simulation results we can say that the temperature dependent current variations are in reasonable range for our design.

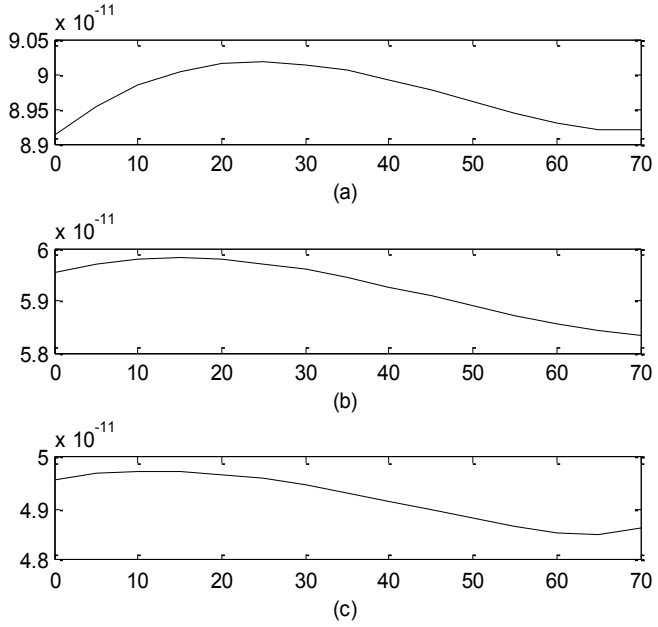


Figure 6.12 : Temperature dependence of critical currents in neuron circuit for simulation with typical process parameters set (TT). Horizontal axis is temperature in degree (^{0}C), vertical axis is current in Ampere (A) (a) Tail current of core THB (b) I_b+I_d and (c) I_b.

6.5 Compare & Reset Circuit

For resetting the membrane voltage value we should discharge the membrane capacitance until its voltage decreases to V_R. For this purpose we should design a comparator circuit which drives a discharge switch with high current capacity. Designed circuit is shown in Figure 6.13. This circuit implements the third expression in equation (6.3). Comparator circuit is implemented by connecting the input of two stage inverter (M_6-M_9) to the output of a simple long tailed circuit (M_1-M_4) which acts as differantial amplifier. Discharge switch is implemented with big sized M_5 transistor $\left(R_5 = \frac{20\mu m}{1\mu m}\right)$ since it should have high current capacity. I_{comp} is tail current which should be high enough to drive output inverter stage as fast as possible. Thus we selected this current $\approx 2.3\ nA$.

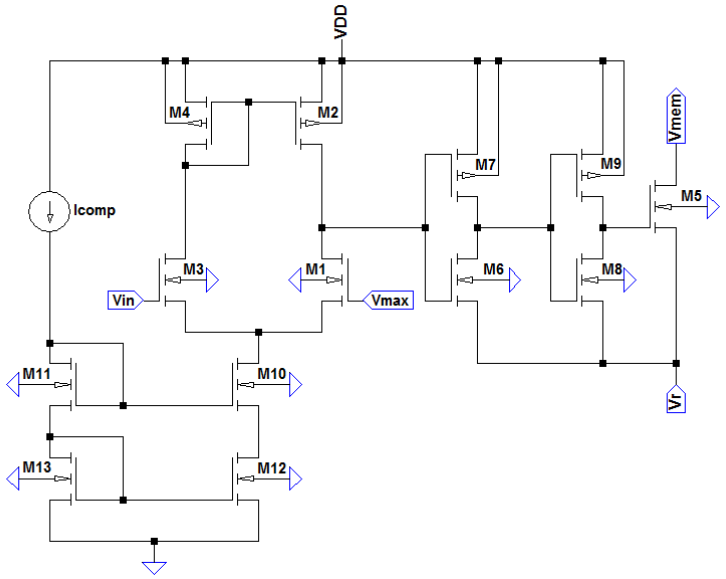
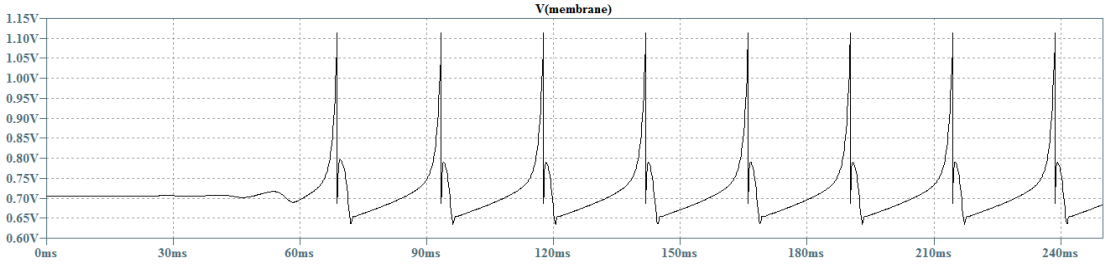


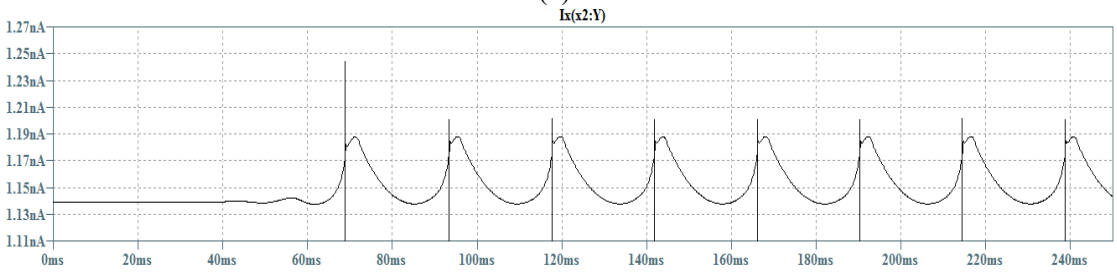
Figure 6.13 : Schematics of the designed Compare and Reset circuit.

6.6 TSMC 0.18µm Simulation Results

We explained all blocks that form the neuron circuit given in Figure 6.5 in previous sections. Constant current source I_c in in Figure 6.5 is determined as *1.2 nA* in overall design. This value is different from the value given in implemented equation (6.3) since the effect of ofsett currents from all blocks should be compensated in this constant current source. Simulation results with TT process parameters are shown in Figure 6.14 and Figure 6.15. In those figures (a) is time variation of membrane voltage that corresponds to *x(t)* and (b) is slow variable current that corresponds to *y(t)* in new neuron model.

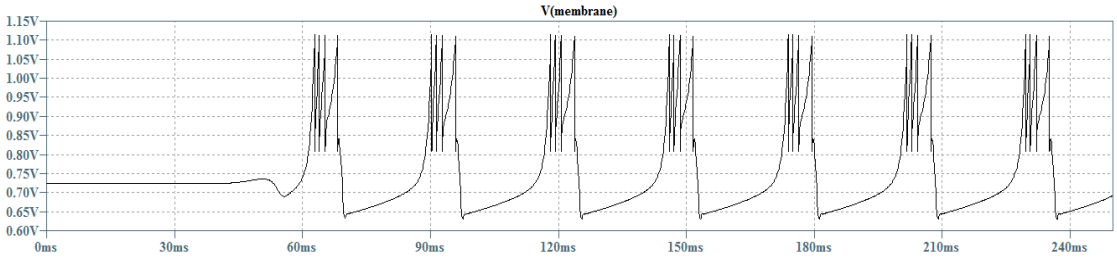


(a)

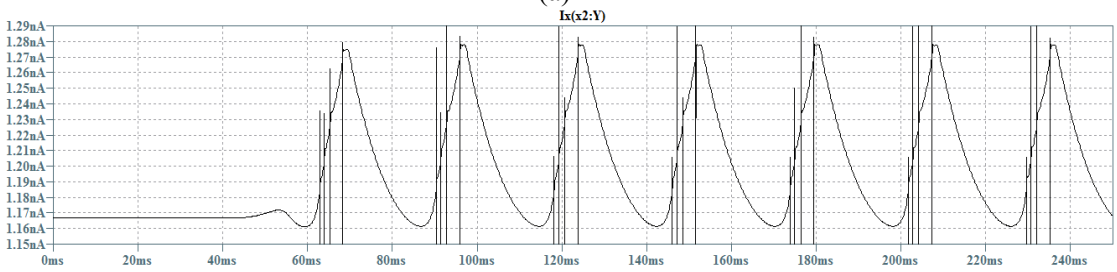


(b)

Figure 6.14 : Simulation results of designed neuron circuit for Tonic Bursting with $V_R = 0.70V$ and $I_{in} = 105pA$ (a) membrane voltage (b) slow variable current.



(a)



(b)

Figure 6.15 : Simulation results of designed neuron circuit for Tonic Bursting with $V_R = 0.82V$ and $I_{in} = 130pA$ (a) membrane voltage (b) slow variable current.

Average power consumption of designed neuron circuit is obtained *241 nW* which meets the low power requirement. As it is expected, simulation results are in well agreement with the numerical simulations given in Figure 6.4. Slow variable currents, shown in Figure 6.14(b) and Figure 6.15(b), have sharp spikes at spiking instants of mebrane voltage even this is not seen in numerical simulations in Figure 6.4. This current is the output of log-domain filter explained in section 6.3. In neuron

circuit this output is connected to the membrane node (see Figure 6.5) so the voltage at this node is same with membrane voltage swing. Eventually sharp spikes in slow variable current causes from the CLM effect (i.e. finite output impedance) at the output cascode transistors M_{15} and M_{16} of log domain filter circuit.

6.7 Layout Design with AMS *0.35μm* Technology

So far, all designs and simulations are carried out with TSMC *0.18μm* technology by using LTSpice design tools. We redesigned all the subblocks and blocks of neuron circuit with AMS *0.35μm* SiGe-BiCMOS process by using Cadence® Virtuoso® tools. This is done for both verifiying the previous design and implementing the layout of the neuron. For obtaining the accurate results we set the Spectre® simulator option G_{min} to 10^{-16} because the circuit operates at low currents.

If we analyse a single MOS transistor we see that the transconductance $\left(g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \right)$ of this transistor is quite lower than the TSMC's transistor which means higher voltage value is needed for AMS to have the same amount of current obtained by TSMC. This situation can be clearly seen when a comparison is made between the Figure 6.2 and Figure 6.16. By fitting the simulation results given in Figure 6.16(b) to equation (6.2) we obtained $\alpha \cong 30.2$ and $I_S \cong 56.8\,fA$ for AMS *0.35μm* process.

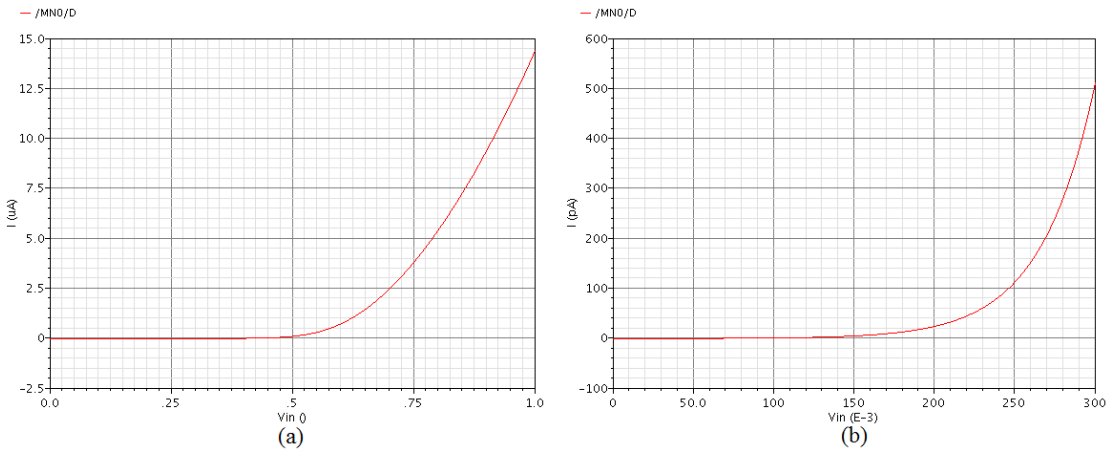


Figure 6.16 : I_{ds} vs V_{gs} characteristic of single NMOS tranzistor (a) for all operation regions and (b) subthreshold region.

We kept the circuit topology and transistor sizes same- except that a few tranzistors in current divider block- as in TSMC design and obtained the same results by only modifiying the value of voltage and currents sources and capacitors. Because the

transconductance of transistors are quite lower for AMS design, operating and supply voltages should be shifted to higher values when compared with TSMC design. By using the results obtained at simulations we determined the optimum value of supply voltage (*VDD*) as *2.5V* and offset voltage *(V_{offset})* of voltage divider and log domain filter circuits as *0.5V*. Other voltage values and design parameters of implemented neuron are given in Table 6.7. Mebrane capacitance value is selected *400 fF*. And capacitance value of log domain filter block is selected *6 pF*. Iterative Curve Fitting Methodology used in TSMC design is also used in this design. Simulation results of main blocks are given in Figure 6.17.

Table 6.7 : Parameter values of VLSI implemented neuron with AMS *0.35μm* Technology (X_{max} *= 1.6 V,* X_o *= -1.0*).

	Figure	τ_x	X_1	X_2	X_{sx}	X_{sy}	τ_y	Y_1	Y_2	X_r	I_{in}
Tonic Spikes	Figure 6.18(a)	4e-12	4e-9	3e-9	15.0	1.5	0.020	1e-8	-3.75e-9	1.10	81e-12
Tonic Bursts	Figure 6.18(b)	4e-12	4e-9	3e-9	15.0	1.5	0.020	1e-8	-3.75e-9	1.28	36e-11

To see the effect of the process parameter deviation on circuit function we simulated the design at all process corners. As we explained in previous sections, constant current sources are the most affected part of the neuron circuit from process parameter deviation. For minimizing that affect we designed the current sources voltage tunable as explained in section 6.4. Thus we obtained the proper tunning voltage values that fix the circuit operation at all corners. Obtained voltage values and corresponding core THB's tail current for different corners are given in Table 6.8. The corners provided with AMS *0.35μm* are:

- **cmostm**: Typical mean parameters. This corner corresponds to TT of TSMC.
- **cmosws**: Worst case speed, the transistors are slower and weaker then typical. This corner corresponds to SS of TSMC.
- **cmoswp**: Worst case power, the transistors are faster and consumes more power then typical. This corner corresponds to FF of TSMC.
- **cmoswo**: Worst case one, the PMOS transistors are slower and the NMOS transistors are faster the typical. This corner corresponds to FS of TSMC.

➢ **cmoswz**: Worst case zero, the NMOS transistors are slower and the PMOS transistors are faster the typical. This corner corresponds to SF of TSMC.

Table 6.8 : Tunning voltage values and corresponding simulated tail current for AMS 0.35µm technology corners.

	tm	wp	ws	wo	wz
Tunning Voltage Value (mV)	*592*	*469*	*658*	*456*	*674*
Core THB Tail Current (pA)	*90.5*	*80*	*104*	*84*	*99*

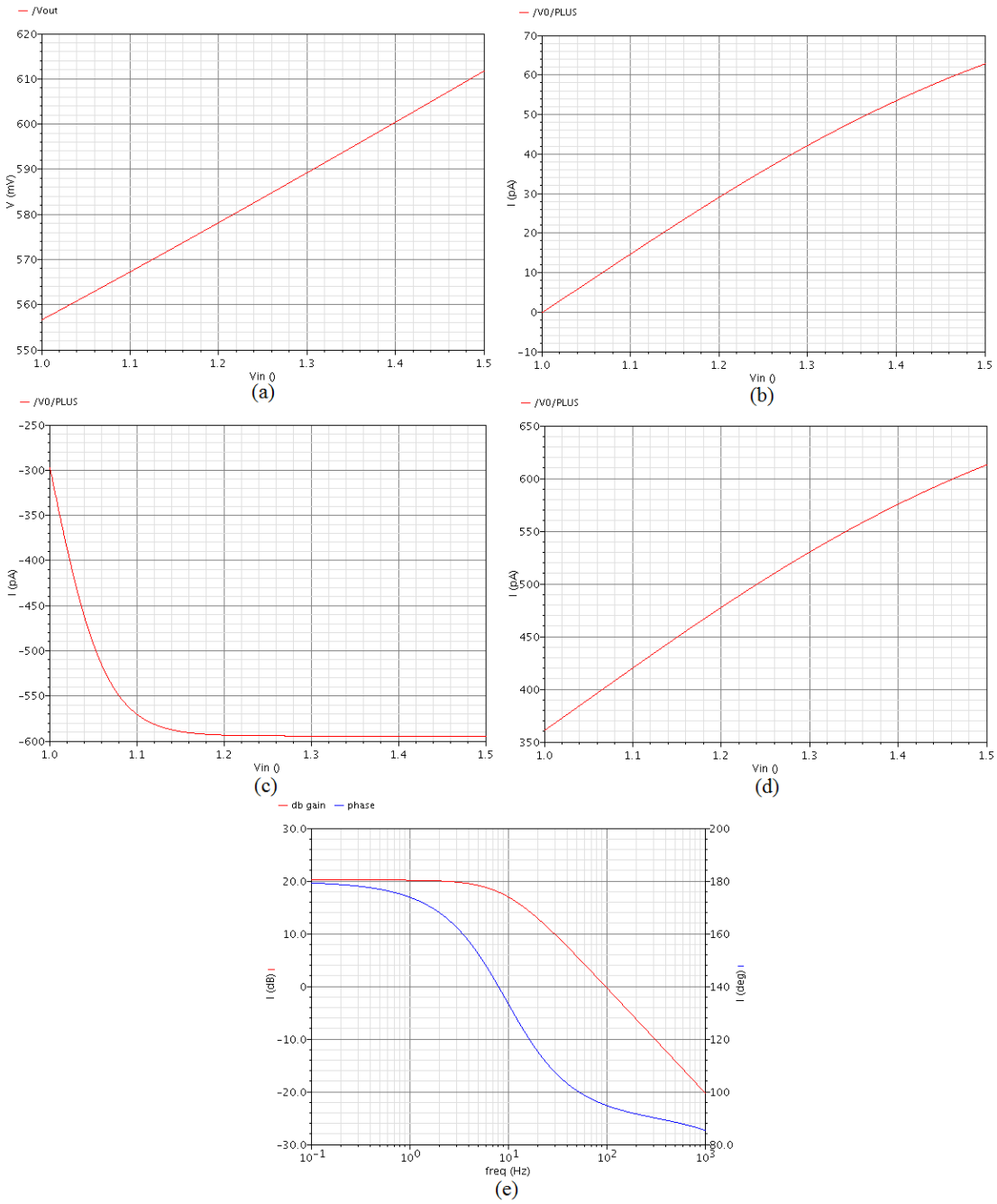


Figure 6.17 : Simulation results of main blocks with typical mean parameters (a) Voltage Divider (b)THB1 (including voltage divider) (c)THB3 (d)THB2 (including voltage divider) (e) Log Domain Filter

Simulation results of full neuron circuit obtained with typical (tm) AMS *0.35μm* process parameters are shown in Figure 6.18. As can be seen from the figure, similar results with previously explained TSMC design are obtained. As we stated earlier we only made a few modifications on TSMC design. Circuit topology and most of tranzistor sizes remained the same with TSMC design. By verifying the design with two different technology and two different design tools we have almost guaranteed the fabricated circuit to operate properly.

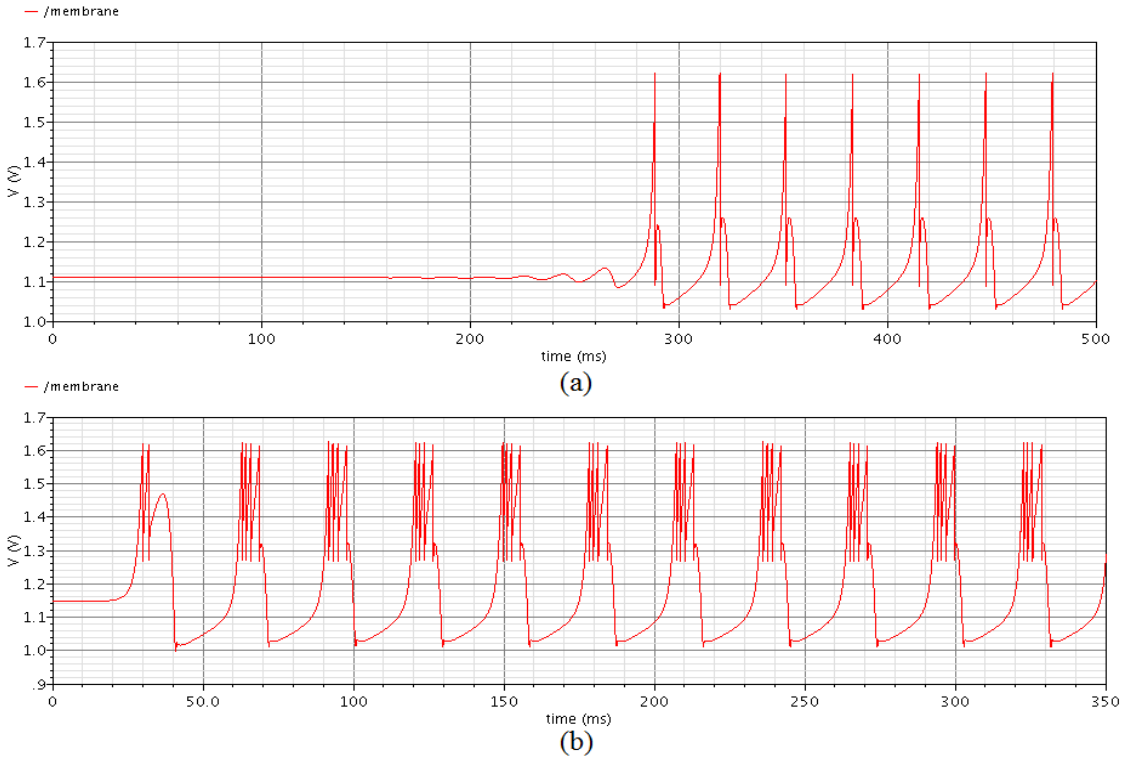


Figure 6.18 : Representation of (a) Tonic Spiking (b) Tonic Bursting behaviour of neuron circuit simulated with AMS *0.35μm* technology.

We implemented the layout of the full neuron circuit by using AMS *0.35μm* design kit. To provide the modularity and reuseability of the design, layout of all blocks and subblocks are drawn seperately and then assembled at the top level as shown in Figure 6.19. Total area of the Layout is $0.099\text{mm} * 0.129\text{mm} \cong 0.0128\,\text{mm}^2$. It can be seen from the Figure 6.19 that the most of the area are occupied by the poly silicon capacitors.

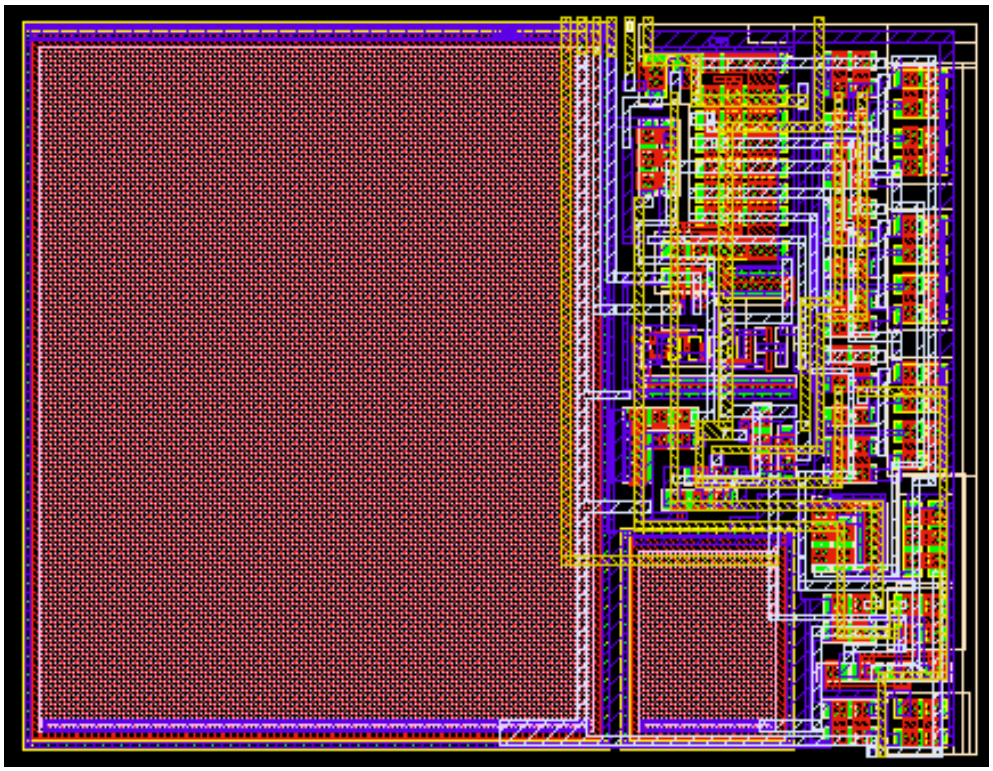


Figure 6.19 : Layout of designed neuron circuit with AMS 0.35 µm.

6.8 Comparison with Similar Designs

In conclusion, comparison between our design and some other similar designs are given in Table 6.9.

Table 6.9 : Comparison of main parameters between our design and some other similar designs.

	Area [µm^2]	Power [nW]	Biological Timescale Factor	Spike Shape Conformity to Real Behaviour	Model Name
[34]	2980	7	x10	not fair	Izhikevich
[38]	-	100.000	x10^5	good	AdEx I&F
[33]	20000	20.000	x1 (real)	good	Izhikevich
[31]	2800	40.000	x10^4	good	Modified Izhikevich
[60]	40000	70.000	x1(real)	not fair	Mihalas-Niebur
This Design for TSMC *0.18µm*	-	241	x1 (real)	very good	Our Model
This Design for AMS *0.35µm*	12800	277.5	x1 (real)	very good	Our Model

7. SIMPLE NETWORK DYNAMICS OF NEURON WITH NEW SYNAPSE MODEL

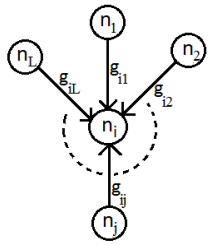
7.1 New Synapse Model

In most of the synapse models, temporal dynamics are neglected and synapses are assumed as an instantaneous multiplier operator. Therefore, those models cannot explain the basic signal processing characteristics of the neuron in principle [39]. A realistic model should take into consideration the spatial and temporal summation of synaptic currents. In the light of these observations, we offered a new dynamical synapse model for coupling the neurons to create realistic SNNs. When we offering the model we inspired from the model and mechanism explained in [61]. Equation of offered model is:

$$I_{syn}\left[n_{pre}, n_{post}\right] = g\, s_{pre}(t) \tanh\left[\left(x_{post}(t) + X_{rev}\right) X_{ss}\right]$$
$$\tau_s \frac{ds_{pre}(t)}{dt} = S_1 \tanh\left[\left(x_{pre}(t) + X_o\right) X_{ss}\right] - S_2 s_{pre}(t) \tag{7.1}$$

where I_{syn} is synaptic current caused by presynaptic neuron, g, maximal synaptic conductance, $s_{pre}(t)$, instantaneous synaptic activation caused by presynaptic neuron, X_{rev}, synaptic reversal potential, τ_s synaptic time constant and $x_{pre}(t)$ and $x_{post}(t)$ are the presynaptic and postsynaptic voltages respectively. As a big advantage of model we can make a synapse excitatory or inhibitory by selecting a proper value for X_{rev} parameter.

By using the new neuron and synapse model given by equation (5.1) and (7.1) respectively we can define a SNN with the generic formulation as in equation (7.2).



$$\tau_{x,i}\frac{dx_i(t)}{dt}=\begin{bmatrix} X_{1,i}\tanh\left[(x_i(t)+X_o)X_{sy}\right]-X_{2,i}\tanh\left[(x_i(t)+X_o)X_{sx}\right]-y_i(t) \\ +\sum_{j=1}^{L} g_{ij}s_j(t)\tanh\left[(x_i(t)+X_{rev,j})X_{ss}\right]+I_{stim,i} \end{bmatrix} \tag{7.2}$$

$$\tau_{y,i}\frac{dy_i(t)}{dt}=Y_{1,i}\tanh\left[(x_i(t)+X_o)X_{sy}\right]-y_i(t)+Y_{2,i}$$

$$\tau_{s,i}\frac{ds_i(t)}{dt}=S_{1,i}\tanh\left[(x_i(t)+X_o)X_{ss}\right]-S_{2,i}s_i(t)$$

$$x_i(t)>X_{\max}\Rightarrow x_i(t)\leftarrow X_r$$

$$g_{ij}=\begin{cases} 0 \rightarrow j^{th}\ neuron\ uncoupled\ to\ i^{th}\ neuron \\ g_{ij} \rightarrow j^{th}\ neuron\ coupled\ to\ i^{th}\ neuron \end{cases}$$

7.2 Phase Response Curve of New Neuron Model

In physics and chemistry, the Phase Response Curve (PRC), i.e. the oscillator's response to weak perturbations, is a useful tool to understand the collective dynamical properties like coherent oscillations, traveling waves, and pattern formation. A perturbation is weak if its effect on the amplitude and intrinsic period is negligible. This approximation is often valid also in firing neurons, where a small current pulse delays or advances the next spike without changing its shape or average firing frequency [62].

Let *t* denote the time since the last spike, let *A* parameterize the amplitude of the perturbing stimulus, and let *T(A, t)* denote the time of the next spike after the stimulus. Note that *T(0, t)* is baseline firing period. We can calculate the phase response (PR) in the following way [63].

$$PR(t)=\frac{T(0,t)-T(A,t)}{T(0,t)} \tag{7.3}$$

PRC calculation is demonstrated in Figure 7.1. According to this illustration, a weak stimuli input with *A* amplitude is applied at the instant of t_i and new period caused by delaying or advancing of the next spike is obtained as $T(A,t_i)$. Then this value is substituted in equation (7.3) so PR value for instant of t_i is obtained. This is done all

through the one period of baseline firing and calculated values are shown on a graphic. Extracted graphic is called PRC.

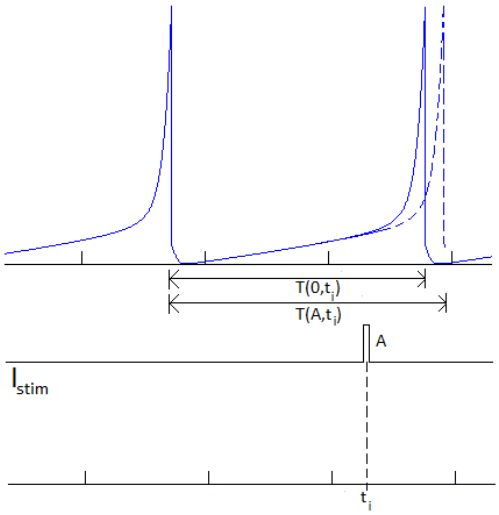


Figure 7.1 : Demonstration of Phase Response Curve (PRC) calculation.

By utilizing the method explained in previous pharagraphs and using the equation (7.3) and (5.1) we extracted the PRC of new neuron model as shown in Figure 7.2. Neuron parameters used in PRC calculation is given in "Tonic Spiking" named row of Table 6.1. Perturbing current is 8% of stimulus current in this calculation. Figure 7.2 shows that our neuron has Type II PRC and can show synchronization behavior in a network.

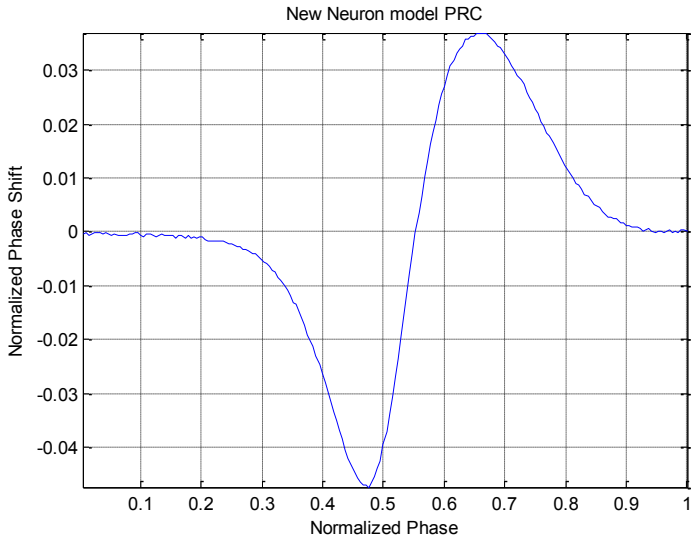


Figure 7.2 : PRC calculation result of VLSI circuit implemented neuron.

Synchronization phenomena in coupled systems are very important models to describe various higher dimensional nonlinear phonomena in the field of natural

science [43]. We can briefly describe the synchronization as an adjustment of rhythms of oscillating systems due to their weak interaction. Neural networks have the ability of producing some kinds of phase patterns, and thought to be utilized for associative memory, image processing etc. [44-46]. Synchronized activity of neurons takes role in a wide range from cognitive functions to rhythmic movements of animals. Coupled neurons (in general oscillators) can show in phase synchronization behaviour if the phase difference is zero, anti phase if the phase difference is close to 180° and N-phase if the phase difference is arbitrary.

A neural network constructed by using offered synapse and neuron model can show rich synchronization behavior by only altering X_{rev} parameter in equation (7.1). If this parameter is selected as I_{syn} will always be positive/negative then the synapse is excitatory/inhibitory.

We connected different number of neurons reciprocally that will form a ring coupled network as in Figure 7.3 for investigating the synchronization phenomena. This analysis can be evaluated as a practical application of offered models. Odd and even number of neurons ($N = 2k+1$ and $N = 2k$ for $k = 1, 2, 3, ...$) is connected and investigated separately. Our goal is to obtain in phase, anti phase and N-phase synchronization patterns.

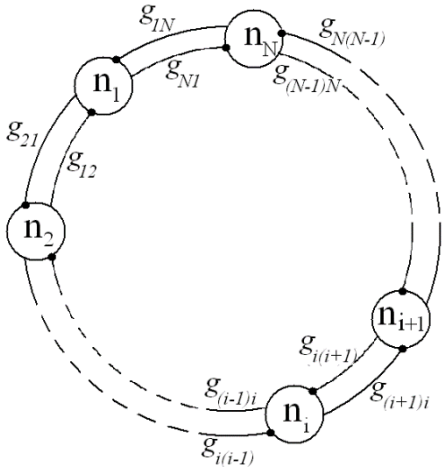
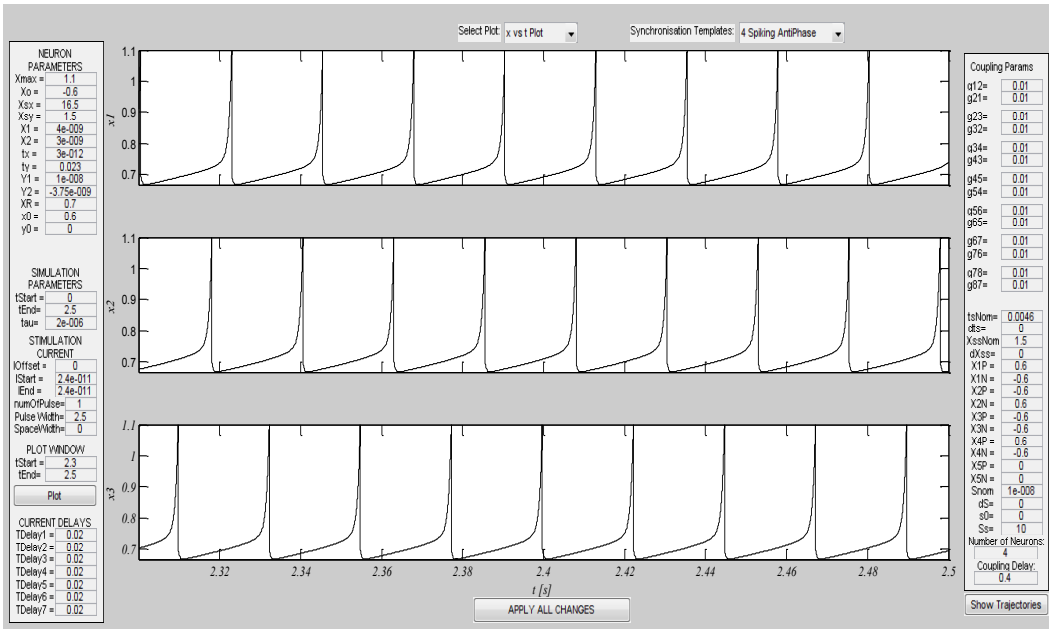


Figure 7.3 : Neural network topology with the ring coupled neurons.

We designed a software application in MATLAB to study the synchronization behaviour of ring coupled neural network. This application has a GUI , shown in Figure 7.4, for accepting the inputs from user and displaying the calculated outputs. By using this GUI one can enter the neuron parameters, simulation time, stimulation

current, synapse and coupling parameters, plotting parameters and can run the simulation. This software allows the analysis of ring coupled network with maximum 5 neuron. Heun's method explained in section 5.1 is used to solve the differential equations numericaly.



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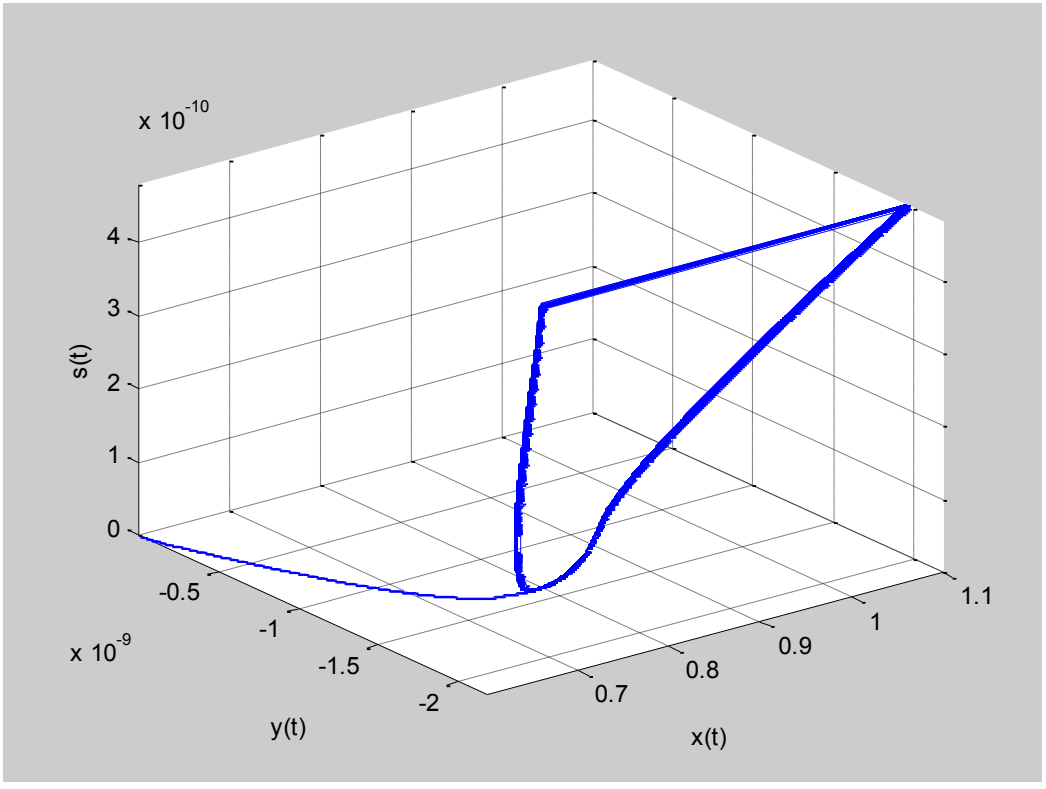


(b)

Figure 7.4 : GUI of software application designed in MATLAB to examine the synchronization behavior of ring coupled neurons (a) main window (b) phase plane analysis window.

Neuron parameters, used all through the analysis at this section, are given in "Tonic Spiking" named row of Table 6.1. To meet the weak coupling condition we limited the I_{syn} to be maximum *10%* of I_{stim}. As we mentioned before we obtained different synchronization patterns by only altering the value of X_{rev}. Synapse parameters except that X_{rev} are also the same for all networks. Used parameters are:

$$\tau_s = 0.0046 \; ; \; S_1 = 10^{-8} \; ; \; S_2 = 10 \; ; \; g_{ij} = 0.015 \; ; \; X_{ss} = X_{sy} = 1.5$$

In all simulations, initially, neurons generate spikes independently throughout the *400 ms* and then the coupling is activated. The initial state of phase difference is also set properly. To see an inphase behavior after coupling, we set the initial phase difference different from 0°. Similarly, we set the initial phase difference close to 0°, for obtaining an antiphase or N-phase behavior. Also, it takes time to settle to a stable synchronization state for neurons since the coupling is weak. Stable synchronization exists after the instant that the amplitude and period of I_{syn} remains constant.

As a beginning we connected two neurons reciprocally as in Figure 7.5 for observing in phase and anti phase synchronization. As expected, we obtained anti phase synchronization with $X_{1rev} = -0.6$ and $X_{2rev} = 0.6$ as shown in Figure 7.6 and in phase synchronization with $X_{1rev} = 0.6$ and $X_{2rev} = 0.6$ as can be seen from Figure 7.7. We can also get inphase behaviour for $X_{1rev} = -0.6$ and $X_{2rev} = -0.6$ but in this case it takes longer time to synchronize as can be seen from Figure 7.8.

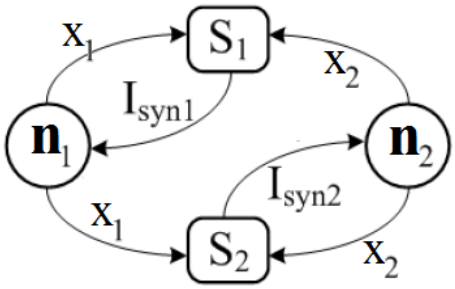
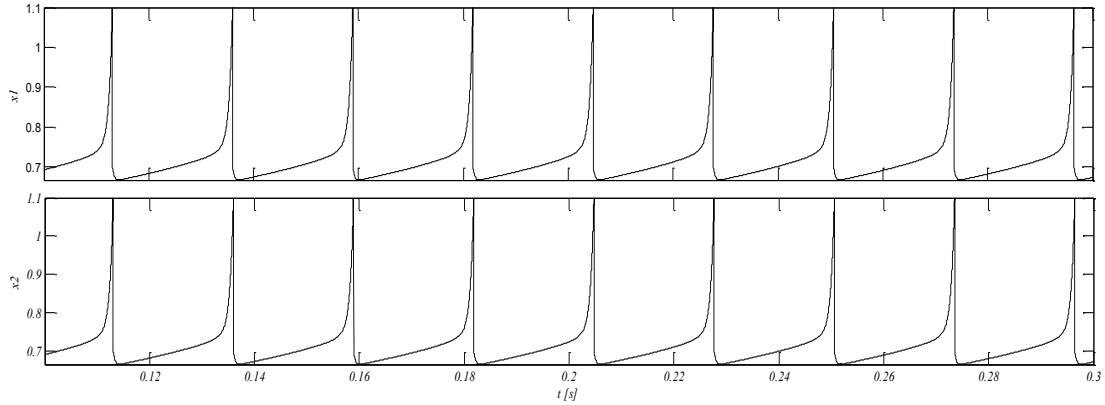


Figure 7.5 : Reciprocal connection of two neurons in a ring topology.



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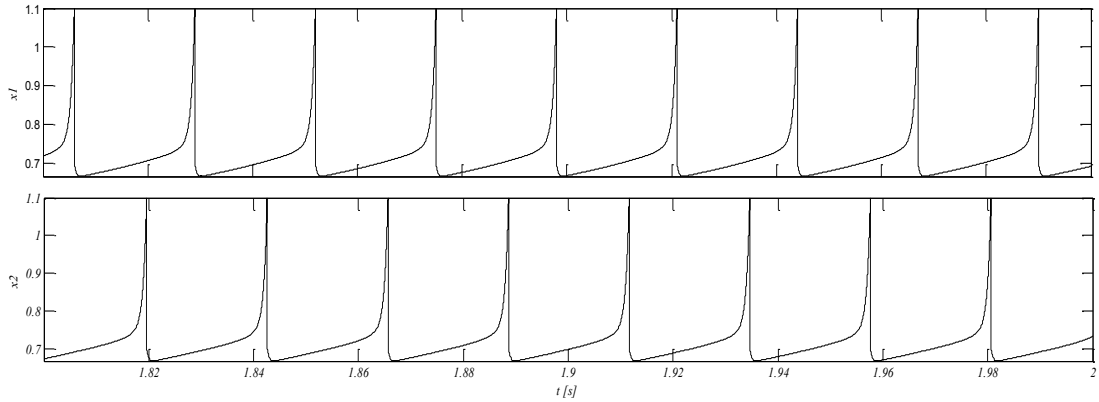

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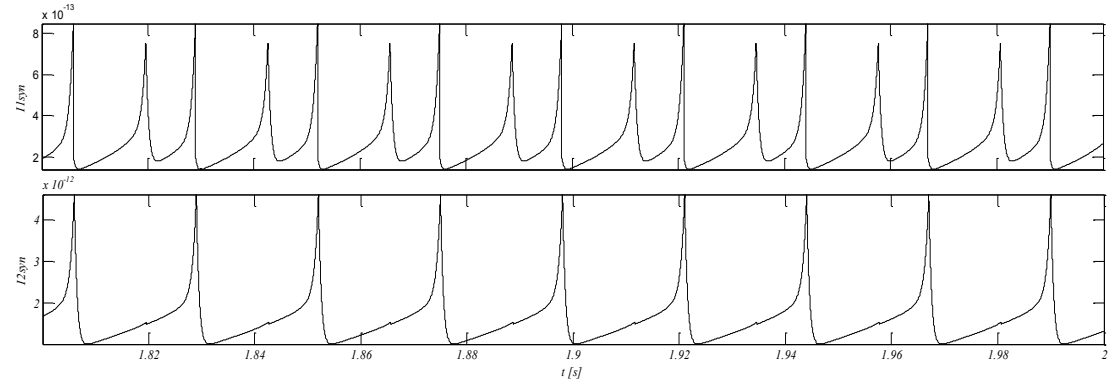
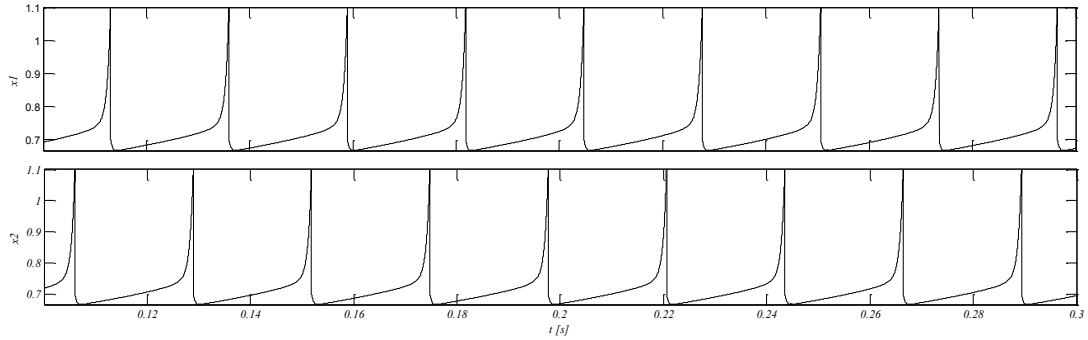
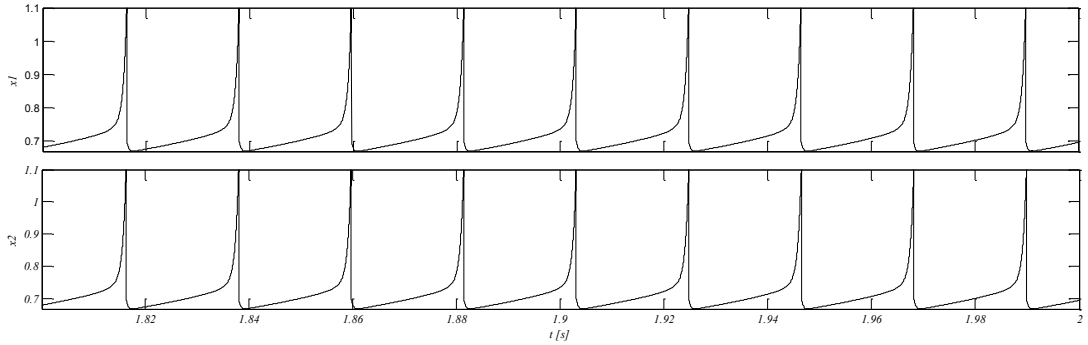


(c)

Figure 7.6 : Antiphase synchronization of two reciprocally connected neurons. (a) Initial independent spiking (b) final synchronized state for $X_{1rev} = -0.6$ and $X_{2rev} = 0.6$ (c) synaptic currents at synchronized state.



(a)



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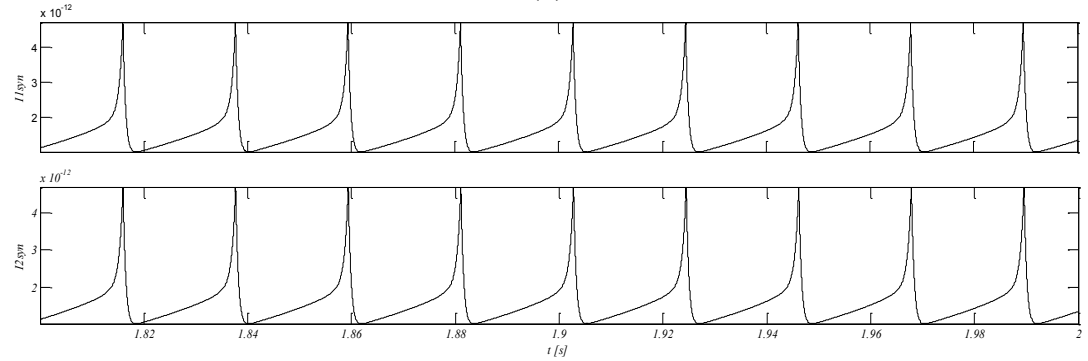


(c)

Figure 7.7 : In phase synchronization of two reciprocally connected neurons. (a) Initial independent spiking (b) final synchronized state for $X_{1rev} = 0.6$ and $X_{2rev} = 0.6$ (c) synaptic currents at synchronized state.

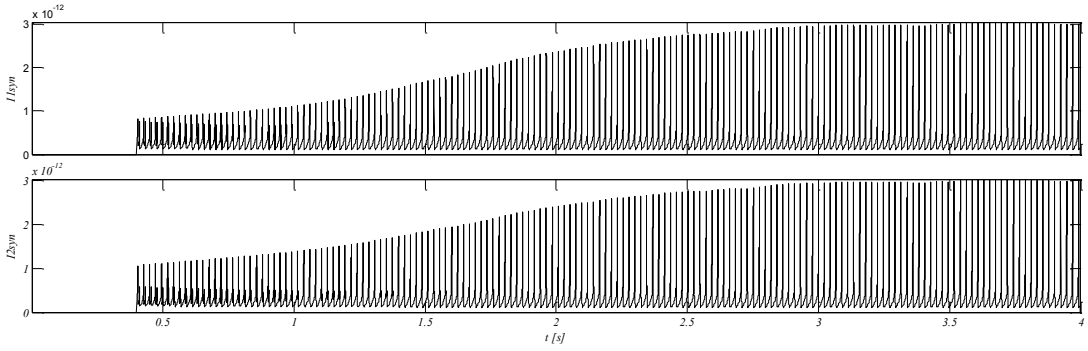


Figure 7.8 : Synaptic currents until the in phase synchronization behavior of two reciprocally connected neurons exist for $X_{1rev} = -0.6$ and $X_{2rev} = -0.6$.

Simulation result for the networks with three and four neurons are given throught the Figure 7.9 and Figure 7.12. For the ring structured networks involving three or more neurons it is seen from Figure 7.3 that all neurons are driven by two neurons since they connected reciprocally. This situation means two X_{rev} parameter is effective on each neuron. One X_{rev} comes from previous and the other one comes from the next neuron. In simulation results we used *P* indice for previous and *N* indice for next. For example, 3rd numbered neuron is affected by $X_{3rev,P}$ and $X_{3rev,N}$.

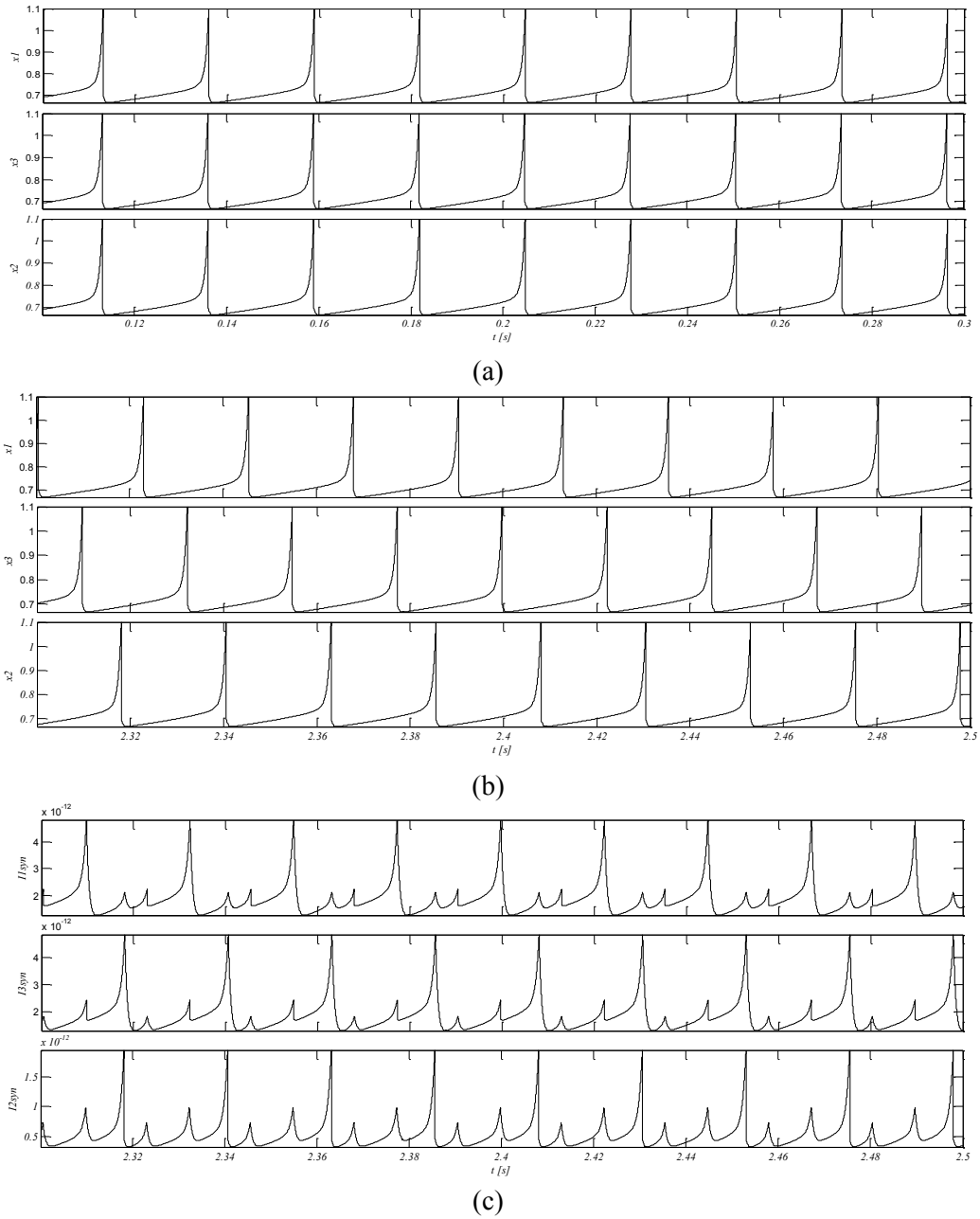
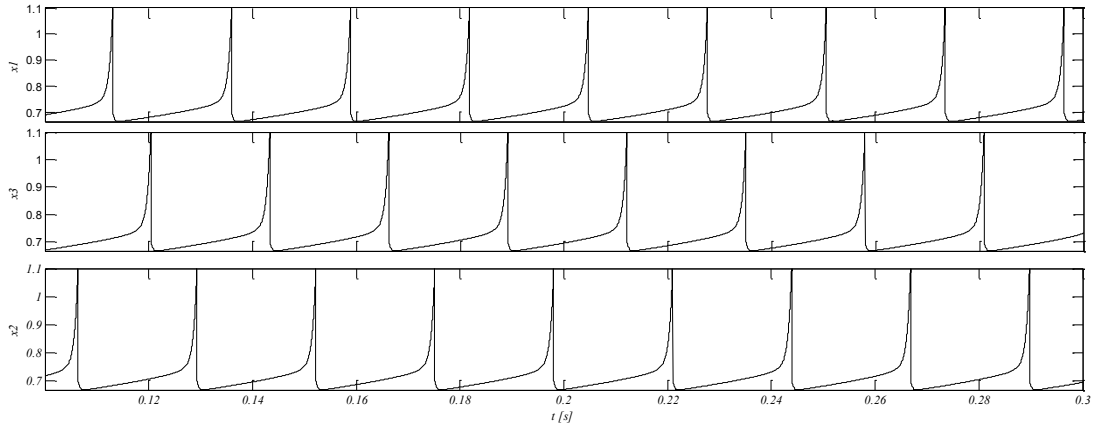
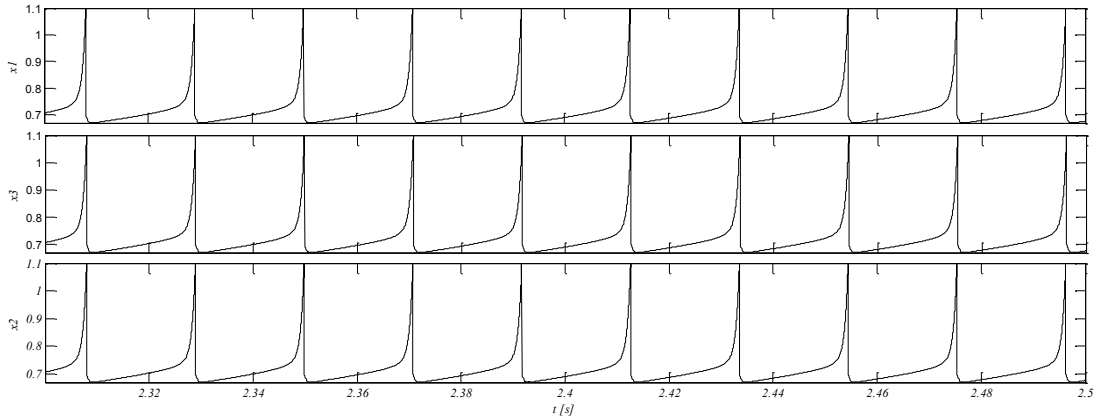


Figure 7.9 : N-phase synchronization of ring coupled network with three neurons. (a) Initial independent spiking (b) final synchronized state for $X_{1rev,N} = -0.6$, $X_{1rev,P} = 0.6$, $X_{2rev,N} = -0.6$, $X_{2rev,P} = -0.6$, $X_{3rev,N} = -0.6$ and $X_{3rev,P} = 0.6$ (c) synaptic currents at synchronized state.



(a)



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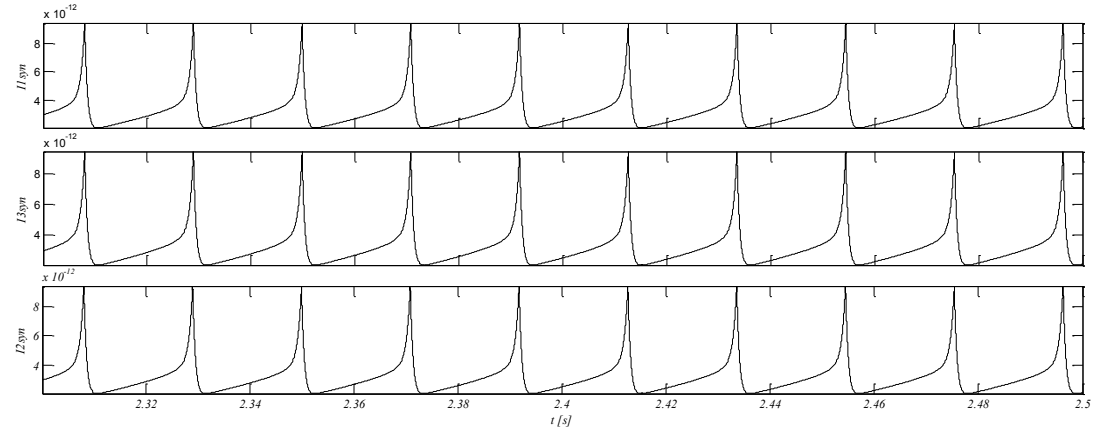
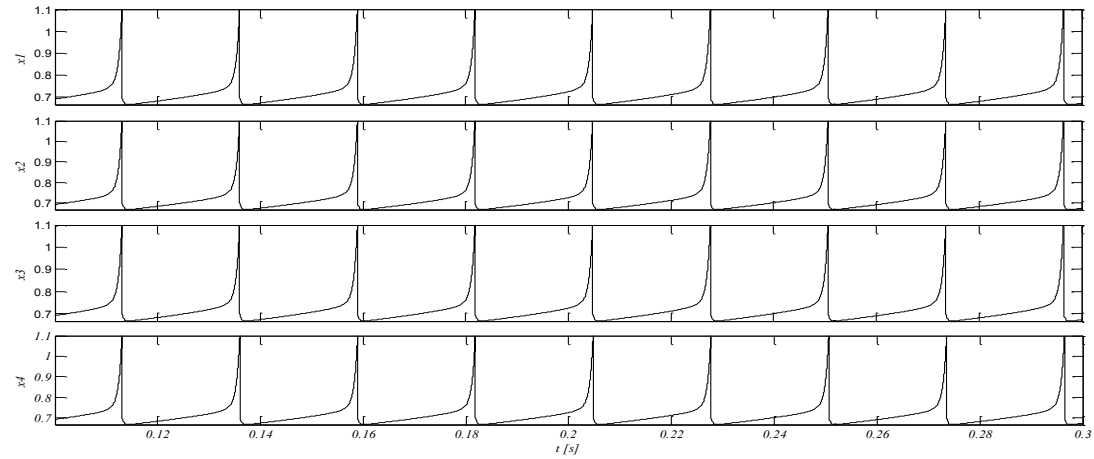


(c)

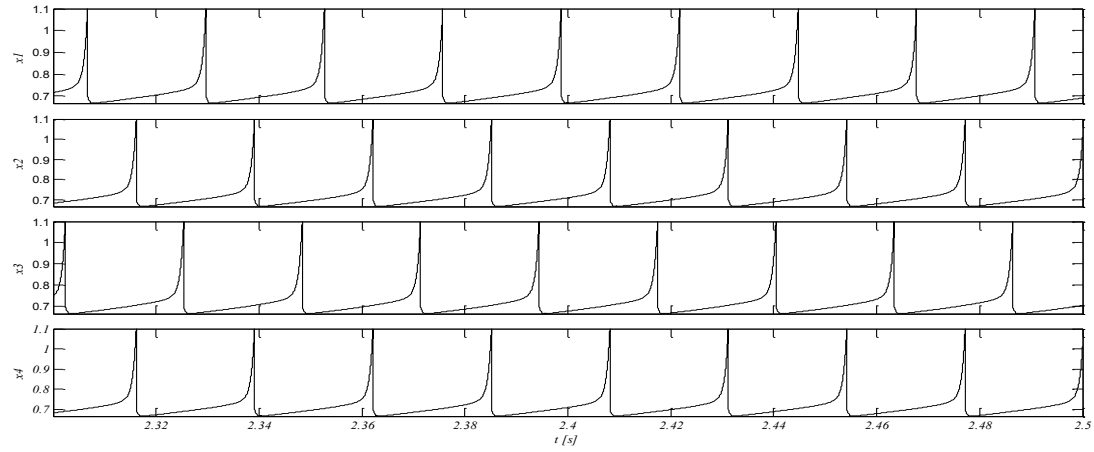
Figure 7.10 : In phase synchronization of ring coupled network with three neurons. (a) Initial independent spiking (b) final synchronized state for $X_{1rev,N} = 0.6$, $X_{1rev,P} = 0.6$, $X_{2rev,N} = 0.6$, $X_{2rev,p} = 0.6$, $X_{3rev,N} = 0.6$ and $X_{3rev,P} = 0.6$ (c) synaptic currents at synchronized state.

For inhibitory coupling it is expected to see antiphase behavior between neighboring neurons of ring structured networks involving even numbers of neurons due to the boundary conditions. This issue can be clearly seen from Figure 7.6 and Figure 7.11. However, if there are odd numbers of neurons in a ring structured network, the phase

difference cannot be exactly 180° so it is expected to see N-phase behaviour [43] as in Figure 7.9.



(a)



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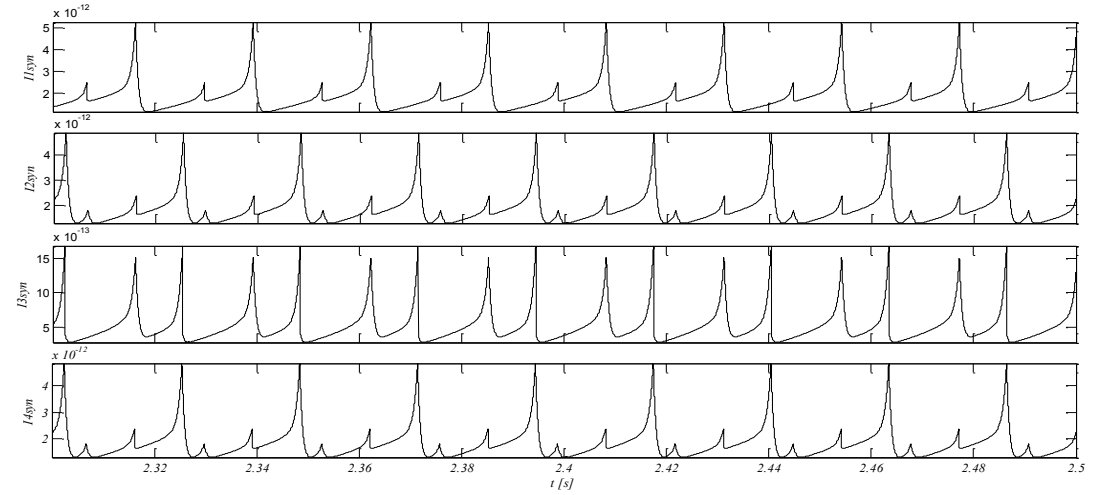
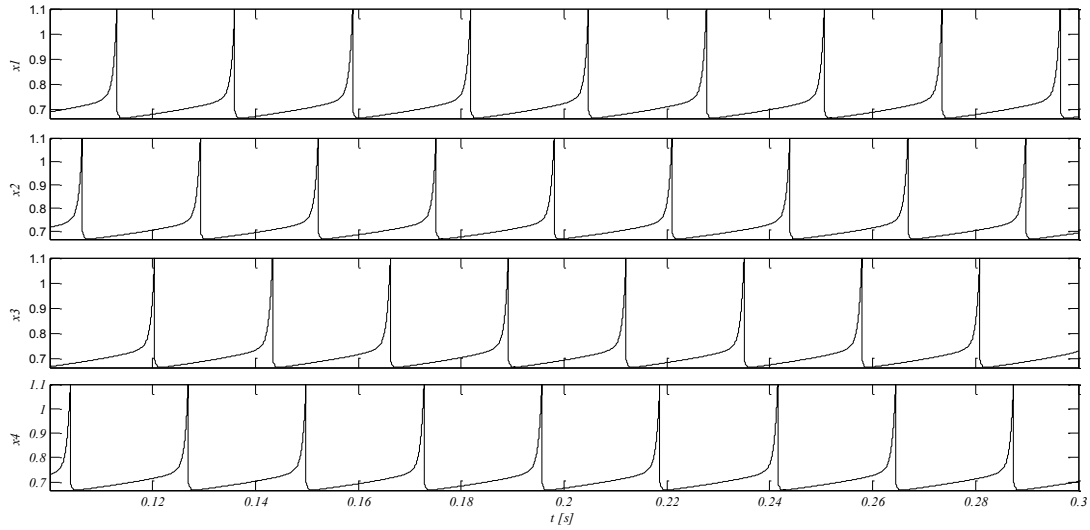
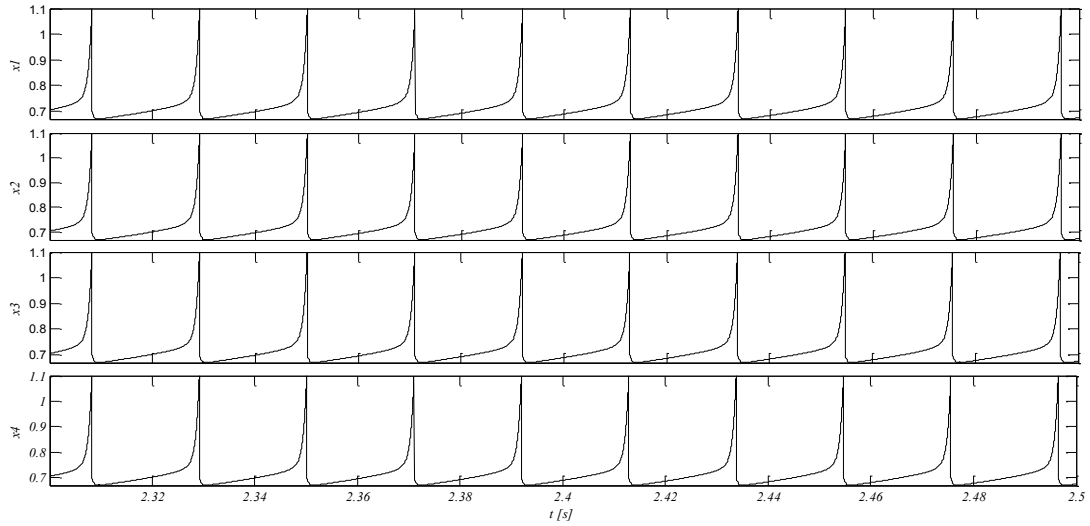


(c)

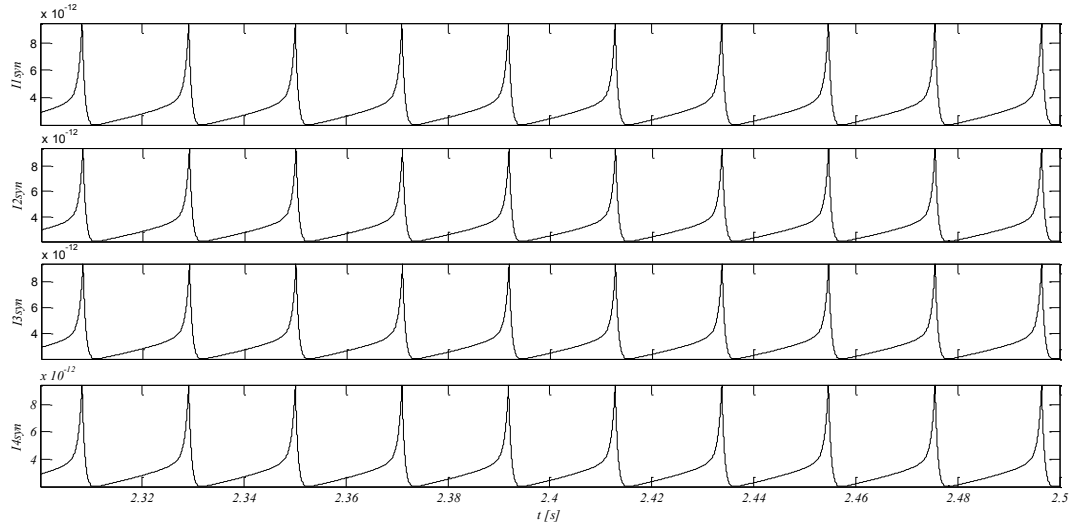
Figure 7.11 : Antiphase synchronization of ring coupled network with four neurons. (a) initial independent spiking (b) final synchronized state for $X_{1rev,N} = -0.6$, $X_{1rev,P} = 0.6$, $X_{2rev,N} = 0.6$, $X_{2rev,P} = -0.6$, $X_{3rev,N} = -0.6$, $X_{3rev,P} = -0.6$, $X_{4rev,N} = -0.6$ and $X_{4rev,P} = 0.6$ (c) synaptic currents at synchronized state.



(a)



(b)



(c)

Figure 7.12 : In phase synchronization of ring coupled network with four neurons. (a) initial independent spiking (b) final synchronized state for $X_{1rev,N} = 0.6$, $X_{1rev,P} = 0.6$, $X_{2rev,N} = 0.6$, $X_{2rev,P} = 0.6$, $X_{3rev,N} = 0.6$, $X_{3rev,P} = 0.6$, $X_{4rev,N} = 0.6$ and $X_{4rev,P} = 0.6$ (c) synaptic currents at synchronized state.

8. CIRCUIT DESIGN OF RING COUPLED NEURAL NETWORK

8.1 Circuit Design with TSMC 0.18μm Technology

We designed the circuit of two reciprocally coupled neuron and ring coupled network with 3 neurons by using TSMC 0.18μm technology. In this design, *x(t)* variable is represented with voltage while *s(t)* and *y(t)* variables are represented with current. Parameter values of synapses and neurons used in this design are explained in section 7.2. For making the model given by equation (7.2) suitable for circuit implementation, we wrote down the model equations with given numerical values and subtract $8.75*10^{-9}$ from *y(t)* and $0.8*10^{-9}$ from *s(t)* and then multiplied first state equation by 10^{-1} and second and third one by $(\alpha*10^{-12})$. After subtractions and multiplications, we made $x(t) \rightarrow v(t)$, $y(t) \rightarrow [10*i_y(t)]$ and $s(t) \rightarrow [10*i_s(t)]$ transformation and broke the final expressions into the corresponding subthreshold CMOS blocks and elements as can be seen from equation (8.1). In this equation $i_{s.P}(t)$ *and* $i_{s.N}(t)$ are instantaneous synaptic activation currents caused by previous and next neuron, respectively. Also $V_{rev,P}$ and $V_{rev,N}$ are synaptic reversal potentials described in the same manner.

Circuit block diagram of the optimized synaptic circuit and the system network consisting of two reciprocally coupled neurons are shown in Figure 8.1 and Figure 8.2, respectively. Because of weak coupling synaptic currents are so small to implement as VLSI circuit. Thus output current of the synapse circuit is not multiplied by synaptic conductance (i.e. $g = 0.015$) at the first step. Synapse circuit output current is summed with $(1/g)*I_{in} = 66*I_{in}$ then this summation is divided by 66 and injected to related neuron as it is seen at Figure 8.2. All those operations are made to shift the synapse circuit output current value in a VLSI implementable range. Sublocks of the circuits in Figure 8.1 and Figure 8.2 is explained in detail at section 6.

$$\underbrace{300*10^{-15}}_{C=300fF}\frac{dv(t)}{dt}=\left\{\begin{array}{l}\underbrace{4*100*10^{-12}*\tanh\left[\left(\frac{\underbrace{v(t)}_{\substack{voltage\\divider}}}{\underbrace{8.8}_{\substack{voltage\\divider}}}-\frac{\underbrace{0.6}_{\substack{voltage\\divider}}}{\underbrace{8.8}_{\substack{voltage\\divider}}}\right)\frac{\alpha}{2}\right]}_{\substack{output\ current\ of\ Long-tailed\ circuit\ with\\100pA\ tail\ current\ multiplied\ by\ 4\ (THB2)}}-\underbrace{3*100*10^{-12}\tanh\left[(v(t)-0.6)\frac{\alpha}{2}\right]}_{\substack{output\ current\ of\ Long-tailed\ circuit\ with\\100pA\ tail\ current\ multiplied\ by\ 3\ (THB3)}}-\underbrace{i_y(t)}_{\substack{2nd\ state\\variable}}+\underbrace{I_c}_{\substack{constatnt\ current\\source=\ 875*10^{-12}}}\\+\ 0.015\left(\underbrace{i_{s,P}(t)*\tanh\left[\left(\frac{\underbrace{v(t)}_{\substack{voltage\\divider}}}{\underbrace{8.8}_{\substack{voltage\\divider}}}-\frac{\underbrace{V_{rev,P}}_{\substack{voltage\\divider}}}{\underbrace{8.8}_{\substack{voltage\\divider}}}\right)\frac{\alpha}{2}\right]}_{\substack{output\ current\ of\ Long-tailed\ circuit\ with\\i_{s,j}(t)\ tail\ current}}+\underbrace{i_{s,N}(t)*\tanh\left[\left(\frac{\underbrace{v(t)}_{\substack{voltage\\divider}}}{\underbrace{8.8}_{\substack{voltage\\divider}}}-\frac{\underbrace{V_{rev,N}}_{\substack{voltage\\divider}}}{\underbrace{8.8}_{\substack{voltage\\divider}}}\right)\frac{\alpha}{2}\right]}_{\substack{output\ current\ of\ Long-tailed\ circuit\ with\\i_{s,j}(t)\ tail\ current}}+\underbrace{\left(\frac{I_{in}}{0.015}\right)}_{\substack{constant\ stimuli\\current\ source}}\right)\end{array}\right.$$

$$\underbrace{\alpha*23*10^{-14}}_{C=\alpha*230fF=7pF}\frac{di_y(t)}{dt}=\underbrace{\left(\alpha*\underbrace{50*10^{-12}}_{\substack{I_b\rightarrow constant\\current\ source}}\right)}_{\left(\frac{R_2R_4}{R_1R_3}\right)}\underbrace{(2)}\left[\underbrace{100*10^{-12}\tanh\left[\left(\frac{\underbrace{v(t)}_{\substack{voltage\\divider}}}{\underbrace{8.8}_{\substack{voltage\\divider}}}-\frac{\underbrace{0.6}_{\substack{voltage\\divider}}}{\underbrace{8.8}_{\substack{voltage\\divider}}}\right)\frac{\alpha}{2}\right]}_{Long-tailed\ circuit\ with\ 100pA\ tail\ current(THB1)}+\underbrace{100*10^{-12}}_{\substack{100pA\ constant\\current\ source}}\right]}_{i_{in}(t)}-\underbrace{(\alpha*\underbrace{10*10^{-12}}_{\substack{I_d\rightarrow constatnt\\current\ source}})i_y(t)}\tag{8.1}$$

$$\underbrace{\alpha*46*10^{-15}}_{C=\alpha*46fF=1.6pF}\frac{di_s(t)}{dt}=\underbrace{\left(\alpha*\underbrace{50*10^{-12}}_{\substack{I_b\rightarrow constant\\current\ source}}\right)}_{\left(\frac{R_2R_4}{R_1R_3}\right)}\underbrace{(2)}\left[\underbrace{100*10^{-12}\tanh\left[\left(\frac{\underbrace{v(t)}_{\substack{voltage\\divider}}}{\underbrace{8.8}_{\substack{voltage\\divider}}}-\frac{\underbrace{0.6}_{\substack{voltage\\divider}}}{\underbrace{8.8}_{\substack{voltage\\divider}}}\right)\frac{\alpha}{2}\right]}_{Long-tailed\ circuit\ with\ 100pA\ tail\ current(THB1)}+\underbrace{80*10^{-12}}_{\substack{100pA\ constant\\current\ source}}\right]}_{i_{in}(t)}-\underbrace{(\alpha*\underbrace{100*10^{-12}}_{\substack{I_d\rightarrow constatnt\\current\ source}})i_s(t)}$$

$$\Rightarrow C\frac{di(t)}{dt}=\left\{(\alpha I_b)\left(\frac{R_2R_4}{R_1R_3}\right)i_{in}(t)-(\alpha I_d)i(t)\right\}\log Domain\ Filter$$

$$\underbrace{v(t)>1.1\ \Rightarrow v(t)=V_R=0.70}_{voltage\ comparator\ and\ resetter}$$

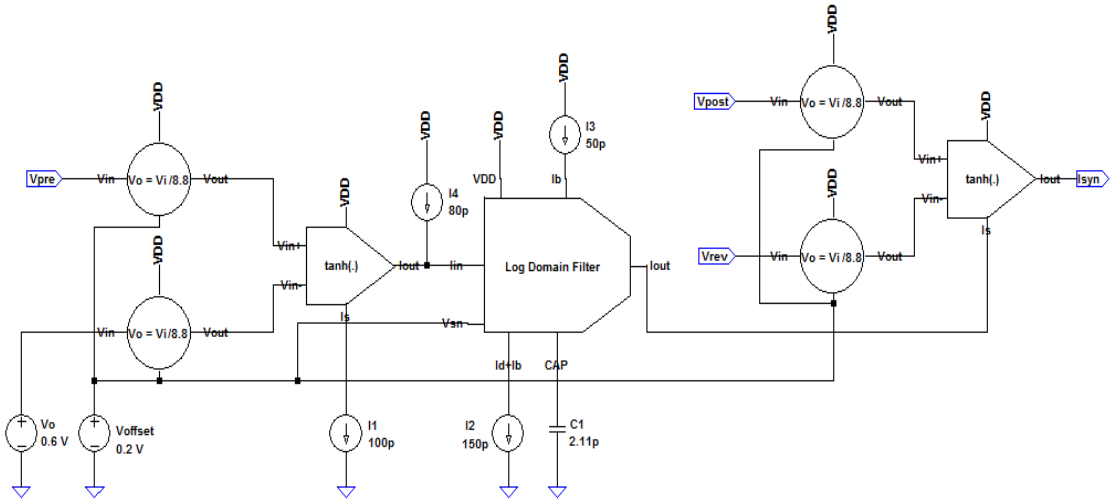


Figure 8.1 : Circuit Block Diagram of the implementes synaptic circuit.

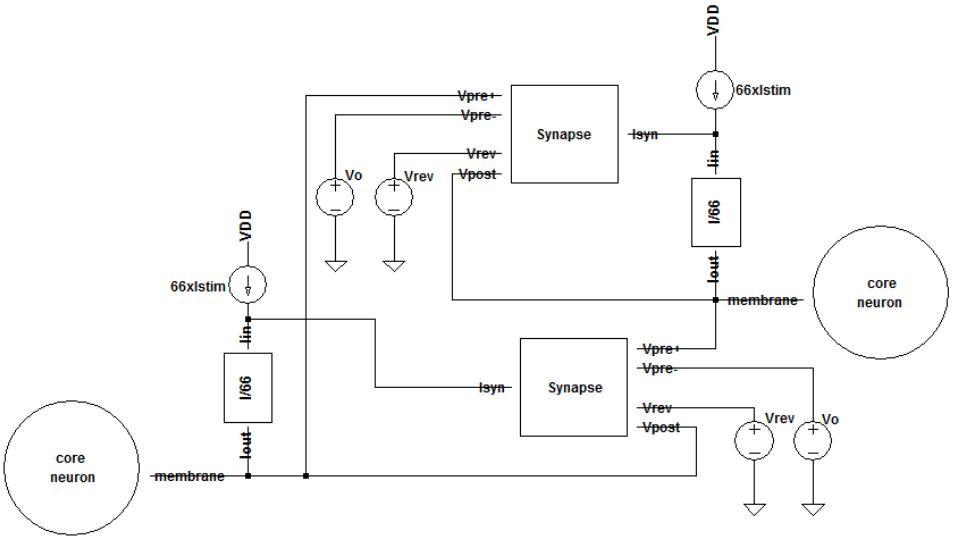
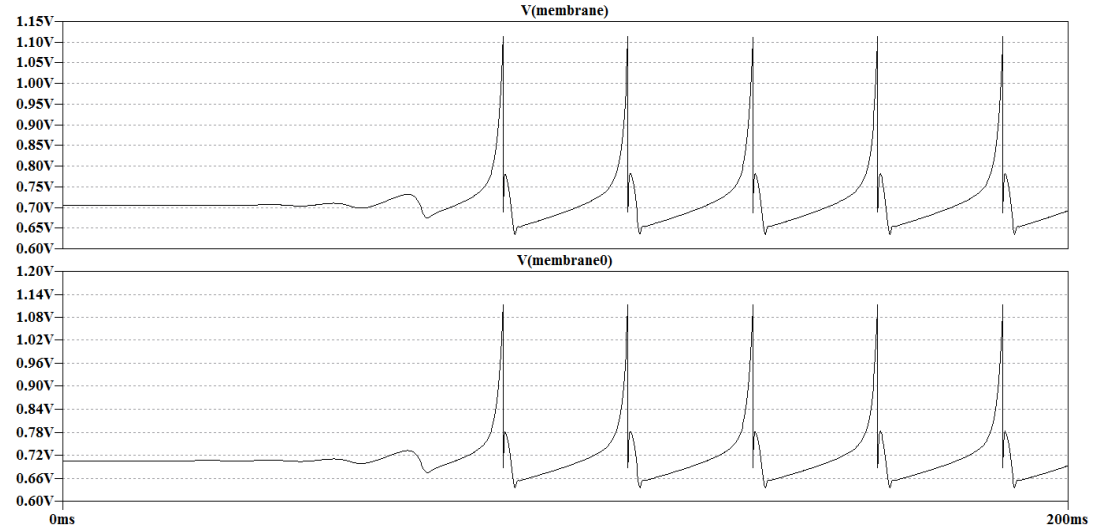


Figure 8.2 : Circuit block diagram of two reciprocally coupled neurons.

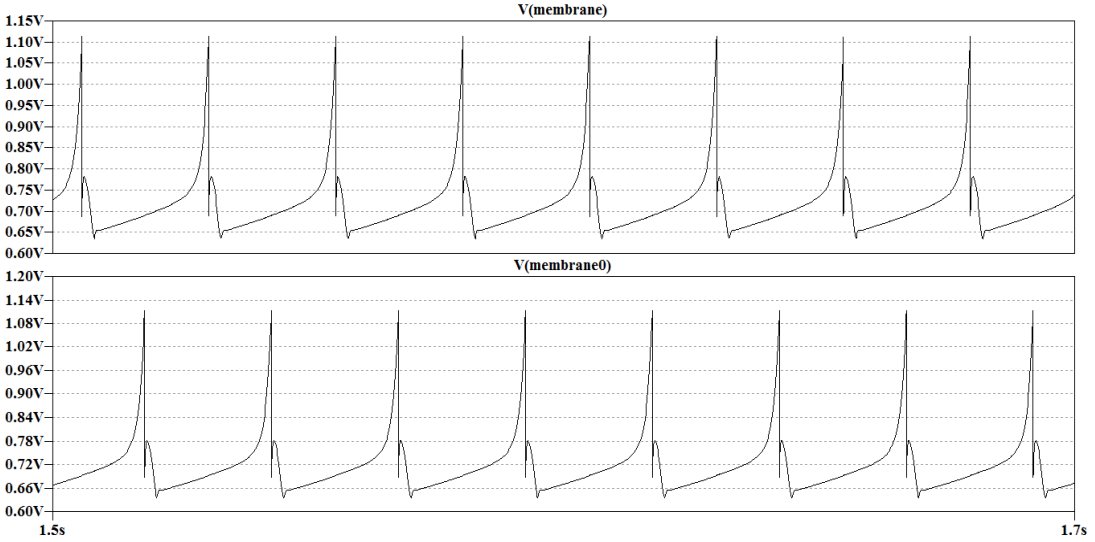
8.2 Circuit Simulation Results

From Figure 8.2 we can deduce that in two reciprocally coupled neurons network there is no previous neuron for neuron 1 and no next neuron for neuron 2 which means $i_{1s,P}(t)=0$ and $i_{2s,N}(t)=0$. Circuit Simulation results are shown in Figure 8.3 for anti phase behavior and in Figure 8.4 for in phase behavior. Note that, initially, neurons generate spikes independently throughout the *200 ms* and then the coupling is activated. Independent spiking for $t<200ms$ can be observed in Figure 8.3(a) and Figure 8.4(a). Antiphase synchronization is obtained with $V_{1rev,N} = -0.6V$ and $V_{2rev,P} = 0.6V$. In phase synchronization is obtained with $V_{1rev,N} = -0.6V$ and $V_{2rev,P} = -0.6V$. Average power consumption of the designed circuit is *282 nW*. Since this value is very close to the power consumption of a single neuron (i.e. *241 nW,* see section 6.6), we can conclude that the most of the power is consumed in the current reference circuit explained in section 6.4.

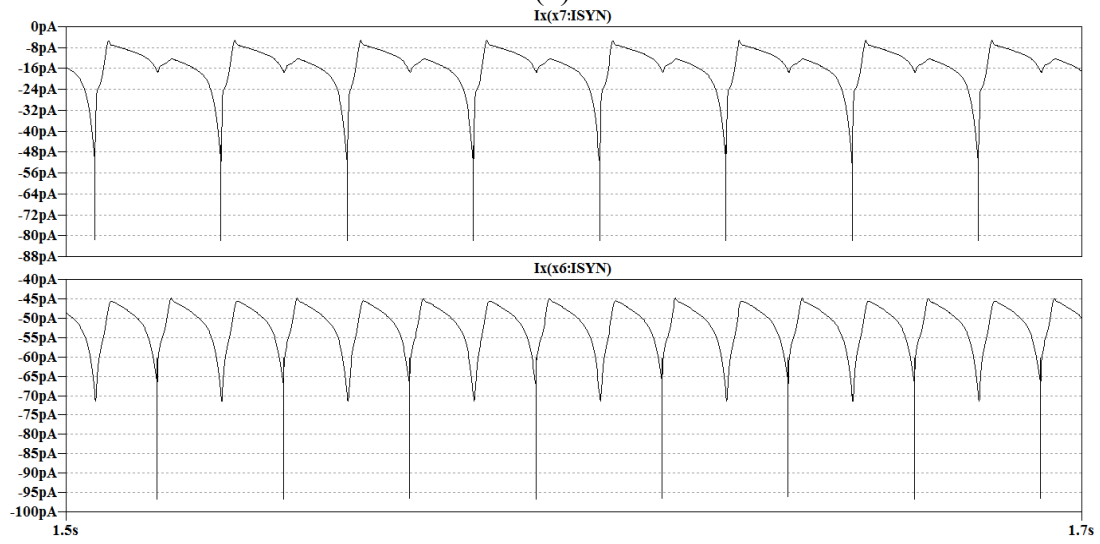
Circuit Simulation results of three ring coupled neuron are shown in Figure 8.5 for N-phase behavior and in Figure 8.6 for in phase behavior. N-phase synchronization is obtained with $V_{1rev,N}=V_{3rev,N}=0.6V$ *and* $V_{1rev,P}=V_{2rev,N}=V_{2rev,P}=V_{3rev,P}=-0.6V$. In phase synchronization is obtained with $V_{1rev,N}=V_{1rev,P}=V_{2rev,N}=V_{2rev,P}=V_{3rev,N}=V_{3rev,P}=-0.6V$. Average power consumption of the designed circuit is *320 nW*.



(a)

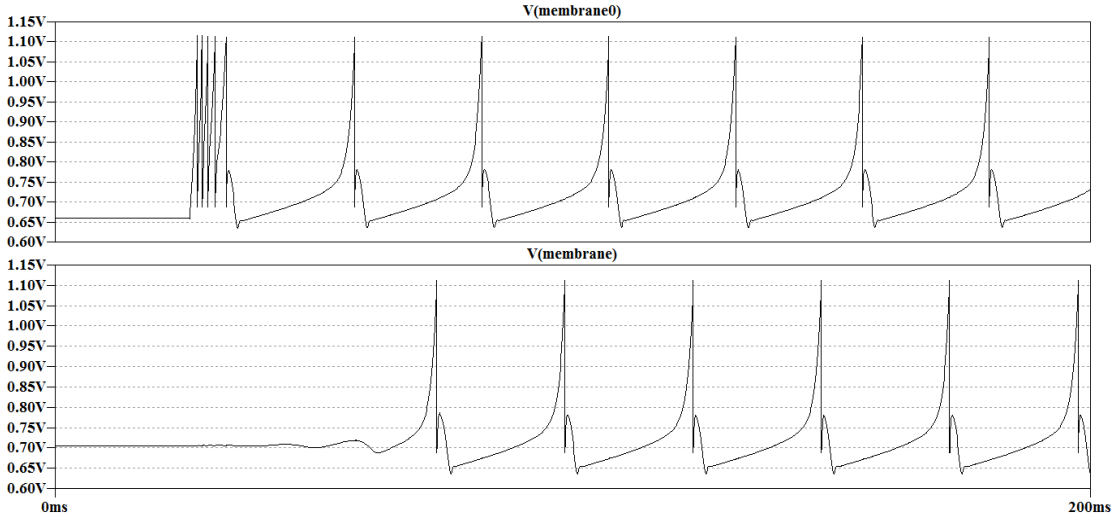


(b)

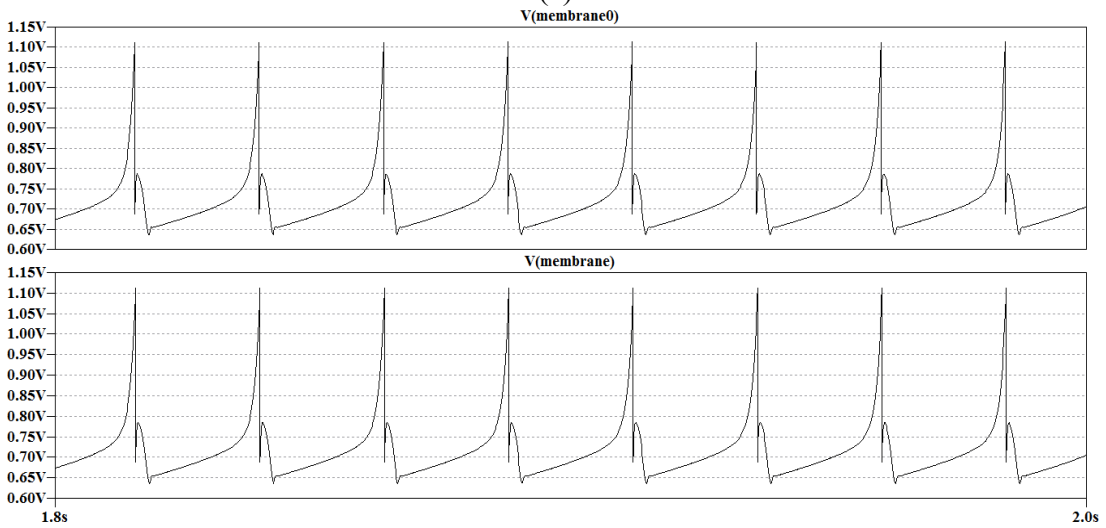


(c)

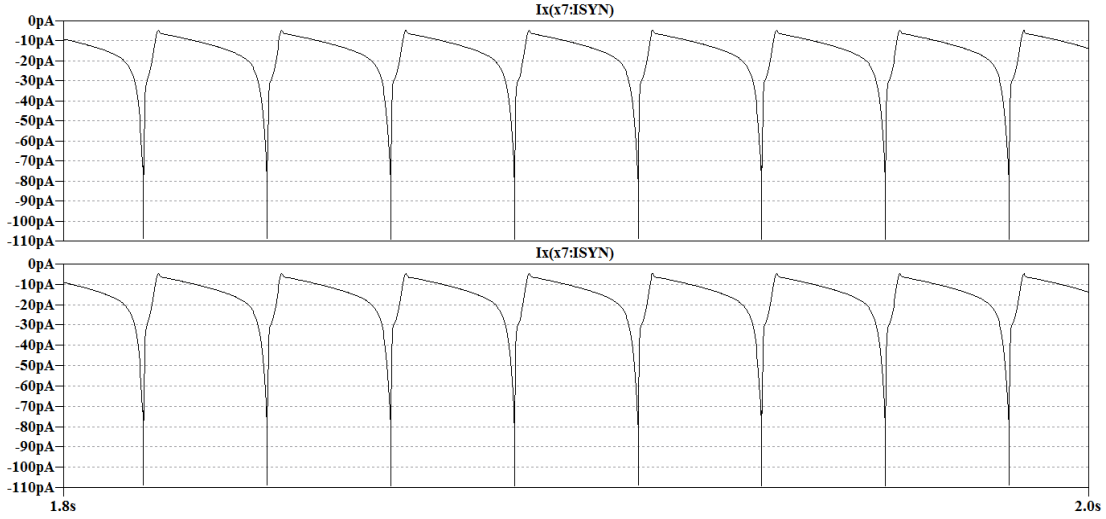
Figure 8.3 : Circuit simulation results for two reciprocally coupled neurons with antiphase synchronization (a) membrane voltages without coupling (b) membrane voltages with coupling (c) synapse current divided by 0.015.



(a)

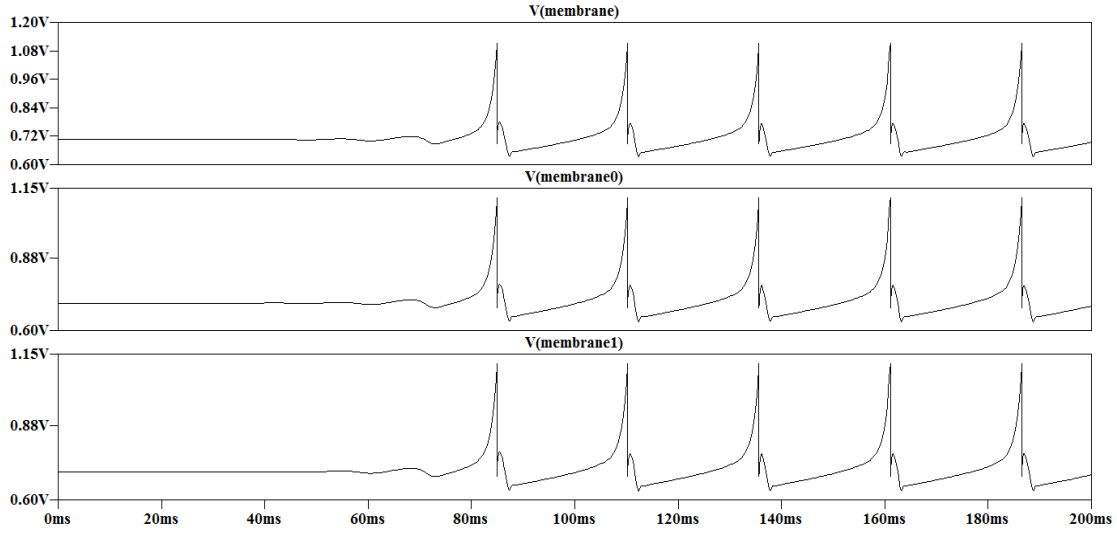


(b)

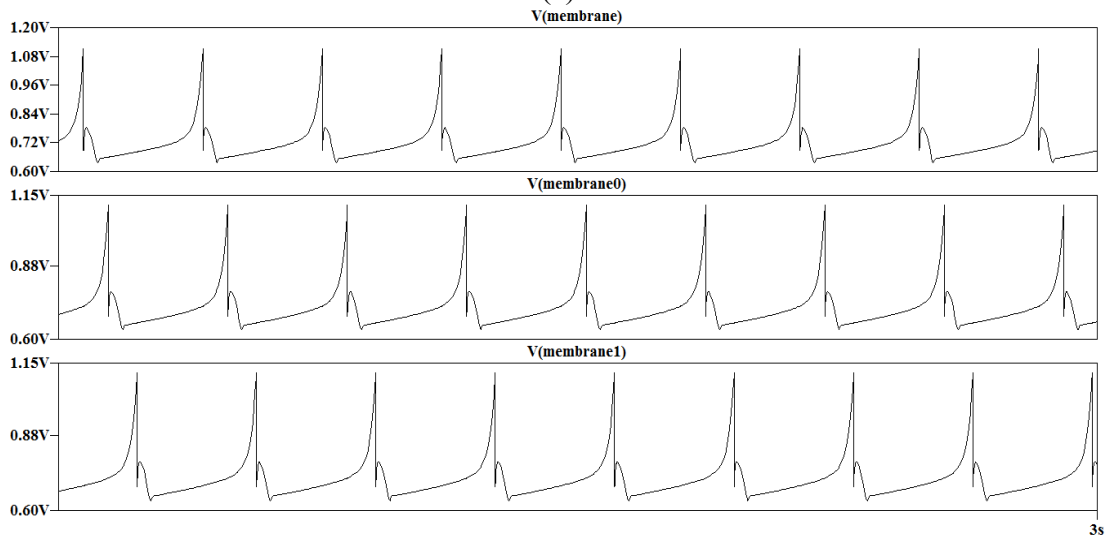


(c)

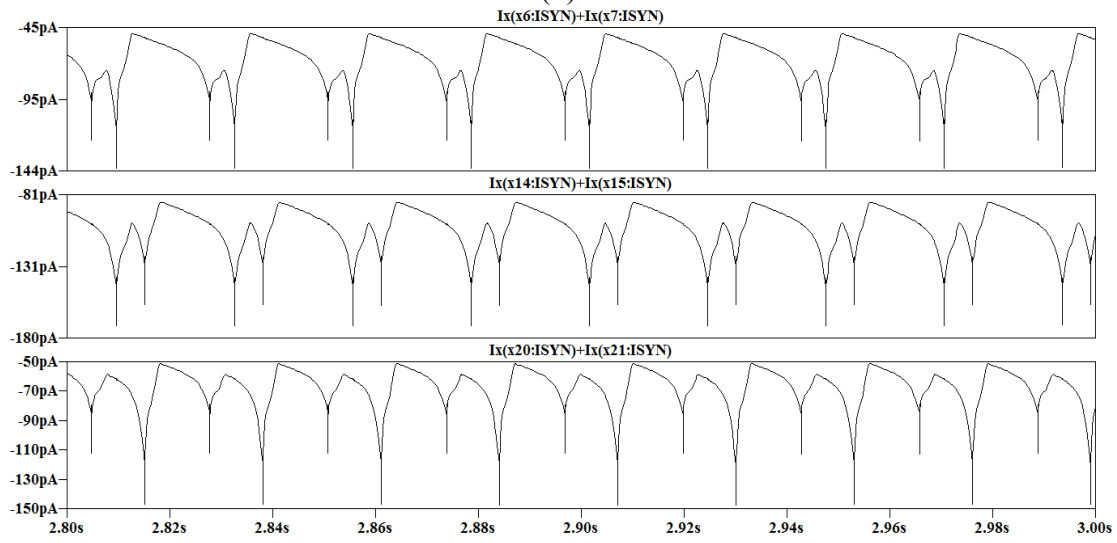
Figure 8.4 : Circuit simulation results for two reciprocally coupled neurons with in phase synchronization (a) membrane voltages without coupling (b) membrane voltages with coupling (c) synapse current divided by 0.015.



(a)

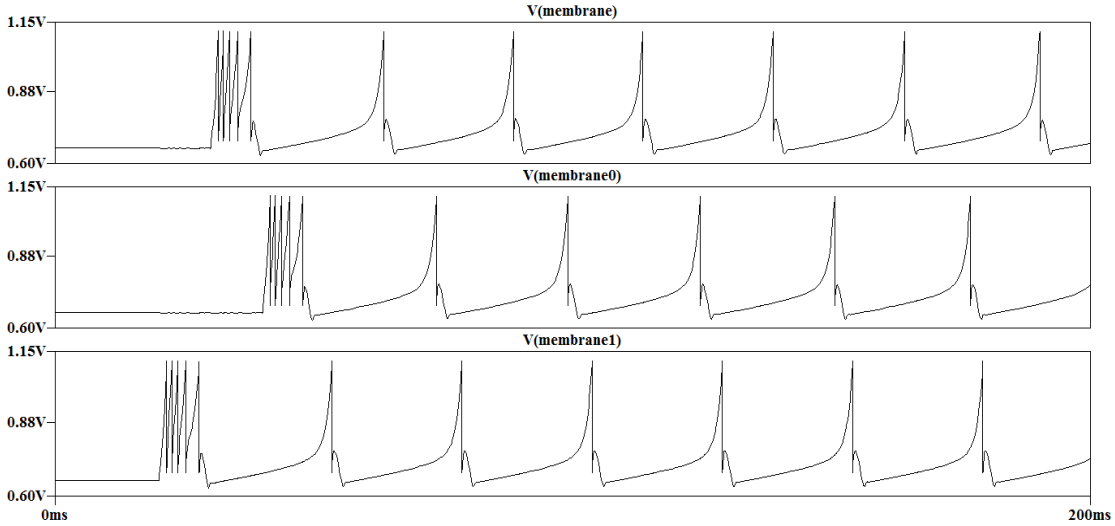


(b)

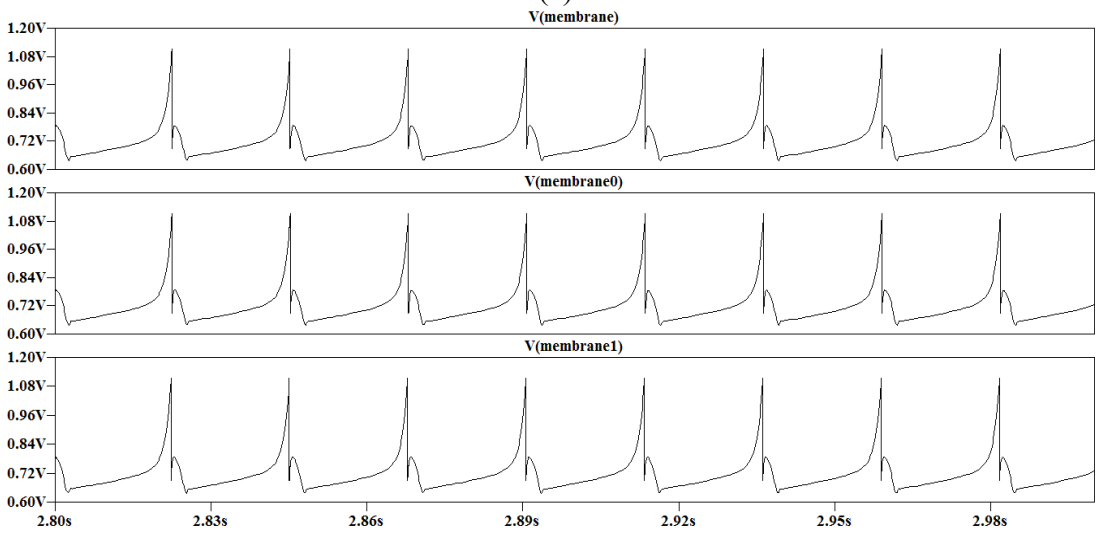


(c)

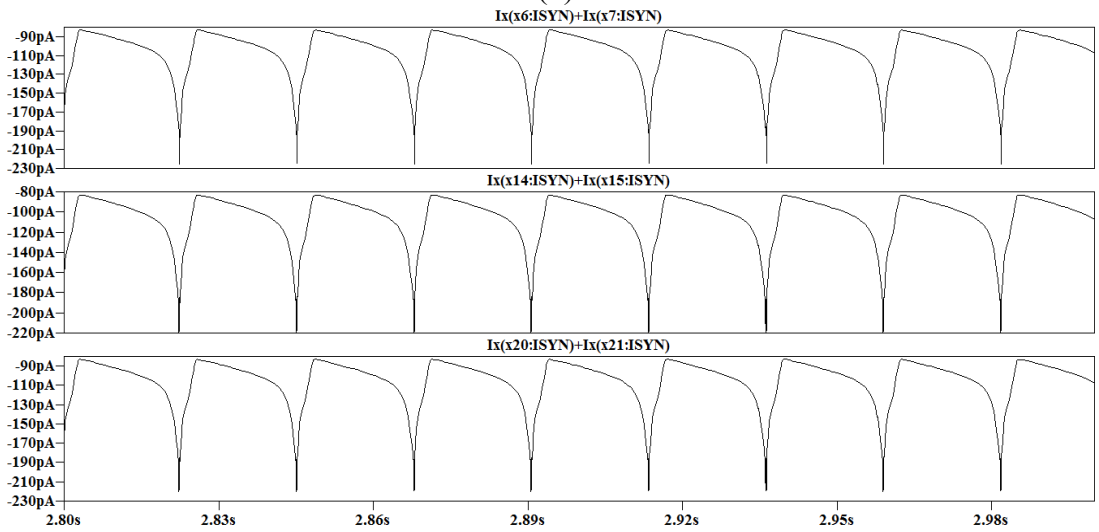
Figure 8.5 : Circuit simulation results for three ring coupled neurons with N-phase synchronization (a) membrane voltages without coupling (b) membrane voltages with coupling (c) total synapse current divided by 0.015.



(a)



(b)



(c)

Figure 8.6 : Circuit simulation results for three ring coupled neurons with in phase synchronization (a) membrane voltages without coupling (b) membrane voltages with coupling (c) total synapse current divided by 0.015.

9. CONCLUSION

In this thesis, we presented a new dynamical neuron model suitable for low power and compact VLSI implementation. This model can operate in biological time and voltage scale. When designing the model we used geometrical nullcline approach. In operational area, model has similar nullclines with $I_{Na,p}+I_K$ model resulting to equivalency in dynamic behaviour at subthreshold region. Offered model has two state variable such that one represents the membrane voltage while the other one represents the recovery variable. Also it has after spike reset mechanism as in hybrid models. Unlike Izhikevich and AdEx I&F model, only the membrane voltage is reset to a constant reset value after the spike reaches its apex. This is a big advantage of our model since implementing the hard reset of recovery variable requires large number of transistors which is a limiting factor for design of large-scale neuromorphic hardware. Recovery variable grows to the desired 'after-spike' value on its own in our model. Tangent hyperbolic characteristic of nullcline slows down the growth speed of state variable while approaching to the positive (or negative) saturation region of tangent hyperbolic. So this mechanism limits the growth speed as it will result to realistic spike timing.

Even the offered neuron model seems to have ten different parameters when it is scaled to obtain the minimum numbers of parameters it is seen that it has only four independent parameters and an input current. One can obtain nearly all of the major spiking templates of real biological neurons by only modifiying two of this parameters and input current. We developed a software application in MATLAB to examine the neuro computational features of new neuron model with numerical simulations. This application has a GUI for accepting the inputs from user and displaying the calculated outputs. By using this application we showed that the model is capable of generating the most of the spiking patterns exhibited by the known types of neocortical and thalamic neurons when the proper parameter set is selected.

New neuron model is constructed with tangent hyperbolic functions since it is odd symetric and easily implementable as VLSI circuit by using subthreshold CMOS technique. Judicious use of this technique leads to a very effective low power CMOS neuron. Implemented neuron circuit consist of a single first-order log domain filter, hyperbolic function generators, linear voltage dividers, compare & reset block and a voltage tunable current reference. In design phase we fitted the simulation results to analytic expressions by using linear least squares curve fitting method. Accuracy metric of fitting was Root Mean Squared Error (RMSE) value. We iterate the design parameters until RMSE value stays below a spesific value. We named this technique Iterative Curve Fitting Method (ICFM).

We used long tailed circuit topology with cascode output stage for implementing the tangent hyperbolic function generators (THB). For minimizing the effect of process parameters deviation we designed a core THB with minimum tail current supplied from matched 100pA current source and then multiplied the output by a constant value for obtaining the real output of different THBs.

Linear voltage divider circuit consist of two layered ladder type diode connected NMOS transistors. Dividing ratio of this block is determined as 8.8. When compared with the conventional MOS voltage dividers offered configuration has the advantage of having less number of transistors for the same divider value and of reduced body effect. We applied source shifting or offset voltage to this circuit since it operates at very low currents.

Log domain filter is a current mode circuit such that it is completely suitable for the implementation of recovery variable of our neuron model. We applied source shifting to this circuit, also.

We designed a comparator circuit which drives a discharge switch. Comparator circuit is implemented by connecting the input of two stage inverter to the output of a simple long tailed circuit that acts as differantial amplifier. Tail current of differantial amplifier should be high enough to drive output inverter stage as fast as possible. Thus we selected this current $\approx$2.3 nA. Discharge switch is implemented with big sized NMOS transistor since it should have high current sink capacity.

Process parameter deviation and temperature dependency are the two most critical problems effective on the circuit operation. Especially for the circuits based on

subthreshold operation, temperature dependency is a very common problem. Therefore, we designed wide temperature range, voltage tunable current reference circuit. Voltage tuning is necessary for minimizing the effect of process parameters deviation. We obtained the tunning voltage values that guarantees the proper operation of neuron circuit at all process corners.

Initial design and simulations are carried out with TSMC 0.18μm technology by using LTSpice design tools. Then we designed all the blocks of neuron circuit again with AMS 0.35μm SiGe-BiCMOS process by using Cadence® Virtuoso® tools for both verifying the previous design and implementing the layout of the neuron. We kept the circuit topology and transistor sizes same as in TSMC design and obtained the same results by only modifiying the value of voltage, currents sources and capacitors. We shifted the operating and supply voltages to higher values since the transistor transconductance of AMS technology is quite lower than TSMC technology. Minimum channel width to length ratio is selected as 2μm/2μm at both design for minimizing the effect of the absolute parameter deviation in sizing caused by the VLSI manufacturing process.

AMS design occupies 0.0128 mm^2 chip area. Power consumption is 277.5 nW for AMS design and 241 nW for TSMC design. Supply and offset voltages are 2.5 V and 0.5 V for AMS circuit, 1.5 V and 0.2 V for TSMC circuit, respectively. Spiking patterns obtained from circuit simulations perfectly matches with numerical results. Rich spiking dynamics are obtained by only modifying reset voltage and stimuli current.

In most of the synapse models, temporal dynamics are neglected and synapses are assumed as an instantaneous multiplier operator. A realistic model should take into consideration the spatial and temporal summation of synaptic currents. In the light of these observations, we offered a new dynamical synapse model for coupling the neurons to create realistic SNNs. This model consist of similar terms as new neuron model that makes it also suitable for compact and low power VLSI implementation. The model allows to make a synapse excitatory or inhibitory by only altering the reversal potential parameter.

Synchronized activity of neurons takes role in a wide range from cognitive functions to rhythmic movements of animals. The phase response curve (PRC), i.e. the

neurons's response to weak perturbations, is a useful tool to understand the collective dynamical properties of a neuron in a network. Therefore we extracted the PRC of new neuron with VLSI implemented parameters and show that it has Type II PRC. Based on our complete neuron and synapse models, we studied synchronization behavior of different number of reciprocally connected neurons that form a ring coupled network with excitatory and inhibitory synapses. Numerical simulations are accomplished and inphase, antiphase and N-phase synchronization behaviour for networks with 2, 3 and 4 neurons are observed.

We designed the VLSI circuit of two reciprocally coupled neuron and a ring coupled network with 3 neurons by using TSMC 0.18μm technology. Because of weak coupling synaptic currents are so small to implement as VLSI circuit. So some scaling operations are made to shift the synapse circuit output current value in a VLSI implementable range. At circuit simulations we successfully observe the expected inphase, antiphase and N-phase synchronization patterns. Power consumption is 282 nW for two reciprocally coupled neuron and 320 nW for three ring coupled neuron network.

As a future work, designed VLSI circuits can be fabricated and simulation results obtained in this work can be verified with experimental results. After that process currents and circuit area can be easily scaled down without corrupting the dynamical behavior of the circuits. This makes possible to fabricate the large networks for using as emulators for experimental scientists or real time interface circuits.

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