

**STATISTICAL DESIGN AND YIELD ENHANCEMENT OF
LOW VOLTAGE CMOS VLSI CIRCUITS**

100 753

PhD Thesis by
Tuna B. TARIM

(494D026)

100753

Date of submission: 4 November 1999

Date of defence examination: 28 December 1999

Supervisor (Chairman): Prof. Dr. H. Hakan KUNTMAN

Members of the Examining Committee Prof. Dr. Duran LEBLEBİCİ (ITU)

Assoc. Prof. Dr. Ali TOKER (ITU)

Prof. Dr. Atilla ATAMAN (YTU)

Prof. Dr. Avni MORGÜL (BU)

DECEMBER 1999

**DÜŞÜK GERİLİMLİ ANALOG VLSI DEVRELERİN
İSTATİSTİKSEL TASARIMI**

DOKTORA TEZİ
Y. Müh. Tuna B. TARIM
(494D026)

Tezin Enstitüye Verildiği Tarih: 4 Kasım 1999
Tezin Savunulduğu Tarih: 28 Aralık 1999

Tez Danışmanı: Prof. Dr. H. Hakan KUNTMAN

Diğer Jüri Üyeleri Prof. Dr. Duran LEBLEBİCİ (İTÜ)

Doç. Dr. Ali TOKER (İTÜ)

Prof. Dr. Atilla ATAMAN (YTÜ)

Prof. Dr. Avni MORGÜL (BÜ)

ARALIK 1999

PREFACE

Thanks to everybody who made this work possible.

May 1999

Tuna B. Tarım



TABLE OF CONTENTS

ABBREVIATIONS	v
LIST OF TABLES	vi
LIST OF FIGURES	ix
SUMMARY	xiii
OZET	xviii
1. INTRODUCTION	1
2. THE STATISTICAL MOS (SMOS) MODEL AND STATISTICAL DESIGN TECHNIQUES	10
2.1. The Statistical MOS (SMOS) Model	11
2.1.1. Statistical Parameter Modeling	11
2.1.2. Parameter Variance Models for MOS Device Mismatch	13
2.2. Statistical Design Techniques	16
2.2.1. Approaches for Experimental Design	17
2.2.2. Guidelines for Designing Experiments	18
2.2.3. Factorial Designs	20
2.2.4. Fractional Factorial Designs	24
2.2.5. Plackett-Burman Designs	24
2.2.6. Three-Level Fractional Factorial Designs	26
2.2.6.1. The Box-Behnken Design	27
2.2.7. The Response Surface Methodology	27
2.2.7.1 Experimental Designs for Fitting Response Surfaces	28
2.3. The Statistical VLSI Design Methodology	29
3. LOW VOLTAGE LOW POWER ANALOG VLSI CIRCUITS	33
3.1. Low Voltage and Low Power CMOS Square-Law Composite Cells	36
3.1.1. Low Voltage CMOS Square-Law Composite Cell	36
3.1.2. Low Voltage Low Power CMOS Square-Law Composite Cell	42
3.1.3. Summary of the Square-Law CMOS Cells	47
3.2. Linear Transconductors	47
3.2.1. Transconductor Using the Low Voltage CMOS Square-Law Composite Cell	48
3.2.2. Transconductor Using the Low Voltage Low Power CMOS Square-Law Composite Cell	50

3.3. Analog Multipliers	52
3.3.1. Multiplier Using the Low Voltage CMOS Square-Law Composite Cell	53
3.3.2. Multiplier Using the Low Voltage Low Power CMOS Square-Law Composite Cell	55
3.4. The Four-MOSFET Structure and a Discussion for Nonlinearity Cancellation	57
3.4.1. Four-MOSFET Structure	57
3.5. D/A Converter Based on The Current Division Technique	61
3.5.1. The 10-bit Current Division Network	62
4. STATISTICAL DESIGN AND YIELD ENHANCEMENT OF LOW VOLTAGE CMOS ANALOG VLSI CIRCUITS	66
4.1. Statistical Design of the Low Voltage and Low Power CMOS Square-Law Composite Cells	70
4.1.1. Statistical Design of the Low Voltage CMOS Square-Law Composite Cell	70
4.1.2. Statistical Design of the Low Voltage Low Power CMOS Square-Law Composite Cell	79
4.2. Statistical Design of the Low Voltage and Low Power Transconductors	84
4.2.1. Nonlinearity Measurement Method	86
4.2.2. Statistical Design of the Transconductor Using the Low Voltage CMOS Square-Law Composite Cell	87
4.2.3. Statistical Design of the Transconductor Using the Low Voltage Low Power CMOS Square-Law Composite Cell	96
4.3. Statistical Design of the Low Voltage and Low Power Multipliers	103
4.3.1. Statistical Design of the Multiplier Using the Low Voltage CMOS Square-Law Composite Cell	104
4.3.2. Statistical Design of the Multiplier Using the Low Voltage Low Power CMOS Square-Law Composite Cell	110
4.4. Summary - Statistical Design of Composite Cells, Transconductors and Multipliers	115
4.5. Statistical Design of the Four-MOSFET Structure	117
4.5.1. Statistical Simulation Results	118
4.5.2. Experimental Results	121
4.6. Statistical Design of the 10-bit Current Division Network	128
4.6.1. Statistical Simulation Results	128
4.6.2. Experimental Results	130
5. DISCUSSION AND RESULTS	133
6. CONCLUSION AND FUTURE WORK	141
REFERENCES	146
APPENDICES	153
BIOGRAPHY	176

ABBREVIATIONS

PDA : Personal Digital Assistant
MOS : Metal-Oxide-Semiconductor
CMOS : Complementary MOS
SMOS : Statistical MOS
DOE : Design of Experiments
RSM : Response Surface Methodology



LIST OF TABLES

	<u>Page number</u>
Table 2.1. Rows of plus and minus signs that are used to construct the Plackett-Burman designs for N=12 and 20	25
Table 2.2. Plackett-Burman design matrix for N=12, k=11	25
Table 3.1. W/L values of the transistors of the low voltage square-law CMOS cell. The bias current is $I_B=120\mu A$	41
Table 3.2. W/L values of the transistors of the low voltage low power square-law CMOS cell. The bias current is $I_B=120\mu A$	46
Table 4.1. Minimum and maximum area assignment for each transistor - low voltage CMOS square-law composite cell	72
Table 4.2. The Plackett-Burman design matrix and simulation results - low voltage CMOS square-law composite cell	73
Table 4.3. SS values and contribution of each transistor - low voltage CMOS square-law composite cell	74
Table 4.4. The Box-Behnken design matrix and simulation results - low voltage square-law composite cell	75
Table 4.5. Minimum and maximum area assignment for each transistor - low voltage low power CMOS square-law composite cell	80
Table 4.6. The Plackett-Burman design matrix and simulation results - low voltage low power CMOS square-law composite cell	80
Table 4.7. SS values and contribution of each transistor - low voltage low power CMOS square-law composite cell	81
Table 4.8. The Box-Behnken design matrix and simulation results - low voltage low power square-law composite cell	82
Table 4.9. Minimum and maximum area assignment for each transistor - transconductor using the low voltage CMOS square-law composite cell	89
Table 4.10. The Plackett-Burman design matrix and simulation results for offset current and nonlinearity - transconductor using the low voltage CMOS square-law composite cell	89
Table 4.11. SS values and contribution of each transistor - transconductor using the low voltage CMOS square-law composite cell	90
Table 4.12. The Box-Behnken design matrix and simulation results for offset current and nonlinearity - transconductor using the low voltage square-law composite cell	91

Table 4.13.	Minimum and maximum area assignment for each transistor - transconductor using the low voltage low power CMOS square-law composite cell	97
Table 4.14.	The Plackett-Burman design matrix and simulation results for offset current and nonlinearity - transconductor using the low voltage low power CMOS square-law composite cell	98
Table 4.15.	SS values and contribution of each transistor - transconductor using the low voltage low power CMOS square-law composite cell	98
Table 4.16.	The Box-Behnken design matrix and simulation results for offset current and nonlinearity - transconductor using the low voltage low power square-law composite cell	100
Table 4.17.	Minimum and maximum area assignment for each transistor - multiplier using the low voltage CMOS square-law composite cell	105
Table 4.18.	The Plackett-Burman design matrix and simulation results for offset current and nonlinearity - multiplier using the low voltage CMOS square-law composite cell	106
Table 4.19.	SS values and contribution of each transistor - multiplier using the low voltage CMOS square-law composite cell	106
Table 4.20.	The Box-Behnken design matrix and simulation results for offset current and nonlinearity - multiplier using the low voltage square-law composite cell	107
Table 4.21.	The Box-Behnken design matrix and simulation results for nonlinearity - multiplier using the low voltage square-law composite cell	108
Table 4.22.	Minimum and maximum area assignment for each transistor - multiplier using the low voltage low power CMOS square-law composite cell	111
Table 4.23.	The Plackett-Burman design matrix and simulation results for offset current and nonlinearity - multiplier using the low voltage low power CMOS square-law composite cell	111
Table 4.24.	SS values and contribution of each transistor - multiplier using the low voltage low power CMOS square-law composite cell	112
Table 4.25.	The Box-Behnken design matrix and simulation results for nonlinearity - multiplier using the low voltage low power square-law composite cell	113
Table 4.26.	The mean and standard deviation for the offset of the four-MOSFET structure on four tiny chips ($W/L=4/4$, $G=28\mu A/V^2$)	123
Table 4.27.	The mean and standard deviation for the offset of the four-MOSFET structure on four tiny chips ($W/L=20/4$, $G=140\mu A/V^2$)	125
Table 4.28.	The mean and standard deviation for the nonlinearity of the four-MOSFET structure on four tiny chips ($W/L=4/4$, $G=28\mu A/V^2$)	125
Table 4.29.	The mean and standard deviation for the nonlinearity of the four-MOSFET structure on four tiny chips ($W/L=4/4$, $G=140\mu A/V^2$)	126
Table 4.30.	The mean and standard deviation of the output current of the 10-bit current division network	129

Table 4.31. The standard deviation of the output current (in terms of LSB units) of the current division network for different digital words and different aspect ratios

130



LIST OF FIGURES

	<u>Page number</u>
Figure 1.1. A typical circuit cost versus yield curve	4
Figure 2.1. Separation of device variability	12
Figure 2.2. Relation between inter- and intra-die parameter standard deviations	12
Figure 2.3. The model calculation procedure for the SMOS model	15
Figure 2.4. Two-factor factorial experiments	20
Figure 2.5. Factorial experiment a) without, b) with interaction	22
Figure 2.6. The complete statistical design methodology	30
Figure 3.1. a) Single MOS transistor, b) Conventional composite transistor	37
Figure 3.2. The basic idea of a) The conventional composite transistor, b) The low voltage square-law CMOS cell	37
Figure 3.3. The idea of using a level shifter to reduce the equivalent threshold voltage	38
Figure 3.4. a) Low voltage CMOS square-law composite cell, b) Representation of the current source	38
Figure 3.5. DC transfer curve of the low voltage square-law CMOS cell	41
Figure 3.6. Constant current source at the drain of the transistor, for keeping the drain current of the transistor constant	42
Figure 3.7. The feedback loop that will keep the threshold voltage constant without having to satisfy any condition for the bias current	43
Figure 3.8. The description of the feedback loop	43
Figure 3.9. a) Low voltage low power CMOS square-law composite cell, b) Re-presentation of the current source	44
Figure 3.10. The DC transfer curve of the low voltage low power square-law CMOS cell	46
Figure 3.11. The transconductor using the low voltage CMOS square-law composite cell	48
Figure 3.12. The DC transfer curve of the transconductor using the low voltage CMOS square-law composite cell	50
Figure 3.13. The transconductor using the low voltage low power CMOS square-law composite cell	51
Figure 3.14. The DC transfer curve of the transconductor using the low voltage low power CMOS square-law composite cell	52
Figure 3.15. Multiplier using the low voltage CMOS square-law composite cell	53

Figure 3.16.	The DC transfer curve of the multiplier using the low voltage CMOS square-law composite cell	55
Figure 3.17.	Multiplier using the low voltage low power CMOS square-law composite cell	56
Figure 3.18.	The DC transfer curve of the multiplier using the low voltage low power CMOS square-law composite cell	56
Figure 3.19.	The four-MOSFET structure	58
Figure 3.20.	The DC transfer curve of the four-MOSFET structure (APLAC simulation results), for a) $W/L=4/4$, b) $W/L=20/4$	59
Figure 3.21.	The DC transfer curve of the four-MOSFET structure (experimental results) for aspect ratios $W/L=4/4$ and $W/L=20/4$	60
Figure 3.22.	The 10-bit current division network	62
Figure 3.23.	Transfer curve of the 10-bit current division network (APLAC simulation results), for the aspect ratio of $W/L=44/4$, and for digital word settings; a) $d_1=1, d_2=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$ and b) $d_2=1, d_1=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$	63
Figure 3.24.	Transfer curve for the 10-bit current division network (experimental results) for two digital word settings; $d_1=1, d_2=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0; d_2=1, d_1=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$; a) $W/L=8/4$, b) $W/L=44/4$	64
Figure 4.1.	a) Low voltage CMOS square-law composite cell, b) Representation of the current source. The circuit description is given in detail in Section 3.1	71
Figure 4.2.	Response surfaces for pairs of transistors for the low voltage CMOS square-law composite cell; a) a_{n1} vs. a_{n2} ($a_{p1}=90\mu\text{m}^2$), b) a_{n1} vs. a_{p1} ($a_{n2}=600\mu\text{m}^2$)	76
Figure 4.3.	Response surfaces for a_{n1} vs. a_{n2} ($a_{p1}=150\mu\text{m}^2$)	77
Figure 4.4.	a) Low voltage low power CMOS square-law composite cell, b) Representation of the current source. The circuit description is given in detail in Section 3.1	79
Figure 4.5.	Response surfaces for pairs of transistors for the low voltage low power CMOS square-law composite cell; a) a_{n1} vs. a_{n2} ($a_{pcm}=450\mu\text{m}^2$), b) a_{n1} vs. a_{pcm} ($a_{n2}=200\mu\text{m}^2$)	83
Figure 4.6.	Nonlinearity measurement method	86
Figure 4.7.	The transconductor using the low voltage CMOS square-law composite cell. The circuit description is given in detail in Section 3.2	88
Figure 4.8.	Response surfaces for the offset current of the transconductor using the low voltage CMOS square-law composite cell; a) a_{n1} vs. a_{pcm} ($a_{p1}=30\mu\text{m}^2$), b) a_{n1} vs. a_{p1} ($a_{pcm}=450\mu\text{m}^2$), and c) a_{pcm} vs. a_{p1} ($a_{n1}=10\mu\text{m}^2$)	93

Figure 4.9.	Response surfaces for the nonlinearity of the transconductor using the low voltage CMOS square-law composite cell; a) a_{n1} vs. a_{pcm} ($a_{p1}=30\mu\text{m}^2$), b) a_{n1} vs. a_{p1} ($a_{pcm}=450\mu\text{m}^2$), and c) a_{pcm} vs. a_{p1} ($a_{n1}=10\mu\text{m}^2$)	94
Figure 4.10.	The transconductor using the low voltage low power CMOS square-law composite cell. The circuit description is given in detail in Section 3.2	96
Figure 4.11.	Response surfaces for the offset current of the transconductor using the low voltage low power CMOS square-law composite cell; a) a_{n1} vs. a_{pcm} ($a_{p1}=30\mu\text{m}^2$), b) a_{n1} vs. a_{p1} ($a_{pcm}=450\mu\text{m}^2$), and c) a_{pcm} vs. a_{p1} ($a_{n1}=10\mu\text{m}^2$)	101
Figure 4.12.	Response surfaces for the nonlinearity of the transconductor using the low voltage low power CMOS square-law composite cell; a) a_{n1} vs. a_{pcm} ($a_{p1}=30\mu\text{m}^2$), b) a_{n1} vs. a_{p1} ($a_{pcm}=450\mu\text{m}^2$), and c) a_{pcm} vs. a_{p1} ($a_{n1}=10\mu\text{m}^2$)	102
Figure 4.13.	The multiplier using the low voltage CMOS square-law composite cell. The circuit description is given in detail in Section 3.3	104
Figure 4.14.	Response surfaces for the nonlinearity of the multiplier using the low voltage CMOS square-law composite cell; a) a_{n1} vs. a_{n2} ($a_{p1}=30\mu\text{m}^2$), b) a_{n1} vs. a_{p1} ($a_{pcm}=200\mu\text{m}^2$)	109
Figure 4.15.	Response surfaces for the nonlinearity of the multiplier using the low voltage CMOS square-law composite cell; a_{n2} vs. a_{pcm}	109
Figure 4.16.	The multiplier using the low voltage low power CMOS square-law composite cell. The circuit description is given in detail in Section 3.3	110
Figure 4.17.	Response surfaces for the nonlinearity of the multiplier using the low voltage low power CMOS square-law composite cell; a_{n2} vs. a_{pcm}	114
Figure 4.18.	The four-MOSFET structure. The description of the circuit is given in Section 3.4	117
Figure 4.19.	Statistical simulation results for the standard deviation of offset vs. channel width. Each contour represents different values of channel lengths	119
Figure 4.20.	Statistical simulation results for the standard deviation of nonlinearity vs. channel width. Each contour represents different values of channel lengths	120
Figure 4.21.	Experimental results for the offset of the four-MOSFET structure ($W/L=4/4$). The results in each item shows the normal distribution for four different tiny chips	122
Figure 4.22.	Experimental results for the offset of the four-MOSFET structure ($W/L=20/4$). The results in each item shows the normal distribution for four different tiny chips	124

Figure 4.23.	Die-photo of the chip of the four-MOSFET structure	127
Figure 4.24.	The 10-bit current division network. The description of the circuit is given in Section 3.5	128
Figure 4.25.	Die-photo of the chip of the 10-bit current division network	132



STATISTICAL DESIGN AND YIELD ENHANCEMENT OF LOW VOLTAGE CMOS VLSI CIRCUITS

SUMMARY

Scaling down transistor sizes has led to low supply voltages (3V and less). Reducing the supply voltage does not require drastic changes in the design of digital circuits, though, this is not the case for analog circuits. In analog circuits gain, signal-to-noise ratio, bandwidth and many other performances are sensitive to the power supply voltage, and are also design specifications. Thus, low voltage analog circuit design with the emphasis of low power consumption is a major challenge for analog circuit designers.

The development of analog circuits requires both a complete understanding of basic circuit design techniques and a knowledge of transistor nonideality effects on circuit performances. One severe effect comes from the device imperfections and variances of the fabrication process. Such variations can ultimately be a limiting factor on how low the supply voltage and how reliable sub-micron designs could be. It is necessary to have a model that includes the random variations of the fabrication process. The statistical MOS (SMOS) model has been developed and incorporated into simulation programs to achieve this purpose. As transistor minimum feature sizes are in the sub-micron ranges and power supply voltages are reduced, the effect of the fluctuations of the fabrication process becomes more important. These effects surface when the chips are fabricated and the measurement results are taken. These fluctuations in many cases reduce the functional yield of the circuit, thus, increase the cost. However, if the random variations are included in the simulation environment, it is possible to estimate the effect of these variations in advance. The SMOS model is used to estimate these variations.

Another important factor in VLSI chip design is the functional yield. The functional yield of the chip is the percentage of the total number of circuit samples which have an acceptable circuit performance determined by the chip specifications, over the total number of circuit samples. The target is to have as high a functional yield as possible. Due to inherent fluctuations in any integrated circuit manufacturing process, the functional yield is always less than 100%. As the complexity of the VLSI chips increase, and the dimensions of VLSI devices decrease, the sensitivity of performance to process fluctuations increases, thus, further reducing the functional yield. Moreover, with current trends of higher level of integration leading to complete mixed signal systems on a chip, yield loss due to the analog component must be minimized such that it has little effect on the yield of the mixed signal chip.

This study demonstrates the critical need to perform statistical design and optimization in order to enhance both the functional yield and reliability of low voltage, low power analog VLSI circuits. Statistical techniques have been used to determine the quantitative effect of different transistor sizes on the performance variations. It is possible to evaluate these variations to obtain the functional yield information. The purpose is to keep the functional yield of the circuit as high as possible, by the appropriate sizing of transistors. In case this robust design methodology is not used, the variation in the circuit performances becomes higher.

In some cases, industry requires an initial yield target; then statistical modeling and design are done to achieve this target. In other cases providing flexibility to designers is the main purpose and to achieve this target the standard deviation of the circuit performance is used to evaluate the functional yield.

In this thesis, the statistical MOS (SMOS) is used together with the statistical techniques. The SMOS model is used to include the fluctuations of the fabrication process into the simulation environment, and the statistical techniques are used to determine the most significant transistors in the circuit and the effect of the significant transistors on the circuit performance. The circuit is represented by an empirical model and the variables of the model are the significant transistors. The performance variation is the output of the empirical model.

The design principal of MOS circuits depends on the perfect matching of transistors, whereas in reality mismatch between transistors exists and affects the circuit performances. The reason of mismatch could be the fluctuations in the fabrication process and the difference between the same parameters of different transistors in a circuit. The SMOS model takes this effect under consideration. The core of the SMOS model is Pelgrom's equation which gives the variance of the parameter mismatch:

$$\sigma^2(P) = \frac{a_p}{WL} + s_p^2 D^2$$

a_p and s_p , in the above equation are process dependent fitting constants, D is the distance between transistors, W and L are the channel width and length, respectively, and $\sigma(P)$ is the standard deviation of parameter P . This equation takes into account two important effects that can be observed in a circuit: The size of the transistors and the placement of the transistors in the layout. Examining the equation shows that, if the area of the transistor is large and the distance between the transistors is small, the standard deviation will be low, and on the contrary, if the area of the transistor is small and the distance between the transistors is large, the standard deviation will be large.

The statistical techniques which are used together with the SMOS model are well known and widely used techniques: "Design of Experiments" (DOE) and "Response Surface Methodology" (RSM). The relationship between the input variables of the circuit and the output performance is represented by an empirical model with the help of DOE. Then RSM is used to view the empirical model with a graphical representation. It is also

possible to obtain the reliability of each term in the empirical model and hence the overall empirical model.

For circuits which have more than two input variables, DOE is applied in two steps. The first step is a two level screening experiment. First, the minimum and maximum of each component in the circuit is determined, thus, the empirical model will be valid in between these minimum and maximum values. The Plackett-Burman screening experiment is selected as the first step due to its efficient number of runs. The most contributing components in the circuit are determined with this step and only these components will be examined in the second step. The second step is a three level model building experiment.

The size of the components, in the second step, are evaluated in their minimum, maximum and their center values. The Box-Behnken experiment is used in the second step.

The results of the second step are evaluated with the help of RSM, and contour curves for a certain range of input variables are obtained. Each of these contours represent a different standard deviation value. RSM views the results in a graphical representation. The x and y axis of these graphs are the sizes of the transistors. It is possible to obtain the standard deviation for different sizes of transistors with the help of these graphs. If the designer has a target output performance and yield, it is possible to determine the minimum transistor sizes that will achieve these targets.

In this thesis the operation principles of eight circuits are given first. Then the statistical design of these circuits are explained in detail. These circuits are two low voltage and low power CMOS square-law analog composite cells, two transconductors and multipliers which use the low voltage and low power composite cells as a main building block, the four-MOSFET structure, and the 10-bit current division network, which are critical blocks in determining the overall performance of the designs they are used in.

The two low voltage and low power CMOS square-law composite cells represent a single MOS transistor. The circuits are statistically examined for their drain current mismatch. Any current mismatch will cause variations in the performance of the overall circuits which use these cells as a main building block.

Two new transconductors and multipliers were designed using the composite cells as a main building block.

The above six circuits were also discussed for achieving the concept of analog programmability. Analog programmability, in other words, using simple analog blocks to build more complex circuits is an ongoing discussion, and the ultimate goal in the analog CAD research area. The idea was discussed in this thesis, by building the transconductors and multipliers using the composite cells as main building blocks. Since effort is put when designing the cells with optimum transistor sizing, no effort is needed when designing the new transconductors and multipliers that will use the composite cells. The transconductor and multipliers are not the best ever circuits, but will definitely be suitable for certain specifications. The circuits may have more transistors than other

transconductor or multiplier circuits, but the advantage is that there was almost no design time required, since the cells were already optimized.

The transconductor and multiplier circuits were statistically examined for their offset and nonlinearity performances. The nominal simulation results gave a zero offset current and a very low nonlinearity, whereas statistical simulation results proved that the offset current can be in the micro amper ranges, and nonlinearity can be higher than the nominal result. This will have a negative effect on the circuit performance.

The four-MOSFET structure was fabricated using the MOSIS 2 μ m process. It was demonstrated that a four-MOSFET structure fully suppresses the even and odd-order nonlinearity terms; however, recent works question the widely accepted nonlinearity cancellation properties of the four-MOSFET structure. The result of the discussion is important because the supposed linearity properties of the four-MOSFET structure is served to justify its use in several recent applications. For exact cancellation of nonlinearities, exact transistor matching is needed, whereas, random variations may not always allow for exact matching of transistors. The circuit performances that are to be examined for the four-MOSFET structure are the offset and nonlinearity, as in the transconductor and multiplier circuits. Simulation and experimental results are in good agreement with each other.

The last circuit that is examined in the thesis is the 10-bit current division network, and is also fabricated using the MOSIS 2 μ m process. The operation of the circuit depends on the perfect matching of transistors; a slight mismatch will effect the resolution of the D/A converter. The performance under consideration is the output current. Generally the error is calculated in terms of the least significant bit (LSB) and the error should be less than 1 LSB. Simulation and experimental results are in good agreement with each other.

The above eight circuits are statistically examined using the SMOS model and the statistical techniques.

The first chapter is the introduction; the motivation of this work and the previous work in this field is explained. The second chapter describes the SMOS model and the statistical techniques. The statistical design methodology is given in detail. The operation principle of eight circuits are given in chapter 3, and the statistical design of these circuits are given in chapter 4. Chapter 5 and chapter 6 give the discussion and conclusion, respectively.

It is obvious from the results that as the transistor sizes are reduced the deviation in the circuit performances are increasing. This is also seen in Pelgrom's equation. It is possible to evaluate the graphical results of this thesis in different aspects: If there is a specific value that is preferred for each transistor, it is possible to find those values from the x and y axis, and find the intersection point. The value of the surface which crosses that intersection point gives the standard deviation value of the current mismatch. If there is a certain current mismatch that is preferred, e.g., according to the design specifications, the circuit cannot tolerate more than a certain value of current mismatch, it is possible to find the surface that corresponds to that value. Then, the areas that intersect on that surface will be the solution. Obviously, there will be more than one solution; this brings the preferred flexibility of selecting the suitable values for different designs.

One final word in this discussion is that, all computer aided methodologies or tools are user dependent. The statistical design methodology that is introduced in this thesis gives good results that agree with statistical simulation results. The goal is to reduce the standard deviation of the mismatch, however, the sizing of the transistors that correspond to the lowest standard deviation does not necessarily have to be the best values. All decisions are made by the designer to get the best performance out of the circuit.

The experimental results prove the accuracy and validity of the statistical techniques that are used in the statistical design methodology. The purpose of using these techniques is to estimate the effect of random process variations on the circuit performances, without having to fabricate the circuits.

The above made discussion leads to the important conclusion, that is considering statistical analysis as a standard step in circuit design. The importance is obvious for the circuits of this work, it will have an important impact on the results of other analog circuits as well. It is indeed possible to use the statistical analysis methodology that is used throughout this thesis as a standard VLSI design step, which will take into account the randomness of the fabrication process.



DÜŞÜK GERİLİMLİ ANALOG VLSI DEVRELERİN İSTATİSTİKSEL TASARIMI

ÖZET

Yarıiletken tümdevrelerdeki eleman sayısı artışına paralel olarak düşük besleme gerilimine duyulan ihtiyaç da artmaktadır. Sayısal devrelerin tasarımı yüksek besleme gerilimi değerlerinden düşük besleme gerilimi değerlerine geçildiğinde (3V ve daha düşük) çok büyük farklar göstermezken, bu geçiş analog devrelerin tasarımında farklı tasarım teknikleri gerektirmektedir. Analog devrelerdeki kazanç, gürültü/işaret oranı, bant genişliği gibi pekçok büyüklük gerilime karşı duyarlıdır ve tasarımda doğrudan etkilidir. Bu durum analog devre tasarımcılarını, düşük besleme gerilimli analog devreler için yeni tasarım teknikleri bulmaya yönlendirmiştir.

İyi bir analog devre tasarımı için, temel tasarım tekniklerinin ve ideal olmayan olayların devre performansı üzerindeki etkilerinin bilinmesi faydalıdır. Devre performansını ciddi olarak etkileyen faktörlerden birisi fabrikasyon sırasındaki rastgele olayların tasarım üzerindeki etkileridir. Bu etkiler devrenin besleme gerilimini ve tasarımın güvenilirliğini kolaylıkla sınırlayabilir. MOS tümdevrelerin yüksek güvenilirlikle üretimini sağlamak için bu rastgele etkilerin devre karakteristikleri ve dolayısıyla devre performansı üzerindeki etkisini içerecek bir modele ihtiyaç vardır. İstatistiksel MOS (statistical MOS - SMOS) modeli bu amaçla geliştirilerek çeşitli simülasyon programlarının yapısına eklenmiş, analog devrelerin performansını modellemek üzere devre tasarımcılarının kullanımına sunulmuştur. Transistör boyutları mikronaltı seviyelere ulaştıkça ve besleme gerilimleri azaldıkça, fabrikasyon sırasındaki işlemlerin devre performansını etkileme olasılığı da artmaktadır. Bu etkiler çoğu zaman kırmık fabrikasyona yollanıp test etmek amacıyla geri yollandığında anlaşılmaktadır. Bu etkiler kimi durumda kırmığın verimini büyük ölçüde düşürebilmekte ve yeniden üretimi gerektirebilmektedir. Bunun ise mali açıdan ne derecede bir külfet olduğu açıktır. Rastgele olaylar devrenin tasarımı sırasında simülasyon ortamına dahil edildiği takdirde, bu etkilerin devre performansı üzerindeki etkisini kestirmek mümkün olabilir. SMOS modeli bu amaçla kullanılmaktadır.

VLSI kırmıkların üretiminde bir başka önemli faktör kırmık üzerinde istenilen performansı gösteren devrelerin kırmık üzerindeki toplam devre sayısına oranıdır. Kırmık üzerinde istenilen performansta çalışan devrelerin sayısı ne kadar yüksek olursa tasarım o kadar başarılı olmuş demektir (kırmığın verimi). Proses sırasında doğal olarak oluşan rastgele olaylardan dolayı kırmığın verimi her zaman %100'den düşüktür. VLSI kırmıklar üzerindeki eleman sayısı arttıkça ve elemanların boyutları küçüldükçe,

kırmık üzerindeki devrelerin performansı proses sırasındaki rastgele olaylara daha duyarlı hale gelmektedir. Bunun yanında, günümüz teknolojisinde analog ve sayısal devreler aynı kırmık üzerinde tasarlanma eğilimindedir ve kırmığın verimi, üzerindeki analog devrelerin verimine bağımlı hale gelmektedir; bu durumda analog devrelerin verimini arttırmak ve devrelerin rastgele proses olaylarına duyarlılığını azaltmak daha da önemli olmaktadır.

Bu çalışma, istatistiksel tasarım ve optimizasyonun kırmık verimini ve düşük güç ve düşük gerilimli devrelerin tasarımdaki güvenilirliğini arttırmak üzere kullanılabileceğini göstermek üzere yapılmıştır. Birtakım istatistiksel teknikler kullanılarak, devre üzerindeki tranzistörlerin boyutları değiştirildiğinde devre performansındaki sapmanın ne kadar olacağı belirlenmekte ve bu sapma değerlerinden yola çıkarak kırmık üzerindeki verimin olabildiğince yüksek tutulmasına çalışılmaktadır. Optimize edilmeyen devrelerin performanslarındaki dağılım da yüksek olmaktadır. Dağılımın normal dağılım olduğu kabul edilirse, bu normal dağılımın altındaki alandan yola çıkarak verimi belirlemek mümkün olabilmektedir. Optimizasyon sonrasındaki dağılım yine bir normal dağılımdır, ancak bu kez, devre optimize edildiği için büyük miktarda bir sapma görülmemektedir. Bu durumda aynı verimi daha sıkı bir aralıkta elde etmek ve dolayısıyla verimi arttırmak mümkün olmaktadır.

Endüstriyel çalışmalarda, kırmık veriminin ne olacağı baştan belirlenmekte, modelleme ve tasarım çalışmaları bu hedefe göre yapılmaktadır. Bu çalışmada ise verimin ne olacağı baştan belirlenmemiş, devre performansındaki standard sapmaya göre verimin nasıl geliştirilebileceği gösterilmeye çalışılmıştır.

Tezde, istatistiksel MOS (SMOS) modeli istatistiksel tekniklerle birlikte kullanılmaktadır. SMOS modeli fabrikasyon sırasındaki rastgele olayları simülasyona katarken, istatistiksel teknikler seçilen devre performansını en çok etkileyen tranzistörleri belirlemekte ve bu tranzistör boyutları değiştirildiğinde devre performansındaki sapmanın ne olacağını göstermektedir. Devre, performansı en çok etkileyen tranzistörlerin değişken olarak kabul edildiği ampirik bir modelle temsil edilmektedir; devrenin performansındaki sapma ampirik modelin çıkış değişkeni olarak alınmaktadır.

Pekçok devrenin çalışma prensibi elemanların mükemmel uyumlu olması prensibine dayanmaktadır. Oysa pratikte devre elemanları arasında uyumsuzluk söz konusudur. Bu uyumsuzlukların sebebi yukarıda belirtilen rastgele olaylar ve devreyi oluşturan ve uyumlu olduğu kabul edilen eleman parametrelerinin farklı olmasıdır (intra-die mismatch). Bu etki devrenin gerçekteki performansını da etkilemektedir. SMOS modeli bu uyumsuzluğu modelleyen Pelgrom eşitliğini temel almaktadır. Pelgrom eşitliğine göre, devre elemanları arasındaki uyumsuzluğun standard sapması devredeki tranzistörlerin geçit alanları ile ters orantılı ve tranzistörlerin yerleşim planında birbirlerine olan uzaklıkları ile doğru orantılıdır:

$$\sigma^2(P) = \frac{a_p}{WL} + s_p^2 D^2$$

Bu bağıntıda a_p ve s_p fabrikasyon sabitlerini, D tranzistörler arası uzaklığı, W kanal genişliğini, L kanal uzunluğunu, $\sigma(P)$ ise P parametresine ait standart sapmayı göstermektedir. Bu bağıntı, devre elemanlarında gözlemlenebilecek iki önemli değişim olan eleman boyutu ve devre elemanlarının yerleşim planını gözönünde tutmaktadır. Bağıntıya göre, büyük boyutlu ve yerleşim planında birbirine yakın yerleştirilen tranzistörler arasındaki uyumsuzluk düşük olacak, tersine, küçük boyutlu ve yerleşim

planında birbirinden uzak yerleştirilen tranzistörler arasındaki uyumsuzluk büyük olacaktır.

Tezde SMOS modeliyle birlikte kullanılan istatistiksel teknikler, deneylerin sistematik olarak hazırlanmasına olanak veren ve bu amaçla çok sık kullanılan iki tekniktir: "Design of Experiments" (DOE) ve "Response Surface Methodology" (RSM). DOE yardımıyla giriş değişkenleri ile çıkış büyüklüğü arasındaki ilişki ampirik bir modelle temsil edilmekte, RSM yardımıyla ise bu ampirik model grafik olarak görüntülenmektedir. Ampirik modelin ve modeldeki terimlerin güvenilirliği de bu istatistiksel teknikler yardımıyla belirlenebilmektedir.

Birden fazla giriş değişkenine sahip devreler için DOE genellikle iki grup deneyle gerçekleştirilir. Bunların birincisi iki seviyeli bir çeşit testtir. Devredeki elemanların boyutları için bir maksimum ve bir de minimum değer belirlenir. Ampirik model, tranzistörlerin belirlenen bu maksimum ve minimum boyut değerleri arasında geçerli olacaktır. İki seviyeli test için Placket-Burman deneyi seçilmiştir. Bu seçimin sebebi, deneyin tasarımındaki kolaylık ve giriş değişkeni sayısı arttıkça yapılan deney sayısında çok büyük bir artışın gerekmemesidir. Placket-Burman deneyi sonucunda devre performansı üzerinde en çok etkili olan devre elemanları belirlenir; ikinci aşamada sadece bu elemanlar gözönüne alınacak, elenen diğer elemanlar ikinci deneye dahil edilmeyecektir. İkinci deney üç seviyeli bir testtir.

Bu deneyde elemanların boyutları minimum, maximum ve merkez değerlerinde incelenir. İkinci aşama için Box-Behnken deneyi seçilmiştir.

İkinci aşama testin sonuçları RSM yardımıyla değerlendirilerek, giriş parametrelerinin belirli bir aralığı için sözkonusu devre performansının hata dağılımını gösteren yüzey dağılımları elde edilir. Bu dağılımların her biri farklı bir standart sapma değerini temsil etmektedir. RSM sonucunda elde edilen grafiklerin x ve y eksenleri eleman boyutlarına karşılık gelmektedir. Bu grafikler yardımıyla istenilen eleman boyutları için devre performansındaki standart sapma değeri elde edilebilmektedir. Çıkış performansı için istenilen değer ve hedeflenen verim belirliyse grafiklerdeki bilgilerden yararlanılarak, bu hedefleri sağlayan en düşük tranzistör boyutlarını belirlemek mümkündür.

Tezde sekiz tane devrenin öncelikle çalışma prensipleri incelenmiş, daha sonra da bu devrelerin, yukarıda belirtilen metod ışığında istatistiksel incelemesi yapılmıştır. İncelemesi yapılan devreler iki adet düşük gerilim ve düşük güçlü kompozit hücre, bu hücrelerden yararlanılarak tez için tasarlanan iki yeni geçiş iletim devresi ve iki adet yeni çarpma devresi, dört-MOSFET tranzistör yardımıyla oluşturulan ve lineer bölgede çalışan yapı ve akım bölücü tekniğine dayalı olarak çalışan ve sayısal/analog çeviricilerin kodlanmasında kullanılan 10-bitlik akım bölücü devresidir.

Düşük gerilim ve düşük güç devreleri tek bir tranzistörün yerini tutmaktadır. Bu hücreler, Seevinck ve Wassenaar tarafından 1987 yılında yayınlanan ve birer NMOS ve PMOS tranzistörün seri olarak bağlanmasından oluşan kompozit tranzistörün düşük gerilimli ve düşük güçlü uygulamalar için uygun hale getirilmiş şekilleridir. Bu hücreler başka devrelerin yapılarında kullanılacak olduklarından hücrelerin tasarlanırken optimize edilmeleri ve çıkış akımlarının doğru bir biçimde belirlenmeleri gerekir. Hücrelerin istatistiksel incelemesi çıkış akımı için yapılmıştır. Rastgele değişimler gözönüne alındığında çıkış akımında büyük bir değişiklik olmaması gerekir; en düşük sapmayı verecek şekilde hücrelerin optimize edilmesi gerekir.

Tezde iki adet yeni geiş iletim devresi ve arpma devresi tasarlanmıřtır. Bu devrelerin tasarımında yukarıda belirtilen hücreler temel yapı bloęu olarak kullanılmıřtır.

Sözü geen bu altı devre analog blokların programlanabilirlięi ve yeniden kullanımı konusunda örnek olarak gösterilebilir. Analog bloklar optimize edildikten sonra daha karmařık devrelerin temel yapı blokları olarak kullanılabilirler. Temel yapı blokları optimum řekilde tasarlandıęı için, yapısına girdikleri devreler için uzun tasarım sürelerine ihtiya duyulmayacaktır. Bu, analog CAD alanında yapılan alıřmaların da hedefini teřkil etmektedir. Tezde bu konuyla ilgili olarak iki adet geiş iletim devresi ve iki adet arpma devresi sunulmuřtur. Bu dört devre yukarıda belirtilen hücreleri temel yapıtařı olarak kullandıęından, tasarımları ok uzun zaman almamıřtır. Bu devreler, literatürdeki pekok dięer geiş iletim devresi ve arpma devresinden daha fazla sayıda tranzistör bulunduruyor olabilir; ancak bu devrelerin tasarım amacı en iyi performansı saęlayan devreler tasarlamak deęil, analog programlanabilirlięe örnek vermektir. Bunun yanında, bu devrelerle pekok uygulamanın gerektirdięi sonuçlar almak da mümkündür.

Geiş iletim devreleri ve arpma devrelerinin ofset akımı ve lineerlięi istatistiksel olarak incelenmiřtir. Bu devrelerin nominal simülasyonları yapıldıęında ofset akımlarının "0" olduęu, nonlinearliklerinin ise ok düşük olduęu görölmüřtür. İstatistiksel sonuçlar ise ofset akımının mikro amperler mertebesinde olabileceęini, nonlinearlięin ise nominal sonuçlardan daha yüksek olabileceęini göstermektedir. Bu tür bir nonlinearlik devrelerin performansını olumsuz yönde etkileyebilecektir.

Tezde incelenen dört-MOSFET yapısı MOSIS 2 μ m prosesi kullanılarak üretilmiřtir. Dört-MOSFET yapısı üzerinde sıka yapılan tartıřma yapının elemanlarının mükemmel uyumlu olması durumunda her türlü nonlinearlięi ortadan kaldıracadıęı řeklinde, oysa pratikte elemanlar arasında mükemmel uyumluluk söz konusu deęildir. Bu durumda yapının lineerlik performansı önem kazanmaktadır, ünkü elde edilen sonuçlar yapıyı kullanan pekok devrenin analiz sonuçlarını da etkileyecektir. Dört-MOSFET yapısı istatistiksel olarak ofset akımı ve lineerlik için incelenmiřtir. Simülasyon sonuçları ile ölçüm sonuçları karřılařtırıldıęında sonuçların uyumlu olduęu görölmüřtür.

Tezde incelemesi yapılan son devre 10 bitlik akım bölücü devresidir ve bu devre de MOSIS 2 μ m prosesi kullanılarak üretilmiřtir. 10 bitlik akım bölücü devresinin alıřması devrenin elemanları arasındaki uyumluluęa dayanır; küçük bir uyumsuzluk devrenin kullanıldıęı sayısal/analog çeviricinin rezolüsyonunu etkileyecektir. İstatistiksel olarak incelenen performans devrenin ıkıř akımındaki hatadır. oęunlukla hata en düşük derecede önemi olan bitten (least significant bit, LSB) akan akım cinsinden hesaplanır ve hatanın 1 LSB'den düşük olması istenir. Simülasyon sonuçları ile ölçüm sonuçları karřılařtırılmıř ve uyumluluk olduęu gözlenmiřtir.

Yukarıda belirtilen bu sekiz devre, SMOS modeli ve eřitli istatistiksel yöntemler kullanılarak istatistiksel olarak incelenmiřtir.

Tezin birinci bölümü giriř nitelięi tařımaktadır; yapılan alıřmanın motivasyonu belirtilmiř ve daha önce bu konuda yapılan alıřmalar özetlenmiřtir. İkinci bölümde SMOS modeli ve tezde kullanılan istatistiksel teknikler ele alınmıřtır. Kullanılan istatistiksel tasarım metodu ayrıntılarıyla verilmiřtir. İstatistiksel olarak incelenen devreler tezin üçüncü bölümünde detaylı olarak ele alınmaktadır. Dördüncü bölüm bu devrelerin SMOS modeli ve istatistiksel yöntemler kullanılarak incelenmesini ele

almaktadır. Beşinci bölüm sonuç ve tartışma bölümüdür. Elde edilen sonuçlar yorumlanarak tartışılmış ve çalışmalar bir sonuca bağlanmıştır.

Tranzistörlerin boyutları küçüldükçe devrelerin belirlenen çıkış performanslarında görülen değişim büyümektedir. Bu Pelgrom eşitliğinde de açıkça görülmektedir. Elde edilen sonuçlardan çeşitli şekillerde yararlanmak mümkündür: Yüzey dağılımlarına bakarak, en düşük sapmayı sağlayan eleman boyutlarının belirlenmesi mümkündür. Tersine, eğer sapmanın ne olması gerektiği konusunda bir bilgi mevcutsa, bu sapmayı veren eleman boyutlarını belirlemek de mümkündür. Belirli bir standart sapmayı ve belirli bir verimi sağlayan en düşük eleman boyutlarının belirlenmesi bu yüzey dağılımlarından yararlanarak gerçekleştirilebilir.

Unutulmaması gereken bir nokta da, tüm yöntemlerin bilgisayar yardımıyla elde edildiği, ve sonuçlar ne kadar uygun olursa olsun, tasarımcının son kararı verecek olmasıdır. Devre performansı için en düşük sapmayı veren boyutlar o tasarım için uygun olmayabilir, bu durumda elde edilen sonuçları yorumlamak ve uygulamaya koymak konusunda son karar tasarımcıya aittir.

Elde edilen sonuçlara bakarak istatistiksel analizin standart devre tasarım adımlarından birisi olarak düşünülmesi gerektiği anlaşılmaktadır. Nominal simülasyon sonuçları devrelerin gerçek performanslarını tam olarak temsil etmeyebilmektedir. Bu durumda devrelerin istatistiksel olarak incelenmesinin önemi büyüktür.

Tezde belirtilen istatistiksel tasarım yöntemi ele alınan devreler için önemli sonuçlar vermiştir, başka pekçok analog devre için de önemli sonuçlar vereceği açıktır. Böylece, fabrikasyon sırasındaki rastgele olayları ve çeşitli istatistiksel yöntemleri bir arada kullanarak devrelerin performansı üzerine gerçeğe yakın bilgi alınabilmektedir. Yapılan ölçümler bu sonucu desteklemektedir.

1. INTRODUCTION

Low power microelectronics has advanced in productivity and performance with an enormous pace, since the invention of transistor in 1947. The requirement for small size and weight, long operating life, utility, and reliability of battery operated equipment was the earliest demand for low power microelectronics. Personal Digital Assistant (PDA), which is characterized as a combined pocket cellular phone, pager, e-mail terminal, fax, computer, calendar, address directory, notebook, etc. had an explosive growth [1, 2], and many approaches were proposed to satisfy the needs of the Personal Digital Assistant for low power electronics [3-7].

After the new micro-power techniques of the 1970s and shifting from NMOS and NPN bipolar technologies to CMOS technology in order to solve the heat removal problems, 1990s brought low power design to the forefront as a primary requirement for mainstream microelectronics [8]. The future opportunities for low power mega-scale integration started to be discussed.

The power supply voltage in VLSI circuits, on the other hand, has decreased to 3V and will continue to decrease. The three main driving forces for low voltage low power systems are technology, design and market. Technology-driven forces come from the reduction of the minimum feature size to scale down the chip area. Scaling down the transistor size can then integrate more circuit components in a single chip area and lower the cost. Also, smaller geometry usually lowers the parasitic capacitances, which means higher operating speed and lower power consumption. A decrease in MOS transistor size means reduced gate oxide thickness as well as reduced channel length. As a MOS

transistor has a thinner gate oxide, in order to prevent the transistor from breakdown because of the higher electrical field across the gate oxide and to ensure its reliability, the power supply voltage is necessary to be reduced.

With the reduction of the device minimum feature size, millions of transistors can be fabricated on the same chip. This will result in a tremendous power consumption and cause excessive heating. Usually most of the chip area is occupied by the digital circuits and the average power consumption for digital circuits is proportional to the square of the power supply voltage. Thus, decrease of the supply voltage reduces the power consumption in a significant amount.

All the above factors contribute to the necessity of low voltage low power circuit solutions. Since digital circuits occupy most of the chip area; they are more popular and computer-aided design tools for digital circuits are very mature. Digital circuit performances do not suffer a lot from lowering supply voltages. On the other hand, analog circuit performances are strongly affected by the low voltage supply. Therefore, new design techniques for low voltage analog circuits are required to be developed. In digital circuit design, a low supply voltage almost guarantees the low power consumption. However, this is not always the case for analog circuit design. To achieve the same goal of circuit performances by either using a low or a higher supply voltage might lead to approximately the same level of power consumption because of the different circuit design techniques utilized for using different supply voltages. Thus, low voltage analog circuit design with the emphasis of low power consumption has become a major challenge for analog circuit designers [9].

The development of analog circuits requires both a complete understanding of basic circuit design techniques and a knowledge of transistor nonideality effects on circuit performance. One severe effect comes from the device imperfections and variances of the fabrication process. Despite the technological progress in the fabrication process steps, the fluctuation in each step that affects the device performances have not been scaled down in proportion. The fabrication process is not easily characterized because these variations are random in nature. Such variations could ultimately be a limiting factor on how low the supply voltage and how reliable sub-micron designs could be. In

order to produce manufacturable analog integrated circuits with high functional yield and a high degree of reliability, the design of such circuits must be robust with respect to random process and device parameter variations [10]. The functional yield of a chip is the percentage of the total number of circuit samples which have an acceptable circuit performance determined by the chip specifications, over the total number of circuit samples. This is different from catastrophic or destructive yield over which circuit designers have no control. Circuit designers must ensure that their chips have an acceptable functional yield under all manufacturing process variations. If there is more than one sample of the circuit on the same chip, the number of working circuits might be high, but in order to have a high functional yield the number of the circuits working with the required performance should be as high as possible. There are two ways to increase the functional yield: By improving the control of manufacturing process and by designing the process and circuits in such a way as to minimize the effect of inherent variations of the process on performance. The latter is typically referred to as “statistical design”. The statistical design problem is clearly to find a set of nominal component values and their tolerances that represent the minimum on the cost versus yield curve shown in Figure 1.1.

Due to inherent fluctuations in any integrated circuit manufacturing process, the functional yield is always less than 100%. As the complexity of VLSI chips increase, and the dimensions of VLSI devices decrease, the sensitivity of performance to process fluctuations increases, thus further reducing the functional yield. Moreover, with current trends of higher levels of integration leading to complete mixed-signal systems on a chip, yield loss due to the analog component must be minimized such that it has little effect on the yield of the mixed-signal chip.

Many meaningful insights have been provided into the statistical design problem. Early works have suffered from having only a few variables [11, 12] or simply consuming excessive CPU time [13]. An efficient technique was presented for yield gradient computation [14]; the number of design variables was primarily limited by the selected constrained nonlinear optimization algorithm in this work. Shyu et al. [15, 16] used statistical methods to examine the random errors affecting capacitance and current ratios

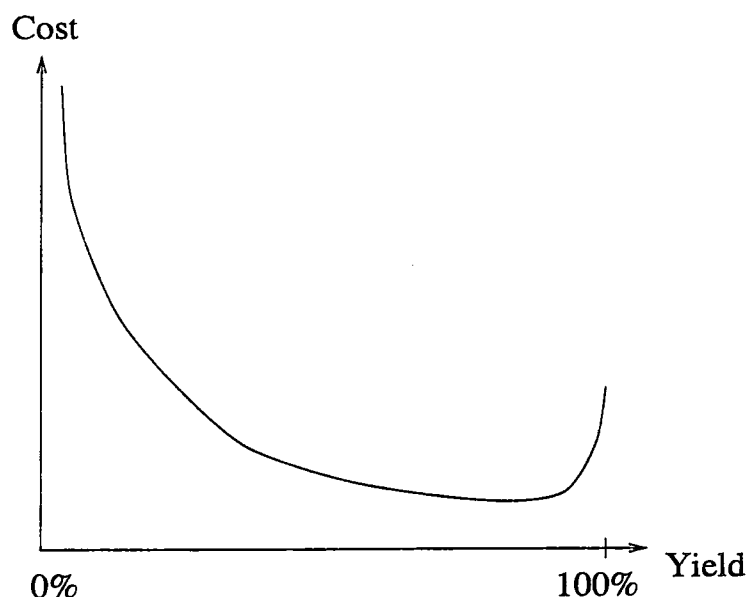


Figure 1.1: A typical circuit cost versus yield curve

in MOS integrated circuits. Explicit formulas were derived to give the dependence of each error source on the physical dimensions, the standard deviations of the fabrication parameters, the bias conditions, etc. All transistor variances were derived in terms of their effect on current matching in a current mirror. Additionally, Shyu examined edge effects which explain the variance of channel length and width. Lakshmikumar et al. [17] furthered Shyu's work and separated the area dependence of transistor mismatch into variance models for the threshold, V_T , and the current factor, β . Pelgrom et al. [18] included a term for the substrate factor variance and also altered the effect of global variations from a constant. Pelgrom also determined that edge effects have a negligible contribution to the overall variance of the current factor. However, it is expected that for very short or narrow devices, edge effects will contribute heavily to the parameter variance. Michael et al. [19] included the correlations among electrical parameters which were not included in Pelgrom's model. The statistical MOS (SMOS) model was presented as a tool for circuit designers to estimate the functional yield of a designed circuit without the fabrication of the device [19]. With the increasing popularity of BiCMOS technology, statistical methods are becoming necessary for BJTs too. The

work of Michael has been extended to BiCMOS circuits and an appropriate test structure for BJT parameter mismatch extraction and characterization has been discussed in [20]. Abel et al. [21] showed that the current mismatch of a pair of MOS transistors at any bias point can be represented by mismatches in four standard MOS parameters: V_{TO} , γ , β and θ . The mismatch of a standard MOS parameter, $\sigma(\Delta P)$, in a large sample of matched transistor pairs is inversely proportional to the square root of the areas of the individual transistors. A graphical approach for the statistical design of RF circuits and systems was given in [22]. Recently, a new test structure for the characterization of MOS transistor mismatch and mismatch drift was presented [23]. Another recent work investigates MOS transistor mismatch and presents a methodology for optimizing mismatch without increasing layout area [24]. The work also examines edge effects and proves that the channel length and width reduction terms have very significant contributions to the area when considered for mismatch. In reference [25], the device matching issues of submicron analog CMOS circuits are addressed.

This study demonstrates the critical need to perform statistical design and optimization in order to enhance both the functional yield and reliability of low voltage low power analog VLSI circuits. The term “enhancing functional yield” stands for using tools and techniques that will target a high functional yield, by reducing the standard deviation of the circuit performance, instead of the typical methods of designing and hoping for the best yield. If the circuits are not optimized the variation of the performance may be very large, thus, the distribution will also be high. After optimization, however, it is possible to reduce the variation and keep the distribution smaller, thus, the yield will be higher. In industry, usually the yield requirement is initially set (e.g., to 99%) and the statistical modeling and statistical design of the circuits target this yield specification. The term statistical design includes the whole process of trying to make a robust design. The success of the chip is determined by how high the yield is; a high yield also reduces the cost. In this thesis, the yield specification is not initially set. It is the goal to show that it is possible to enhance the yield by reducing the standard deviation of the performance and optimizing the circuit.

Previous studies in the area of statistical modeling and simulations were separately successful in determining both the functionality of parameter mismatch variance and a methodology to simulate circuits. Merging the results of these two fields into a unified method to model and simulate performance variances in circuits containing MOS devices has resulted in the well known SMOS model which accounts for parameter correlations and physical layout information (e.g., device area and on-chip separation distance) [10].

The robust design process, in this thesis is the usage of the statistical MOS (SMOS) model to include the random process variations into the simulation environment, and the statistical techniques, such as Design of Experiments (DOE) and Response Surface Methodology (RSM), to determine the most important transistors for the circuit performance, and the optimum size for these transistors. The final objective, besides keeping the functional yield high, is to give flexibility to the designer, in finding the optimum size for the transistors. The response surfaces will provide this flexibility. The complete statistical design methodology is explained in Chapter 2. It is noteworthy that using statistical techniques such as DOE and RSM, together with the SMOS model, to make robust analog CMOS circuit designs is the first serious attempt with this thesis.

Chapter 3 describes the circuits that will be later statistically examined in Chapter 4. The circuits are selected among those which are subject to attention recently. The transconductor and multiplier circuits, however, are new designs for the thesis. The strategy behind these new designs are emphasized in the next page. All circuits are not the only examples of their types, and not the only circuits used for their purpose, but they certainly are one of the most popular, and recently used in several areas. These circuits are two low voltage and low power CMOS square-law analog composite cells, two transconductors and multipliers which use the low voltage and low power composite cells as a main building block, the four-MOSFET structure, and the 10-bit current division network, which are critical blocks in determining the overall performance of the designs they are used in.

Many applications which require reduced supply voltage and low power consumption are based on analog/digital mixed mode signal processing VLSIs. To process analog

signals in such mixed mode systems, low voltage low power transconductors and/or multipliers have been widely used for programmability. These circuits are basically composed of several cells which have a square-law characteristic. A single MOSFET fulfills this characteristic, however, the low input impedance at the source of the transistor limits the applicability of the single transistor solution. Recently, several new low voltage low power CMOS square-law composite cells with two high impedance input terminals were proposed to achieve highly accurate signal processing with low power dissipation. The design and operation principles of two of these cells are introduced in Chapter 3. Two new low voltage low power transconductors and multipliers were designed with these cells. The circuit description of the transconductors and multipliers are also given in Chapter 3. The first transconductor and multiplier circuits operate from a low supply voltage and maintains a wide input voltage swing capability. The second transconductor and multiplier circuits have the advantage of a low standby current, therefore, the circuits are more attractive for low power applications.

One discussion is made for analog circuits being programmable as in the digital area. The long range goals are to make analog circuits programmable, and to realize applications involving analog computation. The goal is to come up with an analog design methodology similar to the one used for digital circuits, and take advantage of the basic building blocks. The low voltage and low power cells of this thesis are referred to as the basic building blocks, and the transconductor and multipliers are the circuits that take advantage of the building blocks, thus, the main effort is put when building the cells, and the cells are put together to build the transconductor and multiplier circuits. This also has an impact on the design time.

Fully integrated continuous time circuits can be realized in MOS technology by using MOS transistors operating in the triode region. MOS transistors used in filter applications for implementing linear resistors, suffer from nonidealities causing signal distortion such as body effect, mobility variation, device mismatch, etc. Extensive research has been conducted on the fully balanced integrator with MOS resistors, and a balanced two-MOSFET configuration was first introduced to cancel out even-order

nonlinearities [26]. It was later demonstrated, using a strong inversion MOS model, that a four-MOSFET structure also fully suppresses the body effect related odd-order terms [27, 28]. However, recent works question the widely accepted superiority of the four-MOSFET structure [29]. The result of the discussion is important because the supposed linearity properties of the four-MOSFET structure is served to justify its use in several recent applications [30, 31]. Therefore, it is of extreme importance to statistically examine the circuit. The four-MOSFET structure is reviewed in Chapter 3.

Digital-to-analog (D/A) converters interface the digital output of signal processors with the analog world, therefore, it is an essential function in data processing systems. The linearity of the D/A converter strongly depends on the accuracy of the reference multiplication or division employed to generate the output levels. The three electrical quantities, voltage, current and charge can be multiplied or subdivided using resistor ladders, current-steering circuits, and switched capacitor circuits, respectively. In this work the current division technique is used to divide the reference current in order to provide binary weighting, for a 10-bit example. The 10-bit current division network and its operation principle is given in Chapter 3.

Chapter 4 consists the main focus of this thesis. The statistical design and analysis of the circuits given in Chapter 3 will be discussed in detail, while providing experimental results for the four-MOSFET structure and the 10-bit current division network.

The CMOS square-law composite cells require highly matched currents flowing through the CMOS pair. Any mismatch in these currents will cause variations in the performance of the overall circuits which use the cells as a main building block, hence, the statistical examination of the relative drain current mismatch is important. It will be shown that statistical design is a crucial step in designing robust transconductor and multiplier circuits, since they depend on device matching to achieve a linearized characteristic. Response surfaces provided allow the circuit designer to be able to optimize the transistor sizes of the circuits before fabrication. Previously reported transconductor and multiplier works ignored the statistical approach in their design, hence, they can exhibit a wide variation in the offset and nonlinearity when manufactured in large numbers.

For exact cancellation of nonlinearities in the four-MOSFET structure, perfect matching is required, whereas random variations may not always allow for exact matching of the transistors. The previously done works have not considered random variations, hence it is important to quantitatively determine the effect of mismatches on nonlinearity cancellation. The experimental results will also be given in Chapter 4.

The achievable resolution of the D/A converter is an important design consideration. The D/A converter presented in Chapter 3 uses a 10-bit current division network in order to provide binary weighting. The current division network is based on the assumption of matched transistors, whereas, random variations may cause mismatch between transistors and a slight mismatch may cause an error which will limit the achievable resolution. Therefore, it is important to consider statistical simulations in the design of the D/A converter and to determine the error in terms of LSB units. The statistical design of the D/A converter based on the current division network is examined in detail in Chapter 4. Experimental results are provided.

The four-MOSFET structure and the 10-bit current division network prove the importance of statistically examining circuits to obtain the quantitative effect of mismatch between transistors, as well as the statistical design of low voltage and low power circuits.

Chapter 5 summarizes the work as well as discussing the results provided in Chapter 4. A conclusion together with future studies is given after this discussion.

2. THE STATISTICAL MOS (SMOS) MODEL AND STATISTICAL DESIGN TECHNIQUES

As feature sizes in MOS processes move into the sub-micron range and power supply voltages are reduced, both device mismatch and inter-die process variations on the performance and reliability of analog circuits is magnified. Random variations in integrated circuit processes result in random variations in transistor parameters. Due to inherent fluctuations in any integrated circuit manufacturing process, the functional yield is always less than 100%. As the complexity of VLSI chips increase, and the dimensions of VLSI devices decrease, the sensitivity of performance to process fluctuations increases, thus further reducing the functional yield. Moreover, with current trends of higher levels of integration leading to complete mixed-signal systems on a chip, yield loss due to the analog component must be minimized such that it has little effect on the yield of the mixed-signal chip. This requires the robust design of the circuits on the chip.

In order to fully utilize the capabilities of a given process, a circuit designer needs to have both a complete knowledge of the statistical distributions of transistor parameters produced by the process and a way to determine the effects of variations in these parameters on the circuit performance.

Previous studies in the area of statistical modeling and simulations were separately successful in determining both the functionality of parameter mismatch variance and a methodology to simulate circuits, but merging the results of these two fields into a unified method to model and simulate performance variances in circuits containing

MOS devices has resulted in the well known SMOS model which accounts for parameter correlations and physical layout information [10].

The robust design process, in this thesis is the usage of the statistical MOS (SMOS) model to include the random process variations into the simulation environment, and the statistical techniques, such as Design of Experiments (DOE) and Response Surface Methodology (RSM), to determine the most important transistors for the circuit performance, and the optimum size for these transistors. The statistical techniques are used to build an empirical model which will represent the circuit. The final objective, besides keeping the functional yield high, is to give flexibility to the designer, in finding the optimum size for the transistors. The response surfaces will provide this flexibility.

The complete statistical design methodology is explained in this chapter, starting with the SMOS model and continuing with the statistical design techniques.

2.1. The Statistical MOS (SMOS) Model

2.1.1. Statistical Parameter Modeling

Random variations in integrated circuit processes cause random variations in transistor parameters. Causes of circuit output variance can be divided into two groups [10]: Inter-die device variability and intra-die device variability. Inter-die device variability is characterized by die-to-die, wafer-to-wafer, or lot-to-lot process variability. Figure 2.1 shows the separation of device variability.

Since inter-die variability equally affects all transistors in a given circuit, it can be represented by a deviation in the parameter mean of every transistor in the circuit, as shown in Figure 2.2.

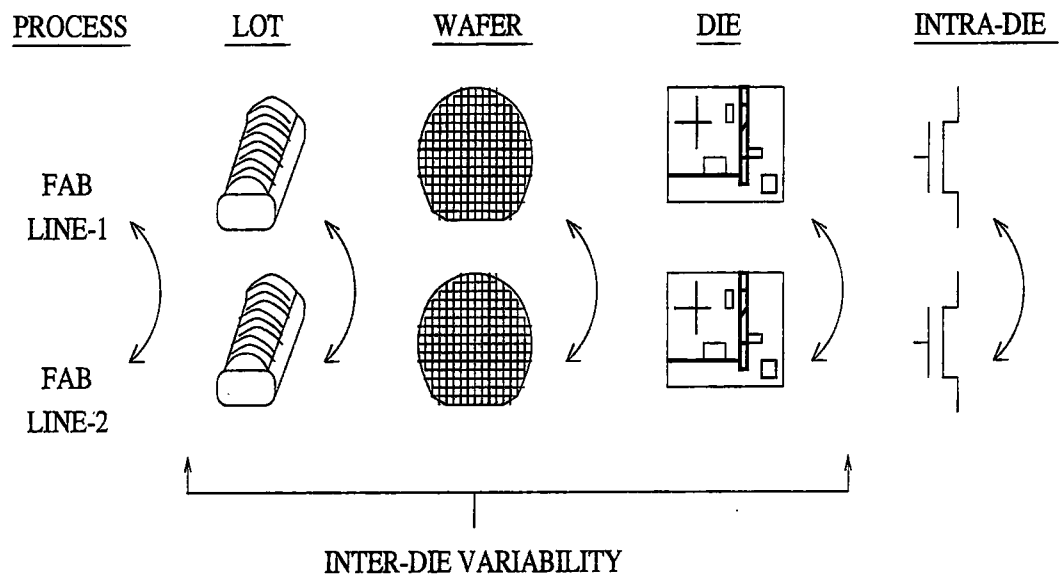


Figure 2.1: Separation of device variability

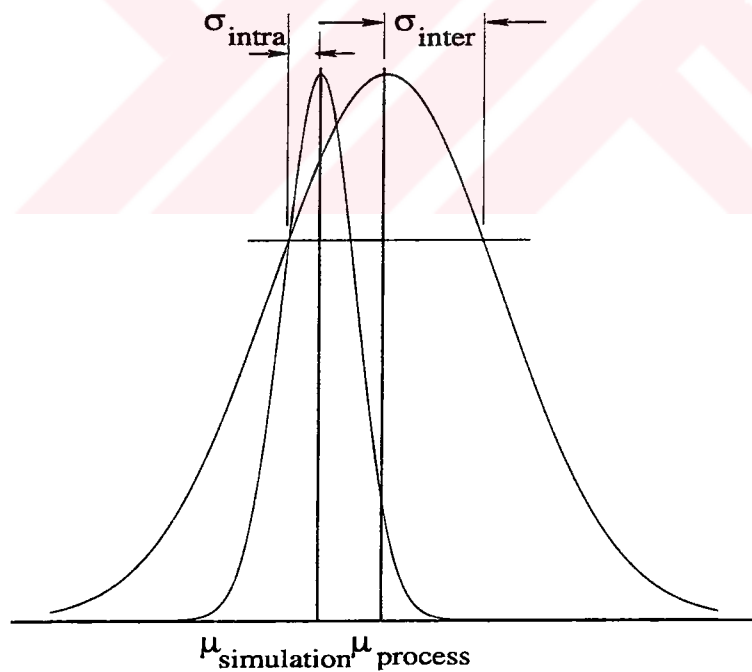


Figure 2.2: Relation between inter- and intra-die parameter standard deviations

μ_{process} is the process-level parameter mean, and $\mu_{\text{simulation}}$ is the randomly determined value of parameter mean used for each transistor in one circuit simulation. Inter-die parameter standard deviation is usually much larger than intra-die parameter standard deviation; however, in many analog circuits, it is intra-die parameter variances or device mismatch which cause the greatest deviations in circuit performance.

Intra-die device mismatch causes similarly designed transistors under equivalent biasing conditions to behave differently. This type of mismatch arises from wafer-level process variability and therefore is much difficult to model. The degree of mismatch between two devices is, in general, dependent on both the size and relative location of the devices. In analog integrated circuits, device mismatch contributes greatly to variances in circuit performance. The effect of inter-die device variability may be counteracted in many analog circuits either by automatic tuning techniques or by altering available bias conditions. Therefore, a statistical model which comprehends device mismatch is necessary for the statistical analysis of analog circuits.

2.1.2. Parameter Variance Models for MOS Device Mismatch

In order to include the random mismatch effects between circuit devices, the statistical model must have a different set of model parameters for each transistor in a circuit. Pelgrom and others [15-18] showed that the variance of the mismatch can be represented by

$$\sigma^2(P) = \frac{a_p}{WL} + s_p^2 D^2 \quad (2.1)$$

where D is the separation distance, WL is the gate area of the transistor, and a_p and s_p are process dependent fitting constants. This model considers two of the greatest effects on device variability of analog circuits: Device size and circuit layout. The two terms on the right-hand side of equation (2.1) are independent and are assumed to be normally distributed, which means, they can be accounted for separately when calculating transistor parameter sets. According to equation (2.1), the standard deviation of the mismatch is reversely proportional to the area of the transistor, and directly proportional

to the square of the separation distance. This equation is a result of Pelgrom's work on measurements that were taken from 2 μ m and longer channel lengths of transistors, which were fabricated over years. Recent works on the matching issues of submicron channel lengths [24, 25] proves that the $1/WL$ phenomena changes. Equation (2.1) is restated such that the variance of the mismatch is reversely proportional to the effective area of transistors, since the effect of the submicron channel length on mismatch becomes a dominant factor.

The complete work for the statistical analysis of CMOS analog circuits of this thesis is done using the statistical MOS (SMOS) model for 2 μ m or longer channel lengths, where equation (2.1) proves a good fit. The SMOS model is a model which includes the random process variations implemented in its framework, and it is applied to 16 BSIM model parameters because of the ability of the BSIM model to account for the effects of both, device geometry and biasing. The chip measurements for the statistical parameters in the SMOS model results were taken from 39 MOSIS 2 μ m n-well process runs, and results for each BSIM parameter were put together to build the Gaussian distribution for that parameter. The model calculation procedure for the SMOS model is presented in Figure 2.3.

The process is characterized by the parameter means, correlations and standard deviations. The MOS transistor is modeled by multiple parameters and these parameters are not independent. The correlation between variances of different parameters have to be preserved for a statistical model to be useful. One way of modeling the correlation between parameters is to use Principal Component Analysis (PCA) [10, 20, 32]. PCA is used to generate normalized parameters from independent unit normal random variables, using a series of linear equations. Thus, correlation among parameters is preserved by their PCA coefficients and the independent variables. 16 PCA coefficients for 16 BSIM parameters were calculated to be used in the SMOS model. It was seen that the first 6 PCA coefficients were sufficient to describe 94.6% of the correlation information between the model parameters, and the other 10 PCA coefficients had a value very close to "0". Thus, it is a good approximation to preserve the correlation between the parameters, with the help of 6 PCA coefficients; the rest can be ignored.

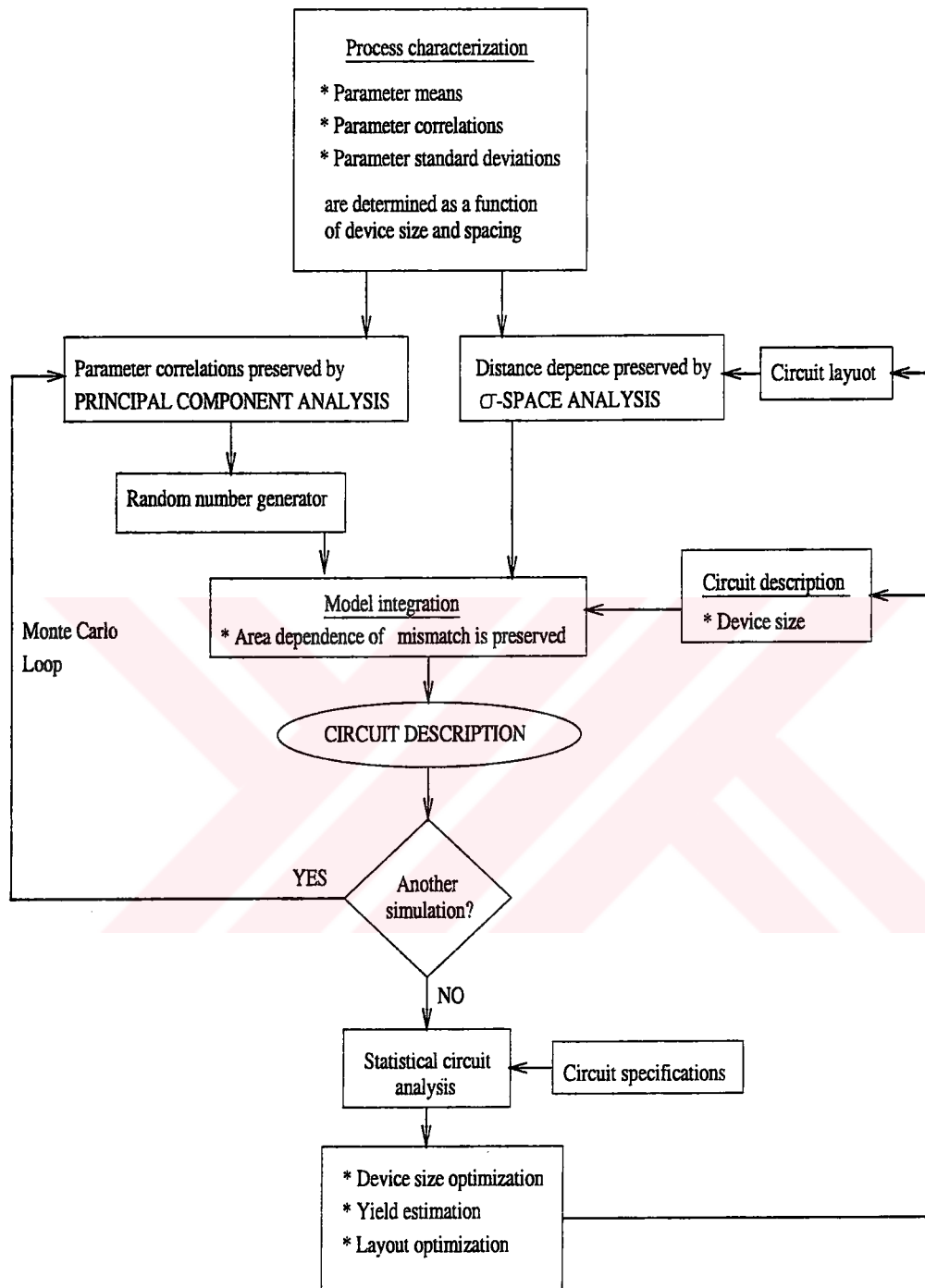


Figure 2.3: The model calculation procedure for the SMOS model

The use of the SMOS model in the simulation environment requires a separate model file that specifies the name of the fitting constants that are used in the mean and variance models, μ_0 , μ_L , μ_W , $\sqrt{a_p}$ and s_p , followed by the 6 PCA coefficients that account for almost 95% of the system variance [19]. The statistical BSIM model files for n- and p-channel MOS transistors in the 2 μ m n-well process are given in Appendix A.

The distance dependency of the mismatch is preserved with the help of σ -space analysis [19]. These analysis methods, together with the circuit layout information and the Monte Carlo loop results in device size optimization, yield estimation and layout optimization.

The statistical MOS model has been incorporated into APLAC (Analysis and Design Program for Mixed, Lumped, and Distributed Circuits) [10,33], which is an object oriented simulation program, under constant development at the Helsinki University of Technology, since 1972. The first generations of APLAC were written, using either the BASIC or the PASCAL programming languages, until 1988, when the C programming language was selected as the language, to add object orientation as a feature in the fifth generation version of APLAC. The object orientation adds advantages, such as simplified coding, easy updating, inclusion of new algorithms and models. The main goal is to offer an environment which can be expanded without having to touch the original code of APLAC, which helps to make the implementation of the SMOS model into APLAC very easy. APLAC has been used for the statistical analysis of the circuits in this thesis.

2.2. Statistical Design Techniques

Circuit designers would like to make as much experiments as possible by changing their input variables in a wide range, in order to optimize their circuit performances. An analytical model is costly to build and difficult to apply, therefore, statistical techniques have to be employed to build the empirical model of the circuit. Variables affecting the circuit performance will be the variables of the empirical model and it will become

possible to vary the input variables in a (relatively) wide range. As a powerful technique of empirical model building, Response Surface Methodology (RSM) [34, 35] characterizes the relationship between the output and independent input variables of the system.

The construction of the empirical model starts with running a series of experiments at different input variable levels. Design of Experiment (DOE) [34] is a widely used systematic method for experiment planning, and can be applied to make the experiments in an efficient way.

This section will review the Design of Experiment Method and also describe two specific methods of experiments, named as Plackett-Burman and Box-Behnken designs. The Response Surface Methodology is described as well. Finally, the complete statistical design methodology used in this thesis will be explained in detail.

2.2.1. Approaches for Experimental Design

An experiment is a series of tests in which changes are made to the input variables of a process or system so that the reasons for changes in the output response can be observed and identified. The objective of experiments, in many cases may be to develop a robust design, that is, a design affected minimally by external sources of variability. In general, experiments are used to study the performances of systems and they often involve several factors. Usually, the objective of the experimenter is to determine the influence that these factors have on the output of the system.

The general approach to planning and conducting an experiment is called the strategy of experimentation. There are several strategies that an experimenter could use, such as the best-guess approach and one-factor-at-a-time approach. Both of these approaches have several disadvantages; the best-guess approach can continue for a long time without any guarantee of success, and the one-factor-at-a-time approach fails to consider any possible interaction between the factors. One-factor-at-a-time experiments are always less efficient than other methods based on a statistical approach to design.

The correct approach to dealing with several factors is to conduct a factorial experiment. This is an experimental strategy in which factors are varied together, instead of one at a time. Generally, if there are k factors, each at two levels, the factorial design would require 2^k runs. All possible combinations of the levels of the factors are used. Clearly, as the number of factors of interest increases, the number of runs required increases rapidly; for instance, a ten-factor experiment with all factors at two levels would require $2^{10}=1024$ runs. This quickly becomes infeasible from time viewpoint.

Fortunately, if there are four to five or more factors, it is usually unnecessary to run all possible combinations of factor levels. A fractional factorial experiment is a variation of the basic factorial design in which only a subset of the runs are made [34, 35]. Before going into the details of factorial and fractional factorial designs, guidelines for designing experiments will be discussed.

2.2.2. Guidelines for Designing Experiments

To use the statistical approach in designing and analyzing an experiment, it is necessary to have a clear idea in advance of exactly what is to be studied, how the data are to be collected, and at least how these data are to be analyzed. An outline of the experimental design procedure could be as follows [34]:

- a) Recognition of and statement of the problem: It is necessary to develop all ideas about the objectives of the experiment. A clear statement of the problem often contributes substantially to a better understanding of the phenomena and the final solution of the problem.
- b) Choice of factors, levels and ranges: The experimenter must choose the factors to be varied in the experiment, the ranges over which these factors will be varied, and the specific levels at which runs will be made. The designer will decide on a region of interest for each variable, that is, the range over which each factor will be varied, and on how many levels of each variable to use. Process knowledge is required to do this. This process knowledge is usually a combination of practical experience and theoretical

understanding. When the objective of the experiment is factor screening or process characterization, it is usually best to keep the number of factor levels low. Generally, two levels work very well in factor screening studies. Choosing the region of interest is also important. In factor screening, the region of interest should be relatively large. As we learn more about which variables are important and which levels produce the best results, the region of interest will usually become more narrow.

c) Selection of response variable: In selecting the response variable, the experimenter should be certain that this variable really provides useful information about the process under study. Most often the standard deviation of the measured characteristics will be the response variable.

d) Choice of experimental design: If the first three steps are done correctly, this step will be relatively easy. There are several interactive statistical software packages that support this phase of experimental design. The experimenter can enter information about the number of factors, levels and ranges, and these programs will either present a selection of designs for consideration or recommend a particular design. These programs will usually also provide a work sheet for use in conducting the experiment.

e) Performing the experiment: When running the experiment, it is vital to monitor the process carefully to ensure that everything is being done according to the plan.

f) Statistical analysis of the data: Statistical methods should be used to analyze the data so that results and conclusions are objective rather than judgemental in nature. If the experiment has been designed correctly and if it has been performed according to the design, then the statistical methods required are not elaborate. Properly applied, statistical methods do not allow anything to be proved, experimentally, but they do allow to measure the likely error in a conclusion or to attach a level of confidence to a statement. The primary advantage of statistical methods is that they add objectivity to the decision-making process.

g) Conclusions and recommendations: Once the data has been analyzed, the experimenter must draw practical conclusions about the results and recommend a course of action.

2.2.3. Factorial Designs

Many experiments involve the study of the effects of two or more factors. In general, factorial designs are most efficient for this type of experiment. A factorial design means that, in each complete trial or replication of the experiment, all possible combinations of the levels of the factors are investigated. The effect of a factor is defined to be the change in the response produced by a change in the level of the factor. This is frequently called a main effect, because it refers to the primary factors of interest in the experiment. A two-factor factorial experiment with design factors at two levels could be given as an example. The levels are called “low” and “high” and are denoted as “-” and “+”, respectively, as shown in Figure 2.4(a).

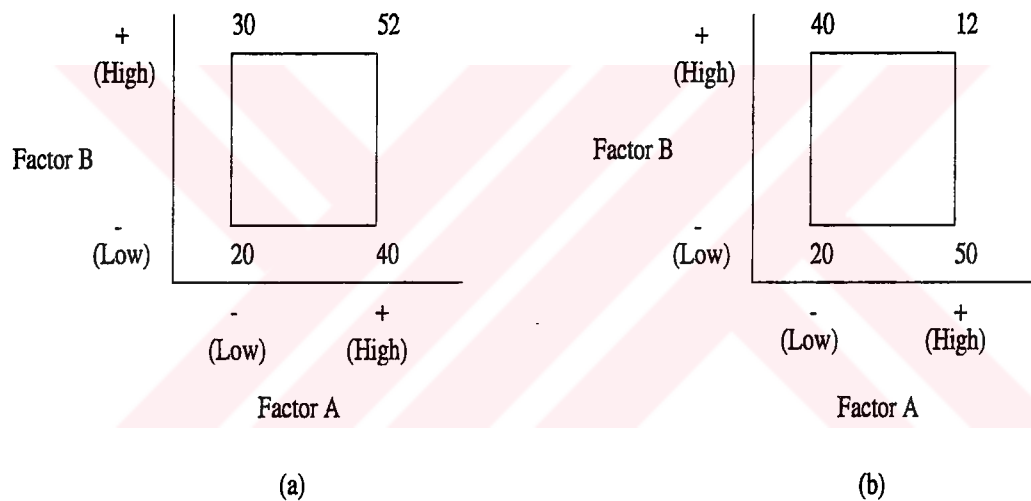


Figure 2.4: Two-factor factorial experiments

The main effect of factor A in this two-level design can be thought of as the difference between the average response at the low level of A and the average response at the high level of A. Numerically, this is

$$A_{effect} = \frac{40 + 52}{2} - \frac{20 + 30}{2}$$

$$A_{effect} = 21$$

This means, increasing factor A from the low level to the high level causes an average response increase of 21 units. Similarly, the main effect of B is

$$B_{effect} = \frac{30 + 52}{2} - \frac{20 + 40}{2}$$

$$B_{effect} = 11$$

In some experiments, it can be found that the difference in response between the levels of one factor is not the same at all levels of the other factors. When this occurs, there is an interaction between the factors. For example, consider the two-factor factorial experiment shown in Figure 2.4(b). At the low level of factor B, the A effect is $A_{effect(low)}=50-20=30$ and at the high level of factor B, the A effect is $A_{effect(high)}=12-40=-28$. Since the effect of A depends on the level chosen for factor B, there is an interaction between A and B. The magnitude of the interaction effect is the average difference in the two A effects

$$B_{interaction} = \frac{-28 - 30}{2}$$

$$B_{interaction} = -29$$

Clearly, the interaction is large in this experiment.

Figure 2.5 shows the factorial experiments once without and once with interactions between the factors.

Figure 2.5(a) plots the response data in Figure 2.4(a) against factor A for both levels of factor B. Note that the B^- and B^+ lines are approximately parallel, indicating a lack of interaction between factors A and B. Similarly, Figure 2.5(b) plots the response data in Figure 2.4(b). In this figure, the B^- and B^+ lines are not parallel. This indicates an interaction between factors A and B.

Such graphs are frequently useful in interpreting significant interactions. However, their interpretation is subjective and their appearance is often misleading.

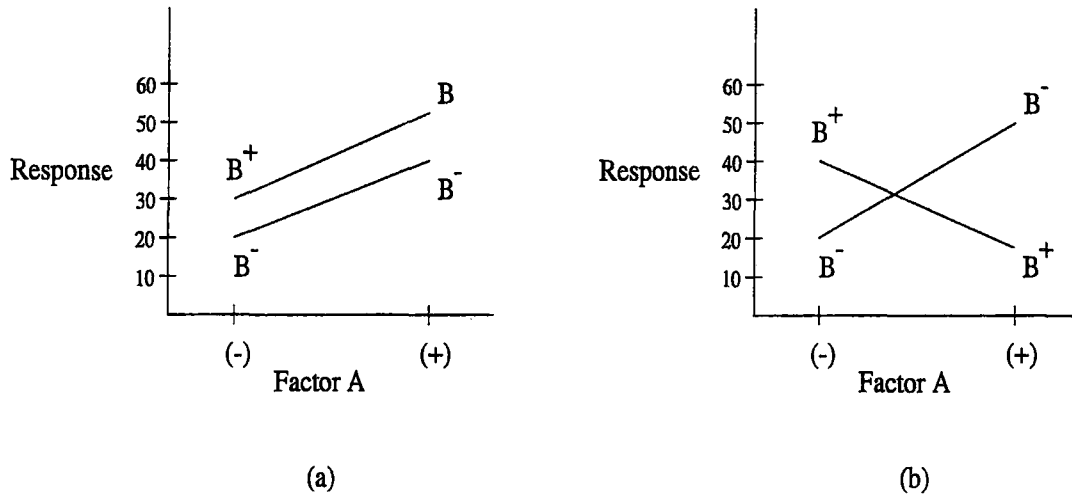


Figure 2.5: Factorial experiment a) without, b) with interaction

There is another way of illustrating the concept of interaction. A regression model representation of the two-factor factorial experiment could be written as

$$y = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_{12} x_1 x_2 + \varepsilon \quad (2.2)$$

where y is the response, the β s are parameters whose values are determined, x_1 is a variable that represents factor A, x_2 is a variable that represents factor B, and ε is a random error term. The variables x_1 and x_2 are defined on a coded scale from -1 to +1, and $x_1 x_2$ represents the interaction between x_1 and x_2 . Generally, when interaction is large, the corresponding main effects have little practical meaning. For the example in Figure 2.5(b), the expected result would be that the main effect of A to be small:

$$A_{effect} = \frac{50 + 12}{2} - \frac{20 + 40}{2}$$

$$A_{effect} = 1$$

The conclusion is that there is no effect due to factor A. However, examining the effects of A at different levels of factor B, A has an effect, but it depends on the level of B. That is, knowledge of the AB interaction is more useful than knowledge of the main effect. A significant interaction will often mask the significance of main effects.

Factorial designs have several advantages. They are more efficient than one-at-a-time experiments. Furthermore, a factorial design is necessary when interactions may present to avoid misleading conclusions. Factorial designs allow the effects of a factor to be estimated at several levels of the other factors, yielding conclusions that are valid over a range of experimental conditions.

Factorial designs are widely used in experiments involving several factors where it is necessary to study the joint effect of the factors on a response. However, there are several special cases of the general factorial design that are important because they are widely used in research work and also because they form the basis of other designs of considerable practical value.

The most important of these special cases is that of k factors, each at only two levels. These levels may be quantitative, such as two values of temperature, pressure, or time; or they may be qualitative, such as two machines, two operators, the “high” and “low” levels of a factor. A complete replicate of such a design requires $2 \times 2 \times 2 \times \dots \times 2 = 2^k$ observations and is called a 2^k factorial design.

As the number of factors in a 2^k factorial design increase, the number of runs required for a complete replicate of the design rapidly grows. For example, a complete replicate of the 2^6 design requires 64 runs. In this design only 6 of the 63 degree of freedom correspond to the main effects, and only 15 degrees of freedom correspond to two-factor interactions. The remaining 42 degrees of freedom are associated with three-factor and higher interactions. If the experimenter can reasonably assume that certain high-order interactions are negligible, then information on the main effects and low order interactions may be obtained by running only a fraction of the complete factorial experiment [34, 35]. The next section will provide the details of fractional factorial designs.

2.2.4. Fractional Factorial Designs

A major use of fractional factorials is the screening experiments. These are experiments in which many factors are considered with the purpose of identifying those factors that have large effects. Screening experiments are usually performed in early stages of a project when it is likely that many of the factors initially considered have little or no effect on the response. The factors that are identified as important are then investigated more thoroughly in subsequent experiments.

The successful use of fractional factorial designs is based on three key ideas:

- 1- Sparsity of effect principle: When there are several variables, the system or process is likely to be driven primarily by some of the main effects and low order interactions.
- 2- The projection property: Fractional factorial designs can be projected into stronger (larger) designs in the subset of significant factors.
- 3- Sequential experimentation: It is possible to combine the runs of two (or more) fractional factorials to assemble sequentially a larger design to estimate the factor effects and interactions of interest [34].

Among several procedures for fractional factorial designs, the Plackett-Burman design [34] has been selected in this thesis for its simplicity and will be discussed next.

2.2.5. Plackett-Burman Designs

Plackett-Burman designs are two-level fractional factorial designs studying $k=N-1$ variables in N runs, where N is a multiple of 4. If N is a power of 2, the Plackett-Burman designs are identical to other fractional factorial designs, however, for $N=12, 20, 24, 28$ and 36, the Plackett-Burman designs receive much of attention.

Table 2.1 presents rows of plus and minus signs that are used to construct the Plackett-Burman designs for $N=12$ and 20.

Table 2.2 shows the design matrix for $N=12$.

Table 2.1: Rows of plus and minus signs that are used to construct the Plackett-Burman designs for N=12 and 20

N																			
12	+	+	-	+	+	+	-	-	-	+	-								
20	+	+	-	-	+	+	+	+	-	+	-	+	-	-	-	-	+	+	-

Table 2.2. Plackett-Burman design matrix for N=12, k=11

Run	A	B	C	D	E	F	G	H	I	J	K
1	1	-1	1	-1	-1	-1	1	1	1	-1	1
2	1	1	-1	1	-1	-1	-1	1	1	1	-1
3	-1	1	1	-1	1	-1	-1	-1	1	1	1
4	1	-1	1	1	-1	1	-1	-1	-1	1	1
5	1	1	-1	1	1	-1	1	-1	-1	-1	1
6	1	1	1	-1	1	1	-1	1	-1	-1	-1
7	-1	1	1	1	-1	1	1	-1	1	-1	-1
8	-1	-1	1	1	1	-1	1	1	-1	1	-1
9	-1	-1	-1	1	1	1	-1	1	1	-1	1
10	1	-1	-1	-1	1	1	1	-1	1	1	-1
11	-1	1	-1	-1	-1	1	1	1	-1	1	1
12	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1

The design matrix is obtained by writing the appropriate row in Table 2.1 as a column (or row). A second column (or row) is then generated from this first one by moving the elements of the column (or row) down (or to the right) one position and placing the last element in the first position. A third column (or row) is produced from the second similarly, and the process continues until column (or row) k is generated. A row of minus signs is then added, completing the design.

In practice, two-level fractional factorial designs with $N=4, 8, 16$ and 32 runs are highly useful [34]. The Plackett-Burman design has been used as a screening experiment in this thesis. This will be discussed later in this chapter.

2.2.6. Three-Level Fractional Factorial Designs

The two-level series of factorial designs and fractional factorial designs are widely used in industrial research and development. There are some extensions and variations of these designs that are occasionally useful, such as the three level designs. The 3^k factorial design is a factorial arrangement with k factors each at three levels. The three levels of the factors will be referred to as low (-), intermediate (0) and high (+1) levels. For example; in a 3^2 factorial design which simply has two factors, where x_1 represents the factor A and x_2 represents the factor B, a regression model relating the response y to x_1 and x_2 can be written as

$$y = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_{12} x_1 x_2 + \beta_{11} x_1^2 + \beta_{22} x_2^2 + \varepsilon \quad (2.3)$$

It is noteworthy that, an addition of a third factor level allows the relationship between the response and the design factors to be modeled as a quadratic. This design is certainly a possible choice by an experimenter who is concerned about curvature in the response function. However, the 3^k design is not the most efficient way to model a quadratic relationship, the response surface designs are strong alternatives.

A number of different robust three-level design procedures have been proposed; these differ in their details but usually not very much in their conclusions [34, 35]. The

Box-Behnken design has been used in this thesis as a three-level design. The details of the method will be given next.

2.2.6.1. The Box-Behnken Design

The Box-Behnken design is a three-level fractional factorial design method. It is usually very efficient in terms of the number of required runs. It has been used in the thesis for this fact as well as for its simplicity.

As mentioned above, three-level designs are not usually the most efficient way for obtaining curvatures in the response function. The Response Surface Methodology is a powerful method for this purpose and will be discussed next.

2.2.7. The Response Surface Methodology

Response Surface Methodology is a collection of mathematical and statistical techniques that are useful for modeling and analysis of problems in which a response of interest is influenced by several variables and the objective is to optimize this response. The response is usually represented graphically by a surface.

In most Response Surface Methodology problems, the form of the relationship between the response and the independent input variables is unknown. Thus, the first step in Response Surface Methodology is to find a suitable approximation for the true functional relationship between y and the set of independent variables. Usually, a low-order polynomial in some region of the independent variables is employed. If the response is well modeled by a linear function of the independent variables, then the approximating function is the first-order model:

$$y = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \dots + \beta_k x_k + \varepsilon \quad (2.4)$$

If there is curvature in the system, then a polynomial of higher degree must be used, such as the second-order model:

$$y = \beta_0 + \sum_{i=1}^k \beta_i x_i + \sum_{i=1}^k \beta_{ii} x_i^2 + \sum_{i \leq j} \beta_{ij} x_i x_j + \varepsilon \quad (2.5)$$

Almost all Response Surface Methodology problems utilize one or both of these models. It is unlikely that a polynomial model will be a reasonable approximation of the true functional relationship over the entire space of the independent variables, but for a relatively small region they usually work quite well.

The method of least squares is used to estimate the parameters in the approximating polynomials. The response surface analysis is then done in terms of the fitted surface. If the fitted surface is an adequate approximation of the true response function, then analysis of the fitted surface will be approximately equivalent to the analysis of the actual system. The model parameters can be estimated most efficiently of proper experimental designs which are used to collect the data [34, 35]. The selection of appropriate designs for fitting response surfaces will be discussed next.

2.2.7.1 Experimental Designs for Fitting Response Surfaces

Fitting and analyzing response surfaces is greatly facilitated by the proper choice of an experimental design. When selecting a response surface design, some of the features of a desirable design could be itemized as follows [34, 35]:

- 1- Provides a reasonable distribution of data points, hence information, throughout the region of interest.
- 2- Allows model adequacy, including lack of fit.
- 3- Allows designs of higher order to be built up sequentially.
- 4- Provides an internal estimate of error.
- 5- Does not require a large number of runs.
- 6- Does not require too many of the independent variables.

Note that the Box-Behnken design, discussed previously, is a response surface design for fitting the second-order model and the number of runs required is quite efficient.

2.3. The Statistical VLSI Design Methodology

Given the SMOS model and the mathematical background on statistical techniques to build the empirical model to represent the circuit under consideration, it is now possible to describe the methodology used in the thesis. The SMOS model implemented into the simulation environment includes the random variations to the design process.

The methodology will help make a robust design, with the aid of statistical techniques, such as Design of Experiments and Response Surface Methodology. Design of Experiments is used to build a systematic way to obtain the empirical model representation of the circuits, and Response Surface Methodology is used to characterize the relationship between the input variables and the output performance of this empirical model. Both techniques were explained in detail in the previous sections.

Figure 2.6 shows the complete block diagram of the statistical design methodology.

Design of Experiments, a widely used systematic method for experiment planning, is applied to make the experiments in an efficient way. To apply Design of Experiments to a circuit modeling task, the designer should understand the problem to be solved and recognize the input variables that affect the response under study. Based on the number of input variables, experimental cost and accuracy requirement of the model, the level and the method of experiment can be chosen.

The methodology will be applied once the initial circuit design is complete. Before starting to run the experiments, the level of the experiments and the range for the input variables should be determined. The common approach for the selection of levels, will be to initially use a two-level experiment, and once the significant transistors are screened out, to switch for a three-level model building experiment, to make a more thorough examination of the input variables. The ranges will also be determined before starting the methodology. A two-level experiment will require two values; a minimum and a maximum value, for the area of each transistor. The choice of these values will be left to the designer. The final empirical model will be valid between these values of the areas, since each experiment will be run within these ranges.

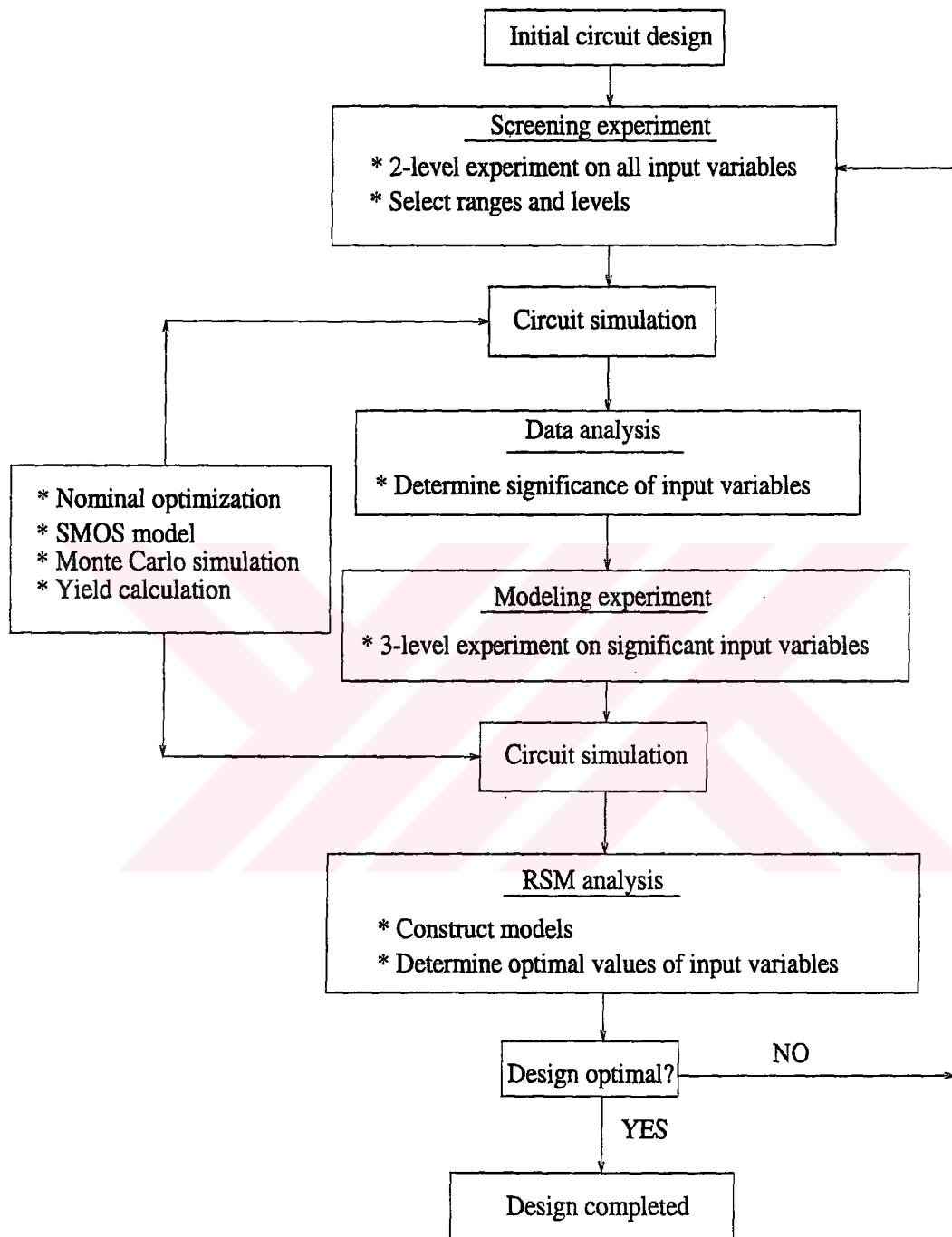


Figure 2.6: The complete statistical design methodology

Once the level and ranges are defined, the design will proceed with the first step of the methodology. The Plackett-Burman experiment will be run to screen out the most contributing transistors. The effect of each input variable, V_i , is indicated by the sum of squares (SS) as

$$SS(V_i) = (N/4) [\text{avg } y(V_i=+1) - \text{avg } y(V_i=-1)]^2 \quad (2.6)$$

where -1 and +1 represent the low and high levels, respectively, N is the number of runs, and y is the output performance. Depending on the specified cut off point, the variables whose SS constitutes a certain value of the total SS are considered in the second step of design. As an example; if 5% is the cut off point, the variables whose SS constitutes 95% of the total SS are taken to the second step. These transistors will be the main focal point once they are obtained. The designer will concentrate on optimizing only these transistors, while knowing the fact that the remaining transistors are not affecting the circuit performance. The selection of the cut off point is a decision that is given by the designer.

The SS values and the contribution of each input variable is calculated with the help of a computer program written in the C programming language. The results of the Plackett-Burman screening experiment are applied as the input of the program, and the output is the SS values and hence the contributions of each input variable. The C program is given in Appendix B, in the floppy disk attached to the thesis.

The second step of the methodology is a three-level model building experiment, with -1, 0, and +1 representing the three levels of design variables. A Box-Behnken design is suitable for this task, due to its ability to construct a full quadratic model. The results of the Box-Behnken design are analyzed and fitted to a polynomial model using the regression method. The regression method fits the data into a polynomial equation with the least squares algorithm. The equation consists of a constant term, linear terms, quadratic terms, and the interaction terms, as shown in equation (2.5). Each term will have a “T” (stands for the first letter of the word target) value, which will determine the significance of the terms. The rule of thumb for determining the statistical significance is to check if the “T” value is between the values -0.5 and 0.5. Any term in the empirical

model which has a “T” value between these values will be considered as statistically insignificant, and will be ignored and excluded from the final empirical formula.

The final step of the statistical design process is to plot the relationship between the input variables and the output performance, using Response Surface Methodology. A statistical software tool, Minitab [36], is used for obtaining the response surfaces. The program will give the “T” values of each term, and will also provide information on the reliability of the empirical model. The Box-Behnken results are applied to this program in order to construct the empirical model. The fitness of the empirical model is indicated by the regression coefficient, R^2 , which explains how good the model is by comparing the overall model and the predicted model. A perfect fit should have $R^2=1$. Response surfaces will help to visualize the model.

The statistical MOS model is used together with statistical design techniques, as explained in this chapter, in the above methodology, to make a robust design of the circuits described in Chapter 3. Chapter 4 will give the application of this method to those circuits, while providing simulation and experimental results.

3. LOW VOLTAGE LOW POWER ANALOG VLSI CIRCUITS

The need for the robust design of low voltage low power CMOS analog VLSI circuits is tremendously growing. There are three main driving forces that are pushing this growth:

- 1- Technology-driven forces
- 2- Design-driven forces
- 3- Market-driven forces

Technology-driven forces come from the reduction of the minimum feature size to scale down the chip area. Scaling down the transistor size can then integrate more circuit components in a single chip area and lower the cost. Also, smaller geometry usually lowers the parasitic capacitances, which means higher operating speed and lower power consumption. A decrease in MOS transistor size means reduced gate oxide thickness as well as reduced channel length. As a MOS transistor has a thinner gate oxide, in order to prevent the transistor from breakdown because of the higher electrical field across the gate oxide and to ensure its reliability, the power supply voltage is necessary to be reduced.

With the reduction of the device minimum feature size, millions of transistors can be fabricated on the same chip. This will result in a tremendous power consumption and cause excessive heating, which leads to the design-driven forces. Usually most of the chip area is occupied by the digital circuits and the average power consumption for digital circuits is proportional to the square of the power supply voltage. Thus, decrease

of the supply voltage reduces the power consumption in a significant amount. In analog circuits, however, reducing the supply voltage does not always mean lower power dissipation, hence, new design techniques for low power analog circuits are necessary to be developed.

The market-driven forces are noteworthy; e.g., current trends indicate that wireless mobile information technology within the next couple of decades will simply encompass the way of working, purchasing, playing, seeking service, purchasing products, by providing complete freedom of location to the individual. The individual demand for internet services, wireless cable television distribution, and information technology implies the development of broadband wireless mobile communications systems against current technology limits, such as the supply voltage and power dissipation.

All the above factors contribute to the necessity of low voltage and low power circuit solutions. Many applications which require reduced supply voltage and low power consumption are based on analog/digital, mixed-signal VLSI systems. The current trends of higher level of integration is leading to complete mixed-signal systems on a chip. One of the most important issues in mixed-signal design is the yield loss due to the analog portion of the chip. In most cases, the analog part will be much smaller than the digital portion, however, the analog part very much affects the overall yield of the chip. Therefore, it is important to make robust designs, to make sure that the yield loss due to analog components are minimized, such that it has little effect on the yield of the mixed-signal chip.

The main contribution of this thesis is the robust design methodology; using statistical models and techniques, to make a robust design of analog circuits. The statistical design of the analog circuits is demonstrated in Chapter 4, while this chapter describes the eight analog circuits that are statistically examined in the thesis. The circuits are selected among those which are subject to attention recently. The transconductor and multiplier circuits, however, are new designs for the thesis. The strategy behind these new designs are emphasized in the next page. All circuits are not the only examples of their types, and not the only circuits used for their purpose, but they certainly are one of the most popular, and recently used in several areas.

The first two circuits are analog CMOS cells which were previously designed for low voltage and low power applications. Both of the cells have a square-law characteristic. The description of these cells are given in detail.

The next four analog circuits, two transconductors and two multipliers, are newly designed for this thesis, and all four use the first two cells as a main building block, hence, understanding the basic principles of the low voltage and low power cells will lead to a better understanding of the transconductor and multiplier circuits.

One discussion is made for analog circuits being programmable as in the digital area. The long range goals are to make analog circuits programmable, and to realize applications involving analog computation. The goal is to come up with an analog design methodology similar to the one used for digital circuits, and take advantage of the basic building blocks. The low voltage and low power cells of this thesis are referred to as the basic building blocks, and the transconductor and multipliers are the circuits that take advantage of the building blocks, thus, the main effort is put when building the cells, and the cells are put together to build the transconductor and multiplier circuits.

Fully integrated continuous time circuits can be realized in MOS technology by using MOS transistors operating in the triode region. MOS transistors used in filter applications for implementing linear resistors, suffer from nonidealities causing signal distortion such as body effect, mobility variation, device mismatch, etc. It was demonstrated using a strong inversion MOS model, that a four-MOSFET structure fully suppresses the body effect related even- and odd-order terms. However, recent works question the widely accepted superiority of this structure. The result of the discussion is important because the supposed linearity properties of the four-MOSFET structure is served to justify its use in several recent applications. Therefore, it is of extreme importance to statistically examine the circuit.

Digital-to-analog (D/A) converters interface the digital output of signal processors with the analog world, therefore, it is an essential function in data processing systems. The linearity of the D/A converter strongly depends on the accuracy of the reference multiplication or division employed to generate the output levels. The three electrical quantities, voltage, current and charge can be multiplied or subdivided using resistor

ladders, current-steering circuits, and switched capacitor circuits, respectively. In this work the current division technique is used to divide the reference current in order to provide binary weighting, for a 10-bit example.

The four-MOSFET structure and the 10-bit current division network prove the importance of statistically examining circuits to obtain the quantitative effect of mismatch between transistors, as well as the statistical design of low voltage and low power circuits.

All the above circuits were simulated using the MOSIS 2 μ m Level-2 n-well process parameters. The model parameters are listed in Appendix C. The power supply voltage for all circuits is 3V. All simulations were done using APLAC. The four-MOSFET structure and 10-bit current division network was fabricated through the MOSIS 2 μ m n-well process, experimental results will be given for these circuits.

3.1. Low Voltage and Low Power CMOS Square-Law Composite Cells

3.1.1. Low Voltage CMOS Square-Law Composite Cell

The low voltage square-law CMOS cell is described in this section. However, before going into the details of the cell, the reasons and the necessity of designing the low voltage and low power cells will be discussed.

The reasons of designing these cells go back to the single MOS transistor (Figure 3.1(a)). The single MOS transistor exhibits the square-law characteristic on the gate-source voltage. However, the low input impedance at the source of the transistor limits the applicability of the single transistor. The conventional composite transistor [37], given in Figure 3.1(b) was proposed in the late 1980s as a solution for this problem.

The circuit has one NMOS and one PMOS transistor placed in series. V_g is the equivalent gate voltage and V_s is the equivalent source voltage, and the high input impedance terminals control the current flow through the transistors. However, the conventional composite transistor has a high equivalent threshold voltage, given by

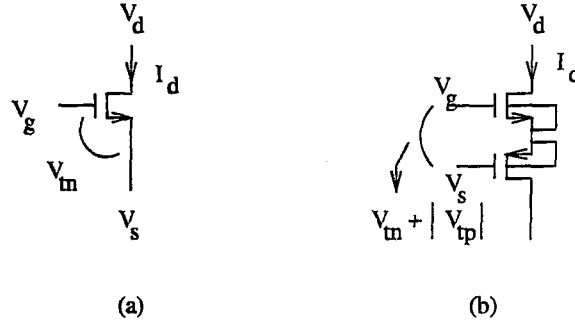


Figure 3.1: a) Single MOS transistor, b) Conventional composite transistor

$V_{Teq} = V_{Tn} + |V_{Tp}|$, where V_{Tn} and V_{Tp} are the threshold voltages of the NMOS and PMOS transistors, respectively, thus, making the threshold voltage almost twice as a single MOS transistor. This fact makes the circuit unsuitable for low voltage applications.

The low voltage square-law CMOS cell [38] was designed to overcome this drawback of the conventional composite transistor using the same idea. The currents flowing through both the NMOS and PMOS transistors are the same in the conventional composite transistor, which is given by $I_{dn} = I_{dp} = I_d$ in Figure 3.2(a). The sources of the transistors are connected to each other, and the condition $V_g - V_s > V_{Tn} + |V_{Tp}|$ should be satisfied, to keep the transistors in the on-state, which makes the range of the signal very small.

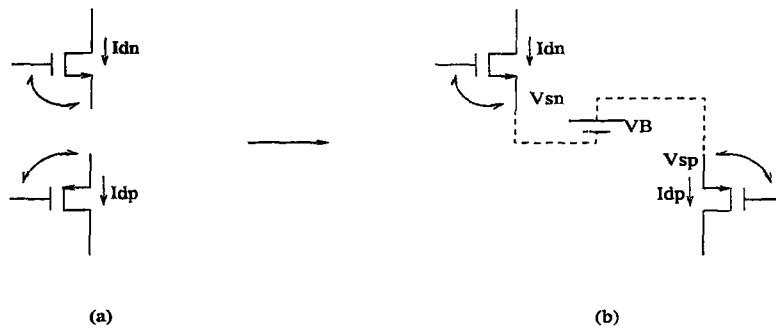


Figure 3.2: The basic idea of a) The conventional composite transistor, b) The low voltage square-law CMOS cell

The goal is to use the same idea but to reduce the equivalent threshold voltage, hence make the design suitable for low voltage applications. This could be done by adding a bias voltage, V_B , between the sources of the two transistors, instead of connecting them to each other. This will reduce the equivalent threshold voltage and the condition to keep the transistors on will be $V_g - V_s > V_{Tn} + |V_{Tp}| - V_B$, where the right-hand side value is less than the previous. This idea is illustrated in Figure 3.2(b).

The simplest way to accomplish this idea is to use a level shifter (Figure 3.3).

Δ , in Figure 3.3, is the shifted voltage value by the level shifter, which is basically the voltage difference between the voltages V_1 and V_2 .



Figure 3.3: The idea of using a level shifter to reduce the equivalent threshold voltage

The implementation of the above described idea to build a low voltage cell [38] is illustrated in Figure 3.4.

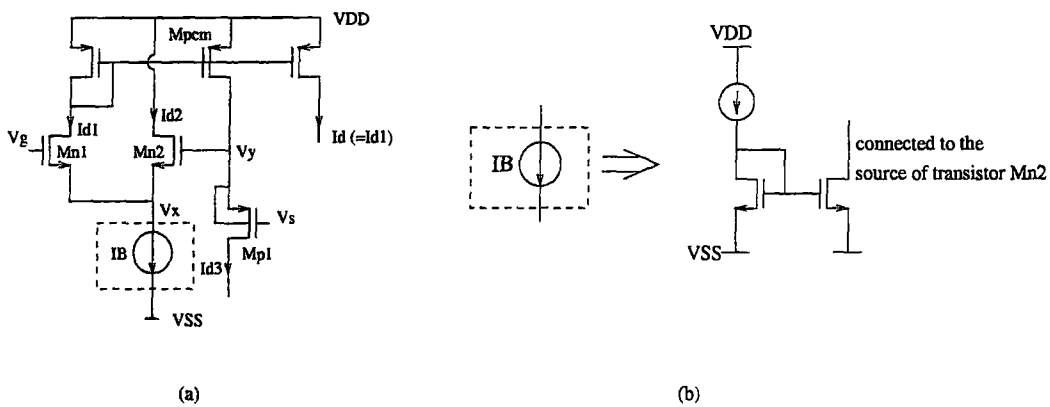


Figure 3.4: a) Low voltage CMOS square-law composite cell, b) Representation of the current source

Transistors M_{n1} and M_{p1} are the NMOS and PMOS transistors of the conventional composite transistor. The currents flowing through these transistors should be the same, and this is done by using a current mirror in the circuit. M_{pcm} is the group of PMOS transistors forming the current mirror to ensure that the currents flowing through transistors M_{n1} and M_{p1} are equal, by taking the current through M_{n1} and mirroring it to M_{p1} . M_{n2} and I_B form a level shifter to decrease the value of the effective threshold voltage. The drain currents I_{d1} through I_{d3} shown in Figure 3.2 are expressed as

$$I_{d1} = \frac{K_{n1}}{2}(V_g - V_x - V_{Tn})^2 \quad (3.1)$$

$$I_{d2} = \frac{K_{n2}}{2}(V_y - V_x - V_{Tn})^2 \quad (3.2)$$

$$I_{d3} = \frac{K_{p1}}{2}(V_y - V_s - |V_{Tp}|)^2 \quad (3.3)$$

Using the fact that $I_{d1} = I_{d3} = I_d$ and $I_{d1} + I_{d2} = I_B$, equations (3.1) through (3.3) can be rewritten in the form of

$$V_g - V_x = \sqrt{\frac{2I_d}{K_{n1}}} + V_{Tn} \quad (3.4)$$

$$V_y - V_x = \sqrt{\frac{2(I_B - I_d)}{K_{n2}}} + V_{Tn} \quad (3.5)$$

$$V_y - V_s = \sqrt{\frac{2I_d}{K_{p1}}} + |V_{Tp}| \quad (3.6)$$

The drain current equation for the low voltage CMOS square-law composite cell can be then written as

$$I_d = \frac{K_{eq}}{2}(V_{gs} - V_{Teq})^2 \quad (3.7)$$

where K_{eq} and V_{Teq} is the equivalent transconductance parameter and the equivalent threshold voltage, respectively, expressed as

$$K_{eq} = \left(\frac{1}{\sqrt{K_{n1}}} + \frac{1}{\sqrt{K_{p1}}} \right)^{-2} \quad (3.8)$$

$$V_{Teq} = |V_{Tp}| - \sqrt{\frac{2(I_B - I_d)}{K_{n2}}} \quad (3.9)$$

It is clear that the threshold voltage is much less than the threshold voltage of the conventional composite transistor, hence the goal of designing a cell which has a square-law characteristic, and which is suitable for low voltage applications is reached. However, the threshold voltage equation given by equation (3.9) quickly reflects the drawback of this cell; that is, the threshold voltage is a function of the drain current, I_d . Hence, the threshold voltage is varying with the input voltage causing distortion.

One way to avoid this is to keep the bias current, I_B , much larger than I_d , so that I_d in equation (3.9) will be canceled, thus, the threshold voltage equation can be simplified as

$$V_{Teq} = |V_{Tp}| - \sqrt{\frac{2I_B}{K_{n2}}} \quad (3.10)$$

which is now a constant value and still much less than the equivalent threshold voltage of the conventional composite transistor. However, the condition $I_B \gg I_d$ means that it is not possible to arbitrarily reduce the bias current, I_B , to obtain an improved power consumption, which brings a trade-off to the cell, between low voltage operation and low power dissipation. This trade-off is also the main drawback of this cell and will be reflected to the circuits that are using the cell as a main building block. It is possible to overcome this trade-off between low voltage operation and low power dissipation, though, and the next section will describe another cell, again using the same original

idea with the conventional composite transistor, with a method to keep the threshold voltage constant.

Finally, the DC transfer curve of the low voltage square-law CMOS cell is given in Figure 3.5.

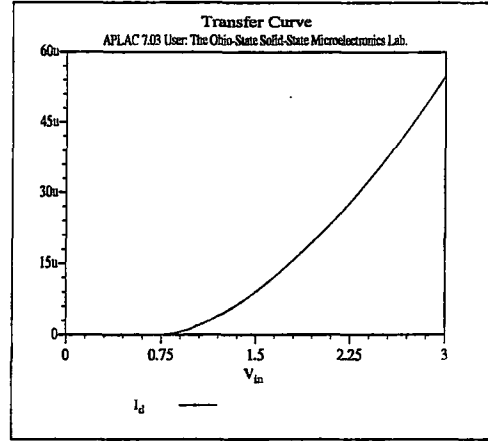


Figure 3.5: DC transfer curve of the low voltage square-law CMOS cell

The W/L values of the transistors in the circuit are given in Table 3.1.

Table 3.1: W/L values of the transistors of the low voltage square-law CMOS cell. The bias current is $I_B=120\mu A$

Transistors	M_{n1}	M_{n2}	M_{pcm}	M_{p1}	M_{ncs}
W/L	5/2	100/2	150/3	15/2	38/3

M_{ncs} represents the transistors that were used for I_B , as shown in Figure 3.4(b).

Simulations were done for the source voltage of $V_s=0.5V$, and the gate-source voltage of $V_{gs}=2V$. The bias current was $120\mu A$, and the supply voltage was $3V$. The simulations were done using APLAC, and the netlist is given in Appendix D.

3.1.2. Low Voltage Low Power CMOS Square-Law Composite Cell

As mentioned in the previous section, the drawback of the low voltage cell is that it simply has to satisfy the condition, $I_B \gg I_d$, for a constant threshold voltage, which brings a trade-off between low voltage operation and low power dissipation to the circuit. The problem is that the current flowing through transistor M_{n1} , in Figure 3.4, is $(I_B - I_d)$, thus varying, which means that the V_{GS} of transistor M_{n1} is varying with current. The current flowing through transistor M_{n1} should be constant, even for a varying I_d .

One way to achieve this is to put a constant current source, I_B , to the drain of transistor M_{n1} , as shown in Figure 3.6.

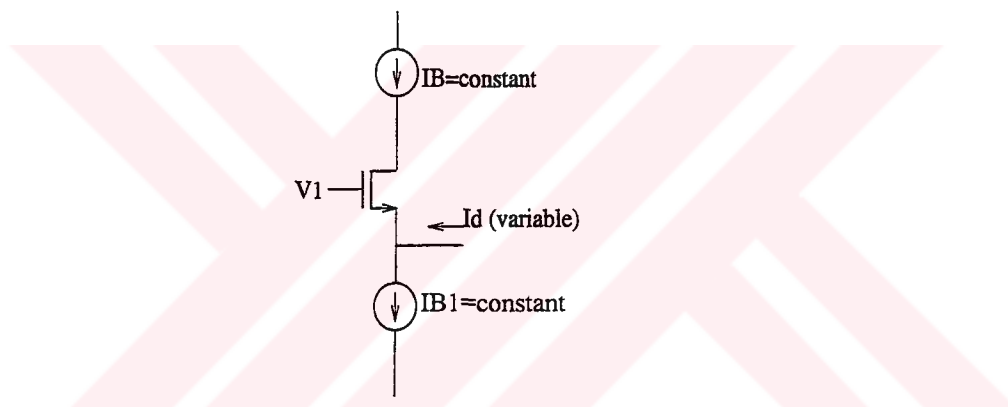


Figure 3.6: Constant current source at the drain of the transistor, for keeping the drain current of the transistor constant

In Figure 3.6, the current going to the drain of the transistor is a constant I_B , and the current going out from the source is a constant I_B as well, whereas the variable drain current, I_d , is also going into the source of the transistor, which brings a contradiction. A simple way to avoid this is to make the I_B (connected to the source of the transistor) variable, e.g., if I_d increases, I_B will automatically increase to accommodate this change of current. Two NMOS transistors will be connected to the circuit, which will take place of I_B (the one connected to the source of the transistor), as shown in Figure 3.7.

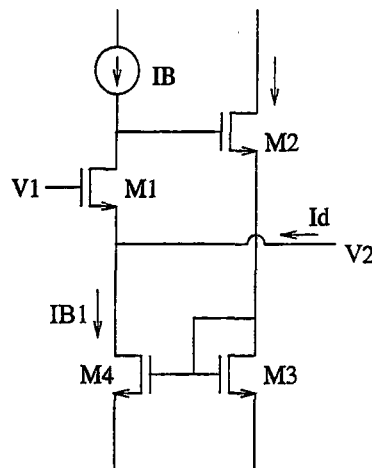


Figure 3.7: The feedback loop that will keep the threshold voltage constant without having to satisfy any condition for the bias current

I_B is coming from the current mirror transistors M_3 and M_4 . It is mirrored by the current mirror and this current should be dependent on the drain current, I_d . This is accomplished by the feedback transistor M_2 ; if I_d increases the current flowing through transistor M_2 should increase, and if I_d decreases the current flowing through transistor M_2 should also decrease. The next paragraph explains how this is done with the help of the illustration in Figure 3.8.

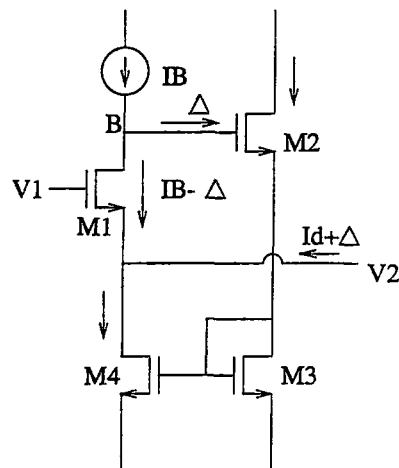


Figure 3.8: The description of the feedback loop

Let's assume I_d increases, and let's also assume that the drain current of transistor M_4 is constant. In that case, the current flowing through transistor M_1 is reduced to $(I_B - \Delta)$. Above point B, in Figure 3.8, the current source has a current of I_B , and the current flowing through M_1 is $(I_B - \Delta)$, thus, an extra current has to flow through the large output impedance at point B. This extra current increases the gate voltage of transistor M_2 , which will result in an increase in the current through M_2 , hence, an increase in the currents flowing through M_3 and M_4 , which will cause the current I_{B1} in Figure 3.6 to increase and accommodate the extra current.

The implementation of the feedback loop given in Figure 3.8 is illustrated in Figure 3.9 [39].

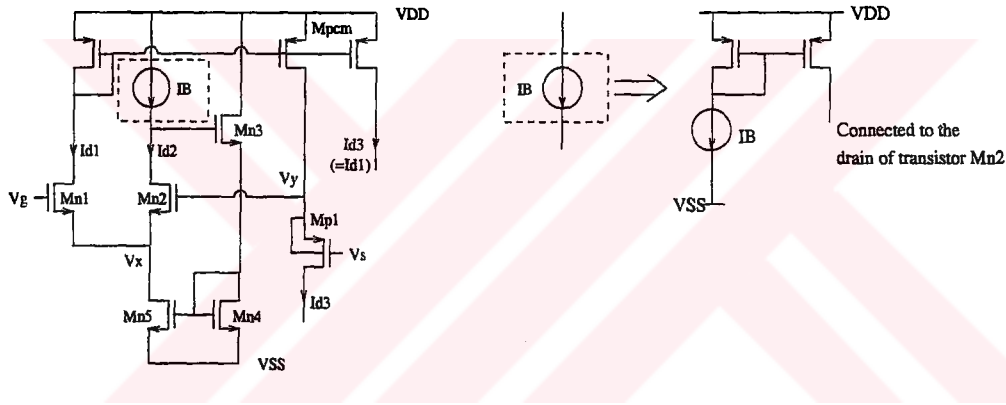


Figure 3.9: a) Low voltage low power CMOS square-law composite cell, b) Representation of the current source

Transistors M_{n1} and M_{p1} are, again, the NMOS and PMOS transistors of the conventional composite transistor, and the current mirror transistors, namely M_{pcm} , help keep the currents flowing through both transistors the same. The feedback loop consists of transistors M_{n2} , M_{n3} , M_{n4} and M_{n5} , and together with the bias current, I_B , it keeps the drain current of transistor M_{n2} equal to I_B .

The drain currents I_{d1} through I_{d3} shown in Figure 3.9 are expressed as

$$I_{d1} = \frac{K_{n1}}{2}(V_g - V_x - V_{Tn})^2 \quad (3.12)$$

$$I_{d2} = \frac{K_{n2}}{2}(V_y - V_x - V_{Tn})^2 \quad (3.13)$$

$$I_{d3} = \frac{K_{p1}}{2}(V_y - V_s - |V_{Tp}|)^2 \quad (3.14)$$

Since $I_{d1} = I_{d3} = I_d$ and $I_{d2} = I_B$, the above equations can be rewritten as

$$V_g - V_x = \sqrt{\frac{2I_d}{K_{n1}}} + V_{Tn} \quad (3.15)$$

$$V_y - V_x = \sqrt{\frac{2I_B}{K_{n2}}} + V_{Tn} \quad (3.16)$$

$$V_y - V_s = \sqrt{\frac{2I_d}{K_{p1}}} + |V_{Tp}| \quad (3.17)$$

Substituting equations (3.15) and (3.17) in equation (3.16) will give

$$I_d = \frac{K_{eq}}{2}(V_{gs} - V_{Teq})^2 \quad (3.18)$$

where K_{eq} and V_{Teq} are the equivalent transconductance parameter and the equivalent threshold voltage, respectively, expressed as

$$K_{eq} = \left(\frac{1}{\sqrt{K_{n1}}} + \frac{1}{\sqrt{K_{p1}}} \right)^{-2} \quad (3.19)$$

$$V_{Teq} = |V_{Tp}| - \sqrt{\frac{2I_B}{K_{n2}}} \quad (3.20)$$

Equation (3.20) shows that the circuit no longer has to satisfy $I_B \gg I_d$, as I_d can be increased regardless of I_B . The trade-off between low voltage operation and low power dissipation for the previous cell has been overcome in this circuit.

The DC transfer curve of the low voltage low power square-law CMOS cell is given in Figure 3.10, for a bias current of $I_B=120\mu A$, $V_s=0.5V$ and $V_{gs}=2V$, and for a supply voltage of 3V.

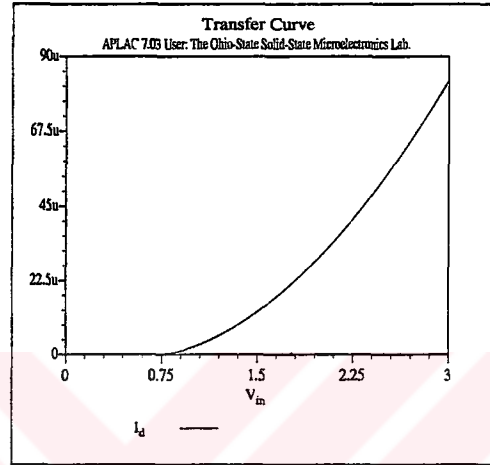


Figure 3.10: The DC transfer curve of the low voltage low power square-law CMOS cell

The W/L values of the transistors in the low voltage low power square-law CMOS cell are given in Table 3.2.

Table 3.2: W/L values of the transistors of the low voltage low power square-law CMOS cell. The bias current is $I_B=120\mu A$

Transistors	M_{n1}	M_{n2}	M_{pcm}	M_{n3}	M_{p1}	M_{n4}, M_{n5}	M_{pcs}
W/L	5/2	100/2	150/3	500/2	15/2	38/3	150/3

M_{pcs} represents the transistors that were used for I_B , as shown in Figure 3.9(b). The simulations were done using APLAC, and the netlist is given in Appendix E.

3.1.3. Summary of the Square-Law CMOS Cells

Many applications which require reduced supply voltage and low power consumption are based on analog/digital mixed-signal VLSI circuits. A certain class of these circuits are basically composed of several cells which have a square-law characteristic. A single MOSFET fulfills this characteristic, however, the low input impedance at the source of the transistor limits the applicability of the single transistor solution. The conventional composite transistor was proposed as a solution for this problem. However, the conventional composite transistor is not suitable for low voltage applications because of its high equivalent threshold voltage. Recently, several new low voltage and low power CMOS square-law composite cells with two high impedance input terminals were proposed to achieve accurate signal processing with low power dissipation. The design and operation principles of two of these cells were described in detail, in the previous sections. Understanding the basic principles of the low voltage and low power cells will lead to a better understanding of circuits which use these cells as a main building block.

Two new transconductors and multipliers were built using the low voltage and low power cells. These circuits will be discussed next, after a brief introduction on linear transconductors.

3.2. Linear Transconductors

MOS transconductors are useful building blocks for the design of analog and mixed-signal systems. Such applications usually require very linear transconductance elements with a good high frequency capability. An elegant way to achieve a linear transconductor, starting with transistors in strong inversion and having a square-law behavior, is to use the difference of squares principle [40]. This principle states that given the variables A and B, the difference of the squares $(A+B)^2$ and $(A-B)^2$ is linear in A or B, that is

$$[(A+B)^2 - (A-B)^2] = 4AB \quad (3.21)$$

This principle can be used to arrive a linear relationship between the difference in the gate-source voltages of two transistors and the difference in their output currents. The realizations given in [37, 41, 42, 43] are based on using MOS transistors operating in the saturation region.

The new transconductors that will be introduced in the next two sections are using the low voltage and low power CMOS square-law cells of Section 3.1 as their main building block. Note that, when using these cells as a building block, the advantages and disadvantages of the cells will be also reflected to the circuits which are using them.

3.2.1. Transconductor Using the Low Voltage CMOS Square-Law Composite Cell

The transconductor using the low voltage CMOS square-law composite cell is illustrated in Figure 3.11 [44].

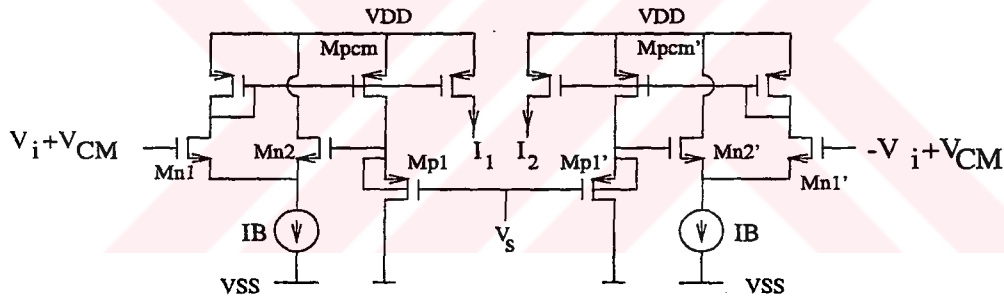


Figure 3.11: The transconductor using the low voltage CMOS square-law composite cell

The low voltage square-law CMOS composite cells are connected in such a way to build a transconductor. The circuit operates in the saturation region with a fully balanced input signal. It is preferable that analog circuits operate in the fully balanced mode, mainly because fully balanced circuits ensure high power supply rejection, improve linearity and increase dynamic range. The input voltages and the control voltage are applied to the NMOS and PMOS pair, respectively. The output differential current equation is derived by using the difference of squares principle:

$$I_1 - I_2 = K_{eq}(V_{gs1} - V_{Teq})^2 - K_{eq}(V_{gs1} - V_{Teq})^2$$

$$I_1 - I_2 = K_{eq}[(V_i + V_{CM} - V_s - V_{Teq})^2 - K_{eq}(-V_i + V_{CM} - V_s - V_{Teq})^2]$$

$$I_1 - I_2 = 4K_{eq}(V_{CM} - V_s - V_{Teq})V_i \quad (3.22)$$

Hence, the transconductance is given by

$$G_m = 4K_{eq}(V_{CM} - V_s - V_{Teq}) \quad (3.23)$$

where K_{eq} and V_{Teq} is the equivalent transconductance parameter and the equivalent threshold voltage, respectively.

Tunability is a very important parameter for transconductors. The transconductance is affected by the threshold voltage and transconductance parameter, which change with temperature (30% typical value). Thus, it is important for the transconductor to be tunable to compensate process and temperature variations. Note that, having the control voltage, V_s , in equation (3.23) allows the transconductance of the circuit to be electronically tuned.

The low voltage cell had a trade-off between low voltage operation and low power dissipation, hence, the transconductor will have the same trade-off as well, since it is using the cell as a main building block.

The DC transfer curve of the transconductor using the low voltage square-law CMOS cell is given in Figure 3.12.

The input voltage is applied to the NMOS transistors and is $V_i = \pm 0.3$ V and the common mode voltage is $V_{CM} = 2$ V. The control voltage is $V_s = 0.6$ V and the bias current is $I_B = 120 \mu A$. The transfer curve is obtained by sweeping V_s from 0.2 V to 0.6 V, with a 0.1 V increment. I_o is the output current defined as $I_o = I_1 - I_2$.

The netlist of the circuit is given in Appendix F.

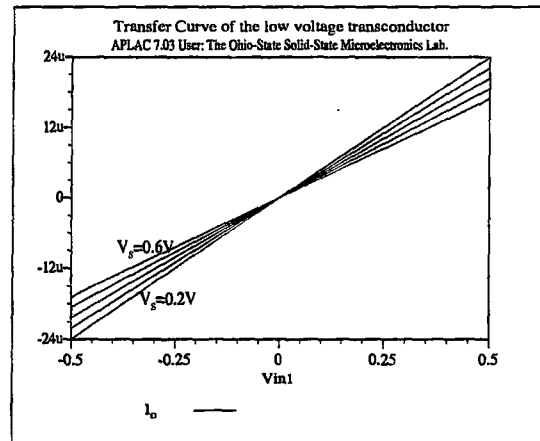


Figure 3.12: The DC transfer curve of the transconductor using the low voltage CMOS square-law composite cell

It is noteworthy that, the input voltage, V_i , can be applied either to the NMOS or the PMOS transistor, in which case the control voltage, V_s , will be applied to the other. In both cases the transconductance will be the same, however, because of the fact that NMOS transistors are faster than PMOS transistors, and also because the output path for the transconductor with inputs on the PMOS pair is longer than the other, the circuit will be faster when inputs are on the gates of the NMOS pair.

3.2.2. Transconductor Using the Low Voltage Low Power CMOS Square-Law Composite Cell

Figure 3.13 shows the transconductor [45] using the low voltage low power square-law CMOS composite cell as a building block. The trade-off between low voltage operation and low power dissipation is avoided with the use of the low voltage low power cell.

The main points of the low voltage transconductor that were emphasized in the previous section, are valid for this transconductor as well. The circuit operates in the saturation region with a fully balanced input signal. The inputs are applied to the NMOS pair and the control voltage, and V_s , is applied to the PMOS pair in the circuit. The transconductance of the circuit is derived by taking the difference of the output currents of each cell:

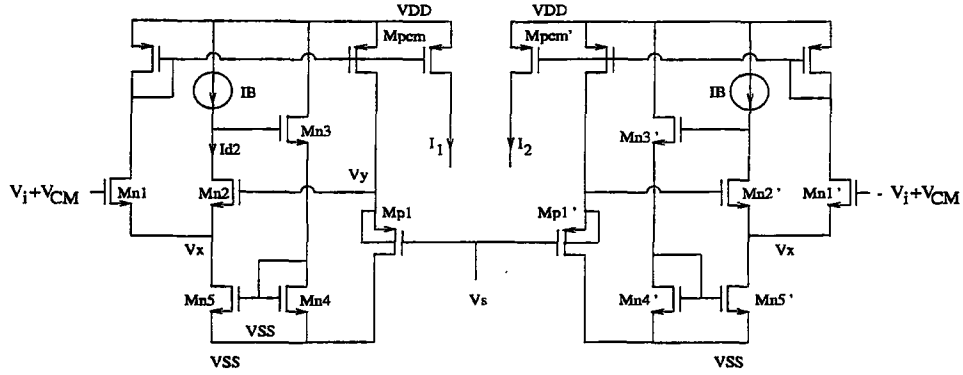


Figure 3.13: The transconductor using the low voltage low power CMOS square-law composite cell

$$G_m = 4K_{eq}(V_{CM} - V_s - V_{Teq}) \quad (3.24)$$

which is similar to equation (3.23).

Figure 3.14 shows the DC transfer curve of the transconductor using the low voltage low power square-law CMOS cell, where I_o is the output current and is defined by $I_o = I_1 - I_2$. The same biasing conditions that were applied to the previous transconductor is used to bias the low voltage low power transconductor: The input voltage is $V_i = \pm 0.3$ V, and is applied to the NMOS transistors of the transconductor. The common mode voltage is $V_{CM} = 2$ V. The control voltage is $V_s = 0.6$ V and the bias current is $I_B = 120 \mu A$. The transfer curve is obtained by sweeping the control voltage, V_s , from 0.2 V to 0.6 V, with a 0.1 V increment.

The netlist of the circuit is given in Appendix G.

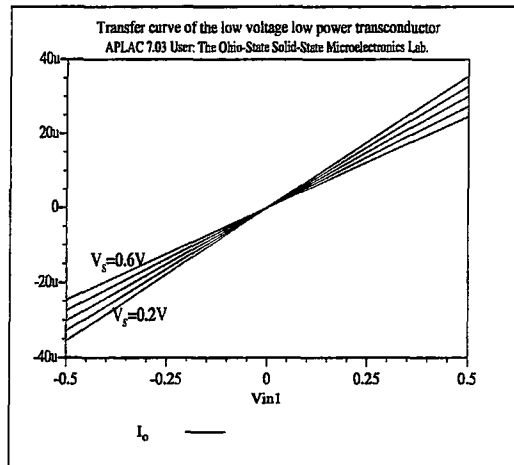


Figure 3.14: The DC transfer curve of the transconductor using the low voltage low power CMOS square-law composite cell

3.3. Analog Multipliers

Analog multipliers are essential building blocks found in a wide range of applications including communications, analog signal processing and neural networks. Multiplier designs have received much of the attention, and may be implemented in a variety of ways including the technique using the square-law characteristic of MOS transistors in the saturation region [46–49]. Many applications require linear multipliers and matching is very important to obtain highly linear multipliers no matter what the implementation is.

Two new multipliers which use the low voltage and low power square-law cells are introduced in this section.

$$I_4 = \frac{K_{eq}}{2}(V_2 - V_4 - V_{Teq})^2 \quad (3.29)$$

Substituting equation (3.26) through (3.29) into equation (3.25) will give the output current equation in terms of the input voltages:

$$I_o = K_{eq}(V_1 - V_2)(V_4 - V_3) \quad (3.30)$$

where K_{eq} is the equivalent transconductance parameter and V_1 , V_2 , V_3 and V_4 are the input voltages of the circuit. The input voltage range of the analog multiplier is usually restricted to a fraction of the power supply voltage, hence, it is convenient to express the input voltages in terms of a differential voltage superimposed as a common mode voltage:

$$V_1 = V_{CM1} + \frac{\Delta v_{12}}{2} \quad (3.31)$$

$$V_3 = V_{CM2} + \frac{\Delta v_{34}}{2} \quad (3.32)$$

$$V_2 = V_{CM1} - \frac{\Delta v_{12}}{2} \quad (3.33)$$

$$V_4 = V_{CM2} - \frac{\Delta v_{34}}{2} \quad (3.34)$$

where V_{CM1} and V_{CM2} are the input common mode voltages, and input differential voltages denoted by Δv_{12} and Δv_{34} are defined as

$$\Delta v_{12} = V_1 - V_2 \quad (3.35)$$

$$\Delta v_{34} = V_3 - V_4 \quad (3.36)$$

Figure 3.16 shows the transfer curve of the multiplier using the low voltage CMOS square-law composite cell.

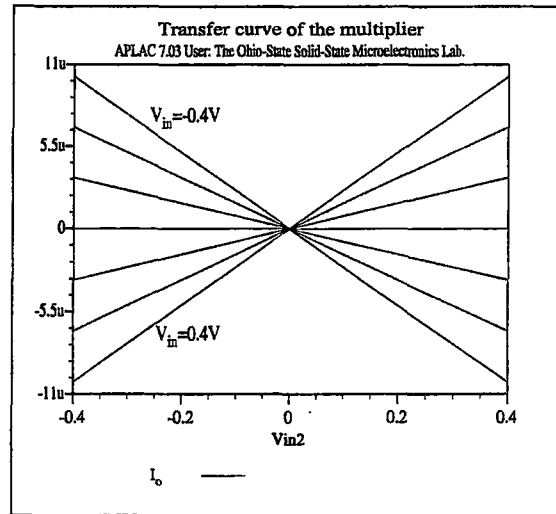


Figure 3.16: The DC transfer curve of the multiplier using the low voltage CMOS square-law composite cell

Simulations were done with APLAC, for a 3V supply voltage and a bias current of $I_B=120\mu A$. The input voltages are $\pm 0.3V$ for V_1 and V_2 , and V_3 and V_4 . The common mode voltages for the inputs V_1 and V_2 , and V_3 and V_4 are 2.4V and 0.6V, respectively. The netlist of the circuit is given in Appendix H.

Note that the trade-off between low voltage operation and low power dissipation exists for the multiplier, since the main block of the circuit has this trade-off.

3.3.2. Multiplier Using the Low Voltage Low Power CMOS Square-Law Composite Cell

Figure 3.17 shows the multiplier using the low voltage low power CMOS square-law composite cell [49].

Unlike the previously introduced multiplier, the circuit does not have a trade-off between low voltage operation and low power dissipation, since the circuit is a combination of four low voltage low power cells, and this cell overcomes this trade-off.

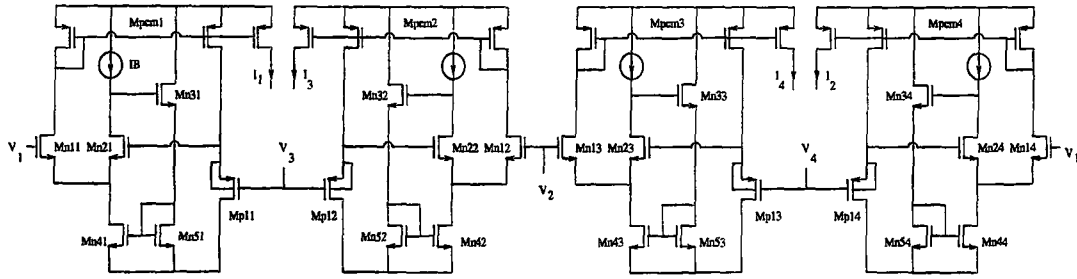


Figure 3.17: Multiplier using the low voltage low power CMOS square-law composite cell

It is possible proceed as in the previous multiplier circuit, to arrive to the output current of the circuit, in terms of the input voltages:

$$I_o = K_{eq}(V_1 - V_2)(V_4 - V_3) \quad (3.37)$$

The transfer curve of the circuit was obtained for the same biasing conditions used for low voltage multiplier. Simulations were made with APLAC, using a 3V supply voltage. The transfer curve of the multiplier using the low voltage low power CMOS square-law composite cell is given in Figure 3.18.

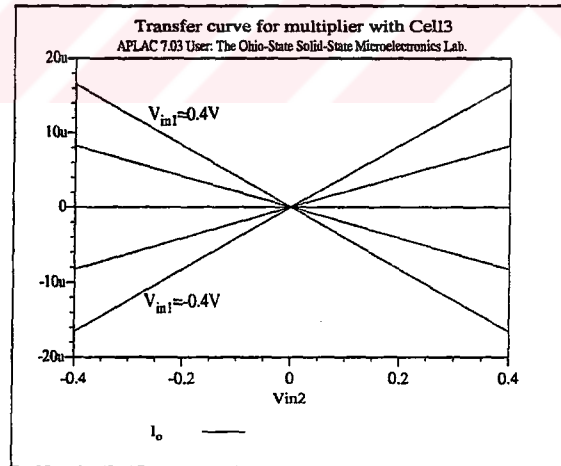


Figure 3.18: The DC transfer curve of the multiplier using the low voltage low power CMOS square-law composite cell

The netlist of the circuit is given in Appendix I.

3.4. The Four-MOSFET Structure and a Discussion for Nonlinearity Cancellation

Fully integrated continuous time circuits can be realized in MOS technology by using MOS transistors operating in the triode region. MOS transistors used in filter applications for implementing linear resistors suffer from nonidealities causing signal distortion such as body effect, mobility variation, device mismatch, etc.

Extensive research has been conducted on the fully balanced integrator with MOS resistors. It was demonstrated, using a strong inversion MOS model, that a four-MOSFET structure fully suppresses the even and odd-order nonlinearity terms [26, 27]. However, recent works question the widely accepted superiority of the four-MOSFET structure [28]. The result of the discussion is important because the supposed linearity properties of the four-MOSFET structure is served to justify its use in several recent applications [29, 30].

For exact cancellation of nonlinearities, exact transistor matching is needed, whereas, random variations may not always allow for exact matching of transistors. Most of the previously done four-MOSFET structure works have not considered random variations, hence, it is important to quantitatively determine the effect of mismatches on nonlinearity cancellation.

The four-MOSFET structure is reviewed in this section.

3.4.1. Four-MOSFET Structure

The four-MOSFET structure is illustrated in Figure 3.19.

All transistors in the circuit are operating in the triode region. The output voltages V_{o1} and V_{o2} , must be equal, i.e. $V_{o1} = V_{o2} = V$, to achieve nonlinearity cancellation. The operation of the circuit depends on the perfect matching of transistors; any mismatch will cause distortion.

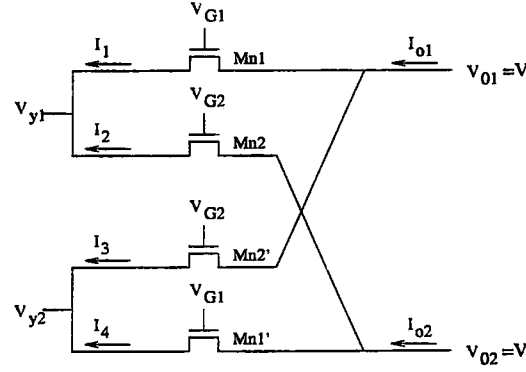


Figure 3.19: The four-MOSFET structure

The output current is given by

$$I_o = (I_1 + I_3) - (I_2 + I_4) \quad (3.38)$$

where I_1 , I_2 , I_3 and I_4 are triode region currents given by

$$I_1 = K_1 \left(V_{G1} - V_{y1} - V_T - \frac{1}{2}(V - V_{y1}) \right) (V - V_{y1}) \quad (3.39)$$

$$I_2 = K_2 \left(V_{G2} - V_{y1} - V_T - \frac{1}{2}(V - V_{y1}) \right) (V - V_{y1}) \quad (3.40)$$

$$I_3 = K_3 \left(V_{G2} - V_{y2} - V_T - \frac{1}{2}(V - V_{y2}) \right) (V - V_{y2}) \quad (3.41)$$

$$I_4 = K_4 \left(V_{G1} - V_{y2} - V_T - \frac{1}{2}(V - V_{y2}) \right) (V - V_{y2}) \quad (3.42)$$

Assuming perfect matching of the transistors will result in $K_1 = K_2 = K_3 = K_4 = K$. As equations (3.39) through (3.42) are placed in equation (3.38), the output current of the four-MOSFET structure is found as

$$I_o = K(V_{G1} - V_{G2})(V_{y2} - V_{y1}) \quad (3.43)$$

The transfer curve of the Four-MOSFET structure for the aspect ratios of $W/L=4/4$ and $W/L=20/4$ are shown in Figure 3.20.

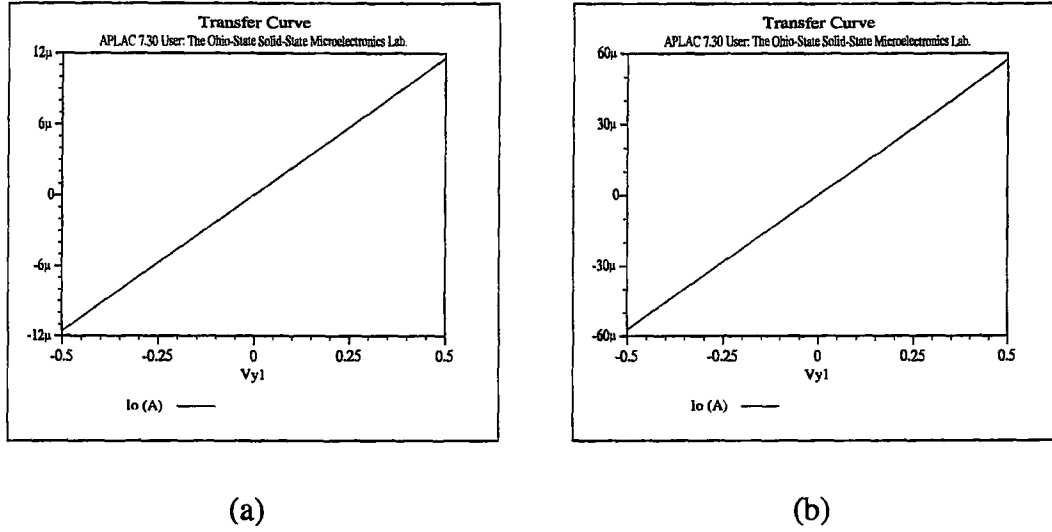


Figure 3.20: The DC transfer curve of the four-MOSFET structure (APLAC simulation results), for a) $W/L=4/4$, b) $W/L=20/4$

Simulations were done using APLAC, for a 3V supply voltage. The circuit is biased as $V_{o1}=V_{o2}=0.8V$, $V_{G1}=2.2V$, $V_{G2}=2.75V$, $V_{y1}=1.1V$ and $V_{y2}=0.5V$. The netlist is given in Appendix J.

The four-MOSFET structure was fabricated through the MOSIS $2\mu m$ process, using MOS transistor Level-2 model parameters, for the aspect ratios of $W/L=4/4$ and $W/L=20/4$. The experimentally found transfer curve for both aspect ratios are shown in Figure 3.21.

The experimental results are obtained with the help of the HP4145B parameter analyzer. Measurements were made on 4 tiny MOSIS chips, each one having 15 samples of the four-MOSFET structure, 7 samples for the aspect ratio of $W/L=4/4$ and 8 samples for aspect ratio of $W/L=20/4$. The results are discussed in Chapter 4.

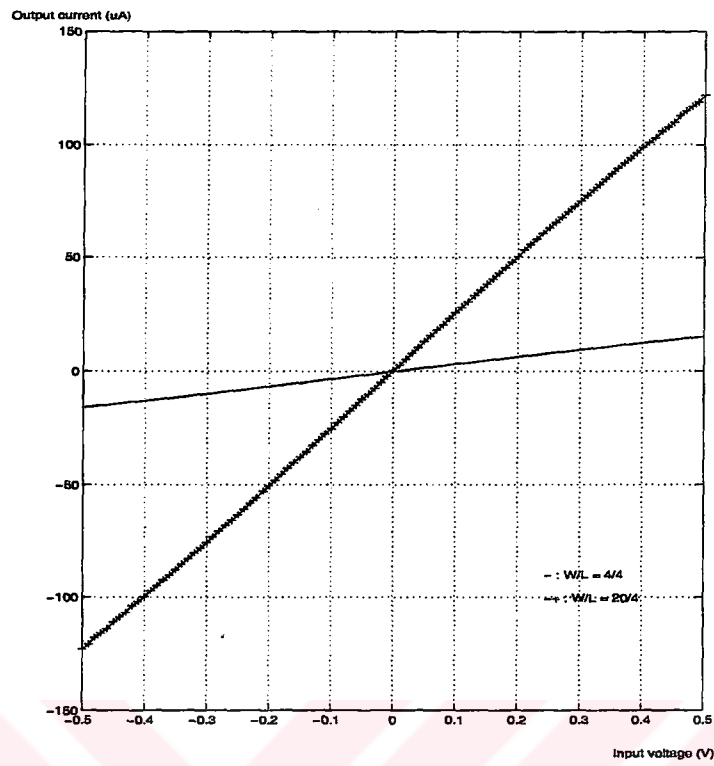


Figure 3.21: The DC transfer curve of the four-MOSFET structure (experimental results) for aspect ratios $W/L=4/4$ and $W/L=20/4$

3.5. D/A Converter Based on the Current Division Technique

Data conversion provides the link between the analog world and digital systems, and is performed by means of sampling circuits, A/D converters, and D/A converters. With the increasing use of digital computing and signal processing applications such as medical imaging, instrumentation, consumer electronics, and communications, the field of data conversion systems rapidly expanded over the past years [50, 51]. D/A converters interface the digital output of signal processors with the analog world, therefore, it is an essential function in data processing systems.

The main concentration in this thesis is on the linearity of the D/A converters. The linearity strongly depends on the accuracy of the reference multiplication or division employed to generate output levels. The three electrical quantities, voltage, current and charge can be multiplied or subdivided using resistor ladders, current-steering circuits, and switched capacitor circuits, respectively. In this work, a current division network will be used to divide the reference current in order to provide binary weighting, for a 10-bit example.

A technique for dividing currents accurately and linearly is useful for various kinds of analog signal processing applications. A common technique is to use resistors or capacitors for the linear and accurate division of current while using MOS transistors as switches or amplifying elements [52, 53].

The MOS transistor can be used for signal division, thus, eliminating the need for resistors or capacitors. Although an MOS transistor exhibits a nonlinear relationship between current and voltage, the current division function is inherently linear [54].

This section describes the 10-bit current division network and its operation principle.

3.5.1. The 10-bit Current Division Network

The 10-bit current division network is illustrated in Figure 3.22.

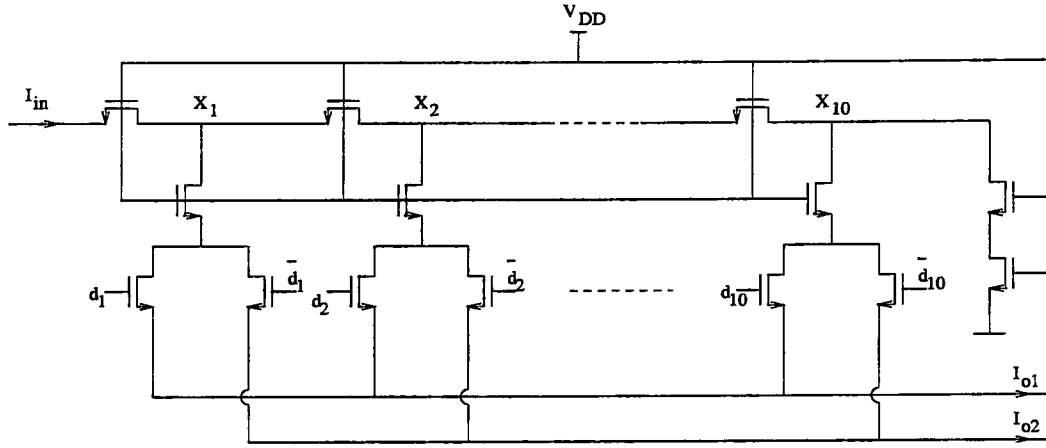


Figure 3.22: The 10-bit current division network

The input current, I_{in} , flowing towards node X_1 is divided equally into two as $I_{in}/2$ at this node. This current is flowing through one of the NMOS transistors, according to d_1 being logic 0 or logic 1. The current entering node X_2 has the value of $I_{in}/2$ and is equally divided as $I_{in}/4$. Again, this current is flowing through one of the NMOS transistors, so forth. The current value of $I_{in}/2^9$ will enter node X_{10} and this current will be divided having the value of $I_{in}/2^{10}$. This will lead to a general expression for the current as

$$I_i = I_{in} \times (2^{-i} d_i) \quad (3.44)$$

where I_i is the current value after being divided at node X_i , I_{in} is the input current, and d_i is the gate voltage of the NMOS transistors, either logic 0 or logic 1. The I_i values contribute to the output currents I_{o1} and I_{o2} [55] which are given by

$$I_{o1} = I_{in} \sum_{i=1}^{10} 2^{-i} d_i \quad (3.45)$$

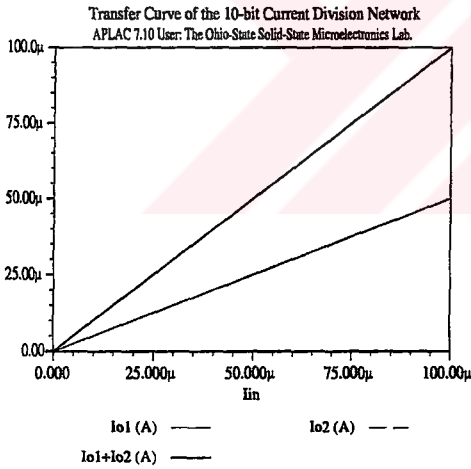
$$I_{o2} = I_{in} \sum_{i=1}^{10} 2^{-i} \bar{d}_i \quad (3.46)$$

Figure 3.23 shows the transfer curve of the 10-bit current division network for the aspect ratio of $W/L=44/4$, and for two different digital word settings;

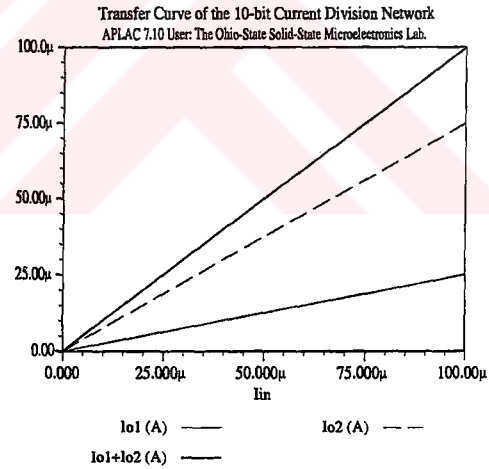
$$d_1=1, d_2=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$$

$$d_2=1, d_1=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$$

Simulations were done for an input current of $I_{in}=100\mu A$. The netlist is given in Appendix K



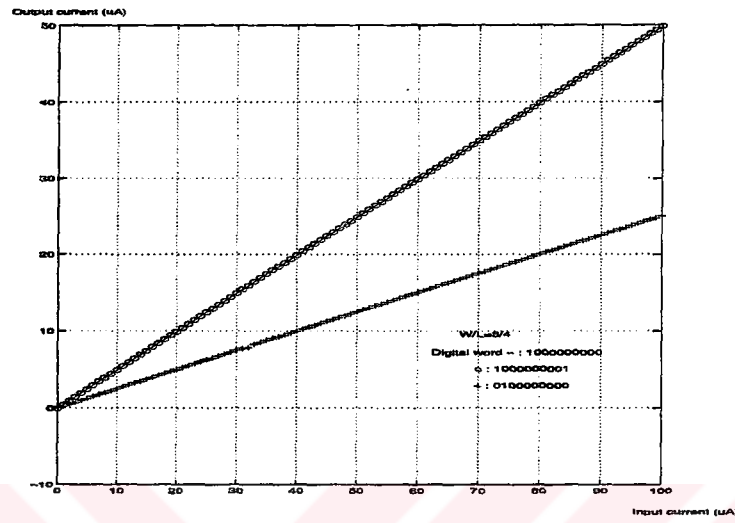
(a)



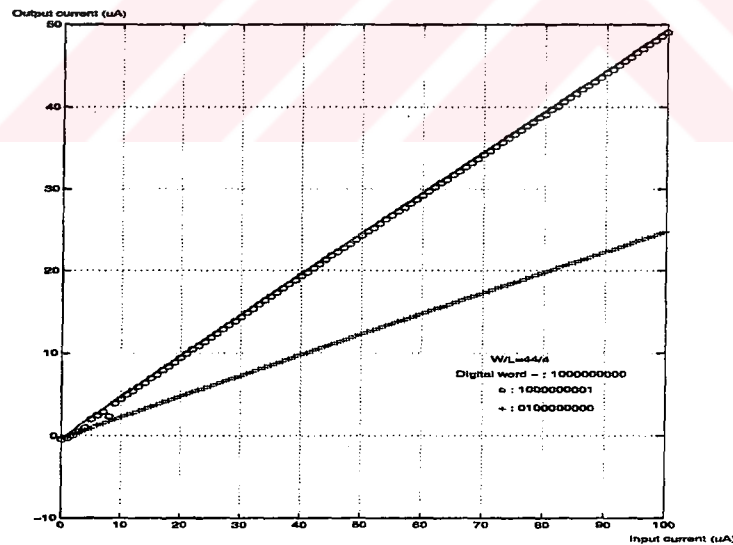
(b)

Figure 3.23: Transfer curve of the 10-bit current division network (APLAC simulation results), for the aspect ratio of $W/L=44/4$, and for digital word settings; a) $d_1=1, d_2=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$ and b) $d_2=1, d_1=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$

The 10-bit current division network was fabricated through the MOSIS 2 μ m process, using MOS transistor Level-2 model parameters, for the aspect ratios of $W/L=8/4$ and $W/L=44/4$. The transfer curve for both aspect ratios and the two different digital word settings given above are shown in Figure 3.24.



(a)



(b)

Figure 3.24: Transfer curve for the 10-bit current division network (experimental results) for two digital word settings; $d_1=1$, $d_2=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$; $d_2=1$, $d_1=d_3=d_4=d_5=d_6=d_7=d_8=d_9=d_{10}=0$; a) $W/L=8/4$, b) $W/L=44/4$

The experimental results for the 10-bit current division network were obtained using the HP4145B parameter analyzer. Measurements were made on 4 tiny MOSIS chips, each one having 11 samples of the 10-bit current division network, 6 samples for the aspect ratio of $W/L=44/4$, and 5 samples for the aspect ratio of $W/L=8/4$. The results are discussed in Chapter 4.



4. STATISTICAL DESIGN AND YIELD ENHANCEMENT OF LOW VOLTAGE CMOS ANALOG VLSI CIRCUITS

The previous chapter discussed several low voltage and low power CMOS analog VLSI circuits and their operation principles. The development of all these circuits requires an understanding of basic circuit design techniques and a knowledge of transistor nonideality effects on circuit performance, since despite the technological progress in the fabrication process steps, the fluctuation in each step that affects the device performances have not been scaled down in proportion. The fabrication process is not easily characterized because these variations are random in nature. Such variations could ultimately be a limiting factor on how low the supply voltage and how reliable sub-micron designs could be. In order to produce manufacturable analog integrated circuits with high functional yield and a high degree of reliability, the design of such circuits must be robust with respect to random process and device parameter variations [10].

Due to inherent fluctuations in any integrated circuit manufacturing process, the functional yield is always less than 100%. As the complexity of VLSI chips increase, and the dimensions of VLSI devices decrease, the sensitivity of performance to process fluctuations increases, thus, further reducing the functional yield. Moreover, with current trends of higher levels of integration leading to complete mixed-signal systems on a chip, yield loss due to the analog component must be minimized such that it has little effect on the yield of the mixed-signal chip. The functional yield of a chip is the percentage of the total number of circuit samples which have an acceptable circuit

performance determined by the chip specifications, over the total number of circuit samples. This is different from catastrophic or destructive yield over which circuit designers have no control. Circuit designers must ensure their chips have an acceptable functional yield under all manufacturing process variations. If there is more than one sample of the circuit on the same chip, the number of working circuits might be high, but in order to have a high functional yield the number of the circuits working with the required performance should be as high as possible, hence, it is important to statistically analyze the circuits to make a robust design. The SMOS model and the statistical techniques, introduced previously in Chapter 2, are used for this purpose.

The most critical issue in the design of analog CMOS circuits is device matching [25]. Matched devices are necessary to achieve high performance, e.g. to ensure low distortion, and minimize DC offset, thus, the design phase requires the statistical analysis of the circuits.

The eight circuits of Chapter 3 will be statistically examined in this chapter. The SMOS model is used to include random variations in the APLAC simulation environment, and the statistical techniques described in Chapter 2 are used to make the robust design of the circuits and enhance the yield.

Device mismatch is a function of the device area and the separation distance, as given in equation (2.1). Hence, when applying the statistical techniques to make a robust design of the circuits, the area of the transistors should be somehow included in the netlist. This is done by using the equations

$$W = \sqrt{ab} \quad (4.1)$$

$$L = \sqrt{\frac{a}{b}} \quad (4.2)$$

where W and L are the transistor width and length, respectively, used in the netlist. The terms “ a ” and “ b ” are constant values.

“ a ” corresponds to the area of the transistors in the circuit. A minimum and maximum value is defined for each area and “ a ” takes these values during the simulation. The minimum “ a ” values for the transistors, in this work, are selected from the aspect ratios

given in Tables 3.1 and 3.2 (such that the minimum area value is $10\mu\text{m}^2$ for transistor M_{n1} , $200\mu\text{m}^2$ for transistor M_{n2} , etc.). The maximum area values are, in general, selected as 5-10 times the minimum area value. The selection of the maximum areas are given in the related sections of this chapter.

“b”, on the other hand, is a constant, and can be any value that will result in an acceptable W and L calculated by equations (4.1) and (4.2) for that transistor. In this work, the b value for each transistor is selected as the aspect ratios given in Tables 3.1 and 3.2; e.g., the “b” value is 5/2 for transistor M_{n1} , 100/2 for transistor M_{n2} , etc.

Let's take the low voltage CMOS square-law composite cell as an example: For transistor M_{n1} , the “a” value is $10\mu\text{m}^2$ and “b” is 5/2. By using equations (4.1) and (4.2) $W=5\mu\text{m}$ and $L=2\mu\text{m}$ is calculated. The maximum value of the transistor area is selected as $50\mu\text{m}^2$ and “b” is again 5/2, thus, making $W=11\mu\text{m}$ and $L=4.5\mu\text{m}$.

During the statistical simulations, the area values corresponding to the transistors will be determined by the Plackett-Burman and Box-Behnken designs. For instance, during the first step of the design, the first column of the Plackett-Burman design matrix is +1, +1, +1, -1, +1, -1, -1, -1, where -1 corresponds to the minimum area and +1 corresponds to the maximum area. During the Plackett-Burman design, transistors will sometimes get their maximum areas and sometimes their minimum areas, eventually building the empirical model that is valid in between their minimum and maximum values, which is representing the circuit.

Device matching is also a function of the separation distance, as mentioned above. The separation distance information is taken from the layout of the transistors. The X and Y coordinates of the transistors are placed in the netlist. If the layout of the circuit does not exist, it is possible to include an estimation of the X and Y coordinates of the transistors in the circuit.

It is possible to make the X and Y coordinates variable, as well as keeping them constant. In case the coordinates are variables, the affect of the separation distance on mismatch will be included in the statistical simulations. If a single coordinate is included

in the netlist, however, the placement of the transistors will not change, thus, the affect of one separation distance will be considered only.

In this work the X-Y coordinates are taken from only one layout and different placements are not tried. Recent works show that the affect of separation distance on the standard deviation of mismatch is proved to be much less than the effect of the transistor area [10, 25]. This work mainly concentrates on the area effect in Pelgrom's equation.

This chapter gives the application of the statistical design methodology to analog circuits.

The statistical analysis of the circuits are done for DC performances. The CMOS square-law composite cells represent a single transistor, therefore requires $I_{d1}=I_{d1}$ in Figure 3.4 and $I_{d3}=I_{d1}$ in Figure 3.9. Any mismatch in these currents will cause variations in the performance of the overall circuits which use the cells as a main building block, hence, the relative drain current mismatch of the cells needs to be statistically examined.

Transconductor and multiplier circuits depend on device matching to achieve linear characteristics. Ignoring statistical design may result in a wide variation in the offset and nonlinearity when manufactured in large numbers. The statistical analysis of the transconductors are done for the DC performances, DC offset and nonlinearity, and the results are given in the related sections of this chapter.

The four-MOSFET structure was presented in Section 3.4 assuming perfect matching. It was mentioned that the four-MOSFET structure cancels even and odd-order nonlinearities, hence, it seems to have a good linearity performance. In case there is mismatch between transistors in the structure, the whole review should be made again. The statistical examination of the four-MOSFET structure is included in this chapter.

A 10-bit current division network was presented in Section 3.5, which can be used in a D/A converter to provide binary weighting. The current division network is based on the assumption of matched transistors, whereas, random variations may cause mismatch between transistors and a slight mismatch may cause an error which will limit the achievable resolution. Therefore, it is important to consider statistical simulations in the design of the D/A converter and determine the error in terms of LSB units.

The statistical design steps for each of these eight circuits is given together with remarks at the end of each section.

The four-MOSFET structure and the 10-bit current division network were fabricated through MOSIS. Statistical measurement results for these circuits are also given in the related sections.

4.1. Statistical Design of the Low Voltage and Low Power CMOS Square-Law Composite Cells

The low voltage and low power CMOS square-law composite cells were described in detail, in Chapter 3. This section explains the statistical analysis of the circuits.

4.1.1. Statistical Design of the Low Voltage CMOS Square-Law Composite Cell

The description of the low voltage CMOS square-law composite cell was given in Section 3.1. The circuit is shown in Figure 4.1, once again, to avoid returning back to Section 3.1 whenever the circuit is referred to.

The CMOS square-law composite cell represents a single MOS transistor, and, requires $I_d = I_{d1}$ in Figure 4.1. Any mismatch in these currents will cause variations in the performance of the overall circuits which use the cell as a main building block. Nominal simulation results may show that there is no mismatch between the currents, I_d and I_{d1} , since they do not include the effect of the random process variations. Statistical analysis, though, will include these variations and may show different results. The statistical simulations are made to compare the nominal and statistical drain current values, and to see the variation between them.

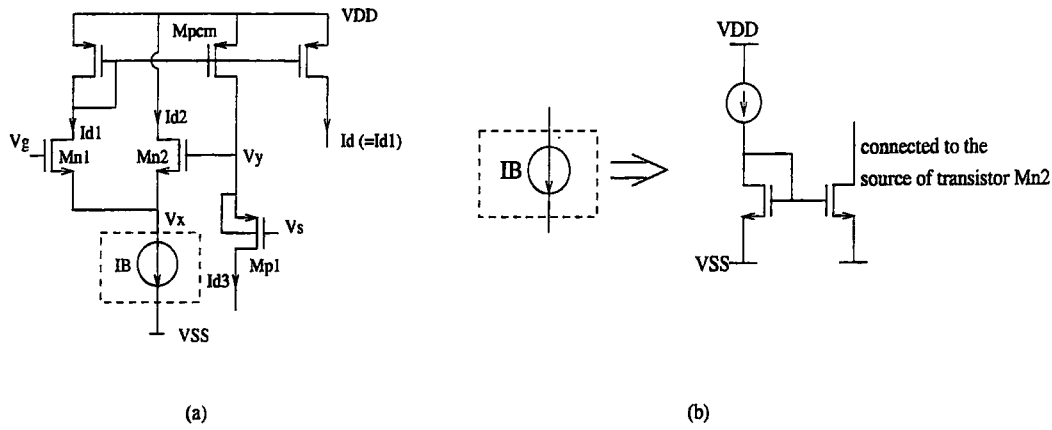


Figure 4.1: a) Low voltage CMOS square-law composite cell, b) Representation of the current source. The circuit description is given in detail in Section 3.1.

The two-step experimental procedure given in Section 2.3 and discussed in the whole of Chapter 2, is used in the statistical design of the cell [56-58]. The final goal is to represent the circuit with an empirical model using the statistical techniques. The empirical model will use the areas of the transistors in the circuit as input variables. The output of the empirical model is the standard deviation of the drain current mismatch. Hence, it is possible to see the effect of the variations of the areas of transistors on the drain current mismatch.

The whole procedure is explained in detail for the statistical design of the low voltage CMOS square-law composite cell; the procedure is repeated in the next sections, mainly concentrating on the conclusions.

The first step of the empirical model is to create a netlist for the circuit, which is already given in Appendix C. The netlist of the statistical simulations will be different then the netlist of the nominal simulations, simply, because the statistical simulations will require the inclusion of the small programs that will help calculate the standard deviation in the drain current mismatch. The netlist for the statistical simulations of the low voltage CMOS square-law composite cell is given in Appendix L, in the floppy disk attached to the thesis. The nominal simulation results and the statistical simulation results are compared. Simply, if random variations do not contribute to the results, the standard

deviations should be “0”, and there should be no transistor mainly contributing to the variation, since there will be no variation.

The second step of the methodology is to select the input variables, and ranges for these input variables. The variables, as discussed above, are the areas of the transistors. Five input variables are selected as a_{n1} , a_{n2} , a_{pcm} , a_{p1} and a_{ncs} , and they represent the areas of transistors M_{n1} , M_{n2} , M_{pcm} , M_{p1} and the transistors for the bias current, I_B , respectively. The ranges of the transistor areas are selected using their aspect ratios, as explained at the first part of this chapter, and are shown in Table 4.1.

Table 4.1: Minimum and maximum area assignment for each transistor - low voltage CMOS square-law composite cell

Transistors	M_{n1}	M_{n2}	M_{pcm}	M_{p1}	M_{ncs}
Areas	a_{n1}	a_{n2}	a_{pcm}	a_{p1}	a_{ncs}
$(-1)\mu\text{m}^2$	10	200	450	30	114
$(+1)\mu\text{m}^2$	50	1000	2250	150	570

The area values corresponding to “-1” represent the minimum area values, and the values corresponding to “+1” represent the maximum values. The minimum area values were determined from the actual aspect ratio of the transistors, and the maximum values are selected as 5 times the minimum values.

The next step is the screening experiment. In this step, the most contributing transistors to the performance chosen are screened out. Since there are five input variables initially, the number of runs for the Plackett-Burman design is eight. The Plackett-Burman design matrix for eight runs and five variables is given in Table 4.2.

Table 4.2: The Plackett-Burman design matrix and simulation results - low voltage CMOS square-law composite cell

Runs	a_{n1}	a_{n2}	a_{pcm}	a_{p1}	a_{ncs}	$\sigma(I_{cm})$
1	1	-1	-1	1	-1	0.0167
2	1	1	-1	-1	1	0.0222
3	1	1	1	-1	-1	0.0213
4	-1	1	1	1	-1	0.0278
5	1	-1	1	1	1	0.0144
6	-1	1	-1	1	1	0.0246
7	-1	-1	1	-1	1	0.0248
8	-1	-1	-1	-1	-1	0.0256

Each column in Table 4.2 represents the five different transistor areas. Let us concentrate on the first column, that is the area of transistor M_{n1} : In the first three runs the area of transistor M_{n1} will take its maximum value, in the fourth run the minimum value, so forth. The area of transistor M_{n1} will be examined in between the minimum and maximum values, hence, if this transistor is screened out to be one of the contributing transistors to the drain current mismatch, the results will be valid only for this range of areas.

The last column of Table 4.2 shows the results of the eight runs of Plackett-Burman simulations. Each run in the design matrix takes 10 seconds of CPU time on a HP715/133 workstation. The netlist of the simulations are given in Appendix L.

$\sigma(I_{cm})$ in Table 4.2 is the standard deviation of the relative current mismatch.

The first step of the experiment will be completed once the SS values and contribution of each variable is calculated. The SS values are calculated with the help of equation (2.6) and the contribution of each variable is calculated by taking the ratio of the variable under consideration and the sum of all the SS values. Table 4.3 shows the SS values and the contribution of each variable, for the low voltage CMOS square-law composite cell.

Table 4.3: SS values and contribution of each transistor - low voltage CMOS square-law composite cell

Variables	SS	Contribution (%)
a_{n1}	9.9073×10^{-5}	69.61
a_{n2}	2.5975×10^{-5}	18.25
a_{pcm}	8.0244×10^{-8}	0.06
a_{p1}	1.3707×10^{-5}	9.63
a_{ncs}	3.4847×10^{-6}	2.45

The results given in Table 4.3 show that three transistors will be considered for the second step of the design; transistors M_{n1} , M_{n2} and M_{p1} , since the contribution of these three transistors will sum up over 95% and the cut off point is selected as 5%. The other two transistors can be kept at their initial values.

The second step is a thorough examination on the three most contributing transistors. An empirical model will be built, which is using these transistors as input variables. Using this empirical model, the areas of these transistors can be changed and the impact of these variations on the output performance will be observed.

The Box-Behnken model building experiment is used to make a thorough examination, as explained in Chapter 2. 15 runs are required for three variables. The Box-Behnken experiment is a three-level experiment, therefore the input variables will be examined in their minimum, maximum and center values. The center value is calculated as the value that is in the middle of the minimum and maximum values, and is represented as "0" in the design matrix.

Table 4.4 shows the results of the Box-Behnken simulations. The netlist of the simulations are given in the second section of Appendix L. Each run in the design matrix takes 10 seconds of CPU time on a HP 715/133 workstation. These simulations end the second step of the design.

The next step is to start building the empirical model using the statistical software Minitab. Table 4.4 is the input of Minitab. This design matrix will help create the coefficients of the empirical model. The software also provides the designer with the model accuracy and the significance of each term in the model. Once the terms of the empirical model is determined, Response Surface Methodology will be used to visualize the relationship between the input variables and the output performance.

Table 4.4: The Box-Behnken design matrix and simulation results - low voltage square-law composite cell

Run	a_{n1}	a_{n2}	a_{p1}	$\sigma(I_{cm})$
1	-1	-1	0	0.0248
2	1	-1	0	0.0187
3	-1	1	0	0.0247
4	1	1	0	0.0233
5	0	0	0	0.0239
6	0	-1	-1	0.0199
7	0	1	-1	0.0229
8	0	-1	1	0.0192
9	0	1	1	0.0253
10	0	0	0	0.0233
11	-1	0	-1	0.0243
12	1	0	-1	0.0223
13	-1	0	1	0.0265
14	1	0	1	0.0241
15	0	0	0	0.0230

The empirical model that is built with the help of Minitab is given as

$$\begin{aligned}\sigma(I_{cm}) = & 0.02487 - 0.0298a_{n1} + 0.00081a_{n2} - 0.00027a_{p1} + 0.02401a_{n1}^2 \\ & - 0.00009a_{n2}^2 - 0.00017a_{p1}^2 + 0.00145a_{n1}a_{n2} - 0.00076a_{n1}a_{p1} \\ & + 0.00033a_{n2}a_{p1}\end{aligned}\quad (4.3)$$

where I_{cm} is the current mismatch and is the performance under considerations. a_{n1} , a_{n2} and a_{p1} are the areas of the most contributing transistors, and are also the variables of the empirical model. The limits for the variables a_{n1} , a_{n2} and a_{p1} are $[10\mu m^2, 50\mu m^2]$, $[200\mu m^2, 1000\mu m^2]$ and $[30\mu m^2, 150\mu m^2]$, respectively, the empirical model is valid within these ranges. The “T” values for the terms a_{p1} , a_{p1}^2 and $a_{n1}a_{p1}$ are between -0.5 and 0.5, therefore, they are statistically insignificant, and excluded from the empirical model. Thus, the final empirical model that is obtained for the circuit is given as

$$\begin{aligned}\sigma(I_{cm}) = & 0.02487 - 0.0298a_{n1} + 0.00081a_{n2} + 0.02401a_{n1}^2 - 0.00009a_{n2}^2 \\ & + 0.00145a_{n1}a_{n2} + 0.00033a_{n2}a_{p1}\end{aligned}\quad (4.4)$$

with 93.3% accuracy. Note that the area values are 1/100'th of their actual values, because they were entered in such way.

Figure 4.2 shows the response surfaces for different pairs of input variables. The third variables are kept constant at their center values.

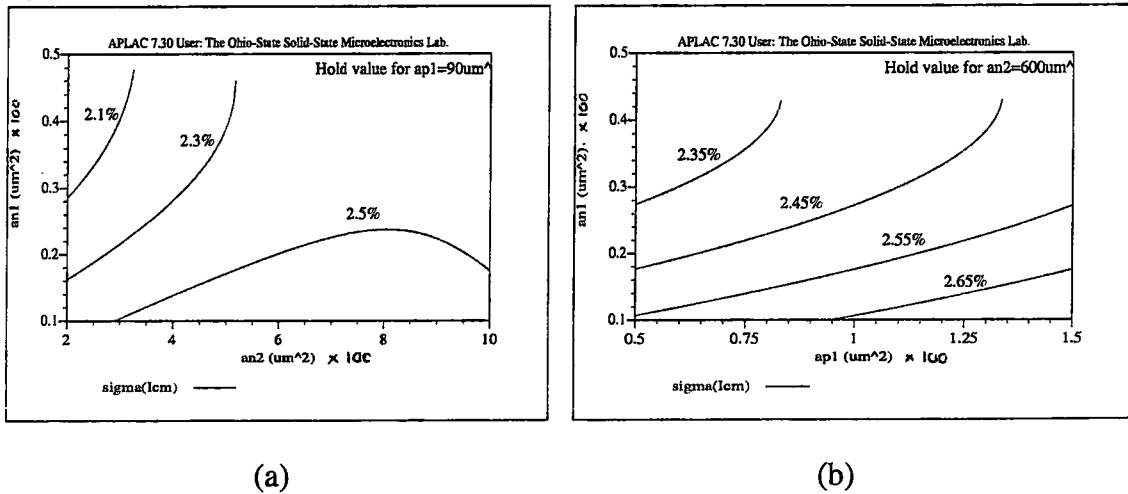


Figure 4.2: Response surfaces for pairs of transistors for the low voltage CMOS square-law composite cell; a) a_{n1} vs. a_{n2} ($a_{p1}=90\mu m^2$), b) a_{n1} vs. a_{p1} ($a_{n2}=600\mu m^2$)

The contour curves given in Figure 4.2 show the standard deviation of the current mismatch in the low voltage CMOS square-law composite cell. The contour curves show that the pair that has a_{p1} as a factor is almost flat, thus, a_{p1} does not have a significant effect. It would be fair to conclude that the effect of a_{p1} is the least among the three variables. One can get the feel for this from equation (4.3), since there is only one term that actually consists of a_{p1} , with a comparably small coefficient value. It is also possible to get to the same conclusion by examining Figure 4.3. Figure 4.3 shows the contour curves for the a_{n1} , a_{n2} pair, but for a different hold value for a_{p1} . Obviously, changing the hold value for a_{p1} did not make a significant effect on the curves.

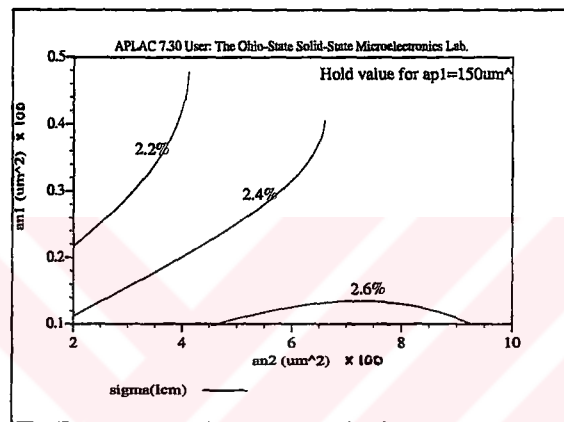


Figure 4.3: Response surfaces for a_{n1} vs. a_{n2} ($a_{p1}=150\mu\text{m}^2$)

Let us now concentrate on Figure 4.2(a), which shows the contour curves for the a_{n1} , a_{n2} pair. The x and y axis for the graph represents the areas of the transistors, and the third transistor has a hold value. There could be two ways to interpret and/or to make use of the graph:

- 1- If there is a specific value that is preferred for each transistor, it is possible to find those values from the x and y axis, and find the intersection point. The value of the surface which crosses that intersection point gives the standard deviation value of the current mismatch.
- 2- If there is a certain current mismatch that is preferred, e.g., according to the design specifications, the circuit cannot tolerate more than a certain value of current mismatch, it is possible to find the surface that corresponds to that value. Then, the areas that

intersect on that surface will be the solution. Obviously, there will be more than one solution; this brings the preferred flexibility of selecting the suitable values for different designs.

The x and y axis shows area values for the transistors. The designer will select the appropriate W and L value which gives that area.

The average standard deviation seen from the contour curves is in the range of 2.3%, which means that the random process variations will affect the circuit performance with a 2.3% variation. The lowest standard deviation value which can be achieved from the curves in Figure 4.2(a), though, are 2.1% with the appropriate sizing of the transistors. The designer has the flexibility of deciding if those values are actually appropriate for the circuit, and if not, to be prepared for the variation on the performance.

It is possible to use the standard deviation information to enhance the yield. Let us assume that the goal of optimization is to obtain the minimum device area while achieving $I_{cm} < 5\%$, with a functional yield of 95%, or equivalently, to achieve the standard deviation of the relative drain current mismatch of 2.5%, since 95% is approximately $\pm 2\sigma$. From Figure 4.2(a), the minimum point on the response surface corresponding to 2.5% is found to be $a_{n1}=10\mu m^2$, $a_{n2}=300\mu m^2$, and $a_{p1}=90\mu m^2$. From the definition of W and L given by equation (4.1) and equation (4.2), $\left(\frac{W}{L}\right)_{n1} = \frac{5}{2}$,

$$\left(\frac{W}{L}\right)_{n2} = \frac{122}{2.5}, \text{ and } \left(\frac{W}{L}\right)_{p1} = \frac{26}{3.5}.$$

Thus, when these aspect ratios are used for transistors M_{n1} , M_{n2} and M_{p1} , the standard deviation will not exceed 2.5%, and the functional yield will be 95%. The only way to prove this result is to fabricate the circuit in large numbers and calculate the standard deviations from the measurement data, but then, the whole purpose of making statistical design is to be able to estimate the yield and standard deviation without actually having to fabricate the circuits in order to reduce the cost. Statistical simulation results will give insight to the designer, and a quantitative measure of how much the standard deviation is going to be. The four-MOSFET

structure and the 10-bit current division network were fabricated, and the comparison of the experimental and statistical simulation results are given in the related sections.

The low voltage low power CMOS square-law composite cell is statistically examined next. A comparison of the results of the two composite cells will be given at the end of the next section.

4.1.2. Statistical Design of the Low Voltage Low Power CMOS Square-Law Composite Cell

The low voltage low power CMOS square-law composite cell is given in Figure 4.4. which is the same as Figure 3.9.

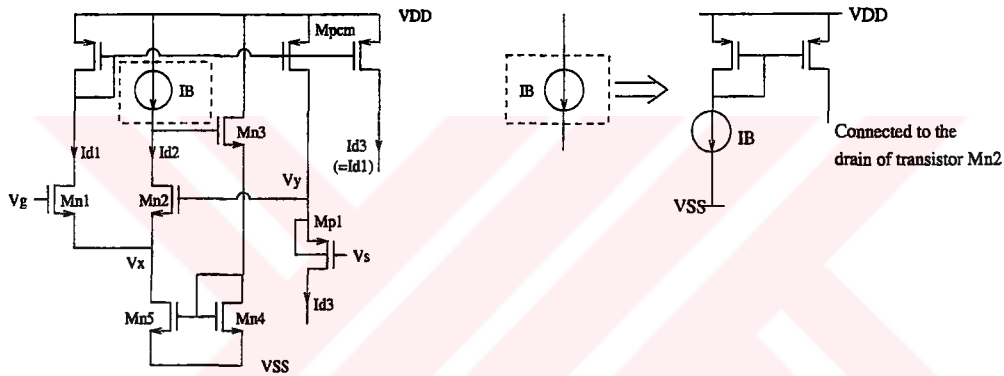


Figure 4.4: a) Low voltage low power CMOS square-law composite cell, b) Representation of the current source. The circuit description is given in detail in Section 3.1

The operation of the circuit was described in Chapter 3, and will not be explained again in this section. The statistical analysis of the circuit will be made [58, 59], using the exact same methodology that is followed in the previous section, hence, the reader can refer to the previous section for the details of the steps.

The netlist for the statistical simulations is given in Appendix M, in the floppy disk attached to the thesis. One difference when compared to the previous circuit netlist is the number of input variables. The present circuit has more transistors, therefore, the number of the initial input variables are seven, whereas, there were five variables for the previous circuit. The seven input variables are selected as a_{n1} , a_{n2} , a_{pcm} , a_{n3} , a_{p1} , $a_{n4,5}$

and a_{pcs} , representing the areas of transistors M_{n1} , M_{n2} , M_{pcm} , M_{n3} , M_{p1} , M_{n4} and M_{n5} , and the transistors for the bias current, I_B , respectively. The selected ranges of the transistor areas are shown in Table 4.5.

Table 4.5: Minimum and maximum area assignment for each transistor - low voltage low power CMOS square-law composite cell

Transistors	M_{n1}	M_{n2}	M_{pcm}	M_{n3}	M_{p1}	$M_{n4,n5}$	M_{pcs}
Areas	a_{n1}	a_{n2}	a_{pcm}	a_{n3}	a_{p1}	$a_{n4,5}$	a_{pcs}
$(-1)\mu\text{m}^2$	10	200	450	1000	30	114	450
$(+1)\mu\text{m}^2$	50	1000	2250	5000	150	570	2250

The area values corresponding to “-1” represent the minimum area values, and the values corresponding to “+1” represent the maximum values. The minimum area values were determined from the actual aspect ratio of the transistors, and the maximum values are selected as 5 times the minimum values.

Since the number of input variables are seven, eight runs for the Plackett-Burman design is sufficient. The Plackett-Burman design matrix for eight runs and seven variables is given in Table 4.6.

Table 4.6: The Plackett-Burman design matrix and simulation results - low voltage low power CMOS square-law composite cell

Runs	a_{n1}	a_{n2}	a_{pcm}	a_{n3}	a_{p1}	$a_{n4,5}$	a_{pcs}	$\sigma(I_{cm})$
1	1	-1	-1	1	-1	1	1	0.0239
2	1	1	-1	-1	1	-1	1	0.0283
3	1	1	1	-1	-1	1	-1	0.0248
4	-1	1	1	1	-1	-1	1	0.0293
5	1	-1	1	1	1	-1	-1	0.0204
6	-1	1	-1	1	1	1	-1	0.0327
7	-1	-1	1	-1	1	1	1	0.0291
8	-1	-1	-1	-1	-1	-1	-1	0.0295

The last column of Table 4.6 shows the results of the eight runs of Plackett-Burman simulations. Each run in the design matrix takes 14 seconds of CPU time on a HP715/133 workstation. Table 4.7 shows the SS values and the contribution of each transistor to the circuit performance.

Table 4.7: SS values and contribution of each transistor - low voltage low power CMOS square-law composite cell

Variables	SS	Contribution (%)
a_{n1}	6.7192×10^{-5}	62.27
a_{n2}	1.8486×10^{-5}	17.13
a_{pcm}	1.5141×10^{-5}	14.03
a_{n3}	3.5175×10^{-6}	3.26
a_{p1}	1.0883×10^{-6}	1.01
$a_{n4,n5}$	1.1173×10^{-6}	1.04
a_{pcs}	1.3660×10^{-6}	1.27

It is seen that four transistor contributions, namely, M_{n1} , M_{n2} , M_{pcm} and M_{n3} , will sum up to 95%. However, the contribution of the fourth variable is small compared to the other three. It is also experienced from the previous circuit that a variable with this small contribution is not going to be effective on the contour curves, hence, it will suffice to take the first three variables and include them in the next step.

Table 4.8 shows the Box-Behnken design matrix and simulation results. The netlist of the simulations are given in the second section of Appendix M. Each run in the design matrix takes 14 seconds of CPU time on a HP 715/133 workstation.

Table 4.8: The Box-Behnken design matrix and simulation results - low voltage low power CMOS square-law composite cell

Run	a_{n1}	a_{n2}	a_{pcm}	$\sigma(I_{cm})$
1	-1	-1	0	0.0286
2	1	-1	0	0.0195
3	-1	1	0	0.0313
4	1	1	0	0.0259
5	0	0	0	0.0258
6	0	-1	-1	0.0257
7	0	1	-1	0.0253
8	0	-1	1	0.0224
9	0	1	1	0.0265
10	0	0	0	0.0261
11	-1	0	-1	0.0302
12	1	0	-1	0.0260
13	-1	0	1	0.0303
14	1	0	1	0.0253
15	0	0	0	0.0257

The Box-Behnken design matrix was applied to the statistical software Minitab, to obtain the empirical model for the circuit. The resulting model is given as

$$\begin{aligned} \sigma(I_{cm}) = & 0.03451 - 0.04611a_{n1} + 0.00056a_{n2} - 0.00031a_{pcm} + 0.04281a_{n1}^2 \\ & - 0.00008a_{n2}^2 + 0.00120a_{n1}a_{n2} + 0.0003a_{n2}a_{pcm} \end{aligned} \quad (4.5)$$

with a 93.9% accuracy. I_{cm} in the model is the current mismatch. The “T” value for the term $a_{n1}a_{pcm}$ is between the values -0.5 and 0.5, hence, this term is excluded from the empirical model. The coefficient of a_{pcm}^2 is “0”, so this term is not in the model either.

The limits for the variables a_{n1} , a_{n2} and a_{pcm} are $[10\mu\text{m}^2, 50\mu\text{m}^2]$, $[200\mu\text{m}^2, 1000\mu\text{m}^2]$ and $[450\mu\text{m}^2, 2250\mu\text{m}^2]$, respectively; the empirical model is valid within these ranges.

Figure 4.5 gives the contour curves for different pairs of variables.

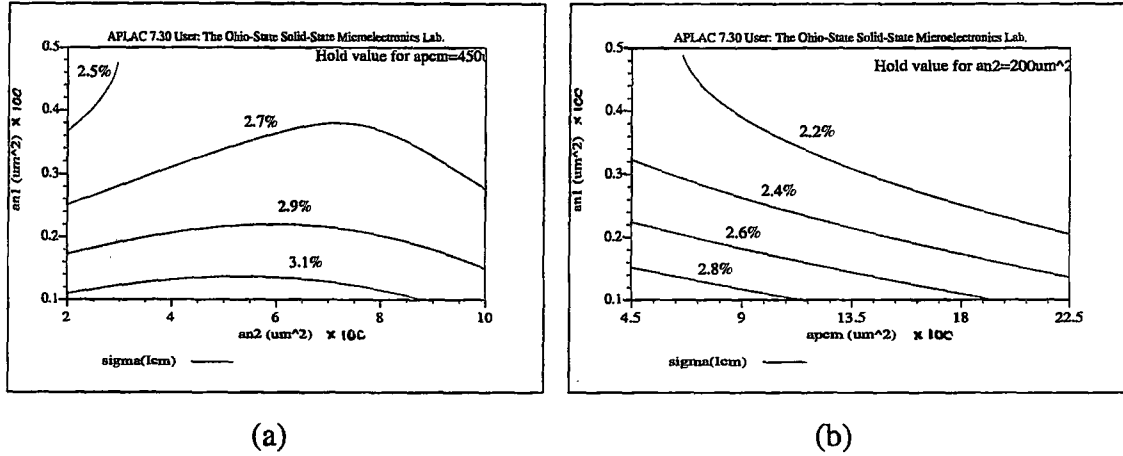


Figure 4.5: Response surfaces for pairs of transistors for the low voltage low power CMOS square-law composite cell; a) a_{n1} vs. a_{n2} ($a_{pcm}=450\mu\text{m}^2$), b) a_{n1} vs. a_{pcm} ($a_{n2}=200\mu\text{m}^2$)

It is possible to make use of the curves the same way as explained in the previous section. Never to mention, the factor a_{pcm} seems to be insignificant for this circuit, thus the main focus is on a_{n1} and a_{n2} . The standard deviation is in the range of 2.5%, somewhat higher than the previous circuit, yet still comparable.

The low voltage low power composite cell has a feedback loop and also the number of transistors are more than the low voltage composite cells, thus, the circuit is more complicated. However, the standard deviation does not differ too much. It is possible to conclude that the circuit not only avoids the trade-off between low voltage operation and low power dissipation, but statistically speaking, overcoming the trade-off does not cost anything to the circuit, from the statistical design point of view. The additional transistors have not degraded the robustness, since their contributions to the circuit performance are not too high anyway, thus, improvement of the circuit was possible for the same functional yield and standard deviation of the drain current mismatch.

It is possible to make a similar analysis of the results, as in the previous section. A specific standard deviation can be targeted, thus, a yield specification can be determined and the minimum area values achieving the targeted standard deviation and yield can be found; e.g., let us assume the goal of optimization is to obtain the minimum device area while achieving $I_{cm} < 6\%$, with a functional yield of 95%, or equivalently, to achieve the standard deviation of the relative drain current mismatch of 3%, since 95% is approximately $\pm 2\sigma$. From Figure 4.5(a), the closest standard deviation values to 3.1% is 3%, thus, the response surface with this value will be considered. The minimum point on the response surface corresponding to 3% is found to be $a_{n1}=11\mu\text{m}^2$, $a_{n2}=200\mu\text{m}^2$, and $a_{pcm}=450\mu\text{m}^2$. From the definition of W and L given by equation (4.1) and equation (4.2), $\left(\frac{W}{L}\right)_{n1} = \frac{5.2}{2.1}$, $\left(\frac{W}{L}\right)_{n2} = \frac{100}{2}$, and $\left(\frac{W}{L}\right)_{p1} = \frac{150}{3}$. Thus, when these aspect ratios are used for transistors M_{n1} , M_{n2} and M_{pcm} , the standard deviation will not exceed 3%, and the functional yield will be 95%. Again, the only way to prove this result is to fabricate the circuit in large numbers and calculate the standard deviations from the measurement data. This way of evaluation also explains how to enhance the yield. By achieving optimization of the circuit, the tolerance of the circuit will be reduced, thus, when this specification is met, the yield will be achieved for a tighter limit, hence, the yield will be enhanced.

4.2. Statistical Design of the Low Voltage and Low Power Transconductors

Two new transconductors were built in this thesis, using the composite cells as a main building block. The transconductors reflect the same advantage and disadvantages of the composite cells. The description of these circuits are given in detail in Chapter 3, together with the motivation of designing these transconductors. The circuit descriptions

will not be discussed in this chapter again. This section deals with the statistical design of the transconductors.

A necessary condition to obtain G_m is to have matched K_{eq} and V_{Teq} between the two cells that are connected in such a way to build the transconductors. K_{eq} and V_{Teq} are affected by different transistors, and it is important to determine how big these effects are. K_{eq} and V_{Teq} variations will affect the offset and linearity performances of the transconductors. Hence, these two performances are selected as the performances under consideration for the statistical analysis of the transconductors.

The typical way of seeing the linearity is by changing the input voltage and the control voltage, then observing the output and checking how linear the curves are. This way of checking linearity, however, may show a low nonlinearity since random variations are not usually included during simulations.

During statistical simulations, the method of calculating nonlinearity should be included in the statistical netlist of the transconductor. Regular ways, such as THD analysis is one possibility to measure how linear the circuit is, however, the lengthy simulation time is the main drawback: The statistical simulations include the Monte Carlo analysis, thus, at least 500 runs for each calculation point in the THD analysis will take a long time.

A method that will give an idea about the nonlinearity of the circuit will be initially sufficient. Once the design specifications are believed to be met, the more accurate but lengthy simulations can be run for once and for all.

The method that is used to calculate the nonlinearity of the circuits is described next. This method will, for sure, be an indication to show if the nonlinearity is getting better or worse during the statistical simulations.

4.2.1. Nonlinearity Measurement Method

Figure 4.6 is used in describing the nonlinearity measurement method.

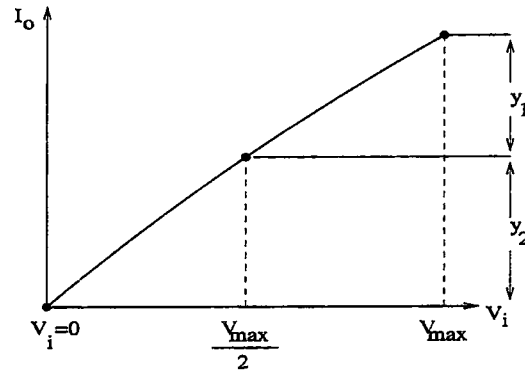


Figure 4.6: Nonlinearity measurement method

The curve in Figure 4.6 illustrates the upper part of the transfer curve of the transconductor. The x axis is the input voltage, V_i , and the y axis is the output current, I_o .

Three points are selected on the curve; $V_i=0$, $V_i=V_{max}$, and $V_i = \frac{V_{max}}{2}$. y_1 and y_2 of Figure 4.6 are calculated as

$$y_1 = I_o(V_{max}) - I_o\left(\frac{V_{max}}{2}\right) \quad (4.6)$$

$$y_2 = I_o\left(\frac{V_{max}}{2}\right) - I_o(0) \quad (4.7)$$

If there is perfect linearity, y_1 will be equal to y_2 ; if there is a slight nonlinearity, though, y_1 will differ from y_2 , and there will no equality. The nonlinearity is expressed with the help of y_1 and y_2 .

Let us assume that there is a nonlinearity in the curve given in Figure 4.6. The curve can then be expressed as

$$I_o = \alpha_0 + GV_i + \alpha_1 V_i^2 \quad (4.8)$$

where $\alpha_0=I_0(V_i=0)$, G is the transconductance, and α_1 is the nonlinearity coefficient. If the curve is linear, α_1 will be “0”, thus, the output current will have a linear equation.

From equation (4.8), the output current is evaluated at $V_i=V_{max}$, and $V_i = \frac{V_{max}}{2}$, then used in equations (4.6) and (4.7) to find α_1 as follows:

$$y_1 = (\alpha_0 + GV_{max} + \alpha_1 V_{max}^2) - \left(\alpha_0 + G\frac{V_{max}}{2} + \alpha_1 \frac{V_{max}^2}{4} \right)$$

$$y_1 = G\frac{V_{max}}{2} + \alpha_1 \frac{3V_{max}^2}{4} \quad (4.9)$$

$$y_2 = \left(\alpha_0 + G\frac{V_{max}}{2} + \alpha_1 \frac{V_{max}^2}{4} \right) - \alpha_0$$

$$y_2 = G\frac{V_{max}}{2} + \alpha_1 \frac{V_{max}^2}{4} \quad (4.10)$$

$$y_1 - y_2 = \alpha_1 \frac{V_{max}^2}{2} \Rightarrow \alpha_1 = \frac{2(y_1 - y_2)}{V_{max}^2} \quad (4.11)$$

This nonlinearity model is used in the netlist of the statistical simulations of the transconductors.

4.2.2. Statistical Design of the Transconductor Using the Low Voltage CMOS

Square-Law Composite Cell

The transconductor using the low voltage CMOS square-law composite cell as a main building block is shown in Figure 4.7.

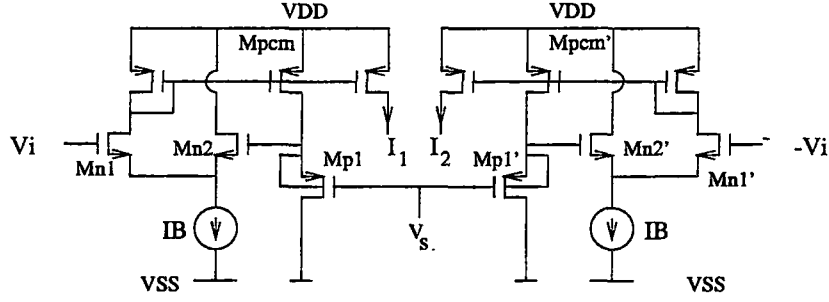


Figure 4.7: The transconductor using the low voltage CMOS square-law composite cell. The circuit description is given in detail in Section 3.2

The statistical design of the transconductor using the low voltage CMOS square-law composite cell is done [44, 60] using the statistical model and statistical techniques described in Chapter 2. The application of these tools and techniques were described in detail in the last section. The same methodology is used for the statistical design of the transconductor.

One difference between the statistical design of the composite cells and the transconductor is the circuit performance under consideration: The composite cells were mainly concentrating on the drain current mismatch, whereas the statistical design of the transconductors mainly focus on the offset and linearity of the circuits. The aforementioned method is used to make the statistical examination of the circuit for nonlinearity. The offset can be calculated also from Figure 4.6: The current value corresponding to $V_i=0$ is the offset current value.

As mentioned previously, two low voltage composite cells are connected in such a way to build the circuit. The aspect ratios of the cells are kept the same when building the transconductors, hence, the minimum and maximum area values for the input variables of the circuit will be the same as for the low voltage composite cell, and is given in Table 4.9.

Table 4.9: Minimum and maximum area assignment for each transistor - transconductor using the low voltage CMOS square-law composite cell

Transistors	M_{n1}, M_{n1}'	M_{n2}, M_{n2}'	M_{pcm}, M_{pcm}'	M_{p1}, M_{p1}'	M_{ncs}, M_{ncs}'
Areas	a_{n1}	a_{n2}	a_{pcm}	a_{p1}	a_{ncs}
$(-1)\mu\text{m}^2$	10	200	450	30	114
$(+1)\mu\text{m}^2$	50	1000	2250	150	570

Two cells are connected to build the transconductor. These two cells are completely identical which makes the area values corresponding to the same transistors equal. Thus, the equal transistors are grouped together as one, and are represented with the same area, e.g., the areas of transistors M_{n1} and M_{n1}' are represented as a_{n1} . If a_{n1} turns out to be a most contributing transistor for offset or nonlinearity, this means both M_{n1} and M_{n1}' are contributing to the performance.

Five input variables are selected as the input variables of the Plackett-Burman design. The Plackett-Burman design matrix and simulation results are given in Table 4.10. Each run in the design matrix takes 18 seconds of CPU time on a HP 715/133 workstation.

Table 4.10: The Plackett-Burman design matrix and simulation results for offset current and nonlinearity - transconductor using the low voltage CMOS square-law composite cell

Runs	a_{n1}	a_{n2}	a_{pcm}	a_{p1}	a_{ncs}	$\sigma(I_{\text{offset}}) (\mu\text{A})$	$\sigma(\alpha_1) (\mu\text{A}/\text{V}^2)$
1	1	-1	-1	1	-1	0.2029	0.5041
2	1	1	-1	-1	1	0.3671	0.5626
3	1	1	1	-1	-1	0.2329	0.3248
4	-1	1	1	1	-1	0.2722	0.2897
5	1	-1	1	1	1	0.1134	0.2154
6	-1	1	-1	1	1	0.3673	0.5140
7	-1	-1	1	-1	1	0.2975	0.4480
8	-1	-1	-1	-1	-1	0.4352	0.5945

The column under $\sigma(I_{\text{offset}})$ and $\sigma(\alpha_1)$ in Table 4.10 shows the standard deviation for the offset current and nonlinearity, respectively. The SS values and contribution of transistors are calculated, and the results are shown in Table 4.11.

Table 4.11: SS values and contribution of each transistor - transconductor using the low voltage CMOS square-law composite cell

Variables	SS (offset current)	Contribution (%) (offset current)	SS (nonlinearity)	Contribution (%) (Nonlinearity)
a_{n1}	2.5991×10^{-14}	34.98	7.1558×10^{-15}	5.54
a_{n2}	4.5337×10^{-15}	6.10	6.2762×10^{-16}	0.49
a_{pcm}	2.6037×10^{-14}	35.03	1.0067×10^{-13}	77.91
a_{p1}	1.7744×10^{-14}	23.88	2.0676×10^{-14}	16.00
a_{ncs}	5.9606×10^{-19}	0.01	9.0990×10^{-17}	0.07

Having Table 4.11 in hand, let us first concentrate on the results obtained for the offset current: The evaluation of Table 4.11 shows that the sum of four transistor contributions pass the 95% limit for offset current. The fourth contribution value (6.10%), however, is comparably small, thus, indicating that even if the fourth contribution is added in the next step of the statistical design, the effect of this factor will eventually be so small and ignored. Therefore, only the first three highest contributions will be taken into account and will be further investigated. The evaluation of the simulations for nonlinearity show also three main contributions from three transistors, which will be included in the next step of the design.

The next step of the statistical design methodology is the Box-Behnken design. If the number of the contributing transistors or the contributing transistors for each performance were different, the method would have proceeded separately for each performance, though, the number of the factors, and the transistors that are screened out are the same for both performances, thus, the Box-Behnken experiment will be run together.

Table 4.12 shows the Box-Behnken design matrix and simulation results for the offset current and nonlinearity, respectively. Each run takes about 18 seconds of CPU time on a HP 715/133 workstation. The netlist of the circuit for statistical simulations is given in Appendix N, in the floppy disk attached to the thesis.

Table 4.12: The Box-Behnken design matrix and simulation results for offset current and nonlinearity - transistor using the low voltage square-law composite cell

Run	a_{n1}	a_{pcm}	a_{p1}	$\sigma(I_{\text{offset}})$ (μA)	$\sigma(\alpha_1)$ ($\mu\text{A}/\text{V}^2$)
1	-1	-1	0	0.3341	0.4802
2	1	-1	0	0.2367	0.5188
3	-1	1	0	0.2217	0.3231
4	1	1	0	0.1216	0.2267
5	0	0	0	0.1549	0.2757
6	0	-1	-1	0.3241	0.5089
7	0	1	-1	0.2098	0.3693
8	0	-1	1	0.2322	0.5018
9	0	1	1	0.1283	0.2174
10	0	0	0	0.1573	0.2924
11	-1	0	-1	0.2993	0.4467
12	1	0	-1	0.1948	0.3583
13	-1	0	1	0.2157	0.3212
14	1	0	1	0.1172	0.2704
15	0	0	0	0.1544	0.3102

The Box-Behnken design matrix is applied to the statistical software Minitab, and the following empirical models are obtained for offset current and nonlinearity, respectively:

$$\begin{aligned}\sigma(I_{\text{offset}}) = & 0.6009 - 0.6772a_{n1} - 0.215a_{pcm} - 0.1957a_{p1} + 0.7014a_{n1}^2 \\ & + 0.0006a_{pcm}^2 + 0.0643a_{p1}^2 - 0.0004a_{n1}a_{pcm} + 0.0124a_{n1}a_{p1} \\ & + 0.0005a_{pcm}a_{p1}\end{aligned}\quad (4.12)$$

$$\begin{aligned}\sigma(\alpha_1) = & 0.7167 - 0.2724a_{n1} - 0.0246a_{pcm} - 0.1820a_{p1} + 0.5528a_{n1}^2 \\ & + 0.0009a_{pcm}^2 + 0.0952a_{p1}^2 - 0.0187a_{n1}a_{pcm} + 0.0784a_{n1}a_{p1} \\ & - 0.0067a_{pcm}a_{p1}\end{aligned}\quad (4.13)$$

The empirical models built for offset current and nonlinearity have a 99.9% and 98.8% accuracy, respectively. The valid ranges for the variables of the empirical models are $[10\mu\text{m}^2, 50\mu\text{m}^2]$, $[450\mu\text{m}^2, 2250\mu\text{m}^2]$ and $[30\mu\text{m}^2, 150\mu\text{m}^2]$, for a_{n1} , a_{pcm} and a_{p1} , respectively.

Before starting to discuss the results it is important to mention that the offset current found from the transfer curve of the transconductor given in Figure 3.12 was “0”, and the nonlinearity was calculated using equation (4.11) of Section 4.2.1, and was found as $0.352\mu\text{A}/\text{V}^2$, for a transconductance value of $44.3\mu\text{A}/\text{V}$. The transfer curve in Figure 3.12 was found without considering any random variation effect.

Let us first concentrate on the offset current: All the terms in the model have a valid “T” value, therefore none of the terms are excluded from the empirical model which is helping to increase the accuracy of the model. The response surfaces for each pair of transistors are shown in Figure 4.8.

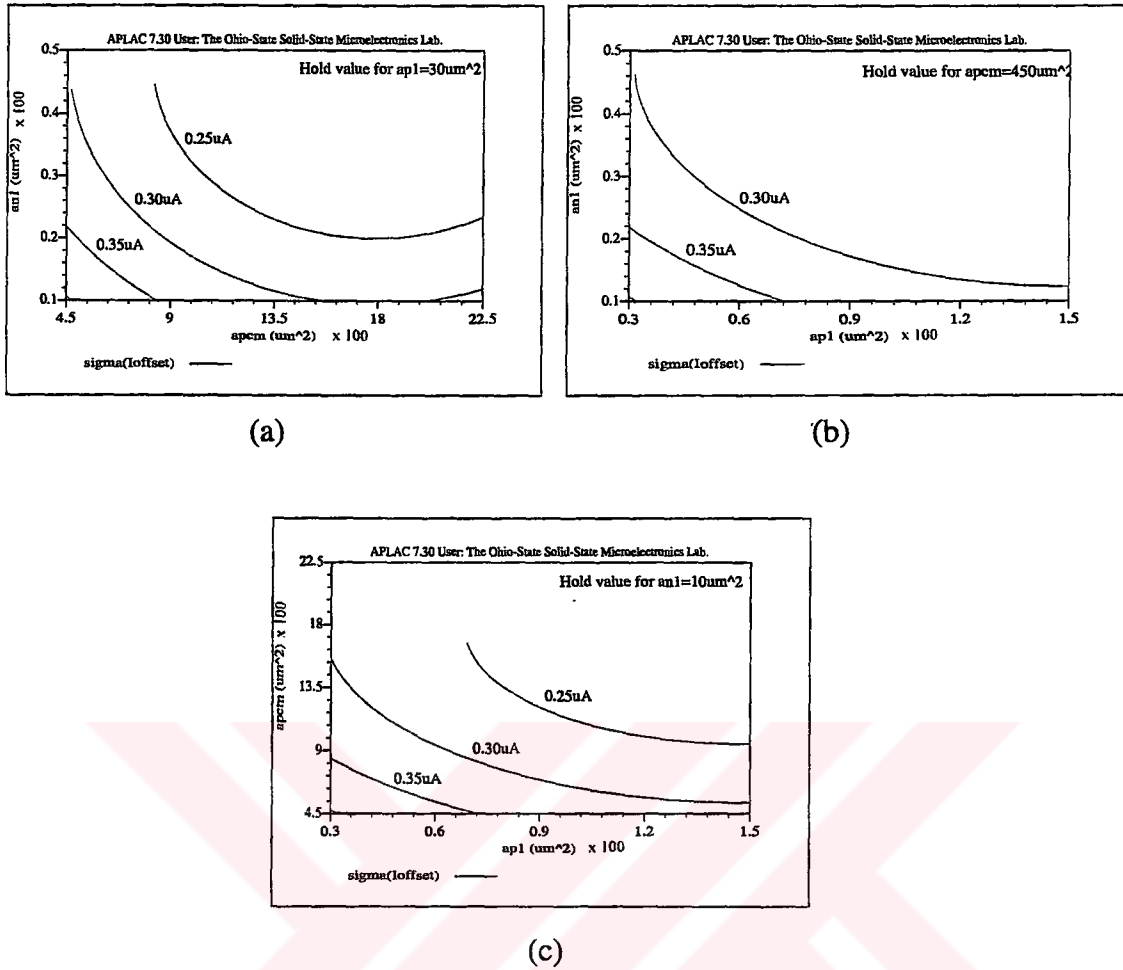


Figure 4.8: Response surfaces for the offset current of the transconductor using the low voltage CMOS square-law composite cell; a) a_{n1} vs. a_{pcm} ($a_{p1}=30\mu\text{m}^2$), b) a_{n1} vs. a_{p1} ($a_{pcm}=450\mu\text{m}^2$), and c) a_{pcm} vs. a_{p1} ($a_{n1}=10\mu\text{m}^2$)

The possible ways to use the contour curves were explained previously. The average standard deviation of the offset current is around $0.30\mu\text{A}$, whereas the offset current was found as “0” from the transfer curve given in Figure 3.12. Hence, the standard deviation value can be accepted as the offset current, which is apparently more than “0”. This again proves the importance of the statistical analysis of the circuit.

The designer should know the range of the output current to understand if the offset current is of any significance: The output current, from Figure 3.12, is about $24\mu\text{A}$, thus, the average offset current is about 1.25%. The design specifications will determine if this value is acceptable or not. Let us evaluate the contours on an example: Let us

consider Figure 4.8(a), and $a_{n1}=20\mu\text{m}^2$, $a_{pcm}=900\mu\text{m}^2$, and $a_{p1}=30\mu\text{m}^2$. The offset current for this design will be $0.3\mu\text{A}$. The designer will decide, though, if these values for a_{n1} , a_{pcm} , and a_{p1} are appropriate, but in any case, the designer will be able to estimate the offset current before fabrication, and if it is possible to achieve a smaller standard deviation, the yield will be enhanced as well.

The response surfaces for nonlinearity are obtained with the help of the empirical model given in equation (4.13), and are illustrated in Figure 4.9.

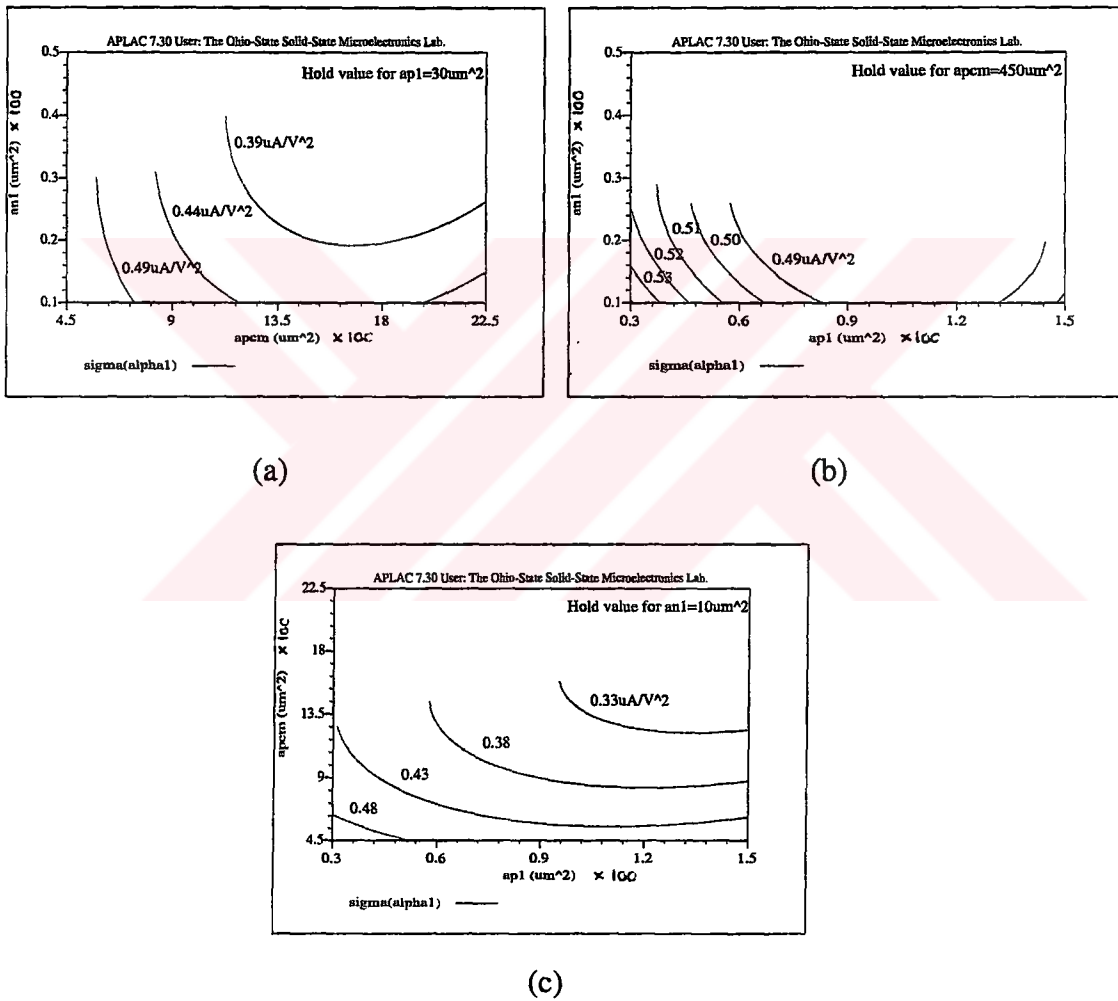


Figure 4.9: Response surfaces for the nonlinearity of the transconductor using the low voltage CMOS square-law composite cell; a) a_{n1} vs. a_{pcm} ($a_{p1}=30\mu\text{m}^2$), b) a_{n1} vs. a_{p1} ($a_{pcm}=450\mu\text{m}^2$), and c) a_{pcm} vs. a_{p1} ($a_{n1}=10\mu\text{m}^2$)

The nonlinearity of the transconductor was found from the transfer curve as $0.352\mu\text{A}/\text{V}^2$, for a transconductance value of $44.3\mu\text{A}/\text{V}$. The contour curves show that the nonlinearity of the circuit is about the same range. However, the numbers on the contour curves can be deceptive: The nonlinearity should be given together with the transconductance value to make a fair comparison, since each point on each surface has a different transconductance value.

The contour curves give the results according to the way the circuit performances are programmed in the netlist. The standard deviation of the nonlinearity was taken without actually comparing the value to the transconductance of the circuit, hence, the comparison should be made by the designer.

Another possible discussion is made on the equivalent transconductance parameter, K_{eq} : This parameter is given by

$$K_{eq} = \left(\frac{1}{\sqrt{K_{n1}}} + \frac{1}{\sqrt{K_{p1}}} \right)^{-2} \quad (4.14)$$

thus, allows the analysis of K_{eq} in three cases:

- 1- $K_n=K_p$; both NMOS and PMOS transistors will be contributing to the transconductance of the circuit.
- 2- $K_n \gg K_p$ or $K_n \ll K_p$; either the NMOS or the PMOS transconductance parameter will be dominant in equation (4.14), hence, either the NMOS or the PMOS transistor will affect the transconductance of the circuit.

The nominal simulation results may be comparable for all three cases, however, statistically, their performances may be different. Therefore, it is important to statistically examine the circuit for the three cases. The statistical examination for all three cases were done, and the results showed no big difference on the statistical performances.

Another argument can be made on where to apply the input voltage of the circuit. The inputs can be the gates of the PMOS transistors, as well as the gates of the NMOS transistors. Statistical simulations show that applying the gates to either of them does not crucially affect the statistical performances of the circuit. However, from nominal simulation point of view, since NMOS transistors are faster than PMOS transistors, and because the output path for the transconductor with inputs on the PMOS pair is longer than the other, the circuit will be faster when the inputs are on the gates of the NMOS transistors. Only the case where the inputs are on the gates of the NMOS transistors are considered in this thesis.

4.2.3. Statistical Design of the Transconductor Using the Low Voltage Low Power CMOS Square-Law Composite Cell

The transconductor using the low voltage low power CMOS square-law composite cell as a main building block is shown in Figure 4.10 (also given in Figure 3.13).

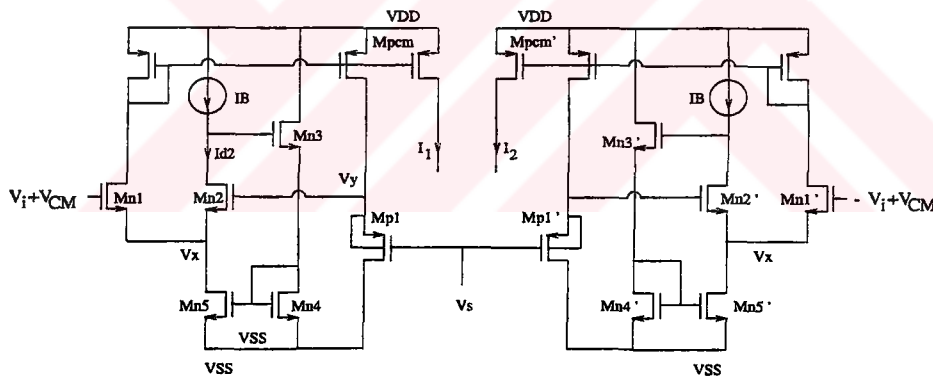


Figure 4.10: The transconductor using the low voltage low power CMOS square-law composite cell. The circuit description is given in detail in Section 3.2

The outline of the statistical design is the same as in the previous transconductor [45]; one can follow the same steps as before and obtain the contour curves for this circuit. The same circuit performances, offset and nonlinearity, are selected for this transconductor. The method presented in Section 4.2.1 is used for nonlinearity

measurement. The netlist of the circuit for statistical simulations is given in Appendix P, in the floppy disk attached to the thesis.

To start with, the same seven input variables of the low voltage low power CMOS square-law composite cell are selected for this transconductor. The two cells that are used to build the transconductor are identical. Therefore, each variable accounts for the same identical transistors of both cells; e.g., a_{n1} accounts for transistors M_{n1} and M_{n1}' .

The minimum and maximum areas assigned for the transistors are given in Table 4.13.

Table 4.13: Minimum and maximum area assignment for each transistor - transconductor using the low voltage low power CMOS square-law composite cell

Transistors	$M_{n1},$ M_{n1}'	$M_{n2},$ M_{n2}'	$M_{pcm},$ M_{pcm}'	$M_{n3},$ M_{n3}'	$M_{p1},$ M_{p1}'	$M_{n4,5},$ $M_{n4,5}'$	$M_{pcs},$ M_{pcs}'
Areas	a_{n1}	a_{n2}	a_{pcm}	a_{n3}	a_{p1}	$a_{n4,5}$	a_{pcs}
$(-1)\mu\text{m}^2$	10	200	450	1000	30	114	450
$(+1)\mu\text{m}^2$	50	1000	2250	5000	150	570	2250

The Plackett-Burman design matrix and simulation results for the transconductor is given in Table 4.14. Each run in the design matrix takes 24 seconds of CPU time on a HP 715/133 workstation.

The last two columns in the design matrix show the simulation results for the standard deviation of offset current and nonlinearity. The SS values and contribution of each transistor to offset and nonlinearity are given in Table 4.15.

Table 4.14: The Plackett-Burman design matrix and simulation results for offset current and nonlinearity - transconductor using the low voltage low power CMOS square-law composite cell

Runs	a_{n1}	a_{n2}	a_{pcm}	a_{n3}	a_{p1}	$a_{n4,5}$	a_{pcs}	$\sigma(I_{offset})$ (μA)	$\sigma(\alpha_1)$ ($\mu A/V^2$)
1	1	-1	-1	1	-1	1	1	0.3216	0.5567
2	1	1	-1	-1	1	-1	1	0.2856	0.5412
3	1	1	1	-1	-1	1	-1	0.2676	0.3389
4	-1	1	1	1	-1	-1	1	0.4110	0.3974
5	1	-1	1	1	1	-1	-1	0.1307	0.2388
6	-1	1	-1	1	1	1	-1	0.4023	0.5865
7	-1	-1	1	-1	1	1	1	0.2417	0.3012
8	-1	-1	-1	-1	-1	-1	-1	0.4703	0.7376

Table 4.15: SS values and contribution of each transistor - transconductor using the low voltage low power CMOS square-law composite cell

Variables	SS (offset current)	Contribution (%) (offset current)	SS (nonlinearity)	Contribution (%) (Nonlinearity)
a_{n1}	3.3787×10^{-14}	40.49	1.5058×10^{-14}	7.47
a_{n2}	5.1190×10^{-15}	6.13	1.1051×10^{-16}	0.05
a_{pcm}	2.2980×10^{-14}	27.54	1.6405×10^{-13}	81.35
a_{n3}	3.3183×10^{-20}	0.01	2.4339×10^{-15}	1.21
a_{p1}	2.1030×10^{-14}	25.20	1.6466×10^{-14}	8.16
$a_{n4,n5}$	5.1971×10^{-16}	0.61	2.1672×10^{-15}	1.07
a_{pcs}	1.4939×10^{-176}	0.02	1.3820×10^{-15}	0.69

The same three transistors as in the low voltage transconductor seem to be contributing the most, thus, will be considered in the next step of the statistical design methodology.

Table 4.16 shows the Box-Behnken design matrix and simulation results for the two statistical performances. Each run in the design matrix takes about 24 seconds of CPU time on a HP 715/133 workstation.

The empirical model for the transconductor using the low voltage CMOS square-law composite cell is obtained by applying the Box-Behnken design matrix to the statistical software Minitab.

The empirical models for the offset current and nonlinearity, respectively, are given as

$$\begin{aligned}\sigma(I_{\text{offset}}) = & 0.6740 - 0.8596a_{n1} - 0.0207a_{\text{pcm}} - 0.2524a_{p1} + 0.8848a_{n1}^2 \\ & + 0.0005a_{\text{pcm}}^2 + 0.0814a_{p1}^2 + 0.0012a_{n1}a_{\text{pcm}} + 0.0210a_{n1}a_{p1} \\ & + 0.0021a_{\text{pcm}}a_{p1}\end{aligned}\quad (4.15)$$

$$\begin{aligned}\sigma(\alpha_1) = & 0.9142 - 0.4658a_{n1} - 0.0378a_{\text{pcm}} - 0.3149a_{p1} + 0.5364a_{n1}^2 \\ & + 0.0011a_{\text{pcm}}^2 + 0.1252a_{p1}^2 - 0.0075a_{n1}a_{\text{pcm}} + 0.0758a_{n1}a_{p1} \\ & - 0.0022a_{\text{pcm}}a_{p1}\end{aligned}\quad (4.16)$$

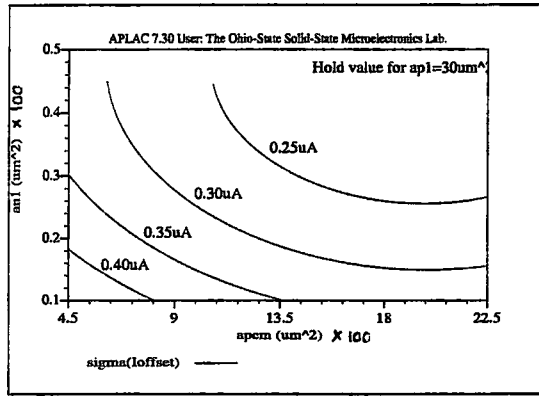
The empirical models for the offset current and nonlinearity have an accuracy of 99.7% and 99.5%, respectively.

The models are valid for the ranges of $[10\mu\text{m}^2, 50\mu\text{m}^2]$, $[450\mu\text{m}^2, 2250\mu\text{m}^2]$ and $[30\mu\text{m}^2, 150\mu\text{m}^2]$, for a_{n1} , a_{pcm} and a_{p1} , respectively. All the terms in both models have a valid “T” value, which helps to improve the accuracy of the model.

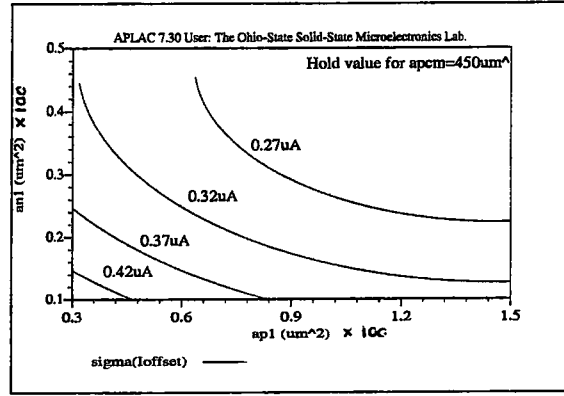
The empirical models given in equations (4.15) and (4.16) are used to obtain the response surfaces for the transconductor. First the offset current will be examined. The contour curves for offset current and nonlinearity are given in Figure 4.11 and Figure 4.12, respectively.

Table 4.16: The Box-Behnken design matrix and simulation results for offset current and nonlinearity - transconductor using the low voltage low power square-law composite cell

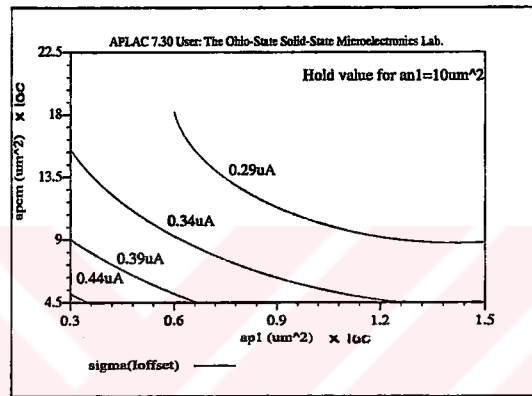
Run	a_{n1}	a_{pcm}	a_{p1}	$\sigma(I_{\text{offset}})$ (μA)	$\sigma(\alpha_1)$ ($\mu\text{A}/\text{V}^2$)
1	-1	-1	0	0.3567	0.5284
2	1	-1	0	0.2426	0.4898
3	-1	1	0	0.2465	0.3461
4	1	1	0	0.1413	0.2536
5	0	0	0	0.1706	0.2980
6	0	-1	-1	0.3548	0.5908
7	0	1	-1	0.2178	0.3781
8	0	-1	1	0.2412	0.5020
9	0	1	1	0.1489	0.2415
10	0	0	0	0.1732	0.3069
11	-1	0	-1	0.3444	0.4674
12	1	0	-1	0.2146	0.3734
13	-1	0	1	0.2586	0.3299
14	1	0	1	0.1389	0.2723
15	0	0	0	0.1796	0.2777



(a)



(b)



(c)

Figure 4.11: Response surfaces for the offset current of the transconductor using the low voltage low power CMOS square-law composite cell; a) a_{n1} vs. a_{pcm} ($a_{p1}=30\mu\text{m}^2$), b) a_{n1} vs. a_{p1} ($a_{pcm}=450\mu\text{m}^2$), and c) a_{pcm} vs. a_{p1} ($a_{n1}=10\mu\text{m}^2$)

The offset current was found “0” from the transfer curve given in Figure 3.14. The statistical simulations show that the standard deviation of the offset current is in the μA ranges, despite what was seen from the transfer curve. The statistical analysis results prove important, since they include the effect of the random process variations.

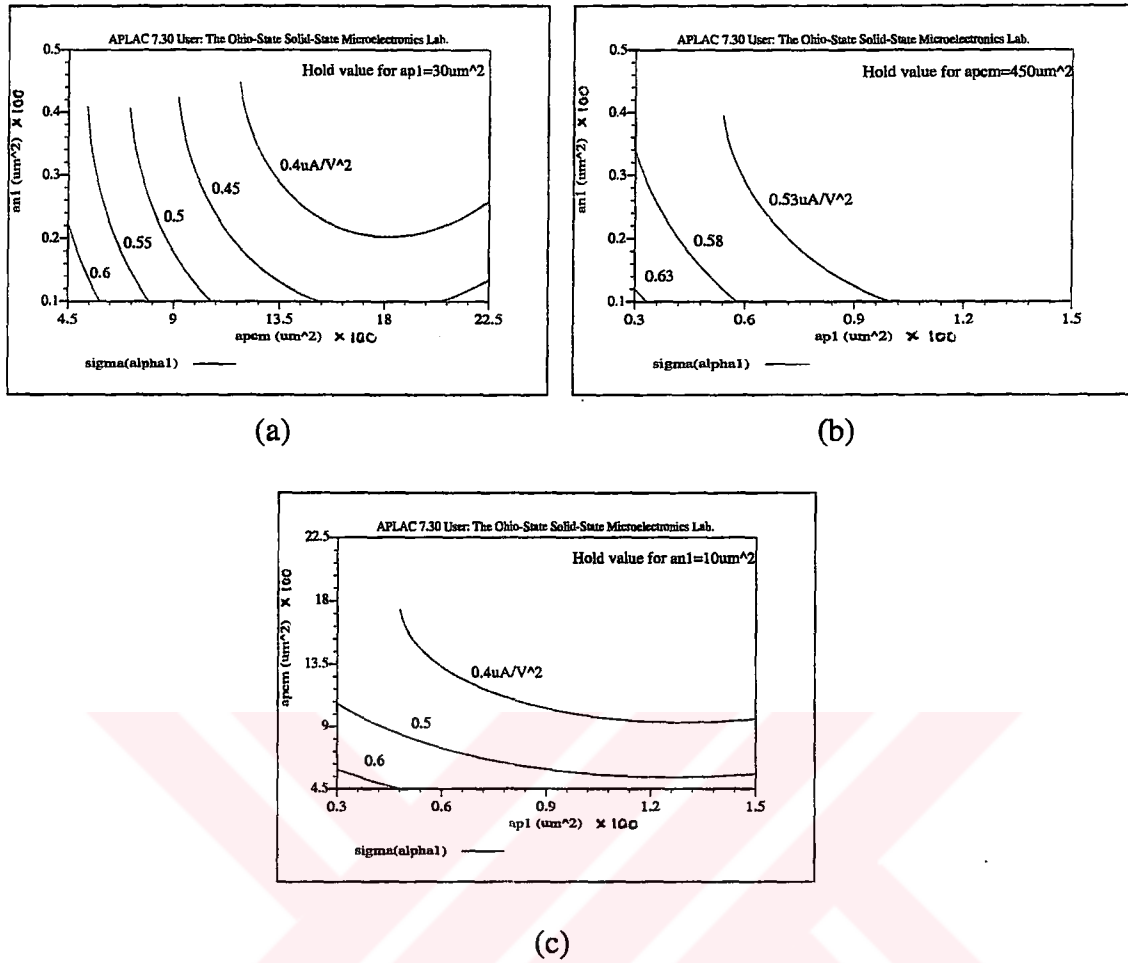


Figure 4.12: Response surfaces for the nonlinearity of the transconductor using the low voltage low power CMOS square-law composite cell; a) a_{n1} vs. a_{pcm} ($a_{p1}=30\mu m^2$), b) a_{n1} vs. a_{p1} ($a_{pcm}=450\mu m^2$), and c) a_{pcm} vs. a_{p1} ($a_{n1}=10\mu m^2$)

The contour curves for nonlinearity should be evaluated together with the transconductance of the circuit, as explained in the previous section.

The contours shown in Figure 4.11 and Figure 4.12 help estimate the effect of random variations on the circuit performances. The contours also provide information regarding which areas are preferable for a better standard deviation. A preferable standard deviation is a smaller one, however, areas that correspond to the smallest standard deviation do not always give the best results. The designer will make the final decision, regarding the size of the transistors.

The nonlinearity, on the other hand, is measured using the method described in Section 4.2.1. The transfer curve shows a low nonlinearity, since the nominal simulations do not consider the random process variations. The transfer curve will be very linear, thus, keeping the nonlinearity low. The statistical simulations include the random variations, hence, they will show how much the results will deviate from the nominal simulation results.

The next section will go through the statistical analysis of the multipliers that were described in Section 3.3.

4.3. Statistical Design of the Low Voltage and Low Power Multipliers

This chapter started with the statistical analysis of two composite cells, in which, one of them had an advantage over the other, of being suitable for low power applications. The transconductors were built by using the cells as their building blocks, thus, the effort was put to build the cells, and the cells were used to build the transconductors. This type of component reuse is the final goal of the research in the analog programmability area. This effort was also used to build multipliers by using the cells as main building blocks. The description of these multipliers were given in Chapter 3. This chapter deals with the statistical analysis of the multipliers.

The same performances as in the transconductors are considered for the multiplier circuits: Offset current and nonlinearity. Matching is even more important for the

Table 4.17: Minimum and maximum area assignment for each transistor - multiplier using the low voltage CMOS square-law composite cell

Transistors	$M_{n11-n14}$	$M_{n21-n24}$	$M_{pcm1-pcm4}$	$M_{p11-p14}$	$M_{ncs1-ncs4}$
Areas	a_{n1}	a_{n2}	a_{pcm}	a_{p1}	a_{ncs}
$(-1)\mu m^2$	10	200	450	30	114
$(+1)\mu m^2$	50	1000	2250	150	570

The multiplier consists of four low voltage composite cells, which are all identical. The same transistors in the four cells are grouped under the same variable name, e.g., the variable a_{n1} stands for transistors M_{n11} , M_{n12} , M_{n13} and M_{n14} in the multiplier. As seen from Table 4.17, five input variables are selected as the input variables of the Plackett-Burman design matrix. The Plackett-Burman design matrix, is shown in Table 4.18. Each run in the design matrix takes about 33 seconds of CPU time on a HP 715/133 workstation. The last two column of the design matrix show the simulation results for offset current and nonlinearity, respectively. The netlist of the statistical simulations is given in Appendix R, in the floppy disk attached to the thesis.

The SS values and the contribution of the transistors to offset current and nonlinearity are calculated, and are given in Table 4.19. Three variables are screened out for both performances, however, the three variables are not the same. Therefore, the next step of the statistical methodology, the Box-Behnken design matrix, will run separately for the two performances, offset current and nonlinearity.

Table 4.18: The Plackett-Burman design matrix and simulation results for offset current and nonlinearity - multiplier using the low voltage CMOS square-law composite cell

Runs	a_{n1}	a_{n2}	a_{pcm}	a_{p1}	a_{ncs}	$\sigma(I_{offset})$ (μA)	$\sigma(\alpha_1)$ ($\mu A/V^2$)
1	1	-1	-1	1	-1	0.9378	0.9055
2	1	1	-1	-1	1	1.2002	0.7318
3	1	1	1	-1	-1	1.3659	0.6455
4	-1	1	1	1	-1	1.3721	0.6359
5	1	-1	1	1	1	9.6707	0.6274
6	-1	1	-1	1	1	1.3637	0.7315
7	-1	-1	1	-1	1	1.3719	0.6426
8	-1	-1	-1	-1	-1	1.4473	0.8961

Table 4.19: SS values and contribution of each transistor - multiplier using the low voltage CMOS square-law composite cell

Variables	SS (offset current)	Contribution (%) (offset current)	SS (nonlinearity)	Contribution (%) (Nonlinearity)
a_{n1}	1.4689×10^{-13}	55.21	2.1157×10^{-18}	0.01
a_{n2}	4.1724×10^{-14}	15.68	1.3360×10^{-14}	14.47
a_{pcm}	2.0476×10^{-15}	0.77	6.3658×10^{-14}	68.94
a_{p1}	6.9310×10^{-14}	26.05	3.0873×10^{-17}	0.02
a_{ncs}	6.0611×10^{-15}	2.28	1.5287×10^{-14}	16.56

The Box-Behnken design matrix and simulation results for offset current and nonlinearity are given in Table 4.20 and Table 4.21, respectively. Each run in the design matrices take about 33 seconds of CPU time on a HP 715/133 workstation.

Table 4.20: The Box-Behnken design matrix and simulation results for offset current - multiplier using the low voltage square-law composite cell

Run	a_{n1}	a_{n2}	a_{p1}	$\sigma(I_{\text{offset}})$ (μA)
1	-1	-1	0	1.1687
2	1	-1	0	1.0293
3	-1	1	0	1.4007
4	1	1	0	1.1501
5	0	0	0	1.1061
6	0	-1	-1	1.2049
7	0	1	-1	1.3222
8	0	-1	1	0.9578
9	0	1	1	1.0937
10	0	0	0	1.1976
11	-1	0	-1	1.5256
12	1	0	-1	1.3306
13	-1	0	1	1.2549
14	1	0	1	1.1118
15	0	0	0	1.2004

The Box-Behnken design matrices were applied to the statistical software Minitab, and the empirical models that represent the circuit for the two performances were obtained:

$$\begin{aligned} \sigma(I_{\text{offset}}) = & 1.499 - 1.696a_{n1} + 0.081a_{n2} - 0.483a_{p1} + 2.254a_{n1}^2 \\ & - 0.004a_{n2}^2 + 0.132a_{p1}^2 - 0.035a_{n1}a_{n2} + 0.108a_{n1}a_{p1} \end{aligned} \quad (4.17)$$

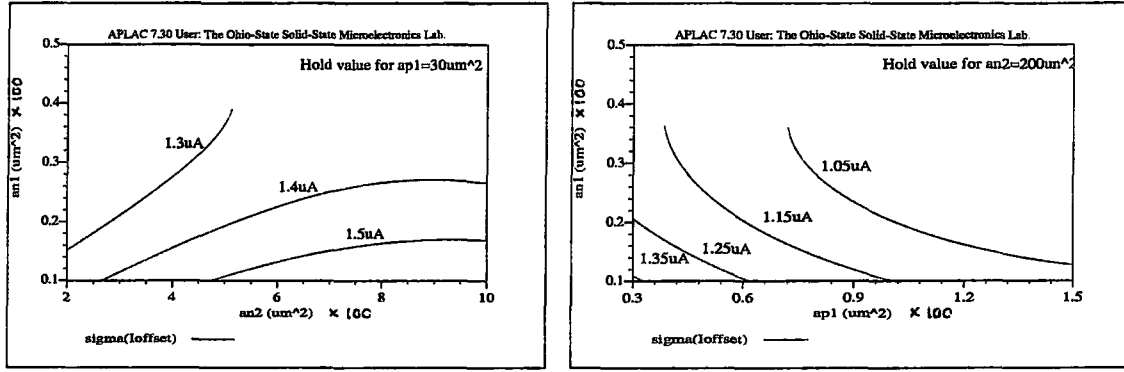
$$\begin{aligned} \sigma(\alpha_1) = & 1.03761 - 0.0373a_{n2} - 0.03135a_{pcm} + 0.00112a_{n2}^2 \\ & + 0.00073a_{pcm}^2 + 0.00091a_{n2}a_{pcm} \end{aligned} \quad (4.18)$$

Table 4.21: The Box-Behnken design matrix and simulation results for nonlinearity - multiplier using the low voltage square-law composite cell

Run	a_{n2}	a_{pcm}	a_{ncs}	$\sigma(\alpha_1) (\mu A/V^2)$
1	-1	-1	0	0.8726
2	1	-1	0	0.6970
3	-1	1	0	0.6858
4	1	1	0	0.6409
5	0	0	0	0.6657
6	0	-1	-1	0.7486
7	0	1	-1	0.6666
8	0	-1	1	0.7273
9	0	1	1	0.6647
10	0	0	0	0.6380
11	-1	0	-1	0.6846
12	1	0	-1	0.6247
13	-1	0	1	0.6877
14	1	0	1	0.6449
15	0	0	0	0.6374

The “T” values for the term $a_{n2}a_{p1}$ in equation (4.17) is in the invalid range, thus, this term is not included in the empirical model. The terms related to a_{ncs} are also excluded from the empirical model in equation (4.18), for the same reason. The empirical models for offset current and nonlinearity have an accuracy of 97.6% and 93.1%, respectively.

Figure 4.14 shows the contour curves that are obtained for the offset current.



(a)

(b)

Figure 4.14: Response surfaces for the nonlinearity of the multiplier using the low voltage CMOS square-law composite cell; a) a_{n1} vs. a_{n2} ($a_{p1}=30\mu m^2$), b) a_{n1} vs. a_{p1} ($a_{pcm}=200\mu m^2$)

The offset current is read “0” from the transfer curve given in Figure 3.16, whereas the standard deviation of the offset current is in the μA ranges. The nominal simulations do not consider the effect of random process variations, whereas this effect may be important. The statistical simulations prove this importance.

The usage of the contours were discussed in detail previously and, thus, will not be examined again.

Figure 4.15 shows the contour curves for the nonlinearity of the circuit.

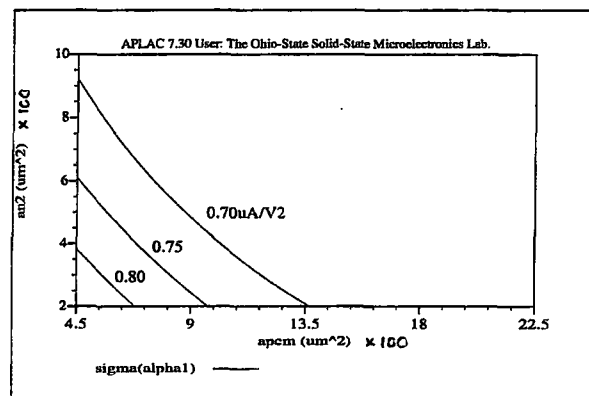


Figure 4.15: Response surfaces for the nonlinearity of the multiplier using the low voltage CMOS square-law composite cell; a_{n2} vs. a_{pcm}

Note that all the terms regarding the third contributing variable were excluded from the empirical model, therefore the contour curves are obtained for one pair of variables. The contours show a high variation in the nonlinearity. The nonlinearity that was read from the transfer curve in Figure 3.16 was $0.05\mu\text{A}/\text{V}^2$, which is very small. Compared to the nonlinearity variation in the transconductors, the results are even higher; the deviation is almost twice as the deviation of the transconductor. The truth is matching of the transistors is even more important for the multiplier. The transconductor has two cells connected whereas the multiplier has four them. This makes the matching requirement of the multipliers higher.

The statistical design of the multiplier using the low voltage low power CMOS square-law composite cell is explained next.

4.3.2. Statistical Design of the Multiplier Using the Low Voltage Low Power CMOS Square-Law Composite Cell

The multiplier using the low voltage low power CMOS square-law composite cell is illustrated in Figure 4.16.

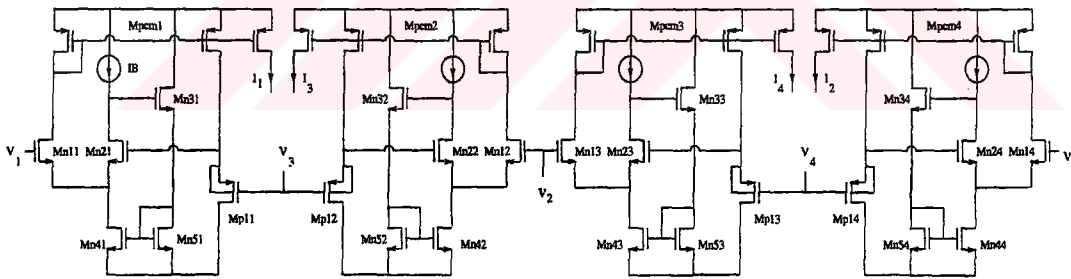


Figure 4.16: The multiplier using the low voltage low power CMOS square-law composite cell. The circuit description is given in detail in Section 3.3

The multiplier consists of four cells connected together; the cells had seven input variables, thus, the multiplier will have the same number of variables. Table 4.22 shows the first step of the statistical design of the multiplier [49]; the minimum and maximum area assignment for each transistor in the circuit.

Table 4.22: Minimum and maximum area assignment for each transistor - multiplier using the low voltage low power CMOS square-law composite cell

Transistors	M_{n11} - M_{n14}	M_{n21} - M_{n24}	M_{pcm1} - M_{pcm4}	M_{n31} - M_{n34}	M_{p11} - M_{p14}	$M_{n(4,5)1}$ - $M_{n(4,5)4}$	M_{pcs1} - M_{pcs4}
Areas	a_{n1}	a_{n2}	a_{pcm}	a_{n3}	a_{p1}	$a_{n4,5}$	a_{pcs}
$(-1)\mu\text{m}^2$	10	200	450	1000	30	114	450
$(+1)\mu\text{m}^2$	50	1000	2250	5000	150	570	2250

The same transistors in the four cells are grouped together under one variable name, as in the previous multiplier. These minimum and maximum area limits are applied to the transistors during the Plackett-Burman runs.

Table 4.23 shows the Plackett-Burman design matrix and simulation results for the offset current and nonlinearity. Each run in the design matrix takes about 50 seconds of CPU time on a HP 715/133 workstation.

Table 4.23: The Plackett-Burman design matrix and simulation results for offset current and nonlinearity - multiplier using the low voltage low power CMOS square-law composite cell

Runs	a_{n1}	a_{n2}	a_{pcm}	a_{n3}	a_{p1}	$a_{n4,5}$	a_{pcs}	$\sigma(I_{\text{offset}})$ (μA)	$\sigma(\alpha_1)$ ($\mu\text{A}/\text{V}^2$)
1	1	-1	-1	1	-1	1	1	1.2645	0.1413
2	1	1	-1	-1	1	-1	1	0.8247	1.7176
3	1	1	1	-1	-1	1	-1	1.2364	0.7526
4	-1	1	1	1	-1	-1	1	1.2738	1.4531
5	1	-1	1	1	1	-1	-1	0.7823	0.1405
6	-1	1	-1	1	1	1	-1	0.8583	2.0475
7	-1	-1	1	-1	1	1	1	0.7834	0.1768
8	-1	-1	-1	-1	-1	-1	-1	1.2989	0.2695

The SS values and the contribution of each transistor for the offset current and nonlinearity are shown in Table 4.24.

Table 4.24: SS values and contribution of each transistor - multiplier using the low voltage low power CMOS square-law composite cell

Variables	SS (offset current)	Contribution (%) (offset current)	SS (nonlinearity)	Contribution (%) (Nonlinearity)
a_{n1}	1.4156×10^{-15}	0.34	1.7851×10^{-13}	4.10
a_{n2}	5.1383×10^{-16}	0.12	3.4358×10^{-12}	78.90
a_{pcm}	3.6208×10^{-15}	0.86	3.4149×10^{-13}	7.84
a_{n3}	1.5691×10^{-16}	0.04	9.3713×10^{-14}	2.15
a_{p1}	4.1631×10^{-13}	98.58	2.6865×10^{-13}	6.17
$a_{n4,n5}$	1.7178×10^{-16}	0.04	2.6731×10^{-14}	0.61
a_{pcs}	1.0967×10^{-16}	0.03	9.7171×10^{-15}	0.22

From Table 4.24, the offset current is mainly affected by the PMOS transistors in the circuit. Therefore the designer should concentrate on the size of the PMOS transistors and also try to match all four of them. The methodology will not proceed for the offset current, since there is only one main contribution to the performance. The statistical method will proceed for the nonlinearity, though, as previously.

The Box-Behnken design matrix and simulation results for the nonlinearity performance is given in Table 4.25. Each run in the table takes about 50 seconds of CPU time on a HP 715/133 workstation.

The netlist of the statistical simulations is given in Appendix S, in the floppy disk attached to the thesis.

Table 4.25: The Box-Behnken design matrix and simulation results for nonlinearity - multiplier using the low voltage low power square-law composite cell

Run	a_{n2}	a_{pcm}	a_{p1}	$\sigma(\alpha_1)$ ($\mu A/V^2$)
1	-1	-1	0	0.4032
2	1	-1	0	2.0059
3	-1	1	0	0.2992
4	1	1	0	1.4713
5	0	0	0	1.1107
6	0	-1	-1	1.9459
7	0	1	-1	1.0602
8	0	-1	1	1.8164
9	0	1	1	1.0253
10	0	0	0	1.1213
11	-1	0	-1	1.8787
12	1	0	-1	1.3056
13	-1	0	1	1.5634
14	1	0	1	1.4529
15	0	0	0	1.0688

The Box-Behnken design matrix and simulation results are applied to the statistical tool Minitab, to obtain the empirical model for the nonlinearity performance of the multiplier. The empirical model is given as

$$\begin{aligned} \sigma(\alpha_1) = & 0.4617 + 0.4639a_{n2} - 0.1233a_{pcm} - 0.04123a_{p1} - 0.0232a_{n2}^2 \\ & + 0.0039a_{pcm}^2 - 0.0030a_{n2}a_{pcm} \end{aligned} \quad (4.19)$$

The square term and interaction terms related to a_{p1} are not included in the model since their “T” value was not in the valid range.

The contour curves were obtained for the a_{n2} - a_{pcm} pair, and are shown in Figure 4.17.

Figure 4.17: Response surfaces for the nonlinearity of the multiplier using the low voltage low power CMOS square-law composite cell; a_{n2} vs. a_{pcm}

The contour curve given in Figure 4.17 might be deceptive; one can ask why the lower curve has a lower standard deviation and the higher curve a lower standard deviation. Simply, the lower curve corresponds to higher areas of a_{pcm} , whereas the curve that covers the $2\mu A/V^2$ curve is not too long anyway. Thus, the lower curve has the highest areas and the lowest standard deviation which agrees with Pelgrom's equation for the standard deviation.

The nonlinearity was found as $0.05\mu A/V^2$ from the transfer curve, whereas the contour curves obtained from the statistical simulations show a much higher value. As mentioned in the previous sections and chapter, the statistical analysis includes the random process variations, thus, gives more realistic results. One should consider statistical analysis to get the feel of the functional yield and the standard deviation of the circuit performances.

The next section is a brief summary on the composite cells, transconductors, and multipliers.

4.4. Summary - Statistical Design of Composite Cells, Transconductors and Multipliers

The statistical analysis results of two low voltage and low power composite cells, two transconductors and two multipliers that were built using these composite cells are explained in detail, so far. Not only the circuits alone, but the comparison of the circuits is important too, since the concept of analog programmability is also being discussed. The analog programmability, in other words, using analog blocks to build more complex circuits is an ongoing discussion, and the ultimate goal in the analog CAD research area. This idea is discussed in this thesis, by building transconductors and multipliers using the composite cells as main building blocks. Since effort is put when designing the cells, with optimum transistor sizing, no effort is needed when designing the new transconductors and multipliers that will use the composite cells. The transconductors and multipliers are not the best ever circuits, but will be suitable for certain specifications. The circuits may have more transistors than other transconductor or multiplier circuits, but the advantage is that there was almost no design time required, since the cells were already optimized.

The layout of the circuits will be probably larger than some other transconductor or multiplier circuits; the area is sacrificed to design time.

The six circuits were statistically examined and compared to each other. The two composite cells, two transconductors and two multipliers do not show a big advantage over the other, when compared to each other. However, the comparison of the transconductors and multipliers show some variation: The low voltage low power composite cell and the circuits using this cell has an additional feedback loop, which complicates the circuits, however, the results show that this feedback loop does not degrade the robustness of the circuits; their contribution to the circuit performances are relatively low. The transconductors use two composite cells whereas the multipliers have four of them. This increases the matching requirement of the multipliers. The main NMOS and PMOS transistors in the composite cells have to be matched two times for

not be very wide. The yield may be the same as before optimizing the circuit, but since the variation in the output performance is smaller, the yield will be actually enhanced. Examples, for selecting a specification for the output performance, and connecting this to the yield was given throughout the previous sections.

However, the smallest standard deviation on the contour curves do not necessarily mean those transistor sizes are the best fit for the circuit. The methodology is used to make a robust design of the circuits, and the contour curves give the flexibility of selecting the optimum transistor sizes; however, the correct transistor size is the designers' decision to make, since the designer has the best feel for the facts of the circuit. The methodology, however, definitely will help ease the task of the designer. It is noteworthy that it is the first time that the statistical tools and the SMOS model, together, are used in the statistical analysis of analog circuits.

So far, the circuits were not fabricated, thus, the results of the statistical analysis of the circuits were evaluated from the contour curves that were obtained.

The next two sections examine the statistical analysis of the four-MOSFET structure and the 10-bit current division network. These two circuits were fabricated through MOSIS, hence, experimental results are also included in each section.

4.5. Statistical Design of the Four-MOSFET Structure

Figure 4.18 shows the four-MOSFET structure that is statistically examined [61] in this section.

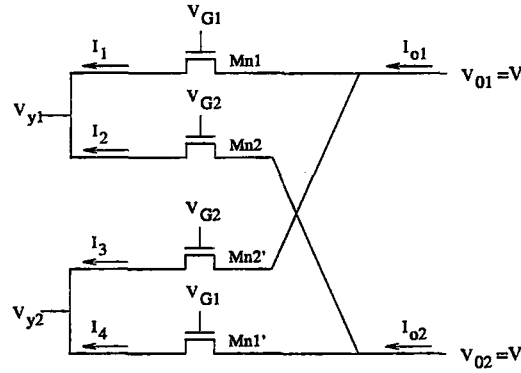


Figure 4.18: The four-MOSFET structure. The description of the circuit is given in Section 3.4.

The circuit can be used in filter applications. In that case it will determine the linearity of the filter. The power dissipation of the filter will be determined by the operational amplifier that is connected to the output of the four-MOSFET structure, thus, the four-MOSFET structure will not degrade the power dissipation performance of the overall filter circuit. The four-MOSFET structure fulfills the resistor part of the filter. If a single resistor is used for the linearity purpose tuning wouldn't be possible, and if a single MOS transistor is used, linearity wouldn't be achieved. It was demonstrated that a four-MOSFET structure fully suppresses the even and odd-order nonlinearity terms [26, 27]. However, recent works question the widely accepted superiority of the four-MOSFET structure [28]. The result of the discussion is important because the supposed linearity properties of the four-MOSFET structure is served to justify its use in several recent applications [29, 30].

For exact cancellation of nonlinearities, exact transistor matching is needed, whereas, random variations may not always allow for exact matching of transistors. The circuit performances that are to be examined are the offset and nonlinearity, as in the transconductor and multiplier circuits discussed previously. The nonlinearity measurement method was explained in Section 4.1.

The statistical design methodology given in Chapter 2 is valid for all circuits that have more than one variable. The four-MOSFET structure transistors all have the same sizing, thus, they will be grouped as one, hence, the circuit has only one variable. The SMOS model and the Monte Carlo analysis will be used to make the statistical analysis of the four-MOSFET circuit. The SMOS model and the Monte Carlo analysis was used in the analysis of the previous circuits as well, with the addition of the statistical techniques. The Plackett-Burman design matrix is used to screen out the most contributing variables to the circuit performance, and the Box-Behnken experiment is run to build an empirical model with at least two variables. Since there is only one variable in this case, there is no reason for screening out the most contributing transistors, thus, there is no reason for going through the Plackett-Burman and Box-Behnken experiments.

The statistical netlist of the four-MOSFET structure is given in Appendix T, in the floppy disk attached to the thesis. The circuit is also fabricated through the MOSIS 2 μ m process. The statistical simulation, and experimental results are given in this section, respectively.

4.5.1. Statistical Simulation Results

The statistical simulations were done for different sizing of the transistors. The results were put together, and are illustrated in the figures of this section. Offset and nonlinearity are the two circuit performances that are statistically examined.

The nominal simulations show an offset of "0", and the nonlinearity that is calculated from the transfer curves for different sizing of transistors is very low, however, nominal simulations do not include the random process variations, thus, the effect of these variations are not reflected to the results.

Seven runs are made to complete the statistical simulations of the four-MOSFET structure; each run keeps the channel width of the transistors same, and varies the channel length, thus, the area of the transistors are different for each run. Each run takes about 28 seconds of CPU time on a HP 715/133 workstation. Results are obtained for the standard deviation of the offset and nonlinearity performance of the circuit.

Figure 4.19 shows the statistical simulation results for the offset.

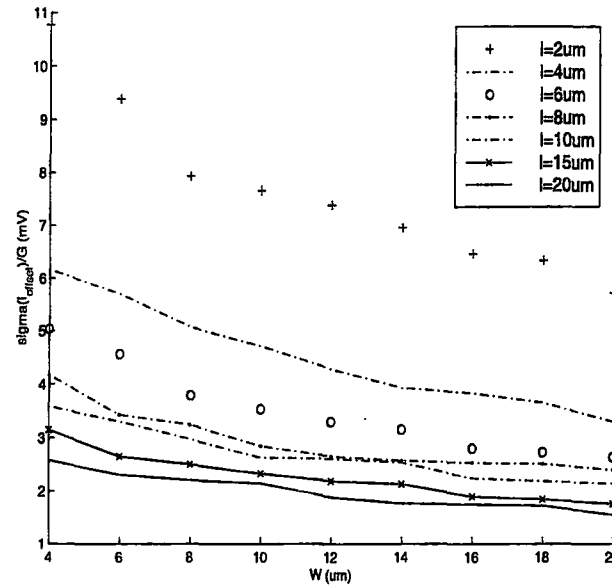


Figure 4.19: Statistical simulation results for the standard deviation of offset vs. channel width. Each contour represents different values of channel lengths.

The x axis on Figure 4.19 shows the channel width of transistors. Each contour curve shows different channel lengths, thus, it is possible to find the deviation of the offset for different sizing of transistors.

As the channel width of the transistors increases, it is expected to have better matching properties. However, increasing the channel width also increases the transconductance. Let us assume that we are trying to achieve a certain transconductance value, and that to achieve this goal we need a W/L value of 2. It is possible to achieve this ratio by selecting $W/L=4/2, 8/4, 12/6$, etc., hence, the standard deviation of each aspect ratio should be compared and perhaps the lowest standard deviation should be selected.

The y axis in Figure 4.19 shows the standard deviation of the offset, over the transconductance value ($\sigma(I_{\text{offset}})/G$). For instance, if the circuit requires an aspect ratio of 2 to achieve a certain transconductance value, it is possible to directly compare the y axis values for $W/L=8/4, 16/8, 20/10$, etc.

It is seen from Figure 4.19 that the standard deviation is decreasing as we increase the area. The curves also show that as the channel length increases, the reduction in the standard deviation of the offset is somehow saturated. It is easy to see this by comparing the curves for $L=2\mu\text{m}$ and $L=20\mu\text{m}$. The tendency of the decrease degrades for smaller channel lengths.

The statistical simulation results for the nonlinearity performance of the circuit is illustrated in Figure 4.20.

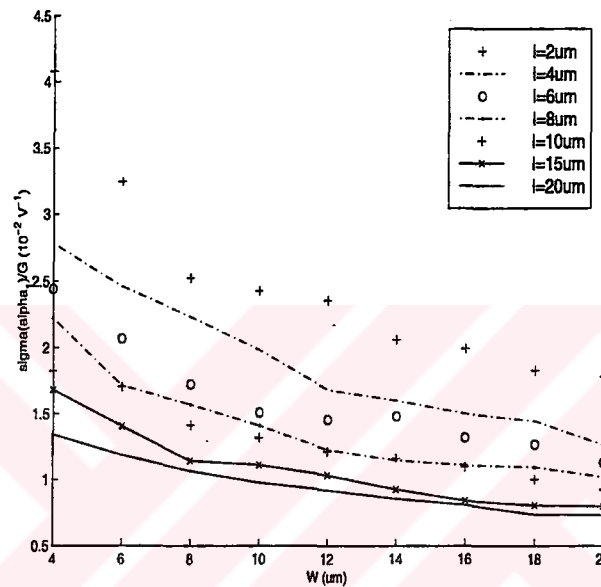


Figure 4.20: Statistical simulation results for the standard deviation of nonlinearity vs. channel width. Each contour represents different values of channel lengths.

The y axis shows the standard deviation for the nonlinearity of the circuit, and the x axis shows different W values. Each contour curve represents a different channel length value.

The constant transconductance is important for the nonlinearity performance as well. The y axis in Figure 4.20 shows the standard deviation of the nonlinearity over the transconductance. The same way of thinking as in the offset case, can be applied to the nonlinearity evaluation too. The nonlinearity is high for smaller areas and as the channel length increases the tendency of the standard deviation reduction also decreases.

Overall, for the considered transistor sizings, it is possible to reduce the nonlinearity variation to less than 1% by the appropriate sizing of transistors. Yet, it is the designers decision to make if the sizing for the least standard deviation is suitable for the circuit.

The goal of the statistical analysis of the four-MOSFET structure is to find the quantitative measure of mismatch on linearity and offset through the contour curves as given in Figures 4.19 and 4.20. It is possible to achieve good offset and linearity performance by selecting the appropriate W and L values for the transistors in the circuit.

The statistical simulation results for the four-MOSFET structure were given in this section. The experimental results are provided next.

4.5.2. Experimental Results

The four-MOSFET structure was fabricated through the MOSIS 2 μ m process. To get accurate statistical experimental results, it is necessary to fabricate as much samples of the circuit as possible, and preferably with different aspect ratios too. In this work, two aspect ratios as W/L=4/4 and W/L=20/4 were fabricated. 7 samples of the four-MOSFET structure with the aspect ratio of 4/4, and 32 samples for the aspect ratio of 20/4 were fabricated on 4 tiny MOSIS chips. The total number of the samples are therefore 28 for W/L=4/4 and 32 for W/L=20/4. The number of the samples are limited because of the limited number of input and output pins of the chip. Due to the fact that this work is mainly focusing on the intra-die variations, the standard deviation for each tiny chip is measured separately. The average of all the standard deviations are, however, also reported.

Measurements were taken using the HP4145B parameter analyzer. The offset was measured from the transfer curve of each circuit; the nonlinearity, on the other hand was calculated by measuring three points from the transfer curves, as described in Section 4.1. The average transconductance of the circuit with W/L=4/4 and W/L=20/4 is measured as 28 μ A/V² and 140 μ A/V², respectively.

To get statistical data, the mean and the standard deviation of the offset and nonlinearity, for both aspect ratios of the circuit on the four chips were calculated. The normal distribution of the measurement data was obtained with the help of the statistical software Minitab.

We will first concentrate on the results for the offset of the four-MOSFET structure.

Figure 4.21 shows the histogram and normal distribution of the measurement results that were taken from the four tiny chips, for the offset of the four-MOSFET structure with $W/L=4/4$. Table 4.26 shows the mean and standard deviation for each tiny chip.

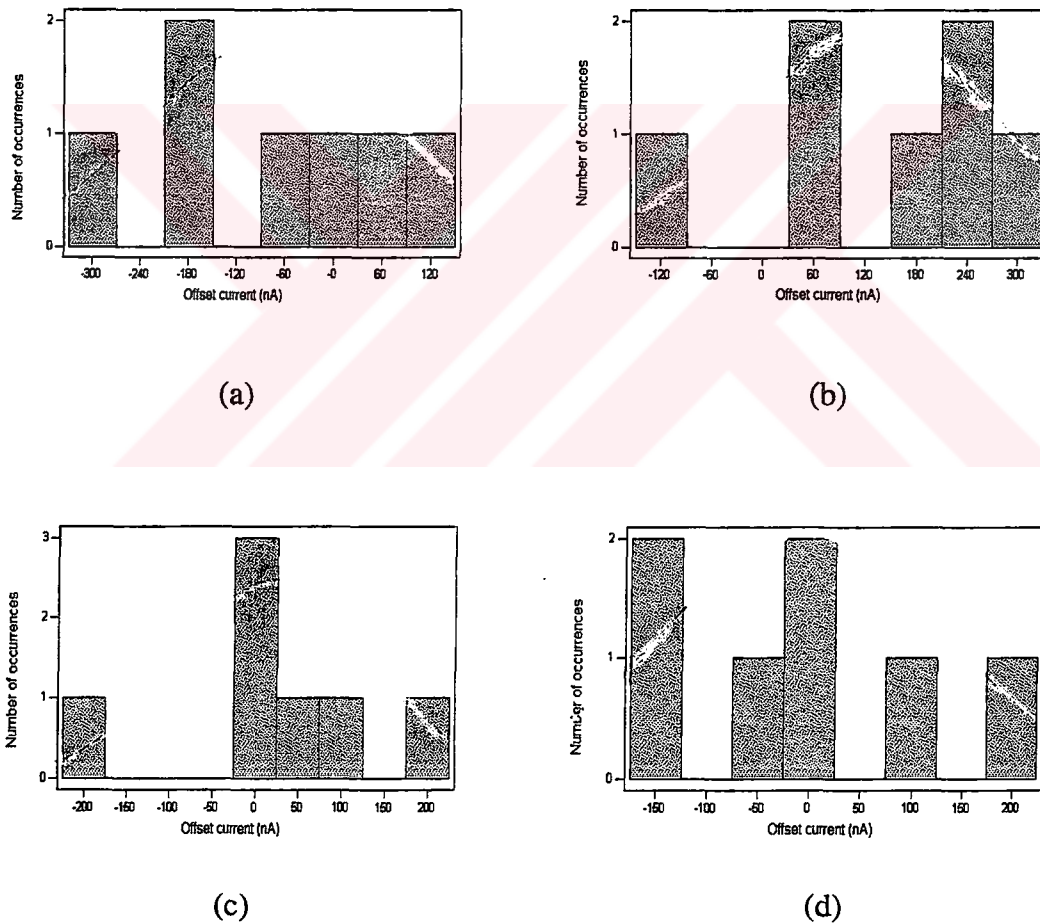


Figure 4.21: Experimental results for the offset of the four-MOSFET structure on four tiny chips ($W/L=4/4$). The histogram in each item is obtained for 7 examples.

Table 4.26: The mean and standard deviation for the offset of the four-MOSFET structure on four tiny chips ($W/L=4/4$, $G=28\mu A/V^2$)

offset ($W/L=4/4$)	Chip A	Chip B	Chip C	Chip D
mean (nA)	-78.0657	130.1143	22.2728	-4.9143
standard deviation/G (mV)	5.6303	5.3191	4.18	4.98

The x axis of the normal distributions in Figure 4.21 show the measured offset values, and the y axis shows the number of occurrences. The normal distribution is drawn over the histogram of the measurement results. The histogram automatically groups the measurement results in small intervals. The offset of all the circuits on four chips were measured, and the data was taken to calculate the mean and standard deviation for both aspect ratios.

The standard deviation for the offset was simulated as 6.1mV in Figure 4.19. From Table 4.26, the experimental results for Chip A and Chip B are relatively close to the simulated value, and the results of Chip C and Chip D seem to deviate. There may be several reasons for this deviation: Any error that is due to the equipment will not be represented in the simulations. This error will add to the difference between the simulation and experimental results. Also, obviously, in order to get good statistical information, the number of samples should be as high as possible. The population of the four-MOSFET structure is distributed to four chips, thus, the number of samples that account for intra-die variations are relatively small. It is noteworthy that the difference between the results of different chips accounts for inter-die variations, which is not the main focus of this work. The first two chips give better offset performance than the last two, when compared to the simulation results. The average standard deviation for all four tiny chips is calculated as 5.03mV.

The statistical randomness of the simulations is provided by the Monte Carlo analysis. Apparently, the higher the number of Monte Carlo runs, the more accurate the results will be, since the number of the Monte Carlo runs correspond to the population of the samples. Still, one should not forget that although the Monte Carlo analysis is used in

the simulations to generate random data, there is no perfect random number generator, and the randomness will be to a certain extent.

Such results were found for the four-MOSFET structure with $W/L=20/4$. Figure 4.22 shows the histogram and normal distribution of the offset measurement results for this circuit. The mean and the standard deviation values are given in Table 4.27.

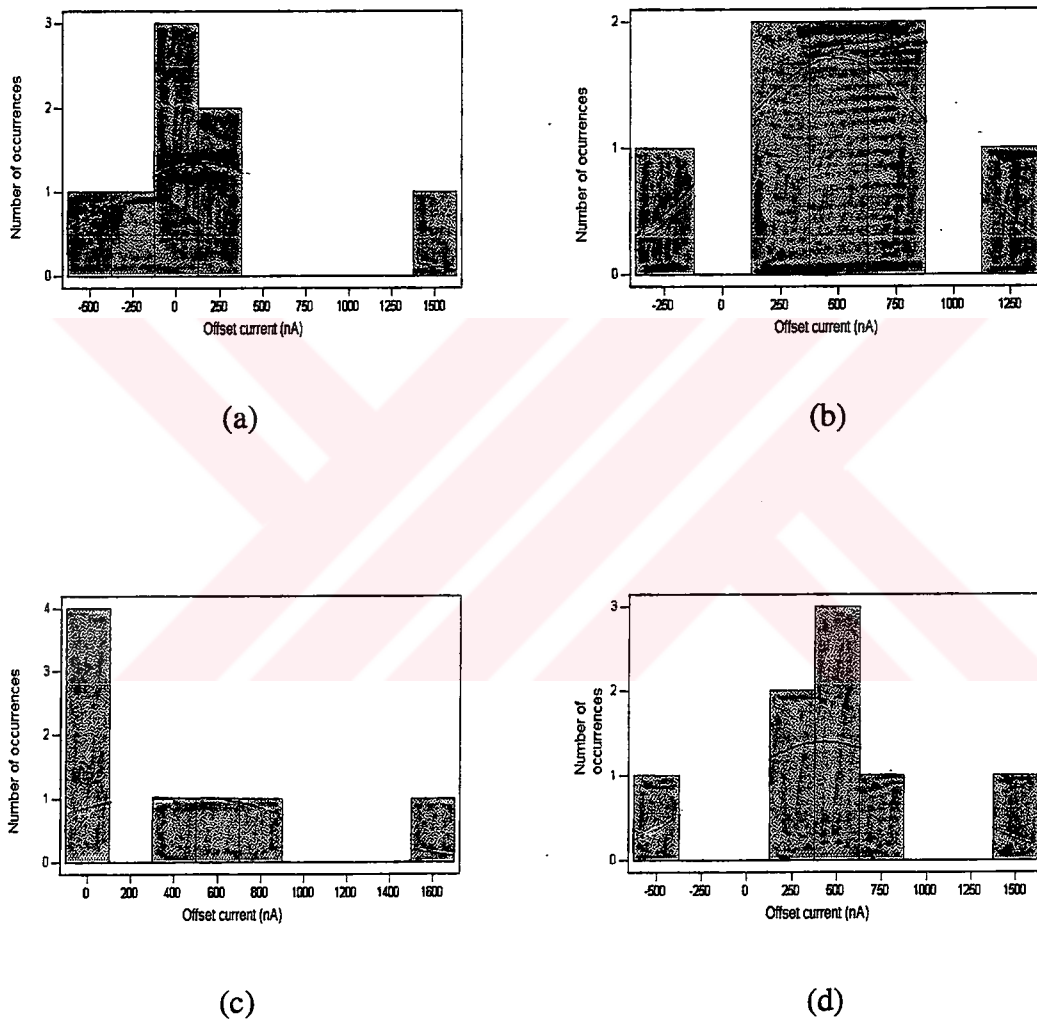


Figure 4.22: Experimental results for the offset of the four-MOSFET structure on four tiny chips ($W/L=20/4$). The histogram in each item is obtained for 8 examples.

Table 4.27: The mean and standard deviation for the offset of the four-MOSFET structure on four tiny chips ($W/L=20/4$, $G=140\mu A/V^2$)

offset ($W/L=20/4$)	Chip A	Chip B	Chip C	Chip D
mean (nA)	163.06	493	394.43	437.38
standard deviation/G (mV)	4.2336	3.329	4.2517	4.0916

The statistical simulation results for the offset of the four-MOSFET structure with $W/L=20/4$ show a standard deviation of 3.75mV. The results for all four chips give a close value to the simulation result. The average of all four standard deviation values is 3.9765mV, which is again very close to the simulation result.

The standard deviation of the offset current for $W/L=20/4$ is less than the standard deviation of $W/L=4/4$, which is expected, since as the area of the devices increase the standard deviation tends to decrease. Both simulation and experimental results agree on this.

One has got the feel for the histogram and normal distribution of the data, thus, the mean and standard deviation values for the experimental results are provided through the below tables, for the nonlinearity of the four-MOSFET structure for both aspect ratios.

Table 4.28 and Table 4.29 give the experimental results for the nonlinearity of the four-MOSFET structure, for $W/L=4/4$ and $W/L=20/4$, respectively. The results are given for four tiny chips as in the previous case.

Table 4.28: The mean and standard deviation for the nonlinearity of the four-MOSFET structure on four tiny chips ($W/L=4/4$, $G=28\mu A/V^2$)

nonlinearity ($W/L=4/4$)	Chip A	Chip B	Chip C	Chip D
mean ($\mu A/V^2$)	1.0886	1.0517	0.7164	0.9707
standard deviation/G (% V^{-1})	3.3801	3.0978	2.282	2.4589

Table 4.29: The mean and standard deviation for the nonlinearity of the four-MOSFET structure on four tiny chips ($W/L=20/4$, $G=140\mu A/V^2$)

nonlinearity ($W/L=20/4$)	Chip A	Chip B	Chip C	Chip D
mean ($\mu A/V^2$)	0.95	4.5907	1.562	4.546
standard deviation/G ($\% V^{-1}$)	0.6061	2.3317	1.3726	2.8147

The average standard deviation of the four tiny chips is 2.8047% for the circuit with $W/L=4/4$, and 1.7813% for the circuit with $W/L=20/4$.

The statistical analysis results of Figure 4.20 give a standard deviation of 2.78% for $W/L=4/4$ and 1.26% for $W/L=20/4$. The deviation in each tiny chip has a close approximation to the statistical simulation result, and the average of all four chip results is obviously very close. For $W/L=4/4$, Chip A has the largest deviation, which tells us that this chip has the worst overall nonlinearity performance among the four chips.

The difference between the results of the four tiny chips when measuring offset and nonlinearity accounts for the inter-die variations, and the variation on one chip is because of the intra-die variations.

Let us work on an example, and assume we would like a minimum device area, while achieving 3% for nonlinearity, with a functional yield of 95%, which is equivalent to a standard deviation less than 1.5%, since 95% is approximately $\pm 2\sigma$. The minimum transistor sizing that achieves these specifications is $W=20\mu m$ and $L=4\mu m$, from the statistical simulation results given in Figure 4.20. The circuit that has transistors with this sizing is fabricated, and the results were reported in Table 4.29. The average nonlinearity of all chips were calculated as 1.7813%. The possible reasons for the variations of the standard deviation on each chip were discussed previously, and will be further discussed below, however, overall results show a good agreement between the statistical simulation results and the experimental results.

One reason for the difference in the statistical simulation and experimental results, could be, as mentioned previously, the small number of circuit samples that were measured. As the number grows large, the results will be more accurate. The work in references [18], [24] and [25] strongly depend on the measurement results that were taken over years, and thus, helped building the well known statistical equations that are strongly in use at present. The offset of the measurement equipment may also contribute to the experimental results, which will cause a deviation from the simulation results.

The main goal of using the statistical techniques during the statistical simulations is to estimate the effect of random process variations on the circuit performances, without having to fabricate the circuits. The experimental results were taken to prove the validity of the statistical techniques, and to show how accurate the results are. The statistical information provides knowledge of the quantitative measure of the effect of mismatch on the circuit performances, and by having this knowledge it is possible to take the necessary steps to avoid the possible drawbacks that could occur after fabrication, e.g., low functional yield.

The die-photo of the chip that was fabricated is given in Figure 4.23.

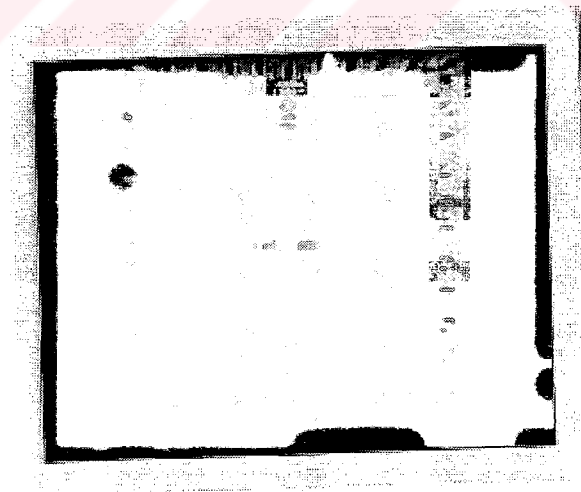


Figure 4.23: Die-photo of the chip of the four-MOSFET structure

4.6. Statistical Design of the 10-bit Current Division Network

The 10-bit current division network is shown in Figure 4.24.

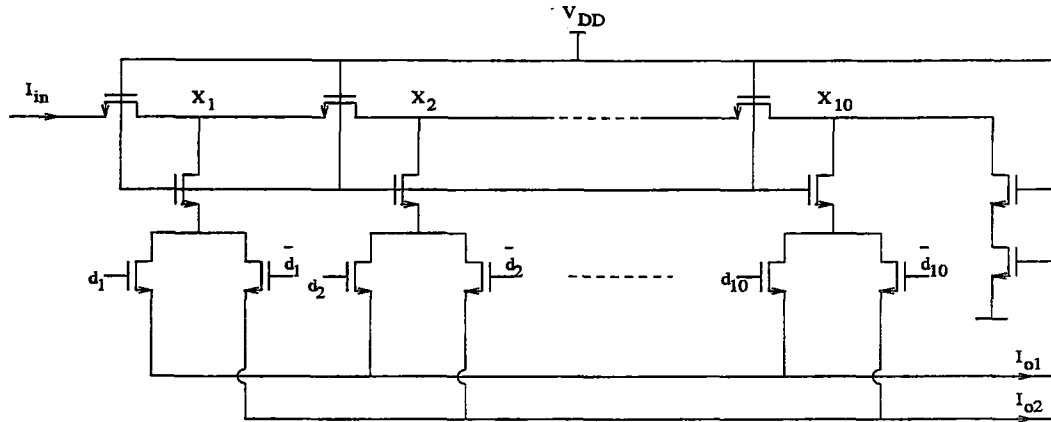


Figure 4.24: The 10-bit current division network. The description of the circuit is given in Section 3.5.

The current division network is based on the assumption of matched transistors; any mismatch will cause an error in the circuit and this will effect the resolution of the D/A converter that uses the current division network, thus, the statistical analysis of the circuit [55] has an important impact on the circuit performance.

The output current of the D/A converter can be represented in terms of LSB units, as I_o/LSB . Because of random variations, the output current will deviate from its theoretical value, thus, the goal is to calculate this deviation at the output current in LSB units.

4.6.1. Statistical Simulation Results

Statistical simulations are done to calculate the standard deviation of the output current of the 10-bit current division network, in LSB units, for different aspect ratios and for different digital word settings. The input current of the network is $I_{in}=100\mu\text{A}$. The current division network operates depending on the matching of all transistors in the circuit. All transistors in the circuit have the same size, thus, in the statistical simulations, they can be grouped as one. The SMOS model in the statistical simulations

provide the intra-die variations, and the Monte Carlo analysis provides randomness. The mean and standard deviation for different sizing of the transistors are simulated. Table 4.30 shows the statistical simulation results. Each run in the table takes 34 seconds of CPU time on a HP 715/133 workstation.

Table 4.30: The mean and standard deviation of the output current of the 10-bit current division network

d_i W/L	1000000000		0100000000		0000000001	
	mean (in LSB's)	σ (in LSB's)	mean (in LSB's)	σ (in LSB's)	mean (in LSB's)	σ (in LSB's)
20/2	0.3210	0.9420	0.3455	0.3890	0.0094	0.0103
50/2	0.3769	0.8096	0.2221	0.3369	0.0053	0.0089
8/4	0.7433	0.8914	0.6391	0.4197	0.0037	0.0140
20/4	1.0074	0.8447	0.1056	0.3578	0.0037	0.0105
44/4	0.7731	0.7908	0.3137	0.2756	0.0112	0.0065
50/4	0.5060	0.7581	0.1281	0.2353	0.0067	0.0046

The mean and the standard deviation values are both written in terms of LSB units. The difference between the ideal and actual output currents is written in terms of LSB units,

as $\frac{I_{o(ideal)} - I_{o(actual)}}{I_{in}/2^N}$, where $I_{o(ideal)}$ is the ideal output current value of the circuit,

$I_{o(actual)}$ is the simulated/measured output current value, I_{in} is the input current, and N is the number of bits; e.g., for the digital word 1000000000 and input current of $I_{in}=100\mu A$

for the 10-bit current division network, the ideal output current is $100\mu A/2^1=50\mu A$. For a $100\mu A$ input current the error in the output current in terms of LSB units is

$\frac{50\mu A - I_{o(actual)}}{100\mu A/2^{10}}$, where $I_{o(actual)}$ will be filled out by the simulation or experimental

results of the circuit. The statistical simulations of the current division network includes the random effects that will vary the output current, and calculates the variation in terms of LSB units. The mean and the standard deviations for different sizing of transistors for

three digital word settings are simulated, and were given in Table 4.30. The standard deviation values should be less than 1 LSB to achieve the required resolution for the D/A converter. Should there be a standard deviation higher than 1 LSB, the D/A converter will not be applicable for that resolution; the number of bits will be reduced and the standard deviation will be checked, until the value is less than 1 LSB.

The netlist of the statistical simulations of the 10-bit current division network is given in Appendix U, in the floppy disk attached to the thesis. The experimental results are given next.

4.6.2. Experimental Results

The 10-bit current division network was fabricated through the MOSIS $2\mu\text{m}$ process. The layouts were prepared for two different aspect ratios; $W/L=8/4$ and $W/L=44/4$. Measurements were made on 4 tiny MOSIS chips with 11 samples of circuits on each chip; 5 samples of the 10-bit current division network with the aspect ratio of $8/4$, and 6 samples for $W/L=44/4$. The number of the samples are limited because of the limited number of input and output pins of the chip. Measurement results were taken with the help of the HP4145B parameter analyzer.

The output current of each circuit on 4 chips was measured and the deviation was calculated, for both aspect ratios. The mean and standard deviations for two digital words and for the aspect ratios of $W/L=8/4$ and $W/L=44/4$ are given in Table 4.31.

Table 4.31: The standard deviation of the output current (in terms of LSB units) of the current division network for different digital words and different aspect ratios

(all results in LSB's)	Chip A	Chip B	Chip C	Chip D	Average
1000000000 - $W/L=8/4$	0.8561	0.4617	0.9184	0.6727	0.7272
1000000000 - $W/L=44/4$	0.6097	0.6924	0.6377	0.6170	0.6392
0100000000 - $W/L=8/4$	0.3802	0.3405	0.3442	0.7527	0.3590
0100000000 - $W/L=44/4$	0.1940	0.3638	0.1952	0.3205	0.2684

The results of each chip are compared with their corresponding simulation results. The difference between the results accounts for intra-die variations; e.g., the standard deviation of the output current for the digital word 1000000000 and aspect ratio of $W/L=44/4$ is 0.7908LSB. The experimental results of the four chips for the same digital word and aspect ratio is given in the second row of Table 4.31. The overall results of all the chips show a consistency and a good agreement with the simulation results. Let us consider the digital word 0100000000 and the aspect ratio of $W/L=8/4$. Chips A, B and C show consistency, whereas the standard deviation of Chip D is relatively high. The number of samples on each chip are not very high, thus, if there is one output current value that has a large deviation from the other samples, this deviation will have an important effect on the overall standard deviation of the chip, which is the case for Chip D. Apparently, the higher the number of circuit samples, the more accurate the results will be. The population was not high for the experimental results of the thesis, because of the limited number of pins for the inputs and outputs of the circuits that were examined. One other reason for the difference between the experimental results and the statistical simulation results can be because of the additional equipment offset that affects the experimental results.

The simulation and experimental results all give a higher standard deviation for transistors with small areas and a smaller standard deviation for transistors with larger areas, which is consistent with Pelgrom's equation.

Let us discuss the results that were found in the statistical simulations and the experimental results on an example: We will assume that we need a minimum device size for the digital word 0100000000 that achieves a 0.55LSB for the deviation in the output current and a yield of 95%. This is equivalent to a standard deviation of 0.275LSB, since 95% is approximately $\pm 2\sigma$. The transistor size that achieves this standard deviation is $W/L=44/4$, from Table 4.30. The 10-bit current division network with this transistor sizing was fabricated and the results were given in Table 4.31. The average standard deviation for the circuit with transistor sizing 44/4, and digital word 0100000000 is calculated as 0.2684LSB, and the deviation on each chip is reported in the table. The results are in agreement with the simulation results, thus, with the above

assumption for the output current mismatch, and yield, the experimental results agree with the simulation results.

The die-photo of the chip is given in Figure 4.25.

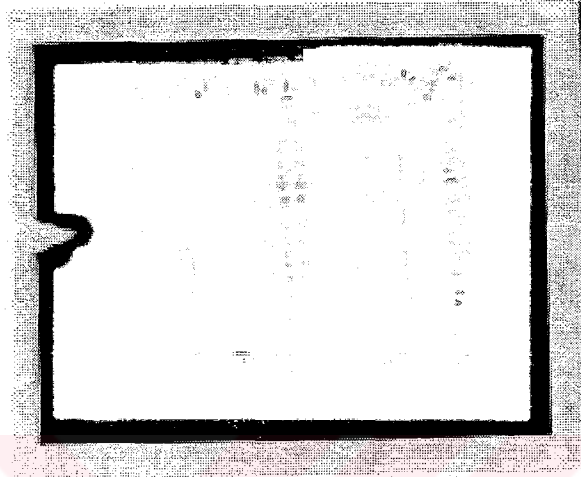


Figure 4.25: Die-photo of the chip of the 10-bit current division network

5. DISCUSSION AND RESULTS

The need for the robust design of low voltage low power CMOS analog VLSI circuits is tremendously growing. To produce cost effective, manufacturable analog and mixed-signal chips, circuit designers must work to enhance the functional yield. Statistical techniques which account for random intra-die variations and process parameter correlations must be used to achieve this goal. This is even more critical for low voltage designs, as random variations do not scale down with feature size and supply voltage. One severe effect comes from the device imperfections and variances of the fabrication process. The fabrication process is not easily characterized because these variations are random in nature. In order to produce analog integrated circuits with high functional yield and a high degree of reliability, the design of such circuits must be robust with respect to random process and device parameter variations.

The statistical design of the circuits comes into the picture at this point; the goal of the designer is to produce integrated circuits with high functional yield and low cost. This also describes the statistical design problem, which is clearly to find a set of nominal component values and their tolerances that represent the minimum cost and highest yield.

A simulation tool which provides a statistical simulation environment will ease this task, as it represents the randomness of the fabrication process. It is important to quantitatively determine the effect of mismatch on the circuit performance. A statistical model, together with statistical techniques will lead to the robust design of circuits.

The complete statistical design methodology was described in detail, in Chapter 2, and the application of this methodology on various circuits was given in Chapter 4. This chapter provides a more compact discussion on the results of the previous chapter.

Due to inherent fluctuations in any integrated circuit manufacturing process, the functional yield is always less than 100%. As the complexity of VLSI chips increase, and the dimensions of VLSI devices decrease, the sensitivity of performance to process fluctuations increases, thus further reducing the functional yield. Moreover, with current trends of higher levels of integration leading to complete mixed-signal systems on a chip, yield loss due to the analog component must be minimized such that it has little effect on the yield of the mixed-signal chip. The most critical issue in the design of analog CMOS circuits that will also affect the yield is device matching; matched devices are necessary to achieve high performance. The statistical analysis of the circuits will determine the effect of mismatch on the circuit performance, and give a quantitative measure of the performance variation.

Chapter 4 was explaining the statistical analysis of eight circuits. The SMOS model was used to include the effect of the random process variations to the simulation of the circuits. The SMOS model uses Pelgrom's equation for the standard deviation of parameter mismatches, in terms of the area of the transistors in the circuit, and the placement of the transistors in the layout. This work mainly focused on the area variation; the placement of the transistors in the layout is assumed to be the same during the statistical simulations. Statistical techniques were used to determine the most critical transistors for the circuit performance. These transistors were examined thoroughly, with the purpose of preserving a high functional yield and minimizing the variation in the circuit performance.

The statistical analysis results of two low voltage and low power composite cells, two transconductors and two multipliers that were built using these composite cells were given first. These two cells were selected to be statistically analyzed, for the reason of being widely used in research, and also in industry. The transconductors and multipliers were newly designed circuits for this thesis; they all use the composite cells as their main building block. These six circuits were also discussed for achieving the concept of

analog programmability. Analog programmability, in other words, using simple analog blocks to build more complex circuits is an ongoing discussion, and the ultimate goal in the analog CAD research area. The idea was discussed in this thesis, by building the transconductors and multipliers using the composite cells as main building blocks. Since effort is put when designing the cells with optimum transistor sizing, no effort is needed when designing the new transconductors and multipliers that will use the composite cells. The transconductor and multipliers are not the best ever circuits, but will definitely be suitable for certain specifications. The circuits may have more transistors than other transconductor or multiplier circuits, but the advantage is that there was almost no design time required, since the cells were already optimized.

The two low voltage and low power CMOS square-law composite cells were statistically examined first in Chapter 4, for the current mismatch of the circuits. Any current mismatch will cause variations in the performance of the overall circuits which use these cells as a main building block. One cell has an advantage over the other of being suitable for low power applications, and this advantage is achieved by adding a feedback loop to the circuit. The question is if the added feedback loop will degrade the robustness of the circuit, since it makes the circuit more complex and perhaps increases the matching requirements.

The standard deviation of the current mismatch showed no significant difference for the two cells. The feedback loop does not have any effect on the matching problems, hence, the improvement of the cell was achieved without causing any drawbacks. The contour curves obtained from the statistical analysis of the circuits show an average standard deviation of 2.5% for the relative drain current mismatch. An example of how to enhance the results for a certain yield was given in the related section. It is possible to improve the standard deviation by the appropriate sizing of transistors, thus, the circuit designer is able to estimate the functional yield and the variation in the circuit performance before the circuit is actually fabricated.

It is possible to use the standard deviation information to enhance the yield. A target can be set for the yield, and also to achieve the minimum sizing for transistors. Targeting a yield value is also equivalent to a target for the standard deviation of the circuit

performance, as explained on examples in Chapter 4. This will help calculate the optimized W and L values for the transistors for targeted yield (95%, 99%, etc.) and standard deviation values.

The two new transconductors were built using the composite cells, and were designed for this thesis. The transconductors can have the input voltages applied either to the NMOS or PMOS transistors. The statistical analysis for both cases did not show a big variation. NMOS transistors, are much faster than PMOS transistors, and also the output path for the transconductor with inputs on the PMOS pair is longer than the other, so the circuit will be faster when inputs are on the gates of the NMOS pair.

The circuits were statistically examined for their offset and nonlinearity performances. The average offset current and nonlinearity of the offset and nonlinearity was about $0.30\mu\text{A}$ and $0.45\mu\text{A}/\text{V}^2$, respectively, whereas, the nominal simulation results showed a “0” offset and about $0.3\mu\text{A}/\text{V}^2$ nonlinearity. The nominal simulations, however, did not take the random process variations into account, thus, the results of the statistical analysis of the circuits may have an important impact on the circuit performances. The contour curves will help keep the variations of the circuit performances small.

The composite cells were also used to build two new multipliers. The same performances as in the transconductors were considered for the multiplier circuits; offset current and nonlinearity. The offset current was read “0” from the transfer curves, whereas the statistical analysis showed a standard deviation of about $1.3\mu\text{A}$. The nominal simulations did not consider the effect of random process variations, whereas the effect may be important. The nonlinearity of the multiplier, on the other hand, was calculated from the transfer curves as $0.05\mu\text{A}/\text{V}^2$, almost nonexistent, thus the transfer curves were almost perfectly linear. However, the statistical simulations show a nonlinearity variation in the $1\mu\text{A}/\text{V}^2$ range. This value is also higher than the nonlinearity of the transconductors. The truth is that matching the transistors in the multipliers is even more important than matching the transistors in the transconductor circuits. The transconductors have two composite cells connected, whereas the

multipliers have four of them, and this makes the matching of the multiplier transistors more difficult and demanding.

The above results prove that statistical design is a crucial step in designing transconductor and multiplier circuits since they depend on device matching to achieve a linearized characteristic. The response surfaces show the trade-off between the area of the transistors and the functional yield. It is possible to find the standard deviation of the offset current and nonlinearity for different areas of the most contributing transistors, or it is possible to find the optimized W and L values of transistors for the desired standard deviation. The contour curves can be used to keep the variation of the offset current and the nonlinearity low by selecting appropriate W and L values for the most contributing input variables. It is also possible to keep the functional yield of the circuit high.

Appendix V includes a table that gives the initial and optimum sizing of transistors which are screened out to be important for the circuit performances. The appendix also includes the DC analysis results with the initial and optimum transistor sizing, for the low voltage and low power square-law CMOS cells, transconductors and multipliers. The comparison of the results show that the performance of the circuits are not seriously degraded by the optimum sizing of transistors, for the selected specifications. It is noteworthy that the comparisons are done for a certain yield (standard deviation) specification of the circuit; obviously any different sizes that are selected from the curve may give different results. The new curves are obtained from nominal simulations, thus, if the offset and nonlinearity for the transconductors and multipliers are calculated from the new curves, they will be found "0". Though, as seen in Chapter 4, statistical simulations will include the effect of random variations and will give the standard deviation of the circuit performance.

As mentioned previously, only the initial placement of the transistors in the layout have been added to the statistical simulations, since recent research proves that distance between the transistors is not very effective on the result of analog circuit simulations [24-25]. The distance information becomes important in digital circuits, e.g., when transistors use the same structure for clock signal are placed far from each other. Digital circuits, though, are not included in the context of this thesis.

Two circuits were fabricated and experimental results were given in Chapter 4, together with the statistical simulation results. The four-MOSFET structure and the 10-bit current division network are the two circuits that were fabricated.

The four-MOSFET structure can be used in filter applications. In that case it will determine the linearity of the filter. It was demonstrated that a four-MOSFET structure fully suppresses the even and odd-order nonlinearity terms; however, recent works question the widely accepted nonlinearity cancellation properties of the four-MOSFET structure. The result of the discussion is important because the supposed linearity properties of the four-MOSFET structure is served to justify its use in several recent applications. For exact cancellation of nonlinearities, exact transistor matching is needed, whereas, random variations may not always allow for exact matching of transistors. The circuit performances that are to be examined for the four-MOSFET structure are the offset and nonlinearity, as in the transconductor and multiplier circuits. Most of the previously done works on the circuit assume perfect matching of transistors; this is not the case in reality. In fact a slight mismatch can cause severe effects on the nonlinearity performance of the four-MOSFET structure.

The statistical simulation results show that the nonlinearity can vary up to 4%, however, it is possible to minimize this result to 1%, by the appropriate sizing of the transistors. The offset and nonlinearity was analyzed for different W and L values of the transistors. As the channel width of the transistors increases, it is expected to have better matching properties. However, increasing the channel width also increases the transconductance. If we are trying to achieve a certain transconductance value and to achieve this goal we need a W/L value of 2, it is possible to achieve this ratio by selecting $W/L=4/2$, $8/4$, $12/6$, etc., hence, the standard deviation of each aspect ratio should be compared and perhaps the lowest standard deviation should be selected. The curves also show that as the channel length increases, the reduction in the standard deviation of the offset is somehow saturated.

The goal of the statistical analysis of the four-MOSFET structure is to find the quantitative measure of mismatch on linearity and offset through the contour curves. It

is possible to achieve good offset and linearity performances by selecting the appropriate W and L values for the transistors in the circuit.

The last circuit that was statistically examined and fabricated is the 10-bit current division network. The circuit is used for the binary weighting of the D/A converter. A mismatch between the transistors in the circuit will effect the achievable resolution of the D/A converter. Statistical simulation results will provide information on the error caused by even slight mismatches, hence, it is important to consider statistical simulation results for obtaining optimized W and L values of transistors as well as determining the resolution of the circuit.

The four-MOSFET structure and the 10-bit current division network were also fabricated through the MOSIS 2 μ m process for two aspect ratios of the transistors: W/L=4/4 and W/L=20/4. The experimental results were taken from four chips, and the results of each chip were evaluated separately, to account for intra-die variations. The measurement data is used to calculate the standard deviation of the circuit performances, for the fabricated aspect ratios. The experimental results may show difference from the simulation results for several reasons: First of all, any error that is due to the equipment will not be represented in the simulations. Hence, this may be contributing to the difference between the statistical simulation and experimental results, is present. Experiments should be made on a high number of population to get accurate results. The number of samples for the four-MOSFET structure and the current division network are relatively small, due to the limited number of input and output pins on the chip, thus, if there is one sample that extremely deviates from the rest of the samples on the chip, the effect of the deviation will be seen in the overall results.

The statistical simulations use the Monte Carlo analysis to provide randomness. One should always keep in mind that there is no perfect random number generator; the result of each Monte Carlo run will be different because of the provided randomness, but the randomness will always be to a certain extent.

The experimental results of the two circuits were given in the related sections. The standard deviations on four chips and for the two aspect ratios were measured, and were compared with the statistical simulation results. The results are in good agreement with

the simulation results. Thus, the designer can quantitatively estimate the effect of mismatch on the circuit performances, by checking the statistical simulation results of the circuit. Examples for how to enhance the yield by the appropriate sizing of transistors were given in both sections.

One final word in this discussion is that, all computer aided methodologies or tools are user dependent. The statistical design methodology that is introduced in this thesis gives good results that agree with statistical simulation results. The goal is to reduce the standard deviation of the mismatch, however, the sizing of the transistors that correspond to the lowest standard deviation does not necessarily have to be the best values. It is very important to give flexibility to the designer throughout the application of the methodology; e.g., defining the range for the areas of transistors, the selection of the suitable areas from the contour curves (even if the areas do not correspond to the smallest standard deviation) and choosing the W and L from the selected area, are all decisions that are made by the designer to get the best performance out of the circuit.

The experimental results prove the accuracy and validity of the statistical techniques that are used in the statistical design methodology. The purpose of using these techniques is to estimate the effect of random process variations on the circuit performances, without having to fabricate the circuits. By having a knowledge of the quantitative measure of the effect of mismatch on the circuit performances, it is possible to take the necessary steps to avoid the possible drawbacks, e.g., low functional yield

The above made discussion leads to the important conclusion, that is considering statistical analysis as a standard step in circuit design. The importance is obvious for the circuits of this work, it will have an important impact on the results of other analog circuits as well. It is indeed possible to use the statistical analysis methodology that is used throughout this thesis as a standard VLSI design step, which will take into account the randomness of the fabrication process.

6. CONCLUSION AND FUTURE WORK

In low voltage low power circuits, random parameter variations present a limiting factor in the light of the fact that these variations do not scale down with feature size and/or supply voltage. After spending a long time for the best design, using the best available models and simulators, it is still possible to result in an unacceptably low functional yield, if the stochastic nature of the manufacturing process was overlooked. It is possible to produce the circuits again, but the low yield means that manufacturing costs will be too high; yield can be improved, but this will require more engineering time. For these reasons, optimizing low voltage low power analog integrated circuits for high functional yield is currently of great importance to the semiconductor industry. Especially, with current trends of higher levels of integration leading to complete mixed-signal systems on a chip, yield loss due to the analog component must be minimized such that it has little effect on the yield of the mixed-signal chip. The application of statistical circuit design techniques could largely prevent the above mentioned problems.

A common technique to make statistical simulations is the worst case method. The circuit simulations are performed at values, which are called process corners. Since each performance exhibits different sensitivity to process variations, an analysis should be carried out separately for each circuit performance. This brings obvious limitations to the method; the numerous circuit performances make this technique unsuitable for analog circuit simulation. An alternative is to use the Monte Carlo analysis for statistical simulations. Monte Carlo simulation requires a statistical model and is limited by the accuracy of this model and the CPU time required to perform the many circuit simulations. Despite its limitations, this approach is the most general method for statistical simulations.

None of the above mentioned statistical analysis methods determines the most important transistors in the circuit that affects the circuit performance, and the placement of these transistors in the layout of the circuit. Without a statistical model and statistical simulations, experienced circuit designers can estimate the effect of a particular transistor on the circuit performance. It is possible to perturb the parameter variation on each transistor in the circuit by making a large number of simulations, however, this is not a cost efficient solution.

The complete statistical design methodology presented and used in this thesis allows for specifying the most important transistors in the circuit, as well as including the initial placement of the transistors in the layout. This study mainly contributes on the optimization of transistor aspect ratios and yield estimation. The quantitative effect of the random process variations on circuit performances is determined by using the statistical design methodology.

This work presents the first serious attempt to perform statistical design and optimization of low voltage low power analog integrated circuits, at the circuit level. The main contribution of this thesis is the robust design methodology; using statistical models and techniques, to make a robust design of analog circuits. Statistical design has been successfully demonstrated on circuit examples including the low voltage squarelaw composite CMOS device architectures, transconductors and multipliers using the composite cells as a main building block, a four-MOSFET structure which is accepted to cancel full nonlinearity and a 10-bit current division network which is used for the binary weighting of D/A converters. The four-MOSFET structure and the 10-bit current division network prove the importance of statistically examining circuits to obtain the quantitative effect of mismatch between transistors, as well as the statistical design of low voltage and low power circuits.

It is possible to use the statistical design methodology, which incorporates the SMOS model and statistical techniques, for any analog circuit; the above mentioned circuits were selected since they have recently become very popular and were used in both

research and industrial applications. The transconductor and multiplier circuits, however, were designed for this thesis by using the composite cells, as an example of analog programmability, which is the ultimate goal of the analog CAD area. The goal is to come up with an analog design methodology similar to the one used for digital circuits, and take advantage of basic analog building blocks; e.g., the composite cells are the basic building blocks, and the transconductor and multipliers are the circuits that take advantage of the analog building blocks, thus, the main effort is put when building the cells, and the cells are put together to build the transconductor and multiplier circuits. This also has an impact on the design time, which, overall, is an important factor in chip design.

The robust design of the circuits is achieved, in this thesis, by using the statistical MOS (SMOS) model to include the random process variations into the simulation environment, and the statistical techniques, such as Design of Experiments (DOE) and Response Surface Methodology (RSM), to determine the most important transistors for the circuit performance, and the optimum size for these transistors. The final objective, besides keeping the functional yield high, is to give flexibility to the designer, in finding the optimum size for the transistors. The response surfaces will provide this flexibility. It is noteworthy that, statistical techniques such as DOE and RSM have been used for so long, in many other areas, but it is the first time to make use of these techniques in robust analog circuit design.

As device feature sizes of analog MOS circuits are reduced to the deep submicron ranges, the effect of process variability on circuit performance and reliability is magnified. Yield is becoming more and more critical. Statistical methods are required to simulate the effect of process variability to enable circuit designers to "design-in" quality through circuit robustness. The SMOS model that was used in this thesis has model parameters for the 2 μ m process. As recent technologies are in the submicron ranges, the statistical model parameters for the recent processes have to be extracted, in order to be used in the statistical design of the circuits. Also, the

effect of the separation distance on the layout should be considered and examined more thoroughly. These require large numbers of test structures that measurements can be done and statistical data can be taken from. This will increase the cost since the whole procedure has to be repeated for every new process, which is one main reason why many designers still use the conventional worst case, corner methods, or pure Monte Carlo simulations despite the drawbacks of using these methods.

One problem of using statistical models is that most statistical models are usually valid for a particular nominal model parameter set. Therefore, statistical analysis results that are obtained for one parameter set may not be valid if the designer has decided or was forced to use a model set which is different from the one that is used to extract the information. A flexible model, which is valid for different model parameter sets will prove useful and efficient; research still continues in this area.

With the increasing popularity of BiCMOS technology, statistical models for circuit designs using both BJT and MOS transistors becomes necessary. Only a little work has been done on mismatch characterization for BJT's, and certainly more research is needed in this field of study.

The statistical design methodology presented in this thesis can be implemented to any CAD program in a user-friendly format, and can be used with any statistical model. It is important that the statistical CAD program is easy to use, as well as it provides flexibility to the user in sizing the transistors.

More work is needed particularly in the areas of modeling and statistical CAD of submicron, low voltage mixed-signal integrated circuits. To produce cost-effective, manufacturable analog and mixed-signal chips, circuit designers must work to make robust designs and to enhance functional yield. Statistical techniques which account for random intra-die variations and process parameter correlations must be used. This is even more critical for submicron low voltage designs since random variations do not scale down with feature size or supply voltage. Moreover, with current trends of higher levels of integration leading to complete mixed-signal systems on a chip, yield

loss due to the analog part must be minimized such that it has little effect on the yield of the mixed-signal chip. It is important to determine the most important devices in the circuit which affects the circuit performances and to optimize the transistor sizes to improve the functional yield, and to determine the effect of random process variations on the circuit performances. The work presented in this thesis will help to make a robust statistical design in the circuit level.



REFERENCES

- [1] **Keonjian, E.**, 1964. *Micropower Electronics*, Pergamon, New York.
- [2] **Meindl, J.D.**, 1969. *Micropower Circuits*, Wiley, New York.
- [3] **Degrauwe, M., et al.**, 1994. "Low power/low voltage: Future needs and envisioned solutions" 1994 IEEE ISSCC Digest of Papers, pp. 98-99.
- [4] **Kohyama, S.**, 1994. "Semiconductor technology crises and challenges toward the year 2000", 1994 Symposium, VLSI Technical Digest of Papers, pp. 5-8.
- [5] **Singh, D.**, 1994. "Prospects for low power microprocessor design", Proceedings of the 1994 International Workshop on Low Power Design, Napa, CA, pp. 1.
- [6] **Molhi, S. and Chatterjee, P.**, 1994. "I-V micro-systems-scaling on schedule for personal communications", IEEE Circuits and Devices, pp. 13-17.
- [7] **Chandrakasan, A.P., Sheng, S., and Brodersen, R.**, 1992. "Low-power CMOS digital design", IEEE Journal of Solid-State Circuits Vol.27, pp. 473-484.
- [8] **Meindl, J.D.**, 1995. "Low power microelectronics: Retrospect and prospect", Proceedings of the IEEE, Vol.83, No. 4.
- [9] **Vittoz, E.A.**, 1990. "Future of Analog in the VLSI environment", Proceedings 1990 IEEE International Symposium on Circuits and Systems, pp. 1372-1375.

- [10] **Michael, C. and Ismail, M.**, 1993. Statistical Modeling for Computer-Aided Design of Analog MOS Integrated Circuits, Kluwer Academics Publishers, Boston.
- [11] **Director, S.W. and Hachtel, G.D.**, 1977. "The simplicial approximation approach to design centering", IEEE Transactions on Circuits and Systems, Vol.CAS-24, pp. 363-372.
- [12] **Bandler, J.W. and Abdel-Malek, H.L.**, 1978. "Optimal centering, tolerancing and yield determination via updated approximation and cuts", IEEE Transactions on Circuits and Systems, Vol. CAS-25, pp. 853-871.
- [13] **Elias, N.**, 1975. "New statistical methods for assigning device tolerances", Proceedings 1975 IEEE International Symposium on Circuits and Systems, pp. 329-332.
- [14] **Singhal, K. and Pinel, J.F.**, 1981. "Statistical design centering and tolerancing using parametric sampling", IEEE Transactions on Circuits and Systems, Vol.CAS-28, No. 7.
- [15] **Shyu, J.-B., Temes, G.C., and Krummenacher, F.**, 1984. "Random error effects in matched MOS capacitors and current sources", IEEE Journal of Solid State Circuits, Vol.SC-19, pp. 948-955.
- [16] **Shyu, J.-B., Temes, G.C., and Yao, K.**, 1982. "Random errors in MOS capacitors", IEEE Journal of Solid State Circuits, Vol. SC-17, pp. 1070 -1076.
- [17] **Lakshmikumar, K.R., Hadaway, R.A., and Copeland, M.A.**, 1986. "Characterization and modeling of mismatch in MOS transistors for precision analog design", IEEE Journal of Solid-State Circuits, Vol. SC-21, pp. 1057-1066.
- [18] **Pelgrom, M.J.M., Duinmaiger, A.C.J., and Welbers, A.P.G.**, 1989. "Matching properties of MOS transistors for precision analog design", IEEE Journal of Solid-State Circuits, Vol. SC-24, pp. 1433-1439.

- [19] **Michael, C.**, 1991. Statistical Modeling for Computer-Aided Design of Analog MOS Integrated Circuits, Ph.D. Dissertation, The Ohio State University, Columbus.
- [20] **To, H.Y., Hung, C.C., Su, H., and Ismail, M.**, 1996. Statistical Design and Optimization for High-Yield BiCMOS Analog Circuits, chapter 17 in Low-Power HF Microelectronics, G.A. Machado (editor), The Institution of Electrical Engineers, London.
- [21] **Abel, C., Michael, C., Ismail, M., C.S. Teng, C.S., and Lahri, R.**, 1993. "Characterization of transistor mismatch for statistical CAD of submicron CMOS analog circuits", Proceedings 1993 International Symposium on Circuits and Systems, Vol.3, pp. 1401-1404.
- [22] **Vizmuller, P.**, 1996. "A new statistical method for designing circuits and systems", RF Design Magazine, pp. 41-49.
- [23] **Abel, C., Michael, C., Ismail, M., Teng, C.S., and Lahri, R.**, 1997. "Reliability characterization of mixed-signal chips", IEEE Circuits and Devices Magazine, pp. 8-10.
- [24] **Lovett, S.J., Welten, M., Mathewson, A., and Mason, B.**, 1998. "Optimizing MOS transistor mismatch", IEEE Journal of Solid-State Circuits, Vol.33, pp. 147-150.
- [25] **Pelgrom, M.J.M., Tuinhout, H.P., and Vertreg, M.**, 1998. "Transistor Matching in Analog CMOS Applications", 1998 IEEE International Electron Devices Meeting, San Francisco, CA.
- [26] **Tsividis, Y., Banu, M., and Khoury, J.**, 1986. "Continuous-time MOSFET-C filters in VLSI", IEEE Journal of Solid-State Circuits, Vol.SC-21, No. 1, pp. 16-29.
- [27] **Song, B.S.**, 1986. "CMOS RF circuits for data communications applications", IEEE Journal of Solid-State Circuits, Vol.SC-21, pp. 310-317.
- [28] **Czarnul, Z.**, 1986. "Modification of Banu-Tsividis continuous-time integrator structure", IEEE Transactions, CAS-33, pp. 714-716.

- [29] **Flandre, D., and Jespers, P.**, 1995. "Charge-sheet modeling of MOS I-V fundamental nonlinearities in MOSFET-C continuous-time filters" *Electronics Letters*, Vol.31, No. 17, pp. 1419-1420.
- [30] **Moon, U.K. and Song, B.S.**, 1993. "Design of a low-distortion 22kHz fifth-order Bessel filter", *IEEE Journal of Solid-State Circuits*, Vol.SC-28, pp. 1254-1264.
- [31] **Smolka, G.J., Grehl, U., Jahn, B., U. Riedle, U., Veit, W., and Werker, H.**, 1991. "A low-noise trunk interface circuit", *Proceedings of the European Solid-State Circuit Research Conference (ESSCIRC)*, pp. 257260.
- [32] **Michael, C., Abel, C., and Ismail, M.**, 1994. Statistical Modeling and Simulation, chapter 14 in *Analog VLSI: Signal and Information Processing*, M. Ismail and Terri Fiez (editor), McGraw-Hill, Inc.
- [33] **APLAC-An Object Oriented Analog Circuit Simulator and Design Tools**, Circuit Theory Laboratory and Nokia Research Center, Helsinki University of Technology.
- [34] **Montgomery, D.C.**, 1997. *Design and Analysis of Experiments*, Wiley, New York.
- [35] **Box, G.E.P.**, 1987. *Empirical Model Building and Response Surfaces*, John Wiley and Sons.
- [36] **MINITAB Statistical Software**, 1997. Release 12, User's Manual, <http://www.minitab.com>
- [37] **Seevinck, E. and Wassenaar, R. F.**, 1987. "A versatile CMOS linear transconductor/square-law function circuit", *IEEE Journal of Solid-State Circuits*, Vol.SC-22, pp. 366-377.
- [38] **Motamed, A.**, 1996. *Low-Voltage Analog VLSI Circuits and Signal Processing*, Ph.D. Dissertation, The Ohio State University, Columbus.
- [39] **Hyogo, A., Hwang, C., Ismail, M., and Sekine, K.**, 1997. "LV/LP CMOS square-law composite transistors for analog VLSI applications", *IEEJ 1st International Analog VLSI Workshop*, ECT-97-59, pp. 139-143, USA.

- [40] **Wassenaar, R.F.**, 1996. *Analysis of Analog CMOS Circuits*, Oxford University Press.
- [41] **Nedungadi, A. and Viswanathan, T.R.**, 1984. "Design of linear CMOS transconductance elements", *IEEE Transactions on Circuits and Systems*, Vol.CAS-31, No. 10, pp. 891-894.
- [42] **Martinez, J.S., Steyaert, M.J., and Sansen, W.M.C.**, 1991. "A large-signal very low-distortion transconductor for high-frequency continuous-time filters", *IEEE Journal of Solid-State Circuits*, Vol.26, No. 7, pp. 946-955.
- [43] **Krummenacher, F. and Joehl, N.**, 1988. "A 4MHz CMOS continuous-time filter with on-chip automatic tuning", *IEEE Journal of Solid-State Circuits*, Vol.SC-23, pp. 750-758.
- [44] **Tarim, T.B., Kuntman, H.H., and Ismail, M.**, 1998. "Statistical design of a transconductor using a low voltage CMOS square-law composite cell", *Proceedings of the IEEE 1998 Midwest Symposium on Circuits and Systems*, pp. 100-103, Indiana.
- [45] **Tarim, T.B., Kuntman, H.H., and Ismail, M.**, 1998. "Statistical design of a transconductor using a low voltage low power CMOS square-law composite cell", *Proceedings of the International Conference on Microelectronics and Packaging*, Curitiba, Parana, Brasil.
- [46] **Babanezhad, J. and Temes, G.C.**, 1985. "A 20-V four-quadrant CMOS analog multiplier", *IEEE Journal of Solid-State Circuits*, pp. 1158-1168.
- [47] **Hyogo, A., Hwang, C., Ismail, M., and Sekine, K.**, 1997. "CMOS analog VLSI composite cell design and its application to high speed multiplier", *IEEJ 1st International Analog VLSI Workshop*, ECT-97-59, pp. 95-98, The Ohio State University, USA.
- [48] **Tarim, T.B., Kuntman, H.H., and Ismail, M.**, 1998. "Statistical design of a multiplier using a low voltage CMOS square-law composite cell", *Proceedings of the IEEE Asia-Pacific Conference on Circuits and Systems*, Chiangmai, Thailand.

- [49] **Tarim, T.B., Kuntman, H.H., and Ismail, M., 1998.** "Statistical design of a multiplier using a low voltage low power CMOS square-law composite cell", Proceedings of the XI Brazilian Symposium on Integrated Circuit Design, pp. 191-194, Buzios, Rio de Janeiro, Brasil.
- [50] **Razavi, B., 1995.** Principles of Data Conversion System Design, The Institute of Electrical and Electronics Engineers, Inc., New York.
- [51] **Johns, D.A. and Martin, K., 1997.** Analog Integrated Circuit Design, John Wiley and Sons, Inc.
- [52] **Muller, R.S. and Kamins, T.L., 1977.** Device Electronics for Integrated Circuits, Wiley, New York.
- [53] **McCreary, J.L. and Gray, P.R., 1975.** "All-MOS charge redistribution analog-to-digital conversion techniques Part I", IEEE Journal of Solid-State Circuits, Vol.SC-10, No. 6, pp. 371-379.
- [54] **Bult, K. and Gielen, G.J.G.M., 1992.** "An inherently linear and compact MOST-Only current division technique", IEEE Journal of Solid-State Circuits, Vol.27, pp.1730-1735.
- [55] **Tarim, T.B., Kuntman, H.H., and Ismail, M., 1998.** "Statistical design of a D/A converter based on the current division technique", Proceedings of the IEEE International Conference on Electronics, Circuits and Systems, Vol.2, pp. 295-298, Lizbon, Portugal.
- [56] **Tarim, T.B., Kuntman, H.H., and Ismail, M., 1998.** "Statistical design techniques for yield enhancement of low voltage CMOS VLSI", Proceedings of the IEEE International Symposium on Circuits and Systems, Vol.2, pp. 331-334, Monterey, California, USA.
- [57] **Tarim, T.B., Lin, C.H., and Ismail, M., to be published in 2000.** Robust Low Voltage Low Power Analog MOS VLSI Design, Chapter 6 in Designs of System on a Chip: Devices and Components, Ricardo Reis and Jochen Jess (editors), Kluwer Academic Publishers.
- [58] **Tarim, T.B., Kuntman, H.H., and Ismail, M., to be published in 2000.** "Statistical Design of Low Power Square-Law CMOS Cells for High Yield", International Journal of Analog Integrated Circuits and Signal Processing.

- [59] **Tarim, T.B., Kuntman, H.H., and Ismail, M.**, 1998. "Statistical design of a low voltage low power square-law CMOS cell", Proceedings of the IEEJ, 2nd International Analog VLSI Workshop, ECT-98-30, pp. 81-85, Santa Clara, California, USA.
- [60] **Tarim, T.B., Kuntman, H.H., and Ismail, M.**, 1999. "Robust Design of Basic Low Voltage CMOS Transconductors", International Journal of Analog Integrated Circuits and Signal Processing, Vol. 20, Issue 3, pp. 175-191.
- [61] **Tarim, T.B., Kuntman, H.H., and Ismail, M.**, 1998. "Statistical Design of the Four-MOSFET Structure", Proceedings of the IEEE 10th International Conference on Microelectronics, pp. 228-231, Monastir, Tunisia.



APPENDIX A:

The use of the SMOS model in the simulation environment requires a separate model file that specifies the name of the fitting constants that are used in the mean and variance models, μ_0 , μ_L , μ_W , $\sqrt{a_p}$ and s_p . The information contained in the model files must be entered in the following order for each of the 16 BSIM model parameters:

First line: Parameter name; μ_0 , μ_L and μ_W , $\sqrt{a_p}$ and s_p

Second line: A “P” followed by the PCA coefficients

The fitting constants are used to model the mean (μ_0 , μ_L and μ_W) and variance ($\sqrt{a_p}$ and s_p) of each BSIM parameter.

The principal components are used to describe the correlations between model parameters. 6 PCA coefficients account for 96.4% of the system variance, hence, a total of 12 PCA coefficients (for n- and p-channel transistors) are required to preserve 95% of the total variability.

The BSIM model files for n- and p-channel transistors in the 2 μ m n-well MOSIS process, respectively, are given below.

NMOS MODEL FILE

	μ_0	μ_L	μ_W	$\sqrt{a_p}$	s_p	
VFB	-0.953553	0.317485	-0.0980128	0.0632	73.3E-6	
P	0.6978	0.4069	-0.4593	0.0894	-0.2617	0.1873
K1	1.34076	-0.464741	0.497882	0.0714	45.3E-6	
P	-0.6734	-0.0643	0.6136	-0.3218	0.2236	-0.1287
K2	0.279434	-0.0632892	-0.0585445	0.0178	7.00E-6	
P	-0.5059	0.3363	0.6646	-0.3308	0.1605	-0.1308
ETA	-0.008943	0.0430343	-0.00350664	0.00541	4.38E-6	
P	0.8557	0.3103	0.0248	0.2247	0.1898	-0.0982
MUZ	590.303	0	0	27.91	0.0399	
P	-0.0527	0.7673	-0.0901	0.3321	0.4877	0.1258
U0	0.0546334	0.040414	-0.0741385	0.00625	5.13E-6	
P	0.4109	0.1562	0.6864	0.0032	0.0404	0.5163
U1	0.0447084	0.969499	-0.777405	0.0714	46.7E-6	
P	-0.6792	0.2479	-0.6611	-0.0143	0.0077	-0.1356
X2MZ	8.10771	-5.46405	80.3594	4.545	1.93E-3	
P	0.0778	0.9278	0.2304	-0.1235	-0.2002	-0.0772
X2E	-0.00191434	-0.00792043	-0.00257321	8.89E-4	0.67E-6	
P	-0.7571	-0.0761	0.4429	0.4327	-0.0670	-0.0086
X3E	0.000747773	-0.00374625	-0.00678198	0.00109	0.43E-6	
P	0.4250	0.7921	0.1654	-0.3487	-0.1651	-0.0411
X2U0	0.001706	-0.000341748	0.03231	0.00178	1.07E-6	
P	0.4250	0.7921	0.1654	-0.3487	-0.1651	-0.0411
X2U1	-0.0387314	0.050498	0.030572	0.0267	6.20E-6	
P	-0.6890	-0.1813	0.4523	0.4725	-0.2146	0.0141
MUS	757.607	382.616	-414.081	87.0	0.0645	
P	-0.6923	0.5493	-0.3713	0.0936	0.1824	0.1529
X2MS	-0.427729	17.9675	135.101	14.11	9.33E-4	
P	-0.4722	0.6385	0.4656	0.1935	-0.3140	-0.0585
X3MS	8.45212	62.8588	-69.4871	19.51	0.0131	
P	-0.8145	0.2912	-0.4228	-0.0065	-0.0012	0.0968
X3U1	-0.00251277	0.0744701	-0.0812578	0.0194	14.7E-6	
P	-0.7682	0.1775	-0.5631	-0.1171	-0.1079	-0.0107

PMOS MODEL FILE

	μ_0	μ_L	μ_W	$\sqrt{a_p}$	s_p	
VFB	-0.249842	-0.0141286	-0.0816092	0.0632	73.3E-6	
P	0.6978	0.4069	-0.4593	0.0894	-0.2617	0.1873
K1	0.514556	0.119801	0.326046	0.0714	45.3E-6	
P	-0.6734	-0.0643	0.6136	-0.3218	0.2236	-0.1287
K2	-0.0493665	0.135142	0.0536444	0.0178	7E-6	
P	-0.5059	0.3363	0.6646	-0.3308	0.1605	-0.1308
ETA	-0.0133368	0.0528533	-3.34849E-5	0.00541	4.38E-6	
P	0.8557	-0.3103	0.0248	0.2247	0.1898	-0.0982
MUZ	203.022	0	0	27.91	0.0399	
P	-0.0527	0.7673	-0.0901	0.3321	0.4877	0.1258
U0	0.109852	0.0456181	-0.0439367	0.00625	5.13E-6	
P	0.4109	0.1562	0.6864	0.0032	0.0404	0.5163
U1	0.00820676	0.259568	-0.100701	0.0714	46.7E-6	
P	-0.6792	0.2479	-0.6611	-0.0143	0.0077	-0.1356
X2MZ	8.25734	-3.94192	4.78739	4.545	1.93E-3	
P	0.0778	0.9278	0.2304	-0.1235	-0.2002	-0.0772
X2E	-0.00201796	-0.00165639	-0.00460235	8.89E-4	0.67E-6	
P	-0.7571	-0.0761	0.4429	0.4327	-0.067	-0.0086
X3E	-2.06119E-4	-7.61773E-4	-4.43034E-3	0.00109	0.43E-6	
P	-0.7048	-0.2639	-0.0817	-0.3399	-0.0675	0.4564
X2U0	0.00365944	-5.03044E-4	1.99878E-3	0.00178	1.07E-6	
P	0.425	0.7921	0.1654	-0.3487	-0.1651	-0.0411
X2U1	-2.07524E-3	0.00124144	0.0223727	0.0267	6.2E-6	
P	-0.689	-0.1813	0.4523	0.4725	-0.2146	0.0141
MUS	202.428	136.838	21.5007	87	0.0645	
P	-0.6923	0.5493	-0.3713	0.0936	0.1824	0.1529
X2MS	5.42690	2.57106	18.1496	14.11	9.33E-4	
P	-0.4722	0.6385	0.4656	0.1935	-0.314	-0.585
X3MS	0.733622	13.7298	1.07236	19.51	0.0131	
P	-0.8145	0.2912	-0.4228	-0.0065	-0.0012	0.0968
X3U1	-0.00179702	-0.00175852	0.00154541	0.0194	14.7E-6	
P	-0.7682	0.1775	-0.5631	-0.1171	-0.1079	-0.0107

APPENDIX C:

MOSIS 2 μ m MOSFET LEVEL-2 N-WELL PROCESS PARAMETERS

- **NMOS Parameters**

Model "nenh" FLAG=N LEVEL=2 PHI=0.700000 TOX=3.7700E-08
+ XJ=0.200000U TPG=1 VTO=0.8412
+ DELTA=3.0730E+00 LD=1.4280E-07 KP=6.4520E-05
+ UO=704.4 UEXP=1.2430E-01 UCRIT=7.8680E+03
+ RSH=1.1630E+01 GAMMA=0.5848 NSUB=8.6440E+15
+ NFS=1.1010E+11 VMAX=5.2720E+04 LAMBDA=3.4E-02
+ CGDO=1.9620E-10 CGSO=1.9620E-10 CGBO=3.4589E-10
+ CJ=1.09E-04 MJ=0.693 CJSW=5.72E-10
+ MJSW=0.234 PB=0.69

- **PMOS Parameters**

Model "penh" FLAG=P LEVEL=2 PHI=0.700000 TOX=3.7700E-08
+ XJ=0.200000U TPG=-1 VTO=-0.89
+ DELTA=2.5470E+00 LD=4.5020E-08 KP=1.6267E-05
+ UO=177.6 UEXP=3.4580E-01 UCRIT=1.3250E+05
+ RSH=9.1460E-02 GAMMA=0.5657 NSUB=8.0880E+15
+ NFS=5.9090E+11 VMAX=1.0000E+06 LAMBDA=4.2E-02
+ CGDO=6.1854E-11 CGSO=6.1854E-11 CGBO=4.9131E-10
+ CJ=3.22E-04 MJ=0.617 CJSW=4.28E-10
+ MJSW=0.179 PB=0.90

APPENDIX D:

APLAC Netlist for the Low Voltage CMOS Square-Law Composite Cell

*** Analysis of the low voltage CMOS square-law composite cell

*** Model parameters

Model MosfetLevelTwo

Model "nenh" FLAG=N LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=1 VTO=0.8412

+ DELTA=3.0730E+00 LD=1.4280E-07 KP=6.4520E-05

+ UO=704.4 UEXP=1.2430E-01 UCRIT=7.8680E+03

+ RSH=1.1630E+01 GAMMA=0.5848 NSUB=8.6440E+15

+ NFS=1.1010E+11 VMAX=5.2720E+04 LAMBDA=3.4E-02

+ CGDO=1.9620E-10 CGSO=1.9620E-10 CGBO=3.4589E-10

+ CJ=1.09E-04 MJ=0.693 CJSW=5.72E-10

+ MJSW=0.234 PB=0.69

* Weff = Wdrawn - Delta_W

* The suggested Delta_W is 2.2580E-09

Model "penh" FLAG=P LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=-1 VTO=-0.89

+ DELTA=2.5470E+00 LD=4.5020E-08 KP=1.6267E-05

+ UO=177.6 UEXP=3.4580E-01 UCRIT=1.3250E+05

+ RSH=9.1460E-02 GAMMA=0.5657 NSUB=8.0880E+15

+ NFS=5.9090E+11 VMAX=1.0000E+06 LAMBDA=4.2E-02

+ CGDO=6.1854E-11 CGSO=6.1854E-11 CGBO=4.9131E-10

+ CJ=3.22E-04 MJ=0.617 CJSW=4.28E-10

+ MJSW=0.179 PB=0.90

MOSFET M1 8 2 3 0 N MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u

MOSFET M2 10 7 3 0 N MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u

MOSFET M3 6 5 7 7 P MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u

MOSFET M4 8 8 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u

MOSFET M5 7 8 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u

```
MOSFET M6 9 8 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M7 3 1 0 0 N MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M8 1 1 0 0 N MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
```

```
Curr IB 10 1 DC=120u
Volt VDD 10 0 DC={VDD=3} I=I_VDD
```

```
Volt Vd 9 0 DC={Vd=1.5} I=I_Vd
Volt Vpd 6 0 DC=0
```

```
Volt Vs 5 0 DC=0.5
Volt Vgs 2 5 DC={Vgs=2}
```

```
Sweep "Transfer Curve"
+ DC
+ Loop 101 APLACVAR Vgs LIN 0 2.5
```

```
Display Y "TVd" Idc(I_Vd)
```

```
EndSweep
```

APPENDIX E:

APLAC Netlist for the Low Voltage Low Power CMOS Square-Law Composite Cell

*** Analysis of the low voltage low power CMOS square-law composite cell

*** Model parameters

Model MosfetLevelTwo

Model "nenh" FLAG=N LEVEL=2 PHI=0.700000 TOX=3.7700E-08
+ XJ=0.200000U TPG=1 VTO=0.8412
+ DELTA=3.0730E+00 LD=1.4280E-07 KP=6.4520E-05
+ UO=704.4 UEXP=1.2430E-01 UCRIT=7.8680E+03
+ RSH=1.1630E+01 GAMMA=0.5848 NSUB=8.6440E+15
+ NFS=1.1010E+11 VMAX=5.2720E+04 LAMBDA=3.4E-02
+ CGDO=1.9620E-10 CGSO=1.9620E-10 CGBO=3.4589E-10
+ CJ=1.09E-04 MJ=0.693 CJSW=5.72E-10
+ MJSW=0.234 PB=0.69
* Weff = Wdrawn - Delta_W

* The suggested Delta_W is 2.2580E-09

Model "penh" FLAG=P LEVEL=2 PHI=0.700000 TOX=3.7700E-08
+ XJ=0.200000U TPG=-1 VTO=-0.89
+ DELTA=2.5470E+00 LD=4.5020E-08 KP=1.6267E-05
+ UO=177.6 UEXP=3.4580E-01 UCRIT=1.3250E+05
+ RSH=9.1460E-02 GAMMA=0.5657 NSUB=8.0880E+15
+ NFS=5.9090E+11 VMAX=1.0000E+06 LAMBDA=4.2E-02
+ CGDO=6.1854E-11 CGSO=6.1854E-11 CGBO=4.9131E-10
+ CJ=3.22E-04 MJ=0.617 CJSW=4.28E-10
+ MJSW=0.179 PB=0.90

MOSFET M1 8 2 11 0 MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M2 4 7 11 0 MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M3 6 5 7 7 MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u

```

MOSFET M4 8 8 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M5 7 8 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M6 9 8 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u

MOSFET M7 10 4 12 0 MODEL=MosfetLevelTwo MODEL=nenh w=500u l=2u

MOSFET M8 11 12 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M9 12 12 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M10 13 13 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M11 4 13 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u

Curr IB 13 0 DC=120u
Volt VDD 10 0 DC={VDD=3} I=I_VDD
Volt Vs 5 0 DC={Vs=0.2}

Volt Vd 9 0 DC={Vo1=0} I=I_Vd
Volt Vpd1 6 0 DC=0

Volt Vin 2 0 DC={Vin=2}

Sweep "Transfer Curve"
+ DC
+ Loop 101 APLACVAR Vin LIN 0 3

Display Y "I_{d}" (Idc(I_Vd))

EndSweep

```

APPENDIX F:

APLAC Netlist for the Transconductor Using the Low Voltage CMOS Square-Law Composite Cell

*** Analysis of the transconductor using the low voltage CMOS square-law composite
*** cell as a main building block

*** Model parameters

Model MosfetLevelTwo

Model "nenh" FLAG=N LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=1 VTO=0.8412

+ DELTA=3.0730E+00 LD=1.4280E-07 KP=6.4520E-05

+ UO=704.4 UEXP=1.2430E-01 UCRIT=7.8680E+03

+ RSH=1.1630E+01 GAMMA=0.5848 NSUB=8.6440E+15

+ NFS=1.1010E+11 VMAX=5.2720E+04 LAMBDA=3.4E-02

+ CGDO=1.9620E-10 CGSO=1.9620E-10 CGBO=3.4589E-10

+ CJ=1.09E-04 MJ=0.693 CJSW=5.72E-10

+ MJSW=0.234 PB=0.69

* Weff = Wdrawn - Delta_W

* The suggested Delta_W is 2.2580E-09

Model "penh" FLAG=P LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=-1 VTO=-0.89

+ DELTA=2.5470E+00 LD=4.5020E-08 KP=1.6267E-05

+ UO=177.6 UEXP=3.4580E-01 UCRIT=1.3250E+05

+ RSH=9.1460E-02 GAMMA=0.5657 NSUB=8.0880E+15

+ NFS=5.9090E+11 VMAX=1.0000E+06 LAMBDA=4.2E-02

+ CGDO=6.1854E-11 CGSO=6.1854E-11 CGBO=4.9131E-10

+ CJ=3.22E-04 MJ=0.617 CJSW=4.28E-10

+ MJSW=0.179 PB=0.90

* First block

```
MOSFET M11 8 2 3 0 N MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M21 10 7 3 0 N MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M31 6 5 7 7 P MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u
MOSFET M41 8 8 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M51 7 8 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M61 9 8 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M71 3 1 0 0 N MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M81 1 1 0 0 N MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
```

* Second block

```
MOSFET M12 84 24 34 0 N MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M22 10 74 34 0 N MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M32 64 5 74 74 P MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u

MOSFET M42 84 84 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M52 74 84 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M62 94 84 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M72 34 1 0 0 N MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
```

```
Curr IB 10 1 DC=120u
Volt VDD 10 0 DC={VDD=3} I=I_VDD
Volt Vs 5 0 DC={Vs=0.6}
```

```
Volt Vo1 9 0 DC={Vo1=0} I=I_Vo1
Volt Vo2 94 0 DC={Vo2=0} I=I_Vo2
Volt Vpd1 6 0 DC=0
Volt Vpd2 64 0 DC=0
```

```
Volt Vin1 2 50 DC={Vin1=0.3}
```

```
Volt Vcm 50 0 DC=2 I=I_Vcm
```

```
VCVS E1 24 50 1 2 50 [-1] LINEAR
```

```
Sweep "Transfer curve of the low voltage transconductor"
+ DC
+ Loop 5 APLACVAR Vs LIN 0.2 0.6
+ Loop 101 APLACVAR Vin1 LIN -0.5 0.5
Display Y "I_{o}" Idc(I_Vo1)-Idc(I_Vo2)
EndSweep
```

APPENDIX G:

APLAC Netlist for the Transconductor Using the Low Voltage Low Power CMOS Square-Law Composite Cell

*** Analysis of the transconductor using the low voltage low power CMOS square-law
*** composite cell as a main building block

*** Model parameters

Model MosfetLevelTwo

Model "nenh" FLAG=N LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=1 VTO=0.8412

+ DELTA=3.0730E+00 LD=1.4280E-07 KP=6.4520E-05

+ UO=704.4 UEXP=1.2430E-01 UCRIT=7.8680E+03

+ RSH=1.1630E+01 GAMMA=0.5848 NSUB=8.6440E+15

+ NFS=1.1010E+11 VMAX=5.2720E+04 LAMBDA=3.4E-02

+ CGDO=1.9620E-10 CGSO=1.9620E-10 CGBO=3.4589E-10

+ CJ=1.09E-04 MJ=0.693 CJSW=5.72E-10

+ MJSW=0.234 PB=0.69

* Weff = Wdrawn - Delta_W

* The suggested Delta_W is 2.2580E-09

Model "penh" FLAG=P LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=-1 VTO=-0.89

+ DELTA=2.5470E+00 LD=4.5020E-08 KP=1.6267E-05

+ UO=177.6 UEXP=3.4580E-01 UCRIT=1.3250E+05

+ RSH=9.1460E-02 GAMMA=0.5657 NSUB=8.0880E+15

+ NFS=5.9090E+11 VMAX=1.0000E+06 LAMBDA=4.2E-02

+ CGDO=6.1854E-11 CGSO=6.1854E-11 CGBO=4.9131E-10

+ CJ=3.22E-04 MJ=0.617 CJSW=4.28E-10

+ MJSW=0.179 PB=0.90

* First block

```
MOSFET M11 8 2 11 0 MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M21 4 7 11 0 MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M31 6 5 7 7 MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u
MOSFET M41 8 8 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M51 7 8 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M61 9 8 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M71 10 4 12 0 MODEL=MosfetLevelTwo MODEL=nenh w=500u l=2u
MOSFET M81 11 12 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M91 12 12 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M101 13 13 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M111 4 13 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
```

* Second block

```
MOSFET M12 84 24 114 0 MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M22 44 74 114 0 MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M32 64 5 74 74 MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u
MOSFET M42 84 84 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M52 74 84 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M62 94 84 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M72 10 44 124 0 MODEL=MosfetLevelTwo MODEL=nenh w=500u l=2u
MOSFET M82 114 124 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M92 124 124 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M112 44 13 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
```

```
Curr IB 13 0 DC=120u
Volt VDD 10 0 DC={VDD=3} I=I_VDD
Volt Vs 5 0 DC={Vs=0.6}
Volt Vo1 9 0 DC={Vo1=0} I=I_Vo1
Volt Vo2 94 0 DC={Vo2=0} I=I_Vo2
Volt Vpd1 6 0 DC=0
Volt Vpd2 64 0 DC=0
Volt Vin1 2 50 DC={Vin1=0.3}
Volt Vcm 50 0 DC=2 I=I_Vcm
VCVS E1 24 50 1 2 50 [-1] LINEAR
```

```
Sweep "Transfer curve of the low voltage low power transistor"
+ DC
+ Loop 5 APLACVAR Vs LIN 0.2 0.6
+ Loop 101 APLACVAR Vin1 LIN -0.5 0.5
Display Y "I_{o}" Idc(I_Vo1)-Idc(I_Vo2)
EndSweep
```

APPENDIX H:

APLAC Netlist for the Multiplier Using the Low Voltage CMOS Square-Law Composite Cell

*** Analysis of the multiplier using the low voltage CMOS square-law composite cell
*** as a main building block

*** Model Parameters

Model MosfetLevelTwo

Model "nenh" FLAG=N LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=1 VTO=0.8412

+ DELTA=3.0730E+00 LD=1.4280E-07 KP=6.4520E-05

+ UO=704.4 UEXP=1.2430E-01 UCRIT=7.8680E+03

+ RSH=1.1630E+01 GAMMA=0.5848 NSUB=8.6440E+15

+ NFS=1.1010E+11 VMAX=5.2720E+04 LAMBDA=3.4E-02

+ CGDO=1.9620E-10 CGSO=1.9620E-10 CGBO=3.4589E-10

+ CJ=1.09E-04 MJ=0.693 CJSW=5.72E-10

+ MJSW=0.234 PB=0.69

* Weff = Wdrawn - Delta_W

* The suggested Delta_W is 2.2580E-09

Model "penh" FLAG=P LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=-1 VTO=-0.89

+ DELTA=2.5470E+00 LD=4.5020E-08 KP=1.6267E-05

+ UO=177.6 UEXP=3.4580E-01 UCRIT=1.3250E+05

+ RSH=9.1460E-02 GAMMA=0.5657 NSUB=8.0880E+15

+ NFS=5.9090E+11 VMAX=1.0000E+06 LAMBDA=4.2E-02

+ CGDO=6.1854E-11 CGSO=6.1854E-11 CGBO=4.9131E-10

+ CJ=3.22E-04 MJ=0.617 CJSW=4.28E-10

+ MJSW=0.179 PB=0.90

* First block

MOSFET M11 8 2 3 0 N MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M21 10 7 3 0 N MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M31 0 5 7 7 P MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u

MOSFET M41 8 8 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M51 7 8 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M61 9 8 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M71 3 1 0 0 N MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M81 1 1 0 0 N MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u

* Second block

MOSFET M12 84 12 34 0 N MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M22 10 74 34 0 N MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M32 0 5 74 74 P MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u

MOSFET M42 84 84 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M52 74 84 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M62 94 84 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M72 34 1 0 0 N MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u

* Third block

MOSFET M13 86 12 36 0 N MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M23 10 76 36 0 N MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M33 0 25 76 76 P MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u

MOSFET M43 86 86 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M53 76 86 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M63 96 86 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M73 36 1 0 0 N MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u

* Fourth block

MOSFET M14 88 2 38 0 N MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M24 10 78 38 0 N MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M34 0 25 78 78 P MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u

MOSFET M44 88 88 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M54 78 88 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M64 98 88 10 10 P MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M74 38 1 0 0 N MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u

Curr IB 10 1 DC=120u

Volt VDD 10 0 DC={VDD=3} I=I_VDD

Volt Vout1 9 0 DC=0 I=I_Vout1

Volt Vout2 94 0 DC=0 I=I_Vout2

Volt Vout3 96 0 DC=0 I=I_Vout3

Volt Vout4 98 0 DC=0 I=I_Vout4

Volt Vin1 2 105 DC={Vin1=0.3}

Volt Vcm1 105 0 DC=2.4 I=I_Vcm1

VCVS E1 12 105 1 2 105 [-1] LINEAR

Volt Vin2 5 50 DC={Vin2=0.3}

Volt Vcm2 50 0 DC=0.6 I=I_Vcm2

VCVS E2 25 50 1 5 50 [-1] LINEAR

Sweep "Transfer Curve"

+ DC

+ Loop 9 APLACVAR Vin1 LIN -0.4 0.4

+ Loop 101 APLACVAR Vin2 LIN -0.4 0.4

Display Y "Iout" (Idc(I_Vout1)+Idc(I_Vout3))-(Idc(I_Vout2)+Idc(I_Vout4))

EndSweep

APPENDIX I:

APLAC Netlist for the Multiplier Using the Low Voltage Low Power CMOS Square-Law Composite Cell

*** Analysis of the multiplier using the low voltage low power CMOS square-law
*** composite cell as a main building block

*** Model Parameters

Model MosfetLevelTwo

Model "nenh" FLAG=N LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=1 VTO=0.8412

+ DELTA=3.0730E+00 LD=1.4280E-07 KP=6.4520E-05

+ UO=704.4 UEXP=1.2430E-01 UCRIT=7.8680E+03

+ RSH=1.1630E+01 GAMMA=0.5848 NSUB=8.6440E+15

+ NFS=1.1010E+11 VMAX=5.2720E+04 LAMBDA=3.4E-02

+ CGDO=1.9620E-10 CGSO=1.9620E-10 CGBO=3.4589E-10

+ CJ=1.09E-04 MJ=0.693 CJSW=5.72E-10

+ MJSW=0.234 PB=0.69

* Weff = Wdrawn - Delta_W

* The suggested Delta_W is 2.2580E-09

Model "penh" FLAG=P LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=-1 VTO=-0.89

+ DELTA=2.5470E+00 LD=4.5020E-08 KP=1.6267E-05

+ UO=177.6 UEXP=3.4580E-01 UCRIT=1.3250E+05

+ RSH=9.1460E-02 GAMMA=0.5657 NSUB=8.0880E+15

+ NFS=5.9090E+11 VMAX=1.0000E+06 LAMBDA=4.2E-02

+ CGDO=6.1854E-11 CGSO=6.1854E-11 CGBO=4.9131E-10

+ CJ=3.22E-04 MJ=0.617 CJSW=4.28E-10

+ MJSW=0.179 PB=0.90

* First block

MOSFET M1 8 2 11 0 MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M2 4 7 11 0 MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M3 0 5 7 7 MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u

MOSFET M4 8 8 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M5 7 8 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M6 9 8 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u

MOSFET M7 10 4 12 0 MODEL=MosfetLevelTwo MODEL=nenh w=500u l=2u

MOSFET M8 11 12 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M9 12 12 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M10 13 13 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M11 4 13 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u

* Second block

MOSFET M41 84 24 114 0 MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M42 44 74 114 0 MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M43 0 5 74 74 MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u

MOSFET M44 84 84 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M45 74 84 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M46 94 84 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u

MOSFET M47 10 44 124 0 MODEL=MosfetLevelTwo MODEL=nenh w=500u l=2u

MOSFET M48 114 124 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M49 124 124 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M411 44 13 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u

* Third block

MOSFET M51 86 24 116 0 MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M52 46 76 116 0 MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M53 0 25 76 76 MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u

MOSFET M54 86 86 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M55 76 86 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M56 96 86 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u

MOSFET M57 10 46 126 0 MODEL=MosfetLevelTwo MODEL=nenh w=500u l=2u

```

MOSFET M58 116 126 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M59 126 126 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M511 46 13 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u

```

* Fourth block

```

MOSFET M61 88 2 118 0 MODEL=MosfetLevelTwo MODEL=nenh w=5u l=2u
MOSFET M62 48 78 118 0 MODEL=MosfetLevelTwo MODEL=nenh w=100u l=2u
MOSFET M63 0 25 78 78 MODEL=MosfetLevelTwo MODEL=penh w=15u l=2u

```

```

MOSFET M64 88 88 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M65 78 88 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u
MOSFET M66 98 88 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u

```

```

MOSFET M67 10 48 128 0 MODEL=MosfetLevelTwo MODEL=nenh w=500u l=2u

```

```

MOSFET M68 118 128 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M69 128 128 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=38u l=3u
MOSFET M611 48 13 10 10 MODEL=MosfetLevelTwo MODEL=penh w=150u l=3u

```

```

Curr IB 13 0 DC=120u

```

```

Volt VDD 10 0 DC={VDD=3} I=I_VDD

```

```

Volt Vout1 9 0 DC=0 I=I_Vout1
Volt Vout2 94 0 DC=0 I=I_Vout2
Volt Vout3 96 0 DC=0 I=I_Vout3
Volt Vout4 98 0 DC=0 I=I_Vout4

```

```

Volt Vin1 2 105 DC={Vin1=0.3}
Volt Vcm1 105 0 DC=2.4 I=I_Vcm1
VCVS E1 24 105 1 2 105 [-1] LINEAR

```

```

Volt Vin2 5 50 DC={Vin2=0.3}
Volt Vcm2 50 0 DC=0.6 I=I_Vcm2
VCVS E2 25 50 1 5 50 [-1] LINEAR

```

```

Sweep "Transfer Curve"
+ DC
+ Loop 9 APLACVAR Vin1 LIN -0.4 0.4
+ Loop 101 APLACVAR Vin2 LIN -0.4 0.4

```

```

Display Y "Iout" (Idc(I_Vout1)+Idc(I_Vout3))-(Idc(I_Vout2)+Idc(I_Vout4))

```

```

EndSweep

```

APPENDIX J:

APLAC Netlist for the four-MOSFET structure

*** Analysis of the four-MOSFET structure

*** Model Parameters

Model MosfetLevelTwo

Model "nenh" FLAG=N LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=1 VTO=0.8412

+ DELTA=3.0730E+00 LD=1.4280E-07 KP=6.4520E-05

+ UO=704.4 UEXP=1.2430E-01 UCRIT=7.8680E+03

+ RSH=1.1630E+01 GAMMA=0.5848 NSUB=8.6440E+15

+ NFS=1.1010E+11 VMAX=5.2720E+04 LAMBDA=3.4E-02

+ CGDO=1.9620E-10 CGSO=1.9620E-10 CGBO=3.4589E-10

+ CJ=1.09E-04 MJ=0.693 CJSW=5.72E-10

+ MJSW=0.234 PB=0.69

* Weff = Wdrawn - Delta_W

* The suggested Delta_W is 2.2580E-09

Model "penh" FLAG=P LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=-1 VTO=-0.89

+ DELTA=2.5470E+00 LD=4.5020E-08 KP=1.6267E-05

+ UO=177.6 UEXP=3.4580E-01 UCRIT=1.3250E+05

+ RSH=9.1460E-02 GAMMA=0.5657 NSUB=8.0880E+15

+ NFS=5.9090E+11 VMAX=1.0000E+06 LAMBDA=4.2E-02

+ CGDO=6.1854E-11 CGSO=6.1854E-11 CGBO=4.9131E-10

+ CJ=3.22E-04 MJ=0.617 CJSW=4.28E-10

+ MJSW=0.179 PB=0.90

MOSFET M1 3 10 2 0 N MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

MOSFET M2 5 100 2 0 N MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

MOSFET M3 3 100 4 0 N MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

MOSFET M4 5 10 4 0 N MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

```
Volt V1 3 0 DC={V1=0.8} I=I_V1  
Volt V2 5 0 DC={V2=0.8} I=I_V2
```

```
Volt VDD 10 0 DC={VDD=3} I=I_VDD  
Volt Vc 100 0 DC=2.75 I=I_Vc
```

```
Volt Vin1 2 50 DC={Vin1=0.3}
```

```
Volt Vcm 50 0 DC=0.8 I=I_Vcm
```

```
VCVS E1 4 50 1 2 50 [-1] LINEAR
```

```
Sweep "Transfer Curve"  
+ DC  
+ Loop 101 APLACVAR Vin1 LIN -0.5 0.5  
Display Y "Io" Idc(I_V1)-Idc(I_V2)
```

```
EndSweep
```



APPENDIX K:

APLAC Netlist for the 10-bit Current Division Network

*** Analysis of the 10-bit current division network

*** Model Parameters

Model MosfetLevelTwo

Model "nenh" FLAG=N LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=1 VTO=0.8412

+ DELTA=3.0730E+00 LD=1.4280E-07 KP=6.4520E-05

+ UO=704.4 UEXP=1.2430E-01 UCRIT=7.8680E+03

+ RSH=1.1630E+01 GAMMA=0.5848 NSUB=8.6440E+15

+ NFS=1.1010E+11 VMAX=5.2720E+04 LAMBDA=3.4E-02

+ CGDO=1.9620E-10 CGSO=1.9620E-10 CGBO=3.4589E-10

+ CJ=1.09E-04 MJ=0.693 CJSW=5.72E-10

+ MJSW=0.234 PB=0.69

* Weff = Wdrawn - Delta_W

* The suggested Delta_W is 2.2580E-09

Model "penh" FLAG=P LEVEL=2 PHI=0.700000 TOX=3.7700E-08

+ XJ=0.200000U TPG=-1 VTO=-0.89

+ DELTA=2.5470E+00 LD=4.5020E-08 KP=1.6267E-05

+ UO=177.6 UEXP=3.4580E-01 UCRIT=1.3250E+05

+ RSH=9.1460E-02 GAMMA=0.5657 NSUB=8.0880E+15

+ NFS=5.9090E+11 VMAX=1.0000E+06 LAMBDA=4.2E-02

+ CGDO=6.1854E-11 CGSO=6.1854E-11 CGBO=4.9131E-10

+ CJ=3.22E-04 MJ=0.617 CJSW=4.28E-10

+ MJSW=0.179 PB=0.90

MOSFET M2 4 100 3 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

MOSFET M3 5 100 4 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

MOSFET M4 6 100 5 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

MOSFET M5 7 100 6 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

MOSFET M6 8 100 7 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

MOSFET M7 9 100 8 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M8 10 100 9 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M9 11 100 10 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M10 12 100 11 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M21 3 100 21 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M22 4 100 22 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M23 5 100 23 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M24 6 100 24 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M25 7 100 25 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M26 8 100 26 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M27 9 100 27 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M28 10 100 28 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M29 11 100 29 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M30 12 100 30 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M41 21 41 81 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M42 21 42 82 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M43 22 43 81 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M44 22 44 82 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M45 23 45 81 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M46 23 46 82 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M47 24 47 81 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M48 24 48 82 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M49 25 49 81 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M50 25 50 82 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M51 26 51 81 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M52 26 52 82 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M53 27 53 81 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M54 27 54 82 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M55 28 55 81 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M56 28 56 82 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M57 29 57 81 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M58 29 58 82 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M59 30 59 81 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M60 30 60 82 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

MOSFET M71 12 100 71 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M72 71 100 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

MOSFET M91 42 41 100 100 MODEL=MosfetLevelTwo MODEL=penh w=8u l=4u
MOSFET M92 42 41 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M93 44 43 100 100 MODEL=MosfetLevelTwo MODEL=penh w=8u l=4u
MOSFET M94 44 43 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M95 46 45 100 100 MODEL=MosfetLevelTwo MODEL=penh w=8u l=4u
MOSFET M96 46 45 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M97 48 47 100 100 MODEL=MosfetLevelTwo MODEL=penh w=8u l=4u
MOSFET M98 48 47 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

```

MOSFET M99 50 49 100 100 MODEL=MosfetLevelTwo MODEL=penh w=8u l=4u
MOSFET M100 50 49 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M101 52 51 100 100 MODEL=MosfetLevelTwo MODEL=penh w=8u l=4u
MOSFET M102 52 51 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M103 54 53 100 100 MODEL=MosfetLevelTwo MODEL=penh w=8u l=4u
MOSFET M104 54 53 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M105 56 55 100 100 MODEL=MosfetLevelTwo MODEL=penh w=8u l=4u
MOSFET M106 56 55 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M107 58 57 100 100 MODEL=MosfetLevelTwo MODEL=penh w=8u l=4u
MOSFET M108 58 57 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u
MOSFET M109 60 59 100 100 MODEL=MosfetLevelTwo MODEL=penh w=8u l=4u
MOSFET M110 60 59 0 0 MODEL=MosfetLevelTwo MODEL=nenh w=8u l=4u

```

```

Volt VDD 100 0 DC={ VDD=3 } I=I_VDD
Volt Vo1 81 0 DC={ Vo1=0 } I=I_Vo1
Volt Vo2 82 0 DC=0 I=I_Vo2

```

```

Volt Vd0 41 0 DC=3 I=I_Vd0
Volt Vd1 43 0 DC=0 I=I_Vd1
Volt Vd2 45 0 DC=0 I=I_Vd2
Volt Vd3 47 0 DC=0 I=I_Vd3
Volt Vd4 49 0 DC=0 I=I_Vd4
Volt Vd5 51 0 DC=0 I=I_Vd5
Volt Vd6 53 0 DC=0 I=I_Vd6
Volt Vd7 55 0 DC=0 I=I_Vd7
Volt Vd8 57 0 DC=0 I=I_Vd8
Volt Vd9 59 0 DC=0 I=I_Vd9
Curr Iin 100 3 DC={ Iin=100u }

```

```

Sweep "Transfer Curve of the 10-bit Current Division Network"
+ DC
+ Loop 101 APLACVAR Iin LIN 0 100u

```

```

Display Y "Io1 (A)" Idc(I_Vo1)
+      Y "Io2 (A)" Idc(I_Vo2)
+      Y "Io1+Io2 (A)" Idc(I_Vo1)+Idc(I_Vo2)

```

```

EndSweep

```

BIOGRAPHY

Tuna B. Tarim received her B.Sc. and M.Sc. degrees in Electronics Engineering in 1992 and 1994, respectively, from Istanbul Technical University, Electrical and Electronics Engineering Faculty, Electronics and Communication Engineering Department, Istanbul, Turkey. She is currently a visiting scholar at The Ohio State University, Electrical Engineering Department. She was with Texas Instruments, Inc., from July 1998 to April 1999 as a wireless design engineer working on the statistical modeling and design of analog VLSI circuits. Her research interests include functional yield enhancement, statistical design and optimization of analog and mixed-signal VLSI circuits, and CAD of VLSI circuits.