İSTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

DESIGN CONSIDERATIONS, MODELING AND CHARACTERIZATION OF GaN HEMTs AND DESIGN OF HIGH FREQUENCY AND HIGH POWER MMIC AMPLIFIERS

M.Sc. Thesis by
Ömer CENGİZ

Department : Electronics and Communication Engineering

Programme : Electronics Engineering

JUNE 2011

İSTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

DESIGN CONSIDERATIONS, MODELING AND CHARACTERIZATION OF GaN HEMTs AND DESIGN OF HIGH FREQUENCY AND HIGH POWER MMIC AMPLIFIERS

M.Sc. Thesis by
Ömer CENGİZ
(504081218)

Date of submission : 05 May 2011
Date of defence examination: 08 June 2011

Supervisor (Chairman) : Prof. Dr. Osman PALAMUTÇUOĞULLARI (ITU)
Members of the Examining Committee : Prof. Dr. Ali TOKER (ITU)
Prof. Dr. Sıddık YARMAN (IU)

JUNE 2011

İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

GaN HEMT YAPILARININ TASARIMI, MODELLENMESİ VE ÖLÇÜMLERİ, VE YÜKSEK HIZLI VE YÜKSEK GÜÇLÜ MMIC YÜKSELTEÇLERİN TASARIMI

YÜKSEK LİSANS TEZİ
Ömer CENGİZ
(504081218)

Tezin Enstitüye Verildiği Tarih : 05 Mayıs 2011

Tezin Savunulduğu Tarih : 08 Haziran 2011

Tez Danışmanı : Prof. Dr. Osman PALAMUTÇUOĞULLARI (İTÜ)
Diğer Jüri Üyeleri : Prof. Dr. Ali TOKER (İTÜ)
Prof. Dr. Sıddık YARMAN (İÜ)

HAZİRAN 2011

FOREWORD

I would like to thank my supervisor Prof. Osman Palamutçuoğulları, for his great support, encouragement and invaluable guidance during this work.

I am also thankful to Prof. Ekmel Özbay for letting me to participate in various advanced projects under his invaluable guidance. It was an honor and extraordinary experience for me to be a part of his team.

I would also like to express my deepest gratitude to Özgür Kelekçi for his priceless comments and advices on designing, modeling and characterization issues. I learned a lot from his immense experiences.

I am thankful to Galip Orkun Arıcan, Onur Serbest, Gökhan Kurt and other Nanotam members for their generous helps and favorable discussions about this work.

June 2011

ÖMER CENGİZ

Electronics Engineer

TABLE OF CONTENTS

Page

LIST OF TABLES

Page

LIST OF FIGURES

Page

DESIGN CONSIDERATIONS, MODELING AND CHARACTERIZATION OF GaN HEMTs AND DESIGN OF HIGH FREQUENCY AND HIGH POWER MMIC AMPLIFIERS

SUMMARY

As the market for advanced telecommunication systems such as high capacity wireless data transferring, cellular, personal communication and worldwide interoperability for microwave access (WiMAX) coming closer to reality, high power and high frequency microwave transistors and amplifiers have attracted great attention. The rapid development of the radio frequency (RF) power electronics requires the introduction of wide bandgap material due to its potential in high output power density, high operation voltage and high input impedance, since there will be no significant performance improvements regarding to this problem in present semiconductor technologies. Gallium nitride (GaN) HEMT technology provides some specific material characteristics including wide bandgap, high breakdown field, high thermal conductivity, and high saturated velocity and promises better high power and high frequency performances compared to other III-V semiconductor materials. These features make GaN HEMT technology suitable for high frequency and high power monolithic microwave integrated circuit (MMIC) power amplifiers (PAs).

Firstly, high power and high frequency design considerations of GaN HEMT transistors were explained in this work. A thermally efficient power HEMT design was introduced based on these considerations. Then, micro fabrication steps and characterization methods of these HEMTs were given. Moreover, 1.1A/mm drain current density, 37.5 GHz of f_T, 48.5 GHz of f_{max} and 1.25 W/mm output power density at 10 GHz are achieved from a fabricated 8x100 μm GaN HEMT device. Next, large signal nonlinear modeling was performed for a 4x75 μm GaN HEMT transistor. By using this nonlinear model, a GaN MMIC PA was designed at 20 GHz and fabricated. According to measurement results, 603 mW output power obtained at 20.1 GHz with 9 dB small signal gain at 19.2 GHz. Finally, two S band GaN MMIC PAs were designed for WiMAX applications by using Cree GaN HEMT design kit. First PA has a 42.6 dBm output power with a 55%PAE @ 3.5 GHz and 16 dB small signal gain in the 3.2-3.8 GHz frequency range. When two of these MMICs were combined by using off-chip Lange Couplers, 45.3 dBm output power with a 45%PAE @3.5Ghz and 16 dB small signal gain were obtained with less than 0.2 dB gain ripple in the 3.3-3.8 GHz frequency range. This work was accepted by The XXX General Assembly and Scientific Symposium of the International Union of Radio Science (Union Radio Scientifique Internationale-URSI) which will be held at Istanbul, Turkey on August 13-20, 2011.

GaN HEMT YAPILARININ TASARIMI, MODELLENMESİ VE ÖLÇÜMLERİ, VE YÜKSEK HIZLI VE YÜKSEK GÜÇLÜ MMIC YÜKSELTEÇLERİN TASARIMI

ÖZET

Yüksek kapasiteli kablosuz veri iletimi, cep telefonu, kişisel iletişim ve mikrodalga erişim için dünya çapında birlikte çalışabilirlik (WiMAX) gibi gelişmiş haberleşme sistemlerinin pazarları hergeçen gün daha da geliştikçe, yüksek güçlü ve yüksek hızlı transistor ve yükselteçler üzerine ilgi de artmaktadır. Yüksek frekanslı güç elektroniği alanında meydana gelen hızlı gelişim, şu anki yarıiletken teknolojirinin performanslarında önemli bir gelişme olmayacağından yüksek çıkış gücü, yüksek çalışma gerilimi ve yüksek giriş empedancı özelliklerine sahip geniş enerji bant aralığına sahipuygu bir malzemenin tanıtılmasını gerektirmiştir. Galyum nitrat (GaN) HEMT teknolojisi diğer III-V grubu yarıiletken malzemelerle karşılaştırıldığında sahip olduğu yüksek enerji bant aralığı, yüksek ısıl iletkenlik, yüksek kırılma alanı ve yüksek doyma hızı gibi özelliklere sahiptir ve bu özellikleri sayesinde daha yüksek güç ve yüksek hız performansları vaat eder. Bu özellikleriden dolayı GaN HEMT teknolojisini yüksek güçlü ve yüksek hızlı MMIC yükselteçler için uygundur.

Bu çalışmada ilk olarak yüksek güçlü ve yüksek hızlı GaN HEMT transistorlarının tasarımlarının önemli noktaları açıklanmıştır. Bu özelliklere dayanarak termal olarak daha verimli bir güç HEMT transistoru tasarımı yapılmıştır. Daha sonra ise HEMT transistorlar için mikrofabrikasyon adımları ve karakterizasyon methodları verilmiştir. Buna göre, 8x100 μm büyüklüğündeki bir GaN HEMT transistorundan 1.1 A/mm savak akım yoğunluğu, 37.5 GHz akım kazancı kesim frekansı, 48.5 GHz güç kazancı kesim frekansı ve 10 GHz frekansında 1.25 W/mm çıkış güç yoğunluğu elde edilmiştir. Sonra 4x75 μm büyüklüğünde bir GaN transistorun büyük işaret modeli elde edilmiştir. Bu model kullanılarak 20 GHz de GaN MMIC tasarlanmış ve üretilmiştir. Bu MMIC'e ait ölçüm sonuçlarına göre ise 20 GHz de 603 mW çıkış gücü ve 19.2 GHz de 9 dB küçük işaret kazancı elde edilmiştir. Son olarak ise WiMAX uygulamaları için Cree GaN HEMT tasarım modelleri kullanılarak S bandında iki adet GaN MMIC PA tasarımı yapılmıştır. İlk PA 3.5 GHz de 42.6 dBm çıkış gücü ve %55 güç ilaveli verim (PAE) ile 3.2-3.8 GHz frekans aralığında 16 dB küçük işaret kazancına sahiptir. İkinci PA ise ilk PA nın dışardan Lange-coupler tekniği kullanılarak parallellenmesi yöntemine dayanmaktadır ve 3.5 GHz de 45.3 dBm çıkış gücü ve %45 PAE ile 3.3-3.8 GHz frekansında 0.2 dB den küçük kazanç dalgalanması ile 16 dB küçük işaret kazancı elde edilmiştir. Bu çalışma 13-20 Ağustos 2011 tarihlerinde İstanbul'da düzenlenecek olan The XXX General Assembly and Scientific Symposium of the International Union of Radio Science (Union Radio Scientifique Internationale-URSI) tarafından kabul edilmiştir.

1. INTRODUCTION

Transistor has become the fundamental building block since its invention in 1947 and is considered to be one of the greatest inventions of the twentieth century [1]. It features such as low cost, reliability and flexibility makes it an inevitable device for modern electronics. Later on, researchers and engineers have always sought for better and better, so the semiconductor technology has been improved until now. Because high performance transistors help push the development of more efficient and reliable communication systems.

On the road to seek high performance transistors, Gallium Arsenide (GaAs) high electron mobility transistor was invented in 1979 [2].

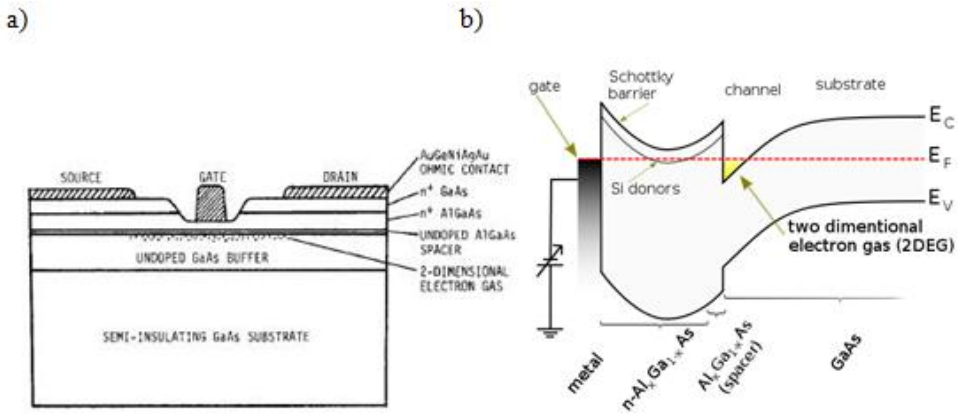

Figure 1.1: Cross section a) and band diagram b) of GaAs HEMT Structure

Figure 1.1 shows the basic epitaxial structure and band diagram of GaAs HEMT. This heterojunction structure consists of a non-doped narrowband GaAs channel layer and an n-type highly doped wideband AlGaAs donor layer. This heterojunction forms a quantum well, called two dimensional electron gas (2DEG), on the GaAs side of conduction band where the electrons move quickly and freely without any impurity collusion. Because of the 2DEG, very low channel resistivity is achieved which leads to very high mobility on the channel.

For high power and high frequency applications, GaAs HEMT technology has reached its limits. Table 1.1 shows the Johnson's figure of merit (JM) and major

parameters of the wide bandgap materials [3]. According to Table 1.1, GaN has very impressive material characteristics to build up high power and high frequency applications. First AlGaN/GaN HEMT structure was produced in 1993 [5].

Table 1.1: Material Properties Related to the Power Performance at High Frequencies for Various Materials [4].

	Si	GaAs	4H-SiC	GaN	Diamond
E_g (eV)	1.1	1.42	3.26	3.39	5.45
n_i (cm^{-3})	$1.5x10^{10}$	$1.5x10^{6}$	$8.2x10^{-9}$	$1.9x10^{-10}$	$1.6x10^{-27}$
ε_r	11.8	13.1	10	9	5.5
μ_n(cm^2/Vs)	1350	8500	700	1200 (Bulk) 2000 (2DEG)	1900
v_{sat}(10^7cm/s)	1	1	2	2.5	2.7
E_{br}(MV/cm)	0.3	0.4	3	3.3	5.6
Θ (W/cm K)	1.5	0.43	3.3-4.5	1.3	20
$JM = \frac{E_{br} v_{sat}}{2\pi}$	1	2.7	20	27.5	50

Major application areas of GaN technology can be seen in Figure 1.2.

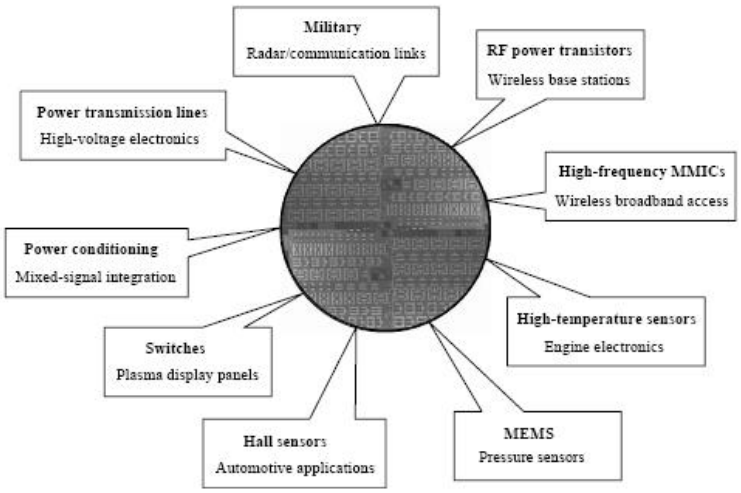

Figure 1.2: GaN-based micro-electronics applications.

We focused GaN based high power and high frequency characteristics of transistors in this work. Steps of achieving extensive MMIC power amplifiers are given from the transistor design stage to MMIC design phase. Firstly, transistor layout was determined and fabrication of transistors performed. Fabrication samples were

characterized and non-linear models of these samples are carried out by using TOPAS software of IMST GmbH [6]. After obtaining the large signal nonlinear model of our GaN HEMTs, two coplanar (CPW) MMIC power amplifiers are designed at 20 GHz and 5 GHz respectively. On the design process, passive structures such as transmission lines, capacitors and inductors are modeled to become compatible with Advanced Design System software of Agilent [7] by using COPLAN software of IMST GmbH. Finally, two 3.5 GHz GaN MMIC PAs were designed by using the GaN MMIC design kit of Cree [41].

Part 2 gives the design considerations, fabrication steps and characterization of high frequency and high power GaN HEMTs. First, layout design issue of GaN HEMTs for high power and high frequency applications are covered. Fabrication steps of HEMT and MMIC processes are given in next. Next, characterization methods of GaN HEMTs are given. This chapter concludes with characterization results of fabricated GaN HEMTs.

Part 3 contains the details of small-signal and large signal modeling of HEMT devices. First, large signal modeling techniques are mentioned. Next, modeling of GaN HEMTs using TOPAS software is explained in detail from the measurement phase to generating model stage. Finally, accuracy of the nonlinear models is compared with measurements.

Part 4 gives the steps of designing two GaN MMIC amplifiers by using our own models and COPLAN software. Design steps, simulation results and characterization of 20 GHz and 5 GHz GaN MMIC PA is given and commented respectively.

Part 5 contains the design steps of two S band high power GaN MMIC PAs for WiMAX applications. First, information about the Cree GaN design kit is given. Next, wideband matching circuit is explained and S band GaN MMIC PA is designed with lumped passive elements and simulation results are given. Its equivalent circuit with real passive elements and transmission lines is built. Next, a Lange coupler is designed with Teflon PCB parameters and it is used to combine the two of these designed GaN MMIC PAs. Finally, its simulation results are given and future works are discussed. This work was accepted by The XXX General Assembly and Scientific Symposium of the International Union of Radio Science (Union Radio

Scientifique Internationale-URSI) which will be held at Istanbul, Turkey on August 13-20, 2011.

Part 6 summarizes works done and results obtained in the work.

2. DESIGN, FABRICATION AND CHARACTERIZATION OF GaN HEMT DEVICES

This part contains the design considerations of GaN HEMTs, a brief explanation of fabrication steps and characterization of these fabricated transistors. First, important aspects of designing high frequency and high power HEMTs are mentioned. Next, fabrication steps are given. Finally characterization results are presented.

2.1 HEMT Design Considerations

While designing a HEMT device, there are some important device design parameters having very high influence on device performance and should be considered carefully based on the application purpose. These design parameters are gate length (L_g), unit gate width (W_{gu}), total gate width (W_g) drain-source spacing (L_{ds}), gate-source spacing (L_{gs}) and gate-drain spacing (L_{gd}). The current gain cut-off frequency of a HEMT device is given in **(2.1)** as a function of gate length:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \approx \frac{v_{sat}}{2\pi L_g} \qquad \textbf{(2.1)}$$

where g_m is transconductance, C_{gs} and C_{gd} are gate-source and gate-drain capacitances respectively, v_{sat} is saturation velocity of electrons in the channel. As seen from (2.1) cut-off frequency is inverse proportional with L_g. Therefore, L_g needs to be decreased for higher frequency operation of a HEMT device. Besides, decreasing Lg is also increases the drain current of the device which is a must for high power applications. Total gate width is also directly proportional with drain current and should also be increased for high power applications. On the other hand unit gate width should be as small as possible for high frequency applications. This problem is solved using several gate fingers in parallel depends on the application; however, number of fingers also have a upper limit related to same reason with unit gate width [8]. To increase the maximum number of gate fingers, the distance between each gate finger (L_{gg}) needs to be as small as possible, but this increases the

channel temperature interferences and decreases the device performance. Figure 2.1 shows a temperature variance of a HEMT device between its terminals [9].

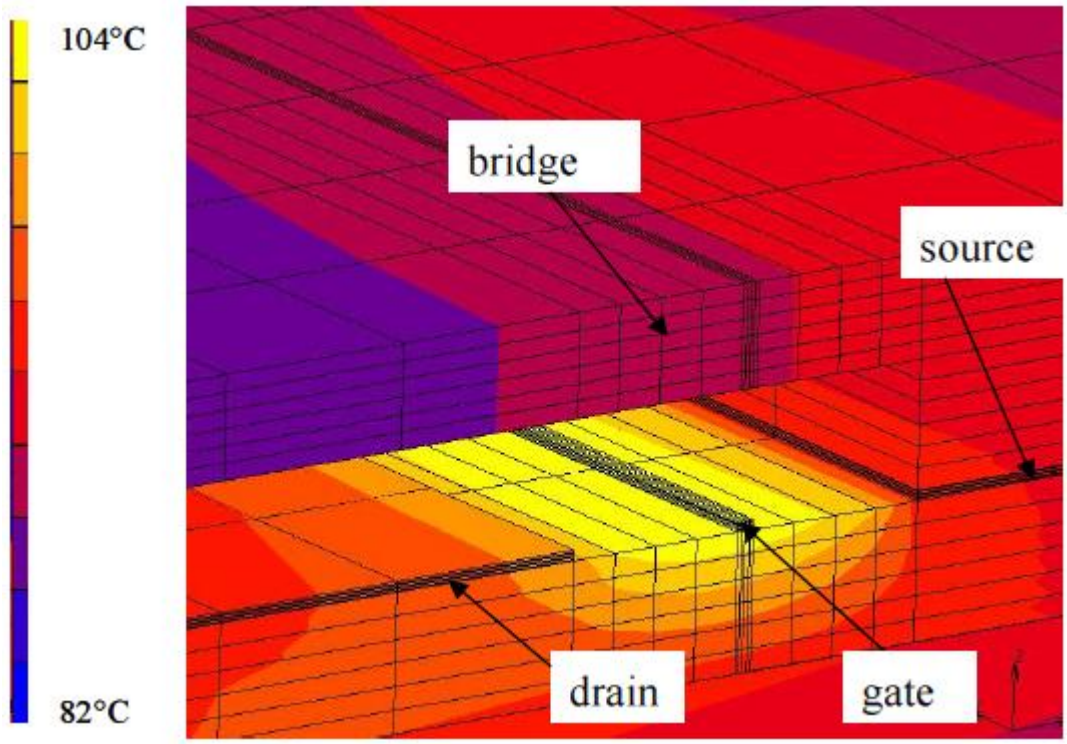

Figure 2.1: Detailed view of the temperature distribution (base temperature is 25 ^{o}C) [9].

As the number of fingers increases, the temperature at center fingers are much more with respect to side fingers as shown in Figure 2.2 [10].

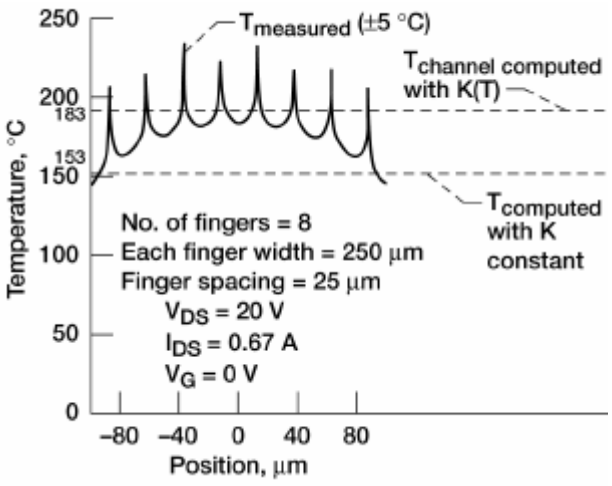

Figure 2.2: Temperature distribution for each finger of an 8 finger HEMT device [10].

For especially high power applications, L_{gg} should be determined carefully not to suffer from temperature dependent degradations. Drain source spacing has an effect on drain current, breakdown voltage and cut-off frequency [11]. Moreover, the position of the gate between drain-source terminals is also important. As drain-gate distance increases, breakdown voltage of the device and average electron speed increases but Ids and gm decreases [12].

Several coplanar wave guide (CPW) HEMT layouts are designed including small periphery and large periphery devices. By considering these important aspects explained above, the drain source spacing selected as 3 µm (ds3 µm) based on experiments in this work. Lg is around 0.25 µm defined by E-beam lithography system at Bilkent NANOTAM, Lgd and Lgs are 1.6 µm and 1.4 µm respectively based on experiments as well. Figure 2.3 shows the latest designed GaN HEMT photomask layout. The mask also has several test patterns such as transmission line model (TLM) patterns for determining the ohmic contact resistances and passive components like capacitors and resistors.

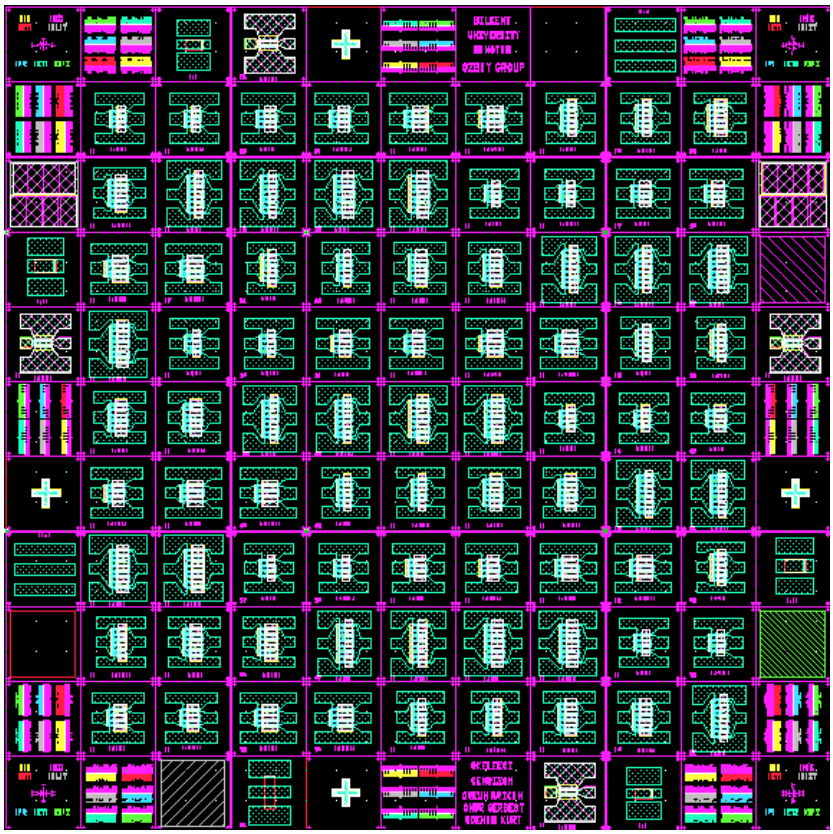

Figure 2.3: HEMT photo-mask.

For high power applications, gate to gate distance should be far away from each other as much as possible. However, this will decrease the gain of the transistor. Another design approach is used for solving this issue, which is increasing the distance between the gate-source-gate terminals. Figure 2.4 shows an example of this design approach for a 6x100 ds3 μm.

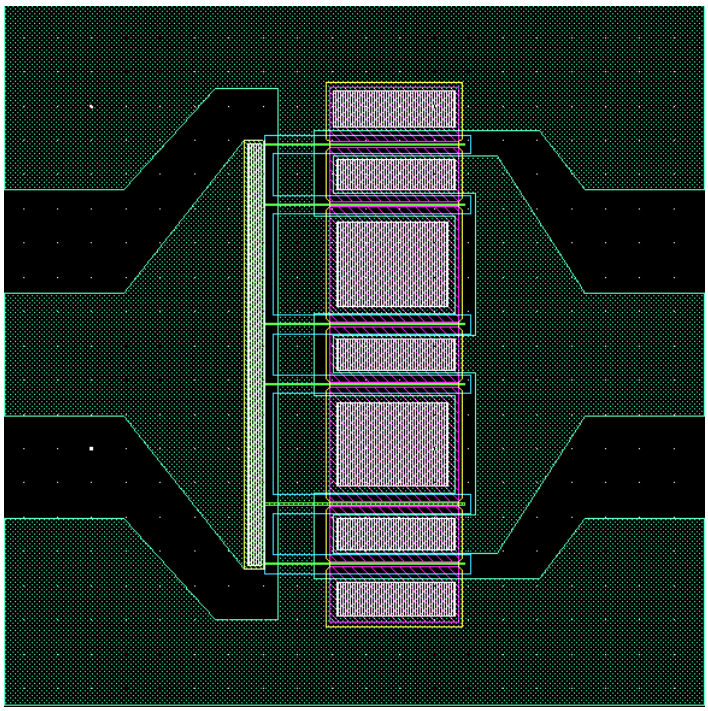

Figure 2.4: Layout of a 6x100 μm HEMT transistor for high power applications.

Based on this design approach, more thermal efficient high power HEMT transistors are designed. Figure 2.5 shows a 16x200 μm ds4 μm power HEMT transistor layout. Its gate fingers are split into two parts to reduce the gate resistance leading to an increase in power gain cut-off frequency, f_{max} [8]. Its characterization results will be given later in this part.

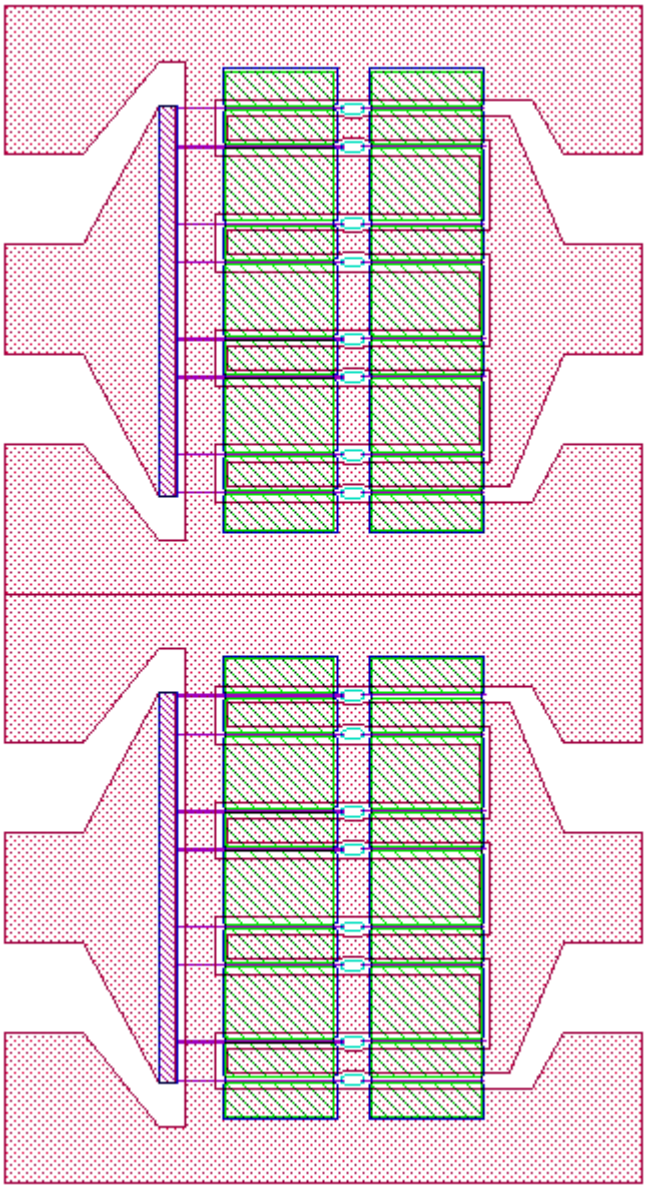

Figure 2.5: Layout of a 16x200 μm HEMT transistor for high power applications.

2.2 Fabrication Steps

Now, fabrication steps of HEMT and MMIC processes will be explained briefly. Sample cleaning is common and very important for all fabrication steps which effects fabrication yield and device quality directly. Before every major step, sample cleaning is performed by using acetone (CH_3COCH_3), isopropyl alcohol ($CH_3CHOHCH_3$). Then, samples are dried using pressured nitrogen (N_2) gas.

First step of the fabrication is mesa etching to isolate the each active device from each other electrically. Reactive ion etching (RIE) technique is used for etching the openings on the device defined by the photolithography. Figure 2.6 shows

schematics for a HEMT device before the mesa etching and after the mesa etching. A photo of a sample after mesa etching is shown in Figure 2.7.

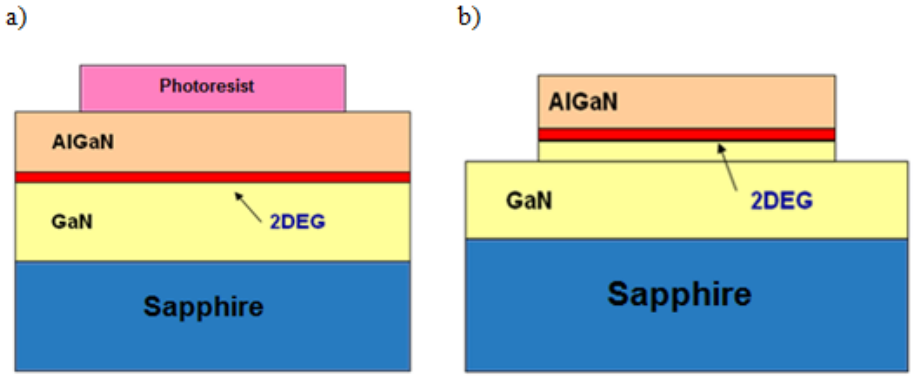

Figure 2.6: Schematic illustration of a HEMT device a) before mesa etching b) after mesa etching.

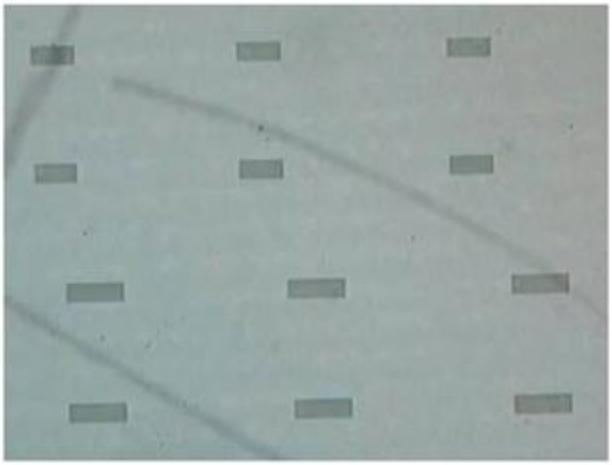

Figure 2.7: A photo of a HEMT sample after mesa etching.

Next step is forming the ohmic contacts to create an electrical connection to the channel from the upper surface. First ohmic contact areas defined by using photolithography technique. Then, e-beam evaporator is used for metallization of the ohmic contacts. Ti-Al-Ni-Au metals used to form the ohmic contacts and finally rapid thermal processing (RTP) is used to anneal the ohmic contacts at 850 ^{o}C. Figure 2.8 shows the schematic illustration and a photo of formed ohmic contacts.

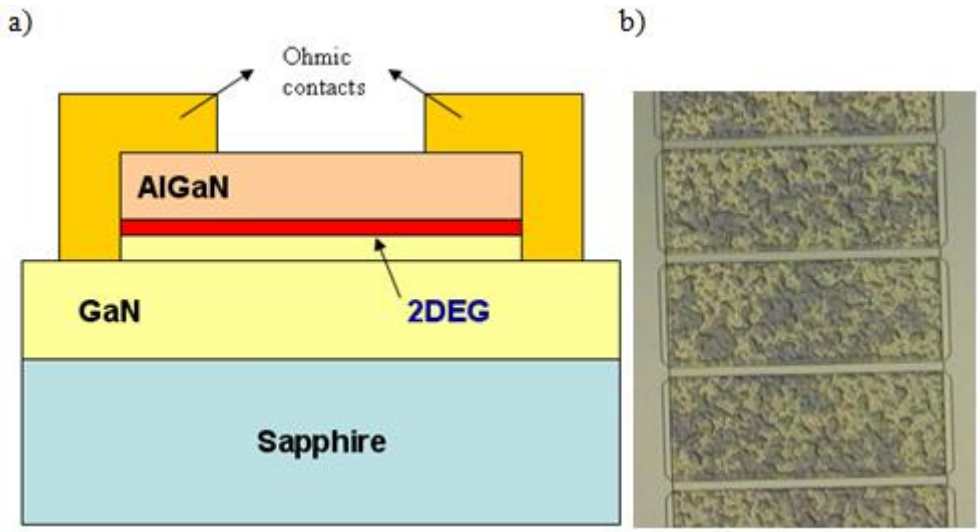

Figure 2.8: a) Schematic illustration b) a photo of formed ohmic contacts.

Next step is forming the gate contacts in HEMTs. Gate contacts are schottky contacts in basic. E-beam lithography workstation is used in order to fabricate sub-micron gates. Ni-Au metals are deposited by using e-beam evaporator as gate metals. A schematic illustration and a photo of gate contacts can be seen in Figure 2.9.

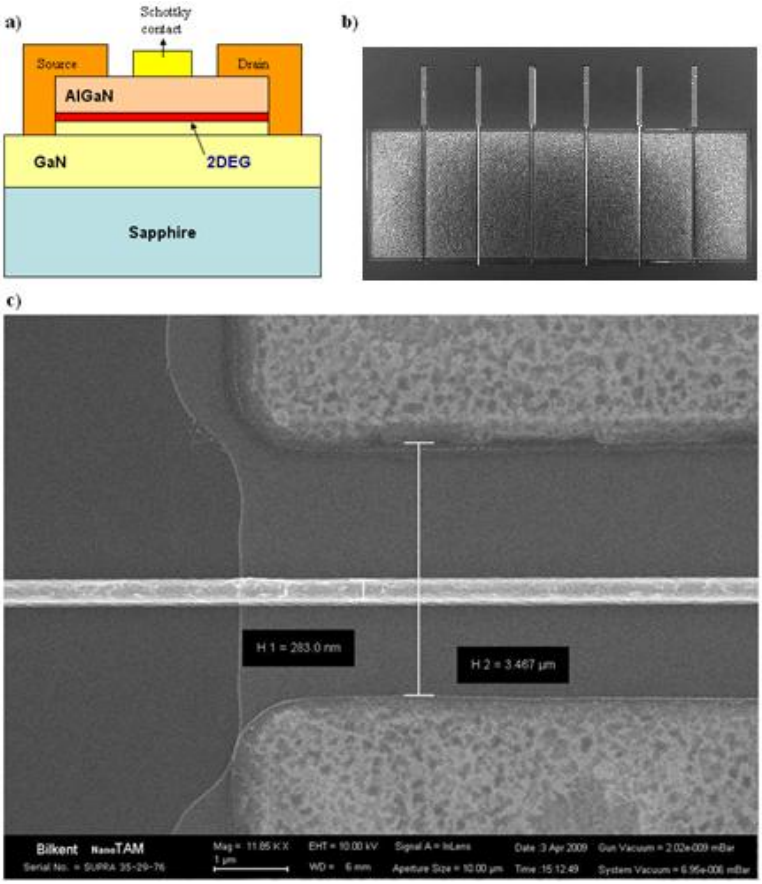

Figure 2.9: a) Schematic illustration b-c) photos of formed gate contacts.

After gate contacts formed, a metallization process is performed in order to create the contact metals such as first metals of capacitors, inductors, underpass contacts and gate pads. Ti-Au metals are used in this process. Figure 2.10 shows the schematic illustration and a photo of first metal.

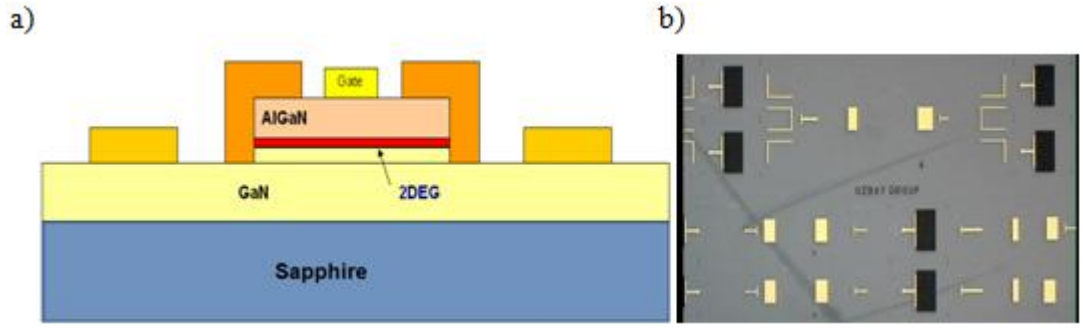

Figure 2.10: a) Schematic illustration b) photos of first metallization step.

Surface passivation comes next as the fabrication step. Several works has been published to understand the connection between the device performance and surface passivation [13-16]. Some has agreed that proper surface passivation prevents the electron trapping which leads to surface neutralization and a positive surface charge is maintained [17-19]. As a result, better device performances achieved. Silicon nitride (SiN) is used as passivation material in this work. SiN is deposited on the samples by using plasma enhanced chemical vapor deposition (PECVD) system. Figure 2.11 shows a sample photo before and after the passivation step.

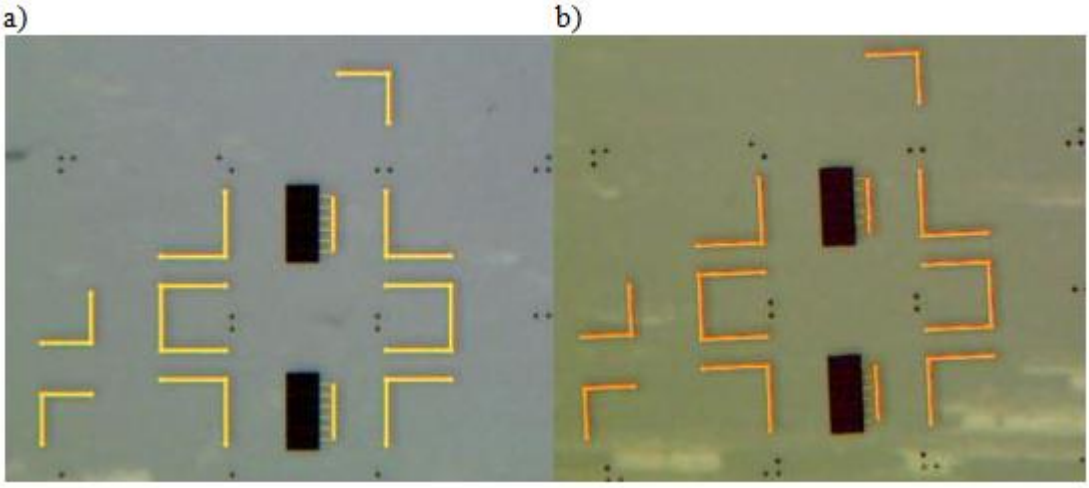

Figure 2.11: A photo of the sample a) before passivation b) after passivation.

SiN openings to form a connection between first metal and second metal come next. First opening areas defined by photolithography technique then, RIE system is used to form these openings. Figure 2.12 shows a photo of an opening on a sample.

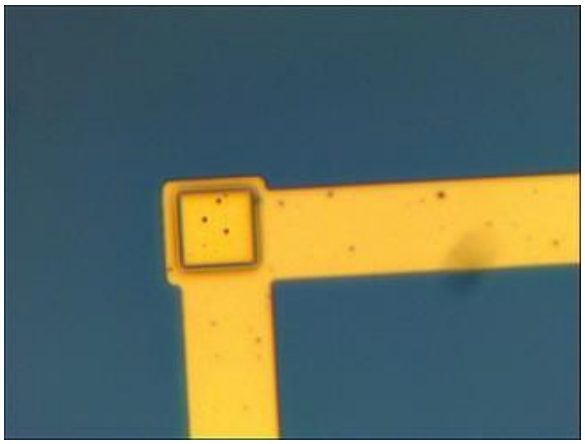

Figure 2.12: A photo of the opening on a sample.

Next, air bridges are formed. This step starts with air-bridge post material lithography and then resist is reflowed to form mechanically stable air-bridges. Figure 2.13 shows a photo of formed air bridges on a HEMT sample.

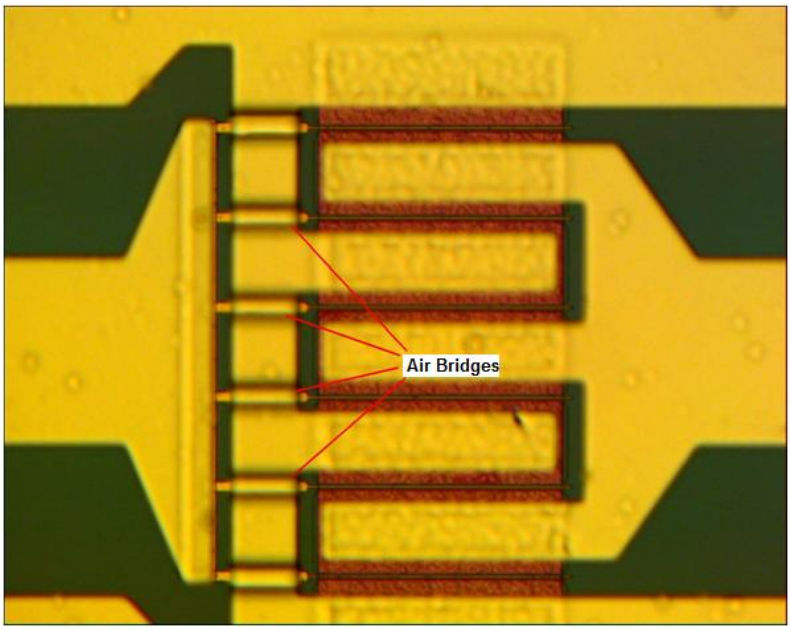

Figure 2.13: A photo of the air bridges on a HEMT sample.

A seed layer consists of Ti-Au metals is formed in order to generate a conductive sample surface for electroplating step by using e-beam evaporator system. After this electroplating process is performed to create the interconnect metals which has approximately 2.5 µm thickness. Last step of the fabrication is removing the seed

layer and air bridge post. Firstly, a Ti protection layer is deposited on top of the interconnect metallization and then seed layer is removed by using wet etch technique. Figure 2.14 and Figure 2.15 show completed HEMT device and air bridges respectively.

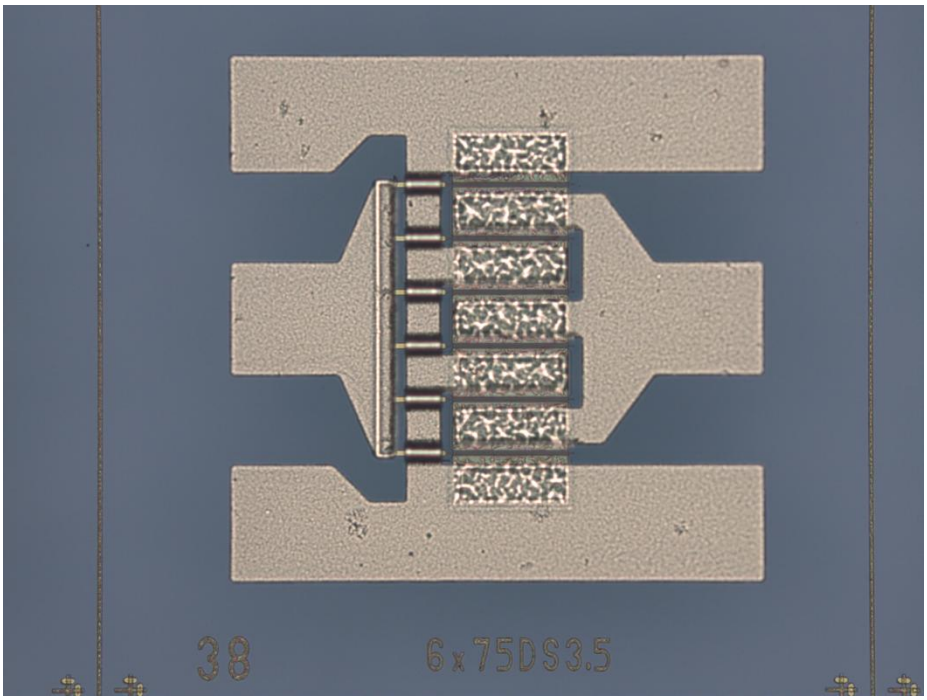

Figure 2.14: A photo of the fabricated HEMT sample.

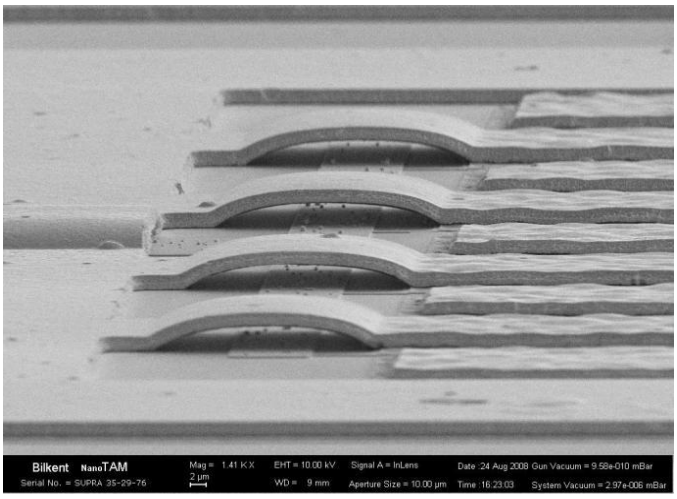

Figure 2.15: A photo of the air bridges on a HEMT sample after fabrication completed.

2.3 Characterization of HEMT Devices

There are three main characterization techniques used for fabricated GaN HEMT devices. First one is DC characterization, second one is AC characterization and third one is large-signal characterization.

For DC characterization; Pinch-off voltage, Knee voltage, maximum drain current, breakdown voltage, and DC transconductance are important device parameters. We use an Agilent B1505A Power Device Analyzer / Curve Tracer and a Cascade M150 probe station for performing DC characterization. A photo of the DC measurement setup is shown in Figure 2.16.

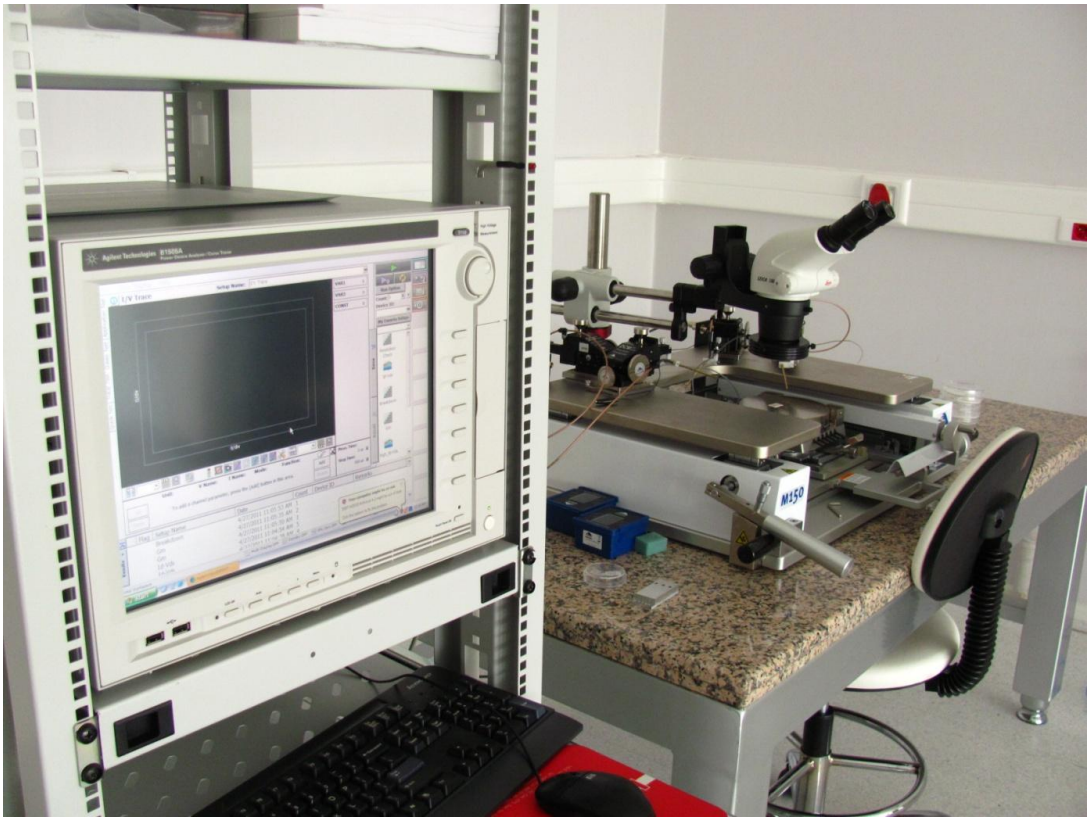

Figure 2.16: A photo of our DC characterization setup

This system has a user friendly interface which gate and drain voltage ranges and number of measurement points are entered. During drain voltage sweep between predefined values for each gate voltage applied, the system records the drain current of the device. A typical HEMT DC-IV graph measured at the system shown in Figure 2.16 is shown in Figure 2.17. Marked point A which is the intersection of linear and saturated regions shows the maximum drain current and knee voltage.

Marked point B shows the gate pinch-off voltage point. Drain current is almost zero at point B.

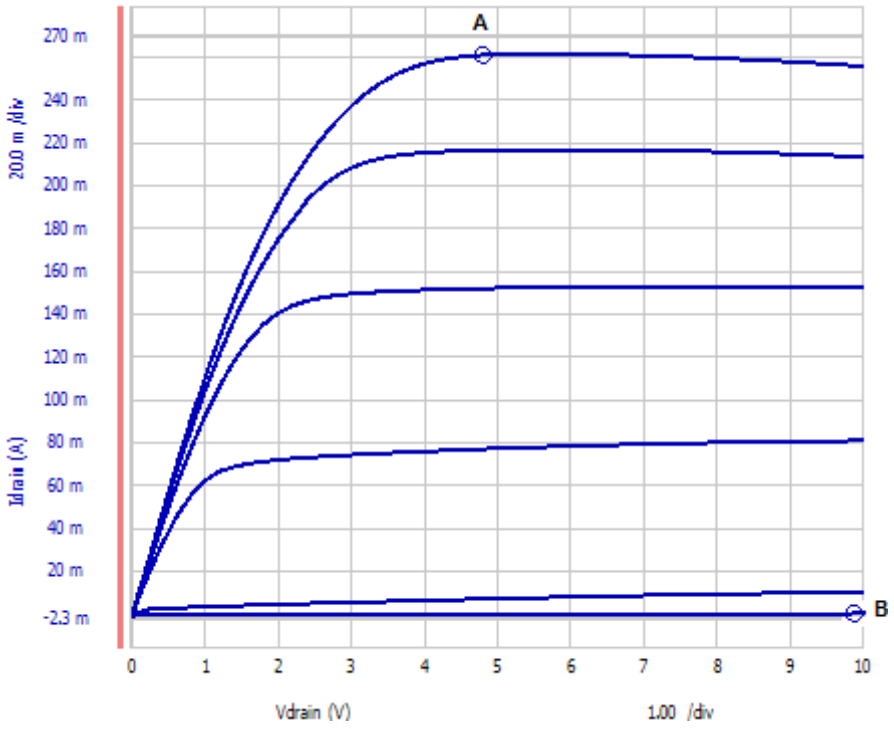

Figure 2.17: A typical DC-IV graph of GaN HEMT device.

For breakdown voltage characterization, gate voltage is kept less than the pinch-off voltage while the drain voltage is increased until 10mA/mm drain current density is measured. DC transconductance is defined as follows:

$$g_{m,\mathrm{DC}} = \frac{\Delta I_{\mathrm{DS}}}{\Delta V_{\mathrm{DS}}}\bigg|_{V_{\mathrm{DC}}=cons.} . \qquad \textbf{(2.2)}$$

Drain voltage is fixed at a voltage such as knee voltage and gate voltage is swept and the drain current is recorded.

DC characterization of a 8x100 µm and 6x75 µm HEMT devices are given in Figure 2.18 and 2.19. For 8x100 µm device, 1.1 A/mm drain current density, higher than 40V breakdown voltage, 6.2 V knee voltage, -5V pinch-off voltage and 226 mS/mm transconductance is achieved. 900mA/mm drain current density, 6.5V knee voltage, -5V pinch-off voltage, higher than 50V breakdown voltage and 223mS/mm transconductance are obtained for 6x75 µm device.

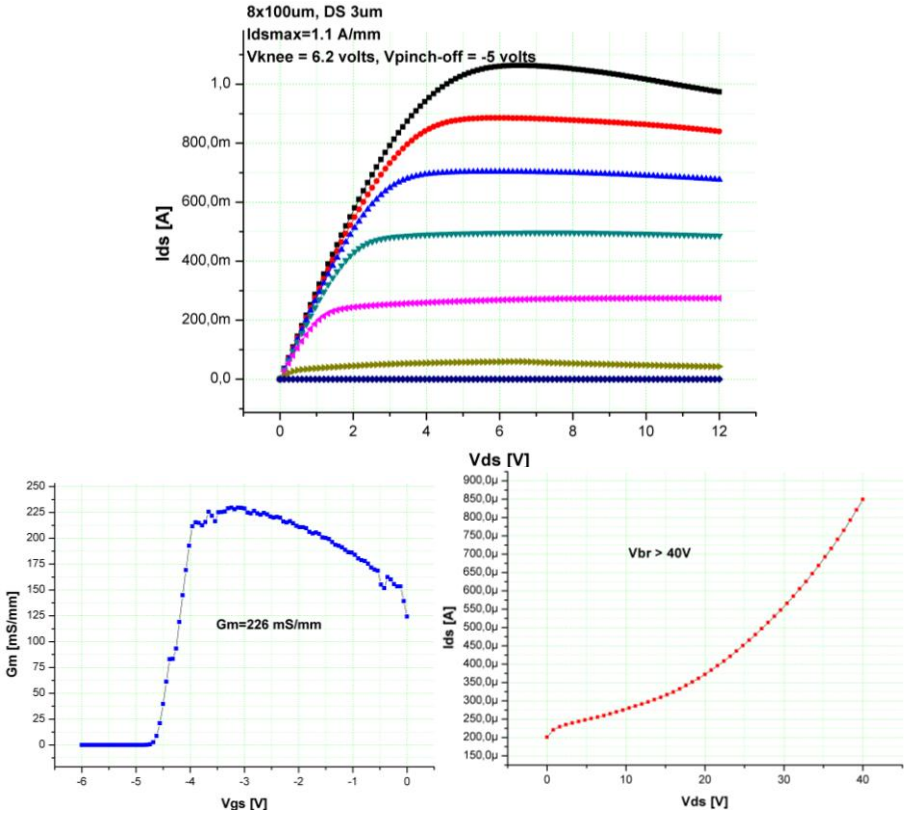

Figure 2.18: DC characterization results of an 8x100µm GaN HEMT device.

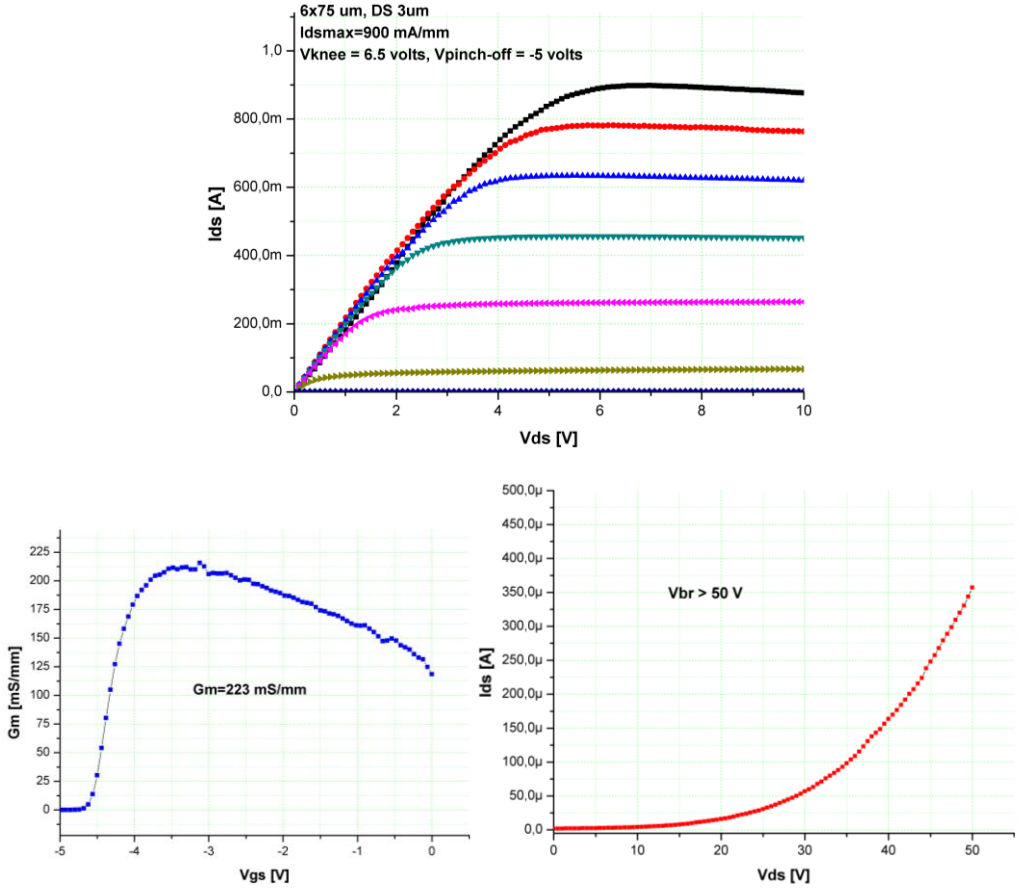

Figure 2.19: DC characterization results of a 6x75 µm GaN HEMT device.

Figure 2.20 shows the DC characterization of the power HEMT device shown in Figure 2.5. Because of the limitations of the characterization setup only one half of the HEMT device was measured at one time. In order to measure the two parts at same time, the device should be bonded to an appropriate HEMT package. As seen from the DC-IV graph, almost no current collapse was occurred due to the heating effects. This proves that the thermally efficient design is successful.

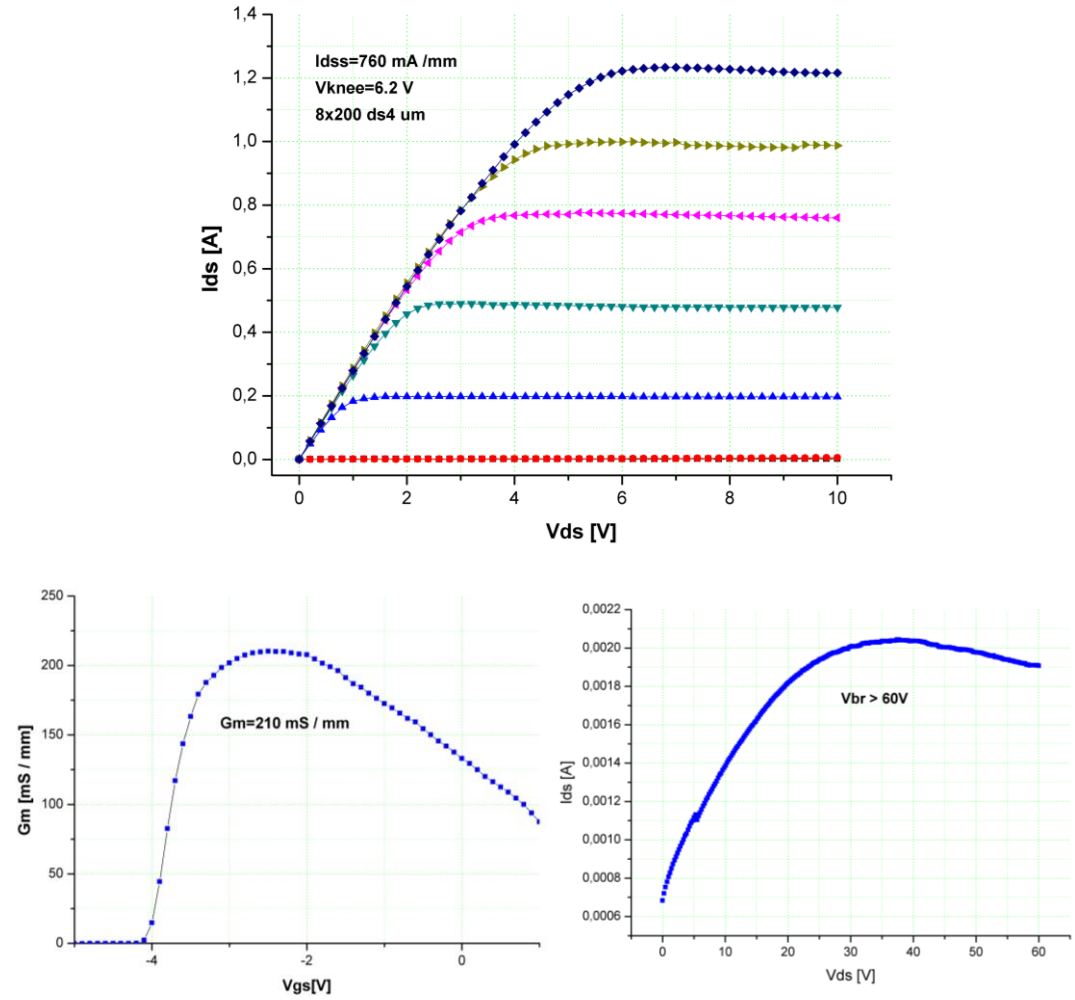

Figure 2.20: DC characterization results of the half part of 16x200 µm (8x200 µm) power HEMT transistor.

AC characterization is performed to determine the current gain cut-off frequency (f_t) and power gain cut-off frequency (f_{max}) of a HEMT device. Figure 2.21 shows the schematic illustration of AC measurement setup and Figure 2.22 shows our AC measurement setup. It consists of an Agilent 8361C PNA network analyzer, Cascade RF1 probe station, Agilent 3631A triple output DC power supply.

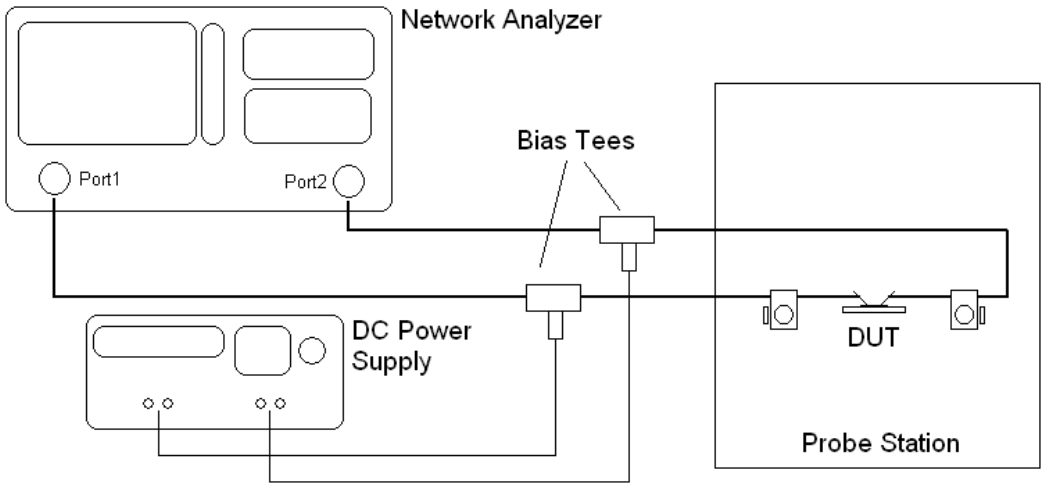

Figure 2.21: Schematic view of an AC measurement setup.

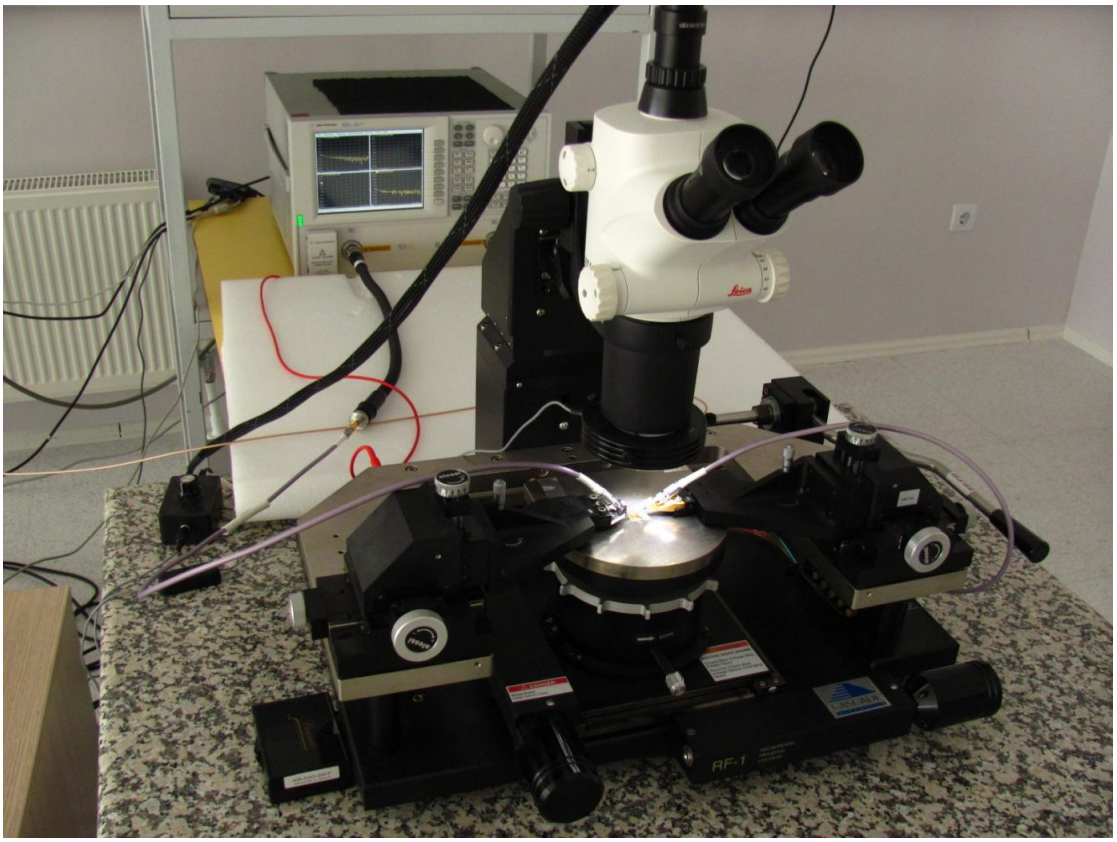

Figure 2.22: A photo of our AC characterization setup.

Network analyzer measures two port S-Parameters of an active device for each frequency point of interest in a desired range. Bias is applied via bias tees from the DC power supply. Measured S-parameters are used to calculate the H21 for each frequency point.H21 formula is given in **(2.3)** [20]. "f_t" is the 0 dB crossing point of the H21 parameter.

$$H_{21} = \frac{-2 \cdot S_{21}}{(1-S_{11}) \cdot (1+S_{22}) + S_{12} \cdot S_{21}} \cdot \qquad \textbf{(2.3)}$$

The unilateral power gain (G_U) is used to determine the f_{max} [21]. Gu is calculated from the measured S-parameters as follows:

$$G_U = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2k \cdot \left|\frac{S_{21}}{S_{12}}\right| - 2\,\mathrm{Re}\left(\frac{S_{21}}{S_{12}}\right)}, \tag{2.4}$$

where *k* is given as follows:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2\,|S_{12}| \cdot |S_{21}|}. \tag{2.5}$$

Calculated G_U is plotted against frequency in dB scale and f_{max} is the 0dB crossing point of the G_U parameter.

AC characterization results of the 8x100 µm and 6x75 µm devices are given in Figure 2.23 and Figure 2.24 respectively.

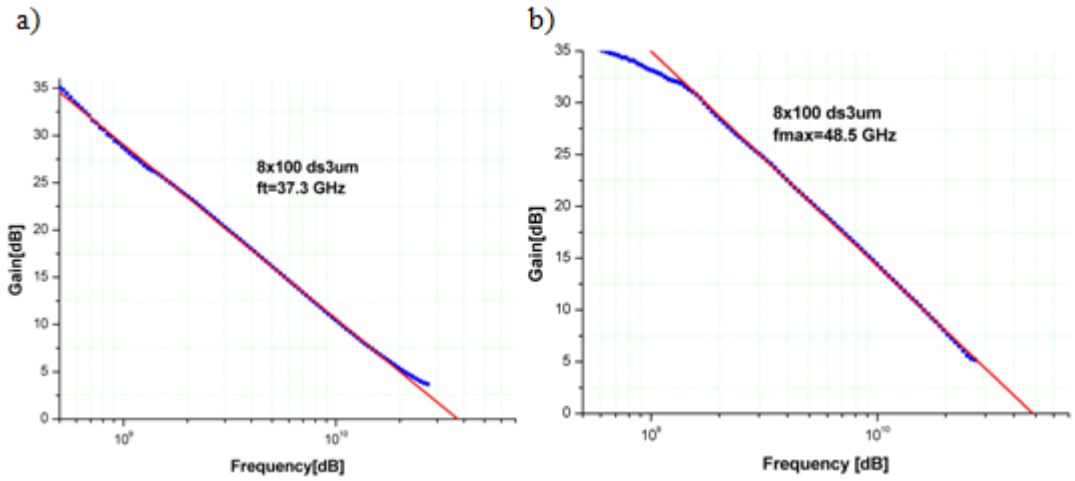

Figure 2.23: Current gain (a) and unilateral power gain (b) graphs of a 8x100 µm GaN HEMT.

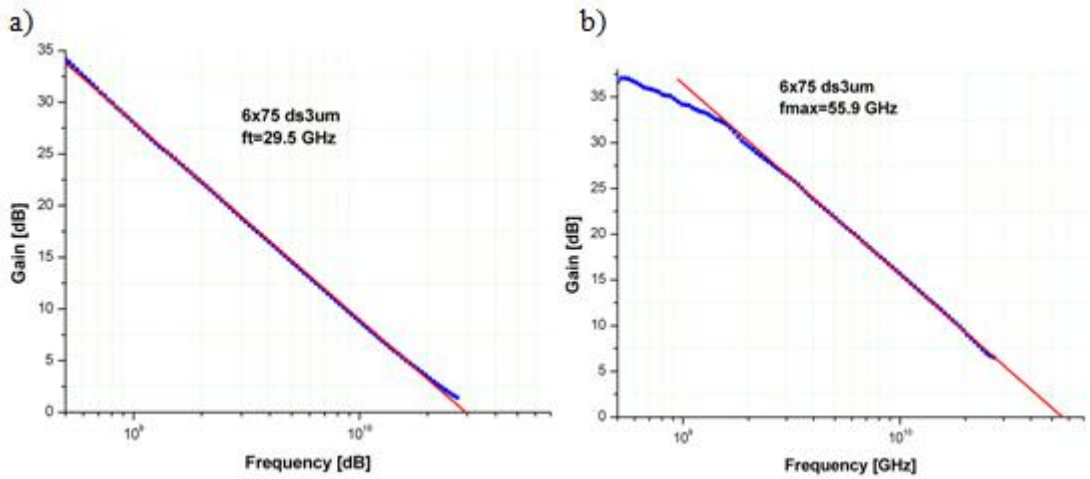

Figure 2.24: Current gain (a) and unilateral power gain (b) graphs of a 6x75 µm GaN HEMT.

Figure 2.25 shows the AC characterization results of the designed power HEMT transistor seen in Figure 2.5. It is again shows only the half of the device because of the limitations of the AC measurement setup. This result proves that our power HEMT design is suitable for high power and high frequency applications.

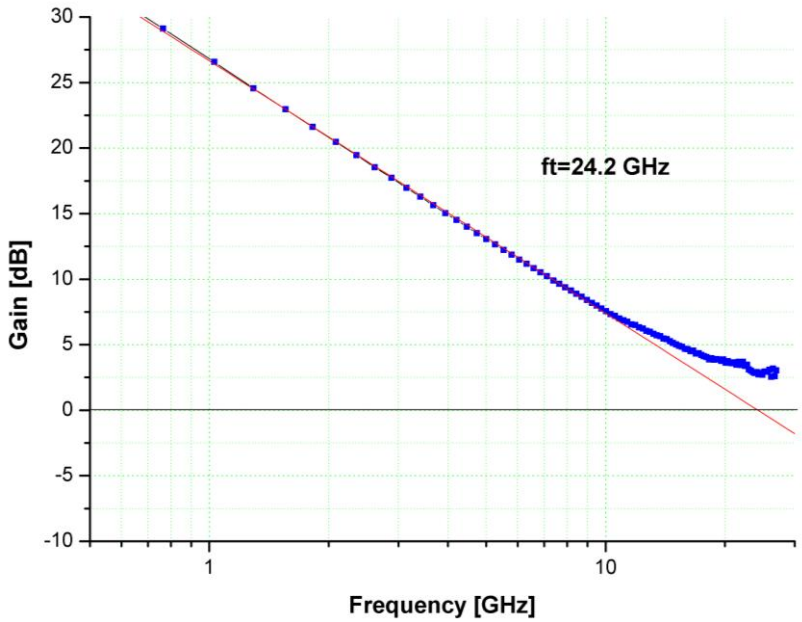

Figure 2.25: Current gain of the half part of the 16x200 µm (8x200 µm) power HEMT transistor

Third characterization is large signal characterization. This characterization is used to determine whether the device is suitable to design amplifiers for any interested frequency and output power. Our large signal measurement setup is shown in Figure 2.26.

Figure 2.26: A photo of our large signal characterization setup.

It consists of a Maury load-pull system (4-26.5 GHz), Agilent 83620B and Agilent 5183A signal generators, Agilent 3631A triple output DC power supply, Agilent 83020A driving amplifier, Agilent 9300B power sensor and Agilent 4419B power meter. Maury load-pull system has two tuners that scans all possible points of the Smith-chart for desired frequencies and performs load-pull measurements. By doing this optimum input and output impedances are determined for maximum output power. For optimum impedances, a power sweep is performed and large signal characterization parameters such as output power, power added efficiency (PAE) and power gain are measured for a fixed output power compliance point such as 3 dB compliance (P_{3dB}). From these results, it is determined whether that HEMT device is suitable for desired specs or not. Figure 2.27 and Figure 2.28 shows large signal measurements of an 8x100 ds3 µm performed at 10 GHz and 6x75 ds3µm performed at 20 GHz GaN HEMT devices respectively.

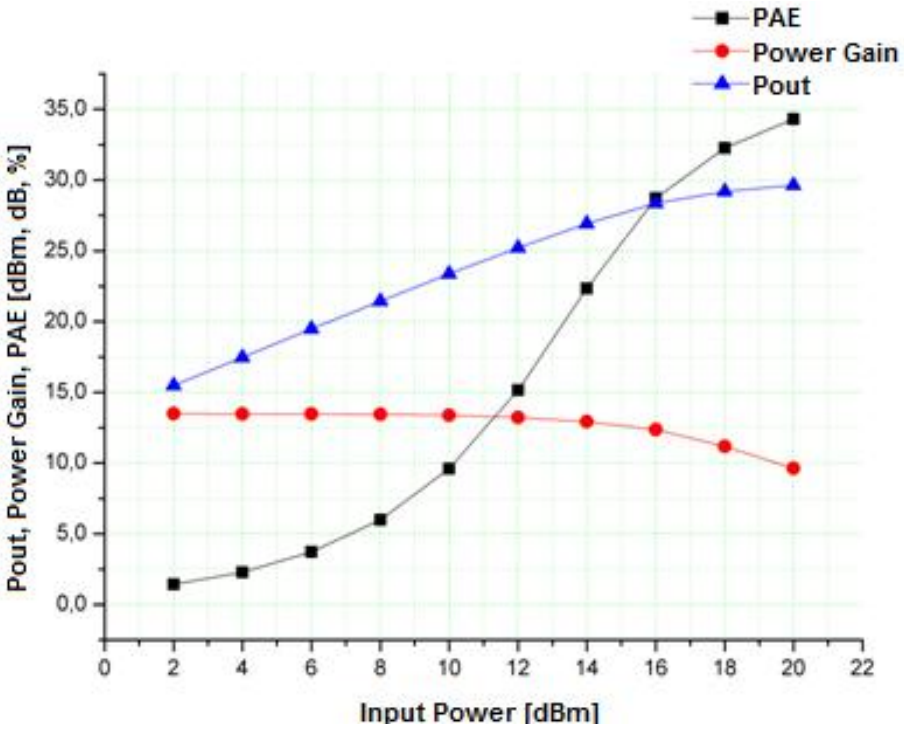

Figure 2.27: Large signal characterization of a 8x100 µm GaN HEMT transistor

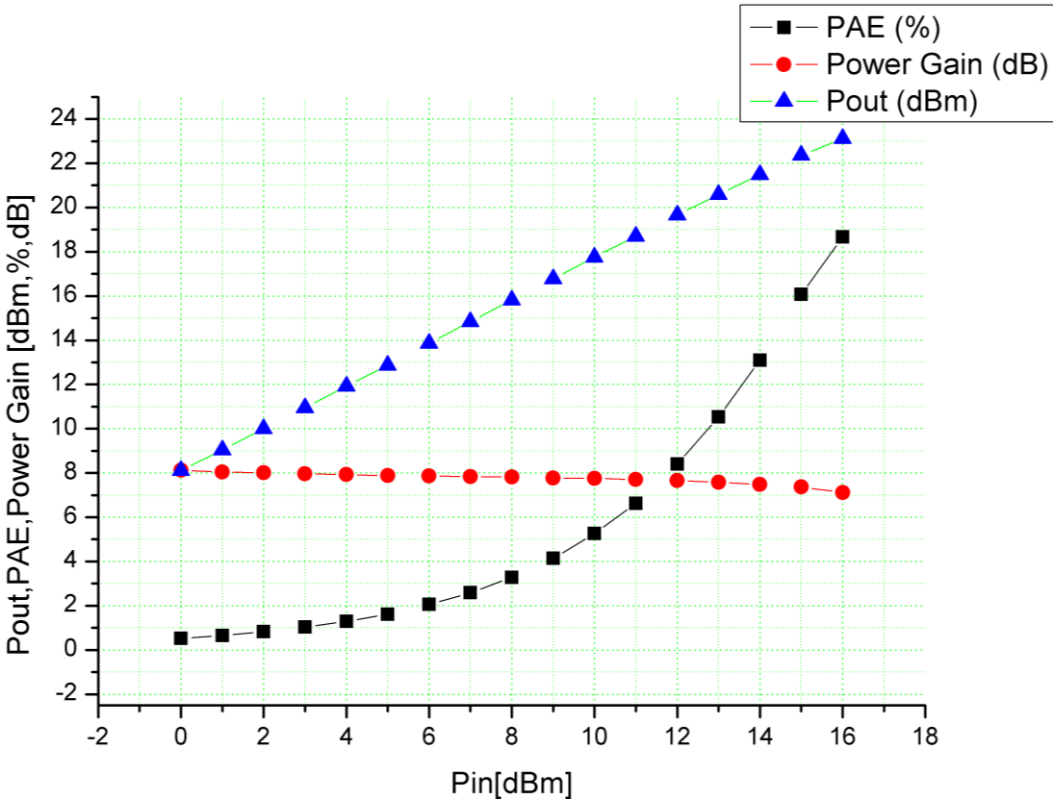

Figure 2.28: Large signal characterization of a 6x75 µm GaN HEMT transistor

3. MODELING OF HEMT DEVICES

Firstly we introduced the details of design considerations, fabrication steps and device characterization of AlGaN/GaN HEMTs. Next step of this cycle is achieving high performance MMICs which requires accurate modeling of these HEMTs. Transistors operating under large-signal conditions exhibit nonlinear behaviors. In this work, especially, we deal with high power amplification, so we need nonlinear large-signal models of AlGaN/GaN HEMT devices in order to design MMIC PAs. These nonlinear models should contain nonlinear behavior of the transistor accurately at high power levels with all possible operation conditions.

Before examining the nonlinear modeling of AlGaN/GaN HEMT devices, let's first talk about small-signal linear modeling which makes up the basis of nonlinear modeling. Small signal modeling gives information about gain, stability, bandwidth and reflection behaviors, however limitations of this models should always be kept in mind while relying on this kind of models. For example, small signal model shows the behavior of transistor for very low signal levels so that the load-line stays near the DC bias point, and when PA is driven with high RF input signals, results can be different than expected because of the nonlinear effects.

3.1 Small-Signal Linear Modeling of HEMTs

The small-signal linear models are extracted from the S-parameter measurements which are taken under various bias conditions. Figure 3.1 shows the electrical equivalent circuit (EEC) of the small-signal model of a typical HEMT device. EEC contains bias independent extrinsic elements like parasitic inductances, capacitances and resistances, and bias dependent intrinsic elements that seen in the dashed area.

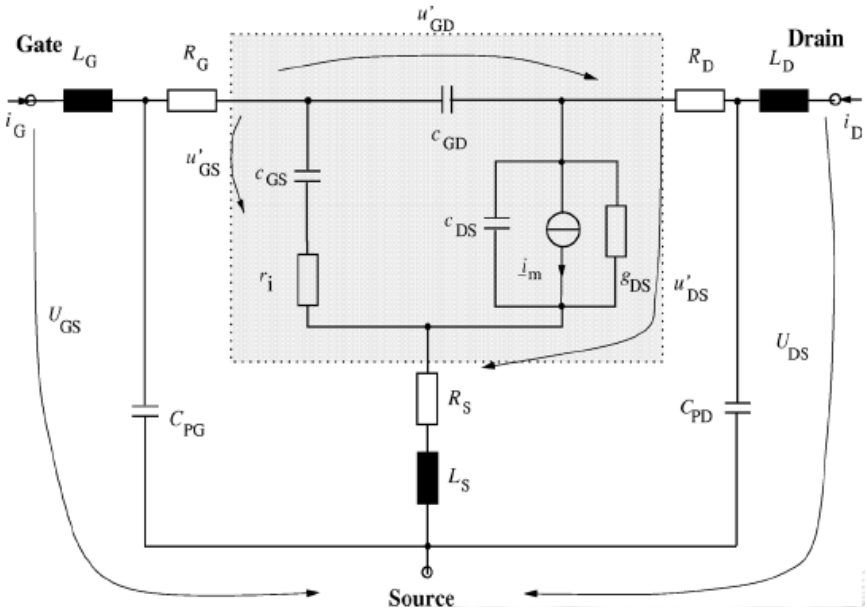

Figure 3.1: The bias dependent small-signal equivalent circuit of the HEMT device.

To obtain the linear small-signal model, these EEC elements need to be extracted systematically using the S-parameter measurements. Extraction methodology steps are:

- Determination of extrinsic elements
  - Extraction of parasitic capacitances
  - Extraction of parasitic inductances and resistances
- Determination of intrinsic elements

Determination of the extrinsic elements are done by using two s-parameter measurements under "*cold*" bias conditions (V_{DS}=0V). For the extraction of parasitic capacitances "*pinched cold*" s-parameters (V_{GS}<$V_{pinch\text{-}off}$, V_{DS}=0V) are used. Under this bias conditions EEC forms a specific "Π" shape configuration which can be seen in Figure 3.2a, so imaginary parts of the Y-parameters of this EEC are considered. Moreover, at low frequency, parasitic capacitances can be determined by linear fitting since resistances and inductances are eliminated under these conditions. Next step is the extraction of parasitic inductances and resistances under *"gate forward cold"* conditions (V_{GS}>0V, V_{DS}=0V). Under this bias conditions EEC forms a "T" shape circuit, so Z parameters are taken into account. Imaginary parts of the Z parameters are used to determine inductances. We have 4 unknown resistances and 3 resistance equations from real parts of the Z-parameters. Additional required information about parasitic resistances is taken from real part of the Z_{22} under

"pinched cold" bias condition. As a result all the extrinsic elements could be extracted based on simple S-parameter measurements.

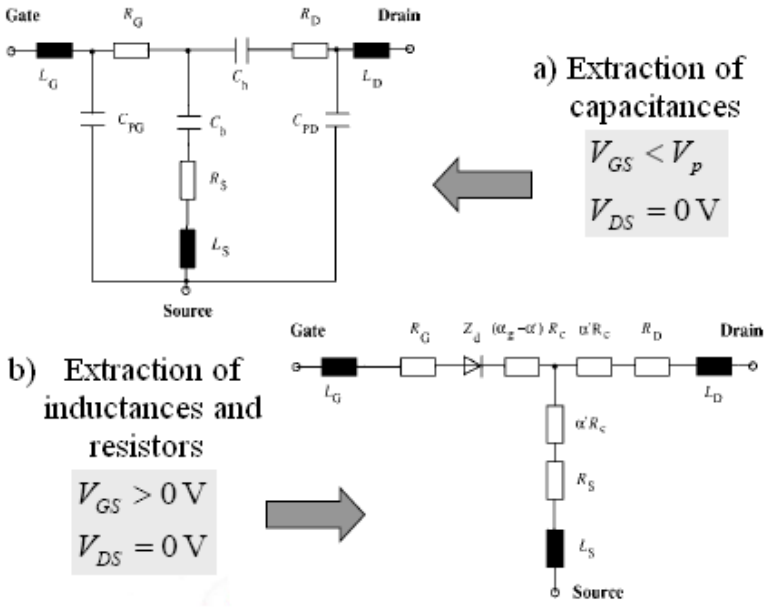

Figure 3.2: Summary of extrinsic element extraction methodology, and corresponding EECs under(a) "pinched-cold" and (b) "gate forward cold" conditions.

Before determining the intrinsic parameters, extrinsic elements need to be de-embedded properly from the S-parameter measurements starting from outer extrinsic elements to inner ones as seen in Figure 3.3. First, s-parameters are converted z-parameters and series elements L_G and L_D are subtracted. Then, resulting Z-parameters are converted to Y-parameters and parallel elements C_{PG} and C_{PD} are subtracted. Finally, updated Y-parameters are converted back to Z-parameters and series elements R_G, R_D, R_S and L_S are subtracted.

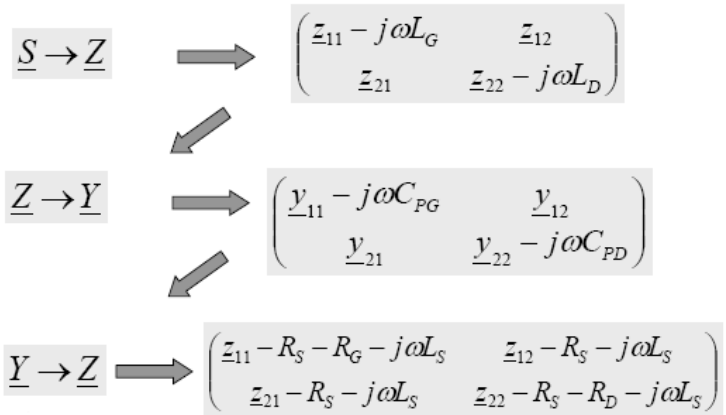

Figure 3.3: Steps of extrinsic elements de-embedding.

Due to EEC has “Π” type topology, the final form after de-embedding process should be converted from Z-parameters to Y-parameters. Similar to determination of extrinsic elements, intrinsic elements are extracted by parameter fitting. Additionally, this process is repeated for all measured bias conditions in order to determine bias dependent intrinsic parameters. As a result, broadband bias dependent small-signal model is completed. This kind of model requires optimization process for each element during extraction steps which allows the model simulation results fit best to the measurement data.

3.2 Large-Signal Nonlinear Modeling of HEMT Devices

There are several methods of large-signal nonlinear modeling, such as physical models, analytical models and table-based models. As illustrated in [22-27], physical models require very accurate data like density of states and dislocations, bandgap energies, polarization properties, doping concentrations, saturated electron velocity and electron mobility in the channel, material growth and fabrication process parameters, and dielectric constants in order to estimate the overall device performance. Physical modeling uses Schrödinger and Poisson’s equations as a tool. Analytical formulas and/or numerically solved nonlinear partial differential equations, describing the internal field distribution, charge transport, current continuity and energy conservation, are used in physical equations in order to obtain the model [28-31]. Moreover, physical models are very time consuming in terms of computation complexity and their results are not directly compatible with circuit simulators. Hence, physical models are generally not appropriate for the circuit design purpose.

Analytical models are based on measurement data of active devices. The measurement data consist of DC or “pulsed” I-V and CW or “pulsed” S-parameters under various bias points. These data are interpreted by using electrical equivalent circuit as explained in small signal linear modeling. Nonlinear model is constructed using extracted intrinsic elements and corresponding analytical functions. On the other hand, transistor physics related analytical functions are used to form the model. Because of these functions are not concerned with the physical properties of the transistor, some physical effects are not considered compared to physical models. This modeling approach is complaint with circuit simulators and able to simulate beyond the measurement range reasonably due to the analytical function behavior of the model.

On the other hand, this technique is technology dependent and requires some understanding in the device modeling process for circuit designers to have effective design cycle.

Table-based models are only based on measurement data and predefined equations defining the transistor behavior are not needed compared to analytical models that this method has more accurate and technology independent models. Measured data are interpolated and smoothed by using multidimensional spline functions. Figure 3.4 shows equivalent circuit used for the table-based nonlinear modeling. Small signal counterparts of the circuit elements are extracted as first and then, nonlinear element functions are derived by integrating over bias dependent differential equations determined from measurement data. Root suggested this method firstly [32]. Afterwards an improvement was achieved by using time delay in charge formulation [33].

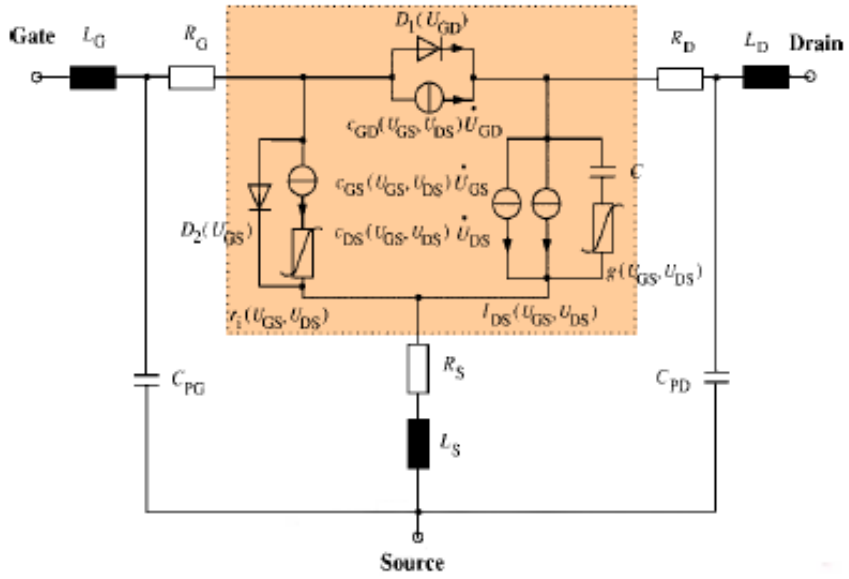

Figure 3.4: The large-signal electrical equivalent circuit of the HEMT device.

In this thesis table-based modeling technique is used in order to obtain a nonlinear large-signal model of our 4x75µm AlGaN/GaN HEMT on SiC substrate. To do so, TOPAS (TransistOr Parameter Scalable model) software developed by IMST GmbH is used. TOPAS is a kind of table based model which produces very promising results compared to other modeling techniques. There are various advantages of this type of nonlinear modeling: no need for time consuming very complex and expensive large signal characterization tools, fast implementation, every measured

characteristic of the device can be transferred into the model accurately without having physical interpretation of the device behavior, extracted model is directly compatible with circuit simulators, small-signal results of large-signal simulations are consistent with S-parameter measurements. Based on 4x75µm GaN HEMT model extraction, details of the nonlinear large-signal table-based modeling using TOPAS software is given in the next subsection.

3.3 Large-Signal Nonlinear Model Extraction of Our GaN HEMT Using TOPAS Software

First, we will focus on measurement method and setup large-signal modeling. For devices suffer from excessive self heating effects and high channel temperature such as GaN HEMTs, "pulsed" I-V and "pulsed" S-parameter measurements are important for appropriate large-signal modeling, however measurements taken under CW I-V can also results accurate models for circuit designing with reasonable error. Our CW measurement setup for modeling can be seen in Figure 3.5.

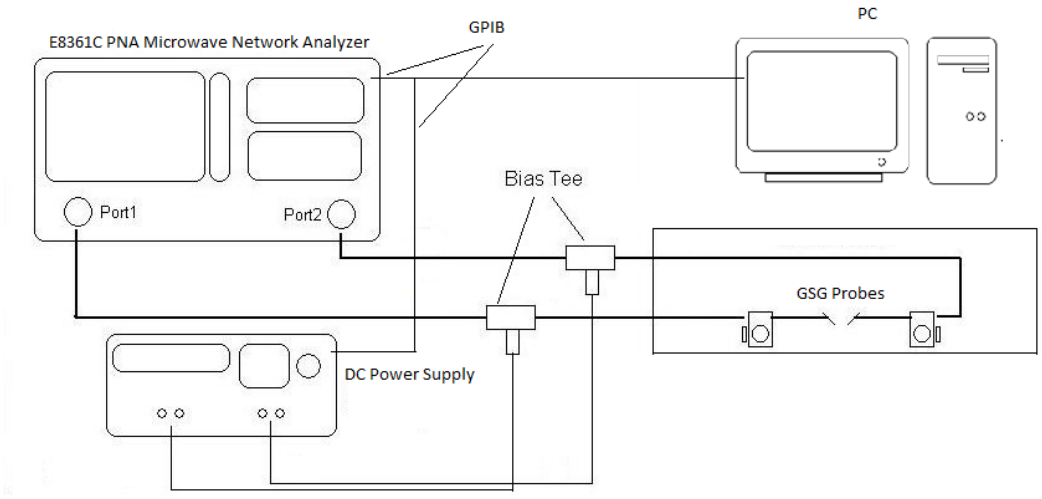

Figure 3.5: Schematic illustration of the CW measurement setup in Bilkent NANOTAM

On the PC we developed a Labview project in order to control the measurement and then save the s-parameter data for every single bias condition defined in the software. Labview software (VI) user interface can be seen in Figure 3.6.

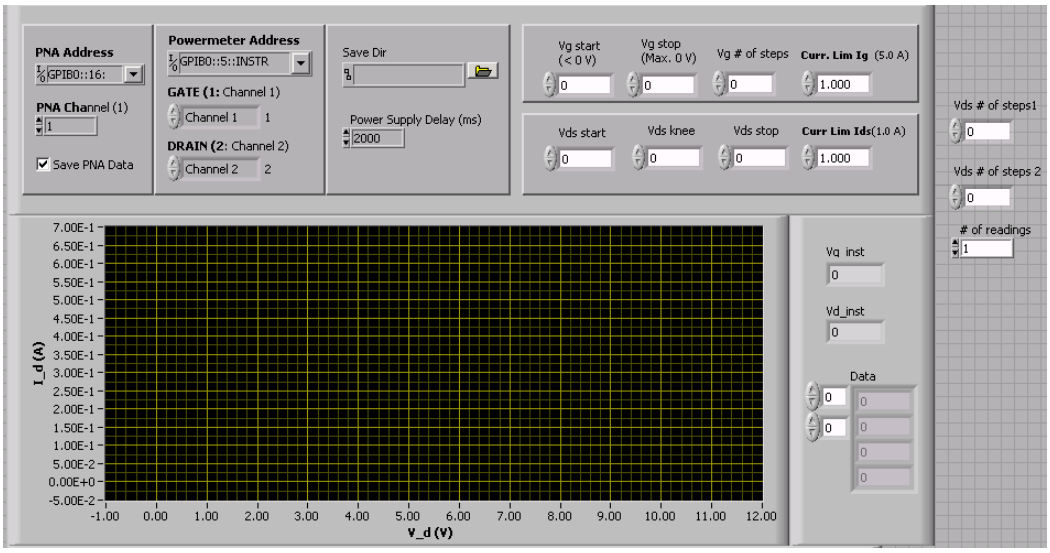

Figure 3.6: Labview software user interface for modeling measurements

In the software gate voltage is swept from pinch-off voltage to 0V gate voltage which is the maximum from the concerning channel of our DC power supply. Drain voltage sweep consists of two phases: first drain voltage is swept from 0V to knee voltage of the transistor with small steps such as 0.1-0.2V, and then drain voltage is swept from knee voltage to 15-20V drain voltage, which is determined mainly by application, with larger steps such as 1V. Accurate large signal modeling needs a lot of s-parameter data for various bias conditions. To reduce the temperature effects especially at high drain voltage points, larger steps are used compared to low drain voltages. S-parameter measurement data is saved for every single bias condition. Power supply delay is required for taking stable S-parameter data for every single bias point. A sample Labview screenshot of the resulting DC-IV plot can be seen in Figure 3.7.

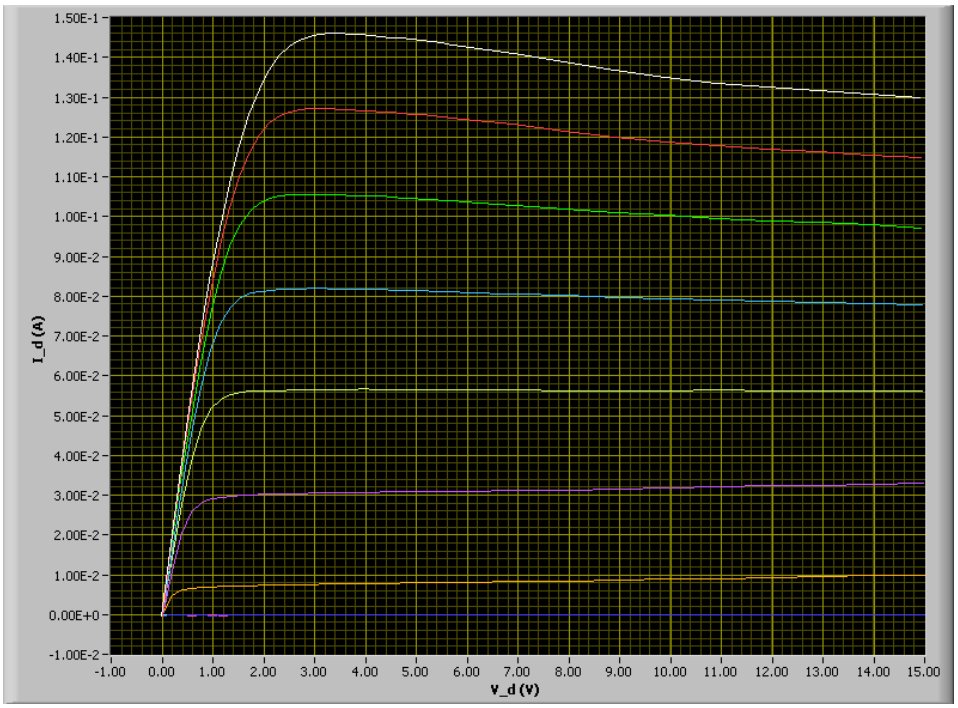

Figure 3.7: Screenshot of a modeling measurement performed in Bilkent NANOTAM

Next step is extraction of the small-signal equivalent circuit elements as basically explained in the beginning of this part. TOPAS software is used for every step of the model extraction. The software has a user friendly interface which guides the user throughout the model generation. First, dummy extrinsic elements are calculated under "cold" conditions as shown in Figure 3.8-a. After that extrinsic elements are optimized as shown in Figure 3.8-b.

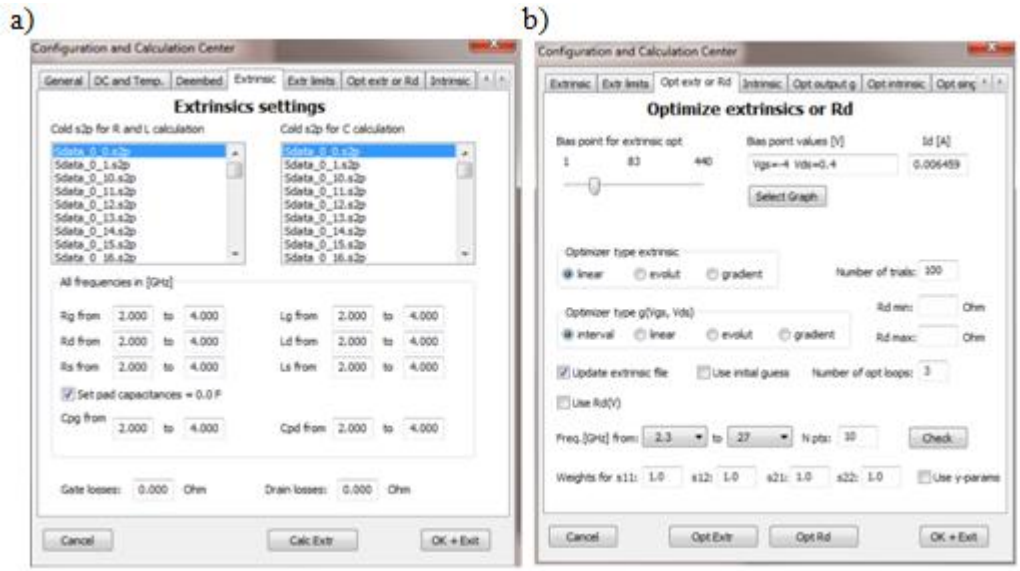

Figure 3.8: Screenshot of the a) dummy extrinsic element calculation b) extrinsic element optimization window on TOPAS.

In the next step, the frequency ranges for intrinsic element extraction are adapted to the GaN measurements, and then intrinsic elements are calculated according to calculated extrinsic elements. Corresponding screenshot is shown in Figure 3.9-a.

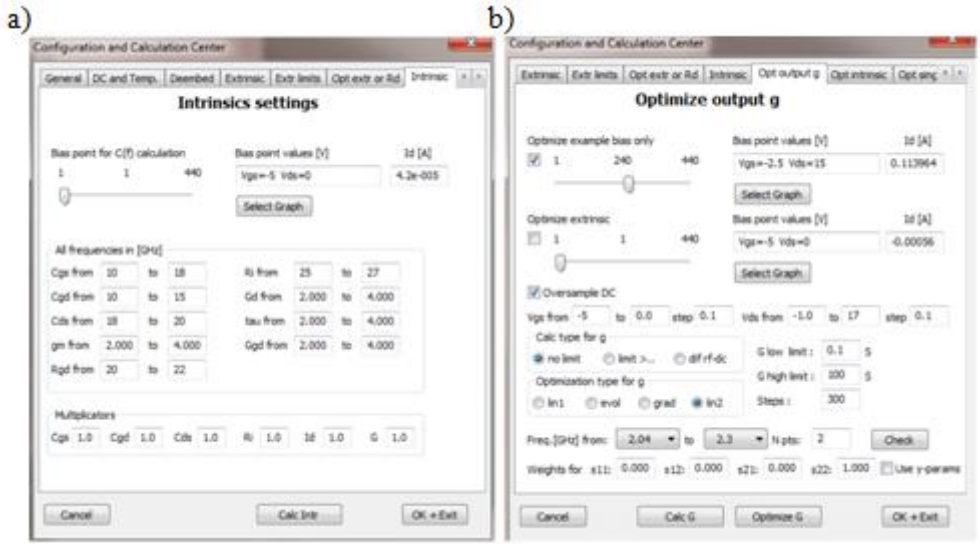

Figure 3.9: Screenshot of the a) frequency range change b) output conductance G optimization window on TOPAS.

Frequency intervals can be change in order to obtain better fit to measured data in the intrinsic section. Output conductance G is calculated and optimized from the optimize output g section in the next step as shown in Figure 3.9-b. This iterative approach is applied until sufficient good fit of s-parameters obtained. An example of a good s-parameter fit of measurement and model result can be seen in Figure 3.10. Here red lines are modeled s-parameters and blue lines are measured data.

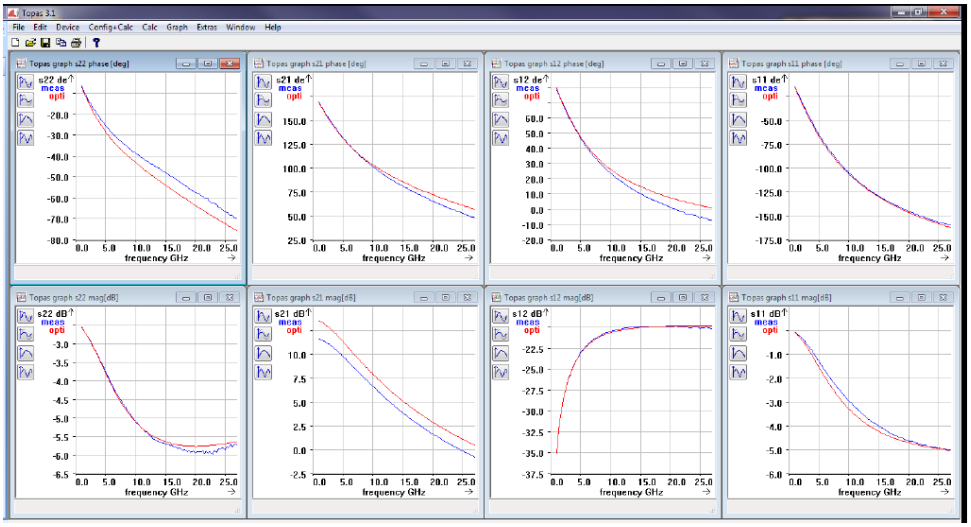

Figure 3.10: Screenshot of the s-parameter fit window on TOPAS.

Voltage de-embedding process, which relates intrinsic element parameters with actual bias voltages, comes next before calculating the nonlinear model parameters. (3.1) and (3.2) show the inner bias voltages as a function of outer voltages and drain source current I_{DS} [34].

$$V_{GS}' = V_{GS} - I_{DS}(V_{GS}, V_{DS}) \cdot R_S \quad \textbf{(3.1)}$$

$$V_{DS}' = V_{DS} - I_{DS}(V_{GS}, V_{DS}) \cdot (R_D + R_S) \quad \textbf{(3.2)}$$

TOPAS software performs spline interpolation technique to generate bias dependent continuous nonlinear function of each intrinsic element. Spline functions need equidistant data; however the data calculated from (3.1) has non equidistant grids. TOPAS uses two dimensional spline interpolations to form equidistant grid for gate and drain voltages in order to solve this problem.

For the last step before the TOPAS model generation, nonlinear model parameters calculated based on the bias dependent intrinsic element functions. In TOPAS, the calculations are made by transforming the charge sources to current sources. By using this technique, transcapacitances are not needed in the small-signal equivalent circuit, because a charge source calculation is not required. Equations of large signal current sources with respect to large-signal capacitances are given as follows [35]:

$$I_{GS} = c_{GS}(V_{GS}, V_{DS}) \cdot \dot{V}_{GS} \quad \textbf{(3.3)}$$

$$I_{GD} = c_{GD}(V_{GS}, V_{DS}) \cdot \dot{V}_{GD} \quad \textbf{(3.4)}$$

$$I_{DS} = c_{DS}(V_{GS}, V_{DS}) \cdot \dot{V}_{DS} \quad \textbf{(3.5)}$$

Conservative extrapolation techniques used by TOPAS allows us to obtain better harmonic balance convergence. Finally all the information about the parameters of equivalent circuit is saved in a file that can be recognized by Agilent's Advanced Design System.

3.4 Testing the Large-Signal Model of GaN HEMT

There are two main steps to test the large signal nonlinear models. First we need to check the model consistency between simulated and measured s-parameters. Second

step is controlling the large-signal behavior by using load-pull measurements and harmonic balance simulations.

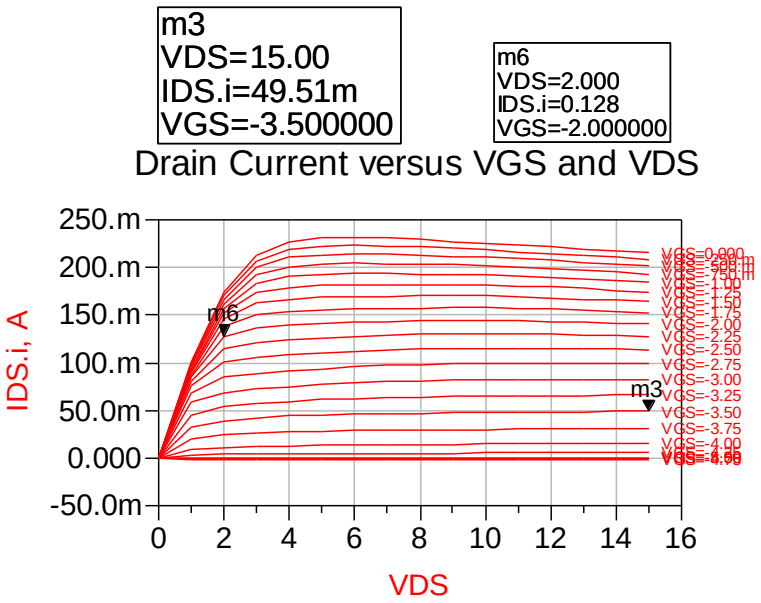

Figure 3.11: Output IV curves of the modeled GaN HEMT.

Output I-V graph of our model is given in Figure 3.11. Simulation and measurement results fits very well for selected two different bias points for our nonlinear GaN HEMT model as shown in Figure 2.12 and Figure 2.13. Therefore, this proves that the model is consistent.

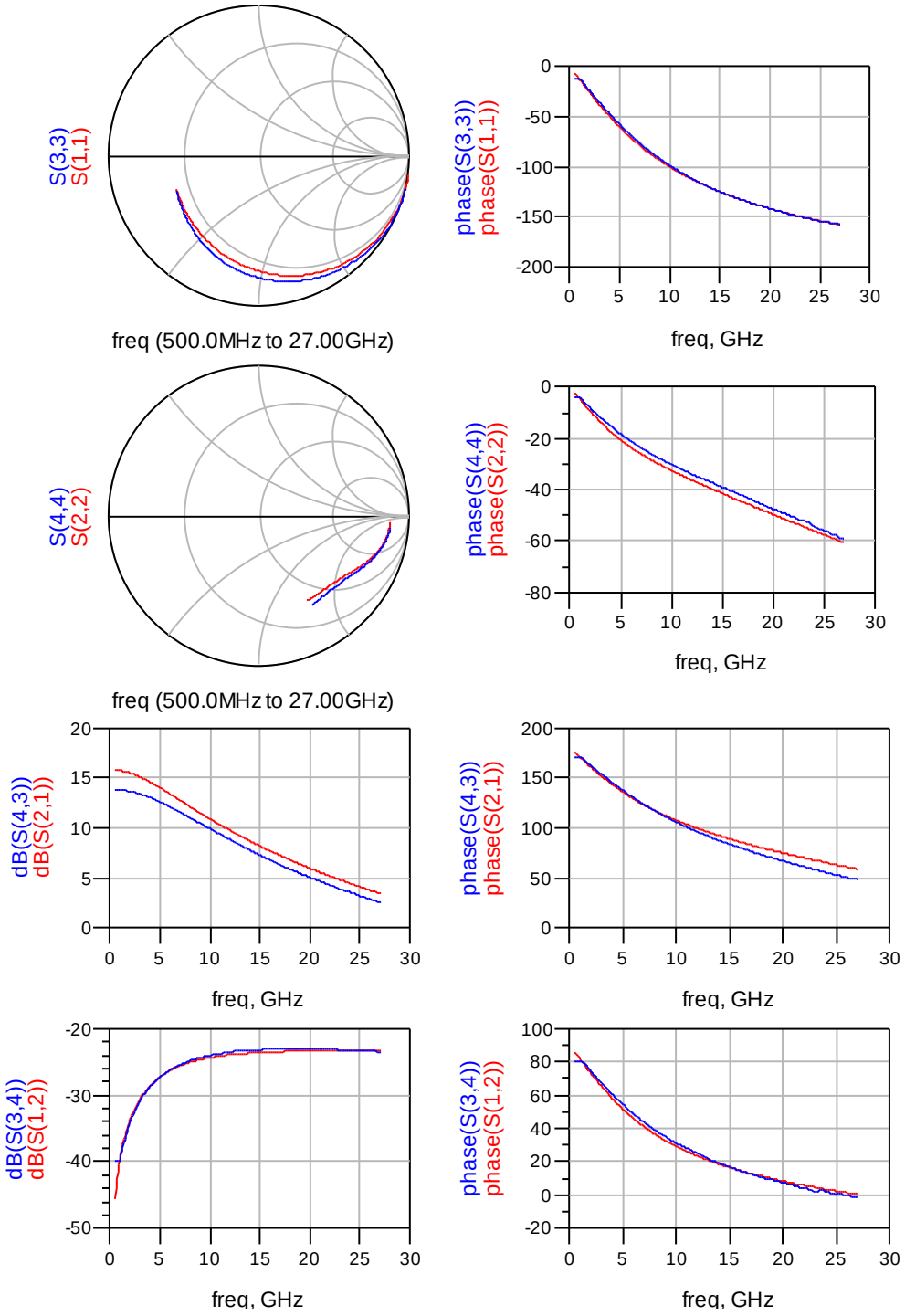

Figure 3.12: Comparison of measured (blue curves) and simulated (red curves) (using nonlinear TOPAS model) S-parameters at bias point "m3" (V_{GS}=-3.5V, V_{DS}=15V).

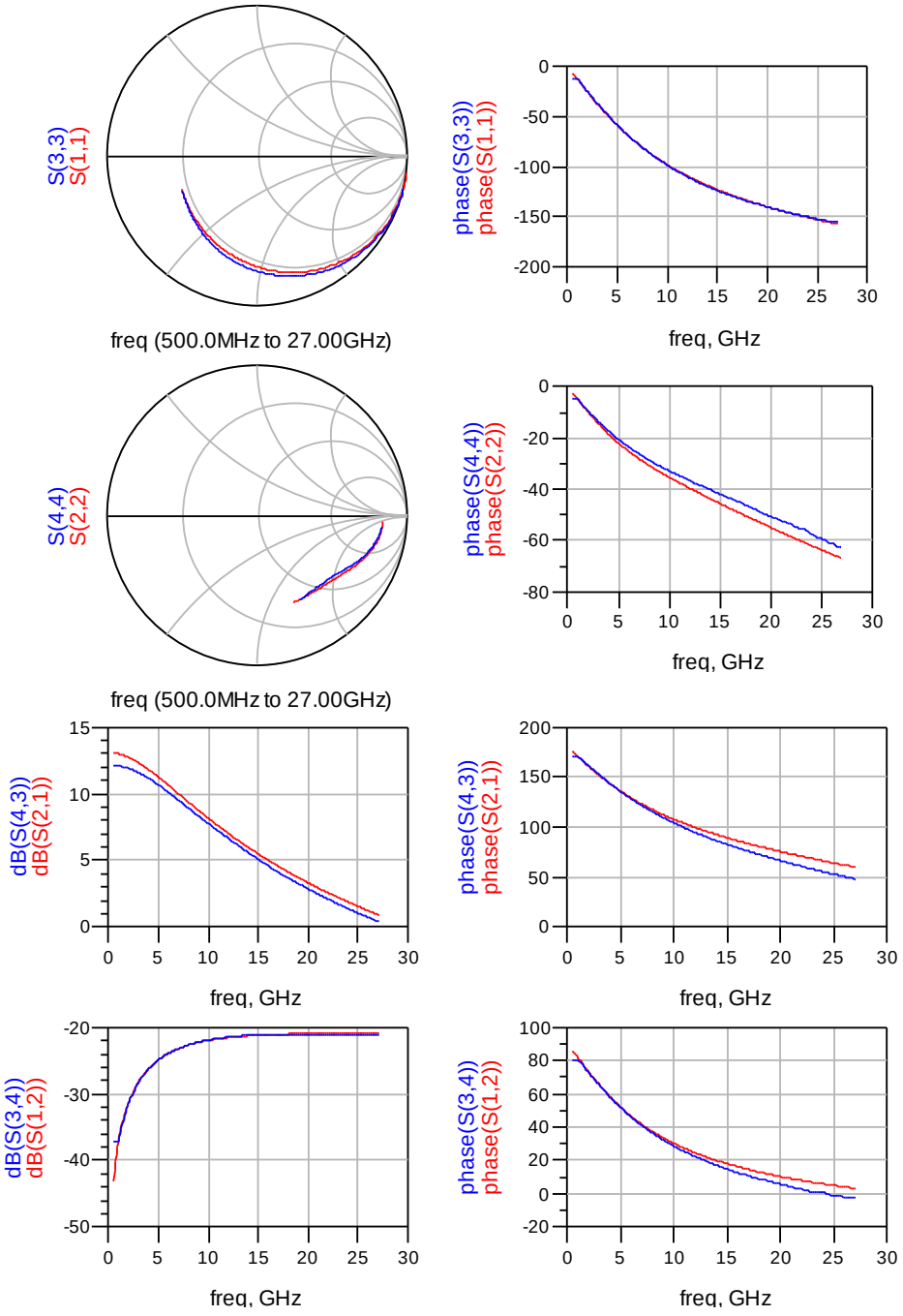

Figure 3.13: Comparison of measured (blue curves) and simulated (red curves) (using nonlinear TOPAS model) S-parameters at bias point "m6" (V_{GS}=-2V, V_{DS}=2V).

The next step is testing the model accuracy under large-signal levels. To do so, load-pull measurements are performed in Bilkent NANOTAM and at the same time harmonic balance simulations are made under the same conditions. Load pull measurements are carried out at 20.2 GHz under CW and 10 dBm input signal. Bias voltages selected as VGS=-3.75V and VDS=15V. Optimum load and source impedances were found to be (16.22 + j*27.88) Ohm and (9.41 + j*10.07) ohm respectively from load-pull measurements. Load-pull and source-pull simulations has

also good agreement with measured impedances, therefore our large-signal results should be similar. Figure 3.14 shows the simulated and measured output power and power gain of the 4x75µm GaN HEMT transistor.

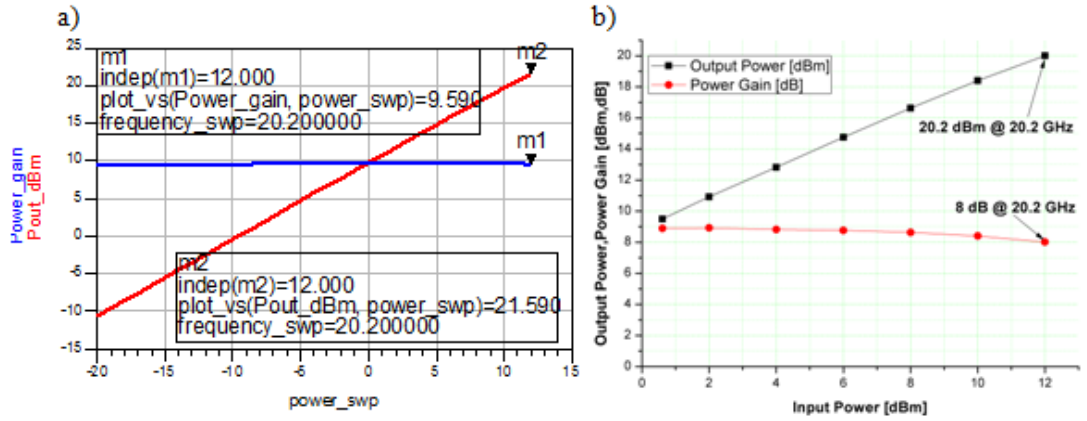

Figure 3.14: Output power and power gain comparisons between a) our GaN HEMT "CW" model b) CW power measurements.

Our model is based on the CW measurements which have taken only at one temperature (room temperature for us) because of the limitations on the measurement setup, so our model cannot predict self heating effects accurately. However, during large signal CW measurements, there is an extreme heat generation occurring in the channel which causes current collapse and output power degradation. Therefore a mismatch between simulation and measurement is expected because of the reason explained above. As seen from the Figure 3.14, there is a mismatch about 1.5 dB between simulation and measurement results. Although there is a mismatch between our model and measurement results, our model can still indicate a good fit for large-signal impedances and can still be used for CW circuit design if the output power is estimated carefully. In the next part, a coplanar MMIC power amplifier designs at 5 GHz and 20.2 GHz using our GaN HEMT models will be presented.

4. GAN HEMT COPLANAR MMIC POWER AMPLIFIER DESIGNS

This part contains two coplanar waveguide (CPW) MMIC power amplifier (PA) designs. The designed GaN MMIC PAs are based on our applications and using our own GaN HEMT large-signal models and COPLAN software of IMST GmbH. First GaN MMIC PA is designed with two 4x75 μm transistors in parallel at 20.1 GHz and second MMIC is designed with 6x150 μm transistor at 5 GHz. First GaN MMIC PA has a 603mW measured output power at 20.1 GHz and second GaN MMIC PA has a 2.7 W measured output power at 5.26 GHz.

Firstly, general PA design considerations and COPLAN software will be explained briefly and continue with our design steps. Lastly, simulation and measurement results will be presented.

4.1 20 GHz CPW GaN MMIC PA Design

In literature we can see numerous amplifier types classified with respect to their bias voltages and output termination impedances of active devices [36-38]. These classes can be split into two main groups as analog-mode and switch-mode. Class-A, Class-AB, Class-B and Class-C Pas can be given as an example for analog mode designs. In the analog mode designs, conduction angle, which is a function of the quiescent bias point and input derive level, defines the classes of operation. Figure 4.1 shows the conduction angles, transfer characteristics and active load-lines of those PAs.

Class-D, Class-E and Class-F are considered as switch mode PA designs. These Pas have very high efficiency levels; however these types are not studied in this work because of their nonlinearities, low power gain outputs and narrow bands compared to analog mode designs.

In this work, Class-A topology is selected among other classes in terms of having highest large signal gain and most linear output. On the other hand, Class-A type PAs have a %50 PAE limit in theory. Figure 4.2 shows the details of Class A operation.

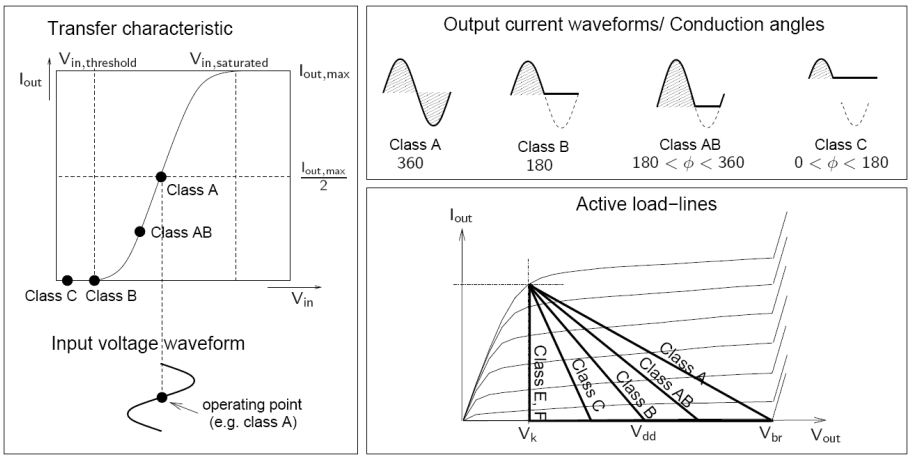

Figure 4.1: Important properties of various PA classes of operation

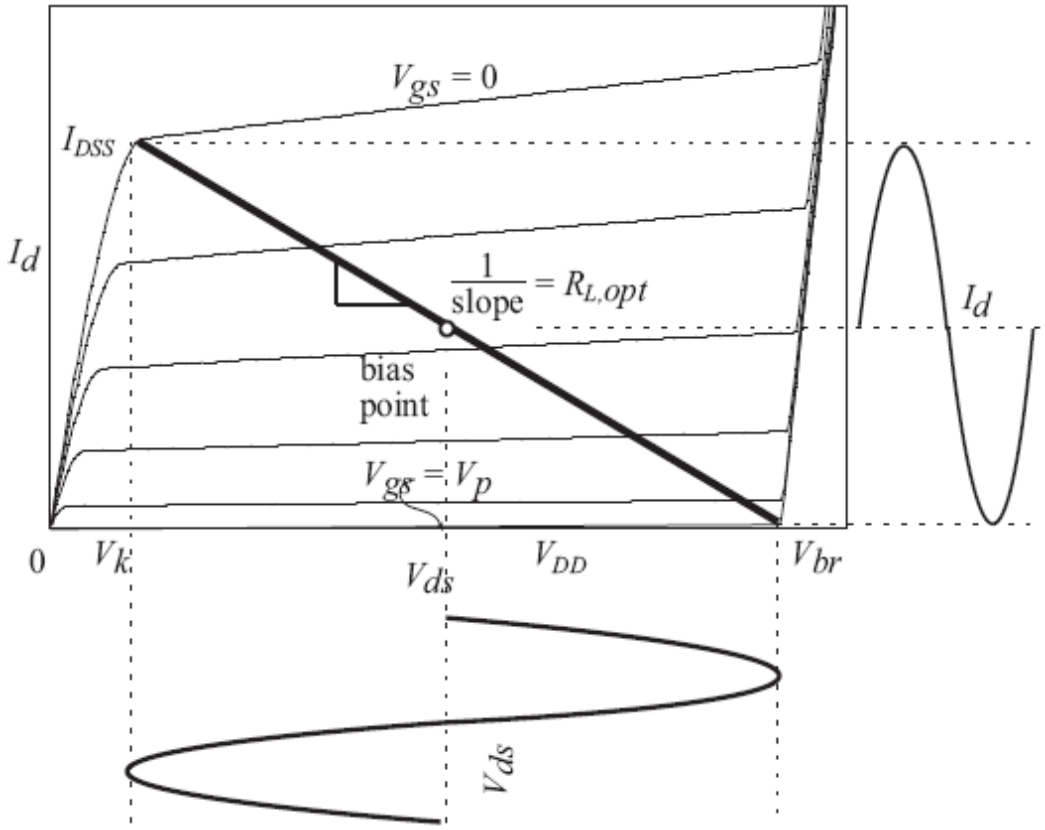

Figure 4.2: Class A PA operation.

Next step is source-load impedance determination to maximize the output power by performing load-pull and source-pull simulations. Firstly, source impedance is set to a low value and load-pull simulation is performed and optimum impedance for maximizing the output power is determined. Next, source-pull simulation is performed according to the output impedance fixed at previous step to get optimum source impedance. This iterative approach is performed until no significant improvement is obtained. Figure 4.3 and Figure 4.4 shows the optimum load and

source impedances respectively performed at 20.1 GHz for two 4x75 um transistors in parallel.

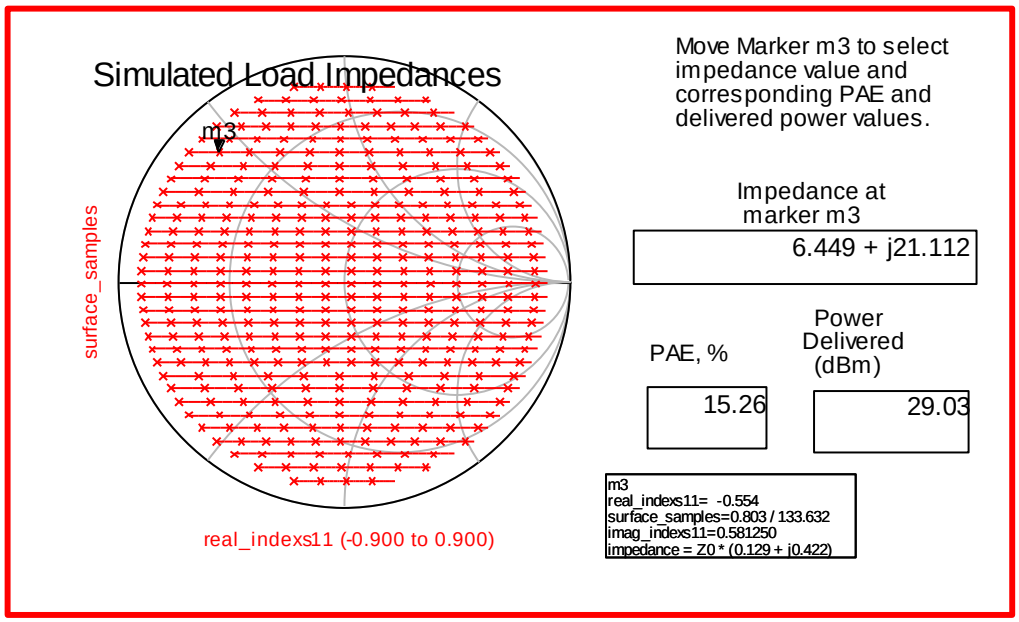

Figure 4.3: Load-pull simulation result of our GaN HEMT model.

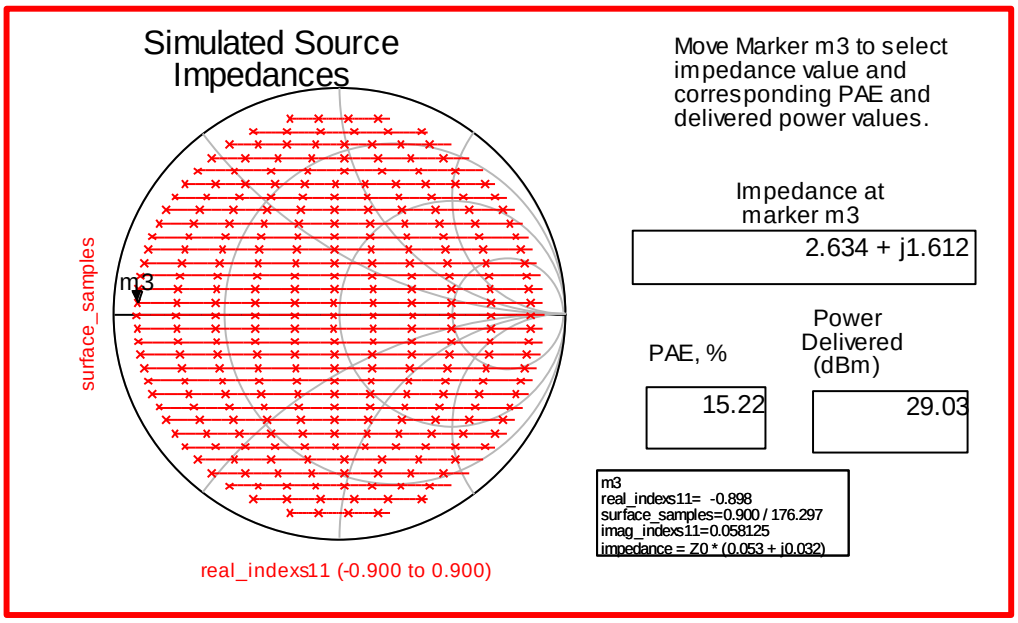

Figure 4.4: Source-pull simulation result of our GaN HEMT model.

These predefined impedances should be transformed to 50Ω environment, which is selected as reference impedance in RF and microwave systems [39, 40]; by using an output matching network (OMN) and input matching network (IMN). Using smith-chart tool in ADS, output and input matching networks are designed with ideal-lumped elements. Screenshot of the smith-chart tool in ADS for OMN and IMN is shown in Figure 4.5 and Figure 4.6 respectively. Single L-C low-pass topologies are

selected for both matching networks and open stub is used for shunt capacitors in the L-C branch.

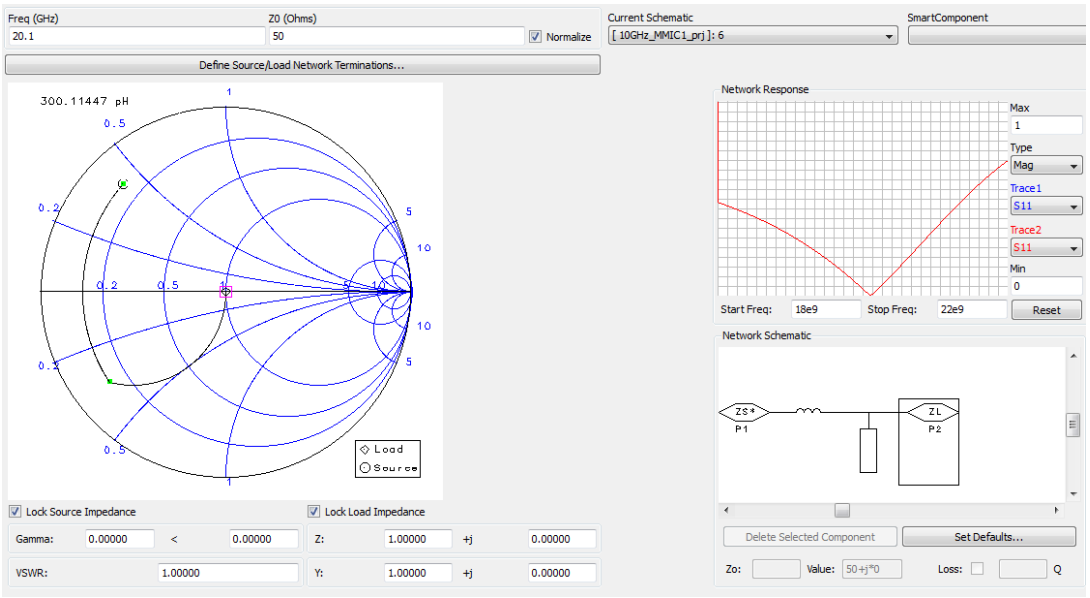

Figure 4.5: Output matching network design with Smith chart tool in ADS.

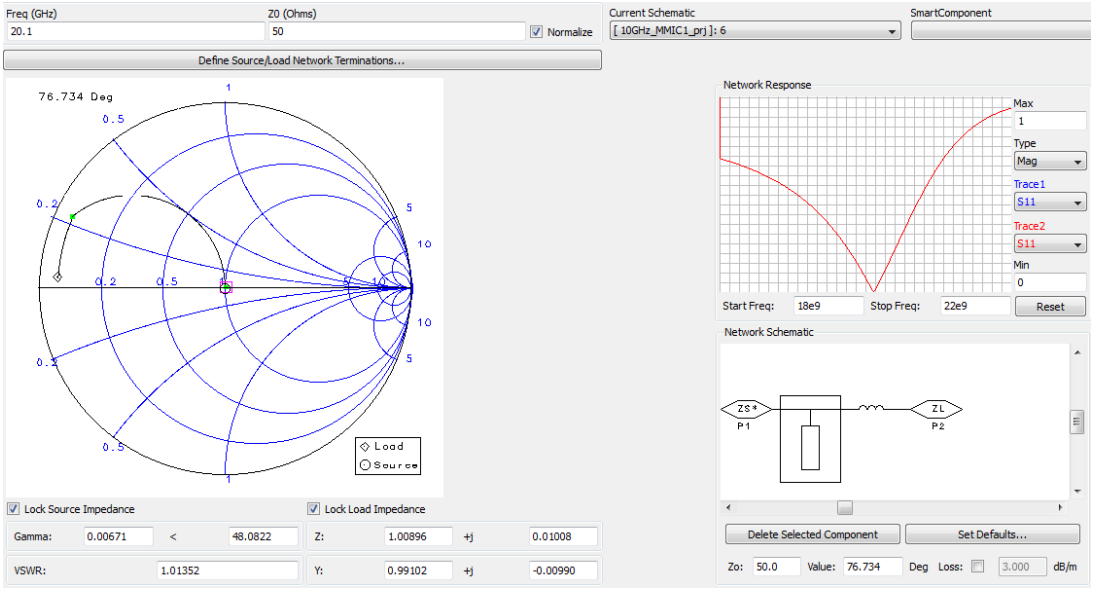

Figure 4.6: Input matching network design with Smith chart tool in ADS.

Complete ADS schematic of the GaN MMIC design with lumped elements is shown in Figure 4.7. These elements are the reference point for the real MMIC design and at next step these ideal elements are replaced with real passive elements and transmission lines. For real elements COPLAN software of IMST GmbH is used.

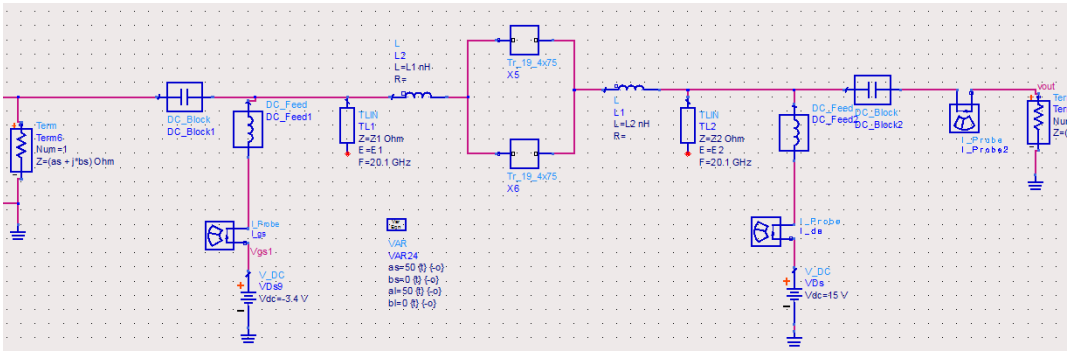

Figure 4.7: ADS schematic of the designed GaN MMIC Power Amplifier (PA) with ideal lumped elements.

COPLAN is a design and simulation tool for CPW structures in ADS. Because of having a quasi-static finite difference method, it can handle 3D electromagnetic simulations of the CPW structures; so, all the parasitic effects like thicknesses in metallization, coupling effects are considered during simulation allowing an accurate CPW MMIC design.

Figure 4.8 shows the ADS schematic of the GaN MMIC design with real COPLAN elements and Figure 4.9 is the final layout representation of this design.

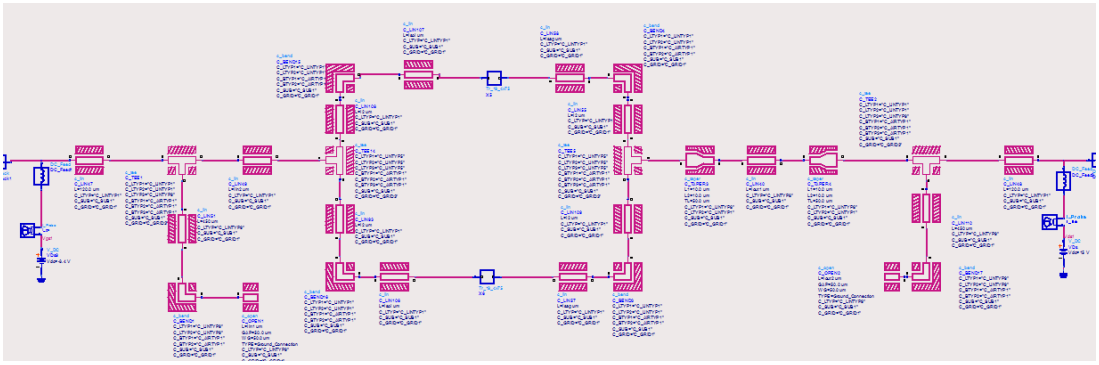

Figure 4.8: ADS schematic of the designed GaN MMIC Power Amplifier (PA) with COPLAN elements

In RF and microwave systems RF grounding is crucial. At such high frequencies like 20 GHz, ground completeness is very important especially for CPW designs. As it can be seen from the layout (Figure 4.9), there are many underpasses for this purpose in the design. External biasing is used to bias the MMIC, therefore there is no DC bias networks included in the design. External biasing is applied using bias-tee connectors combining RF and DC signals at the MMIC port. Bias-tee has DC blocking capacitors preventing the DC current flows to the RF path.

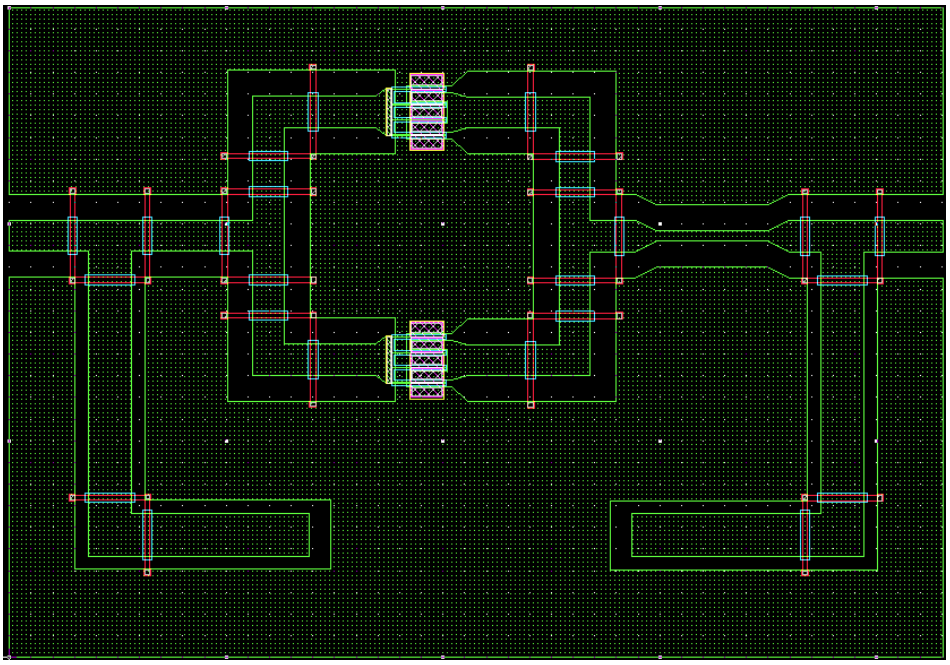

Figure 4.9: ADS layout of the designed GaN MMIC Power Amplifier (PA) with COPLAN elements

S-parameter and harmonic balance optimizations are performed in order to obtain maximum output power while having reasonable small-signal gain. Small-signal and harmonic balance simulation results can be seen in Figure 4.10 and Figure 4.11 respectively.

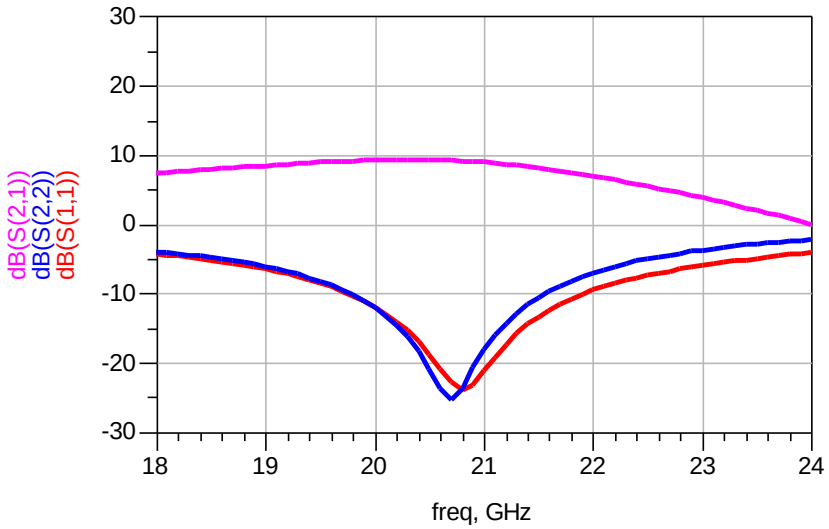

Figure 4.10: S-parameter simulation results of the designed 20 GHz GaN MMIC PA

According to simulation results, GaN MMIC has 9.2 dB small signal gain at 20.1 GHz and 29.1 dBm output power at 2.3 dB compression. Next, photo-mask of the GaN MMIC is designed.

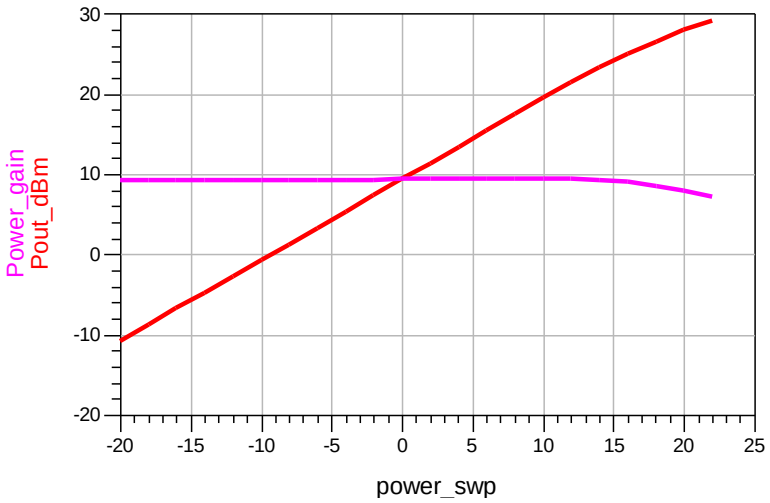

Figure 4.11: Large signal simulation results of the designed 20 GHz GaN MMIC PA

Figure 4.12 shows the photomask which consists of the 20 GHz MMICs and test elements such as capacitors, transistors and inductors. Finally fabrication process of the MMIC was started by using this photomask. Fabrication steps are same with HEMT process steps.

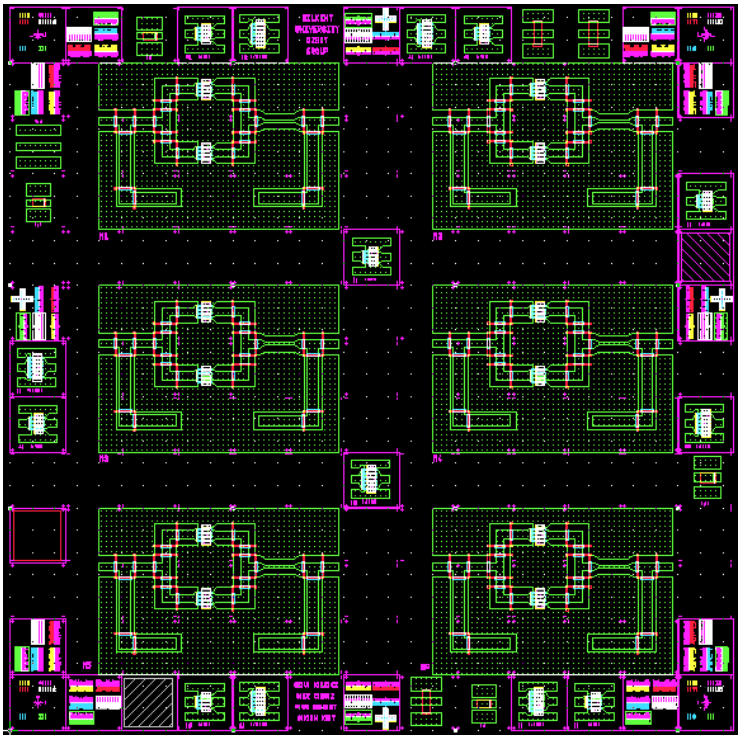

Figure 4.12: Photo-mask including 20 GHz GaN MMICs

After fabrication of GaN MMIC finished, small signal and large-signal measurements were performed. Figure 4.13 shows a photo of the finished MMIC on a chip.

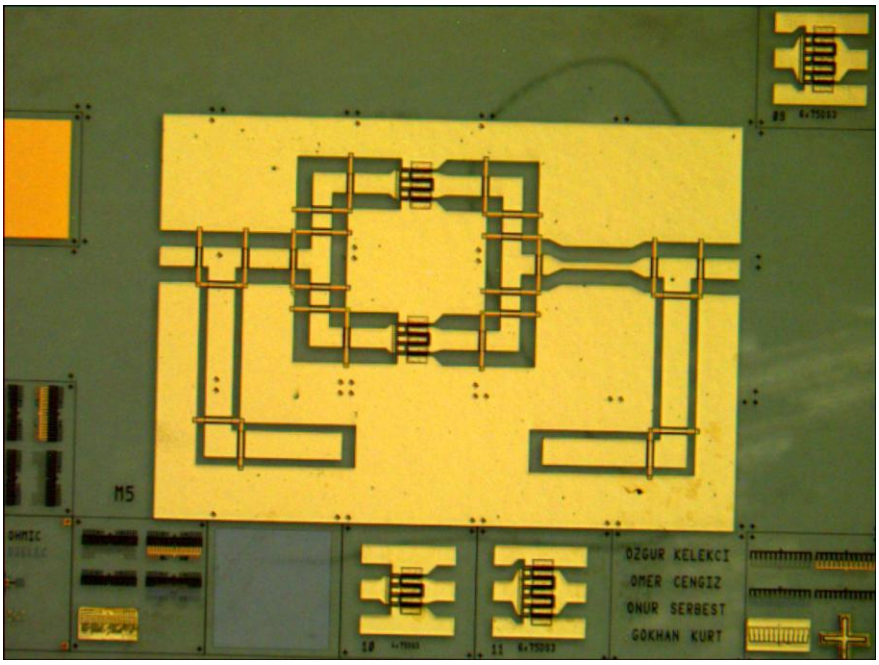

Figure 4.13: MMIC photo on a fabricated chip taken at Bilkent NANOTAM

S parameter measurement results can be seen in Figure 4.14. According to results there is a frequency shift caused by a small mismatch between the model and fabricated transistor. GaN MMIC has 9 dB small signal gain at 19.2 GHz and 6.3 dB at 20.1 GHz. It has still significant small signal gain at desired frequency.

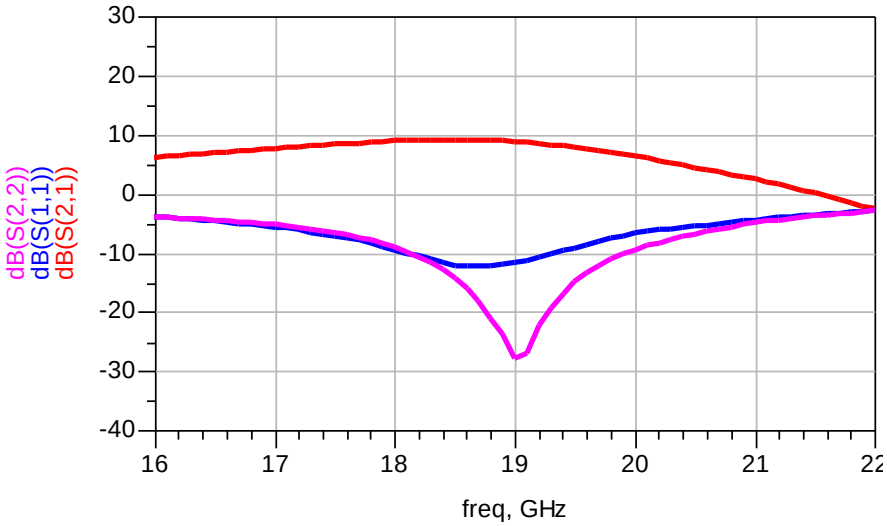

Figure 4.14: S parameter measurement results of the fabricated GaN MMIC

Figure 4.15 shows the large signal measurement results of the fabricated GaN MMIC. According to measurement results, 27.8 dBm output power obtained at 2.7 dB compression point. Measured results are still satisfying results in contrast with having a frequency shift between designed and fabricated MMIC.

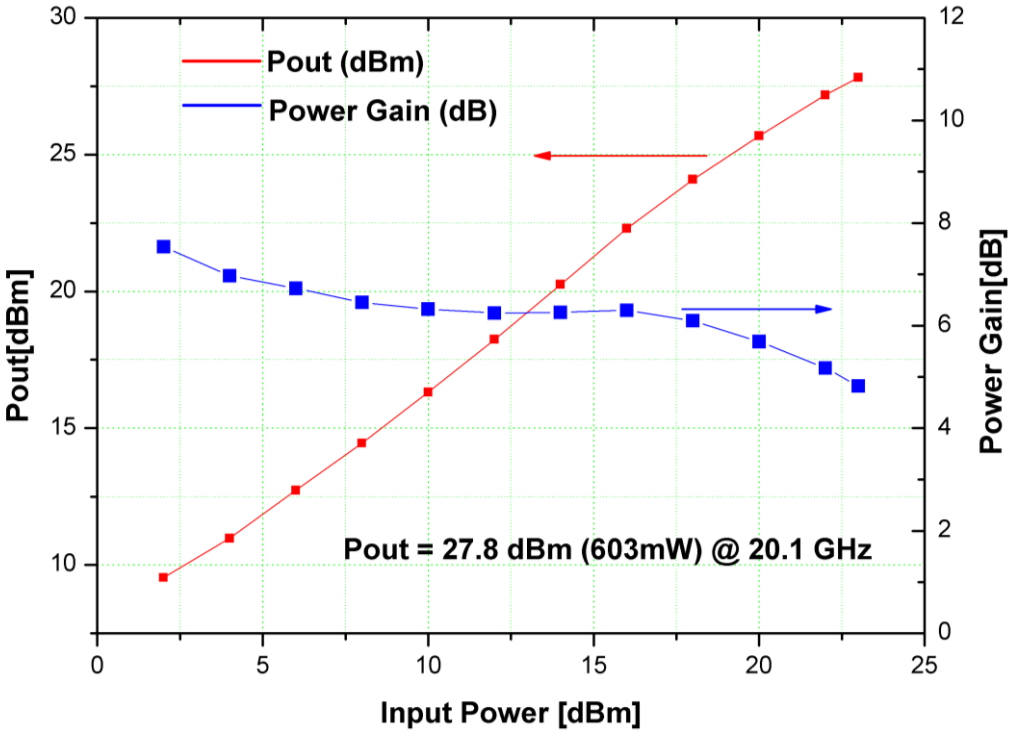

Figure 4.15: Large signal measurement results of the fabricated GaN MMIC

4.2 5 GHz CPW GaN MMIC PA Design

Second GaN MMIC PA was designed at 5 GHz. Design steps are the same with the first designed GaN MMIC PA. Firstly, optimum impedances of 6x150 µm transistor was determined via load-pull and source pull simulations. Next, matching networks of the GaN MMIC were designed by using Smith Chart tool in ADS and GaN MMIC were designed with ideal lumped elements. After this step, ideal elements were replaced with COPLAN elements. Figure 4.16 shows the ADS schematic of 5 GHz MMIC design with COPLAN elements.

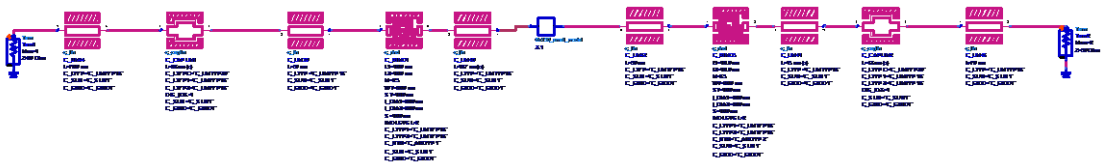

Figure 4.16: ADS schematic of 5 GHz GaN MMIC PA with COPLAN elements

L-C low-pass branch networks were used for input and output matching networks as shown in Figure 4.17.

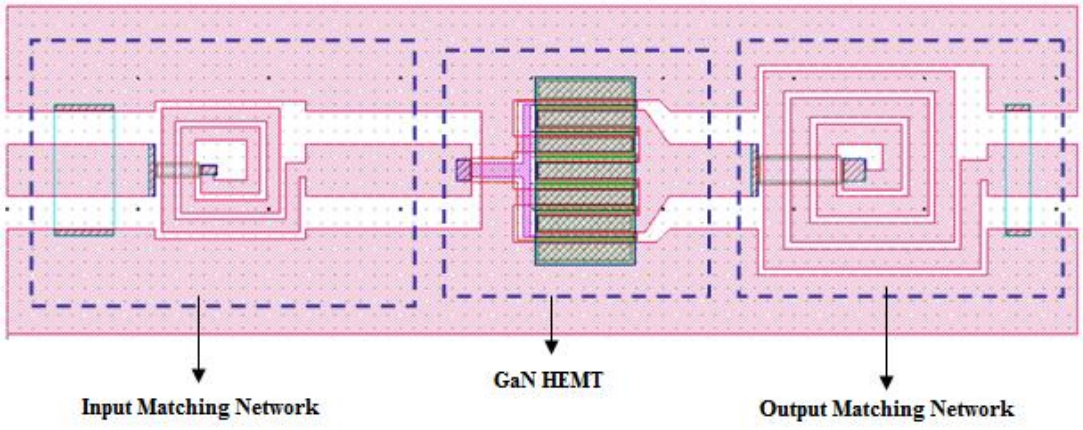

Figure 4.17: Layout of 5 GHz GaN MMIC PA with COPLAN elements

S parameter simulation results can be seen in Figure 4.18. Figure 4.19 shows the photomask of this 5 GHz GaN MMIC PA.

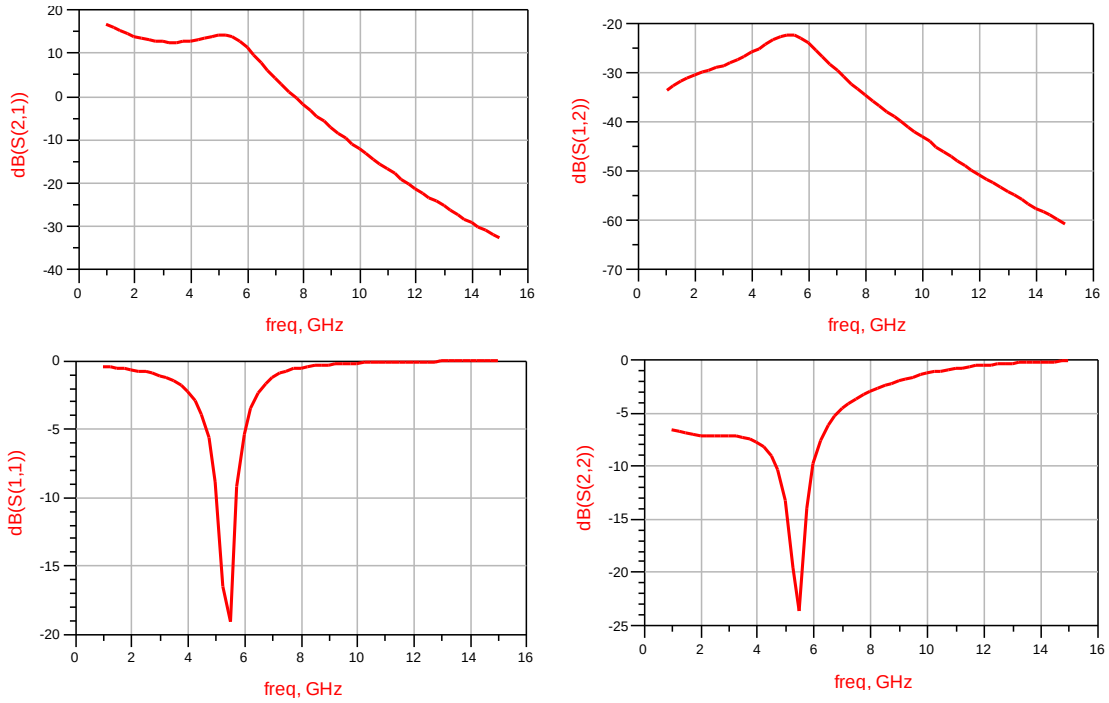

Figure 4.18: S parameter simulation results of 5 GHz GaN MMIC PA with COPLAN elements

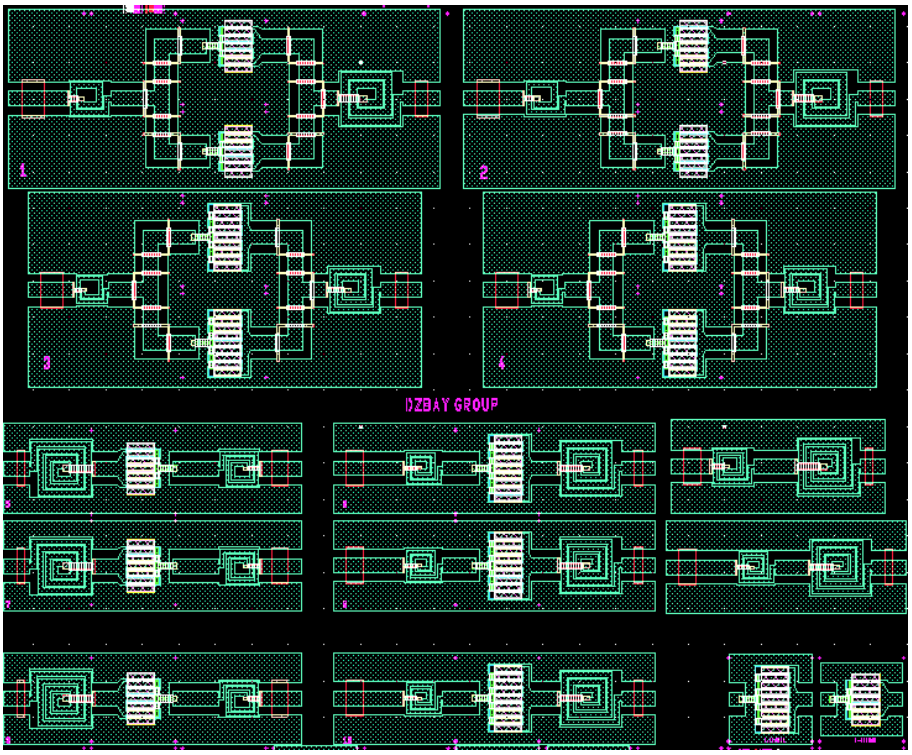

Figure 4.19: Photo-mask of the designed GaN MMIC PAs

After the fabrication of GaN MMIC chip by using the photo-mask shown in Figure 4.19, small signal and large signal measurements were performed. Figure 4.20 shows a photo of a fabricated MMIC chip and Figure 4.21 shows the comparison between small signal measurement and simulation results. According to results, measurement and simulation results fit quite well.

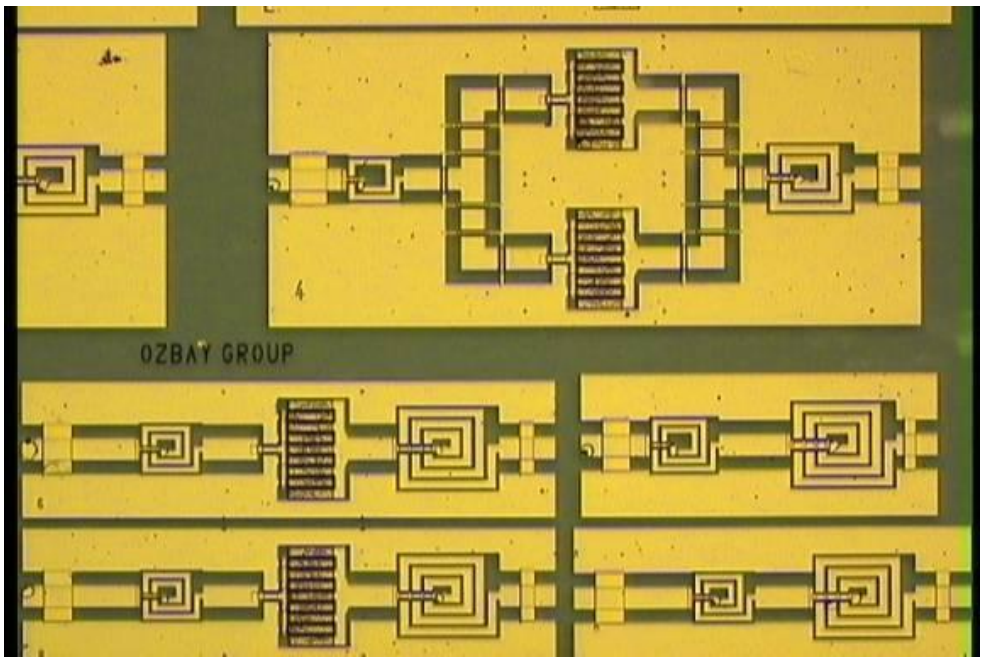

Figure 4.20: MMIC photo on a fabricated chip taken at Bilkent NANOTAM

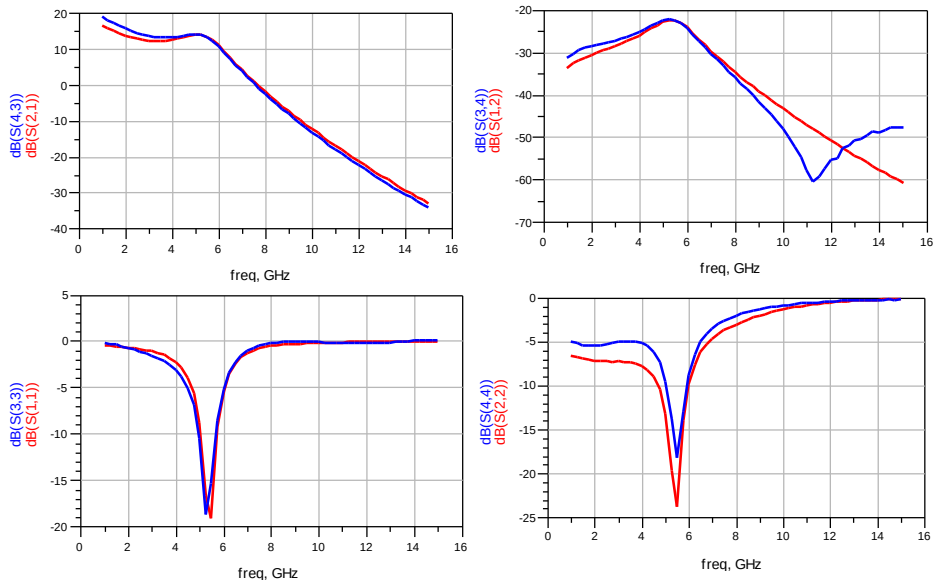

Figure 4.21: Comparison between small signal simulation (red) and measurement (blue) results for 5 GHz GaN MMIC

Figure 4.22 shows the large signal measurements of the GaN MMIC performed at 5.26 GHz with pulsed bias voltage to prevent the overheating of the GaN MMIC. According to measurement results, GaN MMIC has a 2.7W output power at 2.5 dB compression point. This result is quite impressive.

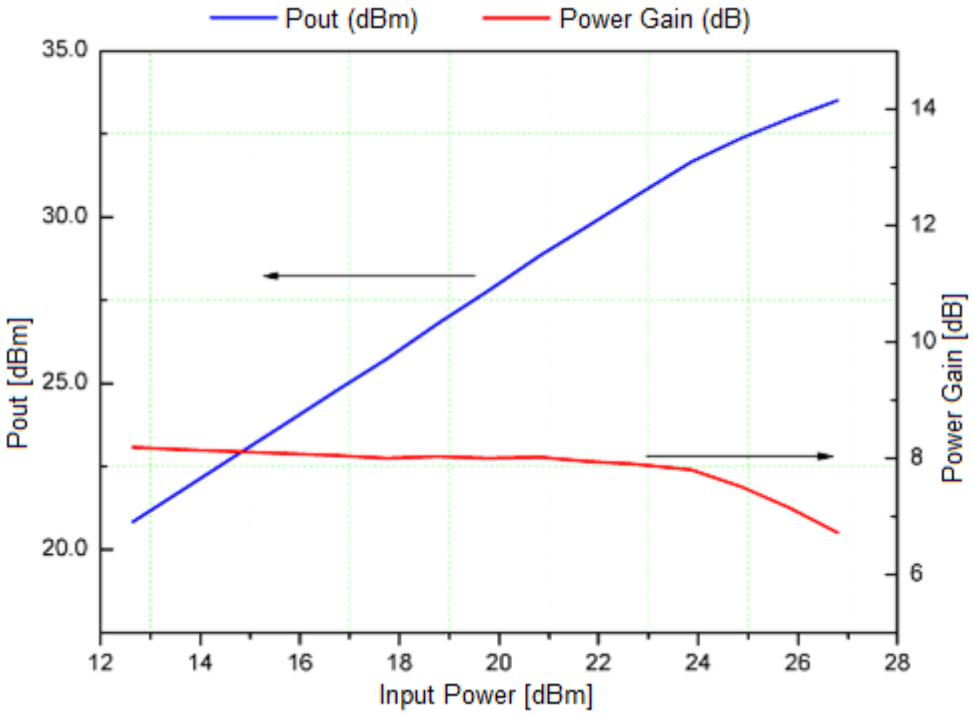

Figure 4.22: Large signal measurement results for 5 GHz GaN MMIC

Figure 4.23 shows a comparison between a fabricated and simulated capacitor used in the 5 GHz MMIC design. According to comparison, our capacitor model is very accurate.

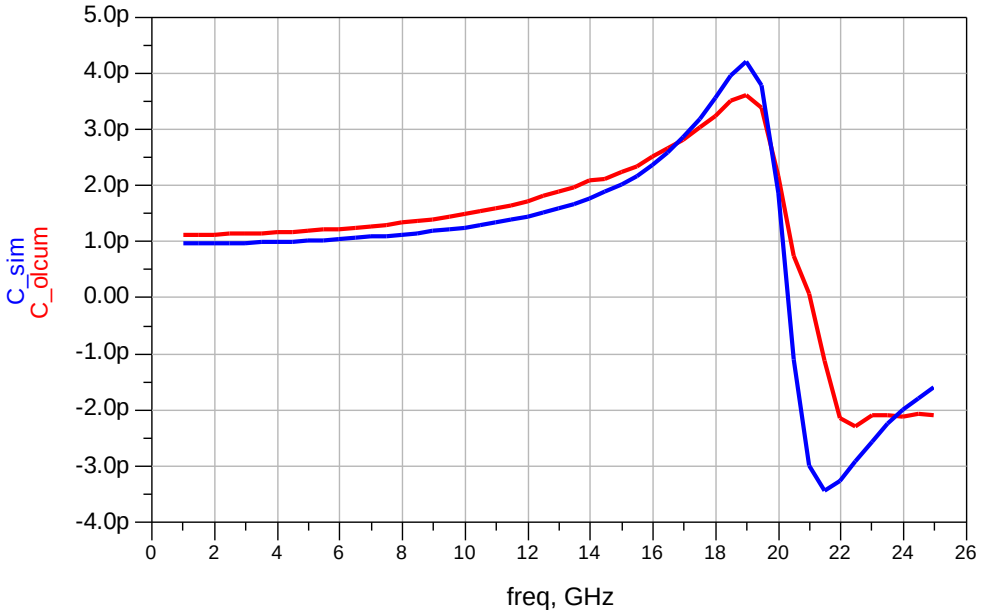

Figure 4.23: Comparison between measurement (red) and model (blue) of a MIM capacitor used in 5 GHz MMIC design.

5. S BAND HIGH POWER GAN MMIC POWER AMPLIFIER DESIGN FOR WIMAX APPLICATIONS

In this part GaN based two different MMIC designs for WiMAX applications will be presented. Agilent Advanced Design System (ADS) is used for design simulations and analyzes. MMICs were designed by using Cree GaN HEMT design kit named Cree_GaN_Design_Kit_v1.101a. Typical HEMT RF performances at 3.5 GHz for this design kit are:

- 4.5 W/mm power density
- 14 dB small signal gain
- High output impedance
- Low input capacitance
- 65% PAE
- 28 volt drain operation

Design goals are minimum 30W output power, 14 dB small signal gain with gain ripple lower than 0.5 dB and maximum -15 dB input return loss in the 3.3-3.7 GHz frequency range.

5.1 3.5 GHz GaN MMIC Power Amplifier Design

First GaN MMIC is designed with ideal lumped passive elements with 8x500 μm Cree transistor and second MMIC is its equivalent circuit with transmission lines and real passive elements.

Π type resonance circuits used to match the input and output impedance of the 8x500 μm transistor to 50 ohm. Circuit schematic can be seen in Figure 5.1. This kind of matching circuit gives the opportunity of bandwidth flatness over the desired frequency.

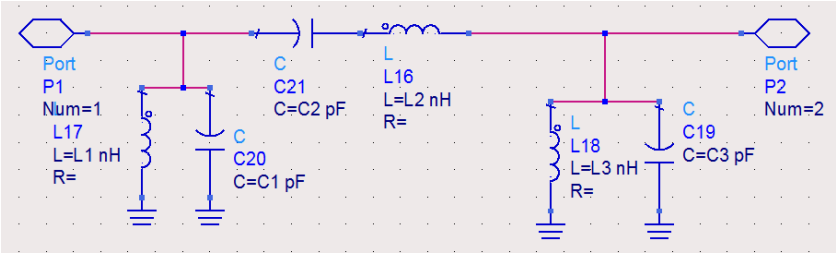

Figure 5.1: General schematic of input and output matching circuits

8x500 µm Cree transistor has a stability factor of K=0.5 at 3.5 Ghz and below frequencies. Parallel R-C stability circuit is used at gate port of the transistor to achieve K>1 at all frequencies to prevent any possible oscillation. The designed GaN MMIC circuit with ideal lumped elements and R-C stability circuit is shown in Figure 5.2. Biasing circuit is embedded into the input and output matching circuits which can be seen in Figure 5.2.

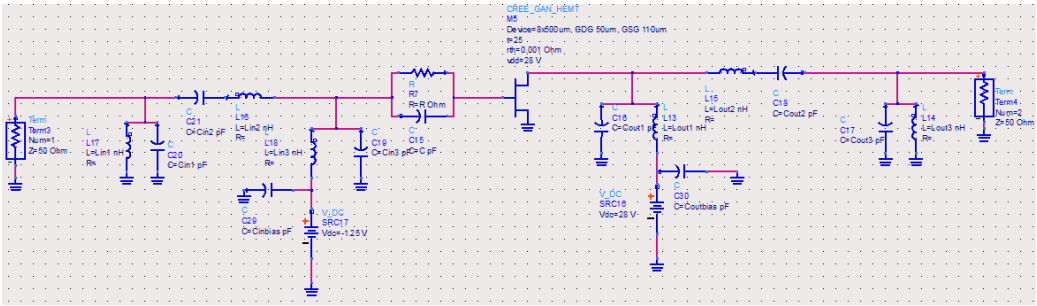

Figure 5.1: ADS schematic of the designed GaN MMIC Power Amplifier (PA) with ideal lumped elements

S parameter simulation results of the designed GaN MMIC are shown in Figure 5.3. The designed GaN MMIC has lower than -14 dB input return loss at 3.5 GHz and 16 dB small signal gain over the 3 GHz- 4GHz frequency band. It has a stability factor K>1 over 0.5 GHz- 10 GHz frequency band as seen in Figure 5.4.

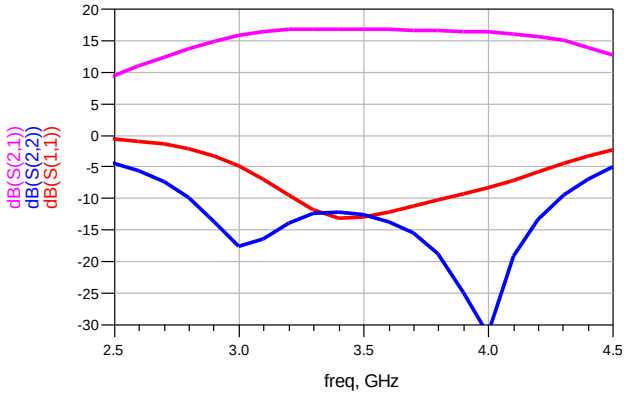

Figure 5.2: S parameter simulation results of the designed GaN MMIC PA with ideal lumped elements.

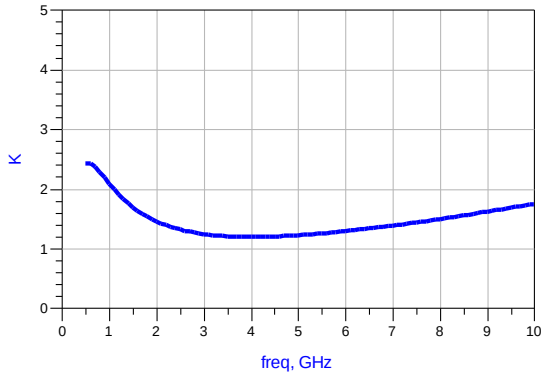

Figure 5.3: Stability factor of the designed GaN MMIC PA with ideal lumped elements.

Large signal simulation results are shown in Figure 5.5. According to results GaN MMIC has a P1dB=42.2 dBm, P3dB=43.9 dBm and 65% PAE.

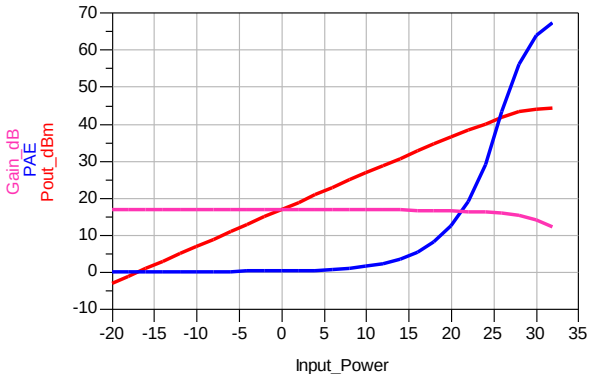

Figure 5.4: Large signal simulation results of the designed GaN MMIC PA with ideal lumped elements

After obtaining the design goals with ideal lumped elements, the equivalent circuit with transmission lines and real passive elements is built. ADS schematic of the designed GaN MMIC PA is shown in Figure 5.6 and the ADS layout of that MMIC is shown in Figure 5.7.

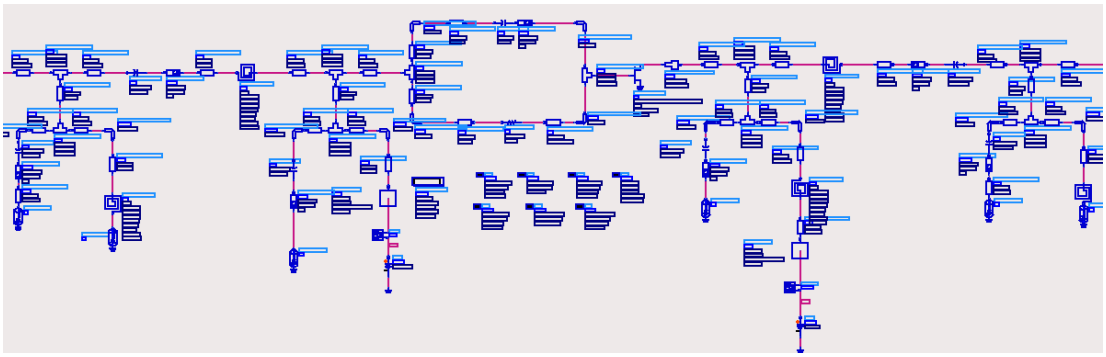

Figure 5.5: ADS schematic of the designed GaN MMIC PA

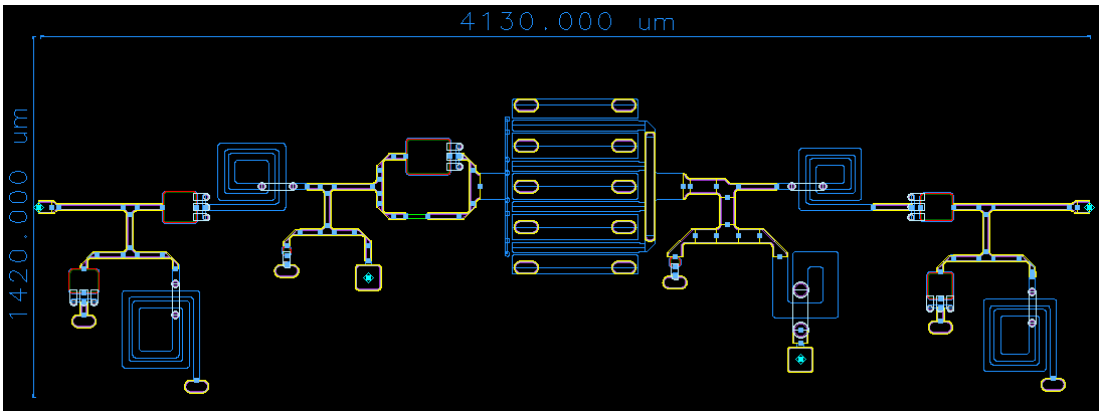

Figure 5.6: Circuit layout of the designed GaN MMIC PA

S parameter results can be seen in Figure 5.8. The designed GaN MMIC has 16 dB small signal gain over the 3.2 GHz- 3.8 GHz frequency band and -13.5 dB input return loss.

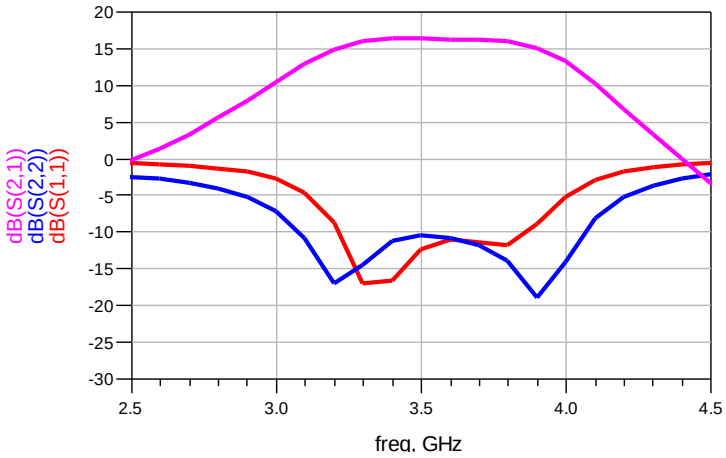

Figure 5.7: S parameter simulation results of the designed GaN MMIC PA

The designed GaN MMIC PA is unconditionally stable in 0.5 GHz- 10 GHz frequency range as seen in Figure 5.9.

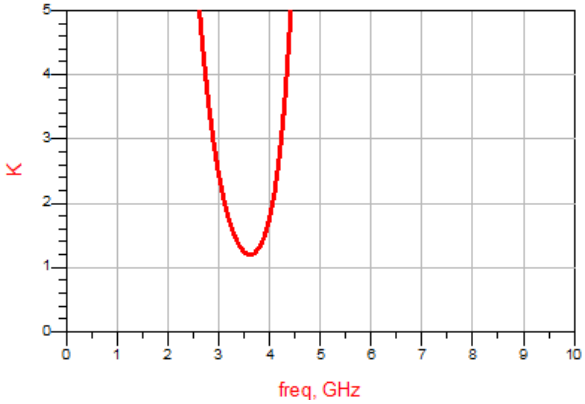

Figure 5.8: Stability factor of the designed GaN MMIC PA

According to large signal simulation results as seen in Figure 5.10, the designed GaN MMIC has P1dB=41.6 dBm, P3dB=42.6 dBm and 55%PAE.

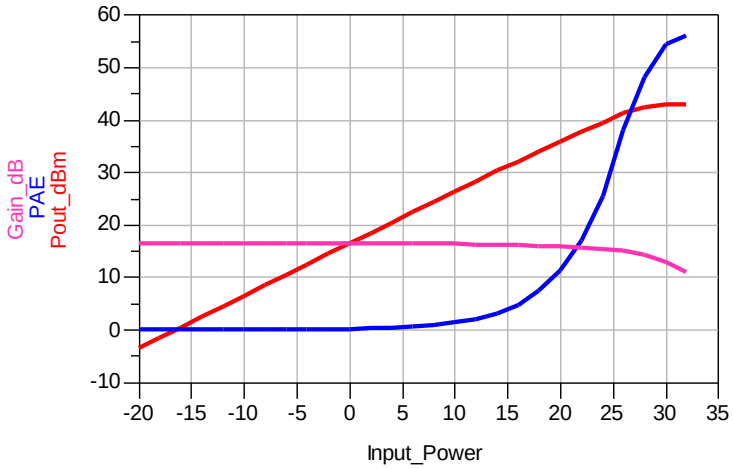

Figure 5.9: Large signal simulation results of the designed GaN MMIC PA

We then combined two of the GaN MMICs with monolithic Lange couplers to increase its output power. First of all a coupler was designed to achieve the operation at 3.3 to 3.7 GHz with Cree process parameters. According to design results, the designed coupler has a length of 8.9 mm. Due to high cost of valuable Cree GaN wafer, it is not reasonable to manufacture such large area couplers as on-wafer. Therefore, it is decided to design and manufacture the couplers as off-chip. Lange couplers were designed by using Teflon PCB parameters. Layout of the Lange coupler which is designed by using Teflon PCB parameters is shown in Figure 5.11 and its s-parameter simulation results is shown in Figure 5.12.

Figure 5.10: Lange Coupler designed with Teflon PCB parameters @3.5 GHz

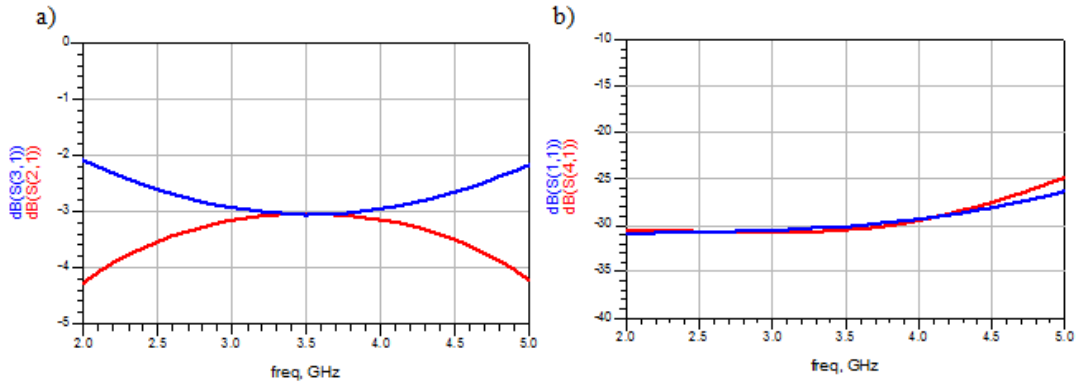

Figure 5.11: S parameter simulation results of the designed Lange Coupler with Teflon PCB parameters

A block diagram of the designed GaN MMIC PA is shown in Figure 5.13.

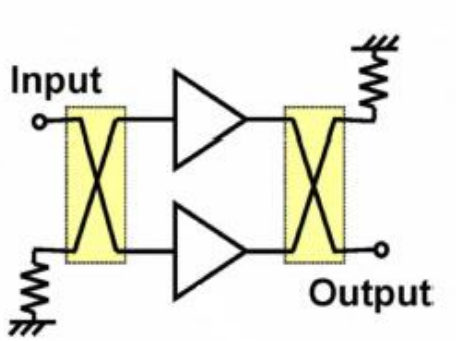

Figure 5.12: Block diagram of the designed GaN MMIC PA

S parameter and stability factor simulation results of the complete design can be seen in Figure 5.14 and Figure 5.15 respectively. The designed GaN MMIC is unconditionally stable in the 0.5-10 GHz frequency range as seen in Figure 5.15.

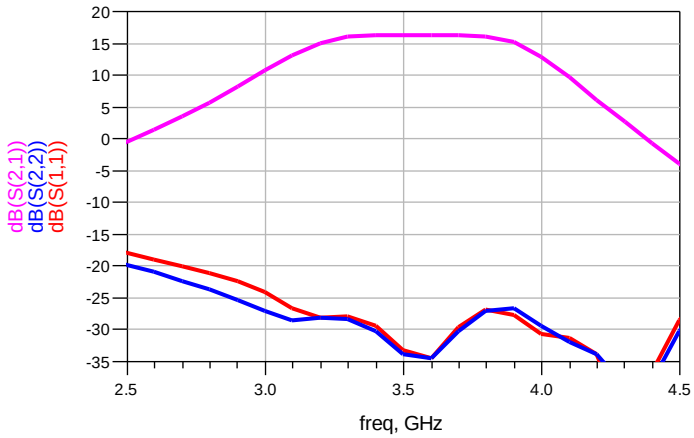

Figure 5.13: S parameter simulation results of the complete GaN MMIC PA with Lange couplers

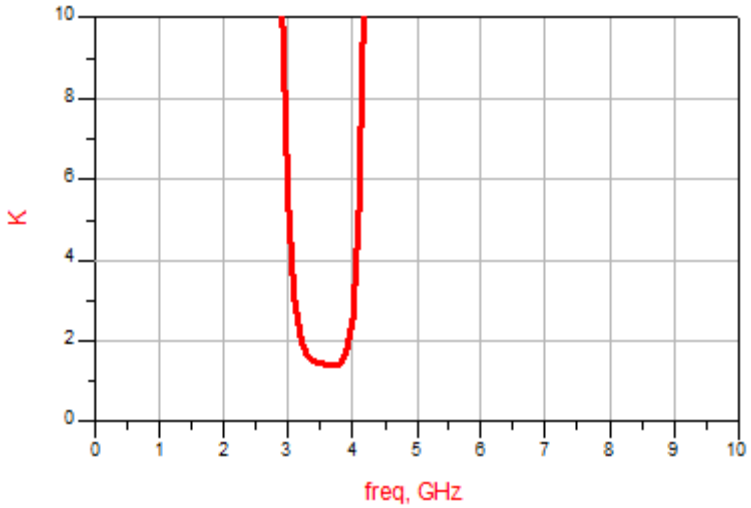

Figure 5.14: Stability factor of the complete GaN MMIC PA with Lange couplers

The complete GaN MMIC PA has a P1dB=44.9dBm, P3dB=45.3 dBm and 45%PAE at 3.5 Ghz as seen at Figure 5.16.

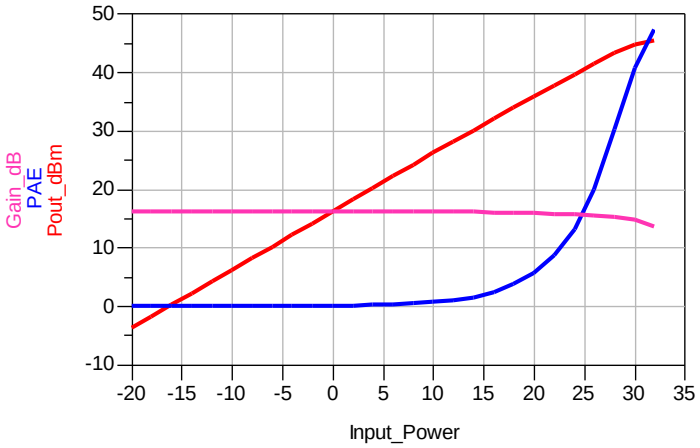

Figure 5.15: Large signal simulation results of the complete GaN MMIC PA with Lange couplers.

Table 5.1 shows the achieved performance results versus design goals.

Table 5.2: Performance summary of the designed GaN MMIC PA

	Goals	Achievements	
Frequency (GHz)	3.3-3.7	3.3-3.8	
Pout	30W (44.7 dBm)	P1dB	30.9W (44.9 dBm)
		P3dB	34W (45.3dBm)
Gain	14 dB	15.9 dB – 16.1 dB	
Gain Ripple	0.5	0.2 dB	
Input Return Loss	< -15 dB	<-20dB	

6. CONCLUSION AND FUTURE WORK

During this work, GaN HEMT technology is mentioned starting from the design considerations, micro fabrication process and characterization steps of the transistors and continues with detailed large signal nonlinear modeling steps. Then, two CPW GaN MMIC PA design works are explained and after simulation and measurement results of these PAs are given. Finally, our GaN MMIC design experiences are applied to design two S band high power GaN MMIC PAs for WiMAX applications. Simulation results of these PAs are illustrated. In the second design, two of these GaN MMICs combined with Lange Couplers to increase the output power of the PA. Due to high cost of valuable Cree GaN wafer, Lange couplers designed and manufactured as off-chip by using Teflon PCB parameters. These results are very promising results for future works.

As a future work, our own design kit based on GaN HEMT technology can be improved further by applying temperature dependant large-signal nonlinear modeling to our fabricated transistors. Moreover, reliability of our transistors should be investigated and mean time to failure (MTTF) times of our transistors should be calculated to build more accurate GaN MMIC PAs.

7. REFERENCES

[1] **Price, R. W.,** 2004. *Roadmap to Entrepreneurial Success*. AMACOM Div American Mgmt Assn. p. 42. New York, USA.

[2] **Mimura, T.,** 2002. The Early History of the High Electron Mobility Transistor (HEMT), *IEEE Trans. on Microwave Theory and Techniques*, March, Vol. **50**, No. 3, pp. 780-782.

[3] **Johnson E. O.,** 1965. Physical limitation on frequency and power parameters of transistors, *RCA Rev.,* Jun pp. 163–176.

[4] **Mishra, U. K., Shen, L., Kazior, T. E., and Wu, Y.-F.,** 2008. GaN-Based RF Power Devices and Amplifiers, *Proceedings of the IEEE*, *vol. **96**, no. 2*, February pp. 287 - 305.

[5] **Khan, M. A., Kuznia, J.N., Olson, D.T., Schaff, W.J., Burm, J.W., and Shur, M.S.,** 1994. Microwave performance of a 0.25μm gate AlGaN/GaN heterostructure field effect transistor, *Appl. Phys. Lett.*, 29 August Vol. **65**, No. 9, pp. 1121-1123.

[6] **Url-1** <http://www.topas.imst.de/Topas/en/home.php>, accessed at 01.07.2009.

[7] **Url-2** <http://www.agilent.com/find/eesof-ads>, accessed at 01.07.2009.

[8] **Palacios, T., Dora, Y. , Chakraborty, A., Sanabria, C., Keller, S., DenBaars, S. P., and Mishra, U. K. ,** 2006. Optimization of AlGaN/GaN HEMTs for high frequency operation *Physica Status Solidi (a)*, Vol. **203**, No. 7, pp. 1845-1850.

[9] **Oprins, H., Das, J., Ruythooren, W., Vandersmissen, R., Vandevelde, B., and Germain, M.,** 2005. Thermal Modeling of Multifinger AlGaN/GaN HEMTs, Belgirate-Italy.

[10]**Freeman, J. C.,** 2004. Channel Temperature Model for Microwave AlGaN/GaN HEMTs on SiC and Sapphire MMICs in High Power, High Efficiency SSPAs, *International Microwave Symposium*, Fort Worth, Texas, June 6–11.

[11] **Vertiatchikh A.V., and Eastman, L.F.,** 2003. Effect of drain-to-source spacing AIGaN/GaN transistor on frequency response and breakdown characteristics, *Electronic Letters*, 29th May, Vol. **39** No. 11.

[12] **Lee, J.W., Kumar, V., and Adesida, I.,** 2006. High-Power-Density 0.25_m Gate-Length AlGaN/GaN High-Electron-Mobility Transistors on Semi-Insulating 6H–SiC Substrates, *Japanese Journal of Applied Physics* Vol.**45**, No.1A, pp.13-17.

[13] **Shen, L., Buttari, D., Heikman, S., Chini, A., Coffie, R., McCarthy, L., Chakraborty, A., Keller, S., DenSaars, S. P., and Mishra, U. K.,** 2004. Improved high power thick-GaN-capped AlGaN/GaN HEMTs without surface passivation, *62nd Device Research Conference*, 23 June, Vol. **1**, pp. 39-40.

[14] **Ohki, T., Kikkawa, T., Kanamura, M., Imanishi, K. , Makiyama, K. , Okamoto, N. , Joshin, K., and Hara, N.,** 2009. An over 100 W AlGaN/GaN enhancement-mode HEMT power amplifier with piezoelectric-induced cap structure, *Phys. Status Solidi C*, Vol. **6,** June, pp. 1365-1368.

[15] **Tan, W. S., Houston, P. A. , Parbrook, P. J., Hill, G. , and Airey, R. J.,**2000. Comparison of different surface passivation dielectric in AlGaN/GaN heterostructure field-effect transistor, *J. Phys. D: Appl. Phys.*,Vol. **35**, pp. 595-598.

[16] **Harrison, I., Clayton, W., and Jeffs, W.,** 2001. High temperature RF characterization of SiN passivated and unpassivated AlGaN/GaN HFETs, *Phys. Stat. Solidi (a)*, Vol. **188**, pp. 275-278.

[17] **Prunty, T. R. , Smart, J. A. , Chumbes, E. M. , Ridley, B. K. , Eastman, L. F. , and Shealy, J. R. ,** 2000. Passivation of AlGaN/GaN heterostructures with silicon nitride for insulated gate transistors, *in Proc. of the IEEE / Cornell High-Performance Devices Conference. IEEE*, pp. 208–214.

[18] **Vetury, R. , Zhang, N. Q., Keller, S., andMishra, U. K. ,** 2001. The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs, *IEEE Trans. on El. Devices*, March, Vol. **48**, No. 3, pp. 560–566.

[19] **Binari, S. C., Ikossi, K., Roussos, J. A. , Kruppa, W. , Park, D., Dietrich, H. B. , Koleske, D. D. , Wickenden, A. E. , and Henry, R. L.,** 2001. Trapping effects and microwave power performance in AlGaN/GaN HEMTs, *IEEE Trans. on El. Devices*, March, Vol. **48**, pp. 465–471.

[20] **Ludwig, R., Bretchko, P.,** 2000. *RF Circuit Design: Theory and Applications*, p.606, Prentice Hall, 2000.

[21] **Gupta, M. S.,** 1992. Power Gain in Feedback Amplifiers, a Classic Revisited, *IEEE Trans. MW Theory and Techniques*, Vol. **40**, No. 5, pp. 864-879.

[22] **Filicori, F. , Ghione, G. , and Naldi, C. U.,** 1992. Physics-Based Electron Device Modelling and Computer-Aided MMIC Design, IEEE *Trans. MW Theory and Techniques*, July, Vol. **40**, No. 7.

[23] **Snowden, C. M.,** 1997. Characterization and Modelling of Microwave and Millimeter-Wave Large-Signal Device-Circuit Interaction Based on Electro-Thermal Physical Models, *IEEE MTT-S Digest*.

[24] **Benbakhti, B., Rousseau, M., and De Jaeger, J-C.,** 2005. Implementation of an 2D Electro-Thermal Model for Power Semiconductor Devices Simulation: Application on Gallium Nitride, *Proceedings of the COMSOL Multiphysics User's Conference*, Paris.

[25] **Xue, L., Wang, Y., Liu, M., Xiel, C., Li, C., He, Z., and Xial, Y.,** 2005. Numerical Simulation of $Al_xGa_{1-x}N$/AlN/GaN HEMT, *IEEE Conf. on El. Devices and Solid-State Circuits*, 19-21 December, pp. 799-802.

[26]**Morton, C. G. , Atherton, J. S. , Snowden, C. M. , Pollard, R. D., and Howes, M. J.**,1996. A Large-Signal Physical HEMT Model, *IEEE MTT-S Digest*.

[27]**Yin, H., Hou, D., Bilbro, G. L., and Trew, R. J.,** 2008. Harmonic balance simulation of a new physics based model of the AIGaN/GaN HFET, IEEE *MTT-S International MW Symposium Digest*, 15-20 June, pp. 1425-1428.

[28] **Tyagi, R. K., Ahlawat, A., Pandey, M., and Pandey, S.,** 2007. An analytical two -dimensional model for AlGaN/GaN HEMT with polarization effects for high power applications, *Microelectronics Journal*, Vol. **38**, pp. 877–883.

[29] **Kumar, S. P., Agrawal, A., Chaujar, R., Gupta, M., and Gupta, R.S.,** 2008. Analytical modeling and simulation of subthreshold behavior in nanoscale dual material gate AlGaN/GaN HEMT, Superlattices and Microstructures, Vol. **44**, pp. 37–53.

[30] **Huq H. F., and Islam, S. K.,** 2007. DC Characterization and Validation of the Improved Analytical Model of AlGaN/GaN HEMT, IEEE *Region 5 Technical Conference*, April 20-21, Fayetteville, AR.

[31] **Wu, S., Webster, R. T., and Anwar, A. F. M.,** 1999. Physics-Based Intrinsic Model for AlGaN/GaN HEMTs, *MRS Internet J. Nitride Semiconductor*, Res. 4S1, G6.58.

[32] **Root, D. E., Fan, S., and Meyer, J.,** 1991. Technology Independent Large Signal FETs Models: A Measurement-Based Approach to Active Device Modeling, *Proceedings of 15th ARMMS Conference*.

[33] **Fernandez-Barciela, M., Tasker, P. J., Demmler, M., Campos-Roca, Y., Massler, H., Sanchez, E., Curras-Francos, C., and Schlechtweg, M.,** 1997. Simplified Nonquasi-Static FET Modeling Approach Experimentally Validated up to 118.5GHz, MTT-S International Microwave Symposium Digest, pp. 1499-1502.

[34] **Corbella, I., Legido, J. M., and Naval, G.,** 1992. lnstantaneous Model of a MESFET for use in Linear and Nonlinear Circuit Simulations, *IEEE Trans. Microwave Theory Tech*, July, Vol. **40**, No. 7, pp. 1410-1421..

[35] **Follmann, R., Tempel, R., Sporkmann, T., and Wolff, I.,** 1997. A new spline based FET model for MESFETs and HEMTs, *Proc. 27th European Microwave Conf.*, Vol. **2**, No. 27, pp. 1360-1366.

[36] **Cripps, S. C.,** 2006. RF Power Amplifiers for Wireless Communications, 2nd Edition. Artech House, Inc., Norwood, MA.

[37] **Albulet, M.,** 2001. RF Power Amplifiers. Noble Publishing Corporation, Atlanta, GA.

[38] **Albulet, M.,** 2005. RF and Microwave Power Amplifiers Design. McGraw-Hill, New-York, NY.

[39] **Breed, G.,** 2007. There's Nothing Magic About 50 Ohms, *High Frequency Electronics*, June, Vol. **6**, No. 6.

[40] **Url-3** < http://www.microwaves101.com/encyclopedia/why50ohms.cfm>, accessed at 01.08.2009.

[41] **Url-4** <http://www.cree.com>, accessed at 01.07.2009.

CURRICULUM VITAE

Candidate's full name: Ömer CENGİZ

Place and date of birth: BOLU-18 April 1985

Permanent Address: Yaşamkent Mah. 102. Ada 3. Blok No:10 BOLU

Universities and Colleges attended: İstanbul Technical University

Publications:

- **Cengiz, O.,** Kelekçi, O., Arıcan, G.O., Ozbay, E., Palamutçuoğulları, O., 2011. Design of High Power S-Band GaN MMIC Power Amplifiers for WiMAX Applications, *The XXX General Assembly and Scientific Symposium of the International Union of Radio Science (Union Radio Scientifique Internationale-URSI),* 13-20 August, İstanbul,Turkey.