İSTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

TRACK-HOLD AMPLIFIER AND MULTIPLYING DIGITAL TO ANALOG CONVERTER (MDAC) DEDICATED TO 10 BIT 8x100MS/s TIME INTERLEAVED PIPELINE ADC

M.Sc. Thesis by

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Department : Electronics and Communication Engineering

Programme : Electronics Engineering

JUNE 2008

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Assoc. Prof.Dr. Shahram MINAEI (Dogus Uni.)

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

8x100MS/s 10 BİT ZAMAN ARALIKLI PIPELINE ANALOG SAYISAL ÇEVİRİCİDE KULLANILMAK ÜZERE TASARLANMIŞ İZLEME-TUTMA DEVRESİ VE ÇARPICI DİJİTAL ANALOG ÇEVİRİCİ (MDAC)

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ABBREVATIONS

ADC	: Analog to Digital Converter
DAC	: Digital to Analog Converter
THA	: Track and Hold Amplifier
SEF	: Switched Emitter Follower
OPAMP	: Operational Amplifier
OTA	: Operational Transconductance Amplifier
MDAC	: Multiplying Digital to Analog Converter
SFDR	: Spurious Free Dynamic Range
THD	: Total Harmonic Distortion
SNDR	: Signal to Noise and Distortion Ratio
LSB	: Least Significant Bit
DC	: Direct Current
PSRR	: Power Supply Rejection Ratio
CMFB	: Common Mode Feedback
ENOB	: Effective Number of Bits
SiGe	: Silicon Germanium
BiCMOS	: Bipolar and Complementary Metal Oxide Semiconductor
SR	: Slew Rate
EF	: Emitter Follower
TI	: Time Interleaved

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LIST OF SYMBOLS

$C_{be\text{-}Qi}$	: Base emitter capacitance of the i^{th} transistor
$V_{BE\text{-}Qi}$	: Base emitter voltage of the i^{th} transistor
Z_{Qi}	: Output impedance of the i^{th} transistor
C_{Hold}	: Hold capacitance
I_{SEF}	: SEF's tail current
C_{S1}, C_{S2}, C_{S3}	: Sampling capacitances
C_F	: Feedback capacitance
V_{IN}	: Differential input voltage
U_T , V_T	: Thermal voltage
β	: Feedback factor
τ	: Time constant

TRACK-HOLD AMPLIFIER AND MULTIPLYING DIGITAL TO ANALOG CONVERTER (MDAC) DEDICATED TO 10 BIT 8x100MS/s TIME INTERLEAVED PIPELINE ADC

SUMMARY

In the context of an ongoing time interleaved analog to digital converter (ADC) project, this thesis studies the design of two critical blocks of a 10-bit TI ADC with eight 100MS/s channels: A high bandwidth THA and a fast-settling residue amplifier for the first pipeline ADC stage. Both blocks are designed in a 0.18µm SiGe BiCMOS technology. While the pipeline ADCs only uses MOSFETs, the THA uses bipolar transistors to handle the large signal swing and the large hold capacitor needed to keep the noise floor below the 10 bit level.

In the front-end of ADC, track and hold amplifier is employed to relax the ADC's timing requirements. To achieve settling and bandwidth requirements, different linearization techniques are merged. With the designed switched emitter follower THA 10 bit accuracy is achieved under Nyquist condition of 800MS/s.

In the second part of the thesis, a class-AB operational transconductance amplifier (OTA) for the Multiplying-Digital-to-Analog-Converter (MDAC) of the first pipeline stage is designed. The task of the first stage is to resolve 2.5 bits. It is used instead of a class-A OTA in an existing single ADC channel design that has already been successfully implemented and measured. The purpose of this study is to evaluate if replacing the existing class-A OTAs with a class-AB design reduces the power consumption of the MDAC. The performance was tested in a 12 bit 100MS/s ADC and the total conversion error is less than 1 LSB. It is observed that no power is saved compared to class A amplifier.

8x100MS/s 10 BİT ZAMAN ARALIKLI PIPELINE ANALOG SAYISAL ÇEVİRİCİDE KULLANILMAK ÜZERE TASARLANMIŞ İZLEME-TUTMA DEVRESİ VE ÇARPICI DİJİTAL ANALOG ÇEVİRİCİ (MDAC)

ÖZET

Bu çalışmada, halen devam etmekte olan 10 bit 8x100MS/s kanallı zaman aralıklı analog sayısal çevirici (ADC) projesi kapsamında iki önemli blok tasarlandı: Geniş bantlı izleme ve tutma devresi ile ADC'nin ilk katında yer alacak hızlı-oturan artık kuvvetlendirici. Her iki blok için 0.18µm SiGe BiCMOS teknolojisi kullanılmıştır. Pipeline analog sayısal çeviricide sadece MOSFET kullanılırken, izleme tutma devresinde büyük işaret salınımlarını sağlamak için bipolar transistorlar ve gürültü seviyesini 10 bit hassasiyetinden düşük tutmak için ise büyük tutma kapasiteleri kullanılmıştır.

Çeviricinin ön uç devresi olarak, izleme tutma devresinin kullanılması, çeviricinin doğrusallık gereksinimlerini önemli ölçüde azaltmıştır. Oturma zamanı ve bant genişliği gereksinimlerini karşılamak için farklı linearizasyon teknikleri bir arada kullanılmıştır. Anahtarlanmış emetör izleyici yapısı ile tasarlanan izleme tutma devresi, 800MS/s hızında Nyquist kriterinin altındaki frekanslar için 10 bit hassasiyet sunmaktadır.

Çalışmanın ikinci bölümünde, pipeline analog sayısal çeviricinin ilk MDAC katında kullanılmak üzere geçiş iletkenliği kuvvetlendiricisi (OTA) tasarlanmıştır. Çeviricinin ilk kat çözünürlüğü 2.5 bittir. Tasarlanan AB sınıfı kuvvetlendirici daha önce gerçeklenmiş ve ölçümleri yapılmış analog sayısal çeviricideki A sınıfı kuvvetlendiriciye alternatif olarak düşünülmüştür. Çalışmanın bu kısmındaki amaç tasarlanan AB sınıfı OTA'nın varolan A sınıfı OTA'ya göre MDAC katında güç tasarrufu sağlayıp sağlayamayacağıdır. Devrenin performansı 12 bit 100MS/s ADC'de denenmiştir ve benzetim sonuçlarına göre toplam çevrici hatası 1 LSB'den azdır. A sınıfı kuvvetlendirici ile kıyaslandığında güç tasarrufu yapılmadığı gözlenmiştir.

CHAPTER 1: INTRODUCTION

Analog-to-digital converters (ADCs) provide the link between the analog world and digital systems. The performance of the analog-to-digital interface often determines the performance of the whole mixed-signal system. For example, the sampling rates of the ADCs have to track the increasing data rates in (communication) systems, while maintaining the required dynamic range, which can be 9 or more effective bits for some applications (e.g. 10GBASE-T Ethernet).

For resolutions above 9 bits, pipelined ADCs offer a good trade-off between speed, resolution, and power consumption [1]. However, at this resolution, the sampling rate is limited to a few hundred megasamples per second [1] by the relatively complex and high precision processing that each stage has to perform in each clock cycle. Higher sampling rates can be achieved by time-interleaved operation of multiple ADCs. While time-interleaved ADCs (TI ADCs) relax the sample rate in the individual channels by the interleaving factor N, the front-end THA still has work at the overall sampling frequency and have full signal bandwidth.

Time-interleaving can be beneficial even when the sampling rate can be achieved with a single channel. When the sampling rate of a channel gets close to the technological limit, the circuit becomes self loaded and power efficiency drops. Splitting such a channel in two reduces the power consumption. Additionally, the channels can be arranged in pairs in order to share the stage amplifiers between channels working in opposite phase [2].

In the context of an ongoing TI ADC project, this thesis studies the design of two critical blocks of a 10-bit TI ADC with eight 100MS/s channels: A high bandwidth THA and a fast-settling amplifier for the first pipeline ADC stage. Both blocks are designed in a 0.18µm SiGe BiCMOS technology. While the pipeline ADCs only uses MOSFETs, the THA uses bipolar transistors to handle the large signal swing and the large hold capacitor needed to keep the noise floor below the 10 bit level.

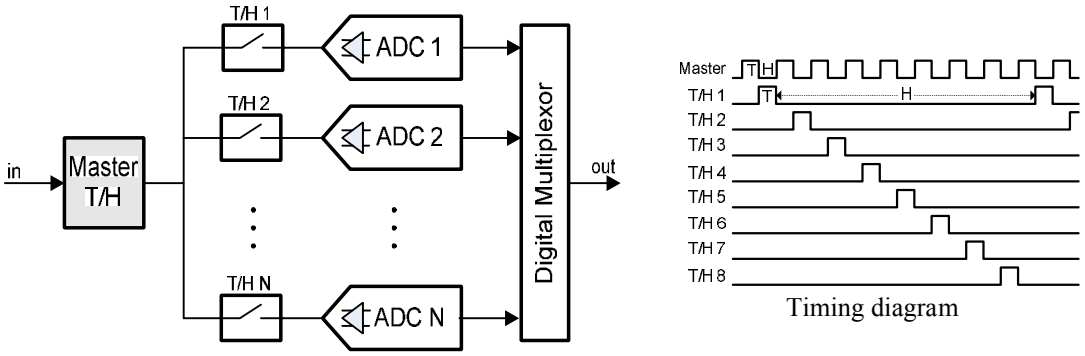


Figure 1.1: TI multi-channel ADC with master-slave THA front-end

The first part of the thesis presents the design of a high bandwidth front-end THA. This THA can be used either as a master THA for a TI ADC as shown in Fig. X, or as a THA for a single channel of the TI ADC. A single channel of the latter configuration could also be used as a sub-sampling ADC with high input bandwidth (for direct down-conversion). Using the presented THA as a master T/H is more suitable because it takes advantage of the fast switching capability of the bipolar switch (switched emitter follower) which comes at the price of large power consumption. As the sampling instants are determined by the edges of a single clock, the master-slave scheme relaxes the skew and jitter requirements for the clock phase generation and distribution, and remove the effect of bandwidth mismatch between the channel front-ends. The slave T/H stages still need high bandwidth in order to acquire the input signal in the short hold period of the master T/H. However, because they do not need to track a high frequency signal but only have to acquire a DC voltage (held by the master THA), simple MOS switches can be used. The signal dependent on-resistance is not a problem as long as the on-resistance is low enough for the step response to settle. The switches can be bootstrapped to obtain low on-resistance with small devices.

In the second part of the thesis, a class-AB OTA for the Multiplying-Digital-to-Analog-Converter (MDAC) of the first pipeline stage is designed. It is used instead of a class-A OTA in an existing single ADC channel design that has already been successfully implemented and measured. The purpose of this study is to evaluate if

replacing the existing class-A OTAs with a class-AB design reduces the power consumption of the MDAC.

CHAPTER 2: TRACK AND HOLD AMPLIFIER

2.1 Introduction to Track and Hold Amplifiers

The track and hold amplifier is used in many activities in data processing systems. For example, it can serve as a presampler in the front end of ADC in order to improve high frequency performance, as a multiplexer in front of time-interleaved ADC channels, or as a deglitcher behind DAC [3].

Sampling circuits are employed in front of the ADC to relax their timing requirements and at the back end of digital to analog converters to suppress the glitches. Until the mid 1980s, the front end circuits were mainly classified into either open loop or closed loop architectures. But recently, open loop topologies are preferred to meet the bandwidth requirements. Thus, recent studies focus on linearization techniques to improve the poor linearity of open loop structures.

In wideband data conversion, the track-and-hold amplifier is mostly used within the ADC or as a separate component preceding it, to condition the signal for acquisition by the converter. The THA' s main function is to sample the input signal at a precise instant and hold the value of the sample constant during the interval required for the ADC to perform the analog to digital conversion (Figure 2.1). This result in signal sampling with a low jitter and it relaxes the ADC's timing requirements.
Since the linearity of the ADC is usually degraded at higher input signal frequencies by slew rate dependent distortion effects, a THA can reduce ADC distortion by providing constant amplitude signals to the ADC during sampling. For this reason, a high linearity, wideband THA can often improve the linearity performance of ADCs in wideband applications such as radar, digital receivers for communications, and sub-sampling for down-conversion. With the continuously increasing demands on speed, design of track and hold becomes more important.

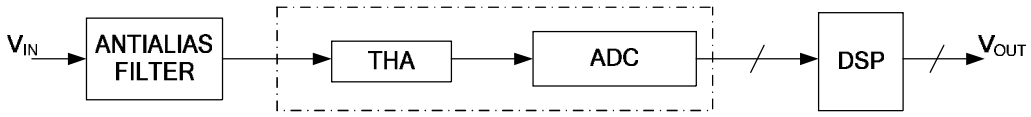
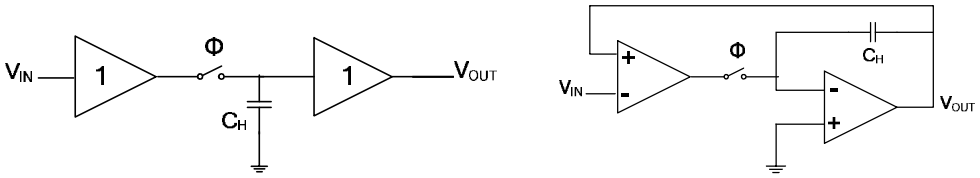


Figure 2.1: Signal Processing System Front End

There are two classical approaches to THA circuits, open loop and closed loop architectures (Figure 2.2). The outstanding features of closed loop THA are high accuracy and the frequency response limitation due to feedback which is necessary for stability. They typically present a dominant design tradeoff of this approach. Thus, to allow high speed operation open loop architecture is employed in this work.



(a) **(b)**

Figure 2.2: Classical open loop THA (a), classical closed loop THA (b)

The two important open loop THA topologies are the diode bridge THA and switched emitter follower THA (SEF). Among open loop topologies, switched emitter follower (SEF) is mostly preferred as the front end of ADC because it achieves lower distortion and higher bandwidth than the diode bridge counterpart. The diode-bridge THA requires relatively higher current to catch the performance of SEF, which in turn will increase power consumption and worsen the switching noise. In addition, SEF has a wider dynamic range because it allows high signal swing [4]. This helps to keep the sampled noise of THA below the quantization noise of ADC.

2.2 Performance Parameters

A switched emitter follower THA can be decomposed into three parts: an input buffer, a switched emitter follower and an output buffer (Figure 2.3). Although the actual circuit is fully differential, for simplicity only one side is shown.

The operation of the track and hold circuit shown in Figure 2.3 is as follows: During the track phase, all three stages behave like level shifters and transfer the input signal to the output. When track signal (T) is high, Q_S is forward biased and the output

tracks the input signal with a constant delay for a single input tone. During the hold phase (H), Q_S is turned off by steering the tail current to resistor load of input pair which pulls down the base voltage of Q_S. Since Q_S is not conducting, the charge on the hold capacitance is isolated and hold capacitance serves as a voltage source which has a value of the input signal at the sampled instant. The sampled data is supplied to following circuitry via output buffer.

The performance of THA is degraded by clock jitter and amplitude errors. The nonlinearity in track and hold phases are caused by different mechanisms. In the following section 2.3, the design of the circuit will be explained with the remedies for nonlinearity. But before going into details of design, performance metrics will be mentioned to clarify the causes of nonlinearity.

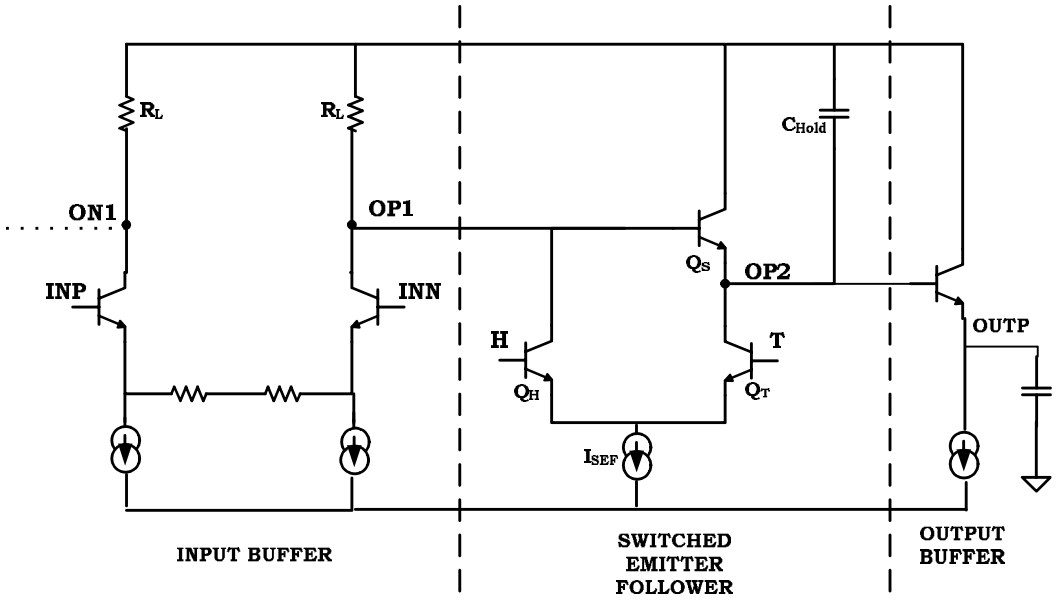


Figure 2.3: Switched emitter follower THA

2.2.1 Dynamic Range

Dynamic range of a system or device is the signal power interval at the output limited by noise floor from bottom and linearity specifications from top. It is usually expressed in dB. In a data conversion system, it means, within the dynamic range, neither output gets lost due to noise nor it exceeds the range of the ADC input. As can be seen in Figure 2.4, increasing the input signal power help dynamic range to enlarge until it becomes limited by distortion.

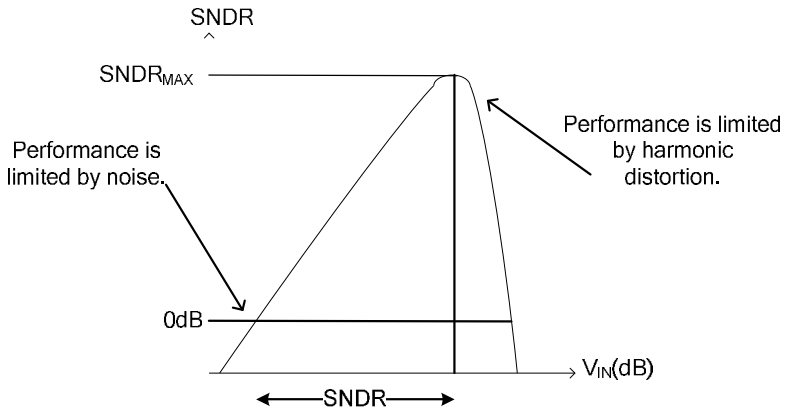


Figure 2.4: SNDR vs. input signal level

2.2.2 Pedestal Error

During the transition from track to hold mode, a non-zero time interval exists for which switching transistors Q_H and Q_T are on simultaneously (Figure 2.3). In this time interval, the input signal through base-emitter capacitance of switched emitter follower Q_S, and the clock signal through the base-collector capacitance of Q_T will create a charge offset on hold capacitance which is called pedestal error. Another contribution to pedestal error will come from tail current of SEF via Q_5. The total charge error is given in Expression (2.1) [5].

$$\Delta q = \int_{t_H}^{t_H+\tau} \frac{V_{OP1}(t) - V_{be,QS}(t)}{Z_{QT}(t)} dt + I_{SEF}\tau + V_{CLK}C_{bc,QT} \qquad \textbf{(2.1)}$$

All the terms in Expression (2.1) are related to input signal. The first term contains the input signal itself. In the second term the time interval τ, during which both switch transistors are conducting, depends on the base voltage of Q_S and the third term contains the nonlinear C_{bc-QT} capacitance which has a dependence on the collector voltage of Q_S. Since the influence of input signal on the amplitude error is not linear, it is not easy to get rid of it. One of the solutions is reducing τ, which can be done by increasing switching signal's steepness. However, this will add switching noise. So making a compromise between these effects, a swing of 300mV is used as V_{CLK}.

2.2.3 Hold Mode Feedthrough

Hold-mode feedthrough occurs in the switching stage, due to coupling through the base-emitter capacitance of the switched emitter follower Q_8. Without any precaution, input signal is added up with a gain given in Equation (2.2) upon sampled value in the hold mode and this causes degradation in the spurious free dynamic range. To cancel the feedthrough to the first order, cross-coupled feed-forward capacitances are added [3]. This method will be mentioned more in detail in the design part.

$$A_{fthr} = \frac{C_{be,QS}}{C_{be,QS} + C_{Hold}} \tag{2.2}$$

2.2.4 Droop Rate

During the hold mode, the hold capacitances are discharged by the base current of the output buffers; this results in voltage droop of sampled value.

2.3 Design of SEF Track and Hold Amplifier

In this work, fully differential signaling is used to reduce the even order terms in the frequency spectrum of output. But practically, we cannot eliminate the even order harmonics totally, due to mismatch. Moreover, the pole at the switch emitter follower stage depends on the transconductance and hold capacitance, and it varies with the operation point. Due to large signal swing, the cut off frequency of two sides will be different and this asymmetrical filtering causes even harmonics to grow.

As mentioned before, switched emitter follower can be decomposed into three parts, input buffer, switching stage and output buffer. In the following sections, the design of each part will be examined.

2.3.1 Input Buffer

In the SEF architecture, since the switching stage destroys the input signal during hold period, it is not possible to use it without an input buffer. This fact will be stated more clearly in the following paragraphs.

The analysis of the input buffer, which is a common emitter differential amplifier, reveals that the nonlinearity of this stage is mainly due to large voltage swing ($1.5V_{PP}$ differential), which is necessary for the noise considerations. This makes it necessary to use linearization techniques. The emitter degeneration, commonly employed, intuitively, introduces negative feedback, which lowers the gain and extends the amplifier's linear operating region to a voltage range nearly equal to $R_E I_E$ [6]. But to achieve the desired linearity performance the inclusion of emitter degeneration resistors is not sufficient. Therefore, a second technique is employed which is based on cross coupling a second differential pair which has a lower gain and higher distortion compared to main pair as shown in Figure 2.5. When the main pair (Q_1, Q_2, R_{E1}) and the secondary pair (Q_3, Q_4, R_{E2}) are cross coupled, at the price of gain reduction, a wider output range that meets the linearity requirements is obtained.

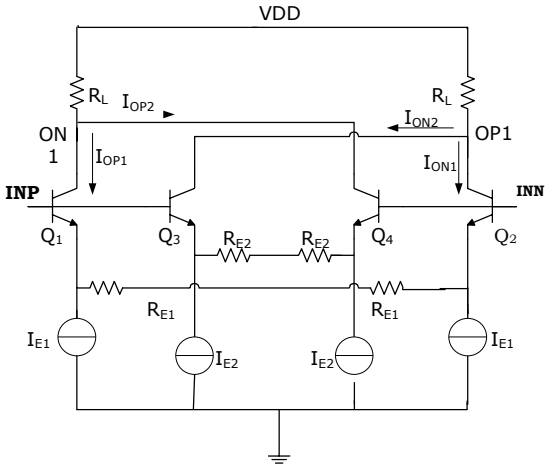


Figure 2.5: Cross coupled input buffer

The large signal analysis of one pair yields:

$$\Delta V_{IN} = U_T \ln\left(\frac{I_{E1} + \frac{\Delta I_O}{2}}{I_{E1} - \frac{\Delta I_O}{2}}\right) + R_{E1} \cdot \Delta I_O \qquad \textbf{(2.3)}$$

where $\Delta I_O = I_{OP1} - I_{ON1}$. Due to logarithmic V-I relationship of bipolar transistors, $I_O = f(V_{IN})$ can't be obtained analytically, but with series inversion method differential output current can be represented as an infinite power series;

$$\Delta I_O = \left(\frac{4I_{E1}}{U_T + 4I_{E1}R_{E1}} \right) V_{IN} - \left(\frac{4I_{E1}}{U_T + 4I_{E1}R_{E1}} \right)^4 \frac{U_T}{8I_{E1}^3} V_{IN}^{\ 3} + \ldots \qquad \textbf{(2.4)}$$

No further terms of the series are given because the main contribution to distortion comes from the third harmonic. V_{IN} vs. V_{OUT} of the two pairs individually and the combined cross-coupled pairs are shown in Figure 2.6.

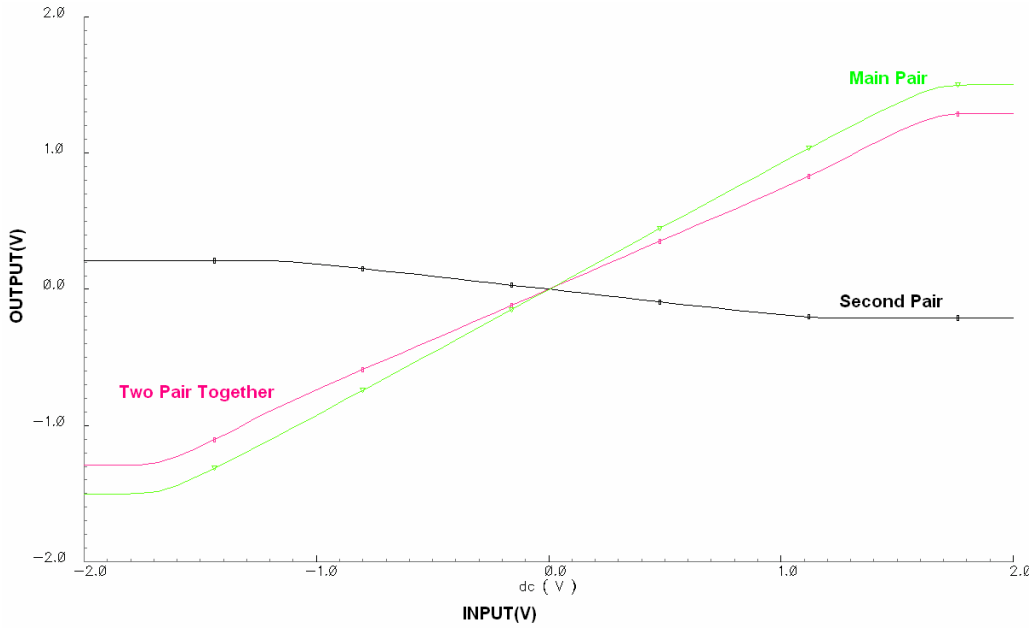


Figure 2.6: Input-output voltage curves of the main amplifier, the second amplifier and the cross-coupled amplifier

In the cross coupled pair the output current will be summed up and under the approximation of $U_T << 4 * I_E * R_E$, the differential output signal is simplified into Expression (2.5). While the existence of the second pair makes it possible to cancel out the third harmonic, the transconductance gets lower correlated to the emitter degeneration resistance of the second pair. After designing the first differential pair according to gain, bandwidth and voltage swing requirements, the compromise between gain and total harmonic distortion will set the second pair's current and emitter degeneration resistance.

$$\Delta I_O = \left(\frac{1}{R_{E1}} - \frac{1}{R_{E2}} \right) V_{IN} - \left[\left(\frac{1}{R_{E1}} \right)^4 \frac{U_T}{8I_{E1}^3} - \left(\frac{1}{R_{E2}} \right)^4 \frac{U_T}{8I_{E2}^3} \right] V_{IN}^{\ 3} + \ldots \qquad \textbf{(2.5)}$$

Usually THA circuits are designed with a gain of 1, which yields $R_L*g_m=1$. The transconductance of an emitter degenerated pair is given $g_m' = g_m / (1 + g_m R_E)$ with small signal approximation. This brings the first condition $\frac{g_m}{1+g_m R_E} R_L \cong \frac{R_L}{R_E} = 1$.

Secondly, to supply the full swing without turning off the transistors completely, there should be a margin between $2*R_L*I_{E1}$ product and the desired voltage swing, $2V_{PP}$. Thirdly, the cutoff frequency $\frac{1}{2\pi R_L C_{be}}$ should be close to the input signal bandwidth to limit the noise of excessive bandwidth before it is down converted to interested bandwidth.

Taking into consideration of non-constant base emitter capacitance of the switch, a few multiple of maximum input frequency which is 500MHz, is used to estimate the load resistance. Then, according to gain requirement, emitter degeneration resistance is chosen equal to load resistance and the current is chosen such that the transistors are switching %75 of the total tail current in order to limit distortion.

The tail current and emitter resistance of the second pair will define the gain reduction and dynamic range of the input stage. With the fulfillment of the condition given in Equation (2.6), the third harmonic can be reduced significantly. Although using a large R_{E2} seems advantageous for minimum gain reduction, the linear region of the second pair I_E*R_E gets smaller for the same SFDR specification. Five multiples of R_{E1} is chosen for R_{E2} based on the parametric analysis of R_{E2} and I_{E2}, to satisfy the linearity requirement for $1V_{PP}$ input signal.

$$\frac{I_{O1}}{I_{O2}} = \left(\frac{R_{E2}}{R_{E1}} \right)^{4/3} \qquad \textbf{(2.6)}$$

The derivatives of transconductance of each pair individually and of the combined pairs versus input signal are shown in Figure 2.7. With the inclusion of the second pair, total harmonic distortion improves nearly 13dB for the price of a gain reduction of 2.5dB. The resistance and current values are given in Table 2.1.

Table 2.1: The current and resistance values of the input pair

I_{E1}	I_{E2}	R_{E1}	R_{E2}	R_L
1mA	140µA	760Ω	3.6kΩ	760Ω

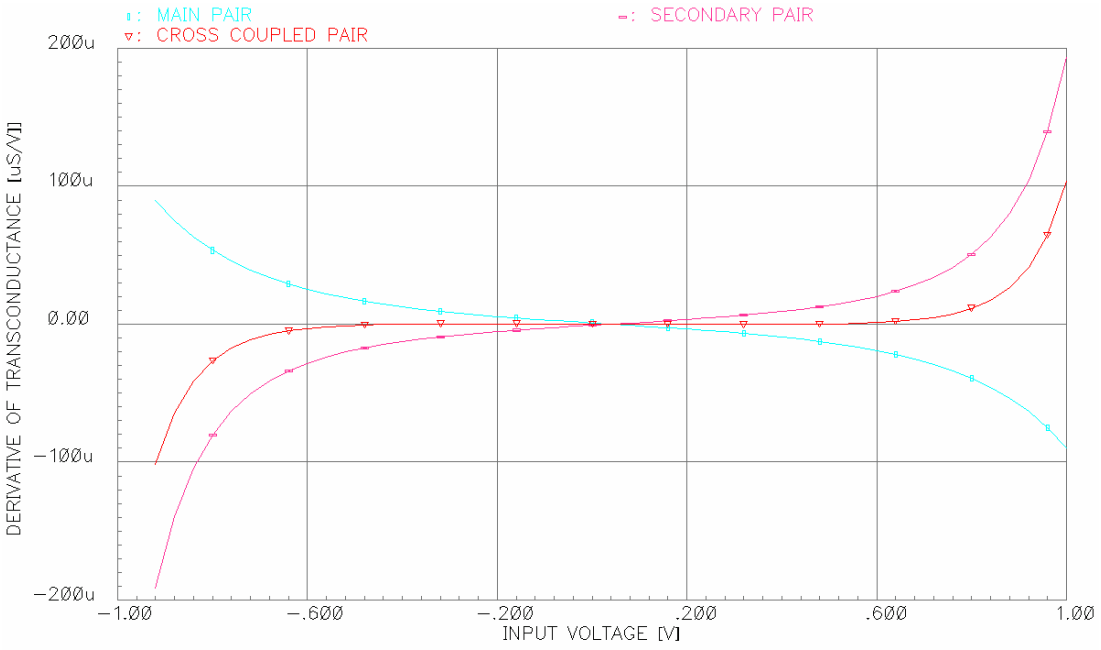


Figure 2.7: Derivative of transconductance [µS/V] vs. input voltage [V]

2.3.2 Switched Emitter Follower

In SEF topology there are two important poles which can be analyzed from the small signal equivalent circuit, which is shown in Figure 2.8; one at the output node of input buffer and one at the output of switched emitter follower. The time constants are given in Equation (2.7). C_{in} is the equivalent capacitance at node O1.

$$\tau_1 = \left[\left(R_{O,IB} \,//\, R_L \right) + r_{bb2} \right] C_{in} \qquad \textbf{(2.7a)}$$

$$\tau_2 = \frac{C_{Hold}}{g_{m,QS}} \qquad \textbf{(2.7b)}$$

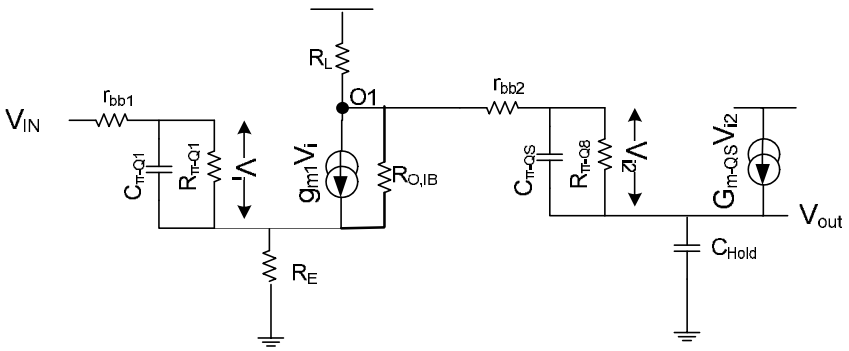


Figure 2.8: Small signal equivalent circuit of input buffer and switched emitter follower in track mode

During the track mode, the switching stage bypasses the signal and it can be examined like an RC circuit whose time constant is τ_2. The time domain step response of a single pole system with time constant τ is:

$$V_o = V_{of}(1 - e^{-t/\tau}) \tag{2.8}$$

The relative error ε is the difference between V_o and V_{of} normalized to V_{of} is:

$$|\varepsilon| = \frac{V_o - V_{of}}{V_{of}} = 2^{-N} \tag{2.9}$$

For 10 bit accuracy settling time is:

$$t_{SET} = N\tau \ln 2 = 10\tau \ln 2 \approx 7\tau \tag{2.10}$$

The settling time of $7\tau_2$ according to Equation (2.10) is much less than the holding time and the main nonlinearity issue turns into slewing limitation, and transconductance or base-emitter voltage modulation due to large signal swing. The voltage swing at a single output node of SEF has $0.75V_{pp}$. At this node, the hold capacitance (1pF) is charged with I_{SEF} and slew rate is equal to

$$SR = I_{SEF} / C_{Hold} \tag{2.11}$$

The constant current will produce a linearly increasing output on the hold capacitance. Maximum input frequency is given as 500MHz and not to be a subject

to slew limitation at this frequency, the condition in Expression (2.12) should be satisfied.

$$\left.\frac{dV_O}{dt}\right|_{MAX} = \left[\frac{0.75}{2}\cos(2\pi f_{in} t)\right]\Bigg|_{MAX} = 2\pi 0.375 f_{in,max} < SR \qquad \textbf{(2.12)}$$

According to condition 2.12, as long as the tail current is higher than 1.18mA, the output signal will not be slew limited. But the variation of base emitter voltage of Q_S will cause distortion.

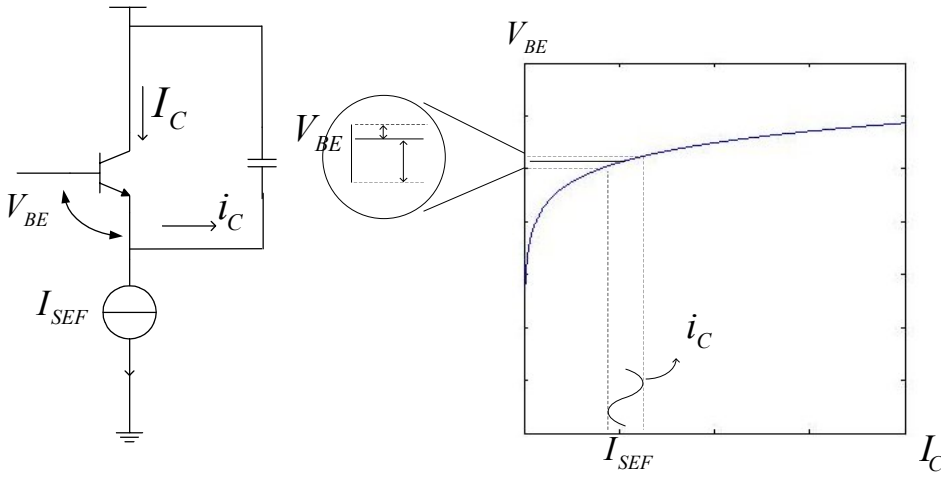


Figure 2.9: Collector current vs. base emitter voltage of the switching transistor

In Figure 2.9, the base emitter voltage vs. the collector current of the switching transistor is shown. The base emitter voltage of the bipolar is changing according to sink/source current of hold capacitance and as the input signal frequency increases, the ratio of the sink/source current of the hold capacitor to DC tail current increases. From Figure 2.9, it can be observed that while the current source is discharging the capacitor V_{BE} variation is larger than the one while the transistor is charging the capacitor. The base emitter voltage of Q_S will swing around tail current according to,

$$V_{BE}(I_C(t)) = V_T \ln\left(\frac{I_{SEF}}{I_S}\right) + \frac{V_T}{I_{SEF}} i_C(t) - \frac{V_T}{2I_{SEF}^{\,2}} i_C(t)^2 + \frac{V_T}{6I_{SEF}^{\,3}} i_C(t)^3 + \ldots \qquad \textbf{(2.13)}$$

where $I_C = I_{SEF} + i_C$ and $i_C = C_H 0.375\cos(2\pi f_{in} t)$. The amplitude of sink/source current is 1.18mA at 500MHz. The higher collector DC current is supplied, the less base emitter voltage variation will occur. Thus the tail current I_{SEF} should be higher

than 10mA, to keep the third harmonic of V_{BE} roughly 65dB below the DC value of V_{BE} and to achieve 10 bit accuracy.

In the hold mode, the SEF tail current, which flows through the load resistance to turn off switched emitter follower, causes additional voltage drop at the output common mode of the input pair. If input pair transistors enter into saturation deeply, in track mode they won't be able to catch the input signal at high frequencies and they will transfer a highly distorted signal into emitter follower where slewing and switching distortion will be added. This reduces the operation frequency extremely. To avoid that, Q_H is splitted into two transistors Q_{Ha} and Q_{Hb} as shown in Figure 2.11(a) to steer only a part of the tail current to the load resistance. The amount of this current should be chosen such that it shouldn't bring input pair transistors into saturation and it should be able to turn off Q_S during hold mode. Although DC drop of this node prevents Q_S to conduct, the output of input buffer will continue to track the input signal with a lower common mode. Thus the leakage of input signal through the base emitter junction capacitance of Q_S causes feedthrough during hold mode. Connecting feed-forward capacitors presented in Figure 2.10 between OP1-ON2 and ON1-OP2 is the most common method to reduce feedthrough. These capacitors will pump charge with the opposite sign of that charge pumped by the emitter follower's base-emitter capacitance. The new hold mode feedthrough will be;

$$A_{ftrh} = \frac{C_{be,QS}}{C_{be,QS} + C_H}\left(1 - \frac{C_{FF}}{C_{be,QS}}\right) \qquad \textbf{(2.14)}$$

When the diode capacitances are equal to $C_{be,QS}$, the second term in Equation (2.14) is cancelled out and first order feedthrough is suppressed. C_{FF} is constructed by paralleling two pairs of back to back diodes [3]. Instead of using a single diode connected transistor, four transistors are employed. Because the two back to back connected transistors will always stay off as long as one of the transistors doesn't break down and each of them shows the base emitter capacitance of switching transistor. Two parallel branches make the total capacitance equal to one C_{be}.

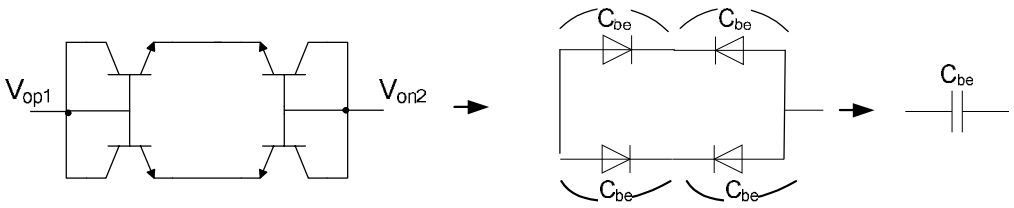
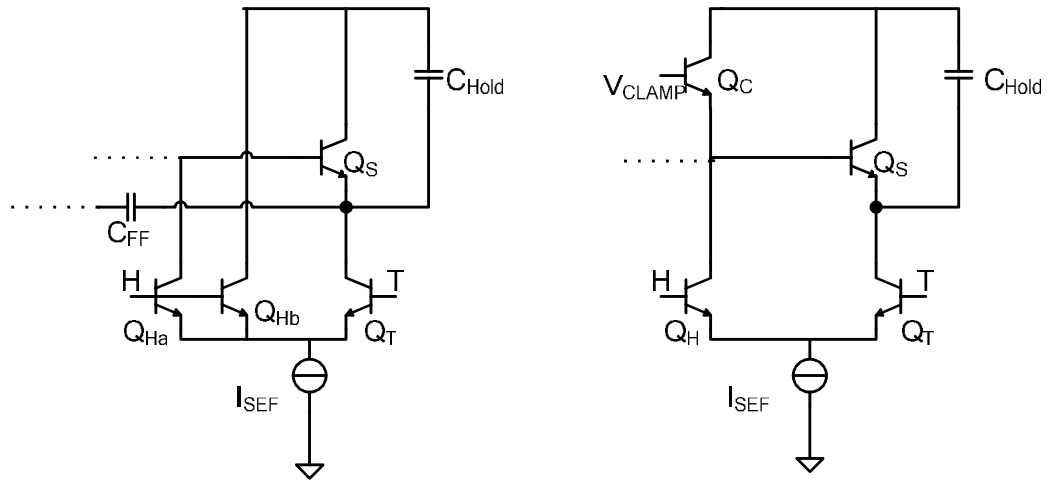


Figure 2.10: Feedforward capacitance used for feedthrough cancellation

The feedforward capacitances are composed of junction capacitances and strongly dependent on the terminal voltages. Therefore, although adding feedforward capacitances suppress the feedthrough significantly, they won't be sufficient for entire cancellation. Choosing C_{Hold} comparably bigger than C_{be} is also necessary to achieve a good feed- through isolation. The large tail current is required to drive the hold capacitance at the desired speed.



(a) **(b)**

Figure 2.11: Switching stage with current splitting: SEF1 (a), switching stage with clamp transistor: SEF2 (b)

In Figure 2.11(b), the second SEF design is shown. The solution to isolate hold capacitance without aggravating the performance of input pair, is clamping the voltage gain of input pair during hold mode by turning on Q_C. When H goes high, the SEF tail current will flow through Q_C and the impedance at nodes OP1 and ON1 gets lower. The voltage swing will decrease and the modulation of base-emitter capacitance of Q7 is prevented. Therefore the feed forward capacitances can be

removed. This will also helps to speed up the circuit since the load capacitance of input pair is decreased. Bias of clamping transistor is one difficulty, but according to simulation results, a variation of ±0.2 V in the base voltage of Q_C worsens THD less than 1dB.

2.3.3 Output Buffer

The output buffer isolates the hold capacitor from the load of THA and provides current driving ability for the THA to drive the subsequent circuitry. A bipolar emitter follower is sufficient in terms of speed and power-saving as an output buffer to drive the load capacitance (2pF) at 100MHz sampling frequency. Although the input frequency bandwidth requirement is 500MHz, the output buffer speed restriction comes from the sampling frequency. It is helpful to emphasize that the bandwidth requirement in the switching stage is based on input signal bandwidth and high current is necessary to avoid the distortion from V_{BE} modulation during track mode. But the output buffer can use the following ADC's sampling period to settle and the time limitation is to settle until the instant that converter samples.

Using an emitter follower as output buffer has the disadvantage that during hold mode, the hold capacitor is the charge across the hold capacitances are discharged due to the base current of the output buffers; this results in common-mode voltage droop. By injecting equal amount of base current to this node (OP2 and ON2), via a replica of output buffer (Figure 2.12) the charge of the hold capacitances are kept constant at the cost of increased power consumption [4].

Alternative output buffer is the CMOS version of emitter follower, source follower which doesn't cause voltage droop. By taking the advantage of triple well process, body effect on n-channel MOSFET is eliminated. Thus, source follower is preferred as the output buffer.

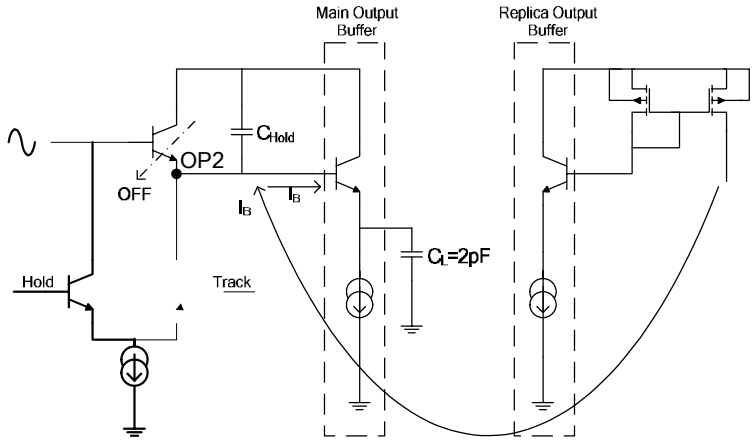


Figure 2.12: EF output buffer

2.4 Simulation Results

The current consumption in each stage is given in Table 2.2 and the supply voltage is 4.5V. Total power consumption of THA is 165mW with the source follower output buffer and 190mW with the emitter follower output buffers. The difference is because of the replica output buffer which is used to avoid voltage droop caused by the base current of EF. The current sources of buffers are separated from that of switching stage, to avoid the switching noise contribution.

Table 2.2: The current consumption of each part in THA

Input Buffer		SEF		Output Buffer	
1st Pair	2nd Pair	Current Splitting (SEF1)	Clamp Transistor (SEF2)	Emitter Follower	Source Follower
2mA	**280µA**	**14mA**	**14mA**	**3mA**	**3mA**

THD and effective number of bits are the most important performance metrics when THA is employed as the front-end of the ADC. Total harmonic distortion and effective number of bits versus input frequency for 100MS/s and 200MS/s sampling frequencies are shown in Figure 2.13. With the SEF1 design, for both sampling frequencies, 11 bits are available under Nyquist condition, and ENOB degrades to 9 bits around 500MHz input frequency mainly due to sink/source current of the hold capacitor.

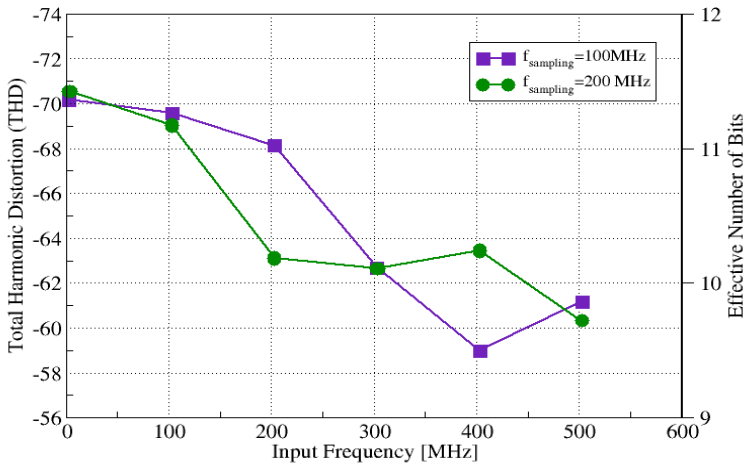


Figure 2.13: THD and ENOB vs. input frequency with SEF1 and EF output buffer

The transient response of the circuit to a $2V_{PP}$ input signal at a frequency close to Nyquist frequency, 46MHz is given shown in Figure 2.14. Because of current mirror mirroring error, there is still a voltage droop of 2.5mV/ns. The gain reduction is 2.5dB due to input buffer gain. To see the tracking behavior more clearly, the input and output signals are shown on different Y axis.

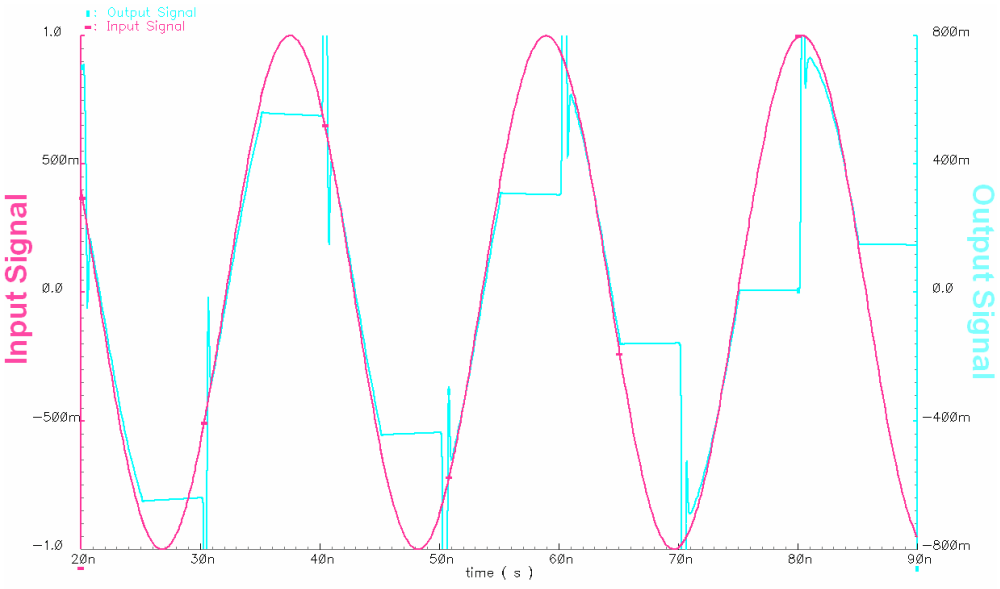


Figure 2.14: Transient response of SEF1 to 46MHz 2 V_{PP} input signal

The THA with SEF2 switching stage performance is shown in Figure 2.15.

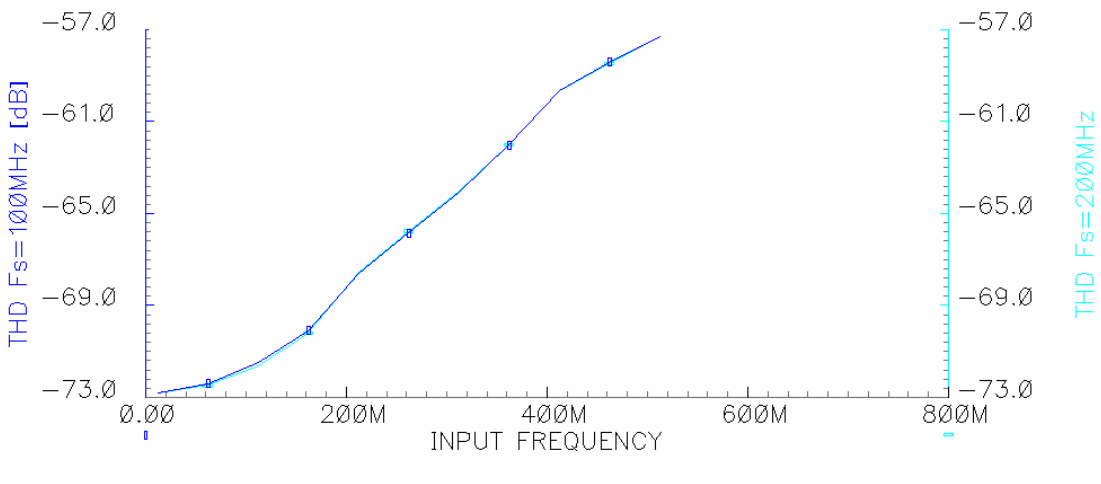


Figure 2.15: THD vs. input frequency with SEF2 and SF output buffer

CHAPTER 3 : MULTIPLYING DIGITAL TO ANALOG CONVERTER

3.1 General Design Considerations for Pipeline ADCs

A wide variety of pipelined analog to digital converter architectures exist. They differ in the quantization and residue characteristics in each stage, of the inter-stage gain factors and in the way the partial conversion results are combined to form the digital output signal.

The typical configuration of a pipeline ADC contains several stages each with a low resolution ADC and an analog circuit calculating the quantization error, which is passed to the next stage. Conceptually, the analog circuit contains a digital to analog converter, a subtractor and a sample/hold amplifier. Usually all three operations are performed by the same block, the so-called multiplying digital to analog converter (MDAC). An N stage pipeline ADC is illustrated in Figure 3.1, where each stage yields B bits.

The first process in each stage is sampling and holding the input signal. This sampled and held analog signal is converted by the coarse ADC, which produces the digital output of the stage. Then, using a DAC, the quantized value is subtracted from the sampled input signal to obtain the quantization error. The quantization error is amplified by the factor of 2^B by the inter-stage amplifier to be sampled by the subsequent stage on the next clock cycle.

The simultaneous operation of each stage allows obtaining high throughput independently from the number of stages. The sample rate is limited only by the time required for the resolution of B bits in a stage. This feature endorses the usage of pipelined ADCs in high sampling frequencies. Generally, if concurrent/interleaved processing is used, the latency of the converter is roughly N/2 clock cycles. This latency is inevitable due to pipeline nature and should be taken into consideration where latency is an issue.

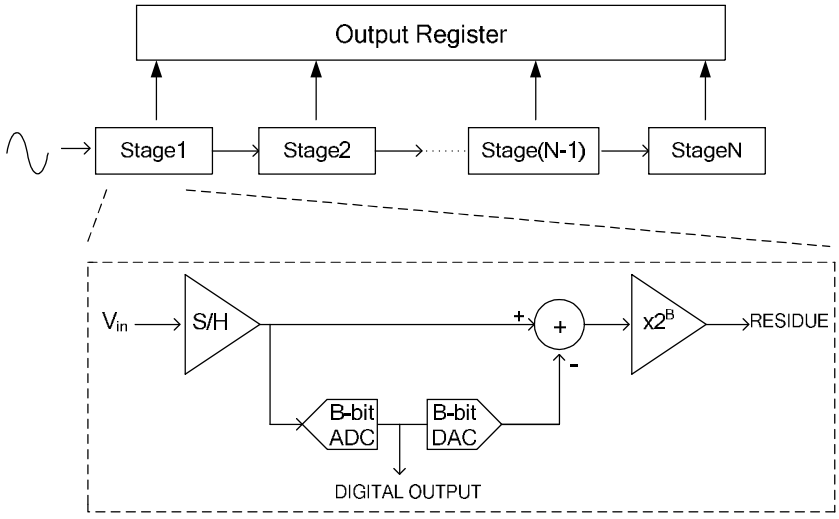


Figure 3.1: General model of pipeline ADC

The advantage of pipeline structure is the possibility of increasing the resolution by simply adding identical stages. Thus, the hardware and area are changing linearly with the number of bits. Because precision residue amplification is required in each stage, fast-settling operational amplifiers are needed, which limit the throughput and increase power consumption. On the other hand, using bit overlapping technique, the accuracy requirements of the sub-ADCs are greatly relaxed allowing low-power comparators. Since the contribution of stages to the input referred noise and error is reduced by the inter-stage gain, the later stages have more relaxed noise and linearity requirements than the first few stages. Therefore, later stages can have scaled down capacitors (and amplifiers) to save power.

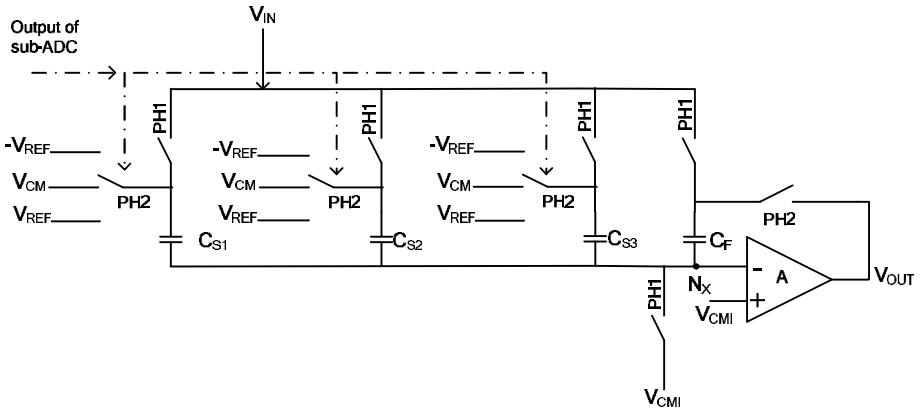
3.2 Multiplying Digital to Analog Converter

3.2.1 Operation of MDAC

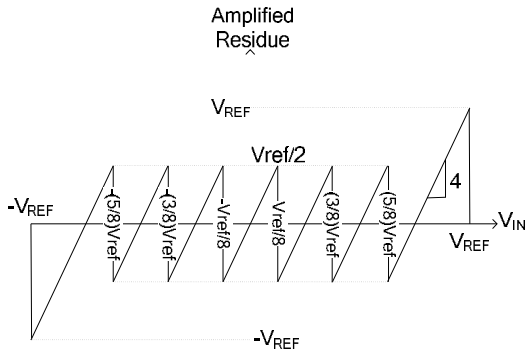
As mentioned in the previous section, in pipeline ADCs, each stage consists of an arithmetic function block called multiplying digital to analog converter and a sub-ADC which usually has a redundant bit to eliminate the effects of the flash quantizer offset errors.

In this work, the task of the first stage of the ADC is to resolve 2 bits, and a half redundant bit is added to minimize the influence of quantizer offset errors. The 2.5bit/stage MDAC and its transfer function are shown in Figure 3.2. For simplicity,

the single ended configuration is shown, but the actual implementation is fully differential. In high performance analog circuit design, fully differential circuits are more popular because of better common mode noise rejection and lower sensitivity to the variation of power supply compared to single ended counterparts. They also cancel even order harmonics and offer larger dynamic range by doubling the effective signal swing. However, they necessitate a common mode feedback loop to define the output common mode [8].



(a)



(b)

Figure 3.2: 2.5bit/stage MDAC (a), and its ideal transfer function (b)

The function of MDAC is threefold; to sample and hold the input signal, to generate a residue that is the difference between the input and a coarse approximation of input, and to amplify this residue. In this approach, the circuit operates on two phases, sampling phase and amplification phase. During the sampling, the input signal is sampled onto the capacitors C_{S1}, C_{S2}, C_{S3} and C_F. Then, in the amplification

phase, the bottom plates of the sampling capacitors are switched to one of three reference voltages, V_{REF}, $-V_{REF}$, and V_{CM} , depending on the output of sub-ADC, and C_F is flipped over the input and output node of the amplifier to act as a feedback capacitor. In this way, the voltages over the sampling capacitors are subtracted from the analog sampled voltage V_{IN} and the resulting residue is multiplied by 4 if the amplifier has a high DC gain. From charge conservation for node N_X;

$$q_{PH1} = q_{PH2} \tag{3.1}$$

$$q_{PH1} = (V_{in} - V_{CMI})\left(C_F + C_{S1} + C_{S2} + C_{S3}\right) \tag{3.2}$$

$$q_{PH2} = C_F(V_O - V_{CMI}) + C_{S1}(b_1 V_{REF} - V_{CMI}) + C_{S2}(b_2 V_{REF} - V_{CMI}) + C_{S3}(b_3 V_{REF} - V_{CMI}) \tag{3.3}$$

For a sufficiently high amplifier gain, the transfer function is obtained as

$$V_O = V_{in}\left(1 + \frac{C_{S1}}{C_F} + \frac{C_{S2}}{C_F} + \frac{C_{S3}}{C_F}\right) - V_{REF}\left(b_1\frac{C_{S1}}{C_F} + b_2\frac{C_{S2}}{C_F} + b_3\frac{C_{S3}}{C_F}\right) \tag{3.4}$$

Where the coefficients b_1, b_2, b_3 take the values -1, 1 or 0 depending on the sub-ADC output. Table 3.1 shows one possible encoding of b_i.

Table 3.1: Truth table of the switched control logic

	C_{S1}	C_{S2}	C_{S3}	b_1	b_2	b_3
$V_{IN} < -0.625V_{REF}$	$-V_{REF}$	$-V_{REF}$	$-V_{REF}$	-1	-1	-1
$-0.625V_{REF} < V_{IN} < -0.375V_{REF}$	$-V_{REF}$	$-V_{REF}$	0	-1	-1	0
$-0.375V_{REF} < V_{IN} < -0.125V_{REF}$	$-V_{REF}$	$-V_{REF}$	$+V_{REF}$	-1	-1	+1
$-0.125V_{REF} < V_{IN} < 0.125V_{REF}$	0	$-V_{REF}$	$+V_{REF}$	0	-1	+1
$0.125V_{REF} < V_{IN} < 0.375V_{REF}$	$-V_{REF}$	$+V_{REF}$	$+V_{REF}$	-1	+1	+1
$0.375V_{REF} < V_{IN} < 0.625V_{REF}$	0	$+V_{REF}$	$+V_{REF}$	0	+1	+1
$V_{IN} > 0.625V_{REF}$	$+V_{REF}$	$+V_{REF}$	$+V_{REF}$	+1	+1	+1

For perfectly matched sampling and hold capacitors, transfer function turns into:

$$V_O = 4\left(V_{in} - \frac{V_{REF}}{4}\left(b_1 + b_2 + b_3\right)\right) \tag{3.5}$$

The maximum resolution achieved is limited by thermal noise, by the gain and nonlinearity errors of the MDAC produced by capacitor mismatches and amplifier gain errors [9]. If the offset of flash quantizer is in the error margin which is provided by redundant bit, it has no influence on linearity. Thermal noise should be reduced by appropriate sizing of the capacitors. The gain and nonlinearity errors in MDAC can be reduced by employing self-calibration techniques [10,11] and appropriate amplifier designs. The effects of these error sources on the ADC performance will be explained in the following section.

3.2.2 Error Sources in MDAC

The error sources in an analog to digital converter can be divided into two categories; random noise (thermal, flicker) errors and deterministic errors due to mostly mismatch, finite gain of the amplifier, and charge injection. While mismatch effects can be corrected by calibration, noise cannot because it is not predictable.

3.2.2.1 Sampling Error Considerations

Thermal Noise

At temperatures above absolute zero, the random motion of electrons causes thermal noise. Since electrons carry charge, their random motion, which is proportional to temperature, result in random currents.

In an MDAC block, the operation is based on switched capacitors. The noise power which is sampled on a capacitor is proportional to kT/C which means large capacitances are required for high dynamic range. On the other side, for a given bandwidth specification, this will increase power consumption. Thus, there exists a fundamental trade-off between thermal noise, speed and power dissipation.

Bottom- Plate Sampling

The bottom plate sampling method is used to eliminate signal dependent charge injection where high accuracy is needed. As shown in Figure 3.3, when PH1' changes from high to low, the circuit stops to track the input signal and the charge on the capacitor C_S is trapped. When M1 turns off, output is isolated from input.

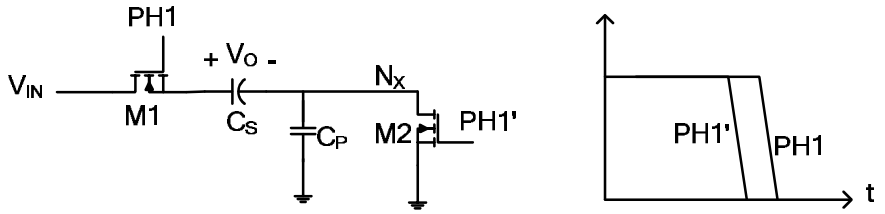


Figure 3.3: Bottom plate sampling circuit

While M2 is off, the charge injected from M1 cannot be stored on C_H, because the negative charge on bottom plate is fixed since there is no DC path that charge can flow. Until PH1 goes down node N_X stays floating and the capacitor plates will both track the input signal and the charge over sampling capacitance which represents the sampled signal stays constant. The charge injection of M2 is constant because it is connected to the amplifier input common mode. Therefore it isn't signal dependent [12]. In the MDAC configuration shown in Figure 3.2(a), in the amplifying phase N_X goes to virtual ground and the charge in the parasitic capacitance Cp is returned to Cs and thus does not alter the signal charge.

3.2.2.2 Comparator Offsets

The comparator's function is to compare two signals and to produce an output showing which of the two is larger. The most important non-ideality in comparators is offset. When the comparator computes the difference between the input and a reference voltage, an internal offset is added which causes wrong decision on the issue whether the two signal levels are close to each other. In a stage without redundancy, when the comparator makes a wrong decision, in addition to wrong output code, a wrong reference voltage is subtracted from the input signal in the MDAC block, causing the amplified residue to be out of range and to saturate the next stage of the ADC [13].

As long as the amplified residue stays within the input range of the next stage, it can be digitized and no error results after bit overlapping. Thus, reducing the gain of the stage relaxes the sensitivity of the converter to the comparator's offset. However, due to gain reduction, resolution of the stage also decreases.

3.2.2.3 Stage Gain Error

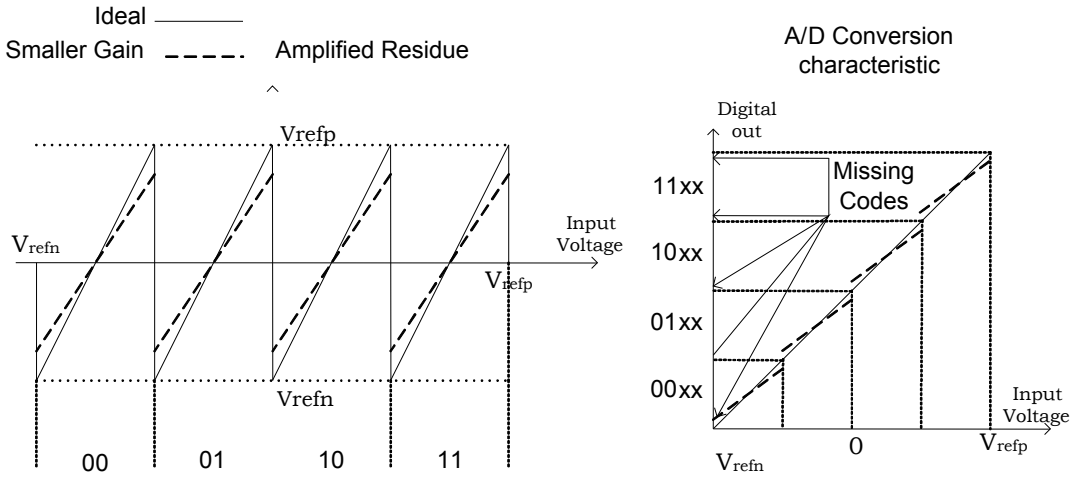
The gain error in the residue amplification can cause the residue range to be smaller or larger than the conversion range of the following stage if there is no redundancy. Figure 3.4 illustrates this problem where the residue amplification characteristic of the MDAC exhibits different segment slope from the ideal one.

In switched capacitor implementations of MDAC, the residue amplification gain error is mainly due to mismatches between the sampling capacitors and the feedback capacitor. Depending on the output code of quantizer, mismatch also shifts the segments. As a result the data conversion characteristic may become non-monotonic or may have missing codes and discontinuities.

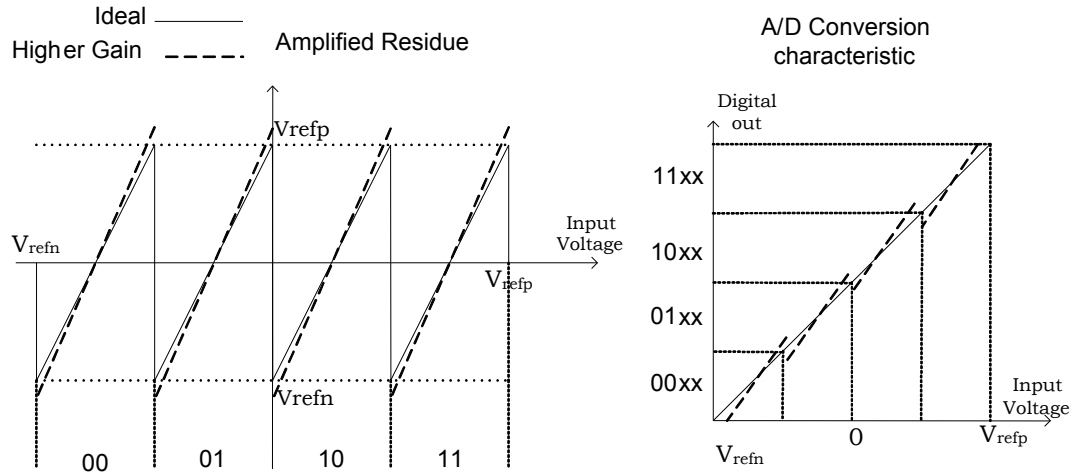
$$V_O = \underbrace{\frac{C_T}{C_F + \frac{C_T + C_p}{A}}}_{\text{SLOPE}} \left[V_{IN} - \underbrace{V_{REF} \sum_{i=1}^{3} \left(\frac{C_{Si}}{C_T} b_i \right)}_{\text{ZERO-CROSSING}} \right] \tag{3.6}$$

Equation (3.6) is the expression of the 2.5 bit MDAC stage that illustrated in Figure 3.2. C_p is the parasitic capacitance at the input of amplifier and C_T is the total capacitance of sampling capacitors and feedback capacitor.

Besides, limited DC gain of OTA also influences the gain error in the residue transfer function. As can be concluded from Equation (3.6), the gain error is independent from the input code, meaning that all segments of the residue amplification have the same slope. In order to overcome the residue amplification gain error and shifts of the segments, which are sub-DAC errors, due to capacitance mismatch, either analog or digital self-calibration techniques can be employed [9]. Also, the non-linearity of the amplifier gain will cause a curved transfer characteristic in A/D conversion graphic and it will contribute to differential nonlinearity.



(a)



(b)

Figure 3.4: Residue amplification and A/D conversion characteristic of a 2 bit MDAC stage with a smaller gain (a), and a higher gain (b) than the ideal

3.3 Design of the Residue Amplifier

In the pipeline ADC, each stage resolves a few bits, 2 bits in this design, in one clock period and transfers the residue to the next stage so that the difference can be resolved further in the subsequent stages. Therefore the accuracy of the inter-stage residue amplifier limits all ADC's performance. For the amplifier in the pipeline, the load capacitance and feedback factor are known for each phase of the clock. Also it is assumed that the desired sampling rate is known.

After choosing the topology, optimization can be achieved by sizing devices, compensation capacitors, and bias currents so as to minimize power dissipation at a fixed sampling rate.

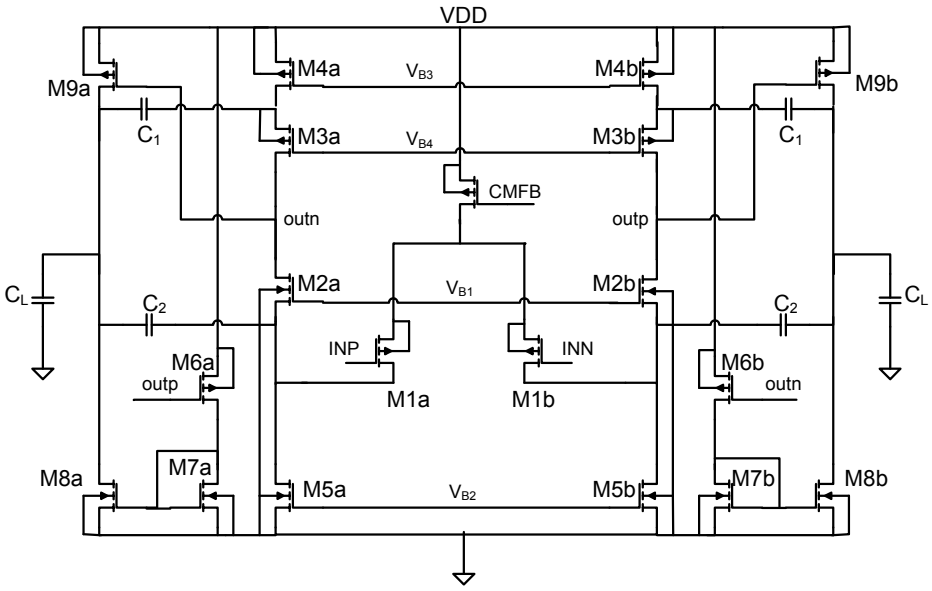


Figure 3.5: Class-AB cascode compensated, folded cascode OTA

The main challenge in an amplifier design is to obtain high DC gain and high unity gain frequency at the same time to meet the speed and accuracy requirements. Especially in switched capacitor application, settling performance which is a reflection of unity gain bandwidth parameter, directly determines the maximum clock frequency. Cascoding is one of the most common methods to enhance DC gain without degrading the performance at high frequency. Thus, a folded cascode structure is used as the first stage. Because of stacked transistors in the cascode structure the voltage swing is limited. For 10 bit accuracy, the gain should be boosted. A second stage is added, in order to avoid voltage swing limitation of folded cascode and to improve gain.

In the existent ADC, class A is used as the first stage amplifier. In this work, as introduced in the introduction, class AB amplifier is investigated as an alternative solution, whether it offers less power consumption or not. The class-AB folded cascode OTA topology is shown in Figure 3.5 [7]. To build a class AB operation, NMOS current mirrors are added. On the other hand, because there are two parallel signal paths with different frequency response, a pole-zero doublet is created (Figure

3.6). Thus, the signals from two paths have different phases and cause two settling behaviors.

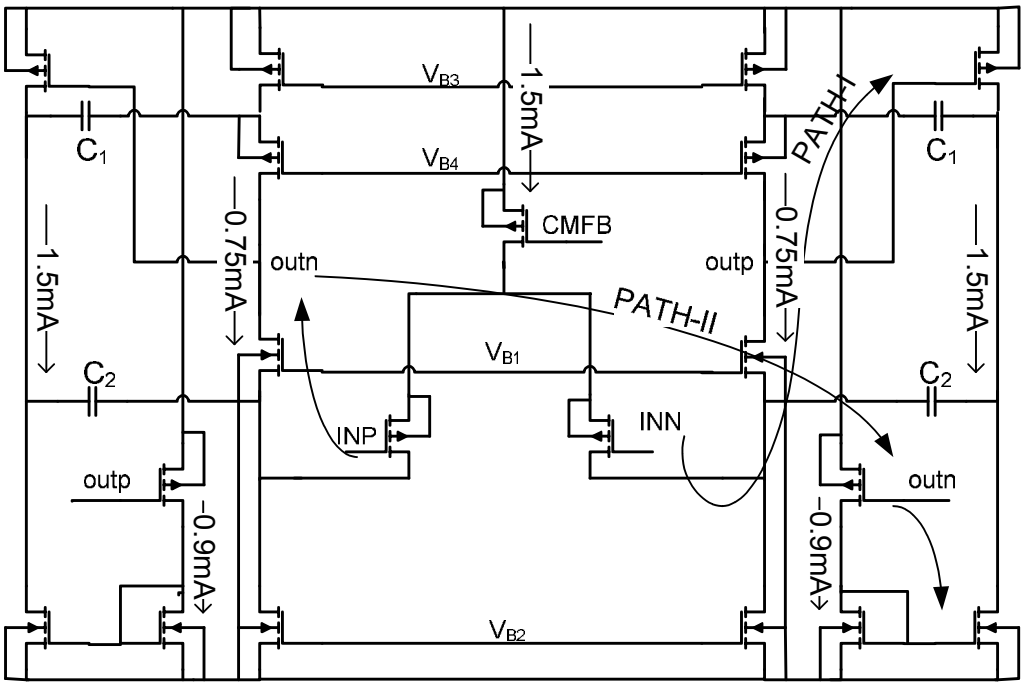


Figure 3.6: Signal paths and branch currents in class AB amplifier

In a two stage amplifier, to avoid instability in the closed loop, the amplifier has to be compensated. In this work, instead of classical miller compensation, cascode compensation is employed for better settling behavior. In cascode compensation, the compensation capacitance is divided into two to create symmetry and connected between the output and low impedance nodes of first stage output. This blocks the feedforward path which creates the right half plane zero in miller compensation. Thus, it eliminates the need of nulling resistor [7]. With cascode compensation, although the bandwidth limitation is mostly overcome, the settling behavior becomes very complex. In [7], a detailed small signal analysis of this circuit is given.

The requirements in the first stage of ADC are $1.5V_{PP}$ differential swing and 8 bit accuracy at the output at 100MHz sampling frequency. It is employed to solve 2 most significant bits. In the existent design for noise considerations and power issues the total sampling capacitor is chosen as 2pF, and the load capacitance is 1pF.

From MDAC requirements, the amplifier specifications are deduced. The gain error in the closed loop is $1/\beta A_O$. Feedback factor is ¼ and for 8 bit accuracy, the required DC gain is:

$$1/\beta A_O < 1/2^{(n+1)} \Rightarrow A_O > 66dB \quad \textbf{(3.7)}$$

In the pipeline architecture, since the accuracy requirement is relaxed from the first stage through the last, the second stage needs 8 bit accuracy. The settling time should be less than half of the clock period. From the unity gain bandwidth and settling time relation for a first order system, unity gain bandwidth requirement is calculated as,

$$t_{SET} = \frac{n \ln 2}{2\pi\beta f_u} \Rightarrow f_u > 880MHz \quad \textbf{(3.8)}$$

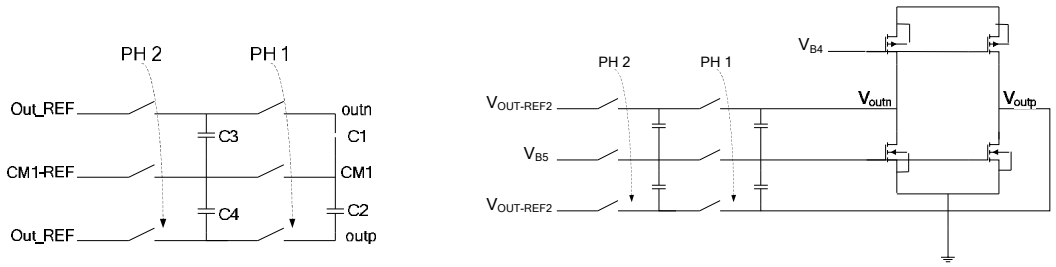
For settling time half of the duty cycle, 2.5ns is taken. The load capacitance is the following stage's input capacitance which is composed of sampling capacitors (1pF). The branch currents are shown on Figure 3.6 and the device sizes are given in Table 3.2.

Table 3.2: Device Sizes of OTA

Devices	M1	M2	M3	M4	M5	M6	M7	M8	M9
W/L of transistors	500	100	300	300	100	180	60	100	300
L [nm]	180	500	500	250	250	180	180	180	180

A fully differential OTA has many advantages compared to single ended OTA, such as high voltage swing and immunity to common mode noise. In addition, even harmonics are eliminated due to symmetrical structure. But the drawback of fully differential OTA is the need of common-mode feedback circuit. Since the common mode level is not defined by the differential feedback at the output, it may drift out of the high-gain region if no common mode feedback is added. On the other hand, employing a CMFB circuit will increase power consumption.

In the designed amplifier, since there is no common mode coupling between the two stages, two separate common mode feedback loops are needed. As illustrated in Figure 3.7 C_1 and C_2 continuously senses the first stage's output common mode. C_3 and C_4 are used to be charged to a desired DC value and pre-charge the main capacitors C_1 and C_2. In PH2, the average of output common modes are taken and shifted to the reference voltage [8]. To drive the output of the second stage, two common source amplifiers are added to the common mode sensing switch capacitor network [7] as shown in Figure 3.7 (b).



(a) **(b)**

Figure 3.7: Common-mode feedback circuits

3.4 Simulation Results

The AC response of the amplifier is given in Figure 3.8. The phase margin at a gain of 12dB (corresponding to 0dB loop gain) is 80º. The folded cascode stage contributes 46 dB to the total gain.

The residue characteristic of the stage is shown in Figure 3.9. The slope of each segment is 4 with %0.05 error. Since mismatch is not modeled in the simulation, the error is coming from the amplifier's nonlinearity and finite DC gain.

The transient response to ramp input is shown in Figure 3.10.

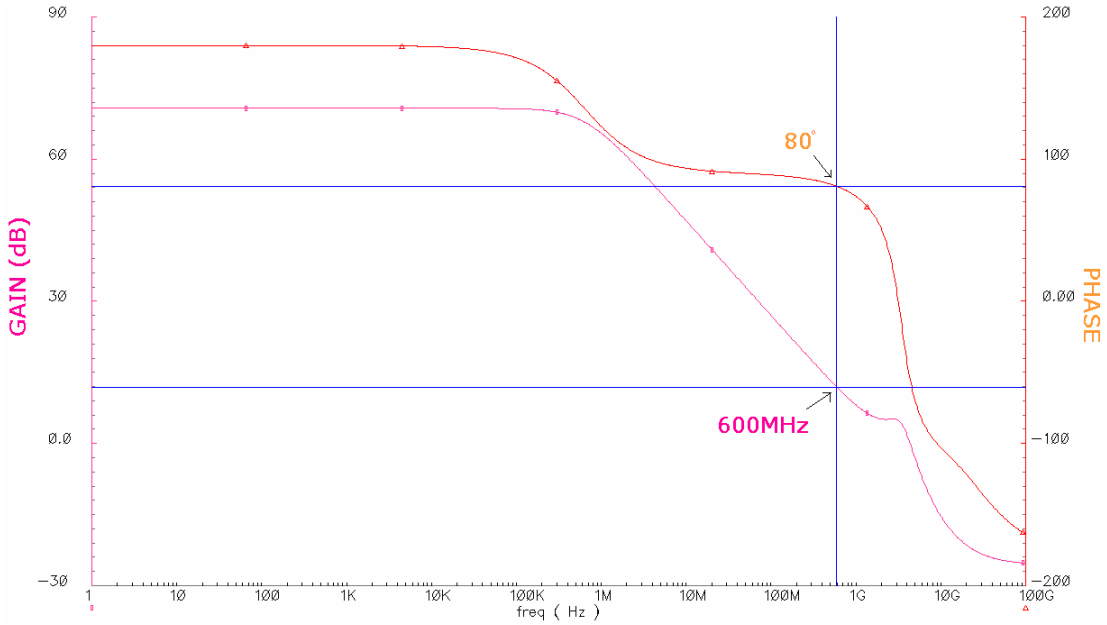


Figure 3.8: AC response of OTA

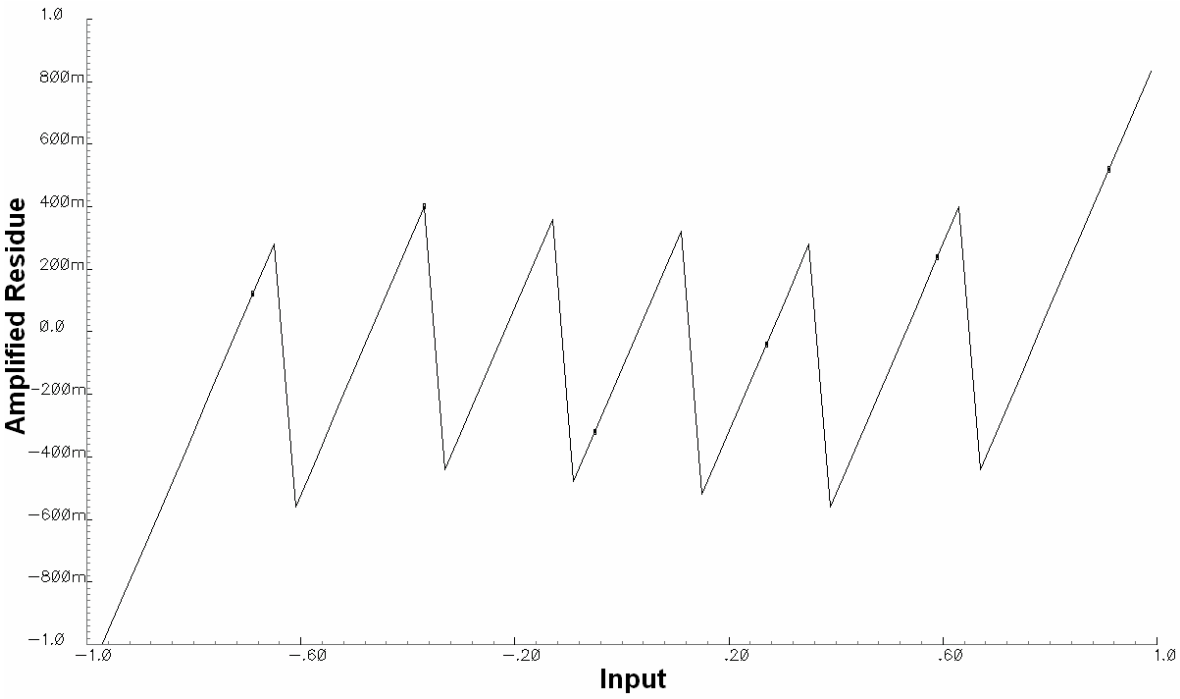


Figure 3.9: Residue characteristic of 2.5bit/stage MDAC with class AB OTA

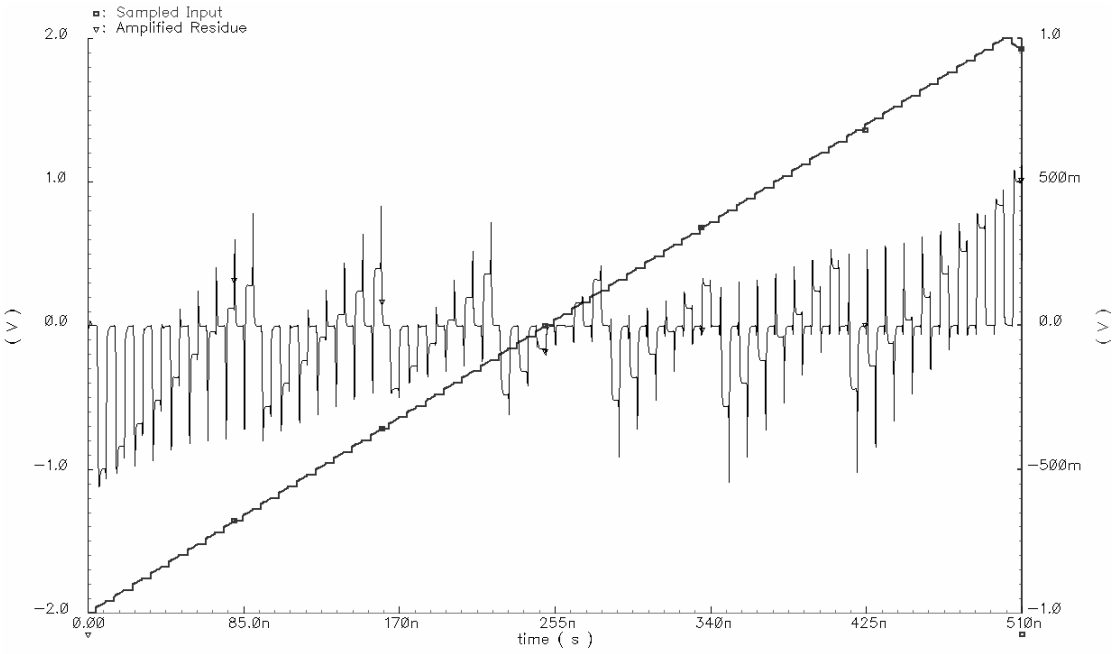


Figure 3.10: Transient response of MDAC to ramp input

In Figure 3.11, Y axis is difference of the step response and the steady state value while X axis is the settling time. 9 bit accuracy is reached after 4.5 ns. This figure shows that the settling to high accuracy is slowed down by the slow-settling component due to the pole-zero doublets.

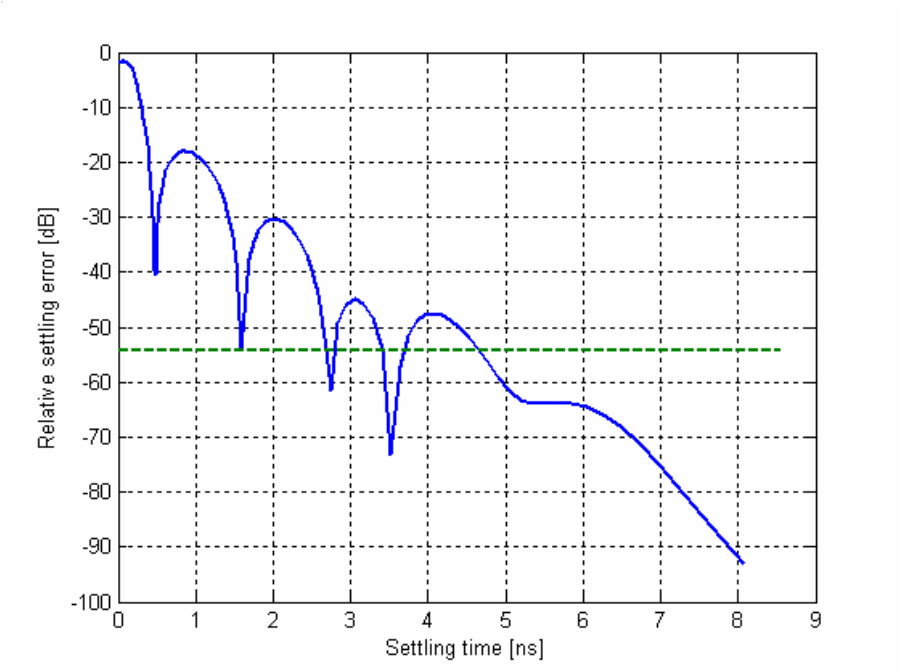


Figure 3.11: Settling error vs settling time

CHAPTER 4 : CONCLUSION

In this thesis, two critical circuits for high resolution and high speed analog to digital converters are designed; a track and hold amplifier that is utilized in the front-end of the ADC and a wide band amplifier that is used in the first stage of the converter as a residue amplifier.

This work is a part of ongoing multichannel ADC project in which 10 bit 100MS/s ADCs will be used with a front end circuit as multiplexer. As discussed in the introduction in the multichannel architecture the front end can be implemented in different ways. From this work, it is observed that a SEF front end approach is beneficial when the speed advantage of HBT is utilized. Because the power consumption is already increased by linearity requirements and not to waste this excessive power consumption which is needed for the linearity, it is more practical to use it as the master THA in front of a multichannel ADC where high sampling rate is necessary. In this case, apparently output buffer should be redesigned for fast settling.

The track and hold amplifier's task is to relax the bandwidth and accuracy requirements of the ADC, therefore the outstanding performance metric comes out as total harmonic distortion and sampling rate. The target input bandwidth is 500MHz. Designed SEF-THA with the clamp transistor, is able to provide 10 bits until 500MHz at 800MHz sampling frequency. Originally, the target was 100MS/s, but now, given the use of the THA as master THA for a 8-channel 800MS/s ADC, the performance at 800MS/s is more important. In Figure 4.1 the layout of THA without the output buffer is shown. THD performance of the circuit is given at 800MS/s in Figure 4.2.

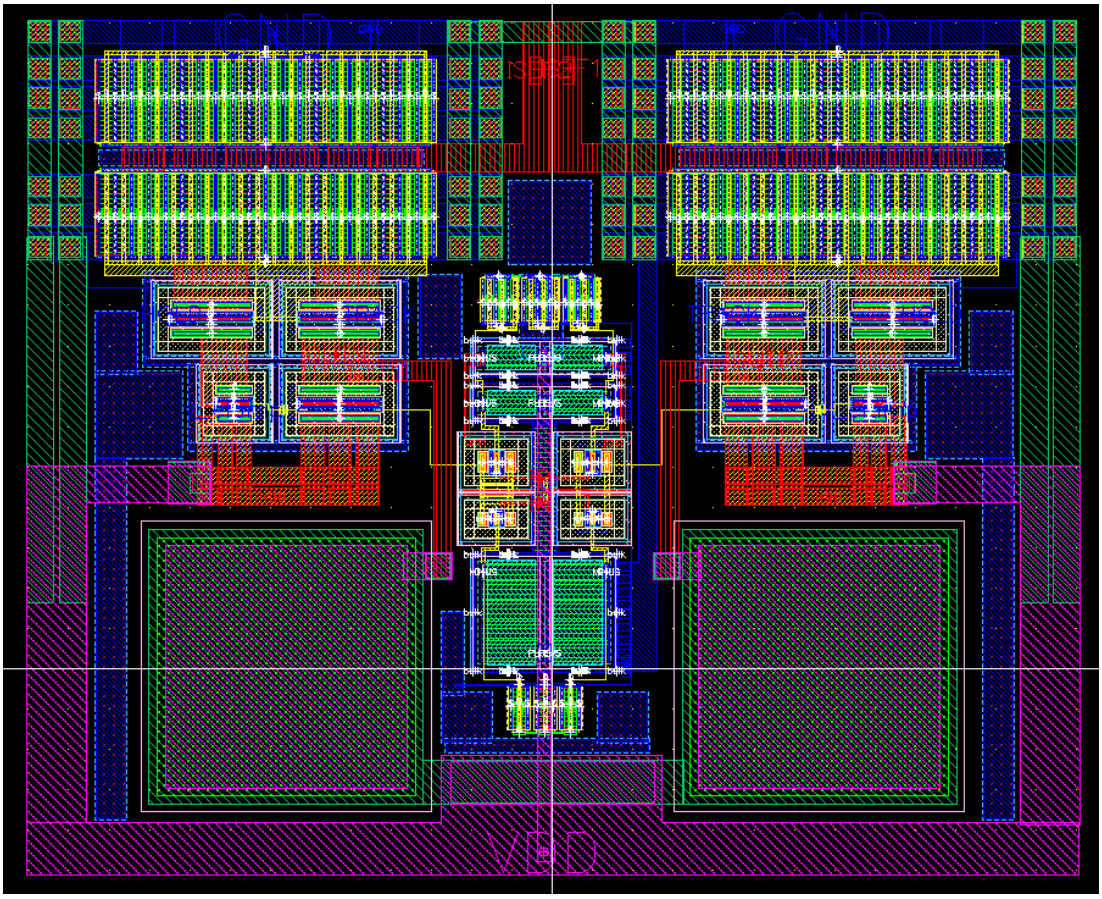


Figure 4.1: Layout of THA without output buffer

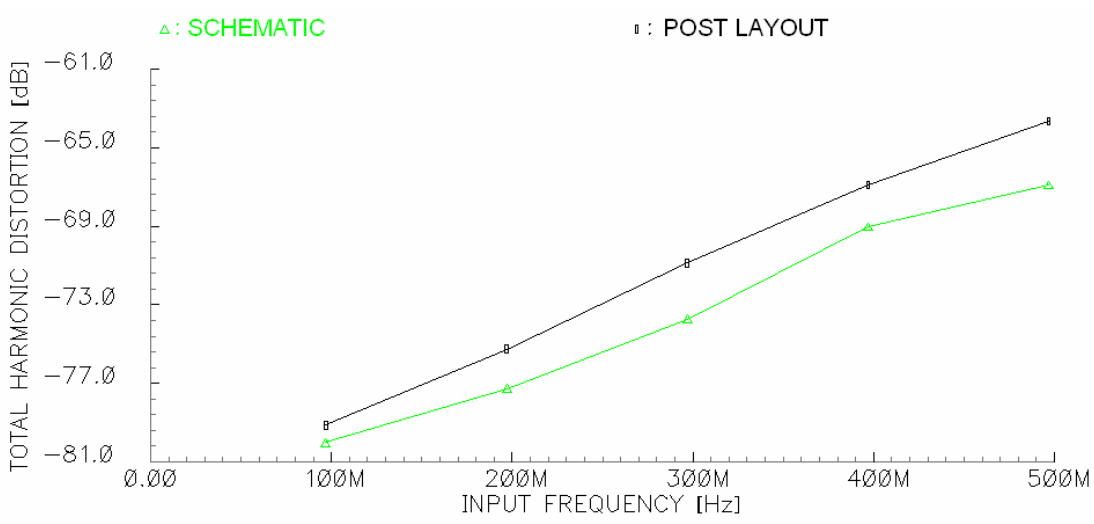


Figure 4.2: Post-layout THD vs. input frequency performance of THA without output buffer at 800MS/s

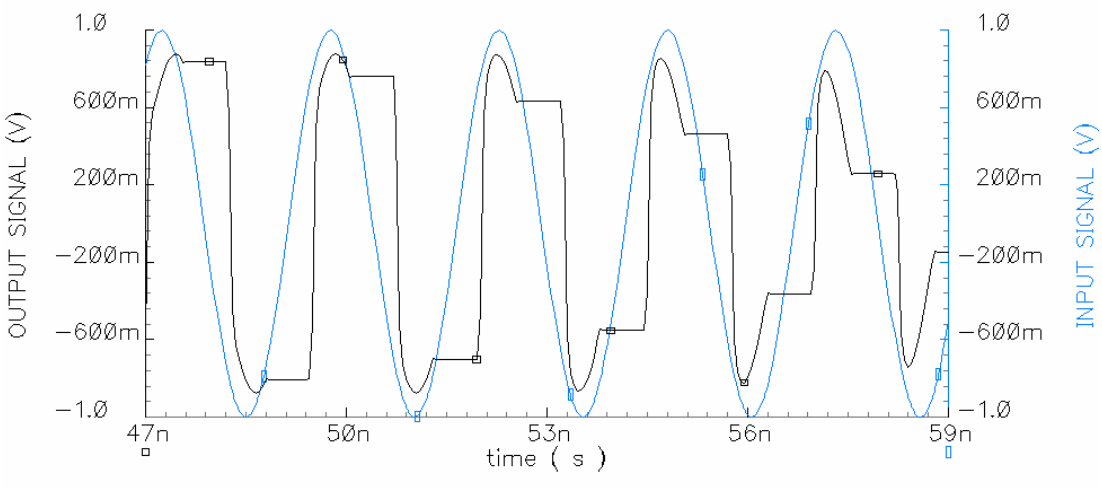


Figure 4.3: Post-layout transient simulation result of THA to 490MHz at 800MS/s

The transient response of the circuit to an input signal near Nyquist frequency at 800MS/s is given in Figure 4.3. The output voltage swing is $1.5V_{PP}$, which provides a good margin over noise floor. The track and hold amplifier characteristics are given in Table 4.1

Table 4.1: Characteristics of THA

Technology	0.18µm 155GHz f_T SiGe BiCMOS
THD	- 66 dB @ 400 MHz
Output Range	1.5 V_{PP}
Sampling Rate	800 MHz
Supply voltage	4.5 V
Hold Mode Feedthrough	-70.5 dB
Power Dissipation	140 mW (w/o output buffer)

The monte carlo simulation that takes device mismatch into account is shown in Figure 4.4. A comparison of the state-of-art is shown in Table 4.2 to see where this work stands. Since the specifications varies depending on the

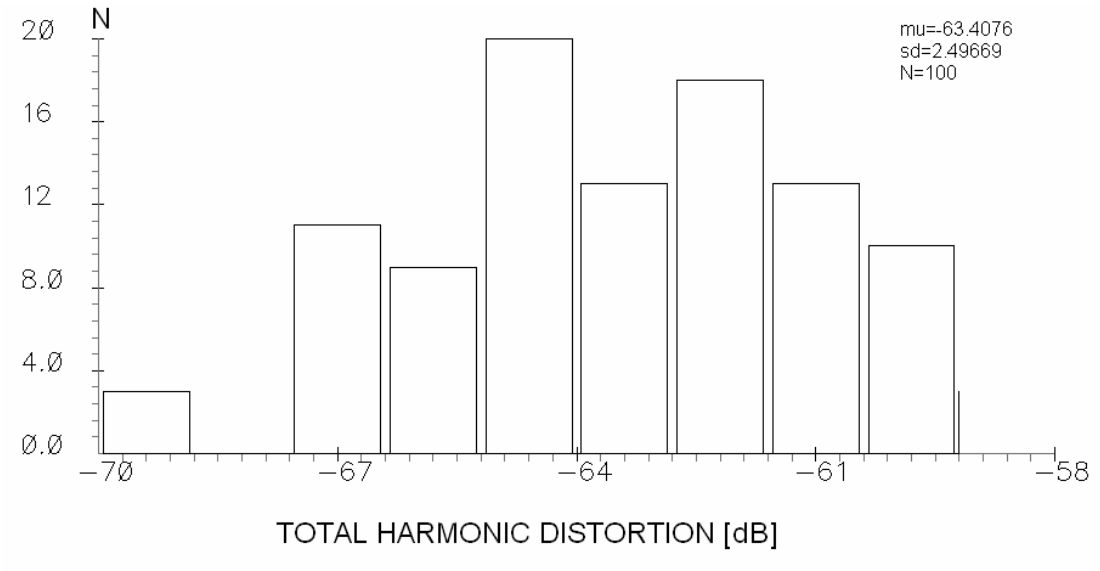


Figure 4.4: Monte carlo simulation results showing the THD distribution for 100 samples (simulation runs), Fin=397MHz, Fs=800MS/s

Noise and nonlinearity error contributions of the first stage amplifier of the pipeline ADC will be direct to the input. Hence it is very crucial to present a fast and accurate settling. In the existent ADC, class A amplifier was employed and in this work, it is investigated if it possible to save power with class AB. The designed class-AB folded cascode OTA performance summary are given in Table 4.2. It is observed that the power consumption is 5mW more than class A amplifier. This difference is due to the additional branches that are necessary for the class AB operation. Also, in Class AB the settling behavior becomes more complex.

Table 4.2: Performance of OTA with 1.25pF load

Technology	0.18μm CMOS
DC Gain	71 dB
Closed Loop BW @ 12dB (β=1/4)	600 MHz
Phase Margin @ 12dB (β=1/4)	80º
CMRR	145 dB
PSRR	84 dB
Output Swing	1.5 V_{PP}
Supply Voltage	1.8 V
Power Consumption	23.5 mW
Integrated MDAC Output Noise	3.5 mV/$\sqrt{Hz}$

The amplifier is employed in the first stage of a 12 bit 100MS/s pipeline ADC. And in Figure 4.5, the total conversion error is shown. This error contains all sources mentioned in chapter 3. Since it is less than 1 LSB, resolution achieved as 12 bits.

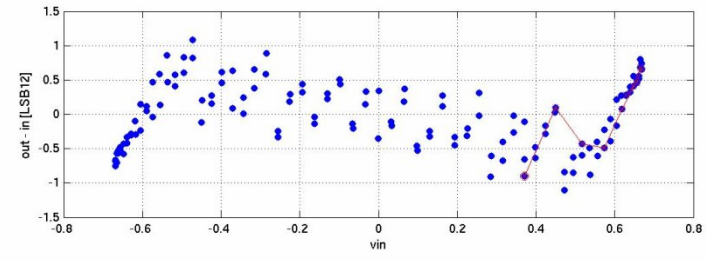


Figure 4.5: Conversion error of 12 bit ADC at 100MS/s, F_{in}=3/64x100MHz

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