ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

HIGH PERFORMANCE TUNABLE ACTIVE INDUCTORS FOR MICROWAVE CIRCUITS

Ph.D. Thesis

Hadi GHASEMZADEH MOMEN

Electronics and Communications Engineering Department

Electronics Engineering Programme

Thesis Advisor: Assoc. Prof. Dr. Metin YAZGI
Thesis Co-Advisor: Assist. Prof. Dr. Ramazan KÖPRÜ

AUGUST 2016

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

MİKRODALGA DEVRELERİ İÇIN YÜKSEK BAŞARIMLI AYARLANABİLİR AKTİF ENDÜKTÖRLER

Doktora Tezi

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AĞUSTOS 2016

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Date of Submission : 15 July 2016
Date of Defense : 04 August 2016

To my family

FOREWORD

First and foremost I would like to express my sincerest appreciation to my advisor and Co-Advisor, Assoc. Prof. Dr. Metin YAZGI and Assist. Prof. Dr. Ramazan KÖPRÜ, who have guided me throughout my Ph.D. dissertation with their patience and knowledge whilst allowing me to work in my own way. It was an honor for me to work with them during my time at Istanbul Technical University.

I would like to thank the members of my dissertation committee; Prof. Dr. Avni MORGÜL, Prof. Dr. Mustafa KARAMAN and Assis. Prof. Dr. Metin HÜNER for their valuable points and motivational advices.

My special thanks go to my brother-in-law, Ali, not only during Ph.D. study but also in my life for his emotional supports and fruitful discussions.

I am deeply and forever indebted to my family; my patient father, great mother, lovely sister and brother for their love, support and encouragement throughout my entire life, and in particular, I must acknowledge my wife, without whose endless help, I would not have finished this dissertation.

July 2016

Hadi GHASEMZADEH MOMEN
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ABBREVIATIONS

ABB : Analog Building Block
AI : Active Inductor
BPF : Band Pass Filter
CAD : Computer Aided Design
CD : Common-Drain
CG : Common-Gate
CS : Common-Source
DCT : Direct Computational technique
FAI : Floating Active Inductor
FFP : Feed Forward Path
GAI : Grounded Active Inductor
GC : Gyrator-C
IC : Integrated Circuits
LNA : Low Noise Amplifier
LPF : Low Pass Filter
MEMS : Micro Electro-Mechanical System
MRC : Multi-Regulated Cascode
OTA : Operational Transconductance Amplifiers
PA : Power Amplifier
PI : Passive Inductor
PSI : Passive Spiral Inductor
PVT : Process Voltage Temperature
QF : Quality Factor
RF : Radio Frequency
RFIC : Radio Frequency Integrated Circuit
RF-LST : Real Frequency Line segment Technique
SF : Scaling Factor
SFG : Signal Flow Graph
SRF : Self-Resonant Frequency
SRFR : Self-Resonance Frequency Range
SRFT : Simplified Real Frequency Technique
TAI : Tunable Active Inductor
TFAI : Tunable Floating Active Inductor
TGAI : Tunable Grounded Active Inductor
VCCS : Voltage Control Current Source
VCO : Voltage Control Oscillator

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HIGH PERFORMANCE TUNABLE ACTIVE INDUCTORS FOR MICROWAVE CIRCUITS

SUMMARY

There is critical need for inductive characteristics in RF applications, especially in filters, LNA, VCO, bandwidth-enhancement in many kinds of amplifiers, phase shifters, power divider and matching networks. The drawbacks of using passive and spiral inductors in CMOS process are discussed in the literature. It is shown that these kind of inductors suffer from a low quality factor, a low self-resonant frequency, a low and fixed inductance value and the need for a large silicon area.

Furthermore, it is shown in the literature that CMOS Active Inductors (AIs), which are synthesized using MOS transistors, offer a number of attractive characteristics as compared with their spiral counterparts. These characteristics include a low silicon consumption, a large and tunable self-resonant frequency, a large and tunable inductance, a large and tunable quality factor, and fully realizable in digital CMOS technologies.

Then principles, topologies, characterizations and implementation of the Gyrator-C (GC) network is discussed in-depth. The GC networks, which are implemented by operational transconductance amplifier, are suitable for RF application. This property arises from their minimum usage of active elements. It is shown that both grounded and floating active inductors can be implemented by GC networks. To provide a quantitative measure of the performance of AIs, a number of figure-of-merits have been introduced in the thesis. These figure-of-merits include frequency range, inductance tunability, quality factor, noise and power consumption. Due to parasitic components of CMOS transistors, designed AIs have inductive behavior in a specified frequency range. The low frequency bound is set by the frequency of the zero of the gyrator-C networks while the upper frequency bound is set by Self-Resonance Frequency (SRF). One of the key advantages of active inductors over their spiral counterparts is the large tunability of their inductance. The inductance of GC AIs can be tuned by varying either the transconductances of the transconductors or the load capacitance, which is implemented by MOS varactor.

Based on GC topology, there are many reported CMOS AI circuits in literature. All of them have tried to invent high performance AI by using different techniques. Some of recent proposed Grounded AI (GAI) and Floating AI (FAI) circuits are reviewed in the thesis. Some of them use negative resistor to compensate the loss of AI for QF enhancement. Some others try to use minimum number of transistors in order to increase the self-resonance frequency of AI for RF applications. In some applications, AIs are used in LNA circuits for gain boosting purpose. In that applications, designers have tried to cancel the noise of AI by using a feedback stage with a degeneration resistor to reduce the noise contribution to the input. The main aim of all the techniques is to cancel or reduce the effects of parasitic components.

In the thesis, four new grounded and floating AIs are designed by using advanced circuit techniques. The first one, Multi Regulated Cascode (MRC) stages are employed for lowering conductance in input and output nodes of AI. Thus, Q performance is improved. Since these stages are used only for increasing impedance of input/output nodes, they are made up of PMOS transistors in order to:

- minimize the input transistor as small as possible in order to adjust second stage biasing,
- decrease the number of transistors in main path of AC signal

Theoretical analysis and post-layout simulation results shows the effectiveness of using MRC stages usage in properties of AI. High Q symmetric floating version of low loss inductor is also designed by utilizing MRC stages.

Designers do their best to improve SRF and QF, two main characteristics in term of AI performance. An AI with ability to adjust its SRF and QF without affecting each other is designed and simulated as a third. The cascoding and RC feedback structures are used in the new design of AI. As it discussed before, input transistor is very important regarding to AI characterizations. Cascoding input transistor gives the ability to adjust the first gyrator’s transconductance and input parasitic capacitance independently which it results in adjusting the self-resonance frequency and quality factor separately. Due to our best knowledge from literature reviewing, it is first time that the properties of an inductor can be adjusted independently. Furthermore, the inductance value can be adjusted by other transistor’s transconductances. Also, the RC feedback is utilized to cancel the parasitic series-resistance of AI which results in QF enhancement. Since, bias condition of cascoding transistors is provided by a diode-connected transistor, the proposed structure is robust in terms of performance over variation in process, voltage and temperature.

The Noise of designed AIs has limited the use of them in RF applications such as LNAs. The main noise source of an AI is its input transistor. In order to have low noise AI, the input transistor should be designed large enough. But it leads to low SRF which limited the inductive frequency band. As a fourth active inductor design, a low-noise and low-loss AI is presented suitable for RF low noise applications. Utilizing all transistors in Common Sourse (CS) configuration on the AI circuit leads to low conductance nodes which causes the AI to have high Q. P-type MOS transistors and Feed-Forward Path (FFP) are employed to decrease noise of the AI, respectively.

The GC topologies can convert a low capacitance variation to high impedance changing which makes it a good choice for capacitive sensors. The capacitive based micro sensors convert mechanical signals to small capacitance variation. The capacitance variation in micro sensor is in the range of femto-Farads which makes it difficult to sense. Thus, the GC topologies can be used in capacitive sensors in order to sense small capacitive variations. In the thesis, this technique is used in a new accelerometer sensor. It is first time that a gyrator-C network is employed as an interface circuit for capacitive change detection in micro sensors. The new accelerometer structure is designed by using with ability to cancel cross section sensitivity. The sensor’s electrodes are located in such a way that enables the structure to detect acceleration in 3-axis independently. Embedding all 3-axis detecting electrodes in a single proof mass and ability to detect acceleration orientation are salient features of the proposed sensor. Consequently, a new GC configuration for sensing very small capacitance changes in a capacitive sensor is presented in the thesis. In the proposed configuration, the operating frequency range and scaling factor can be

adjusted without affecting each other by tuning the bias currents of utilized gyrators. In addition, the proposed configuration employs RC feedback together with the cascoding technique to cancel the effect of the parasitic components in order to get accurate scaling from gyrator-C network.

Finally, in order to show versatility of designed AIs, they are used in designed third and sixth order broadband microwave filters. The first one is a third order Chebyshev low pass filter. The second one, which is designed by using simplified real frequency technique is a sixth order Chebyshev band pass filter. The simulated frequency response of filters prove the workability of the designed AIs.

MİKRODALGA DEVRELERİ İÇİN YÜKSEK BAŞARIMLI AYARLANABİLİR AKTİF ENDÜKTÖRLER

ÖZET

RF uygulamalarında enduktif karakteristiğe önemli ölçüde ihtiyaç duyulmaktadır; bunlar, özellikle filtreler, düşük gürültülü yükselteçler (LNA, low noise amplifiers), gerilim kontrollü osilatörler (VCO, voltage controlled oscillators), pek çok farklı türde yükselteç için band genişliği iyileştirilmesi, faz kaydırıcılar, güç bölücüler ve eşleştirme (matching) devreleri vb. uygulamalardır. Pasif sarmal çip-içi CMOS endüktansların eksik yönleri ayrıntılı olarak literatürde tartışılmıştır. Bu tür endüktanslar düşük değer katsayısı (quality factor), düşük öz-rezonans frekansı (SRF, self-resonance frequency), sabit ve düşük değerli endüktans ve geniş bir silikon (silicon) alanı gerektirmeleri gibi istenmeyen özelliklere sahiptirler.

Diğer yandan, MOS transistorlar kullanılarak sentezlenen CMOS aktif endüktansların, pasif sarmal eşdeğer yapıları ile karşılaştırıldığında pek çok çekici karakteristik özellik sunabildikleri gösterilmiştir. Bunlar; geniş bir bölgede ayarlanabilir öz-rezonans frekansı başarımı, geniş bir bölgede ayarlanabilir endüktans başarımı, geniş bir bölgede ayarlanabilir değer katsayısı başarımı, CMOS teknolojileri ile tümüyle gerçeklenebilme ve az alan kaplama gibi karakteristik özellikleri olarak ortaya konulmaktadır.

Literatürde jiratör-C (GC) prensibi, topolojisi, karakterizasyonu ve uygulamaları ayrıntılı olarak ele alınmaktadır. İşlemsel geçiş-iletkenliği kuvvetlendiricisi (OTA, operational transconductance amplifier) ile gerçeklenen GC devreleri, RF uygulamaları için oldukça uygundur. Bu özellik, GC yapılarının söz konusu yapı kullanılarak en az sayıda aktif eleman ile gerçeklenebilmesinden kaynaklanmaktadır. Gerek topraklı (grounded) gerekse yüzen (floating) aktif endüktansların GC devreleri ile gerçeklenebildiği gösterilmiştir. Aktif endüktansların başarımlarının nicel olarak ölçülmesi amacıyla, çok sayıda ölçüt ortaya konulmuştur. Bu ölçütler frekans çalışma aralığı, endüktans ayarlanabilirliği, değer katsayısı, gürültü ve güç tüketimi gibi temel özellikleri içerirler. CMOS transistorların parazitik bileşenlerinden dolayı tasarlanan

aktif endüktanslar belirli bir frekans bölgesinde endüktif davranış gösterirler. Alt frekans sınırı, GC devrelerinin sıfır frekansı ile belirlenirken; üst frekans sınırı ise öz-rezonans frekansı ile belirlenir. Aktif endüktansların pasif sarmal eşdeğer yapılarına göre en önemli üstünlüklerinden biri de; endüktanslarının geniş bir değer aralığıunda ayarlanabilir olmasıdır. GC aktif endüktansların endüktans değeri, transistorların geçiş-iletkenliklerinin ya da MOS varaktörlerle gerçeklenen yük kapasitanslarının değiştirilmesi ile ayarlanabilir.

Literatürde, GC topolojisine dayalı pek çok CMOS AI (active inductor) devresi bildirilmiştir. Bunların tümü, farklı teknikler kullanılarak yüksek başarımlı AI yapıları oluşturmayı amaçlamışlardır. Bu tezde, bunlardan güncel olan bazı GAI (grounded AI) ve FAI (floating AI) yapıları gözden geçirilmiştir. Bunlardan bazıları, değer katsayısını (QF) iyileştirmek amacıyla, AI kaybını telafi etmek için negatif direnç kullanmışlardır. GC yapıları RF uygulamaları için tasarlandıklarında en az sayıda transistor kullanımı çok kritiktir. Çünkü bu durum AI öz-rezonans frekansının artmasına yardımcı olur. AI'ler, kazanç artırma amacıyla LNA'lerde geniş kullanım alanı bulabilmektedirler. Diğer taraftan, AI yapılarının en önemli dezvantajlarından biri gürültü başarımının pasif endüktanslara nispeten yüksek olmasıdır. Literatürde bu dezavantajı gidermek amacıyla teklif edilen yaklaşımlardan biri dejenerasyon direncinin bulunduğu bir geribesleme katı kullanılarak girişe gelen gürültü katkısını azaltmayı amaçlamıştır. Literatürde teklif edilen tekniklerin amacı, parazitik bileşenlerin etkisini azaltmak ya da tümüyle ortadan kaldırmaktır.

Bu tezde, ileri devre teknikleri kullanılarak, yeni topraklı (grounded) ve yüzen (floting) AI yapıları tasarlanmıştır. AI giriş ve çıkış düğümlerine ait iletkenlikleri azaltmak için çoklu-düzenlenmiş kaskod (multi-regulated cascode, MRC) katları QF değerini iyileştirme amacıyla kullanılmaktadır. MRC katı PMOS transistorlarıyla oluşturulmuştur. PMOS transistor kullanımı,

- ikinci kat kutuplamasını ayarlayabilmek amacıyla, giriş transistor boyutunun mümkün olduğunca azaltılmasını,
- ana AC işaret yolundaki transistor sayısının azaltılmasını,

sağlamaktadır.

Tezde sunulan teorik analiz ve serim sonrası benzetim sonuçları, MRC katı kullanımının AI özelliklerine yaptığı etkiyi göstermektedir. Elde edilen sonuçlar bu katların AI tasarımında yüksek QF elde edilmesini imkan tanıdığını ortaya koynaktadır.

Literatürde, iki ana AI başarım karakteristiği olan SRF ve QF başarımlarının iyileştirmesi için çok sayıda çalışma bulunmaktadır. Bu tezde, birbirlerini etkilemeksizin SRF ve QF başarımlarının ayarlanabilmesi özelliğine sahip bir AI'ın tasarımı ve benzetgimi yapılmıştır. Kaskod ve RC geribesleme yapıları yeni AI tasarımında kullanılmıştır. Daha önce de tartışıldığı üzere, AI karakterizasyonu açısından giriş transistoru çok önemlidir. Girişi transistorunun kaskodlanması, ilk jiratörün geçiş-iletkenliğinin ve giriş parazitik kapasitansının birbirinden bağımsız olarak ayarlanması gibi önemli ve kullanışlı bir özelliği beraberinde getirir. Bunun yanısıra, endüktansın değeri diğer transistorun iletkenliği ile ayarlanabilir. AI parazitik seri-rezistansını yok etmek amacıyla kullanılan RC geribeslemesi, QF iyileştirmesini sağlayabilmektedir. Kaskod transistorların kutuplama koşulu bir diyot-bağlı transistor ile sağlandığından; önerilen yapı proses, gerilim ve sıcaklık değişimleri açısından kararlı ve yüksek başarımlıdır.

AI yapılarında karşılaşılan düşük gürültü başarımı, AI'ların LNA gibi RF uygulamalarda kullanımını sınırlamaktadır. Bir AI'ın ana gürültü kaynağı giriş transistorudur. Düşük gürültülü AI elde etmek için, giriş transistoru yeterince büyük boyutlu olarak tasarlanmalıdır. Ne var ki, büyük boyutlu böyle bir transistor, düşük bir SRF ve dolayısıyla sınırlı bir endüktif bandı beraberinde getirir. Bu tezde, düşük gürültülü ve az kayıplı uygun bir AI, düşük gürültü gerektiren RF uygulamaları için sunulmuştur. Teklif edilen AI devresindeki tüm transistorların ortak-kaynak (common-source, CS) yapısında kullanılması, düşük iletkenliğe sahip düğümlerin dolayısıyla yüksek QF değerine sahip bir AI'ın elde edilmesine olanak sağlamaktadır. AI gürültüsünü azaltmak için, sırasıyla P-tipi MOS transistorlar ve ileri-besleme yolu yapısı (feed-forward path, FFP) kullanılmaktadır.

Bilindiği gibi, sensörler çok çeşitli fiziksel büyüklüklerin eletrik mühendisiliği alanına taşınmasını sağlamaktadır. Çok geniş kullanım alanı bulan sensör tiplerinden biri kapasitif mikro algılıyıcılardır. Kapasitif mikro algılayıcılar mekanik hareketleri küçük kapasitans değişimlerine çevirirler. Micro algılayıcıdaki kapasitans değişimi femto-Farad mertebesinde olup algılamayı zorlaştırmaktadır. Diğer yandan, küçük bir kapasitans değişimini yüksek bir empedans değişimine çevirebilmeleri dolayısıyla, GC topolojilerinin kapasitif algılayıcılarda kullanılabileceğini söylemek mümkündür.

Bu tezde, bu düşünceden yola çıkılarak, kesit duyarlılığını yok etme yeteneğine sahip yeni bir 3-eksen ivme-ölçer tasarlanmıştır. Yapının, her eksendeki ivmeyi bağımsız olarak algılayabilmesi için, algılayıcı elektrodları uygun olarak yerleştirilmiştir. Daha sonra, bir kapasitif algılayıcıdaki çok küçük kapasitans değişimlerini algılayabilmek için yeni bir GC yapısı teklif edilmiştir. Önerilen yapıda, çalışma frekansı aralığı ve ölçekleme çarpanı, kutuplama akımlarının ayarlanması suretiyle birbirini etkilemeksizin ayarlanabilmektedir. Ayrıca, önerilen yapıda, parazitik bileşenlerin etkisini yok etmek için RC geribesleme ve kaskod yapılar kullanılmaktadır.

Son olarak, bu tezde sunulan AI'ların çok amaçlı özellikte olduğunu göstermek amacıyla, 3 ve 6. dereceden geniş bantlı mikrodalga filtrelerde kullanılmaları ele alınmıştır. İlki 3. dereceden bir Chebyshev alçak geçiren filtredir. Basitleştirilmiş gerçel frekans tekniği (SRFT, simplified real frequency technique) ile tasarlanan ikincisi ise, 6. dereceden bir Chebyshev band geçiren filtredir. Filtrelerin benzetimle elde edilmiş frekans yanıtları, bu tezde sunulan AI'ların literatürdeki yapılara güçlü birer alternatif olduklarını ortaya koymaktadır.

1. INTRODUCTION

Most of nowadays high-volume customer applications requires the accessibility of low power, low cost and remote microsystems. According to these necessities, CMOS technology has turn into one of the most important alternatives for wireless communication systems. However, CMOS Spiral Inductors have found a broad range of applications in high-speed analog signal processing including impedance matching [1] and gain-boosting in wireless transceivers [2], bandwidth improvement in broadband data communications over wire and optical channels [3], oscillators and modulators [4, 5], RF bandpass filters [6], RF phase shifters [7], RF power dividers [8], and coupling of high-frequency signals [9], to name a few. Traditionally, passive inductors and transformers are off-chip discrete components. The need for off-chip communications with these passive components severely limits the bandwidth, reduces the reliability, and increases the cost of systems [10, 11]. Since early 1990s, a significant effort has been made to fabricate inductors and transformers on a silicon substrate such that an entire wireless transceiver can be integrated on a single substrate monolithically [12, 13]. In the mean time, the need for a large silicon area to fabricate spiral inductors and transformers has also sparked a great interest in and an intensive research on the synthesis of inductors and transformers using active devices, aiming at minimizing the silicon consumption subsequently the fabrication cost and improving the performance [14, 15].

In this chapter, the properties of spiral and active inductors, their advantages and limitations and the impact of them on the application of these devices are looked. Section 1.1 demonstrates the critical need for an inductive characteristic in high-speed applications. Then section 1.2 dicuses about spiral inductors. In section 1.3, the pros and cons of Active Inductors (AIs) are investigated. The chapter is concluded in section 1.4.

1.1 Inductive Properties in High-Speed Applications

In order to improve performance of the high-speed systems, such as improving bandwith, boosting gain , selecting frequency and matching networks, inductive charactristics are critically needed. These applications include LC tank oscillators, bandwidth enhancement in broadband communications, impedance matching in narrowband communications, phase shifting for RF antennas and radars, RF power dividers, frequency selection, in particular, RF bandpass filters, RF power amplifiers, and gain boosting of RF low-noise amplifiers. Some of the aforementioned applications are discussed briefly in upcoming subsections.

1.1.1 Bandwidth Improvement

Bandwith is a ciritical in Designing broadband circuits, such as amplifiers, matching networks and etc. The bandwidth of a circuit is set by the time constant of the critical node, i.e. the node that has the largest time constant, of the circuit. Three approaches, namely inductive peaking, current-mode signaling, and distributed amplification, are widely used to improve the bandwidth of circuits. The inductive peaking approach is discussed in next paragaragh and extra information about other approaches are fined at [16].

- Inductive peaking: The idea is to place an inductor at the node where a large nodal capacitance exists such that the first-order RC network associated with the node is replaced with a second-order RLC network. Because a RLC network has three different modes of operation, namely over damped, critically damped, and under damped. The bandwidth in these three cases differs with under-damped RLC systems exhibit the largest bandwidth. Both shunt peaking [16, 17] and series peaking [18], have been used, as shown in Figure 1.1. It was demonstrated in [16, 17] that inductive shunt peaking can improve the bandwidth of a common-source amplifier by as much as 70%. As shown in Figure 1.1(a&b), in the shunt peaking the peaking inductor L is in parallel with the dominant capacitor C and in series peaking type it is in series with the dominant C.

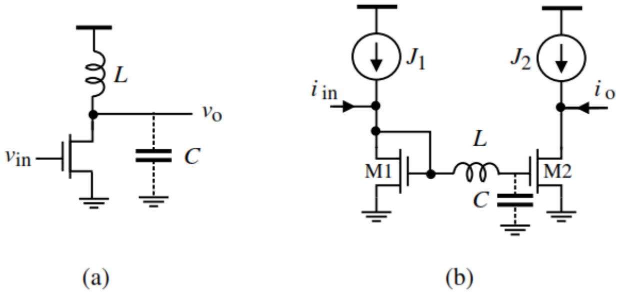


Figure 1.1 : Inductive peaking, (a) Shunt peaking, (b) Series peaking.

1.1.2 Impedance Matching

For decreasing signal reflection at interface of channels and high-speed circuits, impedance matching is required. Resistors are usually used to provide a matching impedance in broadband communication systems as impedance matching is required over a broad frequency spectrum. Frequency-dependent elements, such as capacitors and inductors, can not be used for impedance matching in broadband communication systems simply due to their frequency-dependent characteristics. But most of the communication circuits operate in a narrow-band mode. Although resistors can be used for these applications, the high level of the thermal noise of resistors limited their usage in wireless communications where there is a stringent constraint on the noise performance of these systems. Instead, noiseless and lossless elements such as capacitors and inductors are widely used in narrow-band impedance matching because these frequency-dependent noiseless elements can provide the desired impedance in a narrow frequency band and at the same time keep the noise at required level [19].

Figure 1.2 shows widely used termination scheme for narrowband Low-Noise Amplifiers (LNAs). Neglecting C_{gd} and other parasitic capacitances, the input impedance of the LNA can be written as:

$$Z_{in} = \left[j\omega(L_1 + L_2) + \frac{1}{j\omega C_{gs_1}} \right] + \frac{g_{m1}L_2}{C_{gs_1}} \tag{1.1}$$

Where C_{gs1} and g_{m1} are the gate source capacitance and transconductance of M_1, respectively. It is seen from (1.1) that reactive part of input impedance (first term) can be made zero by imposing:

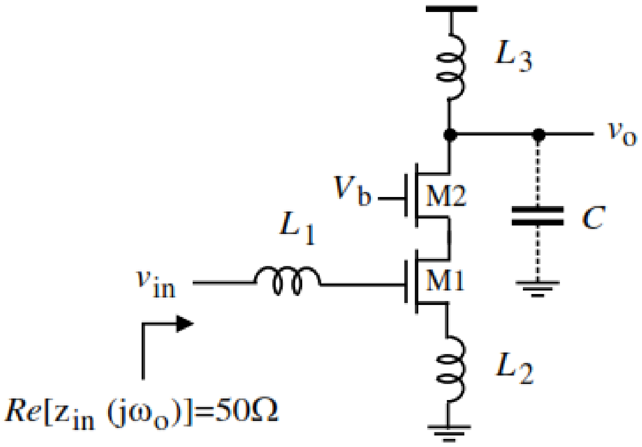


Figure 1.2 : Impedance matching in narrow-band low-noise amplifiers.

$$j\omega(L_1+L_2)+\frac{1}{j\omega C_{gs_1}}=0 \tag{1.2}$$

The input impedance of the LNA in this case becomes purely resistive and is given by:

$$Z_{in}=\frac{g_{m1}L_2}{C_{gs_1}} \tag{1.3}$$

The reason of using two inductors in gate and source of M_1 is as following: Once the dimension of M_1 is chosen, g_{m1} and C_{gs1} are determined. The desired input impedance of the LNA in this case can be obtained by adjusting L_2. Once L_2 is chosen, the value of L_1 can be tuned to ensure the total cancellation of the reactive part of the input impedance.

1.1.3 Phase Shifting

A well-designed phase shifter should possess the characteristics of a low insertion loss, a high return loss, and a large phase shift range. The common configuration of RF phase shifters is shown in Figure1.3. The tuning of the amount of the phase shift is carried out by varying the capacitance of the shunt varactors.

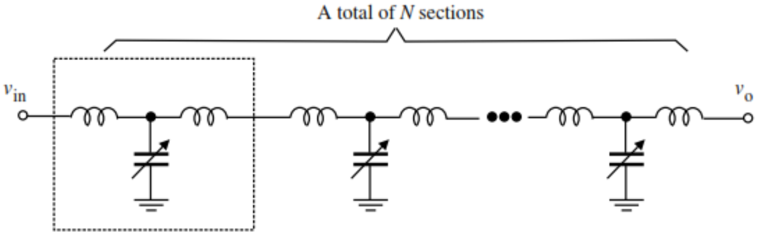


Figure 1.3 : RF phase shifters with floating inductors and shunt varactors.

1.1.4 Frequency Selection

Frequency selection systems are implemented by lumped elements. For instance, Bandpass Filters (BPFs) with a high passband center frequency are used extensively in narrow-band wireless communications for RF band selection. Implementing inductors with antiont approaches are not compatible with CMOS technologies, which are domimnant in Radio Frequency Integrated Circuit (RFIC) designing. The recent effort on integrating RF BPFs on a silicon substrate is accelerated with the emergence of CMOS passive and active inductors. A single-chip realization of RF transceivers with on-chip RF BPFs offers a number of critical advantages including a reduced assembly cost, increased system reliability, and improved performance. Table 1.1 tabulates some recently reported RF bandpass filters with CMOS spiral and active inductors.

Table 1.1 : BPF with CMOS spiral and active inductors.

Ref.	Year	Tech. (µm)	f_0 (GHz)	Filter order	Inductor type
[6]	2002	0.18	1.75	3	spiral
[20]	2002	0.25	2.14	3	spiral
[21]	2010	0.09	3.46	2	active
[22]	2012	0.18	0.6	3	active
[23]	2011	0.13	0.6	1	active

1.1.5 Gain Boosting

Traditional gain-boosting techniques such as cascodes and regulated cascodes lose their potency at high frequencies due to the increased gate-source and gate-drain couplings via the gate-source and gate-drain capacitors of MOSFETs. A technique that is widely used in boosting the voltage gain of narrowband low-noise amplifiers (LNAs) is to use a LC tank as the load of the LNAs [24, 25], utilizing the infinite impedance of ideal LC tanks at their self-resonant frequency. When a LC tank is used as the load of a common-source amplifier whose voltage gain is approximated by $A_v \approx -g_m Z_L$, where g_m is the transconductance of the MOSFET and Z_L is the load impedance, as shown in Figure1.4, the large impedance of the LC tank at its self-resonant frequency $\omega_0 = \frac{1}{\sqrt{L_p C}}$ will significantly boost the gain of the amplifier at ω_0. The resonant frequency of the tank is set to be the same as the frequency of the input of the LNA. Note that voltage gain of the amplifier at frequencies other than ω_0 is low.

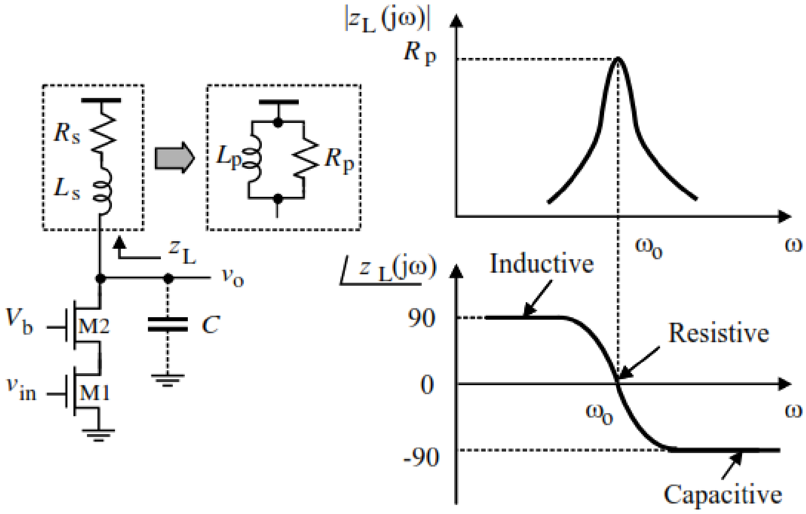


Figure 1.4 : Gain boosting of low noise amplifiers using LC tank load.

1.1.6 Power Divider

Usaully, transmission lines are employed to implement power dividers. But in order to reduce the size of the structure, lumped elements is used to construct power dividers at the cost of a high insertion loss and a limited bandwidth. Equivalent circuit of the lumped Wilkinson power divider is depicted in Figure 1.5. Replacing passive spiral inductors with CMOS AIs brings the advantages of the high quality factor, low silicon consumption, and high self-resonant frequency [26, 27].

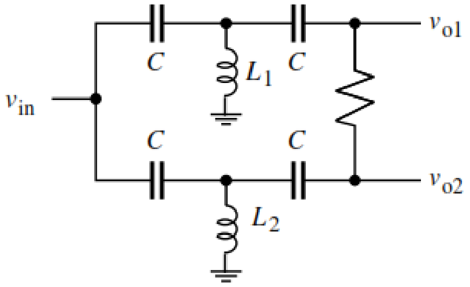
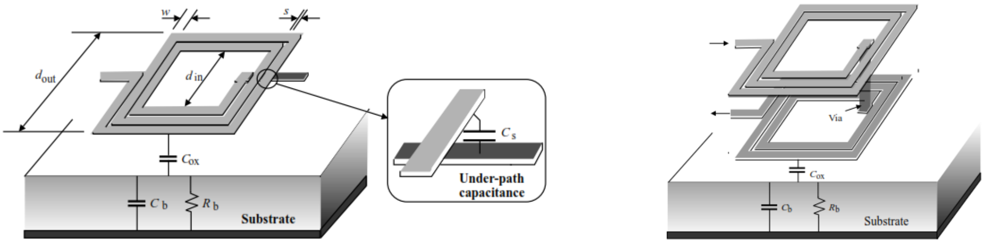


Figure 1.5 : Equivalent circuit of lumped Wilkinson power divider.

1.2 Spiral Inductors

Monolithic on-chip inductors are also known as spiral inductors due to the way in which these inductors are laid out. Both planar and stacked spiral inductors have been illustraded in Figure 1.6(a&b). Modern Computer Aided Design (CAD) tools for Integrated Circuit (IC) design are equipped with spiral inductors as standard elements in their component libraries.



(a) (b)

Figure 1.6 : Spiral Inductors (a) planar (b) stacked.

Spiral inductors offer the key advantages of superior linearity and a low level of noise. The performance and applications of spiral inductors are affected by a number of drawbacks that are intrinsic to the physical geometry of these passive devices and CMOS technologies in which spiral inductors are implemented. These drawbacks include:

- **Low quality factor -** The Quality Factor (QF) of spiral inductors and transformers is limited by the ohmic loss of the spiral at high frequencies. Two sources that contribute to the ohmic loss of the spiral inductors and transformers exist: the skin-effect induced resistance of the spiral and the resistance induced by the eddy currents in the substrate.
- **Low self-resonant frequency** - The self-resonance of a spiral inductor is the resonance of the LC tank formed by the series inductance of the spiral inductor and the shunt capacitance between the spiral of the inductor and the substrate, as well as its underpass capacitance. The low Self-Resonant Frequency (SRF) of spiral inductors is mainly due to the large spiral-substrate capacitance, arising from the large metal area occupied by the spiral.
- **Large silicon area** - Due to the low inductance of spiral inductors, especially planar spiral inductors, and the fact that the inductance of these inductors is

directly proportional to the number of the turns of the spiral of the inductors, the silicon area required for routing the spiral of the inductors is large.

1.3 Active Inductors

AIs are mainly implemented by CMOS transistors which are main elements of electronic systems in recent years. Many architecture are used to improve the performance of AIs such as feedback, cascode stage and Feed Forward Path (FFP). Under certain DC biasing conditions and signal-swing constraints, these networks exhibit an inductive characteristic in a specific frequency range. The main advantages of AIs which push the designer to use them instead of their spiral counterparts, are as follow:

- **Low silicon consumption** - Because only MOS transistors are usually required in the realization of CMOS AIs and the inductance of these active inductors is inversely proportional to the transconductances of the transistors, the silicon consumption of CMOS active inductors is negligible as compared with that of their spiral counterparts.
- **Large and tunable SRF** - CMOS AIs have high SRF. For example, the passband center frequency of an active inductor RF bandpass filter is typically set to the SRF of the active inductor of the filter. The larger the SRF of the active inductor, the higher the passband center frequency of the filter. A large SRF of AIs ensures that the active inductors will have an inductive behavior over a large frequency range.
- **Large and tunable inductance** - As to be seen in Chapter 2, the inductance of CMOS AIs is inversely proportional to the transconductances of the transistors synthesizing the inductors. The smaller the width of the transistors, the larger the inductance. Also the inductance can be tuned conveniently by varying the DC biasing condition of the transistors synthesizing the inductor with a large inductance tuning range. Additionaly, fine tuning of the inductance can be achived by varying the load capacitance of the transconductors.
- **Large and tunable QF** - The QF of CMOS AIs is set by the ohmic loss of the inductors, arising mainly from series resistance of AI. This resistance comes from the finite output resistance of the transconductors of the inductors. Thus QF

can be increased by increasing output resistance of the transcoductors. A number of methods are available to boost the output resistance, such as cascodes, regulated cascodes, and negative resistor compensation.

- **Highly compatibility with CMOS technology** – Spiral inductors are existing in mixed mode technology. However, AIs are compatible with all CMOS process.

These kinds of inductors have found many applications such as oscillators, RF filters, RF phase shifters, LNAs, RF power dividers, communication systems and matching networks. Table 1.2 declares some recently published applications which were employed CMOS AIs.

Table 1.2 : Recent publish applications of CMOS AIs.

Ref.	Year	Tech.	application	Remark
[28]	2012	0.09 µm	LC VCO	13 GHz
[29]	2015	0.18 µm	TAI VCO	0.6-7.2 GHz
[30]	2011	0.13 µm	VCO	0.833-3.72 GHz
[32]	2015	0.18 µm	Matching network	0-6.9 GHz
[31]	2009	0.18 µm	LNA	0.375-2.18 GHz
[34]	2013	0.18 µm	LNA	0.8-2.5 GHz
[33]	2015	0.18 µm	LNA	3.1-10.6 GHz
[35]	2013	0.09 µm	Bandpass Filter	0.8-6 GHz
[36]	2011	0.18 µm	Power divider	5.8-10.4 GHz

These AIs in mentioned applications are influenced by some difficulties such as: limited dynamic range, high level of noise, high sensitive to process variations and supply sources fluctuation. These difficulties arise from the intrinsic characteristics of CMOS devices. Fortunately, the effect of many of these difficulties can be reduced through innovative designs and proper circuit configurations. For example, the limited dynamic range of active inductors can be expanded using class AB configurations [36]. The process variation can be compensated by tuning the inductance and QF [38] and the effect of noise can be decreased by noise cancellation configuration [37]. The developing utilizations of CMOS AIs keep on improving alongside the origin of new design strategies and circuit topologies.

1.4 Conclusion

Due to explanations, it is obvios that inductive charactristics are very crutial in many applications especially in RF. It is shown that integrated spiral inductors suffer from a low quality factor, a low SRF, a low and fixed inductance, and the need for a large silicon area. Meanwhile, CMOS AIs offer a number of attractive characteristics as compared with their spiral counterparts. These characteristics include a low silicon consumption, a large and tunable SRF, a large and tunable inductance, a large and tunable QF and etc. Also, AIs are employed to implement many electronic circuits' blocks such as LNAs, Power Amplifiers (PAs), filters, power dividers, Voltage Control Oscillators (VCOs) and matching networks.

The utilizations of AIs are influenced by a few difficulties emerging from the intrinsic properties of CMOS devices including limited dynamic range, high level of noise, high sensitivity to process variations and supply voltage fluctuations. By using some advanced circuit design techniques and developing the process technology, many of these difficulties can be overcome.

1.5 Dissertation Organization

In chapter 2, the principles, topologies, characterizations and implementation of the gyrator-C is discussed in-depth. The GC networks which are implemented by Operational transconductance amplifier are suitable for RF application. This property arises from their minimum usage of active elements. It is shown that both grounded and floating active inductor can be implemented by gyrator-C networks. To provide a quantitative measure of the performance of active inductors, a number of figure-of-merits have been introduced. These figure-of-merits include frequency range, inductance tunability, quality factor, noise and power consumption. One of the key advantages of active inductors over their spiral counterparts is the large tunability of their inductance. The inductance of gyrator-C active inductors can be tuned by varying either the transconductances of the transconductors or the load capacitance which is implemented by MOS varactor

In chapter 3, new grounded and floating AIs are designed by using advanced circuit techniques. For lowering conductance in input and output nodes of AI, Multi-Regulated Cascode (MRC) stages are employed to Q enhancement purpose. Theoretical analysis and post-layout simulation results shows the effectiveness of using MRC stages usage in properties of AI. Also, these stages are utilized to design high Q floating AI.

Designers do their best to improve SRF and QF, two main characteristics in term of AI performance. An AI with ability to adjust its SRF and QF without affecting each other is designed and simulated. The cascoding and RC feedback structures are used in the new design of AI. As it discussed before, input transistor is very important regarding to AI characterizations. Cascoding input transistor gives the ability to adjust the first gyrator’s transconductance and input parasitic capacitance independently. Furthermore, the inductance value can be adjusted by other transistor’s transconductance. The RC feedback is utilized to cancel the parasitic series-resistance of AI which results in QF enhancement. Since, bias condition of cascoding transistors is provided by a diode-connected transistor, the proposed structure is robust in terms of performance over variation in process, voltage and temperature.

The Noise of designed AIs has limited the use of them in RF applications such as LNAs. The main noise source of an AI is its input transistor. In order to have low noise AI, the input transistor should be designed large enough. But it leads to low SRF which limited the inductive frequency band. A low-noise and low-loss AI is presented suitable for RF low noise applications. Utilizing all transistors in CS configuration on the AI circuit leads to low conductance nodes which it causes to high Q AI. P-type MOS transistors and Feed-Forward Path (FFP) are employed to decrease noise of the AI, respectively.

In chapter 4, GC network in 3 applications are presented. The capacitive based micro sensors convert mechanical signals to small capacitance variation. The capacitance variation in micro sensor is in the range of femto-Farads which makes it difficult to sense. On the other hand, the Gyrator-C topologies can convert a low capacitance variation to high impedance change which makes it a good choice for being interface circuits for capacitive sensors. Then a new 3-axis accelerometer with ability to cancel cross section sensitivity is designed. The sensor’s electrodes are located in such a way that enables the structure to detect acceleration in all axis independently. Consequently, a new GC configuration for sensing very small capacitance changes in a capacitive sensor is presented. In the proposed configuration, the operating frequency range and Scaling Factor can be adjusted without affecting each other by tuning the bias currents. In addition, the proposed configuration employs RC feedback and cascoding techniques to cancel the effect of the parasitic components.

Finally, in order to show versatility of designed AIs, they are used in designed third and sixth order broadband microwave filters. The first one is a third order Chebyshev low pass filter. The second one which is designed by using simplified real frequency technique is a sixth order Chebyshev band pass filter. The simulated frequency response of filters prove the workability of the designed AIs.

Finally, dissertation is concluded in chapter 5 and some scopes for future works are given.

2. CMOS ACTIVE INDUCTORES

This chapter provides a background overview of the principles, topologies, characteristics, and implementation of CMOS active inductors. First, the principles of gyrator-C based synthesis of inductors are explained. Both grounded and floating configuration of Gyrator-C (GC) AIs are investigated. Section 2.2 diclares salient features of AI such as frequency range, inductance tunability, Quality Factor (QF), noise, stability and etc, which quantify the performance. Sections 2.3 and 2.4 detail the CMOS implementation of grounded and floating AIs, respectively. The chapter is summarized in Section 2.5.

2.1 Principles of Gyrator-C Active Inductors

2.1.1 Ideal (lossless) Grounded Gyrator-C Active Inductors

A gyrator consists of two back-to-back connected transconductors. When one port of the gyrator is connected to a capacitor, as shown in Figure 2.1, the network is called the GC network.

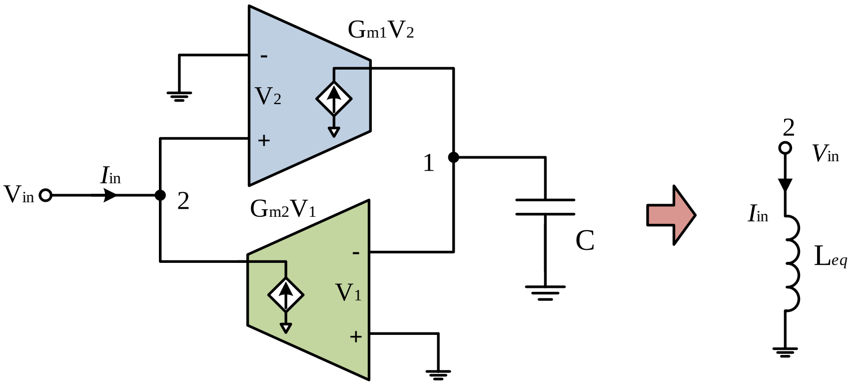


Figure 2.1: Ideal grounded GC AI.

According to the ideal GC network shown in Figure 2.1, the input admittance is calculated as:

$$Y = \frac{I_{in}}{V_{in}} = \frac{1}{s\left(\frac{C}{G_{m1}G_{m2}}\right)} \tag{2.1}$$

Equation (2.1) indicates that port 2 of the GC network behaves as a grounded ideal inductor, which its inductance value is given by:

$$L = \frac{C}{G_{m1}G_{m2}} \tag{2.2}$$

Thus, GC can be used to synthesize inductors. The inductance of GC AI is directly proportional to the load capacitance C and inversely proportional to the product of the transconductances of the transconductors of the gyrator.

Although the transconductors of GC networks can be configured in various ways, the constraint that the synthesized inductors should have a large frequency range, a low level of power consumption, and a small silicon area requires that these transconductors be configured as simple as possible. Figure 2.2 shows the simplified schematics of the basic transconductors that are widely used in the configuration of GC AIs. Common-Gate (CG), Common-Drain (CD), and differential-pair transconductors all have a positive transconductance while the Common-Source (CS) transconductor has a negative transconductance [89].

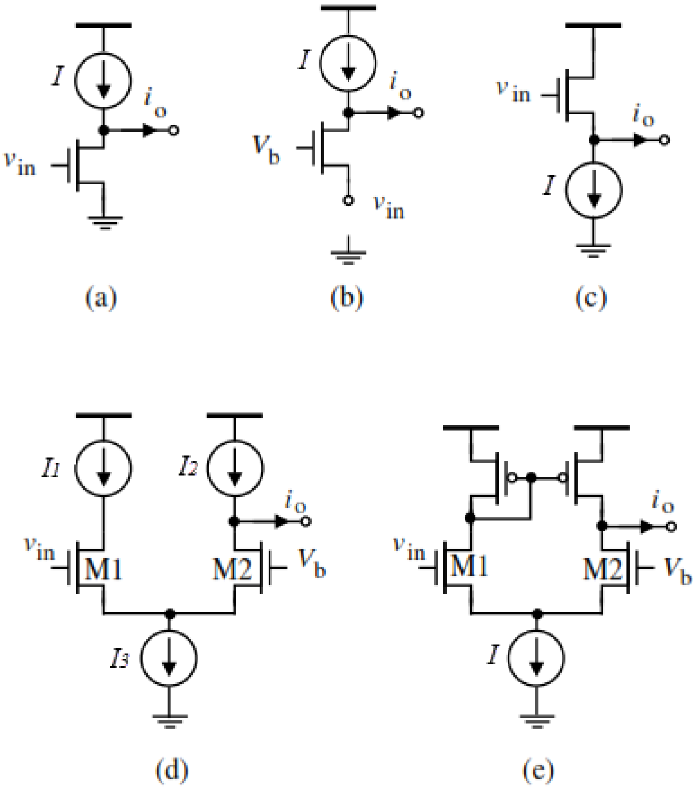


Figure 2.2: Simplified schematic of basic transconductors. (a) CS ($\boldsymbol{i_o = -g_m v_o}$), (b) CG ($\boldsymbol{i_o = g_m v_o}$), (c) CD ($\boldsymbol{i_o = g_m v_o}$), (d, e) differential-pair ($\boldsymbol{i_o = g_m v_o}$).

2.1.2 Ideal Floating Gyrator-C Active Inductors

A Floating Active Inductor (FAI) has floating terminals, which are not connected to ground. Floating GC AIs can be designed by replacing single-ended transconductors with differentially-configured transconductors, as depicted in Figure 2.3 [89]. Because

$$V_{in1}^{+} = -\frac{g_{m1}}{sC}(V_{in2}^{+} - V_{in2}^{-}),\ V_{in1}^{-} = \frac{g_{m1}}{sC}(V_{in2}^{+} - V_{in2}^{-}) \tag{2.3}$$

$$I_{o2} = g_{m2}(V_{in1}^{+} - V_{in1}^{-}) \Rightarrow I_{o2} = -\frac{2g_{m1}g_{m2}}{sC}(V_{in2}^{+} - V_{in2}^{-}) \tag{2.4}$$

Thus, the input admittance is given by

$$\mathrm{Y} = \frac{I_{in}}{V_{in2}^{+} - V_{in2}^{-}} = \frac{1}{s(\frac{2C}{g_{m1}g_{m2}})} \tag{2.5}$$

Equation (2.5) reveals that the GC network in Figure 2.3 behave as a floating inductor with the value of:

$$L = \frac{2C}{g_{m1}g_{m2}} \tag{2.6}$$

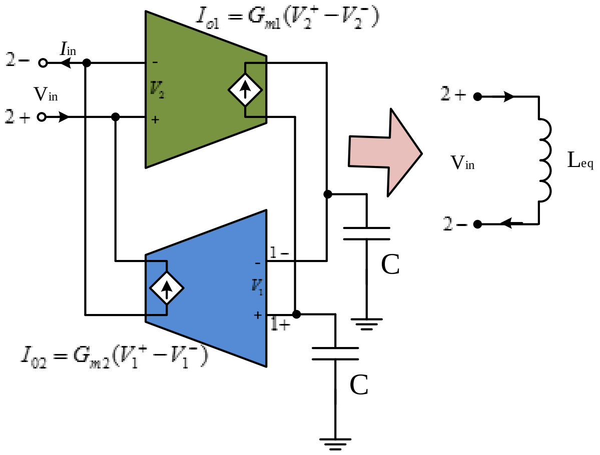


Figure 2.3: Ideal (lossless) Floating GC AI.

The Floating Active Inductors (FAIs) have some attractive advantages in constract with their Grounded Active Inductors (GAIs) counterparts like:

- Their diffirentional configuration leads to reject of common-mode disturbances of AI which make is suitable for mixed signal applications.
- The voltage swing of FAIs is twice than their GAIs counterpart.

2.1.3 Lossy Grounded Gyrator-C Active Inductors

In practical, the AIs do not have inductive behavior in all frequency spectrum due to their parasitic components in input/output nodes. Consider the lossy GC GAI shown in Figure 2.4, where G_{oi} and C_i are parasitic conductance and capacitance in ith node, respectively.

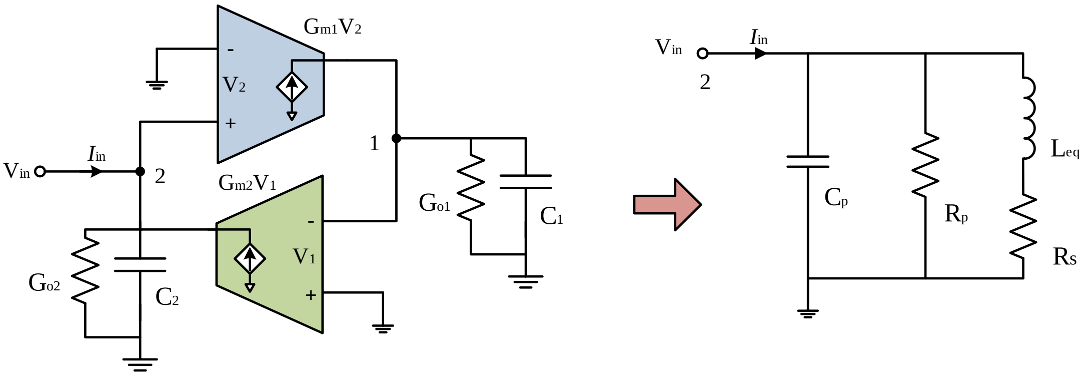


Figure 2.4: Block diagram of GAI realization and its equivalent passive model.

The transconductances of transconductors are assumed constatnt to have simplify analysis. The admittance looking into port 2 of GC topology is calculated as:

$$Y_{in} = \frac{1}{Z_{in}} = \frac{I_{in}}{V_{in}} = sC_2 + G_{o2} + \frac{1}{s(\frac{C_1}{G_{m1}G_{m2}}) + \frac{G_{o1}}{G_{m1}G_{m2}}} \tag{2.7}$$

Equation (2.7) indicates that the GAI can be modeled by a RLC network (Figure 2.4) which its elements value are obtained as:

$$\begin{aligned} R_p &= \frac{1}{G_{02}}, \qquad \mathrm{R}_s = \frac{G_{o1}}{G_{m1}G_{m2}}, \\ C_p &= C_2, \qquad \mathrm{L}_{eq} = \frac{C_1}{G_{m1}G_{m2}} \end{aligned} \tag{2.8}$$

As it can be seen from the equivalent model values, in order to have low ohmic loss R_p should be maximized and R_s should be minimized. The finite input and output impedances of the transconductors of the GC network, however, have no effect on the inductance of the AI. The finite input and output impedances of the transconductors constituting active inductors result in a finite quality factor. For applications such as band-pass filters, active inductors with a large quality factor are mandatory. In these cases, Q-enhancement techniques that can offset the detrimental effect of R_p and R_s

should be used to boost the QF. The resonance frequency of the RLC network of the AI is given by:

$$\omega_0 = \sqrt{\frac{1}{C_p L_{eq}}} = \sqrt{\frac{G_{m1}G_{m2}}{C_2 C_1}} \tag{2.9}$$

ω_0 is the Self-Resonance Frequency (SRF) of the AI. The SRF defines the upper limit of the frequency band range, which AI operates. In other words, the SRF of an AI is set by cut-off frequency of the transconductances which constructing it.

2.1.4 Lossy Floating Gyrator-C Active Inductors

Floting type of GC AI can be analyzed in similer way of GAIs in 2.1.3 section. Figure 2.5 depicts the lossy floating GC network and its passive equivalent model. Calculating the input admittance in port 2 gives:

$$Y_{in} = \frac{1}{Z_{in}} = \frac{I_{in}}{V_{in}} = s\frac{C_2}{2} + \frac{G_{o2}}{2} + \frac{1}{s(\frac{C_1}{2G_{m1}G_{m2}}) + \frac{G_{o1}}{2G_{m1}G_{m2}}} \tag{2.10}$$

Investigation of equation (2.10) shows that it equivalent with RLC network which its parameters given by:

$$\begin{aligned} R_p &= \frac{2}{G_{02}}, & \mathrm{R}_s &= \frac{G_{o1}}{2G_{m1}G_{m2}}, \\ C_p &= \frac{C_2}{2}, & \mathrm{L}_{eq} &= \frac{C_1}{2G_{m1}G_{m2}} \end{aligned} \tag{2.11}$$

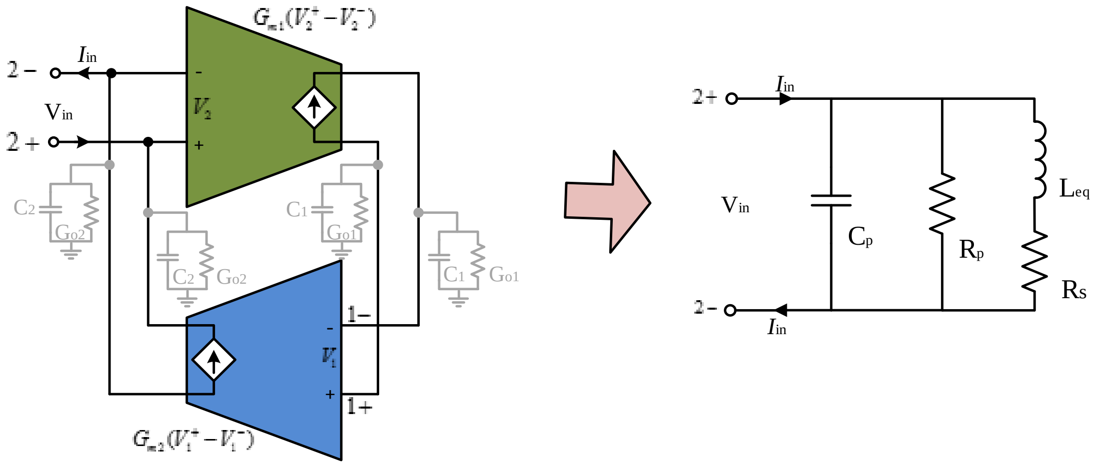


Figure 2.5: Block diagram of FAI realization and its equivalent passive model.

The constant in (2.11) is due to the floating configuration of the AI.

2.2 Active Inductor Properties

The most important properties of AIs which quantify its performance is discussed in this section. They are such as frequency range, inductive tunability, QF, noise, stability and etc.

2.2.1 Frequency Range

It was shown in the preceding section that a lossy GC AI only exhibits an inductive characteristic over a specific frequency range. This frequency range can be obtained by examining the impedance of the RLC equivalent circuit of the lossy active inductor which its input impedance can be calculated as:

$$Z_{in} = \left(\frac{R_s}{C_p L_{eq}}\right) \frac{s\frac{L_{eq}}{R_s}+1}{s^2 + s\left(\frac{1}{R_p C_p} + \frac{R_s}{L_{eq}}\right) + \frac{R_p + R_s}{R_p C_p L_{eq}}} \tag{2.12}$$

When complex conjugate poles are encountered, the pole resonant frequency of Z_{in} is given by:

$$\omega_p = \sqrt{\frac{R_p + R_s}{R_p C_p L_{eq}}} \tag{2.13}$$

Because $R_p \gg R_s$, Eq. (2.13) is simplified to:

$$\omega_p \approx \sqrt{\frac{1}{C_p L_{eq}}} = \omega_0 = SRF \tag{2.14}$$

where, ω_0 is the self-resonant frequency of the active inductor. Also observe that Z_{in} has a zero at the frequency

$$\omega_z = \frac{R_s}{L_{eq}} = \frac{G_{o1}}{C_1} \tag{2.15}$$

The Bode plots of Z_{in} are sketched in Figure 2.6. It is evident that the gyrator-C network is resistive, when $\omega \leq \omega_z$, inductive when $\omega_z \leq \omega \leq \omega_0$, and capacitive when $w \geq w_0$. The frequency range in which the GC network is inductive is lower-bounded by ω_z and upper-bounded by ω_0. Also it is observed that R_p has no effect on the frequency range of the active inductor. R_s, however, affects the lower bound of the frequency range over which the GC network is inductive. The upper bound of the frequency range is set by the SRF of the AI, which is set by the cut-off frequency of the transconductors constituting the active inductor. For a given inductance L_{eq}, in order to maximize the frequency range, both R_s and C_p should be minimized.

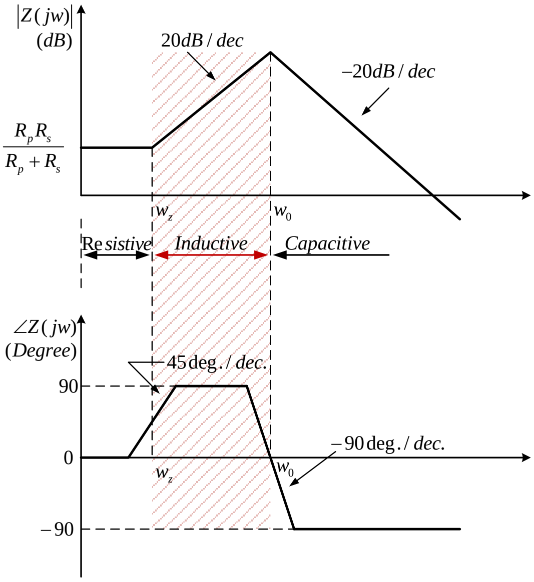


Figure 2.6: Bode plots of the impedance of lossy Gyrator-C AI.

2.2.2 Inductance Tunability

Inductance tunability is required in many applications such as phase-locked loops, Voltage Controlled Oscillators (VCOs) and filters. The salient feature of GC AIs is that their inductance value can be tuned not only by changing the load capacitance but also by varying the transconductances of the transcondutors.

Varactors are employed as tunable capacitors in CMOS technology. Two types of varactors exists, namely pn-junction varactors and MOS varactors. The MOS type is usually used in circuits which are implemented by transistors. Figure 2.7 exhibits the sideview of accumulation-mode MOS varactors. A key advantage of accumulation-mode MOS varactors is the large voltage swing across the terminals of the varactors.

They are the most widely used varactors in voltage/current-controlled oscillators. Figure 2.8 shows the capacitance variation in MOS varactors [89].

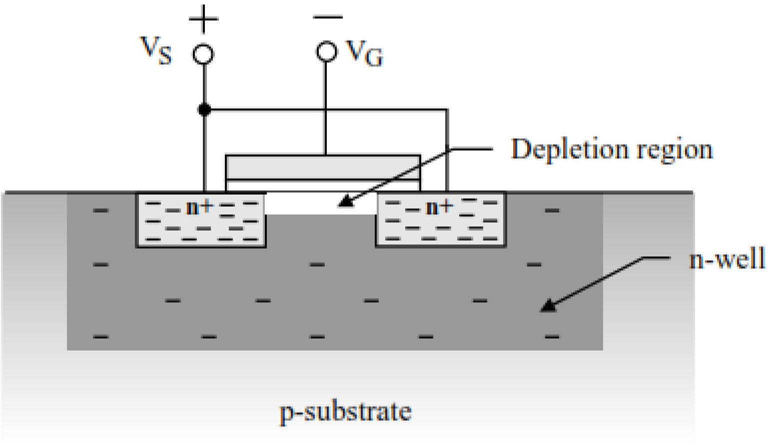


Figure 2.7: Sideview of MOS varactors.

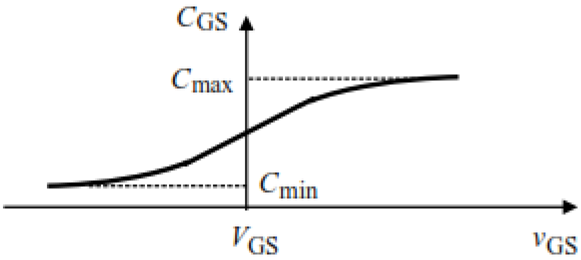


Figure 2.8: Capacitance variation in MOS varactors.

Bias variation is used to transcoductance tuning of transconductores in GC topology of AIs. This approach offers a large conductance tuning range, subsequently a large inductance tuning range. The conductance tuning range is set by the constraint that the transconducting transistors of the transconductors must remain in the saturation. Consequently, conductance varying is used for large inductance variation while load capacitance changing is used for small inductance variation (Figure 2.9). The conductance tuning range is set by the pinch-off condition while the capacitance tuning range is set by the range of the control voltage of the varactors.

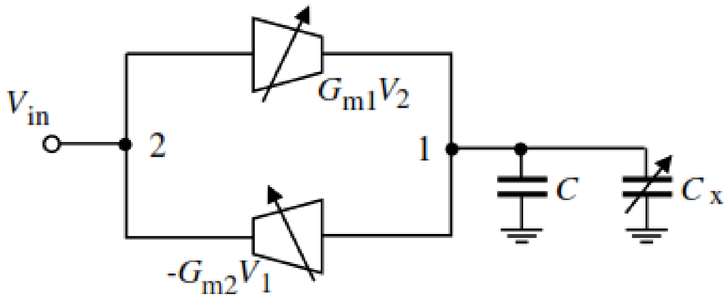


Figure 2.9: Inductance tuning via transconductances or load capacitance variation.

It is obvious that the transconductance variation will affect the parasitic series resistance of AI. This is echoed with a change in the quality factor of the active inductors. The variation of the quality factor due to the tuning of L must therefore be compensated for such that L and Q are tuned independently. The load capacitance changing does not affect the QF of AI.

2.2.3 Quality Factor

High QF is the most salient feature of AIs in contrast with their Passive Spiral Inductors (PSIs). It is independent from voltage/current of PSIs but it is not valid for AIs. The QF of an inductor quantifies the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle. Equation (2.16) convenient way to quantify the Q of linear inductors including AIs.

$$Q=\frac{\mathrm{Im}[Z]}{\mathrm{Re}[Z]} \tag{2.16}$$

Active inductors are linear when the swing of the voltages/currents of the inductors are small and all transistors of the active inductors are properly biased. The quality factor of a lossy gyrator-C active inductor can be derived directly from (2.12) and (2.16).

$$Q=(\frac{\omega L_{eq}}{R_s})\frac{R_p}{R_p+R_s[1+(\frac{\omega L_{eq}}{R_s})^2]}[1-\frac{R_s{}^2C_p}{L_{eq}}-\omega^2C_pL_{eq}] \tag{2.17}$$

It is clear from (2.17) QF is mostly dependent on R_s and R_p. Furthermore, it is seen that the first term of (2.17) ($\frac{\omega L_{eq}}{R_s}$) is dominant part of QF in AI. So, it is used to quantify the QF of AIs. Thus R_s must be taken to account in boosting the QF. There are many many approaches to reduce series resistance of AIs such as:

- Reducing the conductance of node (1) in Figures 2.4 and 2.5 by using advace circuit techniques such as cacoding
- Increasing the transconductances of transconductors
- Using negative resistance circuit

2.2.4 Noise

The most important drawback of AIs in comparison with the SPIs are their high level of noise. In order to investigate the noise of GC based AI, the input-referred noise voltage or current should be carried out. In order to show how the input referred noise power, common-gate, basic building blocks of transconductor which is used to construct GC AIs, is depicted in Figure 2.10. The power of the input-referred noise-voltage generator, denoted by $\overline{v_n^2}$, and that of the input-referred noise-current generator, denoted by $\overline{i_n^2}$, of these transconductors can be derived using conventional noise analysis approaches for 2-port networks [39].

To extract $\overline{v_n^2}$ of the transconductor, we first short-circuit the input of the transconductor, as shown in Figure 2.10.

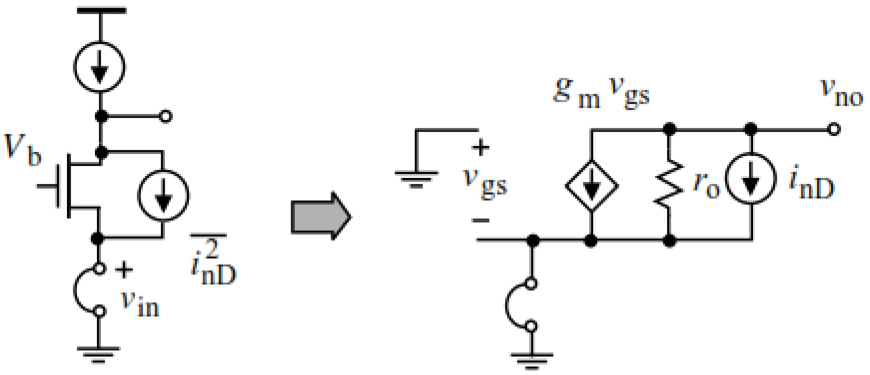


Figure 2.10: deriving the input-referred noise voltage of CG transconductor.

The output noise power of the transconductor due to i_{nD} is obtained as:

$$\overline{v_{no}^2} = r_o^2 \overline{i_{nD}^2} \qquad (2.18)$$

where r_o is the output resistance of the transistor. Then, $\overline{i_{nD}^2}$ is removed and v_n is applied at the input of the transconductor, as shown in Figure 2.10. The output noise power of the transconductor is obtained as:

$$\overline{v_{no}^2} = (1 + g_m r_o)^2 \overline{v_n^2} \tag{2.19}$$

Equating (2.18) and (2.19) yields:

$$\overline{v_n^2} = \frac{r_o^2}{(1 + g_m r_o)^2} \overline{i_{nD}^2} \approx \frac{1}{g_m^2} \overline{i_{nD}^2} \tag{2.20}$$

Once $\overline{v_n^2}$ and $\overline{i_n^2}$ of the transconductors are available, the power of the input referred noise-voltage and noise-current generators of active inductors can be derived.

2.2.5 Stability

GC base active inductors are negative feedback systems. The stability of active inductors is critical to the overall stability of systems employing active inductors. In this section, we investigate the stability of gyrator-C active inductors.

The impedance looking into port 2 of the gyrator-C active inductor shown in Figure 2.4 is given by:

$$Z = \frac{sC_1 + G_{o1}}{s^2 C_1 C_2 + s(C_1 + C_2) + G_{m1} G_{m2}} \tag{2.21}$$

where we have utilized $G_m \gg G_o$ to simply the results. The poles of the system are given by:

$$p_{1,2} = \frac{C_1 + C_2}{2C_1 C_2} \left[-1 \pm \sqrt{1 - \frac{4C_1 C_2 G_{m1} G_{m2}}{(C_1 + C_2)^2}} \right] \tag{2.22}$$

The poles of the gyrator-C active inductor are located in the left half of the s-plane and the gyrator-C active inductor is a stable system.

The degree of stability can be assessed by evaluating its damping factor, which is obtained by comparing the denominator of (2.2) with the standard form of the characteristic equation of second-order systems:

$$s^2 + 2\omega_0 \xi s + \omega_0{}^2 = 0 \tag{2.23}$$

whrer ε denotes the damping factor and ω_0 is the pole resonant frequency. The result is given by:

$$\xi = \frac{1}{2\sqrt{G_{m1}G_{m2}}}\left(\sqrt{\frac{C_2}{C_1}} + \sqrt{\frac{C_1}{C_2}}\right) \tag{2.24}$$

Eq.(2.24) reveals that an increase in G_{m1} and G_{m2} will lead to a decrease in ε. This is echoed with an increase in the level of oscillation in the response of the active inductor. Also observed from (2.24) is that the ratios $\frac{C_1}{C_2}$ and $\frac{C_2}{C_1}$ have a marginal impact on the damping factor simply because these two quantities vary in the opposite directions when C_1 and C_2 change, and the values of C_1 and C_2 are often close.

If $C_1 = C_2 = C$ and $G_{m1} = G_{m2} = G_m$ we have:

$$p_{1,2} = \frac{1}{C}(-1 \pm \sqrt{1+G_m^2}), \quad \xi = \frac{1}{G_m} \tag{2.25}$$

An increase of G_m will lead to a decrease of ε. This is echoed with a reduced level of damping. Because $\lfloor p_{1,2} \rfloor = -\frac{1}{C}$, the absolute stability margin is set by the capacitance C and is independent of G_m. It should be noted that the preceding analysis is based on the assumption that active inductors are 2nd-order systems. When the parasitics of MOSFETs are accounted for, active inductors are no longer 2nd-order systems and their stability will deteriorate.

2.2.6 Power Consumption

CMOS AIs consume dc power, mainly due to their dc biasing currents. The power consumption of gyrator-C active inductors themselves is usually not of a critical concern because the inductance of these inductors is inversely proportional to the transconductances of the transcenductors constituting the inductors. To have a large inductance, G_{m1} and G_{m2} are made small. This is typically achieved by lowering the dc biasing currents of the transconductors. But for boosting the QF, an extra part such as negative resistor is added to AI circuit. This cause power consumption increasing. Furthermore, replica biasing is needed for high performance AI which it causes power consumption increasing too. Often the power consumption of an active inductor is set by that of its replica-biasing and negative resistor networks.

2.3 CMOS Grounded AI Impelementation Base on Gyrator-C Topology

For RF applications high SRF inductors are required thus usually GC topology is selected for implementation CMOS circuit of AIs. Consequently, the configuration of transcoductors which construct the AI, should be as simple as possible. This also lowers their level of power consumption and reduces the silicon area required to fabricate the inductors. Most reported GC AIs employ a common-source configuration as negative transconductors, common-gate, source follower, and differential pair configurations as positive transconductors. These basic transconductors have the simplest configurations subsequently the highest cutoff frequencies and the lowest silicon consumption.

Base on GC topology, there are many reported CMOS AI circuits in literature. All of them have tried to invent high performance AI by using different techniques. In this section, some of them are reviewed.

2.3.1 Active Inductors Proposed by Yodprasit-Ngarmnil

As discussed before to obtain high Q AI, the effect of series and parallel parasitic resistors must be compensated for. The $L - R_s$ branch in RLC model of AI can be replaced by $\hat{L} - \widehat{R_p}$ parallel branch as shown in Figure 2.11 [40].

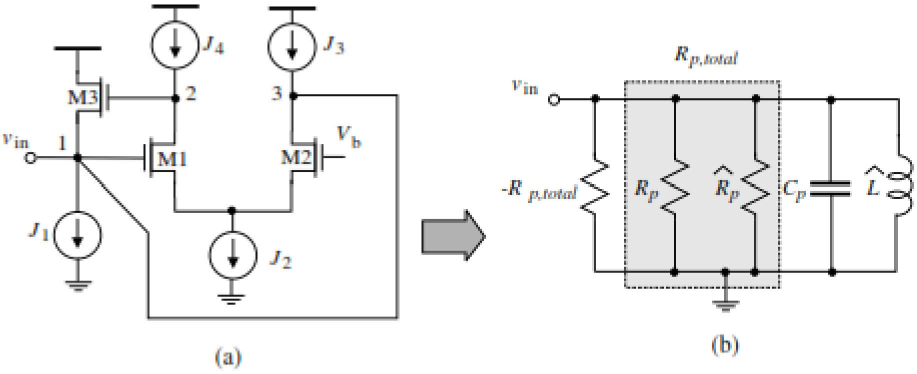


Figure 2.11: Yodprasit-Ngarmnil’s AI and its passive model [40].

The value of modified elements value are calculated as:

$$\hat{L} = L(1+\frac{1}{Q^2})$$
$$\hat{R}_p = R_p(1+Q^2) \tag{2.26}$$

The total modified parallel resistor value will become:

$$\hat{R}_{p,total} = R_p \| \hat{R}_p \tag{2.27}$$

If a negative resistor is added in parallel with the value of $-R_{p,total}$, the resistive loss of the AI vanishes completely. Negative resistor is realized by using positive feedback. In Figure 2.11(a), the added electrical connection between the input terminal of the active inductor and the drain of M_2 forms the needed positive feedback. The impedance looking into the gate of M_1 at low frequencies is given by:

$$Z_{in} \approx -(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}) \tag{2.28}$$

The preceding analysis reveals that the differential pair offers two distinct functions simultaneously. First, it behaves as a transconductor with a negative transconductance to construct the gyrator-C active inductor. Second, it provides the needed negative resistance between the input terminal and the ground to cancel out the parasitic resistances of the active inductor. It was shown in [40] that the quality factor of Yodprasit-Ngarmnil active inductor is given by:

$$Q = \frac{\sqrt{g_{m3} g_{m1} c_{gs3} c_{gs1}}}{\frac{c_{gs1}}{r_{o1}} + \frac{2c_{gs3}}{r_{o3}}} \tag{2.29}$$

It can be seen from (2.29) that the channel length modulation effect models the resistive loss of the inductor and hence a limitation on Q-factor enhancement. Nevertheless, the negative resistance can be deliberately tuned to overcome the need for very high drain-source resistance in Q-enhancing scheme. In order to facilitate the Q tuning, M_2 and M_3 are cascaded (as shown in Figure 2.12) for adjusting output resistor of transistors.

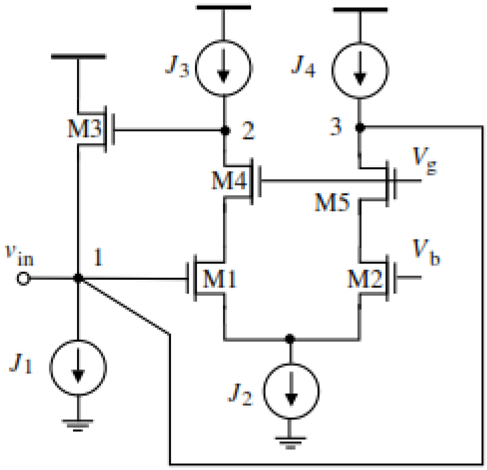


Figure 2.12 : Cascode double-feedback active inductor [40].

In that way the conductance in nodes 2 and 3 are lowered and Q enhancement is obtained.

2.3.2 Active Inductor Proposed by Uyanik-Tarim

AI proposed in [41], is suitable for low voltage RF applications. The negative transconductance is realized by M_1 in CS configuration, whereas $M_2 - M_4$ form the positive transconductance where the simple current mirror comprised of $M_3 - M_4$ is used to invert the negative transconductance of M_2, also configured in CS connection. $M_5 - M_6$ are used for biasing purposes. Since the sole contribution practically comes from a minimum number of MOS transistor drain terminal(s), this configuration allows low equivalent conductances especially at node 2 which results in improved performance.

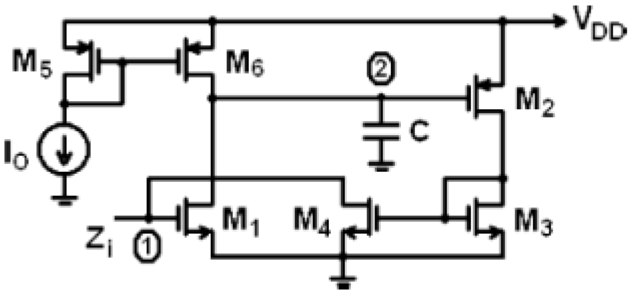


Figure 2.13: Simplified schematic of Uyanik-Tarim active inductor [41].

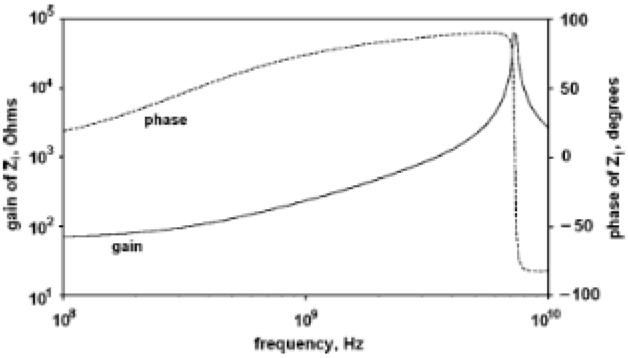


Figure 2.14: Frequency response of the active inductor [41].

Implemented in UMC-0.13µm 1.2V CMOS technology, the simulation result in Figure 2.14 shows that the active inductor had a wide frequency range from 0.3 GHz to its self-resonant frequency of approximately 7.32 GHz. The quality factor of the active inductor exceeded 100 in the frequency range 4.8-6.4 GHz with its phase error less than 1 degree. The maximum quality factor was 3900, occurring at 5.75 GHz. The minimum number of transistors stacked between the power and ground rails also enabled the active inductor to have a large input signal swing of 18 mV. The inductance was from 38 nH to 144 nH.

2.3.3 Noise-Cancelling of A CMOS Active Inductor

A CMOS active inductor with thermal noise cancelling is proposed in [42]. The noise of the transistor in the feed-forward stage of the proposed architecture is cancelled by using a feedback stage with a degeneration resistor to reduce the noise contribution to the input. Simulation results using 90 nm CMOS process show that noise reduction by 80% has been achieved. The maximum resonant frequency and the quality factor obtained are 3.8 GHz and 405, respectively.

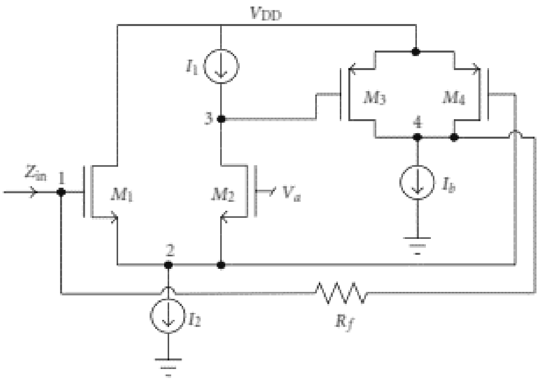


Figure 2.15: Low Noise AI [42].

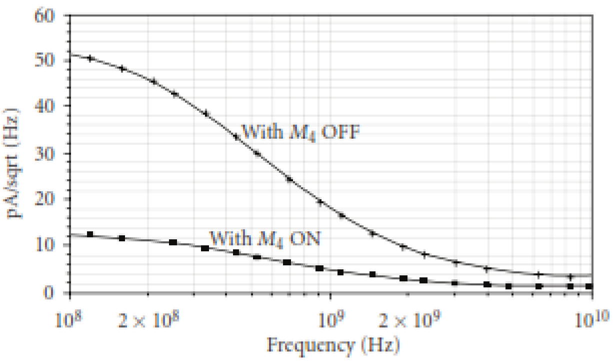


Figure 2.16: Simulated input referred noise with and without NC [42].

The simulated total input referred noise current when M_4 is turned ON/OFF is shown in Figure 2.16. It should be noticed from this graph that the noise has been reduced by 80% when M_4 is ON (with NC).

The equivalent Z_{in} can be obtained from the small signal analysis circuit in Figure 2.17. For better intuition, a few parasitic parameters have been ignored. The approximate expression for Z_{in} is as follows:

$$
\begin{aligned}
&Z_{in}(s) = \frac{s/C_1 + g_3/C_1C_3}{s^2 + \beta s + \alpha} \\
&\beta = (g_{m4}g_{m1}/G_mC_1)(g_4g_f/(g_4+g_f)) + g_1/C_1 + g_3/C_3 + \\
&\qquad g_3g_{m1}C_2/G_mC_1C_3 - \omega^2(C_2/G_m)) \\
&\alpha = (g_{m1}g_{m2}g_{m3} + g_{m1}g_{m4}g_3)/G_mC_1C_3)(g_f/(g_4+g_f))
\end{aligned}
\tag{2.30}
$$

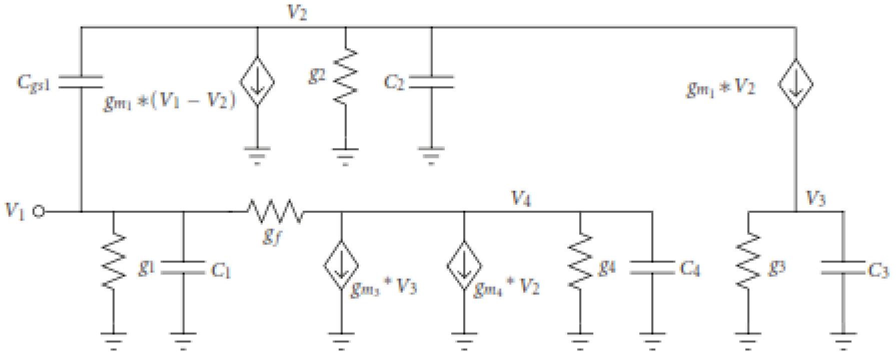


Figure 2.17: Small signal model of the simplified active inductor in Figure 2.15 [42].

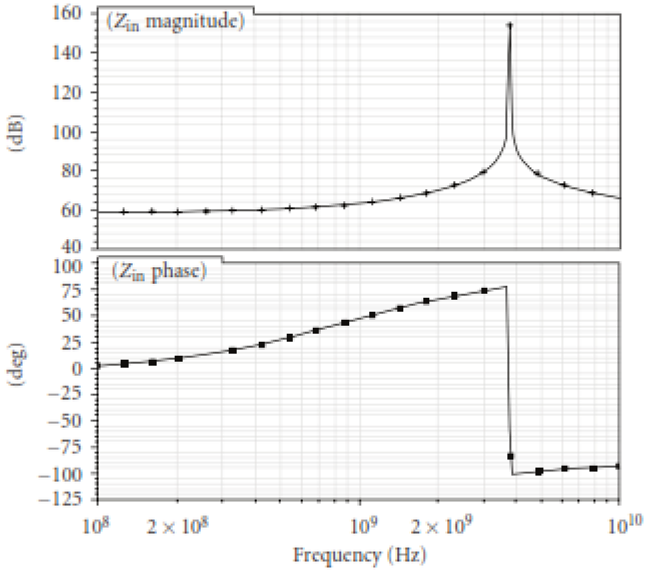


Figure 2.18: Simulated frequency response [42].

The simulated frequency response of the active inductor is shown in Figure 2.18. The simulations are carried out in 90 nm STM CMOS process. The active inductor resonates at centre frequency of $f_0 = 3.8\ GHz$ with a quality factor of 405.

2.3.4 Loss Regulated Active Inductor Proposed by Nair

The AI structure utilized in [43] is shown in Figure 2.19; it has a GC based grounded cascode topology and incorporates a modified feedback loss-regulation R-C network at the gate of transistor M3. First-order small-signal analysis yields an equivalent model for the AI with parameters:

$$\text{effective inductance } L_{eq} = \frac{g_{m2}g_{m3}(c_3 + c_{gs2}) + \omega^2 c_{gs2}{}^2 s(\omega)}{g_{m1}g_{m2}^2 g_{m3} + \omega^2 g_{m1}g_{m3}c_{gs2}{}^2} \approx \frac{(c_3 + c_{gs2})}{g_{m1}g_{m2}} \tag{2.31}$$

$$\text{resistive loss, } R_{loss} = \frac{g_{m2}g_{ds1}g_{ds3} + \omega^2[g_{m3}C_{gs2}^2 - g_{m2}C_{gs2}S(\omega)]}{g_{m1}g_{m2}^2\, g_{m3} + \omega^2\, g_{m1}g_{m3}C_{gs2}^2} \tag{2.32}$$

$$\text{self-resonant frequency, } \omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}(C_3 + C_{gs2})}} \tag{2.33}$$

$$\text{QF at } \omega_0,\ QF = \frac{\omega_0 L_{eq}}{R_{loss}} \simeq \sqrt{\frac{g_{m1}g_{m2}g_{m3}^2(C_3 + C_{gs2})}{C_{gs1}[g_{ds1}g_{ds3} - \omega^2 C_{gs2}S(\omega)]^2}} \tag{2.34}$$

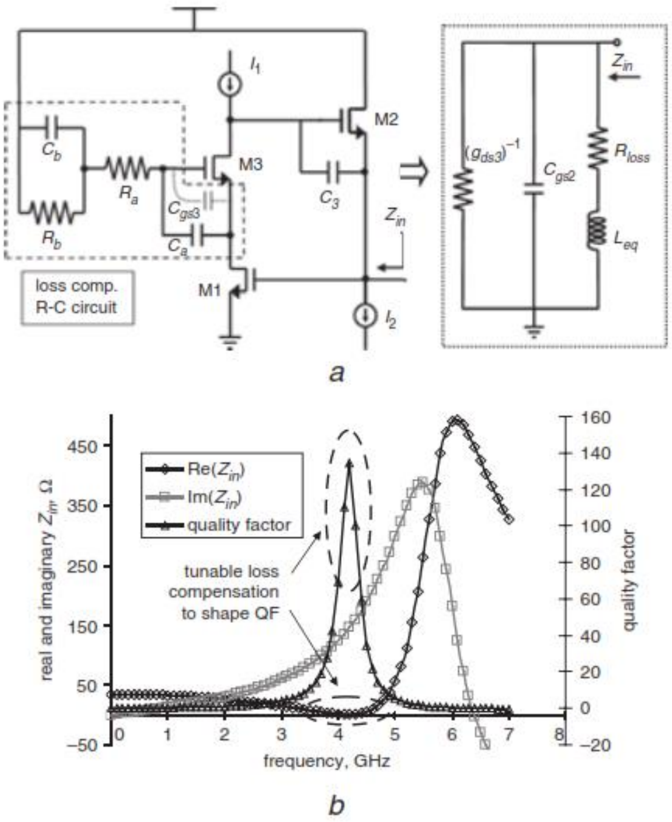


Figure 2.19: Active inductor (a) schematic and equivalent small-signal model, (b) typical AI performance at UWB frequencies [43].

where $S(\omega)$ is the combined admittance of c_{gs3} and the loss compensation R-C network. From (2.32) we see that a frequency-dependent series negative resistance is created by transistor M_3 which compensates for the resistive losses of the other active components in the AI. By tuning the R-C network, we can alter $S(\omega)$ to shape the total resistive loss in the AI and consequently control the value and peaking frequency of the QF independently of the ω_0 and L_{eq} over the desired frequency range, as shown in Figure 2.19. The ω_0 and L_{eq} and QF of the AI can be tuned independently for any I_2 value.

2.3.5 Cascoded Flipped Active Inductor Proposed by Saberkari

Usually, simple structures are preferred for RF circuits. The configuration of basic flipped-active inductor (FAI), shown in Figure 2.20 (a), is very simple and consists of only two transistors. As shown in Figure 2.20 (a), transistor M_2 located in the forward path has a positive transconductance (g_{m2}) while transistor M_1 in the feedback path provides a negative transconductance (g_{m1}). However, it suffers from low input voltage swing limited to the nMOS threshold voltage minus the overdrive voltage of transistor M_2, which is not sufficient in most applications and increases nonlinearity. Furthermore, this design requires more power consumption to achieve adequate inductance value and high quality factor. In order to overcome these problems, a cascoded flipped-active inductor (CASFAI) presented in [44], as shown in Figure 2.20, a CG p-MOS transistor M_3, added in the feedback path, increases the feedback gain and decreases the equivalent series resistance (R_s) of the inductor by a factor of $g_{m3}r_{o3}$. This leads to an increase in the quality factor of CASFAI in comparison to the conventional FAI. Additionally, the input voltage swing of this architecture can be increased with respect to the conventional FAI, as the drain voltage of M_2 has a value of $V_{D2} = V_{SG3}+V_{G3}$, which is close to V_{dd}. Moreover, due to the additional loop gain provided by the transistor M_3, the drain voltage of transistor M_2 has a small variation, leading to a decrease in the effect of the channel length modulation, which in turn improves the linearity performance.

From Figure 2.20 (c), the equivalent RLC model parameters of the CASFAI are as follows:

$$\begin{aligned} & C_p = C_{gs2}, G_p = 1/R_P \approx g_{m2} \\ & R_s = \frac{g_{o2}g_{o3}}{g_{m1}g_{m2}g_{m3}}, L_s = \frac{C_{gs3}}{g_{m2}g_{m3}} \end{aligned} \tag{2.35}$$

An interesting point is that the transistor M_1 does not affect the inductance value of the CASFAI, leading to more degrees of freedom in the design procedure. Hence, increasing the dimensions of M_1 further reduces the series resistance and, opposite to the FAI structure, it helps to achieve a higher quality factor without degrading the inductance value. Additionally, the inductance value can be increased by reducing the transconductance of M_2 enhancing the parallel resistance and the quality factor. In this case, the reduction effect of g_{m2} on the series resistance can be compensated by increasing g_{m1}.

A brief performance characteristic of the proposed CASFAI structure in a 0.18 µm CMOS process and 1.5 V supply voltage is shown in Figure 2.21. As it is obvious, the proposed structure shows inductance behavior in the frequency range between 0–6.9 GHz and has reached to a high quality factor of 4406 and inductance value of 7.56 nH, while consumes only 2 mW power.

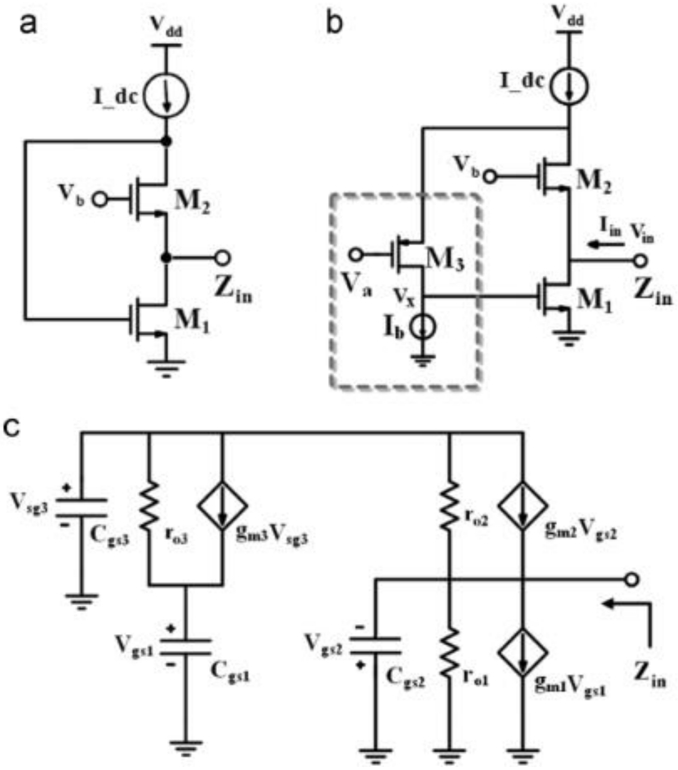


Figure 2.20: (a) Basic flipped-active inductor, (b) cascoded flipped-active inductor, and (c) small signal equivalent circuit [44].

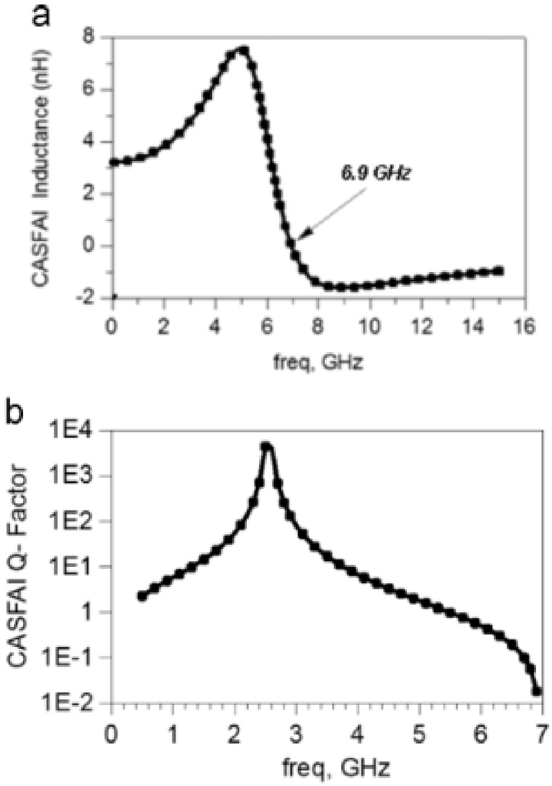


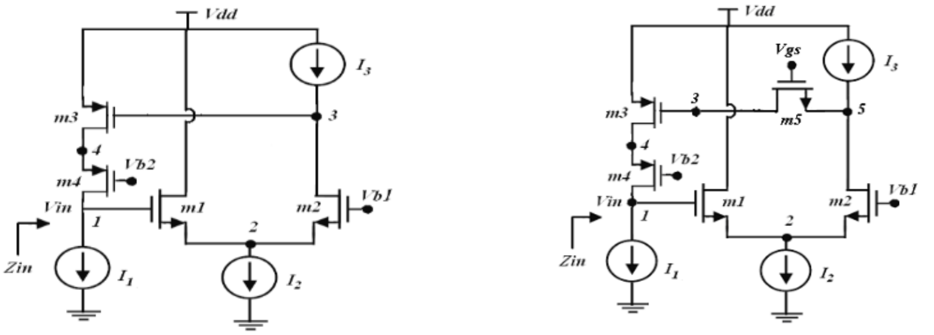
Figure 2.21: Characterizations of the CASFAI: (a) Inductance value, (b) quality factor [44].

2.3.6 Low Noise and Low Loss Active Inductor Proposed by Manjula

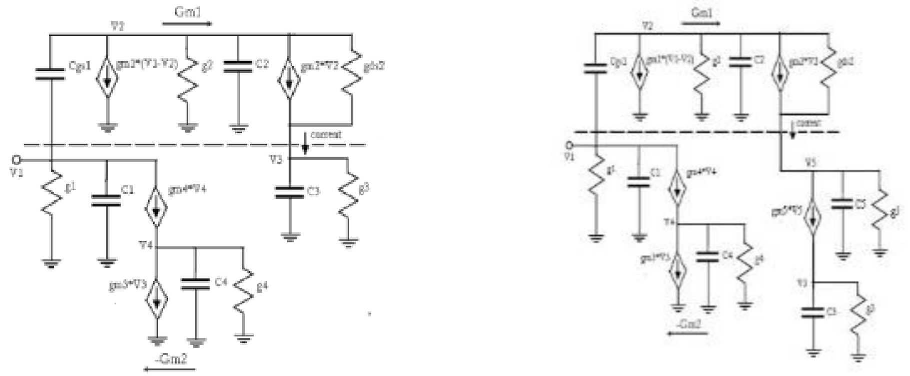
The proposed active inductor circuit in [45] uses PMOS cascode structure as negative transconductor of a gyrator to reduce the noise voltage. Also, this structure provides possible negative resistance to reduce the inductor loss with wide inductive bandwidth and high resonance frequency. To improve the quality factor, a MOS transistor is used as a feedback resistor between the positive transconductor and the negative transconductor. The tuning of quality factor and center frequency for multiband operation is achieved through the controllable current sources. The tunable range of the active inductors varies from 3.9 GHz to 12.3 GHz (without feedback transistor) with the power consumption of 0.6mW and 3.9GHz to 16GHz (with feedback transistor)with the power consumption of 0.65mW. The noise voltage varies from 21nV/√Hz to 7nV/√Hz for the active inductor without feedback transistor and from 12nV/√Hz to 5.612nV/√Hz for the active inductor with feedback transistor. The designed active inductors are simulated in 180 nm CMOS process using Synopsys HSPICE tool.

The proposed single ended AI in [45] is shown in Figure 2.22 (a). It consists of differential pair M_1 and M_2 which represents the positive transconductor G_{m1} between the input (node 1) and the output (node 3). The cascode pair M_3 and M_4 represents the negative transconductor $–G_{m2}$ between the input (node 3) and the output (node 1). Thus the G_{m1} and $–G_{m2}$ forms the gyrator which converts the parasitic capacitance C_3 at node 3 to an equivalent inductance $L_{eq} = C_3/G_{m1}G_{m2}$. Also, the cascode structure provides frequency range expansion by lowering the lower bound of the frequency range, thus increases the inductive bandwidth. The p-channel transistors are preferred for cascode structure as they have low noise and they can be placed in separate n-wells, thus eliminating the non- linear body effect. Thus, the combination of the differential configuration of G_{m1} and cascode configuration of -G_{m2} offers high inductive bandwidth, high resonance frequency and less noise.

To further improve the quality factor, series resistance R_s has to be reduced. This can be done by adding the transistor M_5 between the positive transconductor and the negative transconductor of the active inductor as shown in Figure 2.22 (b). The transistor M_5 act as feedback resistor enhances the loop gain and increases the quality factor of the AI. The current sources are realized using single MOS transistor current sources to make the active inductor compact and to operate at low voltage.



(a) AI without feedback transistor (b) AI with feedback transistor



(c) Small signal equivalent circuit of the AI without feedback transistor (d) Small signal equivalent circuit of the AI without feedback transistor

Figure 2.22: Proposed Low Noise and Low Loss AIs and their Small Signal Models [45].

The equivalent input impedance Z_{in}, is obtained from the small signal analysis circuit shown in Figure 2.22 (d). The equivalent input impedance Z_{in}, of Active inductor with feedback transistor (Figure 2,22 (b)) by using equivalent circuit of Figure 2.22 (d) is given as:

$$Z_{in}(s) = g_1 + sC_1 - \frac{g_{m5}g_{m4}g_{m3}g_{m2}g_{m1}}{(G+sC_2)(g_3+sC_3)(g_{m4}+g_4+sC_4)(g_{m5}+g_5+sC_5)} \tag{2.36}$$

The format of Z_{in} shows that it is equivalent to a parallel RLC network. From Equation (2.36) L_{eq} and R_s are given as:

$$L_{eq} = \frac{C_3 G g_4 g_5}{g_{m5}g_{m4}g_{m3}g_{m2}g_{m1} + Gg_1g_3(g_{m4}+g_4)(g_{m5}+g_5)}$$

$$R_s = \frac{G g_3 g_4 g_5}{g_{m5}g_{m4}g_{m3}g_{m2}g_{m1} + Gg_1g_3(g_{m4}+g_4)(g_{m5}+g_5)} \tag{2.37}$$

The parallel capacitance $C_p = C_1$ and resistance $R_p = 1/g_{g2}$. The resonance frequency ω_0 and the QF are given as:

$$\omega_0 = \sqrt{\frac{g_{m5}g_{m4}g_{m3}g_{m2}g_{m1} + Gg_1g_3\left(g_{m4}+g_4\right)\left(g_{m5}+g_5\right)}{GC_1C_3}}$$

$$Q_0 = \frac{\sqrt{\dfrac{g_{m5}g_{m4}g_{m3}g_{m2}g_{m1} + Gg_1g_3\left(g_{m4}+g_4\right)\left(g_{m5}+g_5\right)}{GC_1C_3}}}{\left[\dfrac{g_1}{C_1} + \dfrac{C_2g_1g_3}{GC_1C_3} + \dfrac{g_3}{C_3} - \dfrac{\omega^2C_2}{G}\right]g_4g_5} \tag{2.38}$$

The simulated frequency response of Z_{in} of the circuit of Figure 2.22 (a&b) is shown in Figure 2.23. Figure 2.24 shows the variation for different values of controllable current source I_2 for QF tuning.

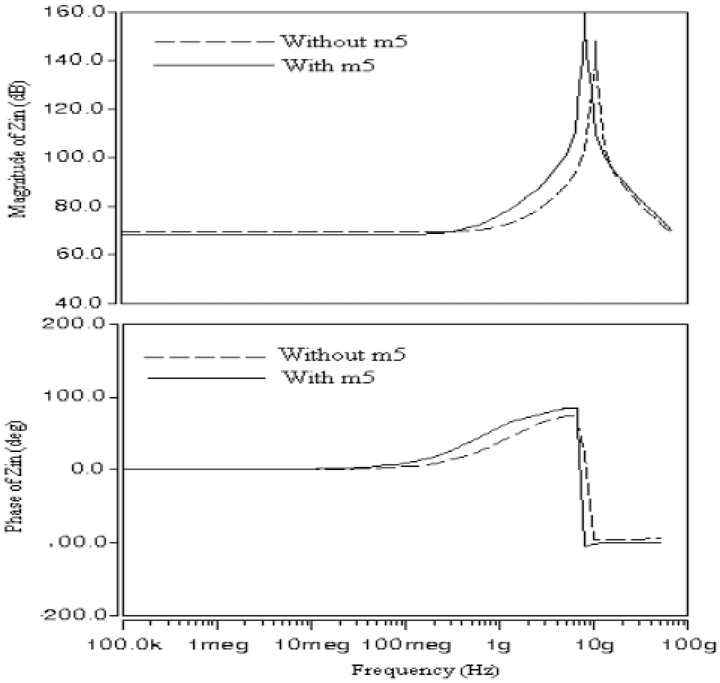


Figure 2.23: Simulated Frequency Response of Input Impedance [45].

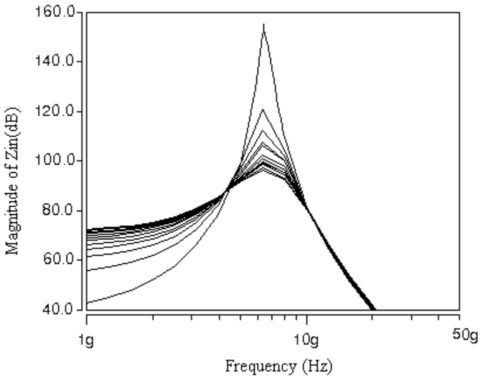


Figure 2.24: QF Tuning of Modified AI [45].

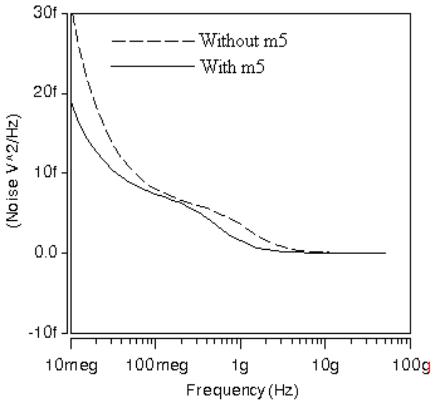


Figure 2.25: Noise Voltage of the Modified AI [45].

Figure 2.25 shows the simulated noise voltage of the active inductors. The noise voltage varies from 21nV/√Hz 7nV/√Hz for the tuning range 3.9GHz to 12.3GHz for AI without feedback transistor M_5. For the AI with feedback transistor with M_5, the noise output voltage varies from 12nV/√Hz to 5.612nV/√Hz for the tuning range 3.99 GHz to 16 GHz. The simulation results shows that both the AIs have less noise voltage make it suitable for designing low noise RF systems.

2.4 CMOS Floating Active Inductors Impelementation Base on GC Topology

2.4.1 Floating Active Inductor Proposed by Mahmoudi

The floating active inductor proposed by Mahmoudi and Salama was used in the design of quadrature down converter for wireless applications [46]. The schematic of Mahmoudi-Salama floating active inductor is shown in Figure 2.26.

It consists of a pair of differential transconductors and a pair of negative resistors at the output of the transconductors. $M_{8,16}$ are biased in the triode and behave as voltage-controlled resistors. They are added to the conventional cross-coupled configuration of negative resistors to provide the tunability of the resistance of the negative resistors without using a tail current source.

The small-signal equivalent circuit of the tunable negative resistor is shown in Figure 2.27 where a test voltage source V_x is added for the derivation of the equivalent resistance of the negative resistor. R represents the resistance of M_8. The resistance of the negative resistors at low frequencies is obtained as:

$$
\begin{aligned}
Z &= \frac{V_x}{I_x} = -\frac{R\left(\frac{1}{g_{m1}}+\frac{1}{g_{m2}}\right)}{R-\left(\frac{1}{g_{m1}}+\frac{1}{g_{m2}}\right)} \\
&= R//\left[-\left(\frac{1}{g_{m1}}+\frac{1}{g_{m2}}\right)\right]
\end{aligned}
\tag{2.39}
$$

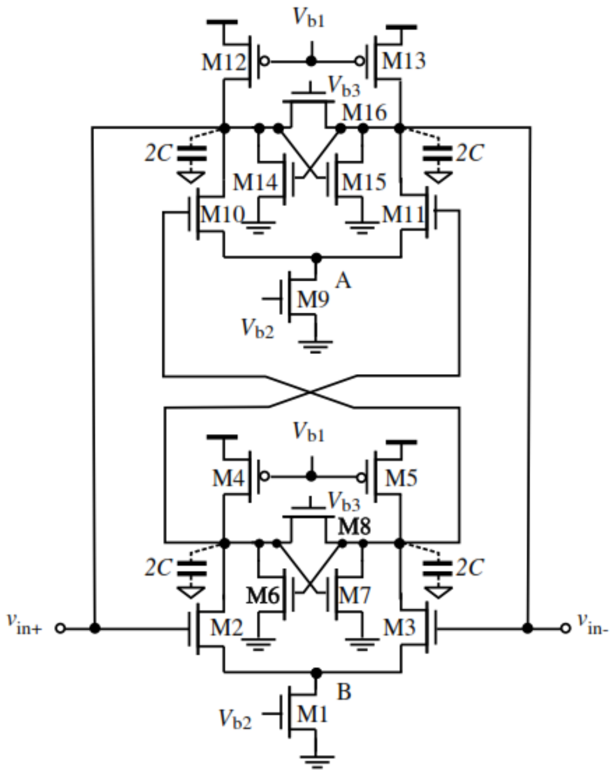


Figure 2.26: Floating AI implementation based on GC architecture [46].

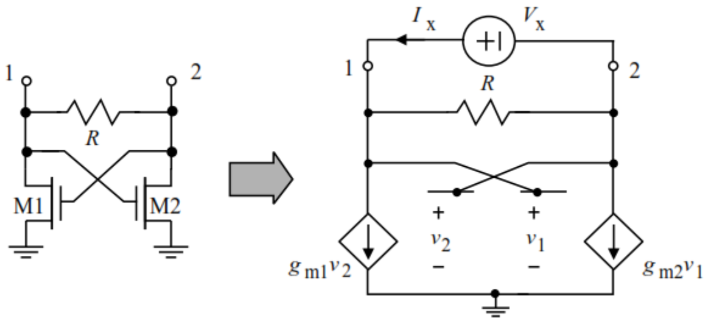


Figure 2.27: Small-signal equivalent circuit of FAI [46].

The inductance of the active inductor is given by $L = \frac{C}{G_{m1}G_{m2}}$, where G_{m1} and G_{m2} are the transconductances of the differential transconductors 1 and 2, respectively. By assuming that nodes A and B are the virtual ground, we have $C \approx \frac{C_{gs2,3,10,11}}{2}$ and $G_m = g_{2,3,10,11}$.

2.4.2 Floating Active Inductor Proposed by Cetinkaya

The Designed FAIs in [47] are designed based on GAI which is illustrated in section 2.3.2. Apparently, the circuit has been replicated and re-designed so that the positive and negative transconductance stages provide the symmetry shown in Figure 2.28.

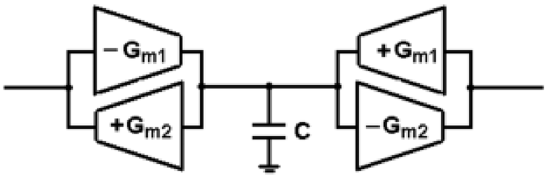


Figure 2.28: The gyrator-C equivalent of the floating active inductor [47].

A passive filter has no biasing problem, however the active implementation of an inductor requires biasing of the active components, the MOS transistors in this case. Also, the effect of the source and load resistances should be considered and the necessary isolation be provided. Therefore, additional circuitry for biasing and isolation has been included. As a result, slightly different floating inductance circuits have been used for inductors L_1 and L_2 in Low-Pass Filter (LPF) (Figure 2.29) apart from the fact that the core part was re-designed so that two different inductance values were realized.

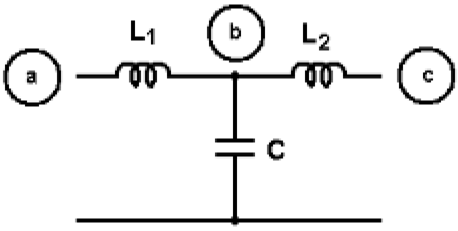
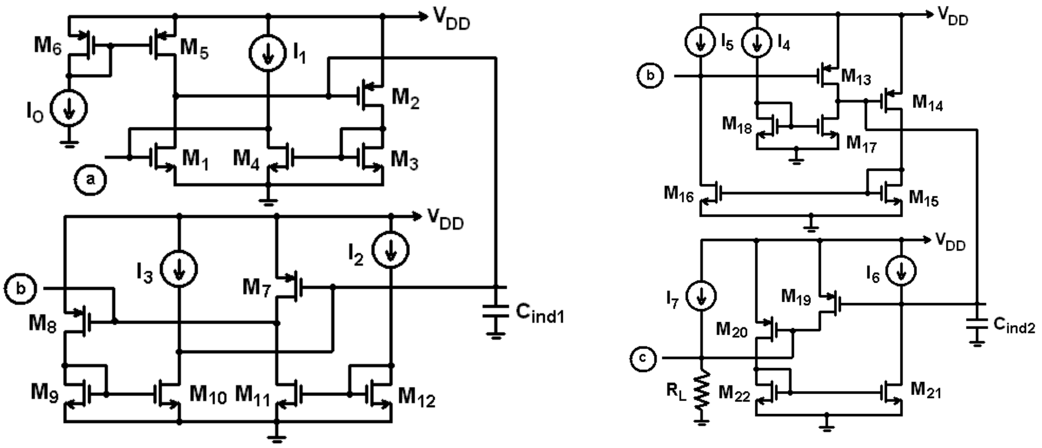


Figure 2.29: 3rd-order LPF [47].

The floating active inductor circuits used to replace L_1 and L_2 are given in Figures 2.30 (a&b), respectively.



(a) L_1 (b) L_2

Figure 2.30: FAIs circuits used in the filter a) L_1, b) L_2 [47].

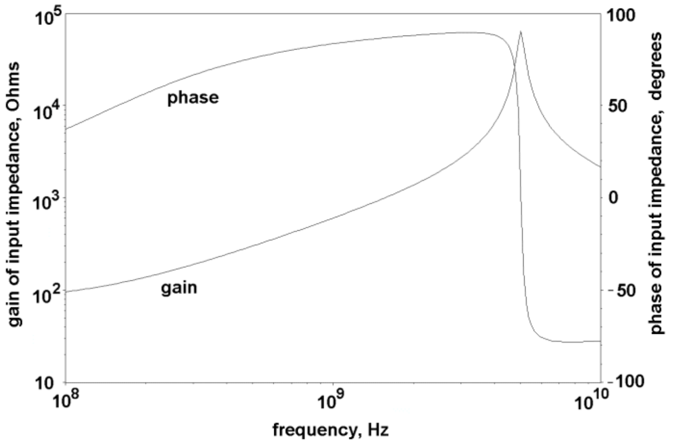


Figure 2.31: Frequency response of FAIs [47].

The simulated frequency response of the input impedance for both inductors shown in Figure 2.31. Both FAI's circuits have similar properties. The FAIs have wide operating bandwidth where the inductive characteristic extends from 100 MHz up to the SRF at 5.72 GHz with a nominal inductance value in nH range. Transient simulations show that there is no danger of instability for the FAI circuits. Both circuits have a spurious-free dynamic range of approximately 30 dB where the total noise voltage was integrated over a 500-MHz bandwidth. Simulations show that the noise performance of the circuit is also low as expected.

2.4.3 Feedback Resistance Floating Active Inductor Proposed by Akbari

The feedback resistance technique was also employed in the design of FAIs by Akbari-Dilmaghani et al. in [48] to improve the performance of these inductors. A similar approach was used by Abdalla et al. in design of high-frequency phase shifters [49].

The schematic of the feedback resistance FAI is shown in Figure 2.32. It consists of two basic differential-pair transconductors and two feedback resistors.

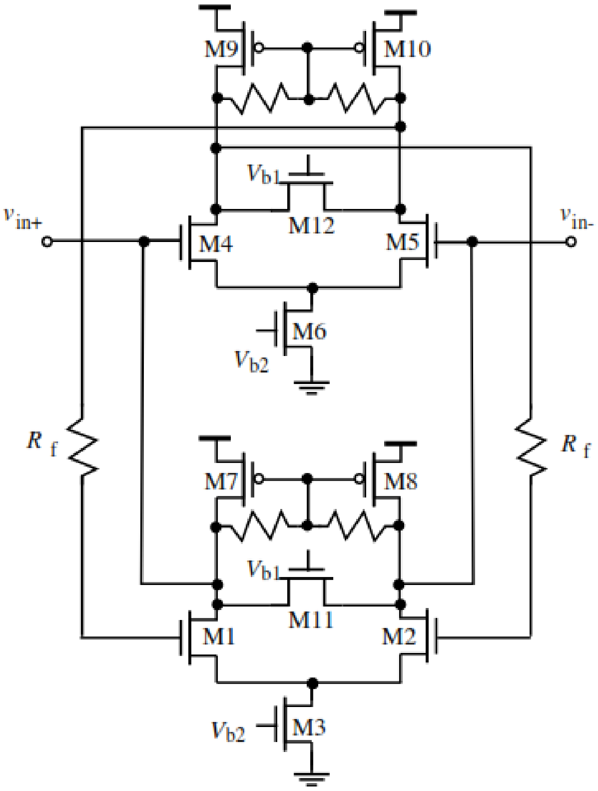


Figure 2.32: Simplified schematic of feedback resistance FAI [49].

$M_{11,12}$ are biased in the triode and behave as voltage-controlled resistors. The inductance and the parasitic series resistance of the floating active inductor are given by:

$$L = \frac{C + C_{gs4,5}\left(1 + \dfrac{R_f}{R_T}\right)}{g_{m1,2}g_{m4,5}},$$

$$R_s = \frac{\dfrac{1}{R_T} - \omega^2 C_{gs4,5} C R_f}{g_{m1,2}g_{m4,5}}, \tag{2.40}$$

$$C = C_{gd7,8} + C_{db1,2} + C_{db7,8} + C_{gs1,2},$$

$$R_T = R_f || R_{ds11,12} || r_{o1,2} || r_{o7,8}. \qquad (2.41)$$

It is evident from (2.40) that R_f boosts L and lowers R_s simultaneously. Both improve the performance of the FAI. Also seen from (2.40) and (2.41) that $M_{11,12}$ control the series resistance R_s of the active inductor. By adjusting V_{b1}, R_s can be minimized.

2.5 Chapter Summery

An in-depth examination of the principles, topologies, characteristics, and implementation of gyrator-C active inductors in CMOS technologies has been presented. It was shown that both grounded and floating (differential) active inductors can be synthesized using gyrator-C networks. To provide a quantitative measure of the performance of active inductors, a number of figure-of-merits have been introduced. These figure-of-merits include frequency range, inductance tunability, quality factor, noise and power consumption. The second part of the chapter has focused upon the CMOS implementation of gyrator-C active inductors. The schematics and characteristics of grounded and floating active inductors have been investigated in detail.

3. DESIGN OF NEW CMOS GROUNDED AND FLOATING ACTIVE INDUCTOR CIRCUITS BASED ON GYRATOR-C ARCHITECTURE

The expanding prevalence and development of wireless communications has inevitably boosted research in the field of Radio-Frequency Integrated Circuit (RFIC) design, especially in CMOS technology due to the shrinking of sizes and low cost availability of the process. Passive inductors are off-chip discrete parts and this seriously confines the bandwidth, diminish dependability, and expand the expense of framework.

The unavailability of inductors characterized by high quality factors, or high “Q,” is a shortcoming of monolithic fabrication processes. This shortfall is limiting when circuit design objectives entail the realization of narrowband radio frequency (RF) amplifiers, high selectivity bandpass and notch filters, and other circuits for a variety of communication and information processing applications. Planar spirals of metalization are used commonly, of course, to synthesize on chip inductors with inductance values in the few tens of nanohenries. These structures, which consume large surface areas, are difficult to parameterize reliably because their inductance and quality factor values are mathematically intricate functions of geometry and the electrical dynamics of distributed parasitic energy storage elements implicit to their underlying bulk silicon. Moreover, they rarely produce inductors having quality factors larger than four to seven at signal frequencies of at least the high hundreds of megahertz. To be sure, anemic inductive Q can be offset by incorporating Q-enhancing negative resistance compensating circuitry. Unfortunately, such compensation increases power dissipation, degrades circuit noise figure, and limits dynamic range.

Moreover, the sensitivity of Q-enhancing subcircuits to parasitic energy storage elements, as well as their outright potential instability, mandates the incorporation of automatic on chip tuning schemes. In addition to requiring further increases in standby power, these tuning subcircuits almost unavoidably degrade circuit frequency response.

An alternative to the passive on chip inductor—with or without Q-enhancing compensation—is the active inductor. Although plagued by higher noise and higher power consumption than are counterpart uncompensated passive realizations, active inductors are theoretically capable of producing relatively high quality factors.

3.1 Introduction

Many AI implementations can be found in literature [50-52]. However, each one of them offers only one or a few of the desirable specifications such as compactness, low voltage operation, wide inductance band, high quality factor, low power consumption, high dynamic range, low noise and tunability.

The gyrator approach to active inductance synthesis is the most popular of available techniques. This popularity derives from the fact that gyrators can be configured straightforwardly with operational transconductors, whose attainable broadband input/output transfer characteristics have improved in direct proportion to the rapid maturation of deep submicron CMOS device technology. Moreover, gyrators realized with operational transconductors feature transconductances than can be adjusted with applied bias, thereby allowing for inductors whose values can be adjusted, or “tuned,” electronically.

The gyrator approach to inductance emulation, like other active synthesis methods, suffers from potentially serious noise, power dissipation, and dynamic range problems. In this chapter, we try to work on charactrsics and performance of our designed AIs. The noise, resistive-loss, input-capacitance and QF are main our concerns in designing desired active block.

The chapter is organized in 5 sections: The low loss GAI is presented in section 3.2. Then, a high performance GAI with ability to adjust its properties is designed and analyzed in section 3.3. Section 3.4 describes a low noise GAI and section 3.5 peresents floating type of low loss AI. Finally, chapter is summarized in section 3.6.

3.2 A New Low loss CMOS Active Inductor Circuit

As previously stated, due to drawbacks of in-chip SI, AIs pulled in consideration of CMOS integrated circuit designers. AIs are able to supplement the passive inclusions to mitigate and overcome loss and bandwidth limitations. Consequently, they are an attractive alternative to their on-chip passive counterparts. Although they are plagued by higher noise and higher power consumption, AIs are theoretically capable of producing relatively high quality factors [53].

There are many efforts to optimize the inductive characterization of AI [54-57]. Among AI designing topologies, GC is popular especially for RF applications. That is because of their transconductance adjustability by their bias current changing which gives tunable capability to structure [56-57].

Some reported AIs benefit from cross-coupled structure. Due to the negative equivalent resistance at the output of this structure, equivalent series-loss resistance at the input node of such AIs decreases [54, 55]. Some others utilize resistive feedback to increase inductance of the AI [55, 56]. However, these structures do not give a high quality factor since the addition of the feedback resistance does not result in a low series-loss resistance. Furthermore, these technics do not lead to high SRF range.

In this section, Multi-Regulated Cascode (MRC) stages are used to decrease conductance in crucial nodes of the AI. However, one of them is located in the circuit such that, input transistor should be designed smaller in order to provide second gyrators bias condition. In addition all transistors of the MRC stages are made up of PMOS transistors. Also employing another MRC stage in the input node makes the parallel conductance very low.

3.2.1 Circuit Level Description

The well-known GC topology is used for designing the proposed GAI. The equivalent inductance in mentioned topology is obtained as:

$$L_{eq} \equiv C/(G_{m1}G_{m2}) \tag{2.1}$$

where G_{mi} is the ith gyrator's transconductance.

In order to have low-loss AI, all important nodes must have low conductance. The basic schematic of GC AI is depicted in Figure 3.1(a). In order to have high impedance nodes, the modified version of basic configuration is depicted in Figure 3.1(b). Here, all transistor are connected in CS configuration which results high impedance nodes. In order to have low-loss active inductor, the impedance in input (1) and output (2) nodes should be as high as possible. In designing analog amplifiers a regulated cascode stage is used to increasing the output impedance for gain boosting [39]. Therefore, to increase the impedance in input and output nodes of AI, the MRC stage is employed.

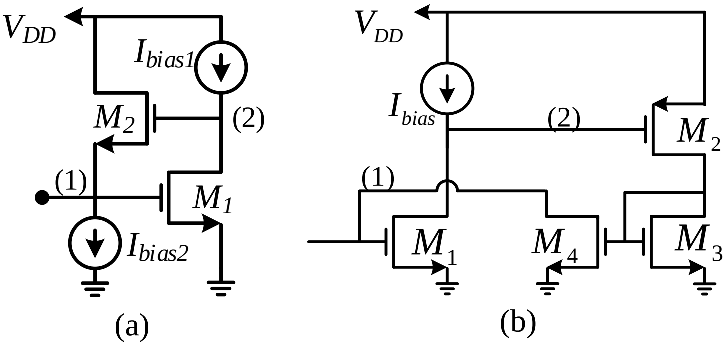


Figure 3.1 : Schematic of gyrator-C active inductors a) Basic b) Modified.

In the proposed GAI circuit circuit (Figure 3.2) M_i, M_{c-i} and M_{b-i} transistors are used for main elements of Gyrator-C, MRC stage and biasing, respectively. The salient feature of the design is that all transistors in main path are utilized in common-source configuration which results in performance improvement and all of them are free from body effect. The negative transconductance is realized by M_1, whereas M_2, M_3 and M_4 forms the positive transconductance.

The sensitivity of the quality factor of the active inductor is merely depends on series-resistive loss in high frequencies. Hence, in order to boost the quality factor of active inductors, it must be decreased. Reducing resistive-loss is done by using advanced circuit techniques, such as MRC stage. Also, the MRC stage is effective in lowering the input conductance, as shown in Figure 3.2.

MRC stage is made up of PMOS transistors in order to:

- minimize the input transistor (M_1) as small as possible in order to adjust second stage biasing,
- decrease the number of transistors in main path of ac signal

Table 1 compares the resistances in nodes (1) and (2), with and without MRC stage.

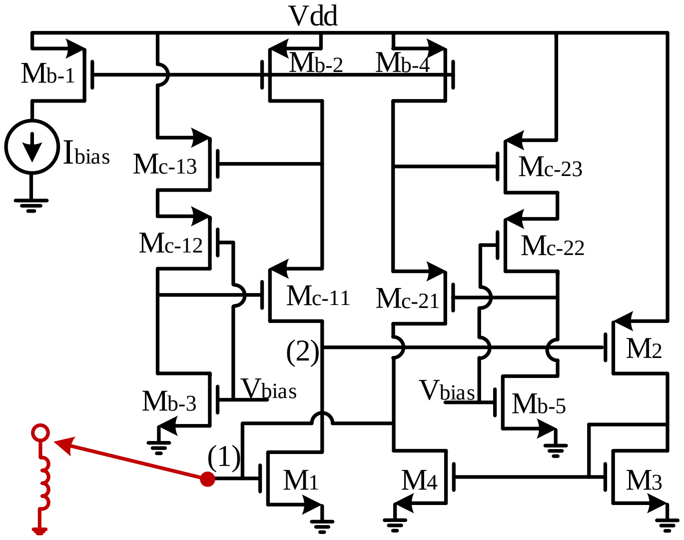


Figure 3.2 : Proposed GAI.

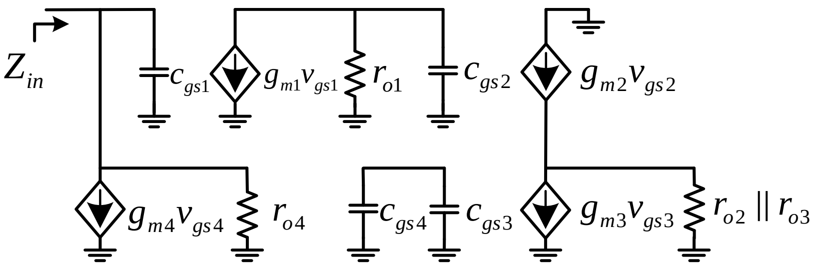


Figure 3.3 : Small-signal equivalent model of proposed GAI.

Table 3.1 : Resistance comparison with-without MRC stage.

node	Resistance	
	without-MRC	with- MRC
(1)	$r_{o,4} // r_{o,b-4}$	$r_{o,1} // (r_{o,b-2} r_{o,c-1} g_{m,c-1} r_{o,c-2} g_{m,c-2} r_{o,c-3} g_{m,c-3}) \cong r_{o,1}$
(2)	$r_{o,1} // r_{o,b-2}$	$r_{o,1} // (r_{o,b-2} r_{o,c-11} g_{m,c-11} r_{o,c-13} g_{m,c-13} r_{o,c-12} g_{m,c-12}) \cong r_{o,1}$

Figure 3.3 demonstrates the small-signal model of proposed circuit (Figure 3.2) in order to verify the input impedance characterization. The input admittance of the circuit of Figure 3.3 is calculated as follows:

$$Y_{in} = \frac{1}{Z_{in}} = sc_{gs1} + \frac{1}{r_{o4}} + \frac{1}{\frac{g_{m3} \times sc_{gs2}}{g_{m1} g_{m2} g_{m4}} + \frac{g_{m3}}{r_{o1} g_{m1} g_{m2} g_{m4}}} \tag{3.2}$$

By analyzing (3.2), it can be seen that proposed circuit consists of four components: an inductor (L_{eq}) and its series-resistance (R_s) and parallel capacitance and resistance (C_p and R_p) where their value are obtained as:

$$R_p = r_{04}, R_s = \frac{g_{m3}}{g_{m1}g_{m2}g_{m4}r_{o1}}, C_p = c_{gs1}, L_{eq} = \frac{g_{m3}c_{gs2}}{g_{m1}g_{m2}g_{m4}} \tag{3.3}$$

The RLC network's SRF which determines the circuit inductive behavior upper limit in frequency band and QF of AI are calculated as:

$$SRF = \sqrt{\frac{1}{C_p L_{eq}}} = \sqrt{\frac{g_{m1}g_{m2}g_{m4}}{g_{m3}c_{gs2}c_{gs1}}} \tag{3.4}$$

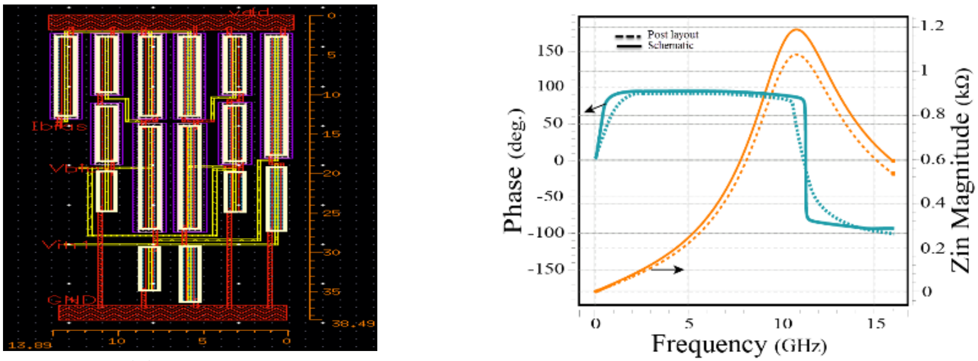
$$Q = \frac{\mathrm{Im}[Z_{in}]}{\mathrm{Re}[Z_{in}]} \tag{3.5}$$

As discussed, bias current variation or adding extra capacitance on the gate of second transistor gives tunable capability for the GAI.

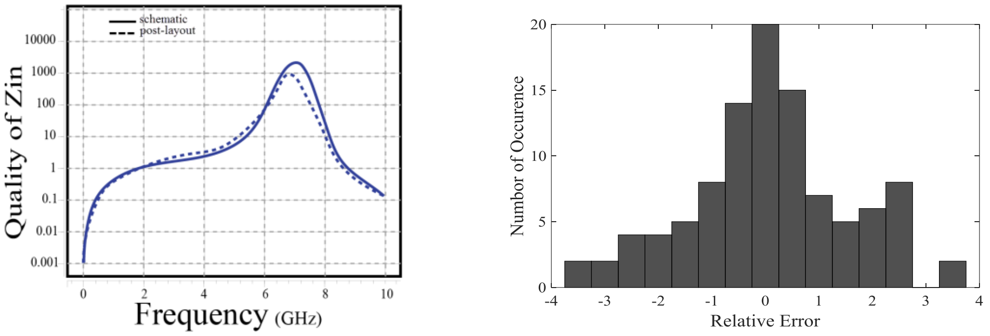
3.2.2 Simulation Results

To verify the performance of the proposed GAI as shown in Figure 3.2, the GAI was implemented by using 0.18 µm RF MOS transistors in an AMS CMOS process in Cadence. Figure 3.4(a) depicts the layout, which is drawn by utilizing a poly and metal (M1) with the total area of 13.9×38.5 µm^2. The magnitude and phase of the GAI is depicted in Figure 3.4(b). The QF simulation is shown in Figure 3.4(c). The post-layout simulations in Figure 3.4(b&c) are carried out from extracted file, which contains parasitic elements.

The Monte Carlo analysis with 100 iterations is performed for inductance value probing by applying ±5 % Gaussian distribution at ±3s level in the variation of transistors aspect ratio and threshold voltage. Figure 3.4(d) proves that 74% of the total samples occurred with the relative error of less than ±1.5 %, while in the worst case 18% of samples lead to the error of more than ±2. Table 3.2 summarizes some important properties of the designed GAI.



(a) Layout (b) Magnitude and Phase



(c) Quality factor (d) Monte Carlo simulation

Figure 3.4 : The GAI simulation results.

Table 3.2 : Proposed GAI Characteristics.

CMOS Tech.	Supply voltage	Inductor value	Inductive frequency band
0.18 µm (AMS)	1.8 v	13 nH	0.3-11.2 GHz
Max. QF	DC power	Area	Transistor model
1000@6.7GHz	1 mW	534.6 µm^2	RF MOS

A low-loss GAI circuit was proposed in this section. The proposed AI was designed on GC topology and used a few number of transistors in the main path of signal which made it suitable for RF applications. The MRC stages were employed to enhance high performance AI. The used MRG stage in output node (2) is configured in such way that it resulted in smaller input transistor (M_1). Thus the SRF enhancement was obtained. The DC power consumption of the proposed AI was 1 mW for 1.8 V dc power supply. Simulation results were provided for a 0.18 um CMOS-AMS process. The results show that the circuit can be used in RF applications for frequency band ranging in the 300 MHz~11.2 GHz. Total area consumption of the structure is 534.6 µm^2.

3.3 A new low-loss active inductor with independently adjustable self-resonance frequency and quality factor parameters

Designers do their best to improve SRF and QF, two main characteristics in term of AI performance [58]. In GC topologies, the input transistors play critical role in active inductor characterization. By selecting the input transistor's gate-source parasitic capacitance sufficiently small, then the SRF Range (SRFR) of AI improves but its QF and stability degrade. On the other hand, large input transistor guarantees the stability of AI and improves the inductance value and QF but decreases the SRFR [59]. Thus, there is a trade-off between SRF and QF.

Another main challenge for AIs designers is their ohmic loss which affect the QF. For decreasing this parasitic components many tricks are used such as Multi-Regulated Cascade stages [53, 60] or cross-coupled structures i.e. Negative Resistance (NR) [61-64]. But these methods are limited input swing and increased input referred noise. Also they need biasing transistors which makes the device larger.

The salient feature of this work is adjusting SRFR and QF of an AI without affecting each other. The cascoding and RC feedback structures are used in the new design of AI. As it discussed before, input transistor is very important regarding to AI characterizations. Cascoding input transistor gives the ability to adjust the first gyrator's transconductance and input parasitic capacitance independently. Furthermore, the inductance value can be adjusted by other transistor's transconductance. The RC feedback is utilized to cancel the parasitic series-resistance of AI which results in QF enhancement. Since, bias condition of cascoding transistors is provided by a diode-connected transistor, the proposed structure is robust in terms of performance over variation in process, voltage and temperature (PVT).

3.3.1 Theoretical and Implementation Description

Signal Follow Graph (SFG) of the well-known GC topology of AIs is depicted in Figure 3.5. In Figure 3.5, VCCS denotes voltage controled current source. The MOS transistors are VCCS devices. If the ideal operational transconductane amplifiers are supposed then the input resistance can be written as:

$$Z_{in} \equiv L_{eq} = \frac{V_{Leq}}{I_{Leq}} = \frac{sC}{G_{m1}G_{m2}} \qquad (3.6)$$

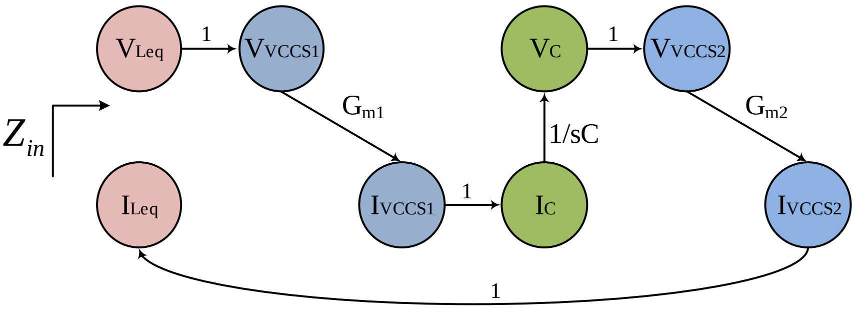
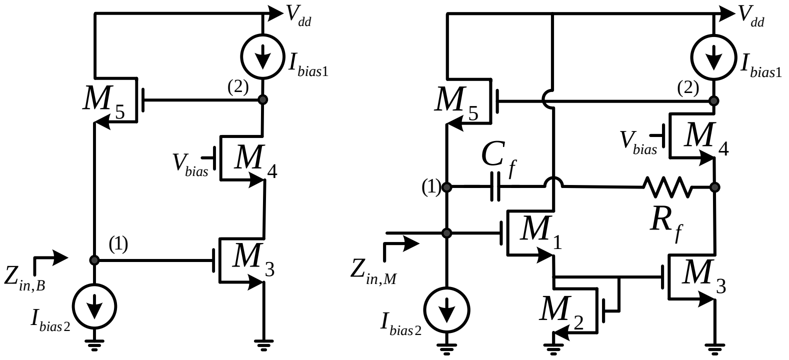


Figure 3.5 : SFG of GC topology.

Due to parasitic components which arise from intrinsic characteristics of MOS transistors, the input impedance is not purely inductive in all frequency range. Regarding to SFG of GC topology (Figure 3.5), Figure 3.6 (a, b) shows the basic [65] and modified circuit level implementation of AI. In basic circuit the M_3 and M_5 and also in modified circuit of the proposed AI the M_1, M_2, M_3 and M_5 transistors are creating G_{m1} and G_{m2} of GC structure, respectively.

The RC feedback (C_f and R_f in Figure 3.6 (b)) is used to eliminate parasitic series-resistance which degrades QF of the AI. Also, the bias voltage (V_{bias}) of cascode transistor (M_4) is employed to improve QF. Furthermore, by adding a diode-connected transistor (M_2), bias condition of input cascoding transistors (M_1, M_3) will be fixed in a given input, regarding to PVT variation. Thus, this topology results a robust structure [66].

The designed AI's SRF is mainly determined by input parasitic capacitance ($\sim C_{gs1}$) and transconductances of M_1 and M_2. On the other hand, QF and inductance value are specified by M_3 and M_4. In other words, use of cascaded input transistors leads to separate affective transistors on SRF and QF of the proposed AI. Therefore, SRF and QF of the proposed AI can be adjusted as desired without affecting each other.



a) Basic b) Modified

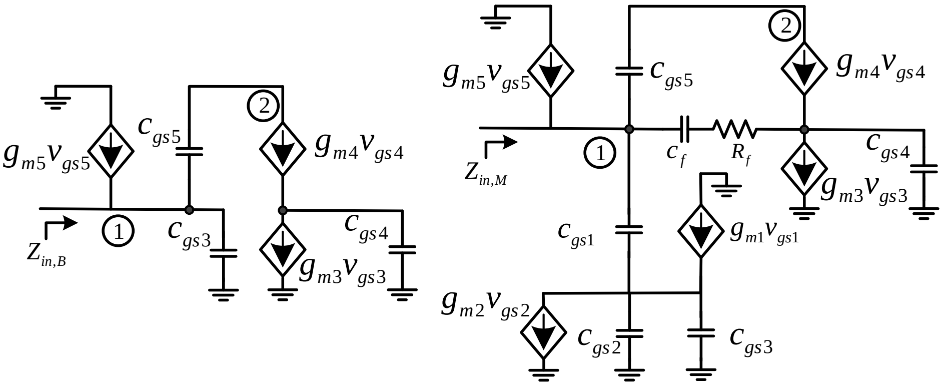
Figure 3.6 : Active inductor implementation, a) Basic, b) Modified.

To verify the input impedance of proposed circuits (Figures 3.6 (a, b)), Figures 3.7 (a, b) show simplified small-signal model. Where, $c_{gsi}\ and\ g_{mi}$ are gate-source capacitance and transconductance of the ith transistor, respectively. As the c_{gsi} is in the range of femto-Farads and the g_{mi} is in $m\mho$ range, then the term $c_{gs}\ w$ is very smaller than g_m in GHz range of frequency. As a result, in the extraction of any relation from the proposed circuit, the terms consisting of $c_{gs}w$ can be ignored in contrast to those consisting of g_m. By considering this note, input admittance of the circuit of Figure 2 is obtained as follows:

$$Y_{in,B}=\frac{1}{Z_{in,B}}\approx\frac{g_{m3}g_{m5}}{c_{gs5}s}+(c_{gs3})s+g_{m5} \tag{3.7}$$

$$Y_{in,M}=\frac{1}{Z_{in,M}}\approx\frac{g_{m1}g_{m3}g_{m5}}{(g_{m1}+g_{m2})c_{gs5}s}+\left(\frac{c_{gs1}g_{m2}}{g_{m1}+g_{m2}}\right)s+\frac{\frac{g_{m3}g_{m1}}{g_{m1}+g_{m2}}c_{gs5}-g_{m5}c_f}{c_{gs5}} \tag{3.8}$$

where subscripts “B” and “M” denote the basic and modified circuits, respectively.



(a) Basic (b) Modified

Figure 3.7 : Small-signal model, a) Basic, b) Modified.

The extracted equation (3.7) and (3.8) from small-signal model shows that the equivalent circuit of Figures 3.7 (a, b) are a parallel RLC network. The expressions of these elements can be derived as:

$$R_B=\frac{1}{g_{m5}},\ C_B=c_{gs3},\ L_B=\frac{1}{g_{m3}g_{m5}}c_{gs5} \tag{3.9}$$

$$R_M=\frac{c_{gs5}}{\frac{g_{m3}g_{m1}}{g_{m1}+g_{m2}}c_{gs5}-g_{m5}c_f},\ C_M=\frac{g_{m2}}{g_{m1}+g_{m2}}c_{gs1},\ L_M=\frac{g_{m1}+g_{m2}}{g_{m1}g_{m3}g_{m5}}c_{gs5} \tag{3.10}$$

By employing feedback in proposed AI, a negative term is added to the resistance in RLC equivalent model of the suggested AI (as seen in (3b)). By selecting proper value of C_f , QF can be high enough. For the parallel RLC combination, if the condition $LCw^2 < 1$ is met, then it behaves like an inductor. Therefore, aforementioned relations determine the upper limit of inductive frequency range which is defined as SRF. The SRF, the frequency in which imaginary part of the input impedance or admittance becomes zero, in basic and modified AI circuits can be calculated as:

$$SRF_B = \sqrt{\frac{1}{C_B L_B}} = \sqrt{\frac{1}{c_{gs3}} \times \frac{g_{m3} g_{m5}}{c_{gs5}}} = \sqrt{\frac{g_{m3} g_{m5}}{c_{gs3} c_{gs5}}} \tag{3.11}$$

$$SRF_M = \sqrt{\frac{1}{C_M L_M}} = \sqrt{\frac{g_{m1} + g_{m2}}{g_{m2} c_{gs1}} \times \frac{g_{m1} g_{m3} g_{m5}}{(g_{m1} + g_{m2}) c_{gs5}}} = \sqrt{\frac{g_{m1} g_{m3} g_{m5}}{g_{m2} c_{gs1} c_{gs5}}} \tag{3.12}$$

As it can be seen from (3.11) and (3.12), the value of inductance, input parasitic capacitance and SRF are determined by adjusting $g_{m1}\ and\ g_{m2}$ while maintaining stability, i.e. $g_{m3} > g_{m5}$ [67]. By cascoding input transistors ($M_1,\ M_3$), we separate the transistors which impress on SRF, QF and stability. Table 3.3 shows influence of $M_1\ and\ M_2$ transconductance variations on properties of the AI.

According to Table 3.3, $g_{m1}\ and\ g_{m2}$ can be adjusted for obtaining desired specifications from the circuit. By considering identical transistors ($M_1 = M_2 \rightarrow g_{m1} = g_{m2}$), the equations for $L, C\ and\ SRF$ in modified case can be written as:

$$L = \frac{2}{g_{m3} g_{m5}} c_{gs5},\ C = \frac{1}{2} c_{gs1},\ SRF = \sqrt{\frac{g_{m3} g_{m5}}{c_{gs1} c_{gs5}}} \tag{3.13}$$

Table 3.3 : Influence of cascoding transistors transconductances variation on the proposed AI properties.

$\boldsymbol{g_{m1} = k g_{m2}}$	$\boldsymbol{k < 1}$	$\boldsymbol{k = 1}$	$\boldsymbol{k > 1}$
L	$L_M = \left(\frac{k+1}{k}\right) L_B \gg L_B$	$L_M = 2\, L_B$	$L_M = \left(\frac{k+1}{k}\right) L_B > L_B$
C	$C_M = \frac{1}{k+1} C_{gsi} < C_{gsi} = C_B$	$C_M = \frac{1}{2} C_{gsi} = \frac{1}{2} C_B$	$C_M = \frac{1}{k+1} C_{gsi} \ll C_{gsi} = C_B$
SRF	$SRF_M = \sqrt{k}\, SRF_B < SRF_B$	$SRF_M = SRF_B$	$SRF_M = \sqrt{k}\, SRF_B > SRF_B$
QF	High	High	High

The subscripts B and M denote basic and modified, respectively

Equation (3.13) shows that for almost same SRF, two times larger inductor can be obtained from the proposed circuit. In identical transistors circumstances, QF in frequencies lower than SRF for the RLC parallel network equivalent model of AI can be formulated as:

$$Q = \frac{R_{\text{Parallel}}}{L_{\text{Parallel}}} = \frac{\dfrac{c_{gs5}}{\frac{1}{2} g_{m3} c_{gs5} - g_{m5} c_f}}{\dfrac{2}{g_{m3} g_{m5}} c_{gs5}} \qquad (3.14)$$

Regarding to (3.14), by choosing c_f close to $\frac{g_{m3}}{2g_{m5}} c_{gs5}$, $R_{Parallel}$ becomes ∞ and the QF in frequencies lower than SRF can be large enough. It can be seen from (3.12) and (3.14) that the properties of proposed AI can be determined almost without affecting each other. Bias currents variation, which cause to transconductances altering and also adding extra capacitance to node (2) give tuning possibility to the proposed AI.

3.3.2 Simulation results and performance analysis

In order to evaluate the performance of the proposed AI as depicted in Figure 3.6(b), the AI was implemented utilizing RF transistors in 0.18 µm CMOS process. The post-layout simulation results as well as performance analysis are presented using HSPICE with TSMC level 49 (BSIM3v3) parameters. Figure 3.8 shows layout of the proposed design which is drawn by Cadence software using single poly and one metal (M1) with the total area of 7.2×39.8 µm^2.

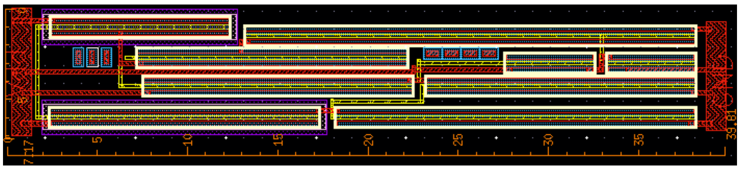


Figure 3.8 : Layout of the proposed circuit.

Figures 3.9 through 3.10 illustrate frequency response of the AI. With respect to Figure 3.9, inductive frequency range of the proposed AI is between 0.3-11.3 GHz, thus it is suitable for RF applications. The real and imaginary parts and QF post-layout simulations results are illustrated in Figure 3.10. According to Figure 3.10, maximum QF is 2.1k which occurs at 5.9 GHz

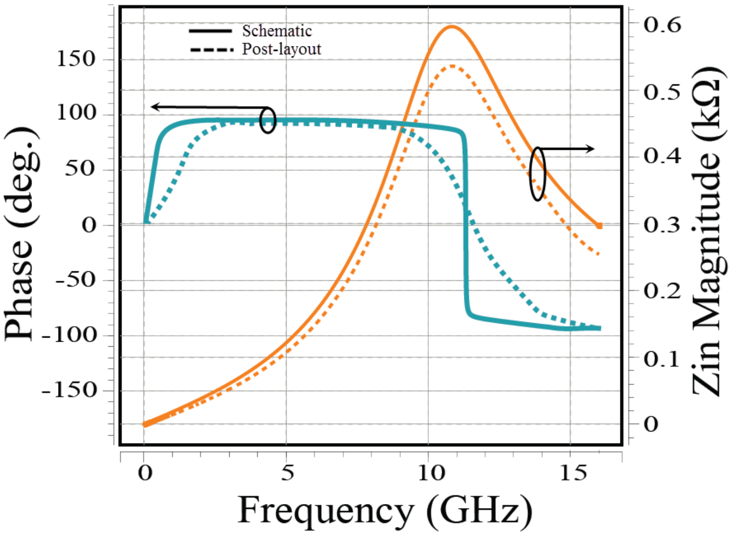


Figure 3.9 : Frequency response of the proposed AI.

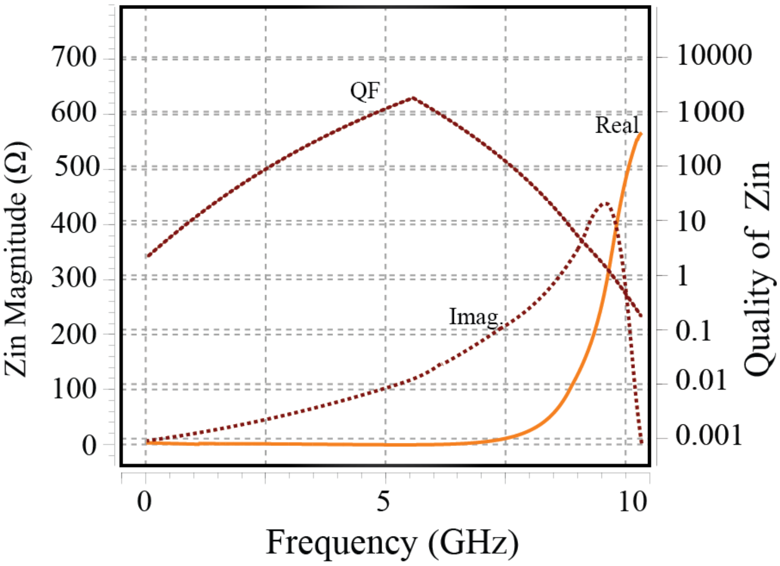


Figure 3.10 : Real part, imaginary part and QF of the of the input impedance Zin.

In order to investigate the robustness of the circuit against the process and threshold voltage variation, the Monte Carlo analysis with 200 iterations is performed by applying ±5 % Gaussian distribution at ±3σ level in the variation of transistors aspect ratio and threshold voltage.According to Figure 3.11, 72 %of the total samples occurred with the relative error of less than ±1.5 %, while in the worst case 20% of samples lead to the error of more than ±2 %.

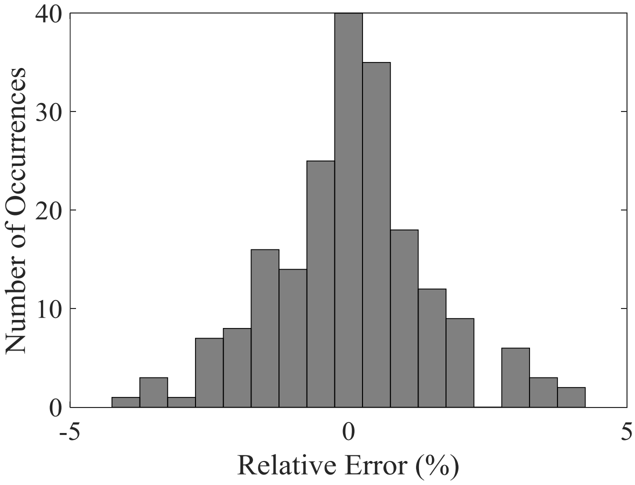


Figure 3.11 : The result of Monte Carlo analysis of GC circuit for ±5 % mismatch in transistors aspect ratio and threshold voltage (No. of iterations = 200).

The threshold voltage is the most important parameter in the analysis of temperature dependence of CMOS circuits, owing to the fact that current–voltage characteristic of MOS transistor is proportional to the square of the difference of gate-source and threshold voltages. Thus, a small variation in threshold voltage causes a large change in the output current. Therefore, transistors current variation affect their transconductance value. According to (3.13), transconductances variation leads to the AI's properties changing. Table 3.4 shows inductance and SRF values changing in different temperatures. This table indicates that the AI is almost stable between -5~55 ℃.

Table 3.4 : charactrization of the proposed AI in different temperature.

T(℃)	-45	-25	-15	-5	5	15	25	35	45	55	65
L(nH)	223	223	221	220	218	217	216	215	213	211	208
ΔL(%)	3.24	3.24	2.31	1.85	0.92	0.46	0	0.46	1.38	1.85	3.7
SRF(GHz)	10.94	10.94	11.02	11.09	11.16	11.25	11.3	11.34	11.46	11.53	11.67
ΔSRF%	3.19	3.19	2.48	1.86	1.23	0.44	0	0.35	1.41	2.03	3.27

Regarding to Figure 7 and Table 2, the proposed AI is robust against PVT variation. The relative changing in inductance and SRF value are less than 2% in 73% of samples between -5~45 ℃.

Table 3.5 is provided for the comparison of the proposed AI characteristics with the other reports.

Table 3.5 : Performance comparison of the proposed AI with reported AIs.

Ref.	Tech. (μm/V)	IBW (GHz)	L (nH)	Q_{max}@ F(GHz)	P_{diss} (mW)
$[64]_M$	0.18/1.8	n.a.	33	33@4	3.6
$[68]_M$	0.13/1.6	0.5-10.2	14.5	3k@3.7	13.6
$[41]_{SS}$	0.13/1.2	0.3-7.32	144	3.9k@5.75	1
TW_{PS}	0.18/1.8	0.3-11.3	216	2.1k@5.9	1

IBW: Inductive Bandwidth n.a.: not assigned TW:This Work
Subscribes M, SS and PS denote measurement, schematic simulation and post-layout simulation, respectively.

A new high Q, grounding active inductor was designed in this section. The proposed AI was designed on Gyrator-C topology and used a few number of transistors in the main path of signal which made it suitable for RF applications. Canceling parasitic components and determining the properties of the AI are salient feature of the design. Simulation results were provided for a 0.18 µm CMOS process. Monte Carlo simulation and temperature analysis results show the structure’s stability over PVT variation. QF enhancement was obtained by canceling resistive loss whose maximum value was 2.1k in 5.9 GHz. The results show that the circuit can be used as an inductor for frequency band 0.3-11.4 GHz. The DC power consumption of the proposed AI was 1 mW from 1.8 V DC power supply. Comparison shows that our circuit is superior in terms of IBW, inductance value, QF and power dissipation.

3.4 Low-Noise CMOS Active Inductor Circuit

The CMOS process has turned to dominant technology in implementation of electronic circuits in recent years. As a result, Active Inductors (AIs) which are designed with CMOS technology, play a vital role in the design of low power, highly integrated RF front end communication circuits like Low Noise Amplifiers (LNAs) [43, 50, 69], Band Pass Filters (BPFs) [70,71] and Voltage Control Oscillators (VCOs) [30, 72]. AIs can potentially alleviate many difficulties of analog circuits in contrast with circuits that are designed with their passive counterparts. The inductance value of the AIs can be easily changed either in a continuous manner or in discrete steps; this provides flexibility in the tuning of matching circuits [60, 73]. Higher accuracy, easier layout floor-planning, small area and absence of magnetic coupling are other advantages of AIs compared to their passive counterparts.

The two transistor GAIs are realized using CS and CD stages or CS and CG stages [15]. The circuits which are implemented by CD stage, cannot achieve high Q structures but they have wide inductive bandwidth. For proper biasing they have limitations on their voltage levels which leads to negative effect on inductance tuning range [65, 74]. On the other hand structures consist of CG are suitable for low voltage and low power applications but they needs cross couple structures such as negative resistance to improve their Q factor [75]. Additionally, AIs can be designed by utilizing three or more transistors where Q factor enhancement is obtained by boosting the gain by advance circuit techniques such as regulated stages [76, 77].

The Noise of designed AIs has limited the use of them in RF applications such as LNAs [33, 34]. The main noise source of an AI is its input transistor. In order to have low noise AI, the input transistor should be designed large enough. But it leads to low Self-Resonance Frequency (SRF) which limited the inductive frequency band [78].

In this section, a low-noise and low-loss AI is presented suitable for RF low noise applications. Utilizing all transistors in CS configuration on the AI circuit leads to low conductance nodes which it causes to high Q AI. P-type MOS transistors and Feed-Forward Path (FFP) are employed to decrease noise of the AI, respectively. Circuit level implementation and performance analysis is discussed in detail in upcoming sections.

3.4.1 Circuit and Performance Description

The proposed high-Q and low-noise AI’s circuit is depicted in Figure 3.12, for which the input impedance is inductive with potentially high QF and high SRF. The parasitic capacitances and the input/output resistances of the transconductance amplifiers degrade the QF and reduce the SRF of the AI. Utilizing all the transistors in CS configuration (Figure 3.12) is a useful design figure of merit for allowing comparably low conductance at critical nodes (1 and 2), hence improved performance. The $M_{1-1}, M_{1-2}\ and\ M_2$ transistors are creating $G_1\ and\ G_2$ of GC structure, respectively. The $M_{1-1}\ and\ M_{1-2}$ are assumed to be identical. The next section describes the noise improvement of AI.

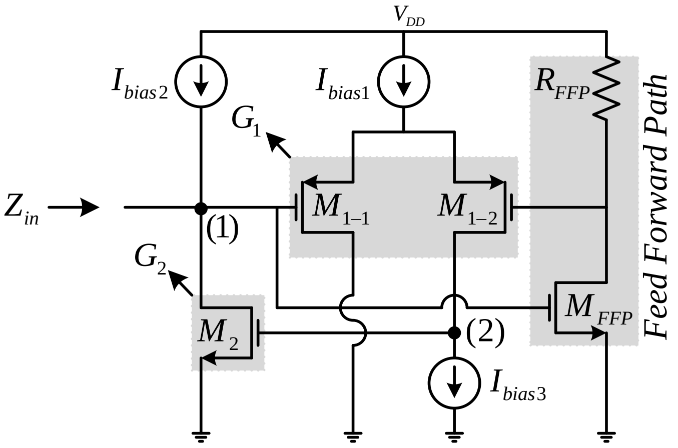


Figure 3.12 : Proposed low-noise and low-loss AI.

3.4.2 Noise improvement of Active Inductor

The flicker noise is neglected at high frequencies and the channel thermal noise is assumed to be $\overline{i_d^2} = 4kT\gamma g_{mi}$ where γ is the channel excess noise factor. The input referred noise current of the circuit shown in Figure 3.12 can be written as:

$$\overline{i_{n,(1)}^2} = 4kT\gamma\left(\frac{2}{g_{m1-1}Z_{in}^2} + g_{m2}\right) \tag{3.15}$$

It can be seen from (3.15) that minimizing g_{m2} and increasing g_{m1-1} improve the noise performance of AI. The transconductance g_{m1-1} can be increased by increasing either the channel with or the bias current of the differential pair M_{1-1} and M_{1-2}. Wider transistors lower the SRF due to larger parasitic capacitances. The bias current is also limited by the power consumption and the velocity saturation that limits g_{m1-1} at higher currents. Consequently, power and operating frequency will set an upper limit for reducing the noise due to the differential stage.

A FFP is used to improve noise performance of differential pair consisting of M_{1-1} and M_{1-2}, as shown in Figure 3.12. The modified differential pair includes the basic differential pair (M_{1-1} and M_{1-2}) and the FFP comprising the common source transistor (M_{FFP}) and its resistive load (R_{FFP}).

In order to compare the noise performance of the designed circuit without and with FFP, circuits in Figure 3.13 are used. As the effect of M_2 is same in both cases, it is neglected in noise probing. The equivalent transconductance ($G_{m,wo}$) and the output noise current (node (2)) generated by the basic differential pair can be written as (wo and w suffixes denote without and with FFP)

$$G_{m,wo} = \frac{i_{(2)}}{v_{(1)}} = \frac{g_{m,wo-1}}{2} \tag{3.16(a)}$$

$$\overline{i_{n,wo}^2} = 4kT\gamma(\frac{g_{m,wo-1}}{2}) \tag{3.16(b)}$$

While these values for the differential pair with FFP can be calculated as:

$$G_{m,w} = \frac{i_{(2)}}{v_{(1)}} = \frac{(1+R_{FFP}g_{m-FFP})g_{m,w-1}}{2} \tag{3.17(a)}$$

$$\overline{i_{n,w}^2} = \underbrace{4kT\gamma(\frac{g_{m,w-1}}{2})}_{\text{Differential Pair Noise}} + \underbrace{kT\gamma\left[\frac{a(a+\frac{1}{\gamma})g_{m,w-1}^2}{g_{m-FFP}}\right]}_{\text{Feed Forward Path Noise}} \tag{3.17(b)}$$

where $a_{FFP} = g_{FFP} \times R_{FFP}$ is the gain of FFP.

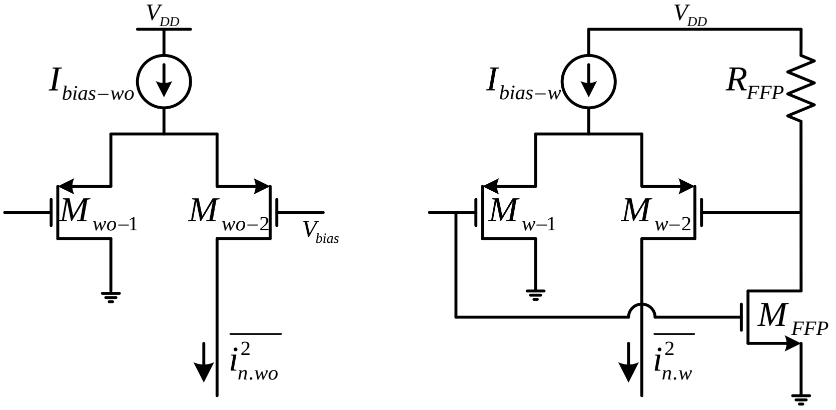


Figure 3.13 : Noise current comparison in differential pair with-without FFP.

To justice comparison, $G_{m,wo}$ and $G_{m,w}$ must be equal. From (3.16(a)) and (3.17(a)), the ratio of $g_{m,w-1}$ to $g_{m,wo-1}$ can be obtained as:

$$\frac{g_{m,w-1}}{g_{m,wo-1}} = \frac{1}{1+a_{FFP}} \tag{3.18}$$

As a result, for same overdrive voltage, the aspect ratio $(\frac{w}{l})$ of the transistors and the bias current (I_{bias}) in the circuit with the FFP can be reduced by $(1 + a_{FFP})$, i.e.,

$$I_{bias-w} = \frac{I_{bias-wo}}{1+a_{FFP}} \tag{3.19(a)}$$

$$(\frac{w}{l})_{w-1} = \frac{(\frac{w}{l})_{wo-1}}{1+a_{FFP}} \tag{3.19(b)}$$

If PR is taken as the ratio of total power consumption in the differential pair with FFP to the power consumed in differential pair itself, them the PR can be calculated as:

$$PR = \frac{I_{bias-w} + I_{FFP}}{I_{bias-wo}} = \frac{1}{1+a_{FFP}} + \frac{I_{FFP}}{I_{bias-wo}} \tag{3.20}$$

where I_{FFP} is DC current of FFP.

From (3.16, 17 and 20) the ratio of the noise current generated by a differential pair with FFP to that generated by a differential pair without FFP (NR) can be derived as:

$$\begin{gathered} NR = \frac{1}{1+a_{FFP}} + \frac{a_{FFP}(a_{FFP} + \frac{1}{\gamma})g^2_{m,w-1}}{g_{m,FFP}}, \xrightarrow[g_m \propto \sqrt{\mu c_{ox}(\frac{w}{l})I_{bias}}]{\gamma=\frac{4}{3}} \\ NR \cong \frac{1}{1+a_{FFP}} + \frac{a_{FFP}}{(1+a_{FFP})\sqrt{12k(PR(1+a_{FFP})-1)}} \end{gathered} \tag{3.21}$$

where $k = \frac{(w/l)_{FFP}}{(w/l)_{w-1}}$,

Due to (3.21), increasing k results in lower NR. But larger FFP degrades SRF of the AI owing to larger parasitic capacitance in node (1). Thus, there is trade of between SRF and NR. In Figure 3.14, the NR is plotted as a function of FFP gain (a_{FFP}) for k=1, 2 and 4.

As it can be seen in Figure 3.14, the power consumption and the noise current of the differential pair can be both reduced by the use of the FFP. It is also clear that increasing a_{FFP} does not always result in noise reduction. This is because, for a given PR and k, the noise of the FFP is proportional to a_{FFP} and when the total noise is dominated by the FFP, increasing a_{FFP} degrades the overall noise performance. Nevertheless, a_{FFP} cannot be increased arbitrarily because as the amplitude of the signals seen at the input of the differential pair increases with a_{FFP}, the circuit becomes more nonlinear.

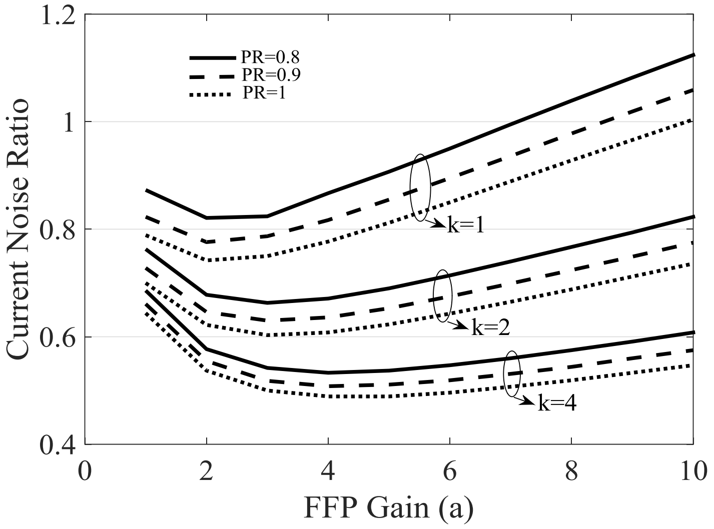


Figure 3.14 : Noise current ratio of proposed AI with FFP.

3.4.3 Proposed Active Inductor Characterization

To verify the input impedance of proposed circuit (Figure 3.12), Figure 3.15 has delineated simplified small-signal model. Where, $c_{gsi}\ and\ g_{mi}$ are gate-source capacitance and transconductance of the i-th transistor, respectively. As the c_{gsi} is in the range of femto-Farads and the g_{mi} is in $m\mho$ range, then the term $c_{gs}\,w$ is very smaller than g_m in the ≤GHz range of frequency. As a result, in the extraction of any relation from the proposed circuit, the terms consist of $c_{gs}\,w$ can be ignored in contrast to those consist of g_m. By considering this note, input admittance of the circuit of Figure 3.15 is obtained as follow:

$$Y_{in} = \frac{1}{Z_{in}} \approx \frac{1}{r_{o2}} + s\left(\frac{c_{gs,1-1}}{2} + c_{gs,FFP}\right) + \frac{1}{\left(\frac{1}{r_{o,1-2}} + sc_{gs,2}\right)\left(\frac{2}{g_{m,2}g_{m.1-1}}\right)} \tag{3.22}$$

The extracted (3.22) from small-signal model shows that the equivalent circuit of Figure 3.12 is a parallel RLC network which is depicted in Figure 3.16. The expressions of these elements can be derived as:

$$
\begin{aligned}
L &= \frac{2c_{gs,2}}{g_{m,2}g_{m.1-1}} \\
c_p &= \frac{c_{gs,1-1}}{2} + c_{gs,FFP} \\
R_p &= r_{o2} \\
R_s &= \frac{2}{r_{o,1-2}g_{m,2}g_{m.1-1}}
\end{aligned}
\tag{3.23}
$$

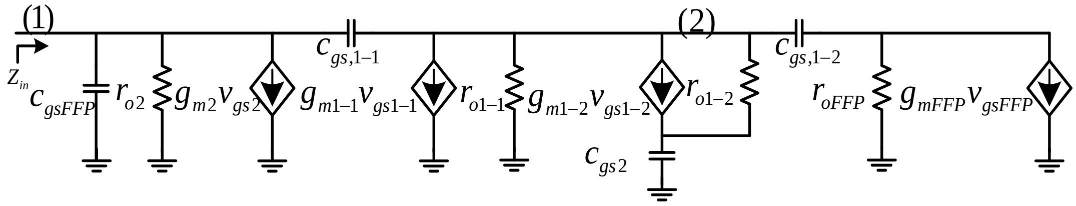


Figure 3.15 : Small-signal model of proposed AI (Figure 3.12).

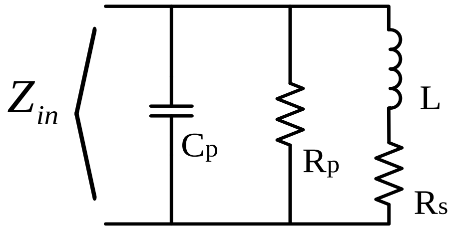


Figure 3.16 : Equivalent RLC model.

For the parallel RLC combination, if the condition $LCw^2 < 1$ is met, then it behaves like an inductor. Therefore, following relation guarantees the inductance behavior at the input node. Furthermore, the upper limit of inductive frequency range can be calculated as:

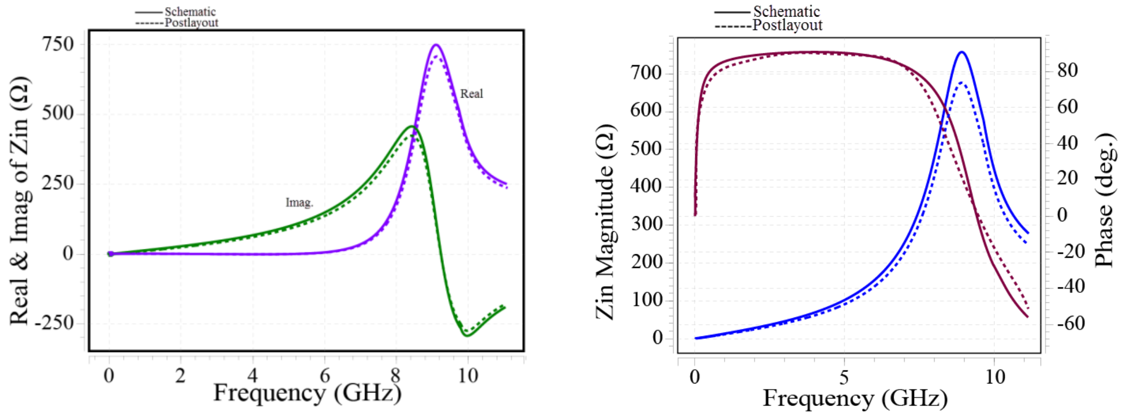
$$
SRF = \sqrt{\frac{1}{C_pL}} = \sqrt{\frac{1}{\frac{c_{gs,1-1}}{2} + c_{gs,FFP}} \times \frac{g_{m,2}g_{m.1-1}}{2c_{gs,2}}}
\tag{3.24}
$$

For the RLC parallel network equivalent model of AI, the QF in frequencies lower than SRF can be calculated as:

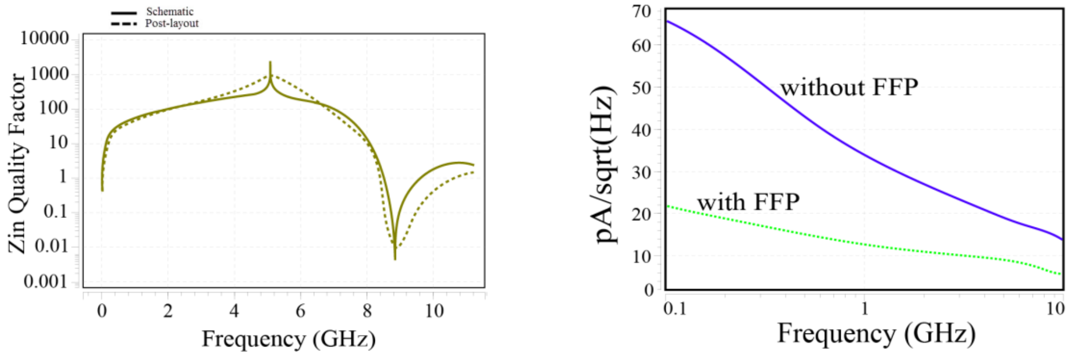
$$
Q = \frac{\mathrm{Im}\left[Z_{in}\right]}{\mathrm{Re}\left[Z_{in}\right]}
\tag{3.25}
$$

3.4.4 Simulation Results

To verify the performance of the proposed AI circuit, simulation results are presented using HSPICE with TSMC level 49 (BSIM3v3) parameters for 180 nm CMOS technology. Figure 3.17 depicts the simulation results of the proposed AI. The SRF of the structure is 9.2 GHz and maximum Q@ 5.1 GHZ is 1.25 k. The average input referred noise current and power dissipation are less than 15 pA/√Hz and 1.3 mW, respectively. Table 3.6 summarizes some important properties of the designed AI. Figure 3.18 shows layout of proposed AI which is drown by using a poly and Metal 1 with total area of 13.13×36.21 μm^2.



(a) Real and Imaginary part of Z_{in} (b) Magnitude and Phase of Z_{in}



(c) Quality factor of designed AI (d) Noise performance of proposed AI

Figure 3.17 : Proposed AI simulation results.

Table 3.6 : Proposed AI Characteristics.

CMOS Tech.	Inductor value	Inductive frequency band	Layout area μm^2
0.18 μm	35 nH	0.6-9.2 GHz	475.44
Max. QF	DC power	noise current	
1.25 k @ 5.1 GHz	1.3 mW	15 pA/√Hz	

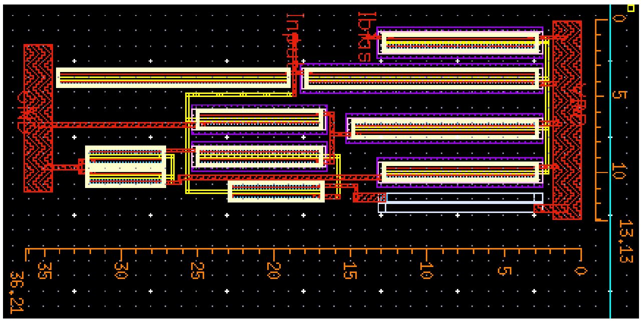


Figure 3.18 : Layout of proposed AI.

A high-Q and low-noise AI was designed based on GC topology in this section. In the proposed AI a few number of transistors was used in the main path of signal which made it suitable for RF applications. All transistors in the structure are free from body effect. The P-type differential pair input transistors and the FFP are employed to improve noise performance of AI. As characterization of AI is highly dependent on transistors' transcoductance, so changing the bias currents gives the design tunable capability. The inductance value of the design was 35 nH. Maximum Q factor was obtained 1.25k at 5.1 GHz. The DC power consumption of the proposed AI was 1.3 mW from 1.8 V dc power supply. Simulation results were provided for a 0.18 µm CMOS process. The proposed AI's layout was drawn by a poly and Metal 1(M1) with total area of 475.44 µm^2. The results show that the circuit can be used in RF applications. Table 3.7 compares the proposed AI with other reported works.

Table 3.7 : Comparison with Other AIs.

	[42]	[45]	[141]	This work
technology	90 nm/1.2 V	180 nm/1.8 V	90 nm/1 V	180 nm/1.8 V
Inductive BW (GHz)	0.6-3.8	0.645-6.3	1.7-5.5	0.6-9.2
L(nH)	165	43	26	35
Q_{Lmax}	120@3 GHz	1067@6.3 GHz	895	1.25k@5.1 GHz
P_{dis} (mW)	1.2	0.65	0.515	1.3
Noise $\boldsymbol{pA/\sqrt{Hz}}$	12	54	76	15

3.5 A New Low Loss Fully CMOS Tunable Floating Active Inductor

The well-known CMOS active inductors, based on gyrator-C networks, have been designed for applications in high-speed analog signal processing and data communication where chip area is critical and a large and tunable inductance is essential [71]. Many Tunable Grounded Active Inductors (TGAIs) and Tunable

Floating Active Inductors (TFAIs) are designed and suggested for different applications [79-82]. However, a large portion of the currently proposed AIs are initially grounded 1-port block. When 2-port floating characteristics are needed, the grounded node is made floating by using extra current sources and bypass capacitors. These FAIs do not have symmetric structure, and demonstrate different characteristics from each port, which deviates from the behavior of an ideal inductor [80, 81].

Some reported Grounded Active Inductors (GAIs) benefit from cross-coupled structure to decrease loss. Due to the negative equivalent resistance at the output of this structure, equivalent series-loss resistance at the input node of such AIs decreases [83, 84]. Some others utilize resistive feedback to increase the inductance of the AI [85, 86]. However, these structures do not give a high quality factor since the addition of the feedback resistance does not result in a low series resistance. Furthermore, these techniques do not lead to high SRFR because of adding parasitic capacitance at the input node. Moreover, these components are located in the main path of the signal which is not desired in RF applications [87]. On the other hand, some structures use positive feedback to decrease the series-resistance of AI which cause stability problems in circuit [88].

In this section, a new TFAI is designed based on modified TGAI. In the new TFAI, the MRC stages are employed to reduce the conductance at input and output nodes to enhance the Q of AI. In AIs, the SRFR of the AI is mainly determined by the gate-source parasitic capacitance of input transistor. Thus, the input transistor should be designed as small as possible in order to have high inductive frequency range. In the proposed TFAI, the SRF is improved due to the utilized MRC stages topology. Thus, the TFAI can provide higher frequency band performances. Furthermore, all transistors in the proposed circuit are n-type transistors which is desired for RF applications.

3.5.1 System Level Description

An ideal inductor can be presented in admittance form by Signal Flow Graph (SFG) with a weighted arrow (*1/sL*), as illustrated in Figure 3.19, where s is the complex frequency and L is the inductance of the inductor.

Current flowing through the inductor is described by the following equation:

$$I_L = (1/sL)V_L \qquad (3.26)$$

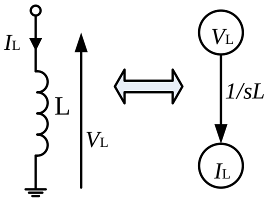


Figure 3.19 : An ideal inductor and SFG representation.

The same transfer function can be obtained by constructing a graph with one capacitor and two VCCS as shown in Figure 3.20.

In order to have high impedance in both input and output nodes, SFG of GAI is modified according to Figure 3.21(a). Figure 3.21(b) depicts floating counterpart of GAI.

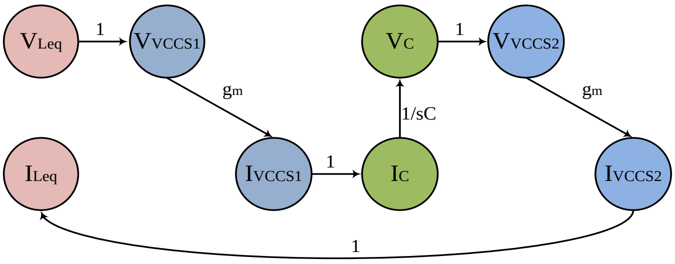


Figure 3.20 : General SFG for AI’s circuit generation with VCCS.

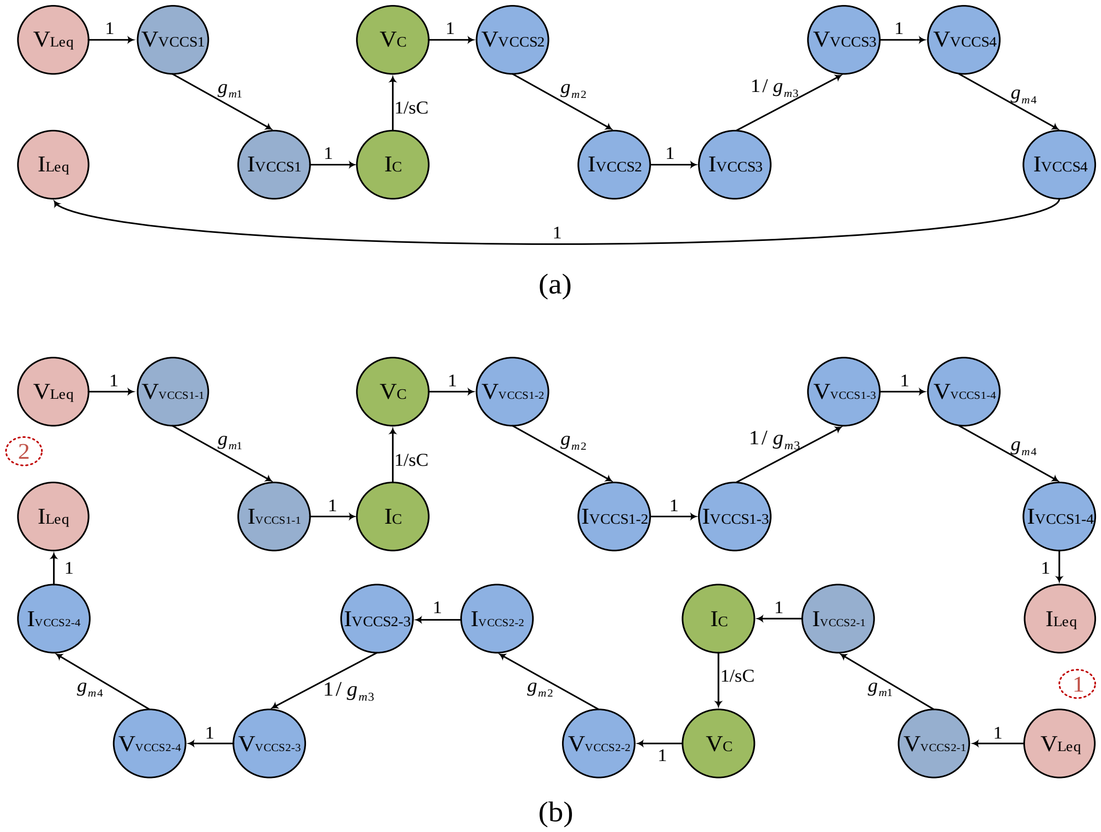


Figure 3.21 : Modified SFG (a) GAI, (b) FAI.

Thus, the SFG of Figure 3.21 is described by equation (3.27) for both grounded and floating AI:

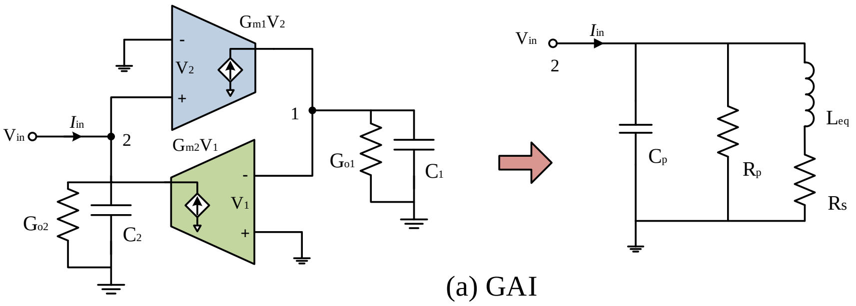
$$I_{Leq} = (1/SL_{eq})V_{Leq} = g_{m1}g_{m2}g_{m4}\big/g_{m3}(sC)V_{Leq} \qquad (3.27)$$

where

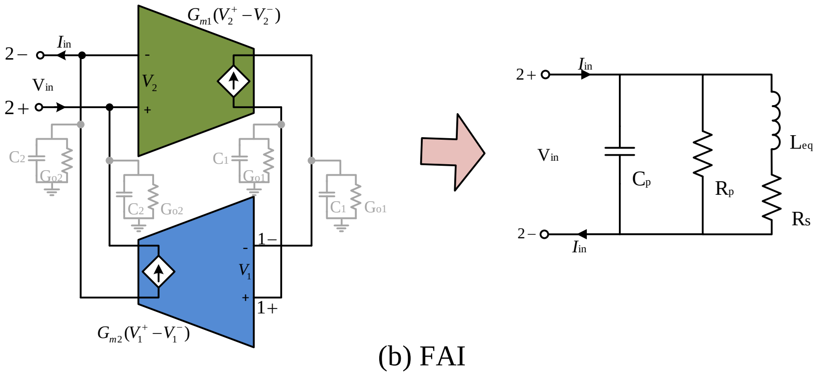
$$L_{Leq} = \frac{g_{m3}C}{g_{m1}g_{m2}g_{m4}} \qquad (3.28)$$

Accordingly, inductors can be synthesized by Gyrator-C (GC) blocks as illustrated in Figure 3.22. These types are named as GC active inductors. The inductance of gyrator-C active inductor is directly proportional to the load capacitance *C* and inversely proportional to the product of trans-conductors of the gyrator [89].

The SFGs presented in Figures 3.20 and 3.21 can be designed using two classical Operational Transconductance Amplifiers (OTAs). Figures 3.22 (a, b) presents a lossy grounded and floating inductors, respectively. In Figure 3.22. C_1, C_2, G_{o1} and G_{o2} represent the total capacitances and conductances at nodes 1 and 2, respectively.



(a) GAI



(b) FAI

Figure 3.22 : Block diagram of AI realization by OTA and equivalent passive model (a) Grounded (b) Floating.

In comparison of Figures 3.21 and 3.22, the transconductance of the OTAs can be written as:

$$G_{m1}=g_{m1}\ ,\ G_{m2}=\frac{g_{m2}g_{m4}}{g_{m3}} \tag{3.29}$$

Floating GC AIs have some benefits in contrast with their GAI counterparts [89]:

I. There are appropriate for circuits in which digital and analog parts are manufactured in the same substrate because of their differential configuration. The differential transconductors effectively reject the common-mode disturbances of the network.

II. Input voltage swing of FAIs is twice larger than their GAIs counterparts.

The parasitic components of AI (Figure 3.22) limit the inductive behavior frequency range. This frequency range can be obtained by examining the impedance of the RLC equivalent circuit of the lossy active inductor (Figures 3.22(a and b)).

$$Z_{in}=\left(\frac{R_s}{C_pL_{eq}}\right)\frac{s\dfrac{L_{eq}}{R_s}+1}{s^2+s\left(\dfrac{1}{R_pC_p}+\dfrac{R_s}{L_{eq}}\right)+\dfrac{R_p+R_s}{R_pC_pL_{eq}}} \tag{3.30}$$

When complex conjugate poles are encountered, the pole resonant frequency of Z_{in} is given by:

$$\omega_p = \sqrt{\frac{R_p + R_s}{R_p C_p L_{eq}}} \tag{3.31}$$

Because $R_p \gg R_s$, Eq. (6) is simplified to:

$$\omega_p \approx \sqrt{\frac{1}{C_p L_{eq}}} = \omega_0 = SRF \tag{3.32}$$

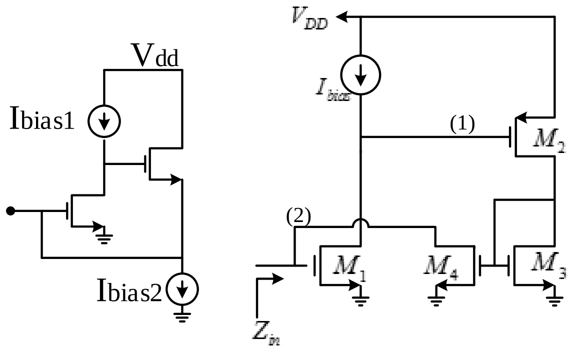
where, ω_0 is the self-resonant frequency of the active inductor. Also observe that Z_{in} has a zero at the frequency.

$$\omega_z = \frac{R_s}{L_{eq}} = \frac{G_{o1}}{C_1} \tag{3.33}$$

It is evident that the gyrator-C network is resistive, when$\omega \leq \omega_z$, inductive when $\omega_z \leq \omega \leq \omega_0$, and capacitive when $w \geq w_0$. The frequency range in which the gyrator-C network is inductive is lower-bounded by ω_z and upper-bounded by ω_0. Also it is observed that R_p has no effect on the frequency range of the active inductor. R_s, however, affects the lower bound of the frequency range over which the gyrator-C network is inductive. The upper bound of the frequency range is set by the self-resonant frequency of the active inductor, which is set by the cut-off frequency of the transconductors constituting the active inductor. For a given inductance L_{eq}, in order to maximize the frequency range, both R_s and C_p should be minimized.

3.5.2 Circuit Level Design

The basic CMOS implementation of SFG which presented in Figure 3.20, is depicted in Figure 3.23(a). According to SFG in Figure 3.21(a), the circuit implementation of GAI can be modified as Figure 3.23(b). All transistores are n-type except M_2, which is desired in RF applications.



(a) (b)

Figure 3.23 : Simplified CMOS-based GAI (a) basic, (b) modified.

In modified GAI, the negative transconductance is realized by M_1 in common-source configuration, whereas M_2, M_3 *and* M_4 form the positive transconductance where the simple current mirror comprised of M_3 *and* M_4 is used to invert the negative transconductance of M_2, also configured in CS connection. Since the sole contribution practically comes from a minimum number of MOS transistors drain terminals, this configuration allows low equivalent conductances especially at node (1) which results in enhancement of QF by decreasing series resistance of equivalent inductance. Furthermore it results bigger inductance value. The QF can be obtained as [60, 89]:

$$Q = \frac{\mathrm{I}M[Z]}{RE[Z]} \tag{3.34}$$

The quality factor of a lossy gyrator-C active inductor can be derived directly from (3.30) and (3.34) as:

$$Q = \left(\frac{\omega L_{eq}}{R_s}\right) \frac{R_p}{R_p + R_s\left[1 + \left(\frac{\omega L_{eq}}{R_s}\right)^2\right]} \times \left[1 - \frac{R_s^{\,2} C_p}{L_{eq}} - \omega^2 L_{eq} C_p\right] \tag{3.35}$$

The sensitivity of the quality factor of the active inductor is merely depends on R_s in high frequencies. In order to boost the quality factor of active inductors, R_s must be decreased. Reducing R_s is done by using advanced circuit techniques, such as MRC stage. The MRC stage is effective in lowering the output conductance and can be used here to reduce R_s, as shown in Figure 8 [15]. In the proposed circuit M_n, M_{c-n} and M_{b-n} transistors are used for main elements of Gyrator-C, MRC stage and biasing, respectively.

MRC stage is made up of PMOS transistors in order to:

- Minimize the input transistor as small as possible in order to control second stage biasing,
- Decrease the number of transistors in main path of AC signal.

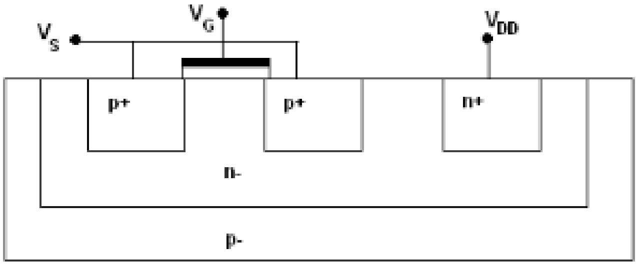
Table 3.8 shows equivalent resistance at node (1), with and without MRG stage in modified GAI (Figure 3.25).

Table 3.8 : Equivalent resistance with-without MRC stage.

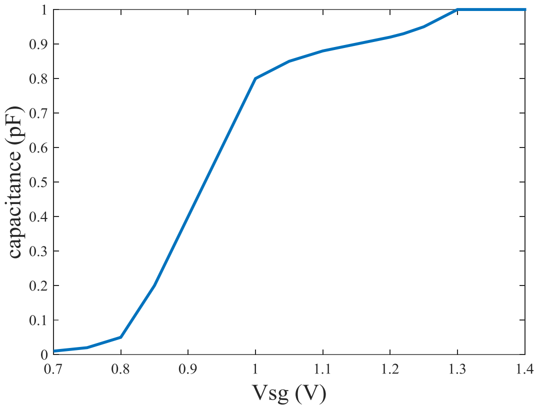
Node (1) (Figure 3.25)	resistance
Without MRC	$r_{o,1}//r_{o,b-2}$
With MRC	$r_{o,1}//(r_{o,b-2}r_{o,c-1}g_{m,c-1}r_{o,c-2}g_{m,c-2}r_{o,c-3}g_{m,c-3}) \cong r_{o,1}$

It can be seen from Table 3.8, by adding MRC stage, the resistance enhancement is achieved. This stage can be employed at the input-output (1&2) nodes in order to decrease the conductance which affects the performance of the AI.

The tunability of the AI is enhanced by variation of bias current (I_{bias}) and varactor capacitance value ($C_{varactor}$). Varactor in CMOS technology is implemented by diode and MOS transistors. PMOS is usually employed to implement varactor. Working with a p-MOS transistor structure, the bulk is connected to the highest voltage of the circuit (V_{dd}) and the capacitor is formed between the gate and the drain and source. As the n-well connection of the device is always connected to the highest possible voltage, the gate voltage shall be equal or lower to the bulk voltage and the transistor is working always in the inversion zone (I-MOS) (Figure 3.24(a)). The characteristic of this device is monotonic and non-linear, and the transition between the minimum possible capacitance (C_{min}) to the maximum one (C_{max}) is very sharp. It is clearly visible the sharp slope of the curve, which means that with a small variation of the bias voltage the capacitance changes considerably. Here the transition from C_{min} and C_{max} happens in 595 mV bias voltage variation [90, 91].



(a) Physical structure



(b) Capacitance variation versus Vsg

Figure 3.24 : I-MOS varactor.

Figure 3.26 demonstrates small-signal model of the proposed structure (Figure 3.25) in order to verify the input impedance characterization. In this figure, c_{gsi} and g_{mi} are gate-source capacitance and transconductance of the ith transistor, respectively. The input admittance of the circuit of Figure 3.26 is calculated as follows:

$$Y_{in} = \frac{1}{Z_{in}} = sc_{gs1} + \frac{1}{r_{o4}} + \frac{1}{\dfrac{g_{m3} \times sc_{gs2}}{g_{m1} g_{m2} g_{m4}} + \dfrac{g_{m3}}{r_{o1} g_{m1} g_{m2} g_{m4}}} \tag{3.36}$$

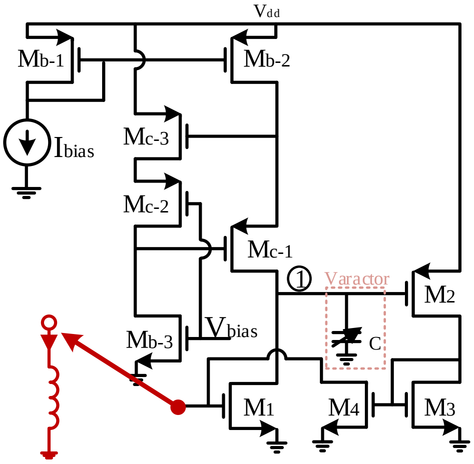


Figure 3.25 : Modified GAI.

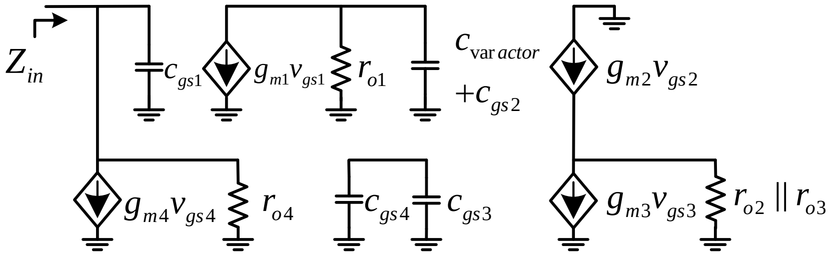


Figure 3.26 : Small-signal equivalent of proposed GAI.

By considering the SFG (Figure 3.21(b)) and block diagram (Figure 3.22(b)) of FAI, the floating counterpart of proposed GAI is designed in Figure 3.25. Standard circuit analysis techniques yield the important parameters of the grounded and floating AI as follows:

$$R_p = r_{04}\,,\; R_s = \frac{1}{g_{m1}\dfrac{g_{m2}g_{m4}}{g_{m3}}r_{o1}}\;,\; C_p = c_{gs1}\;,\; L_{eq} = \frac{c_{gs2} + c_{\mathrm{var}\,actor}}{g_{m1}\dfrac{g_{m2}g_{m4}}{g_{m3}}} \tag{3.37}$$

The aspect ratio of transistors in proposed FAI circuit is given in Table 3.9.

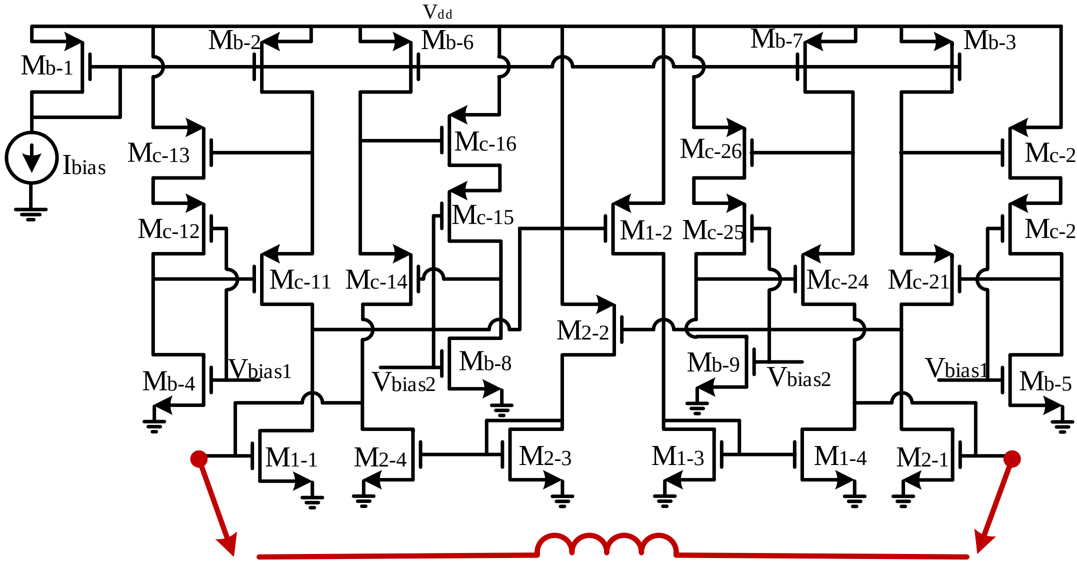


Figure 3.27 : Circuit implementation of the proposed FAI.

It can be seen from Figure 3.27 and Table 3.9 that the designed FAI is completely symmetrical from both ports, which it results in the same properties from both sides. The MRC stage not only used in input node but also used in output node, which leads to performance enhancement.

Table 3.9 : Transistors aspect ratio of proposed circuit.

Transistor name	W/L (µm/ µm)
M_{1-1} , M_{2-1}	4.8/0.18
M_{1-2} , M_{2-2}	16.5/0.18
M_{1-3} , M_{2-3}	5/0.18
M_{1-4} , M_{2-4}	6.1/0.18
M_{c-11} , M_{c-21}	10.9/0.18
M_{c-12} , M_{c-22} , M_{c-13} , M_{c-23}	5.2/0.18
M_{c-14} , M_{c-24}	11.3/0.18
M_{c-15} , M_{c-25} , M_{c-16} , M_{c-26}	5.9/0.18
M_{b-n} n=1,2,3,6,7	10/0.2
M_{b-n} n=4,5	3.7/0.18
M_{b-n} n=8,9	3.9/0.18

3.5.3 Simulation Results

The proposed GTAI and FTAI are designed and simulated using the AMS 0.18um CMOS process in Cadence. The width of the transistors, the values of I_{bias} and $C_{varactor}$ are chosen to optimize the quality factor and inductance value of the AI.

The simulated frequency response of the GAI is given in Figure 3.28. The proposed circuit has a very high operating bandwidth where the inductive characteristic extends from 100 MHz up to the self-resonance frequency at 6.2 GHz which makes it suitable for RF applications. Also, Figure 3.28 compares GAI with and without MRC stage.

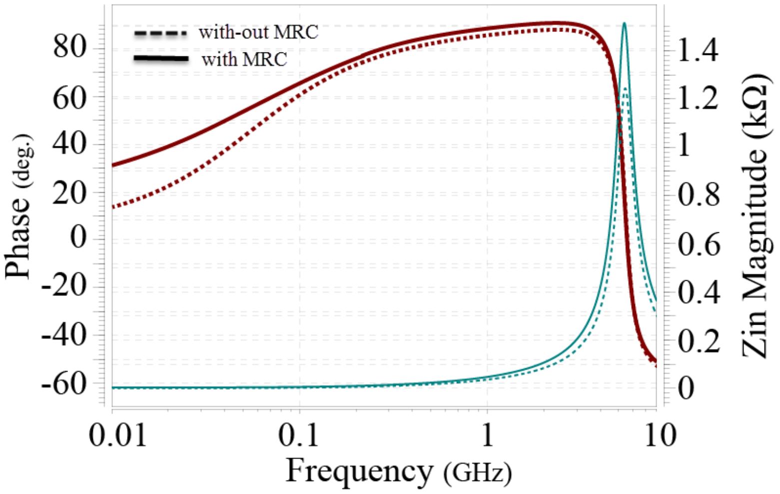


Figure 3.28 : Comparison AI circuits with and without MRC stage (magnitude and phase).

For investigating the FAI performance, Figure 3.29 configuration is used for simulation of ideal and CMOS FAI. The simulation result is shown in Figure 3.30.

Quality factor is tuned through the controllable bias current source (I_{bias}) of Figures 3.25 and 3.27. Figure 3.31 shows the variation of inductance for different values of controllable bias current source and varactor capacitance. As seen from this figure, the inductance increase is controlled via bias current by the same load capacitance. On the other hand, for constant bias current the effective inductance can be tuned by changing the varactor capacitance value.

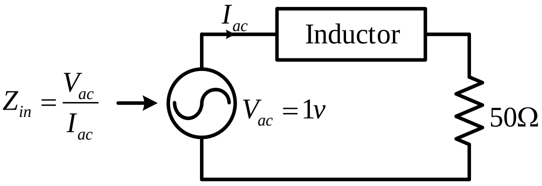
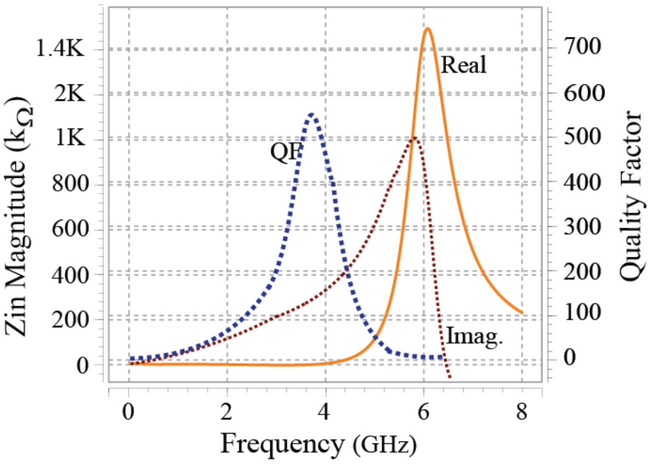
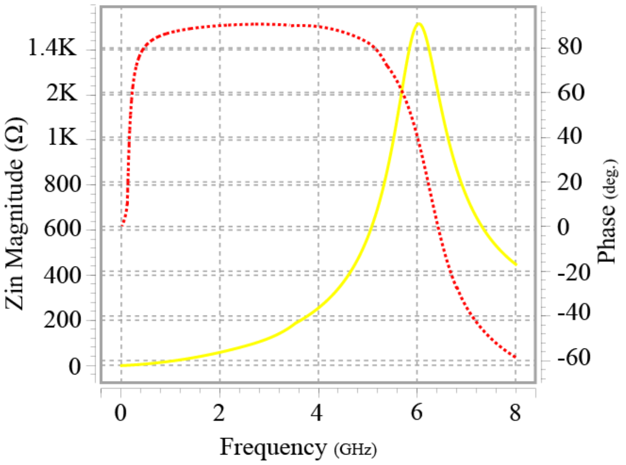


Figure 3.29 : Circuit for FAI simulation.



(a)



(b)

Figure 3.30 : Performance of proposed AI, (a) real and imaginary parts and QF, (b) magnitude and phase.

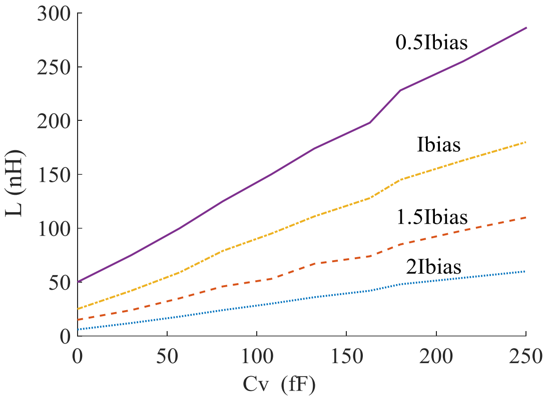


Figure 3.31 : Tunability of AI by changing bias current and varactor capacitance.

By adjusting the bias current and varactor capacitance, the QF and SRF can be optimized for each inductance value. Table 3.10 shows optimized QF and SRF for some inductance values.

Table 3.10 : Optimized Q and SRF value for different inductance values.

L	Q		SRF (GHz)	
(nH)	calculation	simulation	calculation	simulation
6	1000	567@3.7GHz	10.4	6.2
50	700	456@3.5GHz	7.1	4.6
100	800	534@2.6GHz	6	3.3
200	900	498@1.9GHz	4.2	2.3
286	650	397@1.4GHz	2.4	1.6

In order to check the robustness of the proposed FAI circuit versus process variation, the Monte Carlo simulation with 200 iterations is done for specified inductance value by applying ±5 % Gaussian distribution at ±3σ level in the variation of transistors aspect ratio and threshold voltage. Regarding to Figure 3.32, 69% of the total samples occurred with the relative error of less than ±1.5 %, while in the worst case 21% of samples lead to the error of more than ±2 %. Figure 3.33 shows layout of the proposed FAI, which is drawn by Cadence software using single poly and metal (M1) with the total area of 26.1×35.8 μm^2. As seen from layout configuration, the FLA is completely symetric, which results the same characterization from both ports of AI. Figure 3.34 depicts the schematic and post-layout simulation results. Table 3.11 compares the performance of the proposed FAI with the previous ones.

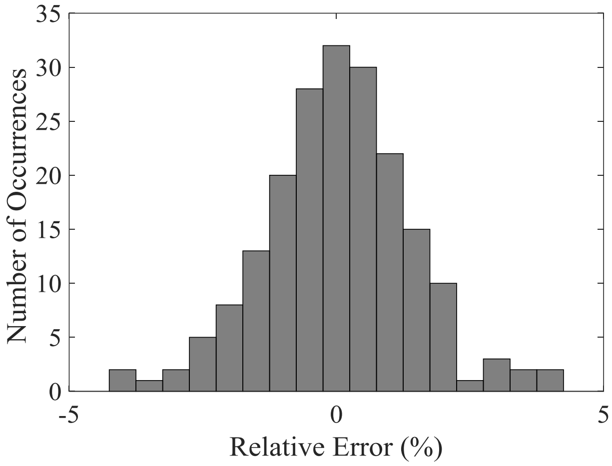


Figure 3.32 : The result of Monte Carlo analysis of GC circuit for ±5 % mismatch in transistors aspect ratio and threshold voltage (No. of iterations = 200).

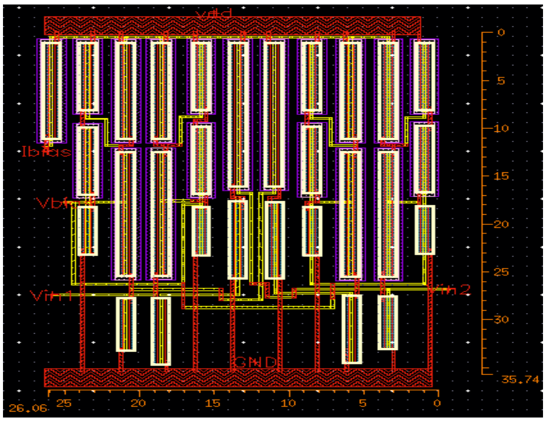


Figure 3.33 : Layout of the proposed FAI.

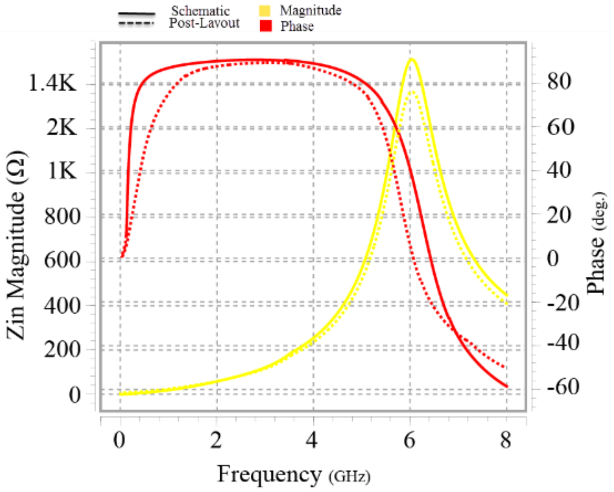


Figure 3.34 : Maginitude and Phase of AI (schematic and post-layout simulation).

Table 3.11 : Comparison with other FAIs.

Ref	CMOS process	V_{dd} (V)	L (nH)	Q	Inductive Frequency Range (GHz)	Area (μm^2)	DC Power Consumption (mW)
[71]	TSMC-0.18 um	1.8	-	40–200	0.375 – 2	-	3
[142]	AMS-0.8um	3	294-394	-	1	-	8.6
[79]	0.35 um	3.3	685uH-12.4mH	-	0.25-0.75	170×10^3	2
[55]	TSMC-0.18 um	1.8	33	68	4	810	3.6
[57]	TSMC-0.13 um	1.2	1.9	38.8	3.5	2600	6.4
This work	AMS-0.18 um	1.8	6-284	10-567	0.1-6.2	934.4	2

A new high Q, tunable floating active inductor was designed based on modified TGAI in this section. The proposed AI was designed on Gyrator-C topology and used a few number of transistors in the main path of signal, which made it suitable for RF applications. A CMOS varactor in the AI circuit was used to adjust the inductance value from few nH to 284 nH in the specific frequency range. Q factor can be tuned by changing bias current from 10 to 567. The DC power consumption of the proposed AI was 2 mW from 1.8 V dc power supply. Simulation results were provided for a 0.18 um CMOS-AMS process. The results show that the circuit can be used in RF applications for frequency band 0.1-6.2 ranging in the 100 MHz~6.2 GHz frequency band. Total area consumption of the structure is 934.4 μm^2. Comparison shows that our circuit has minimum power consumption, maximum BW and QF.

3.6 Chapter Summery

An examination of the principles, topology, characterization and implementation of GC AIs in CMOS technology has been presented. It is shown that both grounded and floating AIs can be synthesized and implemented by using GC networks. To provide a quantitative measure of the performance of active inductors, a number of figure-of-merits have been introduced. In a low loss GAI, MRG stages are employed to lower conductance of input and output nodes. The RC feedback and cascoding techniques are used to design a high performance AI with ability to adjust its SRF, QF and inductance value independently. FFP and p-type differential input transistors are utilized to design low noise AI and based on low loss GAI, a FAI is designed.

4. CMOS GYRATOR-C ARCHITECTURES APPLICATIONS

In order to show workability of the designed circuits based on in previous chapter, they are used in three applications. All designed AIs are based on GC architecture which it converts a capacitance to large impedance. On the other hand, micro sensors convert mechanical signal to capacitance variation in fF range.

4.1 A 3-Axis Accelerometer With an Accurate CMOS GC Based Interface Circuit

The capacitive based micro sensors convert mechanical signals to small capacitance variation. The capacitance variation in micro sensor is in the range of femto-Farads which makes it difficult to sense. On the other hand, the Gyrator-C topologies can convert a low capacitance variation to high impedance changing which makes it a good choice for being interface circuits for capacitive sensors. Then a new 3-axis accelerometer with ability to cancel cross section sensitivity is designed. The sensor's electrodes are located in such a way that enables the structure to detect acceleration in all axis independently. Consequently, a new GC configuration for sensing very small capacitance changes in a capacitive sensor is presented. In the proposed configuration, the operating frequency range and Scaling Factor can be adjusted without affecting each other by tuning the bias currents. In addition, the proposed configuration employs RC feedback and cascading techniques to cancel the effect of the parasitic components.

4.1.1 A 3-Axis MEMS Capacitive Accelerometer Free of Cross Axis Sensitivity

An accelerometer is a sensor that measures the physical acceleration experienced by an object due to inertial forces or due to mechanical excitation. Designing sensors with MEMS technology have advantages of miniaturization, low cost, low power and good dynamic characteristics. Accelerometers as a major member of MEMS sensors, have been broadly used in different applications such as: vibration checking systems, inertial guidance, mobile devices, biomedical and automotive applications [92-100].

The accelerometers are classified due to their sensing method for example: tunneling, piezoelectric, pizoresistive and capacitive [92, 93, 98]. The capacitive sensors are preferred in microelectronics because of their compatibility to CMOS technology, less thermal sensitivity, high accuracy, low power consumption and low noise [93, 94, 99, 100].

Capacitive position sensing is done by interdigitated comb electrodes. They have become an integral part of many MEMS devices such as pressure sensors, gyroscopes and accelerometers. However, lateral accelerometers have been developed using comb electrodes and differentially detecting parallel electrodes to obtain linear output. The use of vertical capacitance change between comb fingers is limited by parasitic capacitance among fixed and movable electrodes and electrical isolation difficulties. There are many reported accelerometers in literature but most of them are one or two axis sensors [3, 5] and usually they suffered from cross axis sensitivity which decrease device performance. For detecting acceleration in more than one direction, generally designers use more than one proof mass i.e. for each direction a proof mass is embedded [95, 97].

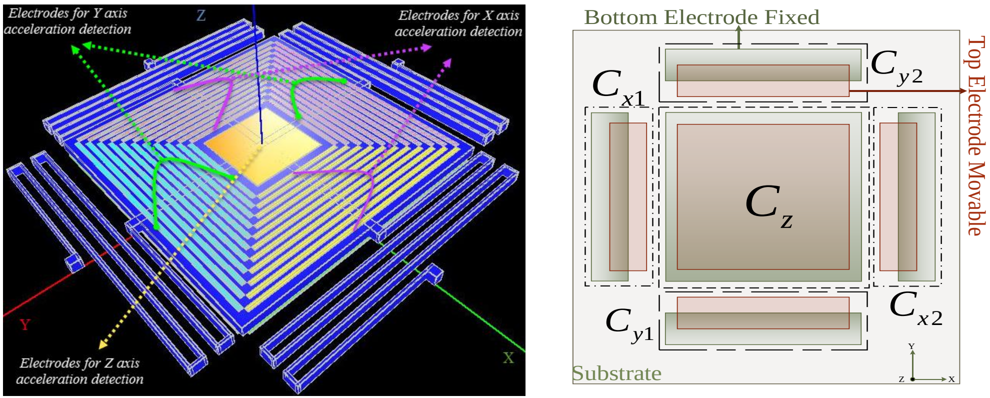
In this work to measure acceleration on 3-axis, it is proposed a unique configuration of electrodes which enables the sensor to measure acceleration in multi axis by one proof mass. The presented structure eliminates cross axis sensitivity in all directions of capacitive micro-machined accelerometer. Upcoming section describes the device operational principles and structural design. Next, simulation results are exhibited and then suggested fabrication process is explained.

4.1.1.1 Operation Principles and Structural Design

According to [92] rectangular shape is good choice due to its moderate displacement and capacitance variation compared to others. Consequently, it is choosen for designing proposed sensor. The whole suggested design is shown in Figure 4.1(a). The vertical and horizontal comb electrodes are designed to sense acceleration in X and Y axis, respectively. However, the central Square shape electrode is embedded to detect acceleration in Z axis direction. Capacitance variation in X and Y directions is due to area changing between fixed and movable electrodes but in Z axis is due to distance changing between them. This structure is free of cross axis sensitivity in all directions. The movable electrode fingers are smaller than their fixed counterparts which enable the device to detect 3-axis accelerations without any interface on each other. To the best of authors' knowledge, this is first time a 3-axis accelerometer is designed free of cross axis sensitivity.

To show eliminating cross axis sensitivity by new configuration, the simple capacitance relation (C=kA/D), is used. As the structure measures acceleration in 3-axis, so the investigation should be done for all directions separately. Calculations for applied acceleration in X and Y axis electrodes due to similarity is the same, thus calculation is done for X axis. The capacitance variation is calculated in four conditions:

1. Applied acceleration is in plane (X or Y),
2. Applied acceleration is in out plane (Z),
3. Applied acceleration is in both out & in plane (Z&X or Z&Y),
4. Applied acceleration is in three directions(X&Y&Z)



(a) (b)

Figure 4.1 : Proposed Structure, (a) 3D view, (b) Electrodes Arrangement (2D, top view).

Since for each of mentioned states the capacitive changing is detected by separated electrodes, then the electronic circuit can easily detects acceleration orientation.

4.1.1.2 Applied Acceleration Is In One Direction

Figure 4.1(b) shows sample of electrodes embedded for acceleration detecting on 3-axis. Since movable electrodes are smaller than their fixed counterparts, then Y and Z electrodes do not sense applied acceleration in X axis. This results in eliminating cross axis sensitivity completely. If it is considered that the acceleration applied just in X axis in positive direction, then total capacitance changing after acceleration applying can be calculated as:

$$\Delta c = c_{x2,x} - c_{x1,x} = k\left(\frac{A+\Delta a}{D} - \frac{A-\Delta a}{D}\right) = k\frac{2\Delta a}{D} \tag{4.1}$$

Where in ($C_{\Delta ⌂,\square}$), Δ defines the axis which capacitance is belong to, ⌂ shows number of capacitance and □ denotes the axis which acceleration is applied in. Since $C_{X2,X}$ is increased and $C_{X1,X}$ is decreased, the analyzing part can easily detect the acceleration orientation. For Y axis, it is like as X case. If the acceleration is applied in positive Z direction, then the governing equations for the capacitance variation will be:

$$\frac{1}{\Delta c_Z} = \frac{1}{\mathrm{c}_{Z,Z}} - \frac{1}{c_Z} = \frac{D+\Delta d}{kA} - \frac{D}{kA} = \frac{\Delta d}{kA} \tag{4.2}$$

4.1.1.3 Applied Acceleration Is In Two Directions

If the acceleration is exerted to two-axis (out & in plane), two circumstances occur, XZ and YZ. For XZ case, capacitance calculations are as:

$$\Delta c_x = c_{x2,xz} - c_{x1,xz} = k\left(\frac{A+\Delta a}{D} - \frac{A-\Delta a}{D}\right) = k\frac{2\Delta a}{D} \tag{4.3(a)}$$

$$\frac{1}{\Delta c_Z} = \frac{1}{\mathrm{c}_{Z,XZ}} - \frac{1}{c_Z} = \frac{D+\Delta d}{kA} - \frac{D}{kA} = \frac{\Delta d}{kA} \tag{4.3(b)}$$

In Y direction electrodes, there is not capacitance changing. The YZ case is same as XZ.

4.1.1.4 Applied Acceleration Is In Three Directions

If acceleration is applied in 3-axis i.e. XYZ, capacitance variation calculation in all orientations are as:

$$\Delta c_x = \frac{c_z}{c_{z,xyz}}(c_{x2,xyz} - c_{x1,xyz}) = k\frac{D+\Delta d}{D}\left(\frac{A+\Delta a}{D+\Delta d} - \frac{A-\Delta a}{D+\Delta d}\right) = k\frac{2\Delta a}{D} \tag{4.4(a)}$$

$$\Delta c_y = \frac{c_z}{c_{z,xyz}}(c_{y2,xyz} - c_{y1,xyz}) = k\frac{D+\Delta d}{D}\left(\frac{A+\Delta a}{D+\Delta d} - \frac{A-\Delta a}{D+\Delta d}\right) = k\frac{2\Delta a}{D} \tag{4.4(b)}$$

$$\frac{1}{\Delta c_Z} = \frac{1}{\mathrm{c}_{Z,XYZ}} - \frac{1}{c_Z} = \frac{D+\Delta d}{kA} - \frac{D}{kA} = \frac{\Delta d}{kA} \tag{4.4(c)}$$

By comparing all states, it can be seen that capacitance variation for all of them in each axis is same. In other words the sensor is capable to eliminate cross axis sensitivity in all directions.

4.1.1.5 Fabrication Process

As suggested structure is design by the aim of automotive application, the dimensions should be accurate. Consequently surface micromachining is selected to fabrication process. Surface micromachining fabrication process for suggested device can be written as:

1. Thermal wet oxidation (200nm),
2. Al evaporation for bottom electrode (0.5um),
3. Al pattern (forming bottom electrodes),
4. Spin photoresist for air gap and lithography (2um),
5. Polysilicon deposition by LPCVD (proof mass, 5um),
6. Sio2 deposition by LPCVD (to form dielectric of proof mass),
7. Sio2 and polysilicon pattern (forming proof mass),
8. Al evaporation for top electrode (0.5um),
9. Al pattern (forming top electrode),
10. Releasing the structure (plasma ashing)

The final 2D structure is depicted in Figure 4.2. The Y orientation electrodes cannot be seen in cross section view.

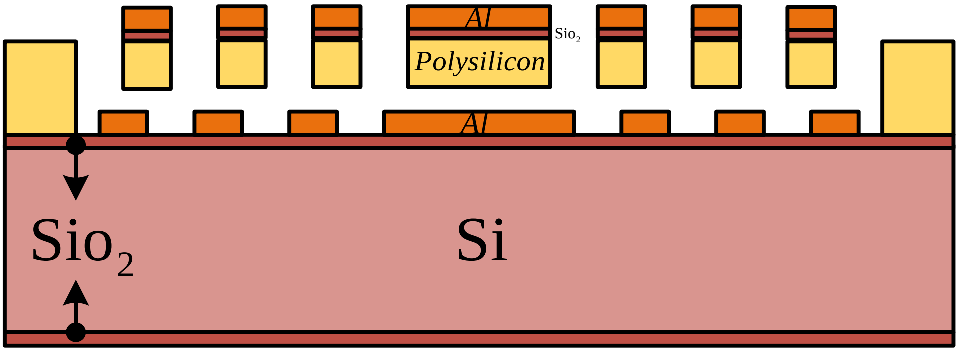


Figure 4.2 : Cross section view of final structure.

4.1.1.6 Simulation Results

The simulation of the designed accelerometer is done by a MEMS-specific CAD tool named IntelliSuite. Figures 4.3(a and b) depict displacement and capacitance variation versus applied acceleration for 3-axis, respectively. The crucial characteristics of the accelerometer are given in Table 4.1.

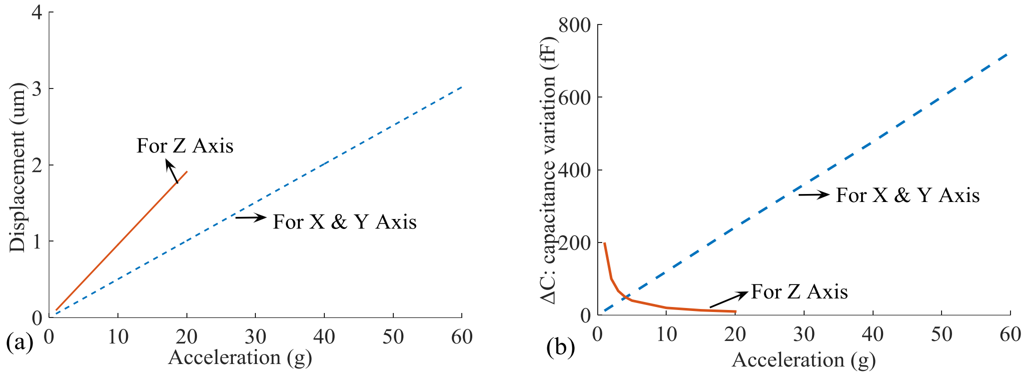


Figure 4.3 : (a)Displacement versus applied acceleration in 3-Axis, (b)Capacitance variation versus applied acceleration in 3-Axis

Table 4.1 : Accelerometer Characteristics

Acceleration measuring axis		X, Y and Z
Mass		22.81 µgram
Range of measurable acceleration	X and Y	±67 g
	Z	±18 g
Spring constant in	X and Y	633.52
	Z	239.27
Sensitivity in	X and Y	12 fF/g
Total size		1.85 mm^2

A new 3-axis acceleration’s structure, fabrication process and simulation results are explained. The figure of merit of design was its entirely eliminating cross axis sensitivity. Furthermore, it could be measured acceleration in 3-axis with only one proof mass. On the other hand, in 3-axis, the applied acceleration has a linear relationship with the result of part II which is easily calculated by processing electronic circuits. The designed sensor is suitable for automotive application, therefore surface micromachining is chosen for fabrication process.

4.1.2 An Accurate CMOS Interface Capacitance Variation Sensing Circuit

The capacitive sensing method is a popular method compare to other sensing methods in the sensors. Its popularity comes from low thermal sensitivity, high accuracy, low power dissipation and it can be integrated with CMOS process for electronic sensing part [101, 102]. CMOS has been the dominant Integrated Circuit (IC) design technology for more than two decades, which offers great advantages including low power consumption, ability to make analog and digital circuits on the same chip and easy of technology scaling. The integration of sensing and analysing parts results in a high accurate and more reliable device.

The capacitance variation in micro sensor is in the range of femto-Farads (fF) which makes it difficult to sense [102, 103]. There are many reported works in order to design interface circuits for capacitive sensors [104-107]. Most of them have used front-end switched capacitor charge amplifier in the entrance gate of the interface circuit [104]. This method needs to add clocking part for analysing which makes the system more complex. On the other hand adding extra components such as sampling capacitors, active rectifiers and filters to the design, increases the parasitic components which in turn degrade performance of the sensing circuit [105, 106]. Some interface capacitance readout circuits need to employ floating variable capacitance which is not practical in some applications such as sensor because of serious problem in implementation phase [104, 105].

Gyrator-C (GC) topologies can convert a low capacitance variation to high impedance changing. Inevitable parts of these topologies are their parasitic components. There are different modified version of GC topologies in the literature for minimizing the parasitic effects [108, 109]. These methods have some disadvantages such as their need to extra biasing parts which causes extra power consumption and more noise, and their limitation of the input signal swing.

This section presents a new GC configuration for sensing very small capacitance changes in a capacitive sensor. In the proposed configuration, the operating frequency range and Scaling Factor (SF) can be adjusted without affecting each other by tuning the bias currents. In addition, the proposed configuration employs RC feedback and cascading techniques to cancel the effect of the parasitic components.

4.1.2.1 Circuit Description

Figure 4.4 shows GC topology which is implemented by ideal operational transconductance amplifier as a basic block. The input impedance of the circuit can be written as:

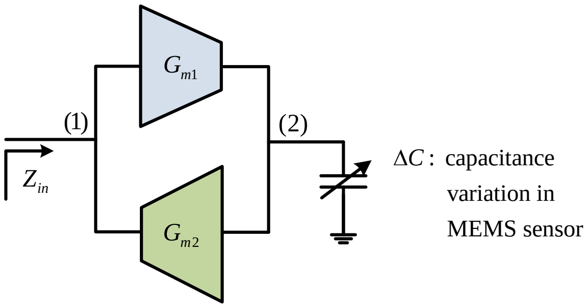


Figure 4.4 : Gyrator-C topology.

$$Z_{in} = \frac{sC}{G_{m1}G_{m2}} \tag{4.5}$$

According to (4.5), SF is $\mathbf{1/G_{m1}G_{m2}}$. If we suppose $\boldsymbol{G_{m1} = G_{m2} = 1\ m℧}$ then the SF will be $\mathbf{10^6}$. In other word, 1 fF capacitance variation is as a 1 nH changing in input impedance. In Figure 4.4, nodes (1) and (2) are critical in term of determining circuit performance. The RC feedback and cascading techniques are employed for parasitic resistance cancellation in node (2) and parasitic capacitance controlling in node (1), respectively.

4.1.2.2 Proposed Circuit

Figure 4.5 shows the proposed capacitance scaling structure. The G_{m1} in Figure 4.4 is mainly determined by transistors M_2 and G_{m2} is created with M_4. In order to guarantee the stability and adjust operating frequency range of the GC structure, cascade input transistors (M_1 and M_2) are employed.

In MOS transistors, gate-source capacitance and transconductance are directly proportional to size of the transistor. Input gate-source capacitance component (c_{gs1}) restricts operating frequency range of the equivalent input impedance of the proposed circuit. On the other hand, transconductance values determine SF. For decreasing input parasitic capacitance a small transistor is needed but for high transconductance a large transistor is used. While the input parasitic capacitance is decreased, the transconductance (G_{m1}) can be increased by cascading input transistors (M_1, M_2 *and*

M_5) to satisfy the stability condition of the structure [110, 111]. In this structure, G_{m1} and parasitic input capacitance can be controlled as desired without effecting each other. On the other hand, the G_{m2} is determined by M_4 ($G_{m2} = g_{m4}$) and since the proposed circuit scales the total capacitance in the gate of M_4 ($\approx \Delta c + c_{gs4}$) then its gate-source capacitance determines the minimum capacitance which can be detected with the structure. However, the size of M_4 has to be selected in such a way that it guarantees the stability of the design ($G_{m1} > G_{m2}$) [110, 112]. The stability of the circuit is insured by adjusting the size of M_4.

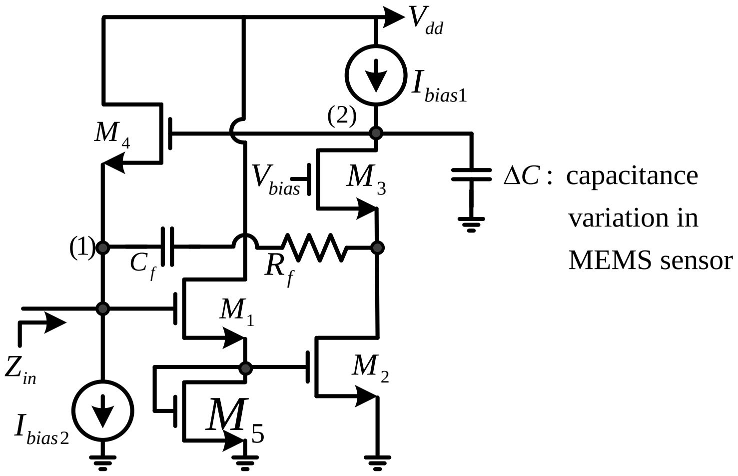


Figure 4.5 : Schematic of the proposed circuit.

Figure 4.6 demonstrates small-signal model of the proposed structure (Figure 4.5) in order to verify the input impedance characterization. In this figure, c_{gsi} and g_{mi} are gate-source capacitance and transconductance of the $i-th$ transistor, respectively. c_{gs} and g_m are in the order of some tens of fF and $m\mho$, correspondingly. Consequently, the term $c_{gs}\omega$ is very smaller than g_m in the ≤G-Hz range of frequency. As a result, in the extraction of any relation from the proposed circuit, the terms consist of $c_{gs}\omega$ can be ignored beside to those consist of g_m. In this way, input admittance of the circuit of Figure 4.6 is obtained as follow:

$$Y_{in} = \frac{1}{Z_{in}} \approx \frac{g_{m1}g_{m2}g_{m4}}{(g_{m1}+g_{m5})(c_{gs4}+\Delta c)s} + \frac{\frac{g_{m2}g_{m1}}{g_{m1}+g_{m5}}c_{gs4} + g_{m4}(\Delta c - c_f)}{c_{gs4}+\Delta c} + \left(\frac{c_{gs1}g_{m5}}{g_{m1}+g_{m5}} + \frac{c_{gs4}(\Delta c - c_f)}{c_{gs4}+\Delta c}\right)s \tag{4.6}$$

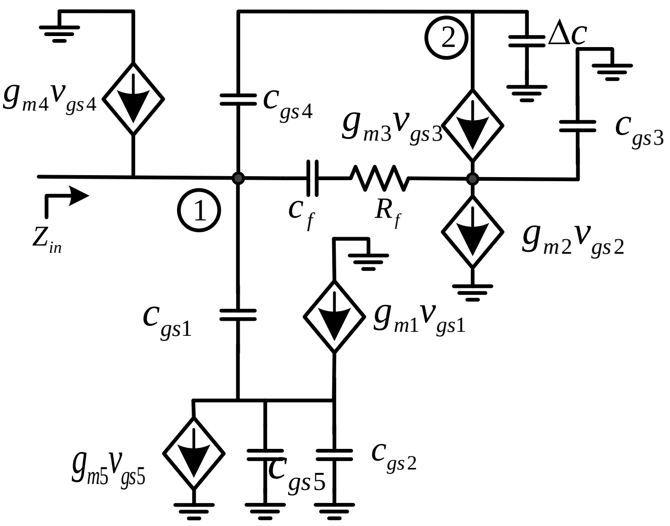


Figure 4.6 : Small-signal equivalent of proposed circuit.

The input admittance has other terms but they are very small in comparison with written terms in (4.6), thus they can be neglected. As seen from equation (4.6), by adding RC feedback, a negative term is appeared in the parasitic components (parallel resistance and capacitance). If this term is selected properly, it can cancel or decrease parasitic effects in the input impedance. Equation (4.6) shows that equivalent circuit of Figure 4.5 is a parallel RLC network and the expressions of these elements can be derived as:

$$\begin{aligned} \mathrm{L} &= \frac{(g_{m1}+g_{m5})(c_{gs4}+\Delta c)}{g_{m1}g_{m2}g_{m4}}, \\ C &= \frac{c_{gs1}g_{m5}}{g_{m1}+g_{m5}} + \frac{c_{gs4}(\Delta c - c_f)}{c_{gs4}+\Delta c}, \\ \mathrm{R} &= \frac{c_{gs4}+\Delta c}{\dfrac{g_{m2}g_{m1}}{g_{m1}+g_{m5}}c_{gs4} + g_{m4}(\Delta c - c_f)} \end{aligned} \tag{4.7}$$

If the M_1 and M_5 are supposed identical ($\Rightarrow g_{m1} = g_{m5}$) and c_f is selected close to $(\frac{g_{m2}c_{gs4}}{2g_{m4}}) + \Delta c$, then the R is cancelled ($R = 0$) and the C is decreased to some extent. As a result, the input admittance expression can be written as:

$$Y_{in} = \frac{1}{Z_{in}} \approx \frac{g_{m2}g_{m4}}{2(c_{gs4}+\Delta c)s} + \left(\frac{c_{gs1}}{2} - \frac{g_{m2}c_{gs4}^{\,2}}{2g_{m4}(c_{gs4}+\Delta c)}\right)s \approx \frac{g_{m2}g_{m4}}{2(c_{gs4}+\Delta c)s} \tag{4.8}$$

$$Z_{in} \approx \frac{2(c_{gs4}+\Delta c)s}{g_{m2}g_{m4}} = (\frac{2\Delta c}{g_{m2}g_{m4}} + \frac{2c_{gs4}}{g_{m2}g_{m4}})s \tag{4.9}$$

As it can be seen from (4.8 & 4.9) the input impedance is inductive in low frequency but it is capacitive in high frequency range (≥5 GHz). Equation (4.9) consists of two terms: the first term provides the capacitance scaling while the second term can be cancelled by a calibration step. According to equation (4.9), SF can be derived as:

$$SF \approx \frac{2}{g_{m2}g_{m4}} \tag{4.10}$$

The upper limit working of the proposed structure is determined by SRF because it increases (behaves inductively) up to SRF which can be calculated as:

$$SRF = \sqrt{\frac{1}{LC}} \Big/ 2\pi \approx \sqrt{\frac{g_{m2}g_{m4}}{c_{gs1}(c_{gs4}+\Delta c)}} \Big/ 2\pi \tag{4.11}$$

The extracted equation of proposed structure proves that the scaling factor is determined by transconductances of M_2 and M_4. After obtaining the desired SF, the SRF range can be adjusted by c_{gs1}. In this way, the circuit properties can be determined as desired separately.

4.1.2.3 Simulation results

To verify the performance of the proposed structure in capacitance scaling for micro sensors application, simulation results are carried out by HSPICE (TSMC level 49) in 180 nm CMOS technology. In the simulation, the range of ΔC variation is between $0 \; and \; 200 \; fF$. The magnitude changing of Zin versus frequency with respect to ΔC variation is depicted in Figure 4.7. It is seen from the figure that the SRF range of the circuit becomes lower when the value of ΔC increases. Thus, a smaller value of ΔC gives a higher frequency limit for linear scaling performance. As shown in Figure 4.8, for ΔC of 200fF, the magnitude changing of Zin is purely affected by the imaginary part up to 1.4GHz. Changing of Zin at 0.25, 0.5, 0.75 and 1 GHz is depicted in Figure 4.9 (schematic and post-layout simulations), which shows almost linear behaviour versus ΔC variation. It is seen from Figure 4.7, 4.8, 4.9 and Table 4.2, up to ~0.7 GHz, highly linear scaling performance (linearity≥90%) is obtained from the proposed circuit. Table 4.2 declares linearity for proposed circuit in different frequencies which is obtained based on Figure 4.9. Regarding Figure 4.9 and Table 4.2 there is trade-off between frequency and linearity. In other words, although the input-impedance magnitude is larger in high frequency but linearity is low. So according to the application proper frequency value should be determined.

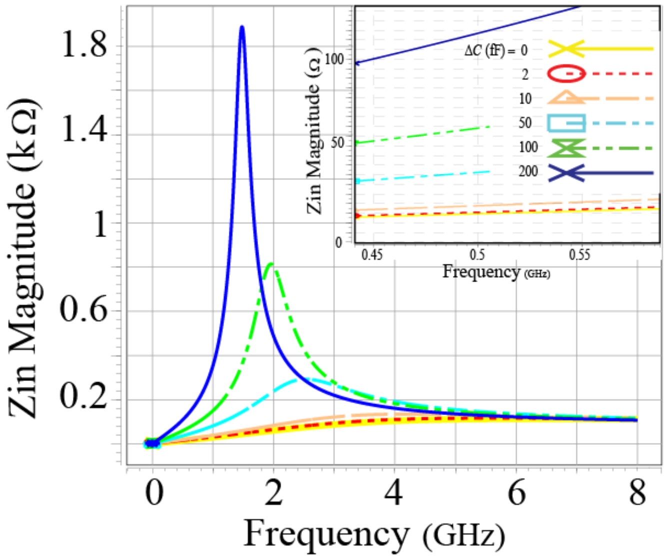


Figure 4.7 : Zin Mag. versus frequency in different capacitance variation.

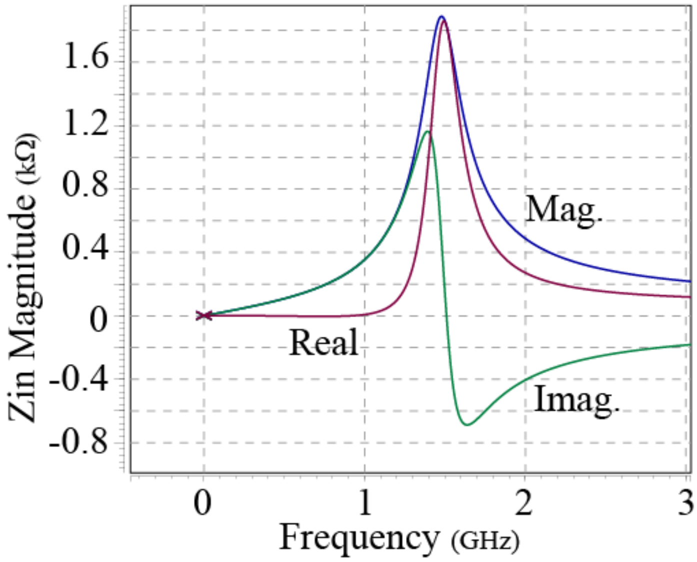


Figure 4.8 : Mag., real and Imaginary Parts of Zin when ΔC=200fF.

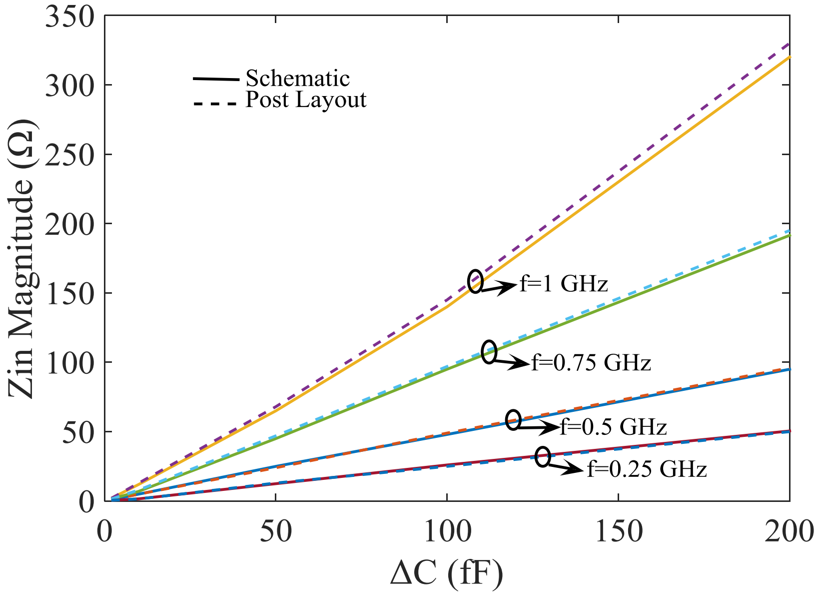


Figure 4.9 : Zin Magnitude versus capacitance changing in f=0.25, 0.5, 0.75 and 1 (GHz).

Table 4.2 : Linearity in different frequencies.

	Frequency (GHz)			
	0.25	0.5	0.75	1
Linearity (%)	97	95	86	67

To ensure the robustness of the circuit against the process variation, the Monte Carlo analysis with 100 iterations is performed by applying ±5 % Gaussian distribution at ±3σ level in the variation of transistors aspect ratio and threshold voltage. According to Figure 4.10, 75 %of the total samples occurred with the relative error of less than ±1.5 %, while in the worst case 7% of samples lead to the error of more than ±2.5 %. Figure 4.11 shows layout of the proposed design which is drown by Cadence software using single poly and one metal (M1) with the total area of 7.2×39.8 µm^2.

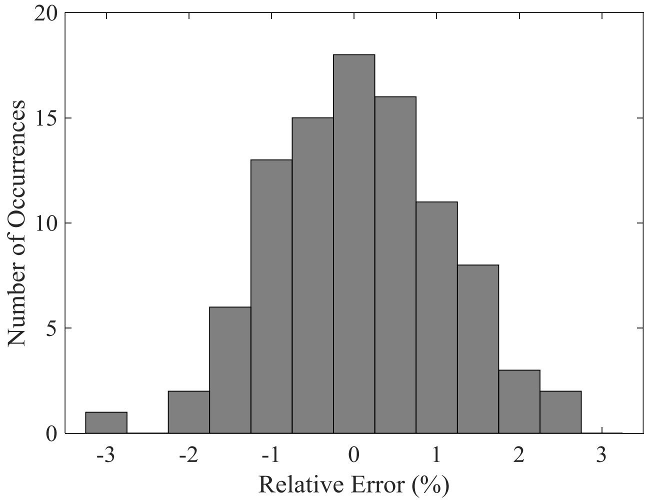


Figure 4.10 : The result of Monte Carlo analysis of GC circuit for ±5 % mismatch in transistors aspect ratio and threshold voltage when ΔC=100 fF and f=0.5 GHZ (No. of iterations = 100).

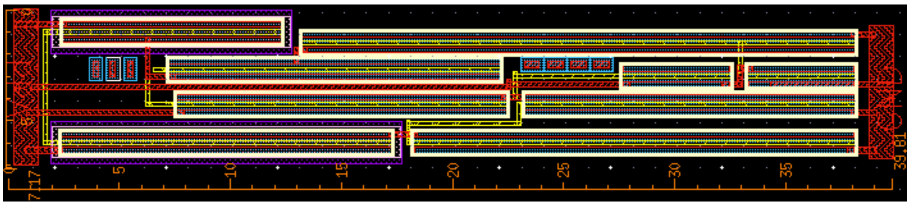


Figure 4.11 : Layout of proposed circuit.

An accurate front-end interface CMOS circuit is suggested for capacitive micro sensor applications. The proposed circuit converts small capacitance changing in sensor to sensible high magnitude impedance. In order to obtain high-performance from proposed circuit, the RC feedback and cascading structures are employed to diminish parasitic components effects. In the configuration of the circuit, SF and SRF values can be tuned separately. In order to simulate the circuit, HSPICE simulator was utilized to verify the validity of the theoretical formulations. The simulated characteristics have proved the efficiency of the circuit regarding linear scaling and tunability. Furthermore, Monte Carlo analysis of the circuit has showed robustness of the circuit performance against the process variation.

4.2 Filter Designing By Using Designed Active Inductors

Filters are widely used in analog signal processing [113, 114] to select the particular frequency. Voltage-mode and current-mode circuits such as current conveyors [115] and current feed back operational amplifiers [116] are getting much attention as compared to other active elements due to wider bandwidth, simple circuitry, low power consumptions and dynamic ranges.

In the last decade, a huge number of active building blocks were introduced for analogue signal processing. However, there is still the need to develop new active elements that offer new and better advantages. This section, focused on designing of other novel Analog Building Blocks (ABBs) such as Low-Pass Filters (LPFs) and Band-Pass Filters (BPFs) structure designs.

In RF transceivers, filters are inevitable circuit blocks. Cost and power considerations drive the field for highly integrable systems forcing filters to be implemented with minimum number of passive elements where specifically inductors cause significant problems. Typical RF filters either use off-chip passive elements or their on-chip counterparts where the inductor presents major disadvantages such as large silicon area, limited inductance value and quality factor. In most cases, the inductor is a key factor in determining the total chip area where higher inductance values imply larger area consumption. An alternative way of addressing this problem has been designing active implementations of the inductor which offer much less area consumption independent of the desired inductance value, high quality factors and tunability [117-121]. Obviously, the noise performance and dynamic range will be degraded, however they can be maintained at reasonably low levels for many applications.

Due to disadvantages of conventional inductors, active element-based inductor design is very desirable to designers today. During the last few decades, various floating inductors have been created using different high-performance active building blocks. That is why replacement of conventional inductors by synthetic ones in passive LC ladder filters belongs to well-known methods of high-order low-sensitivity filter design.

This section presents RF active filters based on designed AIs in previous chapters. The employed AIs are compact and have wide inductance band, high quality factor, low power consumption, low noise, and provide tunability. Based on these inductors, for demonstration purposes, third and six order Chebyshev filters with AMS 0.18 µm CMOS process are choosed.

4.2.1 Low-Pass Filter

AIs are used widely for designing active filters. To show versatility of using AIs in filter applications, a third order Chebyshev LPF is selected. Topology of the selected filter is illustrated in Figure 4.12. Its cutoff frequency and ripple factor are 900MHz and 0.4 dB, repectively. The normalized transfer function of the proposed filter is as:

$$T(s)=\frac{0.805}{s^3+1.34s^2+1.65s+0.805} \tag{4.12}$$

The application of impedance scaling and frequency transformation rules for 50 Ω source resistance, 250 Ω load resistance, and 900 MHz cutoff frequency, yields the filter component values as L1=60.2 nH, L2=37 nH, C=925 fF. Figure 19 compares the magnitude and phase responses of proposed filter when the pasiive inductores and their active counterparts are employed.

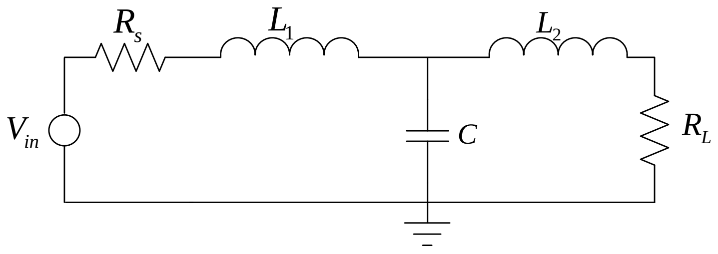


Figure 4.12 : Lowpass filter topology.

The GAI topology which is used as the core of the FAIs, is dipicted in Figure 4.13. The GAI topology is based on GC approach. The circuits analysis techniques yeild the important parameters of the GAI as follows:

$$\omega_z=\frac{G_2}{C_2},\quad \omega_p=\sqrt{\frac{G_{m1}G_{m2}+G_1G_2}{C_1C_2}},\quad \mathrm{Q}_L=\frac{\omega C_2}{G_2} \tag{4.13}$$

$$L=\frac{C_2}{G_{m1}G_{m2}},\quad \mathrm{R}_s=\frac{G_2}{G_{m1}G_{m2}} \tag{4.14}$$

where $G_{m1}=g_{m1},\ G_{m2}=\frac{g_{m2}g_{m4}}{g_{m3}}$

ω_z and ω_p are zero frequency and SRF of the proposed GAI in Figure 4.13 and Q_L the inductor QF, L the inductance value, R_s the parasitic series resistance of the inductor, G_1, G_2, C_1 and C_2 are the respective equivalent conductance and capacitances at nodes 1 and 2.

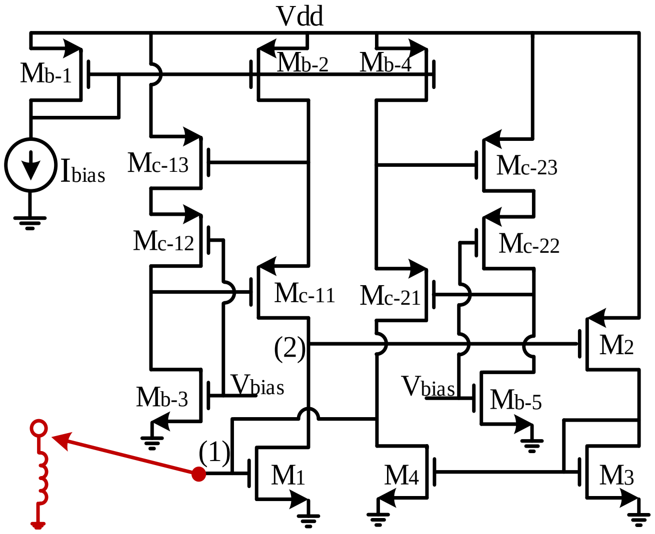


Figure 4.13 : Core GAI of FAI.

Since the RF filter shown in Figure 4.12 requires floating inductors, it remains a task to design an active circuit which would replace these components. One approach to solve this problem is to extend the GC configuration used in the previous chapters so that the circuit behaves like a floating inductor as shown in Figure 4.14. It can easily be shown that (4.13) and (4.14) maintain valid for this circuit also.

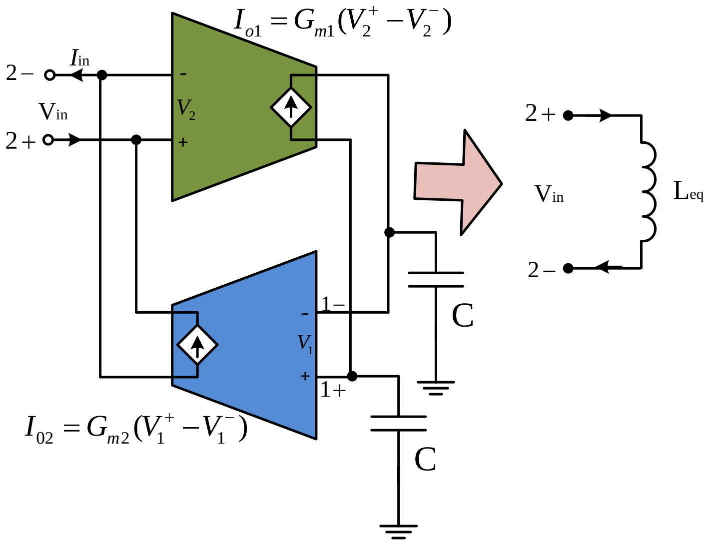


Figure 4.14 : The GC equivalent of the FAI.

The floating inductors used in the RF filter have been designed based on the active inductor circuit given in Figure 4.13. Apparently, the circuit has been replicated and re-designed so that the positive and negative transconductance stages provide the symmetry shown in Figure 4.14. Obviously, a passive filter has no biasing problem, however the active implementation of an inductor requires biasing of the active components, the MOS transistors in this case. The FAI circuit used to replace L_1 and L_2 is given in Figure 4.15.

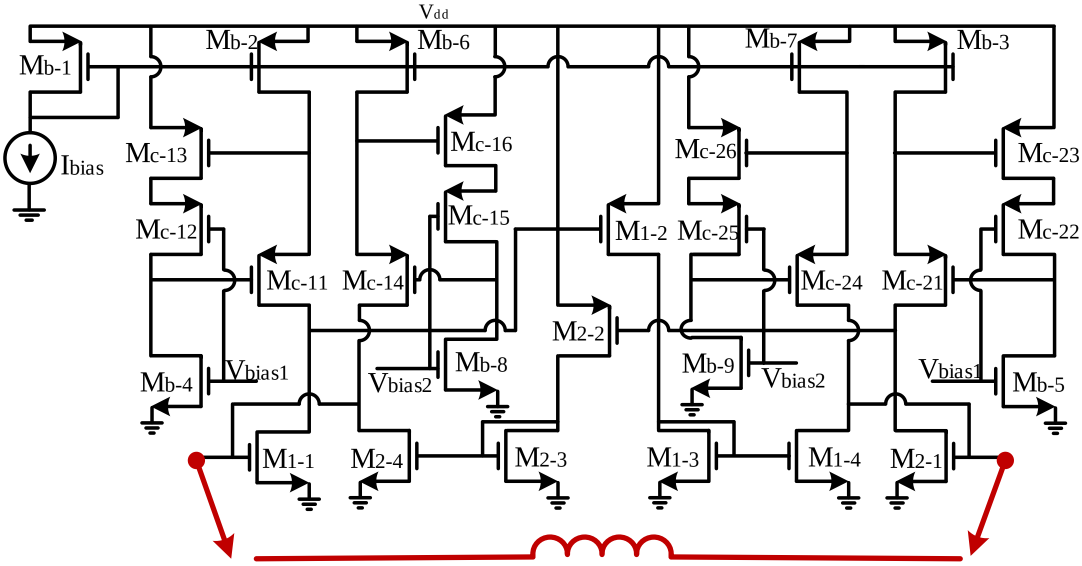


Figure 4.15 : FAI circuit used in filter designing.

Using the active inductor circuits mentioned above, the third-order Chebyshev lowpass filter shown in Figure 4.12 with 900 MHz cutoff frequency and 0.4 dB ripple has been simulated. Figure 4.16 compares the magnitude and phase responses of the filter where on-chip passive inductors (red-solid) and their active counterparts (green-dashed) have been used. The cutoff frequency of the active filter has been found almost 900 MHz, whereas the amount of ripple is 0.39 dB.

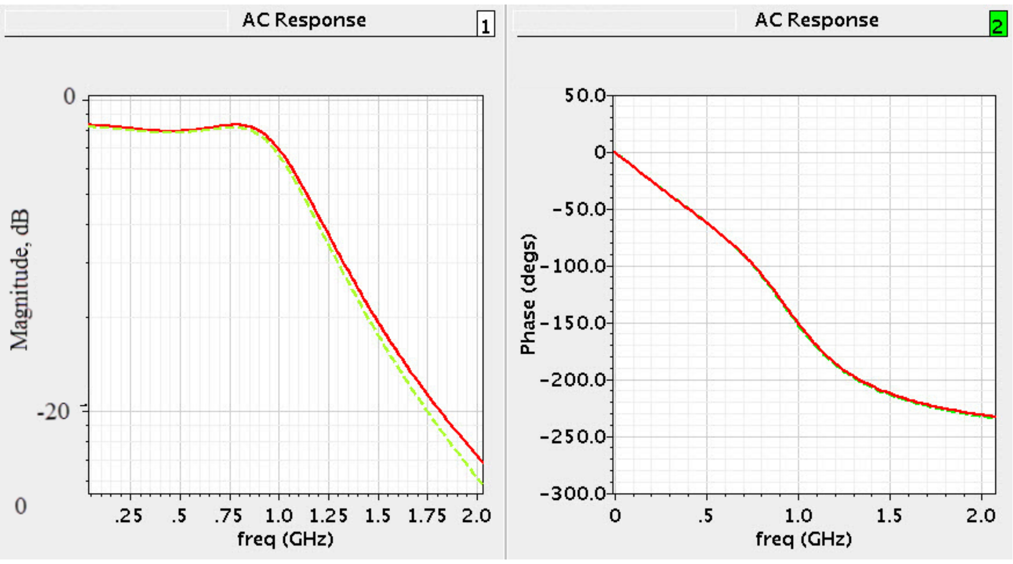


Figure 4.16 : Frequency response of LPF with passive (red-solid) and active (green-dashed) inductors.

4.2.2 Band-Pass Filter

In RF transceivers, frequency detection networks or filters are inevitable circuit blocks. Cost and power considerations drive the field for highly integrable systems forcing filters to be implemented with minimum number of passive elements where specifically inductors cause significant problems. Typical RF filters either use off-chip passive elements or their on-chip counterparts where the inductor presents major disadvantages such as large silicon area, limited inductance value and quality factor. It is very easy to create an impedance match using passive elements which consist of lumped and distributed [122-124]. On the other hand, in many applications, there is a demand to construct lossless two-ports for various kinds of problems such as filters, power transfer networks or equalizers. But passive elements, especially inductors, have large resistive loss which degrade there quality factor which can be decreased by replacing them with active counterparts [125].

The analytic theory for RF application is used for simple problems [126-128], but it is not accessible for practical ones. Therefor it is essential to use Computer Aided Design (CAD) approach to design immittance equalizers with lumped, distributed or mixed elements [123]. Commercial CAD tools are used for optimization of frequency detection network performance, then characteristic impedance of the lumped elements are calculated according to process parameters and specifications. Unfortunately, performance optimization is highly nonlinear with respect to characteristic impedances and needs proper initial values [129]. On the other hand selection of initial values is very important in order to have convergence optimization.

The Simplified Real Frequency Technique (SRFT) is used to design filter. In [130], a similar technique called Modeling-based Real Frequency Technique (M-RFT) was proposed, while in this technique, circuit model of the load should be formed from the given numerical load data. But in SRFT, it is not necessary to obtain the model of the load. So the proposed method is simpler than M-RFT and gives the same performance as well.

4.2.2.1 Mathematical Framework

Filter designing can be considered as lossless two port block between a generator and complex load. It is expected that the block transfers maximum power from the source to the load over operation frequency band. The power transfer capability of the lossless equalizer is precisely measured by means of the Transducer Power Gain (TPG) which can be defined as the ratio of power transferred to the load to the available power which is generated by source. By considering two port network in Figure 4.17, TPG can be calculated in terms of the normalized real and imaginary parts of load impedance ($Z_L=R_L+jX_L$) and the back end impedance ($Z_2=R_2+jX_2$) or generator impedance ($Z_G= R_G+jX_G$) and the front end impedance ($Z_1=R_1+jX_1$) as follow:

$$TPG(\omega)=\frac{P_L}{P_A}=\frac{4R_2R_L}{\left(R_2+R_L\right)^2+\left(X_2+X_L\right)^2}=\frac{4R_1R_G}{\left(R_1+R_G\right)^2+\left(X_1+X_G\right)^2} \tag{4.15}$$

where P_L and P_A are power delivered to the load and available power from the generator, respectively.

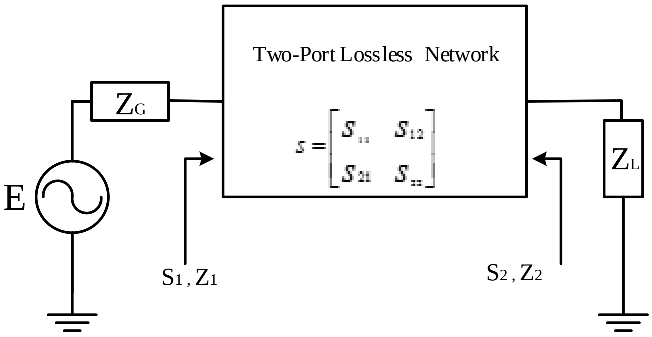


Figure 4.17 : Two port network.

To design lossless two port network, the TPG should be maximized inside desired frequency band with. Thus, the Z_1 and Z_2 (Figure 4.17) must be determined very carefully. When they are determined properly, the network can be easily synthesized.

There are many approaches to modeling the aforementioned networks. Carlin used Real Frequency Line segment Technique (RF-LST) to realize Z_2 [131, 132]. In this approach, Z_2 is realized as a minimum reactance function and its real part $R_2(\omega)$ is represented by line segments in such a way that $R_2(\omega)=\sum_{k=1}^{m} a_k(\omega)R_k$, passing through m selected pairs designated by $\{R_k, \omega_k; k=1,\dots,m\}$. In this formalism, the break points (or break resistances) R_k are considered to be the unknowns of the network problem. Then, these points are calculated via the nonlinear optimization of TPG. The Imaginary part $X_2(\omega)=\sum_{k=1}^{m} b_k(\omega)R_k$ of Z_2 is also written by means of the same break points R_k. It must be noted that coefficients $a_k(\omega)$ are known quantities and calculated in terms of the preselected break frequencies ω_k. The coefficients $b_k(\omega)$ are generated by means of the Hilbert transformation relation given for minimum reactance functions. Let $H\{0\}$ represent the Hilbert transformation operator. Then, $b_k(\omega) = H\{a_k(\omega)\}$. The disadvantages of RF-LST are the two independent approximation steps. Although this approach guarantees the realization of impedance but increases complexity of computational steps and nonlinearity of the TPG with respect to the optimization parameters.

Another approach is Direct Computational technique (DCT) which is similar to RF-LST [133]. Here, the real part of the unknown matching network impedance R_2 is expressed as a real even rational function. Then, the unknown coefficients of this function are chosen to optimize the gain performance.

In another method proposed by Fettweis, the parametric representation of the positive real back-end driving point impedance Z_2 is utilized [134]. More specifically, the positive real impedance Z_2 is written in a partial fraction expansion, and then, the poles of Z_2 are determined by optimizing the gain performance of the system in the interested frequency band. The parametric approach can be used for solving single matching problems. The difficulty is to initialize the locations of the poles, which are critical.

In aforementioned methods, the lossless network is designed in terms of free parameters by means of driving point impedance Z_2. In the real frequency scattering approach, which is referred to as the SRFT, the canonic polynomial representation of the scattering matrix is used to describe the lossless network [135-140].

In all discussed approaches the aim is to express Z2 of the network and then synthesizing it to extract network's elements values. After, the TPG is optimized by (1). Also the front-end and back-end impedances (Z1 and Z2) can be determined by using three parameters; the scattering parameters of the network, source reflection coefficient and load reflection coefficient. In the next section, the canonic polynomial representation of the scattering parameters is calculated.

4.2.2.2 Extracting the characterization of two port network

According to Figure 4.17, scattering parameters of passive two-port network can be figured out from energy point of view as:

$$S(p) = \begin{bmatrix} S_{11}(p) = \dfrac{h(p)}{g(p)} & S_{12}(p) = \dfrac{\mu f(-p)}{g(p)} \\ S_{21}(p) = \dfrac{f(p)}{g(p)} & S_{22}(p) = -\dfrac{\mu h(-p)}{g(p)} \end{bmatrix} \tag{4.16}$$

Where $p = \sigma + j\omega$ is the classical complex frequency variable, g is a strictly Hurwitz polynomial, f is a real monic polynomial, and μ is a unimodular constant ($\mu = \pm 1$). If the two-port network is reciprocal, then the polynomial f is either even or odd and $\mu = f(-p)/f(p)$. The polynomials $\{f, g, h\}$ are related by the Feldtkeller equation [135].

$$g(p)g(-p) = h(p)h(-p) + f(p)f(-p) \tag{4.17}$$

Therefore, if the $f(p)$ and $h(p)$ are specified by designer, then the whole scattering parameters and the network itself can be defined completely. In all applications, designers have an idea about the zero locations of their network. Hence, the $f(p)$ which is constructed on the transmission zeroes is defined by the designers. So, the following form can be used for $f(p)$:

$$f(p) = p^{m_1} \prod_{i=0}^{m_2} (p^2 + a_i^2) \tag{4.18}$$

Where m_1 and m_2 are nonnegative integers and a_i's are arbitrary real coefficients. This form corresponds to ladder-type minimum phase structures, whose transmission zeroes are on the imaginary axis of the complex p-plane.

The input reflection coefficient (S_1) of the network when its output port is terminated in Z_L can be written in terms of the scattering parameters of the matching network as:

$$S_1 = S_{11} + \frac{S_{12} S_{21} S_L}{1 - S_{22} S_L} \tag{4.19}$$

where S_L is the load reflection coefficient expressed as:

$$S_L = \frac{Z_L - 1}{Z_L + 1} \tag{4.20}$$

Consequently, the output reflection coefficient (S2) of the network when its input port is terminated in Z_G can be written in terms of the scattering parameters of the network as:

$$S_2 = S_{22} + \frac{S_{12} S_{21} S_G}{1 - S_{11} S_G} \tag{4.21}$$

Where S_G is the source reflection coefficient and expressed as:

$$S_G = \frac{Z_G - 1}{Z_G + 1} \tag{4.22}$$

Then the front-end and back-end driving point impedances of the network can be calculated by the following equations, respectively:

$$Z_1 = \frac{1 + S_1}{1 - S_1} \tag{4.23}$$

$$Z_2 = \frac{1 + S_2}{1 - S_2} \tag{4.24}$$

Finally, obtained Z_1 or Z_2 function is synthesized by Darlington theory and yields the desired equalizer topology with initial element values. Eventually, performance of the matched system is optimized using the CAD tools. If an equation is written for the load impedance in terms of the network parameters (impedance or admittance) and the input impedance of the network, then this equation can be used in the process design. It can be seen that the proposed method is very simple, and there is no need to obtain a proper model of the given load data. By using the proposed technique, networks with lumped elements can be designed.

4.2.2.3 Computational Steps

Firstly, the inputs and outputs of algorithm should be defined.

Inputs:

- Z_L and Z_G: Load and source impedances
- w_i:sampling frequencies, $w_i = 2\pi f$, and operation frequencies
- R_n, f_n: normalization factors
- n: number of UEs in equalizer
- $h_0, h_1, \dots, h_n$: Initial real coefficients of $h(\mathrm{p})$ polynomial. (n is the degree of the polynomial which is equal to the number of lumped elements in power transfer network)
- $f(\mathrm{p})$: A polynomial structured on transmission zeros of frequency detection network (its practical form is in (4.18))
- δ_c: the stopping criteria of the sum of the square errors

Outputs:

- Analytic form of the input reflection coefficient of the lossless frequency detection network, $S_{11}(p) = \frac{h(\mathrm{p})}{g(\mathrm{p})}$. It is noted that this algorithm determines the coefficients of the polynomials $h(\mathrm{p})$ and $g(\mathrm{p})$, which in turn optimizes the gain performance of the system.
- TPG of network: $|S_{21}|^2$ (forward reflection coefficient) denotes the transducer power gain of the network.
- Lumped elements values and topology of network: This step is resulted from S_{11} synthesis.

In order to construct the gain function of Chebyshev type the algorithm steps can be expressed as follows:

- Step 1: Normalization of frequencies and impedances with respect to f_n, R_n
- Step 2: Generation of the strictly Hurwitz polynomial $g(\mathrm{p})$ (from (4.17)) and scattering parameters (from (4.16)).
- Step 3: calculation of the source and load reflection coefficients S_G and S_L (from (4.22 and 4.20))
- Step 4: calculation of the Z_1 and Z_2 (from (4.23 and 4.24))
- Step 5: obtaining TPG (from (4.15))
- Step 6: calculation of error via $\epsilon(\omega) = 1 - TPG(\omega)$; then $\delta = \sum|\epsilon(\omega)|^2$
- Step 7: if δ is acceptable ($\delta \leq \delta_c$), then synthesize $S_{11}(p)$. Otherwise, change the initialized coefficients of the polynomial h(p) and starting from step 2.

4.2.2.4 Designing 6-order BPF

In this section, explained algorithm is employed for designing of a 6-order filter. The pass band of the BPF is 1 GHz between 1.5-2.5 GHz and its ripple factor is 0.6. The Z_L and Z_G are 50Ω. The structural scattering parameters structural polynomials are as:

$$\begin{aligned} h(p) &= 4.36p^6 + 0.00534p^5 + 13.94p^4 - 0.000734p^3 + 13.94p^2 - 0.007p + 4.36 \\ f(p) &= p^3 \\ g(p) &= 4.36p^6 + 4.4p^5 + 16.16p^4 + 9.8p^3 + 16.16p^2 + 4.4p + 4.36 \end{aligned} \tag{4.25}$$

After synthesizing the obtained scattering parameter or the corresponding impedance function, the BPF seen in Figure 4.18 is obtained. Figures 4.19 and 4.20 show the TPG performance of the designed BPF, which are simulated by MATLAB and Cadence respectively. In Figure 4.20, passive inductors are replaced with their active counterparts and the result is looked almost similar.

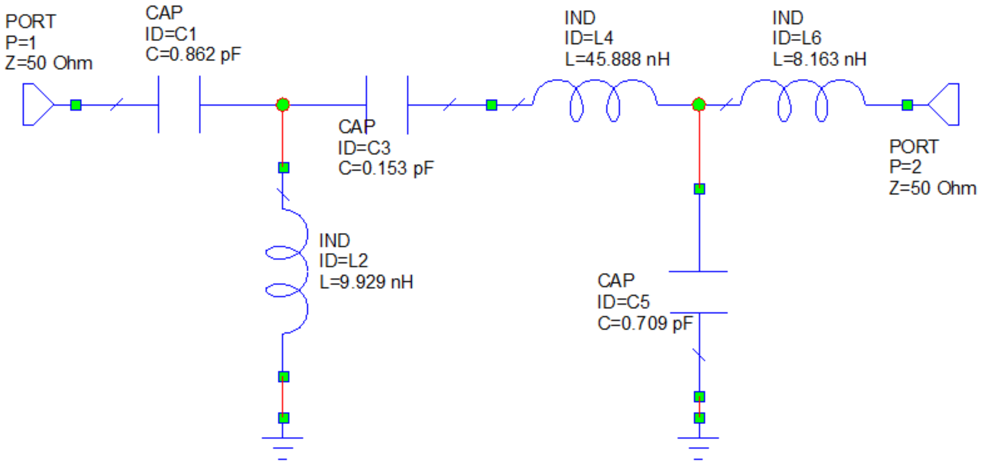


Figure 4.18 : Designed lumped element BPF.

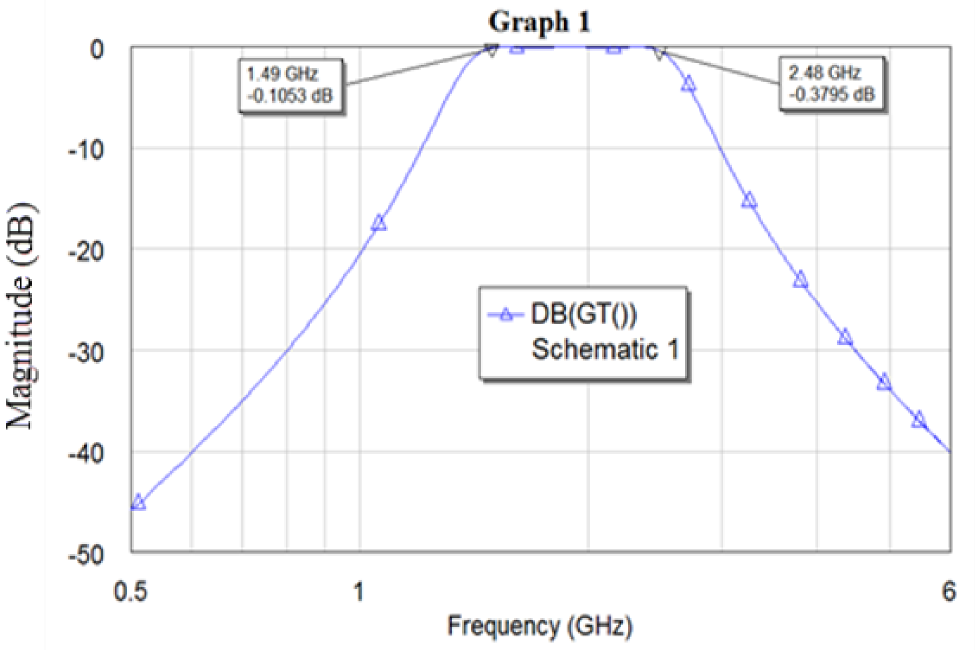


Figure 4.19 : TPG performance of designed BPF.

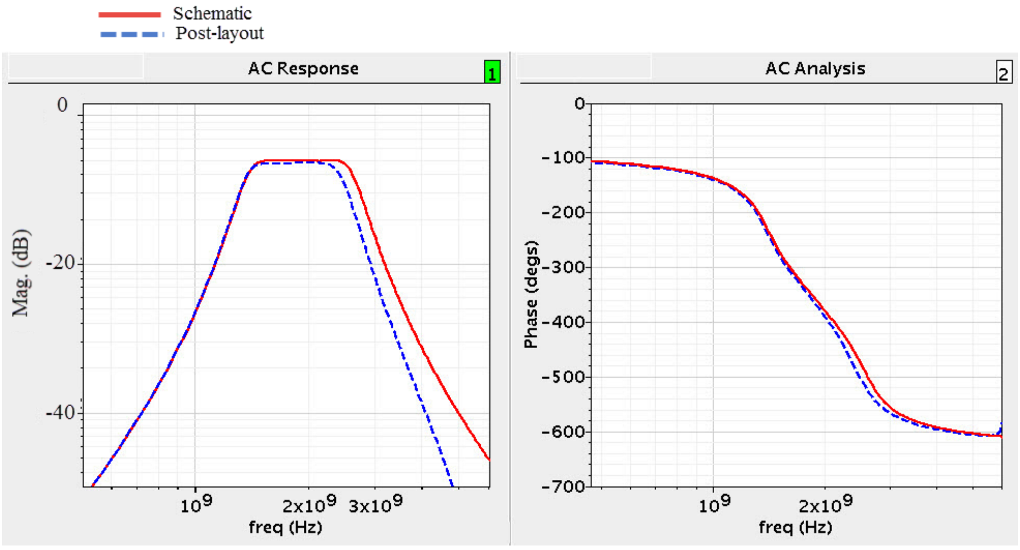
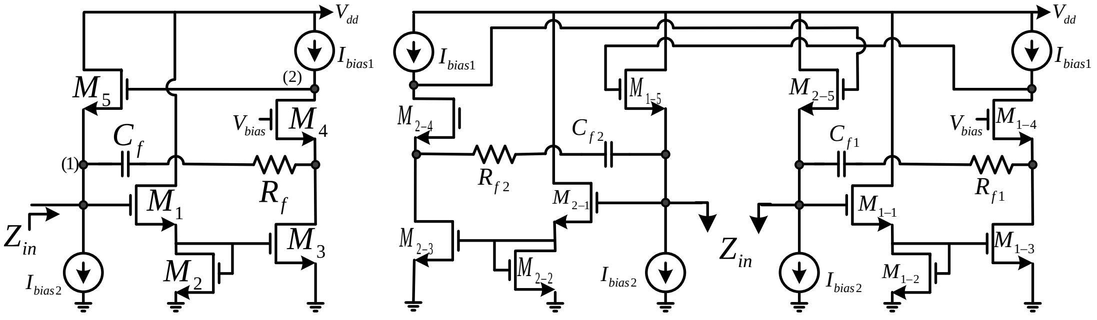


Figure 4.20 : AC response proposed BPF with passive (red-solid) and active (blue-dashed) inductors - Magnitude and Phase.

The grounded and floating active inductors, which are replaced with their passive counterparts in BPF are shown in Figure 4.21. Detailed explanation of the employed AI was in previous section.



(a) Grounded (b) Floating

Figure 4.21 : Utilized grounded and floating AIs in 6-order BPF, a) Grounded, b) Floating.

4.3 Chapter Summery

This chapter focused on GC network applications. Firstly, it is used as an accurate interface circuit for detecting capacitance variation in MEMS sensor. Then, in order to show workability of designed GC based AIs in Chapter 3, they are employed in LPF and BPF circuits. The simulation results prove their performance in filter implementation.

5. CONCLUSION

5.1 Summary of the Work

CMOS technology has turned to dominant technology for implementing electronic circuits, nowadays. The structures which are designed with CMOS technology are very compact and low cost and low power. On the other hand, spiral CMOS inductors, which are the major components of RFICs, cannot provide high and tunable inductance, high QF and occupy large silicone area. Therefore, AIs have become a good alternative for them. They are used widely in many applications such as LNAs, power-dividers, phase-shifters and matching networks.

There are many approaches in implementation of AIs in CMOS technology. Among them current conveyers and GC networks are very popular for designing AIs in low and high frequency applications, respectively. The popularity of GC approach arises from its ability to adjust gyrator’s transconductance and load capacitance easily by bias currents and MOS varactors. So, this approach is used in this thesis to implement new and high performance AI circuits.

The main concerns about AIs are their loss and noise. At the our first AI circuits, the MRC stages were used to reduce the loss of the proposed circuit. As a result QF of the designed AI was maximized. Constructing the MRC stages with PMOS transistors made the input transistor as small as possible. Consequently, the SRF of the structure was increased due to reduced input parasitic capacitance. Furthermore, the number of active elements were reduced in main path of the ac signal, which makes the circuit suitable for RF applications. However, these stages did not cause to noise performance degrading.

There is a tradeoff between the QF and SRF of the AIs. A large input transistor is needed for high-Q and high inductance value AI but a small input transistor is required for high SRF AI. This idea became the main motivation to design the second AI with ability to adjust its characterization independently. As it discussed before, input transistor is very important regarding to AI characterizations. Cascoding input transistor gives the ability to adjust the first gyrator’s transconductance and input parasitic capacitance independently. Furthermore, the inductance value can be adjusted by other transistor’s transconductance. The RC feedback is utilized to cancel the parasitic series-resistance of AI, which results in QF enhancement. Since, bias condition of cascoding transistors is provided by a diode-connected transistor, the proposed structure is robust in terms of performance over variation in process, voltage and temperature. Reviewing the literatures proves that it is first time the properties of AI can be independently adjusted without affecting each other.

The Noise of designed AIs has limited the use of them in RF applications such as LNAs. The main noise source of an AI is its input transistor. In order to have low noise AI, the input transistor should be designed large enough. But it leads to low SRF which limits the inductive frequency band. A new low-noise and low-loss AI was presented as third AI circuit, which is suitable for RF low noise applications. Utilizing all transistors in CS configuration on the AI circuit leads to low conductance nodes which causes to high-Q AI. P-type MOS transistors and Feed-Forward Path (FFP) are employed to decrease noise of the AI, respectively.

As a fourth AI circuit, floating version of low-loss GAI was designed in symmetric configuration. Similar to the grounded type its properties can be tuned very easily by changing its gyrators’ transconductance and load capacitance value. Four MRC stages were employed to reduce its input/output nodes conductance. Table 5.1 compares pros and cons of all designed AIs in this thesis. Table 5.2 compares the designed AI circuits with reported ones in the literature.

Table 5.1 : Comparison pros and cons of designed AIs.

Proposed AI	Approach	Employed techniques	Salient feature	Disadvantage
3.2 Low-loss	GC	MRC stage in input MRC stage in output	Low-loss High SRF (result of MRC stage location)	Input voltage swing
3.3 Adjustable	GC	RC feedback Input transistor Cascoding	Adjusting the properties of AI independently Decreasing the parasitic components	Noise
3.4 Low-noise	GC	P-MOS Differential pair transistors FFP	Low noise High-Q	Low-SRF
3.5 Floating	GC	MRC stages in input/output nodes Symmetric configuration	Symmetric configuration	Low-IBW Large area

Based on Table 5.1, for each application a suitable designed AI can be selected. For instance for LNA, low noise one is appropriate than the others. Among all newly designed GAI, the adjustable properties are the best in term of AI characterization. Because its parasitic components are diminished as much as possible and its properties can be adjusted separately from each other regarding employed techniques.

Table 5.2 : Comparison of designed AIs with reported AIs.

Section or Ref. No.	Tech. (μm/V)	L (nH)	IBW (GHz)	SRF	Q_{max}	P_{diss} (mW)	Area (μm^2)	Robustness (relative	Noise $pA/\sqrt{Hz}$
3.2	0.18/1.8	13	0.3-11.2	11.2	1k	1	534.6	74	n.a.
3.3	0.18/1.8	216	0.3-11.3	11.3	2.1k	1	286.56	72	n.a.
[64]	0.18/1.8	33	n.a.		33	3.6	n.a.	n.a.	n.a.
[68]	0.13/1.6	14.5	0.5-10.2	10.2	3k	13.6	3750	n.a.	n.a.
[41]	0.13/1.2	144	0.3-7.32	7.32	3.9k	1	n.a.	n.a.	35
Low-Noise AIs									
3.4	0.18/1.8	35	0.6-9.2	9.2	1.25k	1.3	475.44	68	15
[42]	0.09/1.2	165	0.6-3.8	3.8	120	1.2	n.a.	n.a.	12
[45]	0.18/1.8	43	0.645-6.3	6.3	1k	0.65	n.a.	n.a.	54
[141]	0.09/1	26	1.7-5.5	5.5	895	0.515	605	n.a.	36
Floating AIs									
3.5	0.18/1.8	284	0.1-6.2	6.2	567	2	934.4	69	n.a.
[57]	0.13/1.2	1.9	3.5	3.5	38.8	6.4	2600	n.a.	n.a.
[55]	0.18/1.8	33	4	4	68	3.6	810	n.a.	n.a.
[79]	0.35/3.3	12400	0.25-0.75	0.75	n.a.	2	170×10^3	n.a.	n.a.

Table 5.2 can be devided to three groups as: 1) GAIs (white), 2) low-noise GAI (gray), 3) Floating AI (darker gray). Among all presented GAIs in Table 5.2, our designed AI which is described in detail in section 3.3, has high performance in term of AI charactrization. Futhermore, its properties such as SRF, QF and inductance value can be adjusted independently. It has largest SRF and lowest area consumption.

Among second group's GAIs, which are suitable for low noise application, our designed has best SRFand QF and its noise performance is the best among the circuits which use 0.18 µm technology. In other words, it can utilized in wider frequency bandwidth applications. Above mentioned advantages are also valid for our designed FAI according to the third group of FAIs in Table 5.2. Although the number of transistores are increased, its power consumption is the one of the lowest. Its simmetric configuration leads to low area consumtion compared to the other FAIs.

Two applications are presented in the thesis to show the usability of our new AIs. One of them is the capacitive micro sensors which convert mechanical signals to small capacitance variation. The capacitance variation in micro sensor is in the range of femto-Farads which makes it difficult to sense. On the other hand, the Gyrator-C topologies can convert a low capacitance variation to high impedance change which makes it a good choice as interface circuits for capacitive sensors. In this thesis, a new 3-axis accelerometer with ability to cancel cross section sensitivity was designed. It is first time in the litrerature that an accelerometer can measure all axis accelerations by using one proof mass. The sensor's electrodes were located in such a way that enables the structure to detect acceleration in all axis independently. This is another new contribution in designing sensors. Consequently, a new and accurate GC configuration for sensing very small capacitance changes in a capacitive sensor was presented. In the proposed configuration, the operating frequency range and SF can be adjusted without affecting each other by tuning the bias currents. In addition, the proposed configuration employs RC feedback and cascoding techniques to cancel the effect of the parasitic components.

Finally, in order to show versatility of designed AIs, they are used in designed third and sixth order broadband microwave filters. The first one is a third order Chebyshev low pass filter. The second one, which is designed by using simplified real frequency technique is a sixth order Chebyshev band pass filter. The simulated frequency response of filters prove the workability of the designed AIs.

5.2 Scope of Future Works

Some points are suggested as future works, which can be probably improve the performance of the designed circuits implementation and applications of AIs.

- Design AI with high linearity
- Design AI with high dynamic range
- Other topologies to design AI suitable for RF applications
- GC network as a frequency dependent negative impedance

$$NI = \frac{\prod G_{mi}}{\prod G_{mj}} s^2 C_{L1} C_{L2} = -\frac{\prod G_{mi}}{\prod G_{mj}} \omega^2 C_{L1} C_{L2}$$

- Design of floating version of designed GAIs
- Design AI with mutual inductance characterization
- Using designed AIs in implementation of:
    - transformers
    - LNAs
    - All kinds of filters
    - Power dividers
    - Matching networks
    - Phase shifters
    - VCOs
    - Trans-impedance amplifiers

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REFERENCES

[1] **Shoghi, P., Barnwell, C.J., and Weldon, T. P.** (2008). Experimental results for an inductively matched microwave amplifier in a standard 0.5 micron CMOS process using four identical spiral inductors. *Southeastcon, 2008. IEEE,* Huntsville, AL. pp. 64-68

[2] **Lee, D. H., Han, J., Park C., and Hong, S.,** (2007). A CMOS Active Balun Using Bond Wire Inductors and a Gain Boosting Technique. *IEEE Microwave and Wireless Components Letters, vol. 17,* no. 9, pp. 676-678, Sept. 2007.

[3] **Analui, B., and Hajimiri, A.** (2004). Bandwidth enhancement for transimpedance amplifiers. *IEEE Journal of Solid-State Circuits, vol. 39,* no. 8, pp. 1263-1270.

[4] **Tang, A., Yuan, F., and Law, E.,** (2007). A New CMOS BPSK Modulator with Optimal Transaction Bandwidth Control. *Circuits and Systems, ISCAS 2007. IEEE International Symposium on,* New Orleans, LA, 2007, pp. 2550-2553.

[5] **Tang, A., Yuan, F., and Law, E.,** (2008). A New CMOS Active Transformer QPSK Modulator with Optimal Bandwidth Control. *IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 55,* no. 1, pp. 11-15.

[6] **Wu, Y.C., and Chang, M.F.** (2002). On-chip RF spiral inductors and bandpass filters using active magnetic energy recovery. *Custom Integrated Circuits Conference, 2002. Proceedings of the IEEE*, pp. 275-278.

[7] **Lu, L.H., and Liao, Y.T.** (2005). A 4-GHz phase shifter MMIC in 0.18-µm CMOS. *IEEE Microwave and Wireless Components Letters, vol. 15,* no. 10, pp. 694-696.

[8] **Wang, S.** (2011). Design of CMOS Wilkinson Power Divider Incorporating Semi-passive Inductors. *Future Intelligent Information Systems,* Volume 86 of the series Lecture Notes in Electrical Engineering pp 231-238, Springer.

[9] **Veenstra, H., and Long, J. R.** (2008). *Circuit and Interconnect Design for RF and High Bit-Rate Applications*. Analog Circuits and Signal Processing Series, Springer.

[10] **Burghartz, J., Edelstein, D., Soytter M., Ainspan H. and Jenkins K.,** (1998). RF circuit design aspects of spiral inductors on silicon. *Solid-State Circuits Conference, Digest of Technical Papers. IEEE International,* San Francisco, CA, USA, 1998, pp. 246-247.

[11] **Burghartz, J. N., and Rejaei, B.** (2003). On the design of RF spiral inductors on silicon. *IEEE Transactions on Electron Devices, vol. 50,* pp. 718-729.

[12] **Chiang, M. j., Wu, H.S., and Tzuang, C.K.C.** (2006). Design of CMOS Spiral Inductors for Effective Broadband Shielding. *Microwave Conference, 36th European,* Manchester, pp. 48-51.

[13] **Uddin, M.J., Nordin, A.N., Ibrahimy M.I., Reaz, M.B.I., Zulkifli, T.Z.A., and Hasan, M.A.** (2009). Design and Simulation of RF-CMOS Spiral Inductors for ISM Band RFID Reader Circuits. *Microelectronics and Electron Devices, WMED 2009. IEEE Workshop on, Boise, ID,* 2009, pp. 1-4.

[14] **Belini, V.L., and Romero, M.A.** (2002). Design of active inductors using CMOS technology. *Integrated Circuits and Systems Design, Proceedings. 15th Symposium on 2002,* pp. 296-301.

[15] **Thanachayanont A.** (2002). CMOS transistor-only active inductor for IF/RF applications. *Industrial Technology, IEEE ICIT '02. 2002 IEEE International Conference on,* 2002, pp. 1209-1212 vol.2.

[16] **Voinigescu S.**, (2013). *High-Frequency Integrated Circuits*. Cambridge University Press

[17] **Mohan, S.S., Hershenson, M.D.M., Boyd, S.P., and Lee, T.H.** (2000). Bandwidth extension in CMOS with optimized on-chip inductors. *IEEE Journal of Solid-State Circuits, vol. 35,* no. 3, pp. 346-355.

[18] **Sun, B., and Yuan, F.** (2003). A new inductor series-peaking technique for bandwidth enhancement of CMOS current-mode circuits. *Analog Integrated Circuits and Signal Processing,* 37(3):259–264.

[19] **Razavi, B.** (1998). *RF microelectronics*. Prentice-Hall, Upper Saddle River, N.J.

[20] **Soorapanth, T., and Wong, S.S.** (2002). A 0-dB IL 2140±30 MHz bandpass filter utilizing Q-enhanced spiral inductors in standard CMOS. *IEEE Journal of Solid-State Circuits, vol. 37,* no. 5, pp. 579-586.

[21] **Praveen, M.C., Venkatesan, V.V., Raja, J., and Srinivasan, R.** (2012). Active inductor based differential Low Noise Amplifier for ultra wide band applications. *Recent Trends In Information Technology (ICRTIT), 2012 International Conference on,* Chennai, Tamil Nadu, pp. 401-406.

[22] **Colucci, P., Leuzzi, G., Pantoli, L., and Stornelli, V.** (2012). Third order integrable UHF bandpass filter using active inductors. *Microwave and Optical Technology Letters, Volume 54,* Issue 6, pages 1426–1429.

[23] **Leuzzi, G., Stornelli, V., and Del Re, S.,** (2011). A Tuneable Active Inductor with High Dynamic Range for Band-Pass Filter Applications. *IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 58,* no. 10, pp. 647-651.

[24] **Huang, Z.Y., and Huang, C.C.** (2007). Multi-Stage Low-Noise Amplifier with LC-Tank Load for Ultra-Wideband Wireless Receiver. *Electron Devices and Solid-State Circuits, (EDSSC) 2007. IEEE Conference on,* Tainan, 2007, pp. 993-996.

[25] **Sturm, J., Groinig, M., and Xiang, X.** (2014). Tunable Balun Low-Noise Amplifier in 65 nm CMOS Technology. *Radioengineering Journal, Vol. 23,* NO. 1.

[26] **Lu, L.H., Liao, Y.T., and Wu, C.** (2005). A miniaturized Wilkinson power divider with CMOS active inductors. *IEEE Microwave and Wireless Components Letters, vol. 15,* no. 11, pp. 775-777.

[27] **Wang, S.** (2011). Design of CMOS Wilkinson Power Divider Incorporating Semi-passive Inductors. *Future Intelligent Information Systems.* Springer.

[28] **Zito, D., Pepe, D., and Fonte, A.,** (2012). 13 GHz CMOS Active Inductor LC VCO. *IEEE Microwave and Wireless Components Letters, vol. 22,* no. 3, pp. 138-140, March.

[29] **Kao, H.L., Lee, P.C., and Chiu, H.C.** (2015). A Wide Tuning-Range CMOS VCO with a Tunable Active Inductor. *Mathematical Problems in Engineering, Hidawi Journal, Volume 2015,* Article ID 382483, 7 pages

[30] **Xu, J., Saavedra, C. E., and Chen, G.** (2011). An Active Inductor-Based VCO with Wide Tuning Range and High DC-to-RF Power Efficiency. *IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 58,* no. 8, pp. 462-466.

[31] **Gao, M., Wang, Y., Wang, Y. and Guo D.** (2009). Design of wideband CMOS LNA with active inductor and using noise-canceling technique. *2009 3rd International Conference on Anti-counterfeiting, Security, and Identification in Communication,* Hong Kong, pp. 262-265.

[32] **Saberkaria, A., Ziabakhsha, S., Martinezb, H., and Alarcónb, E.** (2016). Active inductor-based tunable impedance matching network for RF power amplifier application. *Integration, the VLSI Journal, Volume 52,* Pages 301–308

[33] **Saberkaria, A., Kazemia, S., Shirmohammadlia, V., and Yagoub,b M.C.E.** (2016). gm-boosted flat gain UWB low noise amplifier with active inductor-based input matching network. *Integration, the VLSI Journal, Volume 52,* Pages 323–333

[34] **Kia, H.B., A'ain, A.K., Grout, I., and Kamisian, I.** (2013). A Reconfigurable Low-Noise Amplifier Using a Tunable Active Inductor for Multistandard Receivers. *Circuits, Systems, and Signal Processing, Volume 32,* Issue 3, pp 979-992

[35] **Ren, S., Benedik, C.** (2013). RF CMOS active inductor band pass filter with post fabrication calibration. *AEU - International Journal of Electronics and Communications, Volume 67,* Issue 12, Pages 1058–1067

[36] **Pantoli, L., Stornelli, V., and Leuzzi, G.** (2015). Class AB tunable active inductor. *Electronics Letters, vol. 51,* no. 1, pp. 65-67.

[37] **Taparia, A., Banerjee, B., and Viswanathan, T. R.** (2011). Power-Supply Noise Reduction Using Active Inductors in Mixed-Signal Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19,* no. 11, pp. 1960-1968.

[38] **Hammadi, A.B., Mhiri, M., Haddad, F., Saad, S., and Besbes K.** (2015). Design of wide-tuning high-Q differential active inductor for multistandard applications. *Systems, Signals & Devices (SSD), 2015 12th International Multi-Conference on*, Mahdia, pp. 1-6.

[39] **Razavi, B.** (2001). *Design of Analog CMOS Integrated Circuits*. McGraw-Hill publisher.

[40] **Yodprasit, U., and Ngarmnil, J.** (2000). Q-enhancing technique for rf CMOS active inductor. Circuits and Systems, 2000. *Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on*, Geneva, pp. 589-592.

[41] **Uyanik, H., and Tarim, N.** (2007). Compact low voltage high-Q CMOS active inductor suitable for RF applications. *Analog Integrated Circuits and Signal Processing*, 51:191–194.

[42] **Krishnamurthy, S.V., El-Sankary, K., and El-Masry, E.** (2010). Noise-Cancelling CMOS Active Inductor and Its Application in RF Band-Pass Filter Design. *International Journal of Microwave Science and Technology, Hindawi, Volume 2010*.

[43] **Nair, M.U., Zheng, Y.J., and Lian, Y.** (2008). 1 V, 0.18 μm-area and power efficient UWB LNA utilising active inductors. *Electronics Letters, vol. 44*, no. 19, pp. 1127-1129.

[44] **Saberkari, A., Ziabakhsh, S., Martinez, H., and Alarcón, E.** (2016). Active inductor-based tunable impedance matching network for RF power amplifier application. *Integration, the VLSI Journal, Volume 52,* Pages 301-308.

[45] **Manjula, J., and Malarvizhi, S.** (2013). Design of low power low noise tunable active inductors for multiband RF front end communication circuits. *Communications and Signal Processing (ICCSP), 2013 International Conference on*, Melmaruvathur, pp. 868-872.

[46] **Mahmoudi, F., and Salama, C.A.T.**, (2006). 8 GHz 1V, CMOS quadrature downconverter for wireless applications. *Analog Integrated Circuits and Signal Processing, Volume 48*, Issue 3, pp 185–197

[47] **Cetinkaya, H., and Tarim, N.** (2008). A tunable active filter in CMOS for RF applications. *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on*, St. Julien's, pp. 121-124.

[48] **Akbari-Dilmaghani, R., Payne, A., and Toumazou, C.** (1998). A high Q RF CMOS differential active inductor. *In Proc. Int'l Conf. Electronics, Circuits Syst., volume 3*, pages 157–160.

[49] **Abdalla, M., Eleftheriades, G., and Phang, K.** (2006). A differential 0.13μm CMOS active inductor for high-frequency phase shifters. *In Proc. IEEE Int'l Symp. Circuits Syst.*, pages 3341–3344.

[50] **Kia, H.B.** (2014). Adaptive CMOS LNA using highly tunable active inductor. *Electrical Engineering (ICEE), 22nd Iranian Conference on*, pp.1-6.

[51] **Xu, J., Saavedra, C.E., and Guican, Chen.** (2011). An Active Inductor-Based VCO With Wide Tuning Range and High DC-to-RF Power Efficiency. *Circuits and Systems II: Express Briefs, IEEE Transactions on, vol.58,* no.8, pp.462-466.

[52] **Manjula, J., Malarvizhi, S.,** (2013). Design of low power low noise tunable active inductors for multiband RF front-end communication circuits. *Communications and Signal Processing (ICCSP), 2013 International Conference on,* pp. 3-5.

[53] **Momen, H.G., Yazgi, M., and Kopru, R.** (2015). A low loss, low voltage and high Q active inductor with multi-regulated cascade stage for RF applications. *2015 IEEE International Conference on Electronics, Circuits, and Systems (ICECS),* Cairo, pp. 149-152.

[54] **Zito, D., Fonte, A., and Pepe, D.** (2009). Microwave active inductors. *IEEE Microwave and Wireless Components Letters,* 19(7): 461-463.

[55] **Lai, Q., and Mao, J.** (2010). A new floating active inductor using resistive feedback technique. *IEEE Int. Microwave Symp.* pp. 23-28.

[56] **Hwang, K.S., Cho, C.S., Lee, J.W., and Kim, J.** (2008). High quality-factor and inductance of symmetric differential-pair structure active inductor using a feedback resistance design. *Microwave Symposium Digest, 2008 IEEE MTT-S International,* Atlanta, GA, pp. 1059-1062.

[57] **Ahmed, A., and Wight, J.** (2010). 6.7 GHz high-Q active inductor design using parasitic cancellation with process variation control. *Electronics Letters,* IET, 46(7): 486-487.

[58] **Saberkari, A., Ziabakhsh, S., Martinez, H., and Alarcón, E.** (2016). Active inductor-based tunable impedance matching network for RF power amplifier application. *Integration, the VLSI Journal, Volume 52,* Pages 301-308.

[59] **Li, N., et al.** (2015). High- Q Inductors on Locally Semi-Insulated Si Substrate by Helium-3 Bombardment for RF CMOS Integrated Circuits. *IEEE Transactions on Electron Devices, vol. 62,* no. 4, pp. 1269-1275.

[60] **Momen, H.G., Yazgi, M., and Kopru, R.** (2015). Designing a new high Q, fully CMOS tunable floating active inductor based on modified tunable grounded active inductor. *2015 9th International Conference on Electrical and Electronics Engineering (ELECO),* Bursa, pp. 1-5.

[61] **Szczepkowski, G., Baldwin, G., Farrell, R., and Young, M.** (2007). Wideband 0.18µm CMOS VCO Using Active Inductor with Negative Resistance. *Circuit Theory and Design, ECCTD 2007. 18th European Conference on,* Seville, pp. 990-993.

[62] **Zito, D., Fonte, A. and Pepe, D.** (2009). Microwave active inductors. *IEEE Microwave and Wireless Components Letters, Vol. 19,* No. 7, pp. 461-463.

[64] **Wang, S., Koickal, T.J., Hamilton, A., Mastropaolo, E., Cheung, R., and Smith, L.** (2013). A floating active inductor based CMOS cochlea filter with high tunability and sharp cut-off. *2013 IEEE International Symposium on Circuits and Systems (ISCAS2013),* Beijing, pp. 193-196.

[65] **Thanachayanont, and Payne, A.** (1996). VHF CMOS integrated active inductor. *Electronics Letters, vol. 32,* no. 11, pp.999-1000, May 1996

[66] **Bucossi, W., and Becker, J.** (2008). Practical Considerations In The Use of CMOS Active Inductors. *Silicon Monolithic Integrated Circuits in RF Systems, SiRF 2008. IEEE Topical Meeting on,* Orlando, FL, pp. 90-93

[67] **Bakken, T., and Choma, J.** (2003). Gyrator-Based Synthesis of Active On-Chip Inductances. *Analog Integrated Circuits and Signal Processing, Volume 34,* Issue 3, pp 171-181

[68] **Li, C., Gong, F., and Wang, P.** (2010). Analysis and design of a high-Q differential active inductor with wide tuning range. *IET Circuits Devices & Systems, Vol. 4,* No. 6, pp. 486-495.

[69] **Reja, M., Filanovsky, I. and Moez, K.** (2008). A CMOS 2.0–11.2 GHz UWB LNA using active inductor circuit. *Circuits and Systems, ISCAS 2008. IEEE International Symposium on,* Seattle, WA, pp. 2266-2269

[70] **Ren, S., and Benedik, C.** (2013). RF CMOS active inductor band pass filter with post fabrication calibration. *AEU - International Journal of Electronics and Communications, Volume 67,* Issue 12, Pages 1058–1067

[71] **Sunca, A., Cicekoglu, O., and Dundar, G.** (2012). A Wide Tunable Bandpass Filter Design Based on CMOS Active Inductor. *Ph.D. Research in Microelectronics and Electronics (PRIME), 2012 8th Conference on,* Aachen, Germany, pp. 1-4.

[72] **Zito, D., and Pepe, D.** (2010). LC-active VCO for CMOS RF transceivers. *International Journal of Circuit Theory and Application, Volume 38,* Issue 1, pages 69–84.

[73] **Branchi, P., Pantoli, L., Stornelli, V., and Leuzzi, G.** (2015). RF and microwave high-Q floating active inductor design and implementation. *International Journal of Circuit Theory and Applications, Volume 43,* Issue 8, pages 1095–1104.

[74] **Lsmail, M., Wassenaar, R., and Morrison, W.** (1991). A high-speed continuous-lime bandpass VHF filter in MOS technology. *Proc. IEEE ISCAS'YI, Vol. 3,* pp. 1761-1764.

[75] **Wu, Y., Ismail, M., and Olssan, H.** (2000). A novel CMOS fully differential inductorless RF bandpass filter. *Proc. IEEE ISCAS'2000, Vol. 4,* pp. 149-152.

[76] **Khoury, S.G.E.** (1996). New Approach to the design of Active Floating Inductors in MMIC technology. *IEEE Transactions on Microwave theory and Techniques, Vol. 44,* (No. 4), pp. 505-512.

[77] **Chang, Y., Choma, J., and Wills, J.** (2000). The Design and Analysis of a RF CMOS Bandpass Filter. *IEEE International Symposium on Circuits and Systems, Vol. 2,* pp. 625-628.

[78] **Rafei, M., and Mosavi, M.R.** (2013). A New 0.25–12.5 GHz High Quality Factor Low-Power Active Inductor Using Local RC Feedback to Cancel Series-Loss Resistance. *Arab J Sci Eng, Volume 38,* Issue 11, pp 3125–3132.

[79] **Nagel, I., Fabre, L., Pastre, M., Krummenacher, F., Cherkaoui, R., and Kayal, M.** (2012). Tunable floating active inductor with internal offset reduction. *Electronics Letters, vol.48,* no.13, pp.786-788.

[80] **Branchi, P., Pantoli, L., Stornelli, V., and Leuzzi, G.** (2015). RF and microwave high-Q floating active inductor design and implementation. *Int. J. Circ. Theor. Willey, volume 43*:1095–1104.

[81] **Tripetch, K.** (2014). Symbolic Analysis of Input Impedance of CMOS Floating Active Inductors with Application in Fully Differential Bandpass Amplifier. *2014 IEEE 79th Vehicular Technology Conference (VTC Spring),* Seoul, pp. 1-6.

[82] **Ibrahim, M.A., Minaei, S., Yuce, E., Herencsar, N. and Koton, J.** (2012). Lossy/Lossless Floating/Grounded Inductance Simulation Using One DDCC. *Radioengineering, Vol. 21*, NO. 1.

[83] **Szczepkowski, G., Baldwin, G., and Farrell, R.** (2007). Wideband 0.18µm CMOS VCO using active inductor with negative resistance. *Circuit Theory and Design ECCTD 2007. 18th European Conference on,* Seville, pp. 990-993.

[84] **Karacaoglu, U., and Robertson, I.D.** (1995). MMIC active bandpass filters using varactor-tuned negative resistance elements. *IEEE Transactions on Microwave Theory and Techniques, vol. 43*, no. 12, pp. 2926-2932.

[85] **Hwang, K.S., Cho, C.S., Lee, J.W., and Kim, J.** (2008). High quality-factor and inductance of symmetric differential-pair structure active inductor using a feedback resistance design. *Microwave Symposium Digest, 2008 IEEE MTT-S International,* Atlanta, GA, pp. 1059-1062

[86] **Chen, M., and Lin, J.** (2009). A 0.1–20 GHz Low-Power Self-Biased Resistive-Feedback LNA in 90 nm Digital CMOS. *IEEE Microwave and Wireless Components Letters, vol. 19,* no. 5, pp. 323-325.

[87] **Reja, M.M., Moez, K., and Filanovsky, I.** (2010). An Area-Efficient Multistage 3.0- to 8.5-GHz CMOS UWB LNA Using Tunable Active Inductors. *IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 57,* no. 8, pp. 587-591.

[88] **Chen, Y., Mak, P.I., Zhang, L., Qian, H., and Wang, Y.** (2013). A Fifth-Order 20-MHz Transistorized- LC -Ladder LPF With 58.2-dB SFDR, 68- \mu\hbox {W/Po\le/MHz} Efficiency, and 0.13- \hbox {mm}^{2} Die Size in 90-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 60,* no. 1, pp. 11-15.

[89] **Yuan, F.** (2008). *CMOS Active Inductors and Transformers: Principle, Implementation, and Applications.* Springer.

[90] **Bunch, R.L., and Raman, S.** (2003). Large-signal analysis of MOS varactors in CMOS -Gm LC VCOs. *IEEE Journal of Solid-State Circuits, vol. 38,* no. 8, pp. 1325-1332.

[91] **Sameni, P., et al.** (2005). Modeling of MOS varactors and characterizing the tuning curve of a 5-6 GHz LC VCO. *2005 IEEE International Symposium on Circuits and Systems, Vol. 5,* pp. 5071-5074

[92] **Tavakoli H., and Sani, E.A.** (2013). A new method for eliminating cross axis sensitivity in two axis capacitive micromachined accelerometers. *2013 21st Iranian Conference on Electrical Engineering (ICEE),* Mashhad, pp. 1-5.

[93] **Zhou, X., Che, L., Liang, S., Lin, Y., Li, X., and Wang, Y.** (2015). Design and fabrication of a MEMS capacitive accelerometer with fully symmetrical double-sided H-shaped beam structure. *Microelectronic Engineering,* Elsevior, *Volume 131,* Pages 51–57.

[94] **Tsuchiya, T., and Funabashi, H.** (2004). A z-axis differential capacitive SOI accelerometer with vertical comb electrodes. *Sensors and Actuators J.,* Elsevior, *Volume 116,* Pages 378–383.

[95] **Rödjegårda, H., Johanssonb, C., Enokssonc, P., and Andersson, G.** (2005). A monolithic three-axis SOI-accelerometer with uniform sensitivity. *Sensors and Actuators A: Physical, Volumes 123–124,* Pages 50–53.

[96] **Tanga, B., Satob, K., Xia, S., Xiea, G., Zhanga, D., and Chenga, Y.** (2014). Process development of an all-silicon capacitive accelerometer with a highly symmetrical spring-mass structure etched in TMAH + Triton-X-100. *Sensors and Actuators A: Physical, Volume 217,* Pages 105–110.

[97] **Junseok, C., Kulah, H., and Najafi, K.** (2005). A monolithic three-axis micro-g micromachined silicon capacitive accelerometer. *Journal of Microelectromechanical Systems, vol. 14,* no.2, pp.235-242.

[98] **Sethuramalingam, T.K., and Vimalajuliet A.** (2010). Design of MEMS based capacitive accelerometer. *Mechanical and Electrical Technology (ICMET), 2010 2nd International Conference on,* pp.565-568.

[99] **Benmessaoud, M., and Nasreddine M.M.** (2013). Optimization of MEMS capacitive accelerometer. *Microsystem Technologies,* Springer, *Volume 19,* pp 713-720.

[100] **Akhtar, K., and Juliet, A.V.** (2013). Design of MEMS capacitive accelerometer with different perforated proof- mass for enhancement of performance. *Journal of Electronics and Communication Engineering, Volume 5,* PP 80-87.

[101] **Samyuktha, N., Maneesha, P., Sreelakshmi, B.R., Pattnaik, P.K., and Narayan, K.** (2015). Application of MEMS based capacitive sensor for continuous monitoring of glucose. *TENCON 2015 - 2015 IEEE Region 10 Conference,* Macao, pp. 1-4.

[102] **Aydemira, A., Terzioglua, Y., and Akin, T.** (2016). A new design and a fabrication approach to realize a high performance three axes capacitive MEMS accelerometer. *Sensors and Actuators A: Physical, Volume 244,* Pages 324–333.

[103] **Momen, H.G., Tavakoli, H., and Sani, E.A.** (2016). A 3-Axis MEMS Capacitive Accelerometer Free of Cross Axis Sensitivity. *24th Iranian Conference on Electrical Engineering (ICEE),* Shiraz, Iran.

[104] **Preethichandra, D.M.G., and Shida, K.** (2001). A simple interface circuit to measure very small capacitance changes in capacitive sensors. *Instrumentation and Measurement, IEEE Transactions on, vol. 50,* no.6, pp.1583-1586.

[105] **Wang, Y. and Chodavarapu, V.P.** (2014). Design of a CMOS readout circuit for wide-temperature range capacitive MEMS sensors. *Quality Electronic Design (ISQED), 2014 15th International Symposium on*, pp.738-742.

[106] **Amini, B.V., and Ayazi, F.** (2004). A 2.5-V 14-bit ΣΔ CMOS SOI capacitive accelerometer. *Solid-State Circuits, IEEE Journal of, vol.39,* no.12, pp. 2467-2476.

[107] **Qu, H., Fang, D., and Xie, H.** (2008). A Monolithic CMOS-MEMS 3-Axis Accelerometer with a Low-Noise, Low-Power Dual-Chopper Amplifier. *Sensors Journal, IEEE, vol.8,* no.9, pp.1511-1518.

[108] **Momen, H.G., Yazgi, M., and Kopru, R.** (2015). A Low Loss, Low Voltage and High Q Active Inductor with Multi-Regulated Cascade Stage for RF Applications. *Proc. of ICECS 2015*, pp. 149-152, Cairo-Egypt.

[109] **Szczepkowski, G., Baldwin, G., and Farrell, R.** (2007). Wideband 0.18μm CMOS VCO using active inductor with negative resistance. *Circuit Theory and Design (ECCTD 2007), 18th European Conference on,* Seville, pp. 990-993.

[110] **A. Mal, R. Mehra, A. K. Dwivedi and A. Islam,** (2015). CMOS based compact wide band tunable active inductor design," Innovations in Information, Embedded and Communication Systems (ICIIECS), 2015 International Conference on, Coimbatore, 2015, pp. 1-6.

[111] **Hammadi, A.B., Mhiri, M., Haddad, F., Saad, S. and Besbes, K.** (2015). Design of wide-tuning high-Q differential active inductor for multistandard applications. *Systems, Signals & Devices (SSD), 2015 12th International Multi-Conference on,* Mahdia, pp. 1-6.

[112] **Pantoli, L., Stornelli, V., and Leuzzi, G.** (2015). Class AB gyrator-based active inductor. *Integrated Nonlinear Microwave and Millimetre-wave Circuits Workshop (INMMiC 2015),* Taormina, pp. 1-3.

[113] **De, B.P., Ghoshal, S.P., Kar, R., and Mandal, D.** (2015). Optimal selection of components value for analog active filter design using simplex particle swarm optimization. *International Journal of Machine Learning and Cybernetics, Volume 6,* Issue 4, pp 621–636.

[114] **Matteis, M.D., Pezzotta, A., D'Amico, S., and Baschirotto, A.** (2015). A 33 MHz 70 dB-SNR Super-Source-Follower-Based Low-Pass Analog Filter. *IEEE Journal of Solid-State Circuits, vol. 50,* no. 7, pp. 1516-1524.

[115] **Kumngern, M., Khateb, F., Dejhan, K., Phasukkit, P., and Tungjitkusolmun, S.** (2013). Voltage-Mode Multifunction Biquadratic Filters Using New Ultra-Low-Power Differential Difference Current Conveyors. *Radioengineering, Vol. 22,* No. 2.

[116] **Senani, R., Bhaskar, D.R., and Singh, A.K.** (2014). First, Second and Higher Order Filter Design Using Current Conveyors. *Current Conveyors*. Springer.

[117] **Wang, S., Koickal, T.J., Hamilton, A., Mastropaolo, E., Cheung, R., and Smith, L.** (2013). A floating active inductor based CMOS cochlea filter with high tunability and sharp cut-off. *2013 IEEE International Symposium on Circuits and Systems (ISCAS2013)*, Beijing, pp. 193-196.

[118] **Halkhams, I., Hamdani, W.E., Mazer, S., and Bekkali, M.E.** (2014). Comparative study between CMOS and pHEMT active filter. *Proceedings of 2014 Mediterranean Microwave Symposium (MMS2014)*, Marrakech, pp. 1-4

[119] **Pantoli, L., Stornelli, V., and Leuzzi, G.** (2015). RF active circuit simulating a floating inductance. *Integrated Nonlinear Microwave and Millimetre-wave Circuits Workshop (INMMiC) 2015*, Taormina, pp. 1-3.

[120] **Pramanik, A., and Gupta, A.K.** (2015). Implementation of low frequency band pass filter by 3-OTA based floating active inductor. *2015 Communication, Control and Intelligent Systems (CCIS)*, Mathura, pp. 255-258.

[121] **Hu, F., and Mouthaan, K.** (2014). L-band bandpass filter with high out-of-band rejection based on CMOS active series and shunt inductors. *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, Tampa, FL, 2014, pp. 1-3.

[122] **Yarman, B.S.** (1999). *Broadband networks*. Wiley Encyclopedia of Electrical and Electronics Engineering.

[123] **Yarman, B.S.** (2010). *Design of Ultra Wideband Power Transfer Networks*. Wiley.

[124] **Sengul, M.,** (2013). Design of Practical Broadband Matching Networks with Lumped Elements. *Circuits and Systems II: Express Briefs, IEEE Transactions on, vol.60,* no.9, pp.552-556.

[125] **Momen, H.G., Yazgi, M., Kopru, R., and Saatlo, A.N.** (2016). Design of a new low loss fully CMOS tunable floating active inductor. *Analog Integrated Circuits and Signal Processing Journal*, Springer.

[126] **Youla, DC.A,** (1964). New theory of broadband matching. IEEE *Trans Circ Theory*, 11:30–50.

[127] **Fano, RM.** (1950). Theoretical limitations on the broadband matching of arbitrary impedances. *Journal of Franklin Institution*, 249:57–83.

[128] **Wu, H., Liu, C.** (2013). Broadband Matching Network Design for Antennas Using Invasive Weed Optimization Algorithm. *Cyber-Enabled Distributed Computing and Knowledge Discovery (CyberC), 2013 International Conference on*, pp. 500-503.

[129] **Yarman, B.S., Sengul, M., and Kilinc, A.** (2007). Design of Practical Matching Networks with Lumped Elements via Modeling. *Circuits and Systems I: Regular Papers, IEEE Transactions on, vol.54,* no.8, pp. 1829-1837.

[130] **Sengül, M.** (2008). Modeling based real frequency technique. AEU - International Journal of Electronics and Communications, *Volume 62,* Issue 2, Pages 77–80.

[131] **Carlin, H.J.** (1977). A new approach to gain-bandwidth problems. *IEEE Trans. Circuits Syst., vol. CAS-23,* no. 4, pp. 170–175.

[132] **Carlin, H.J., and Civalleri, P.P.** (1998). *Wideband Circuit Design*. Boca Raton, FL, USA: CRC Press.

[133] **Carlin, H.J., and Yarman, B.S.,** (1983). The double matching problem: Analytic and real frequency solutions. *IEEE Trans. Circuits Syst., vol. CAS-30,* no. 1, pp. 15–28.

[134] **Fettweis,** (1979). Parametric representation of Brune functions. *Int. J. Circuit Theory Appl., vol. 7,* no. 1, pp. 113–119.

[135] **Yarman, B.S.** (1982). A simplified real frequency technique for broadband matching complex generator to complex loads. *RCA Rev., vol. 43,* pp. 529–541.

[136] **Yarman, B.S., and Carlin, H.J.** (1982). A simplified real frequency technique applied to broadband multi-stage microwave amplifiers. *IEEE Trans. Microw. Theory Tech.,* vol. MTT-30, no. 12, pp. 2216–2222.

[137] **Köprü, R., Kuntman, H. and Yarman, B.S.** (2013). A novel method to design wideband power amplifier for wireless communication. *2013 IEEE International Symposium on Circuits and Systems (ISCAS2013),* Beijing, pp. 1942-1945.

[138] **Köprü, R., Kuntman, H. and Yarman, B.S.** (2013). Novel Approach to Design Ultra Wideband Microwave Amplifiers: Normalized Gain Function Method. *Radioengineering, VOL. 22,* NO. 3.

[139] **Nesimoglu, T., Aydın, Ç., Atilla, D.Ç, and Yarman, B.S.** (2013). A frequency tunable broadband amplifier utilizing tunable capacitors and inductors. *Microwave Techniques (COMITE), 2013 Conference on,* Pardubice, pp. 65-68.

[140] **Kılınç, S., Köprü, R., Aksen, A. and Yarman, B.S.** (2014). Mixed element wideband microwave amplifier design via simplified real frequency technique. *2014 Mediterranean Microwave Symposium (MMS2014),* Marrakech, pp. 1-3.

[141] **Saad, S., Mhiri, M., Hammadi, A.B., and Besbes, K.** (2016). A New Low-power, High-Q, Wide Tunable CMOS Active Inductor for RF Applications. *IETE Journal of Research,* 62:2, 265-273.

[142] **Thanachayanont, A., and Payne A.** (2000). CMOS floating active inductor and its applications to bandpass filter and oscillator designs. *Circuits, Devices and Systems, IEE Proceedings, Vol. 147,* no.1, pp.42-48.

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  - MEMS capasitive Pressure Sesor, Design and Simulation with MEMS Tech.

- Erasmus IP grants for T.I.M.E. European Summer School, 2013.

PUBLICATIONS, PRESENTATIONS AND PATENTS ON THE DISSERTATION:

- **Momen, H.G.,** Yazgi, M., Kopru, R. and Saatlo, A.N. (2016): Design of a New Low Loss Fully CMOS Tunable Active Inductor, *Analog Integrated Circuits and Signal Processing, Springer*, doi: 10.1007/s10470-016-0784-3.
- **Momen, H.G.,** Yazgi, M., Kopru, R. and Saatlo, A.N. (2016): An Accurate CMOS Interface Small Capacitance Variation Circuit for Capacitive Sensor, *International Journal of Electronics Letters, Taylor & Francis*, Accepted (Awaiting Production).
- **Momen, H.G.,** Yazgi, M., Kopru, R. and Saatlo, A.N. (2016): Low-Loss Active Inductor with independently Adjustable Self-Resonance Frequency and Auality Factor Parameters, *Integration, the VLSI Journal, Elsevier*, under revision
- **Momen, H.G.,** Yazgi, M., Kopru, R. and Saatlo, A.N. (2016): Low-Loss CMOS Active Inductor Circuit, *Frequenz, Taylor & Francis*, under review.
- **Momen, H.G.** & Tavakkoli H. (2016): A 3-Axis Accelerometer Free of Cross Axis Sensitivity, *Journal of the Chinese Institute of Engineers, Taylor & Francis,* under review.
- **Momen, H.G.,** Yazgi, M. & Kopru, R. (2015): A Low-loss, Low Voltage And High Q Active Inductor With Multi-Regulated Cascade Stage For RF Applications, *2015 IEEE International Conference on Electronics, Circuits and Systems* (*ICECS*), Dec. 6-9, 2015, Cario. DOI: 10.1109/ICECS.2015.7440271
- **Momen, H.G.,** Yazgi, M. & Kopru, R. (2015): Designing A New High Q Fully CMOS Tunable Floating Active Inductor Based On Modified Tunable Grounded Active Inductor, *2015 9th international conference on electrical and electronic engineering (ELECO),* Nov. 26-28, 2015, Bursa.
- **Momen, H.G.,** Tavakkoli H. & Sani. A.B. (2016): A 3-Axis MEMS Capacitive Accelerometer Free Of Cross Axis Sensitivity, 2016 24th Iranian Conference on Electrical Engineering (ICEE), May 10-12, Shiraz.
- **Momen, H.G.,** Yazgi, M., Kopru, R. and Saatlo, A.N. (2016): A New High Performance CMOS Active Inductor, *39th International Conference on Telecommunications and Signal Processing* (*TSP*), June 27-29, Vienna.
- **Momen, H.G.** & Kopru, R. (2016): A Method for Low Pass Filter Designing By Commensurate Transmission Lines, *39th International Conference on Telecommunications and Signal Processing* (*TSP*), June 27-29, Vienna.
- **Momen, H.G.,** Yazgi, M., Kopru, R. and Saatlo, A.N. (2016): CMOS High-Performance UWB Active Inductor Circuit, 2016 12th Conference on *Ph.D. Research in Microelectronics and Electronics (PRIME),* June 27-30, Lisbon.

OTHER PUBLICATIONS, PRESENTATIONS AND PATENTS :

JOURNAL PAPERS:

- Naderi Saatlo, A., Khoei, A., Hadidi, Kh. and **Ghasemzdeh, H**. (2009). A new high speed and low power four-quadrant CMOS analog multiplier in current mode. *International Journal of Electronics and Communications* (*AEU*), vol. 63, no. 9, 769-775, (IF=0.51).
- Naderi Saatlo, A., **Ghasemzadeh, H.,** Pourazar, A. and Aliasghary, M. (2009). Design of a Fuzzy Controller Chip with New Structure Supporting Rational-Powered Membership Functions, *Amirkabir Journal, International Journal of Electrical and Electronics Engineering*, vol. 41, no. 2, pp. 65-71, (ISC indexed).

CONFERANCE PAPERS:

- Naderi Saatlo, A., Aliasghary, M., Pourazar, A. and **Ghasemzadeh, H.** (2011). A 19MFLIPS CMOS Fuzzy Controller to Control Continuously Variable Transmission Ratio, *Ph.D. Research in Microelectronics and Electronics (PRIME), 2011 7th Conference on* , vol., no., pp.45-48.
- Aliasghary, M., Naderi Saatlo, A., **Ghasemzadeh, H.** and Pourazar**,** A. (2011). Design of Radial Basis Function Neural Networks Controller Based on Sliding Surface for a Coupled Tanks System, *Information Technology and Artificial Intelligence Conference (ITAIC), 2011 6th IEEE Joint International* , vol.1, no., pp.8-12.
- Naderi Saatlo, A., **Ghasemzadeh, H.**, Khoei, A. and Hadidi, Kh. (2010). Design of a Fuzzy Controller Chip with New Structure, Supporting Rational-Powered Membership Functions, *17th International Conf. on Electrical Engineering, Elec. And Comp. (ICEE) Tehran, Iran*, pp. 29 - 36.
- Naderi Saatlo, A., Mojarrad, H., **Ghasemzadeh, H.,** Khoei, A. and Hadidi, Kh. (2009). Four-Quadrant CMOS Analog Multiplier Based on New Current Squarer Circuit with High-Speed, *EUROCON 2009, EUROCON '09. IEEE* , vol., no., pp.282-287.
- Naderi Saatlo, A., Mojarrad, H., **Ghasemzadeh, H.,** Khoei, A. and Hadidi, Kh. (2009). Circuit Implementation of Programmable High-Resolution Rational-Powered Membership Functions in Standard CMOS Technology, *EUROCON 2009, EUROCON '09. IEEE* , vol., no., pp.1236-1241.