ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

FULLY INTEGRATED VOLTAGE REFERENCE CIRCUITS

Ph.D. THESIS

Pınar Başak BAŞYURT

Department of Electronics and Communication Engineering

Electronics Engineering Programme

APRIL 2014

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(504072205)

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

TAMAMIYLA TÜMLEŞTİRİLMİŞ GERİLİM REFERANS DEVRELERİ

DOKTORA TEZİ

Pınar Başak BAŞYURT
(504072205)

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Elektronik Mühendisliği Programı

Tez Danışmanı: Assist. Prof. Dr. Devrim Yılmaz AKSIN

NİSAN 2014

Pınar Başak BAŞYURT, a Ph.D. student of ITU Graduate School of Science Engineering and Technology 504072205 successfully defended the thesis entitled **"FULLY INTEGRATED VOLTAGE REFERENCE CIRCUITS"**, which he/she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor :	**Assist. Prof. Dr. Devrim Yılmaz AKSIN** Istanbul Technical University	.....
Jury Members :	**Assist. Prof. Dr. Devrim Yılmaz AKSIN** Istanbul Technical University	.....
	Prof. Dr. Franco MALOBERTI University of Pavia	.....
	Prof. Dr. Ali TOKER Istanbul Technical University	.....
	Prof. Dr. Yasar GÜRBÜZ Sabancı University	.....
	Assoc. Prof. Dr. Türker KÜYEL Istanbul Technical University	.....

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To my parents,

FOREWORD

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ABBREVIATIONS

ADC	**:** Analog to Digital Converter
BGR	**:** Bandgap Reference
BJT	**:** Bipolar Junction Transistor
CMOS	**:** Complementary Metal Oxide Semiconductor
CRL	**:** Current Regulated Loop
CTAT	**:** Complementary-to-Absolute Temperature
DAC	**:** Digital to Analog Converter
DCRL	**:** Duty-Cycle Regulated Loop
DTMOS	**:** Dynamic threshold MOS
EEPROM	**:** Electrically Erasable Programable Read Only Memory
FG	**:** Floating Gate
IC	**:** Integrated Circuit
JFET	**:** Junction Field Effect Transistor
LDR	**:** Load Regulation
LNR	**:** Line Regulation
MOSFET	**:** Metal-Oxide-Semiconductor Field Effect Transistor
PSD	**:** Power Spectral Density
PSR	**:** Power-Supply Rejection
PSRR	**:** Power-Supply Ripple Rejection
PTAT	**:** Proportional-to-Absolute Temperature
RBVP	**:** Reverse Bandgap Voltage Principle
RTS	**:** RandomTelegraphic Signal
SC	**:** Switched-Capacitor
SRH	**:** Shockley-Read-Hall
SoC	**:** System on Chip
SOI	**:** Silicon on Insulator
TC	**:** Temperature Coefficient
TIA	**:** Transimpedance Amplifier
XFET	**:** eXtra implantation junction Field Effect Transistor

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FULLY INTEGRATED VOLTAGE REFERENCE CIRCUITS

SUMMARY

Voltage references are one of the basic building blocks of many SoCs and mixed-signal ICs such as data converters, voltage regulators and operational amplifiers as they constitute a stable reference voltage for other sub-circuits to generate predictable and repeatable results. Ideally, this reference point should not change with external influences or operating conditions such as temperature, fabrication process variations, power supply variations and transient loading effects.

Along with the rapid development of modern communication systems and consumer products, which constitutes the main market for semiconductor industry, the market demand for these System on Chip (SoC) or Mixed Signal ICs to have lower power consumption, higher accuracy and lower cost, and thus, higher integration. Since the performance of the whole system depends strongly to the performance of the reference circuit, this work is focused on fully integrated voltage reference architectures.

With this motivation, firstly, different kinds of high precision low noise voltage reference circuits are designed in standard 0.35 μm CMOS technology that we have more experience and knowledge of. The essential goal of these studies was high precision and temperature coefficient of the designed voltage reference circuits are on the order of 3 ppm/°C with trimming after production. However, since 0.35 μm CMOS technology is used in these designs and also due to the chosen topologies, their minimum supply voltage can be down to 1.8 V and while current consumption is on the order of 20-30 μA. In the design of the this voltage reference block bulk isolation technique is proposed (for triple-well CMOS processes), in which system blocks are bulk isolated by a reverse biased junction diode from the rest of the die to drastically reduce substrate noise coupling. This is especially important if a very low power voltage reference is designed in a very noisy SoC. Moreover, the switched biasing technique, which is mostly applied to the oscillators, is also implemented to the designed BGR in order to improve the low noise performance of the circuit.

The rest of the thesis is focused on new voltage reference topologies that are appropriate for sub-micron technologies operating with low supply voltages. With this motivation two new low voltage and low power voltage reference topologies are proposed. The proposed voltage reference topologies are implemented and fabricated in 0.18 μm CMOS technology. Measurement results show that the proposed voltage reference circuits are working properly down to 0.65 V and achieve an output voltage of 193 mV with a temperature coefficient on the order of 50 ppm/°C in the temperature range of 0-120 °C. The total power consumption of the two designed voltage references are 0.3 μW and 0.4 μW at 27 °C, while occupying the area of 0.2 mm^2 and 0.08 mm^2, respectively. As a result, the proposed voltage reference topologies generate a reference voltage with comparable level of temperature coefficient and quite low

power consumption with respect to the other sub-1V voltage reference circuits reported in the literature.

TAMAMIYLA TÜMLEŞTİRİLMİŞ GERİLİM REFERANS DEVRELERİ

ÖZET

Gerilim referans devreleri, elektriksel sistemlerde diğer alt blokların çalışmaları için kararlı bir çalışma noktası üretmeleri sebebiyle veri dönüştürücüler (ADC - DAC), frekans sentezleyiciler, DC - DC ve AC - DC dönüştürücüler ve lineer regülatörler gibi pek çok elektriksel sistemin en temel yapı bloklarındandır. İdeal olarak, üretilen bu referans noktası, sıcaklık, üretim süreçleri, besleme gerilim değişimleri ve yükleme etkileri gibi çalışma koşullarından etkilenmemelidir. Bir referans devresinin doğruluğu bahsedilen çalışma koşullarının etkisiyle mutlak değerinden ne kadar saptığı olarak tanımlanır.

Modern haberleşme sistemleri ve tüketici ürünlerindeki gelişmeler ile birlikte yüksek entegrasyon ve doğruluklu sistemlere olan talep artmıştır. Bir sistemin performansı ise onu oluşturan alt bloklardan en kötü performansa sahip olanı tarafından sınırlanmaktadır. Tümdevre sistemlerinde, alt blokların çalışma noktalarını belirlemesi nedeniyle özellikle referans devrelerinin performansları bütün sistemin performansının belirlenmesinde önemli rol oynamaktadır. Düşük geometrili günümüz üretim teknolojileri yüksek entegrayon ve düşük maliyet ihtiyaçlarını, sayısal, analog ve RF blokları aynı kırmık üzerinde gerçekleyerek sağlamasına rağmen analog bloklar açısından yüksek doğruluk ve düşük besleme gerilimleri ile çalışılması gib bir çok problemi de beraberinde getirmektedir. Çünkü, sayısal devreler çok düşük besleme gerilimlerine (transistor eşik gerilimlerinden biraz daha fazla) kadar rahatlıkla çalışabilmelerine rağmen analog blokların pek çoğu için bu durum gerekli çıkış salınım genliği, giriş ortak işaret seviyesi vb. sebepler dolayısıyla mümkün olmamaktadır. Dolayısıyla yüksek performanslı sistemlere olan talep, bu performansların elde edilmesi için kullanılan düşük geometrili üretim teknolojilerine uygun, yani giderek azalan besleme gerilimleri ile çalışabilecek yüksek doğruluklu referans devrelerine olan talebi de arttırmıştır. Bu nedenle bu çalışmada yüksek doğruluklu ve düşük besleme gerilimi ile çalışabilecek standart CMOS band aralığı gerilim referans devre topolojilerine odaklanılmıştır.

Band aralığı referans devrelerinin çalışma prensibi, ileri aktif yönde kutuplanmış bir diyot gerilimini temel alıp birinci ve/veya daha yüksek dereceden sıcaklık kompanzasyonu yapılarak referans geriliminin elde edilmesine dayanmaktadır. Bu devrelerin bu adı almasının nedeni istenilen bir sıcaklık değeri için sıcaklık kompanzasyonu tam olarak yapıldığında çıkışta elde edilen referans geriliminin silisyumun band aralığı değerine ($\approx$1.2 V) eşit olmasıdır. Birinici dereceden BGR devrelerinin performansları özellikle yüksek sıcaklıkta etkin olan diyot geriliminin sıcaklığa logaritmik bağımlılığı ile sınırlanmaktadır. İkinci ve daha yüksek dereceden referans devrelerinde diyot geriliminin sıcaklığa bağlı polinomundaki lineer terimler ile birlikte logaritmik terim de kompanze edilmektedir.

Bu doğrultuda, öncelikle yüksek doğruluklu, düşük gürültülü band aralığı gerilim referans (BGR) devre topolojileri üzerinde çalışılarak farklı tasarımlar yapılmış ve 0.35 μm CMOS teknoljisinde gerçeklenmiştir. Tasarlananan band aralığı referans devreleri akım modlu çalışma presibine dayanmaktadır ve bu devrelerde yüksek doğruluk ihtiyacı, çıkış geriliminin nonlineer sıcaklık bağımlılığının yüksek dereceden eğrisel (curvature) düzeltme teknikleri uygulanarak giderilmesi ile sağlanmaya çalışılmıştır.

Yapılan tasarımlarda, gelenkesel işlemsel kuvvetlendirci yerine tek bir kazanç katı tercih edilerek önerilen devreler güç harcaması ve alan bakımından optimize edilmiştir. İlk BGR devresinin tasarımı sırasında, sıcaklık kompanzasyonunun yanısıra baz akımlarından kaynaklanan hatalar da önerilen yönetem ile kompanze edilmiştir. Bu tasarımlar sırasında (triple-well üretim teknlojileri için), önerilen blok gövde izolasyon stratejisi, tasarımı yapılan devrenin gövdesinin tümdevrenin geri kalan kısmından ters kutuplanmış bir jonksiyon diyodu sayesinde izole edilmesine dayanmaktadır ve devrenin gövde gürültüsünden etkilenmesini önemli ölçüde azalttığı gösterilmiştir. Bu durum, analog ve sayısal devre bloklaının bir arada bulunduğu karışık işaret tümdevre sistemleri (SoC) açısından oldukça önemlidir.

Sonuç olarak, ilk aşamada (bölüm 3) temel hedef, yüksek doğrulukluk olarak belirlenmiş ve yapılan tasarımlarda, üretim sonrası ayarlamalardan sonra sıcaklık katsayısı 3 ppm/$^\circ$C olabilecek devreler tasarlanmıştır. Ancak, tasarlanan BGR devreleri ile yüksek doğruluk ve düşük gürültü özellkikerinin sağlanmasına rağmen, 0.35 μm CMOS üretim teknolojisi kullanılması ve kullanılan topolojiler dolayısıyla, devrelerin çalışabileceği minimum besleme gerilim seviyesi 1.8 V ile sınırlı kalmıştır. Devrelerin çektikleri akımlar ise 20-30 μA seviyesindedir. Son olarak, çoğunlukla osilatör devrelerinde uygulanan anahtarlamalı kutuplama tekniği uygulanarak devrelerin düşük frekans gürültü performansının iyileştirilmesi amaçlanmıştır.

Çalışmanın geri kalan kısmında, düşük besleme gerilimleriyle (1V-altı) çalışabilecek mikron-altı üretim teknolojilerine uygun gerilim referans devre topolojileri üzerine odaklanılmıştır. Bu doğrultuda, standart CMOS üretim teknolojisine uygun iki yeni çok düşük besleme gerilimli ve düşük güç tüketimli gerilim referans devre topolojileri önerilmiştir. Önerilen topolojiler, bilinen temel akım modlu bad aralığı referans hücresi, bu hücrenin akımını sağlayan bir PMOS transistor (LDO) ve bu transistorun akımı kontrol etmek üzere tasarlanmış bir kontrol çevriminden oluşmaktadır. Bu kontrol çevrimi ise bir örnekme tabanlı (anahtarlamalı-kapasite mimarisinde) kuvvetendiriciye ve bu kuvvetlendiricinin sükunet halindeki çıkış gerilim değerinin giriş hatasını (sıcaklıkla) en aza indirecek şekilde optimize etmek üzere kompanze edilmesi temeline dayanmaktadır.

Önerilen iki gerilim referans topolojisi arasındaki temel fark, örnekleme tabanlı bu kuvvetlendiricinin çıkış geriliminin sıcak kompanzasyonun yapılmasına ilişkindir. Önerilen ilk topoloji de kuvvetlendiricinin çıkış gerilimin sıcaklık kompanzasyonu, kuvvetlendiricinin sıcaklıktan bağımısız bir akım yerine sıcaklıkla ters orantılı olarak değişen bir akım kullanılarak kutuplanmaı ile sağlanmıştır. İkinci toplojide ise kuvvetlendiricinin çıkış geriliminin sıcaklık kompanzasyonu kuvvetlendircin etkin fazının süresi ikinci bir geri besleme çevrimi tarafından kontrol edilerek sağlanmıştır. Bu topolojide kullanılan kuvvetlendirici tamamen aynı olmasına rağmen girişinde chopper yöntemi kullanılarak çıkışta iki farklı kontrol gerilimi üretilmiştir. Bu iki gerilimin farkı ile bir önceki topolojide sabit olan kuvvetlendirme fazının süresi

mimari yapısı örnekleme tabanlı kuvvetlendiriciye oldukça benzeyen değişken iş süreli (duty-cycle) bir işaret üreteci modüle edilerek kuvvetlendircinin çıkışında LDO için uygun kontrol gerilimin üretilmesi sağlanmıştır. Her iki geri besleme çevrimi de kuvvetlendirci çıkış geriliminin giriş gerilim hatasını (referans gerilimleri arasındaki farkı) en aza indirecek şekilde belirlemek üzere kurulmuştur.

Önerilen devrelerinin çalışabileceği minimum besleme geriliminin, topolojilerin geneline bakıldığında, elde edilmek istenilen referans gerilimi, eşik-altı bölgesinde çalışan PMOS transistorlar üzerindeki diyot gerilimi ve M_{LDO} üzerinde düşen gerilim değeri tarafından belirlendiği görülmektedir. Önerilen gerilim referans devreleri 0.18μm standart CMOS üretim teknolojisinde gerçeklenmiştir. Örneğin, bu teknolojide gerçeklenilen devrelerde, 200 mV çıkış gerilimi, 300 mV diyot gerilimi ve LDO transistoru üzerinde 100 mV gerilim düşümü ile yapılan tasarımda, bu devreler için minimum besleme gerilim değeri 0.6 V olarak ortaya çıkmaktadır. Ancak, devrenin çalışması ile ilgili alt bloklardan kaynaklanabilecek kısıtlamaların gözardı edilmemesi gerekmektedir. Nitekim, alt bloklar incelendiğine, devrenin geneli için verilen bu kısıtın en azından bu teknoloji için baskın olan kısıt olmadığı görülmüştür. Önerilen gerilim referans devrelerinin minimum besleme gerilimi, örnekleme tabanlı kuvvetlendiricinin giriş katı tarafından sınırlandırılmaktadır. Çünkü, gerçeklemenin yapıldığı üretim teknolojisinde giriş katında anahtar olarak kullanılan NMOS transistorlar için eşik gerilimlerinin 0.4 V mertebesindedir. Dolayısyla, 200 mV bir referans gerilimi ve 50 mV bir M_{LDO} çalışma gerilimi ile birlikte devrenin çalışabileceği minimum besleme geriliminin 0.65 V olacağı görülmektedir. Ayrıca, bu koşul nominal sıcaklıklar için geçerlidir, devrenin daha düşük sıcaklık değerlerinde de çalışması istendiği takdirde transistorların eşik gerilimlerinin artması nedeniyle ihtiyaç duyulan mininmum besleme gerilim değeri de bununla orantılı olarak artacaktır. Bu nedenle devrelerin ölçümleri sırasında 0.8 V besleme gerilimi nominal besleme gerilimi olarak kullanılarak performansları verilmiştir.

Ölçüm sonuçları, tasarlanan gerilim referans devrelerinin 0.65 V besleme gerilimi ile çalışabildiğini göstermiştir. Önerilen devre topolojileri ile 0-120 °C sıcaklık aralığında, sıcaklık katsayısı 50 ppm/°C olan 193 mV seviyesinde referans gerilimleri elde edilmiştir. Devrelerin güç tüketimleri sırasıyla 0.3 μW ve 0.4 μW iken kapladıkları alan 0.2 mm^2 ve 0.08 mm^2'dir. Sonuç olarak, önerilen devre topolojileri ile literatürde yer alan diğer 1V-altı referans devreleri ile karşılatrılabilir seviyede sıcaklık katsayısı olan referans gerilimleri çok daha düşük güç harcamasıyla elde edilmiştir.

1. INTRODUCTION

1.1 Motivation

Along with the rapid development of modern communication systems and consumer products, which constitutes the main market for semiconductor industry, the market demand for System on Chip (SoC) or Mixed Signal ICs with lower power consumption, higher accuracy and lower cost, thus, higher integration has increased.

Voltage references are one of the basic building blocks of many SoCs and mixed-signal ICs such as data converters, voltage regulators and operational amplifiers, as they constitute a stable reference voltage for other sub-circuits to generate predictable and repeatable results. Ideally, this reference point should not change with external influences or operating conditions such as temperature, fabrication process, power supply variations and transient loading effects.

Precision of a reference is described by the amount of fluctuation from its absolute value with respect to these variations. Absence of absolutely accurate quantities that can be used in IC, is the driving point for reference circuit topologies that depend on a ratio between two similar elements rather than the absolute characteristics of each individual element; since, any quantity that has dimensions or units is always a suspect of being inaccurate unless it is equal to a universal constant that does not depend on the fabrication process, supply voltage, or temperature.

Performance of a system made up of sub-blocks (either electrical or not) is limited by/with the sub-block that has the lowest performance/accuracy. Therefore, the performance of the system strongly depends on the reference circuits and the precision requirement of the reference depends on the given application. For instance, choosing a reference that has ± 1 mV tolerance may be effective for a 12-bit system, while 14-bit or 16-bit ADC/DAC applications demand higher precision references [1]. However, the growing demand for battery-operated circuits that require high accuracy and high performance with low quiescent current and low voltage operation increases the need

for higher precision and more stringent references [2]. On the other hand, for many applications low precision voltage references are also necessary for proper biasing. However, low voltage and low power operation and cost effective solutions are primary concerns in the design of references.

1.2 Primary Specifications in Voltage Reference Design

Voltage references have a pivotal role on the performance and accuracy of analog and mixed-signal systems and design specifications of a voltage reference rely on several factors, that are mostly governed by the overall system specifications.

The principal role of a voltage reference circuit is to generate an accurate and reliable reference voltage that should not fluctuate significantly under various operating conditions or in the presence of error sources such as temperature variations, variations in power supply voltages, process variations and transient loading effects. Therefore, performance of a reference is quantified by its deviation from its ideal value in its nominal operating conditions. Initial accuracy, temperature drift, line regulation, load regulation, quiescent current and input voltage range are the metrics that are describing the performance of a voltage reference.

The initial accuracy of a reference is the deviation of the actual output voltage from the desired specification and quantifies the effect of random process variations, mismatch, and package stresses on the DC accuracy of the reference voltage. Since this is a random effect, initial accuracy can only be specified with statistical analysis of an adequate number of samples and is defined as

$$Initial\ Accuracy = \pm\frac{3\sigma_{V_{REF}}}{\mu_{V_{REF}}} \tag{1.1}$$

where $\sigma_{V_{REF}}$ is the standard deviation and $\mu_{V_{REF}}$ is the mean value of the voltage reference. The most common method to achieve a given accuracy specification is using trim bits. Trimming procedure is generally carried out at room temperature for convenience, hence the initial accuracy is typically specified at room temperature (27°C).

Temperature coefficient (TC) is the typical metric used for quantifying temperature drift performance of the reference voltage and it is normally expressed in parts-per million per degree Celsius (ppm/°C) [2]. TC is given by:

$$TC = \frac{1}{V_{Nominal}} \frac{\Delta V_{REF}}{\Delta T} \tag{1.2}$$

where ΔT is the temperature difference between upper and lower extremes of the temperature range, ΔV_{REF} is the voltage difference between the maximum and minimum values of the reference voltage in this range, $V_{Nominal}$ is the nominal value of reference voltage, respectively. In other words, the TC of a reference is given by the deviation of the output voltage from its nominal value due to the change in temperature that affects the dc accuracy of the reference.

Line regulation (LNR) is a parameter which quantifies the DC immunity of the voltage reference with respect to the input voltage (i.e. power supply) and defined as the DC change in the output voltage (ΔV_{REF}) caused by the DC change of the input voltage (ΔV_{IN}). Typically it is expressed in ppm per volt or percentage per volt as follows:

$$LNR = \frac{\Delta V_{REF}}{\Delta V_{IN}} \tag{1.3}$$

An additional key parameter is the power supply ripple rejection (PSRR). It is an AC parameter that quantifies the AC immunity of the reference voltage to the power supply and is defined as the frequency dependent ratio of the small signal AC ripple in the reference voltage (δV_{REF}) induced by the corresponding ripple in the power supply (δV_{IN}). The PSRR is defined as:

$$PSRR = \frac{\delta V_{REF}}{\delta V_{IN}} \tag{1.4}$$

Load regulation (LDR) is another DC parameter that is defined by the DC change in the reference voltage (ΔV_{REF}) for a given DC change in the load current (ΔI_{OUT}). Moreover, the output impedance of the reference (Z_{out}) is a frequency dependent ac specification that quantifies the small signal change in the reference (δV_{REF}) for a small-signal change in the load current (δI_{OUT}). LDR and Z_{out} are given by

$$LDR = \frac{\Delta V_{REF}}{\Delta I_{OUT}} \tag{1.5}$$

$$Z_{out} = \frac{\delta V_{REF}}{\delta I_{OUT}} \tag{1.6}$$

Noise performance of a voltage reference is determined by the electrical noise on the output of a voltage reference. It can include wide-band thermal noise and narrow-band $1/f$ noise. Wide-band noise can be effectively filtered with a simple RC network. 1/f noise is inherent in the reference and cannot be filtered. It is specified in the 0.1 to 10 Hz range. Low 1/f noise references are important in precision designs [3].

Another concern in a voltage reference design is the process technology, since it limits the voltage reference topology choice and the achievable performance of the reference designed in that particular process. Standard bipolar and simple complementary metal oxide semiconductor (CMOS) processes, silicon-on-insulator (SOI) and BiCMOS technologies are the most common available process technologies. However, since the major portion of the semiconductor device production is digital, the standard CMOS technology is referred as technology of choice [4]. In addition, process parameters vary from die to die, wafer to wafer and lot to lot, so trimming and/or calibration of the reference circuit are also important concepts that are affecting the accuracy of a voltage reference.

As the demand for more stringent performance increases, the need for compensating first-order, second-order, and even higher-order temperature effects and parasitic effects become necessary. This increases the complexity of the circuits and demands for more complex structures, higher quiescent current, larger silicon area and higher input voltages.

1.3 Types of Voltage References

Voltage reference circuits can be classified in four different groups with respect to their design origin. In other words, the classification depends on which mechanism is used to build up the reference voltage. Examples are using diode voltages of a simple diode or a Zener voltage, the energy-band-gap voltage of integrated transistors, junction field effect transistors and tunnelling mechanism of diodes with floating gate architectures.

Each technology offers inherent performance characteristics that can be enhanced with compensation networks or additional active circuitry.

1.3.1 Simple diode and Zener references

The simplest way of generating a reference voltage is forcing a current through a forward-biased diode, as shown in Figure 1.1(a). The temperature drift performance will be approximately -2.2 mV/°C [2] and it has numerous deficiencies such as sensitivity to input voltage and/or loading current changes and inflexibility of the output voltage. The advantage of this type of shunt, or two-terminal references, is the reversible polarity by flipping connections and reversing the drive current; however, a basic limitation is that the load current must always be less than the driving current. Moreover, the resistor in series with the diode establishes a constant current allowing the diode to achieve a stable reference voltage.

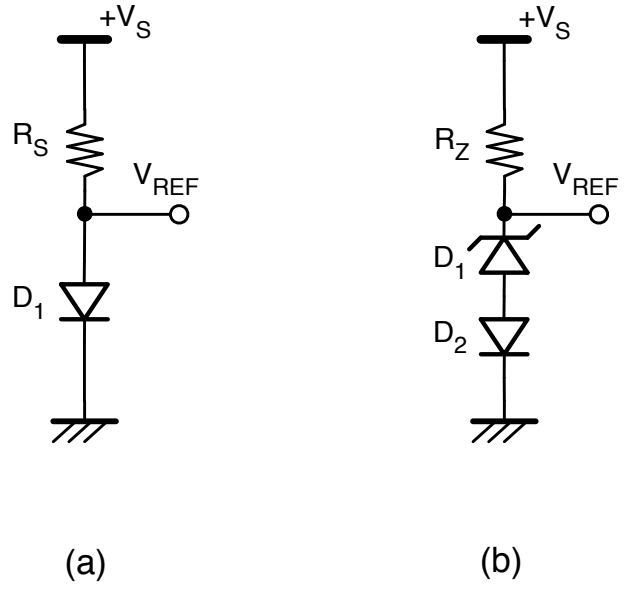

Figure 1.1: (a) Simple diode (b) Zener reference.

Another common realization of a voltage reference consists of using a Zener or avalanche diode, as shown in Figure 1.1(b). The diode operates in the reverse breakdown region since a current is forced to flow from the cathode of the diode. In this operating region, the load current changes cause nearly negligible fluctuations in diode voltage. While true Zener breakdown occurs below 5 V, avalanche breakdown takes place at higher voltages, in the range from 5 to 8 V, with a positive temperature

drift of approximately +1.5-5 mV/°C [2]. Therefore, Zener diodes are generally used for high voltage applications.

Additionally, in an IC, surface operated diode junction breakdown is prone to crystal imperfections and other contamination sources. For this reason, Zener diodes formed at the surface are more noisy and less stable than the buried (or sub-surface) Zener diodes [5]. In Figure 1.2, the cross-section view of a simple surface zener and of a buried zener is shown. As seen in Figure 1.2, in the buried zener, the junction is placed below the surface of the silicon, so well away from the region where contamination and oxide effects. Therefore, to improve the noise and drift performance of surface operated zener, buried zener diodes are more likely to be used in the design of voltage references.

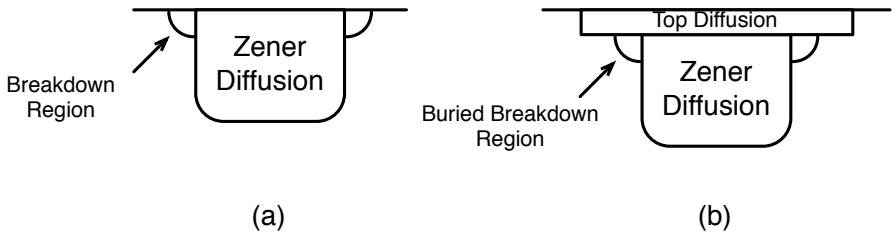

Figure 1.2: (a) Surface Zener (b) Buried (Sub-surface) Zener.

Buried zener references offer very low temperature drift, down to the 1-2 ppm/°C, and the lowest noise as a percent of the full-scale, i.e., 100 nV/$\sqrt{Hz}$ or less [6]. However, as mentioned before, they are not appropriate for low voltage applications since the zener voltage and operating current of zener type references are usually relatively high, typically on the order of 5 V and several mA, respectively.

1.3.2 Bandgap references

For relatively lower supply voltages, there is another class of voltage references, called "bandgap references", which are essentially forward biased diode references with first-order and second-order temperature compensation. The basic operation relies on the addition of two voltages having opposite temperature dependencies. The forward biased diode voltage decreases linearly with temperature except for a small curvature (or non linear dependency), so it has complementary to absolute temperature (CTAT) dependence. However, the voltage difference between two

forward biased diodes operating under different current densities results in a voltage that is proportional to absolute temperature (PTAT). In a bandgap reference, the generation of temperature-independent voltage V_{REF} is achieved through the addition of a CTAT voltage with an appropriately scaled PTAT voltage:

$$V_{REF} = V_{CTAT} + KV_{PTAT} \tag{1.7}$$

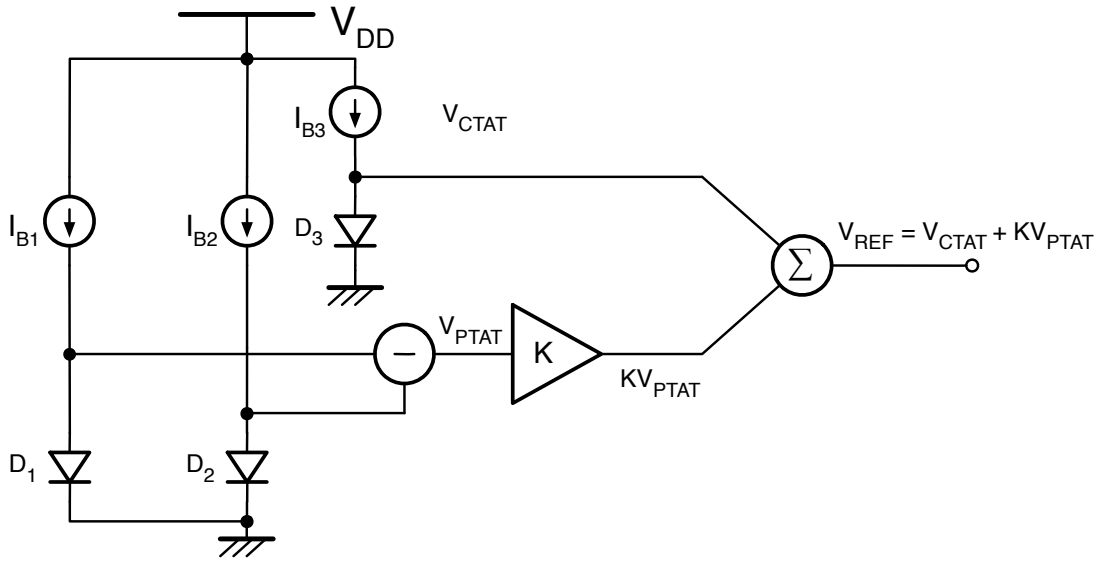

Figure 1.3: Principle of bandgap reference.

Traditionally, since the CTAT component is generated from a diode or from a base-emitter voltage of a BJT transistor, the value of the reference voltage is close to the bandgap voltage of silicon ($\approx$ 1.2 V). The reason is that the diode voltage has various temperature dependent terms and its zero-order or temperature-independent component is the bandgap voltage [7]. The temperature drift performance of the resulting reference voltage is between 20 and 100 ppm/°C [8]. Further improvement of the temperature drift performance is limited by the logarithmic temperature dependence of a diode voltage.

1.3.3 XFET voltage references

XFET (eXtra implantation junction Field Effect Transistor) references are a relatively new category of integrated references. Their design is based on the properties of junction field effect (JFET) transistors. The basic XFET based topology is shown in Figure 1.4. It consists of a pair of junction field effect transistors in which one of

the two transistors uses an extra ion implantation to raise its pinch-off voltage. The difference in the pinch-off voltages is amplified and used to generate the reference voltage. Therefore, from the operation principle point of view, this scheme is similar to the bandgap reference implemented with bipolar transistors.

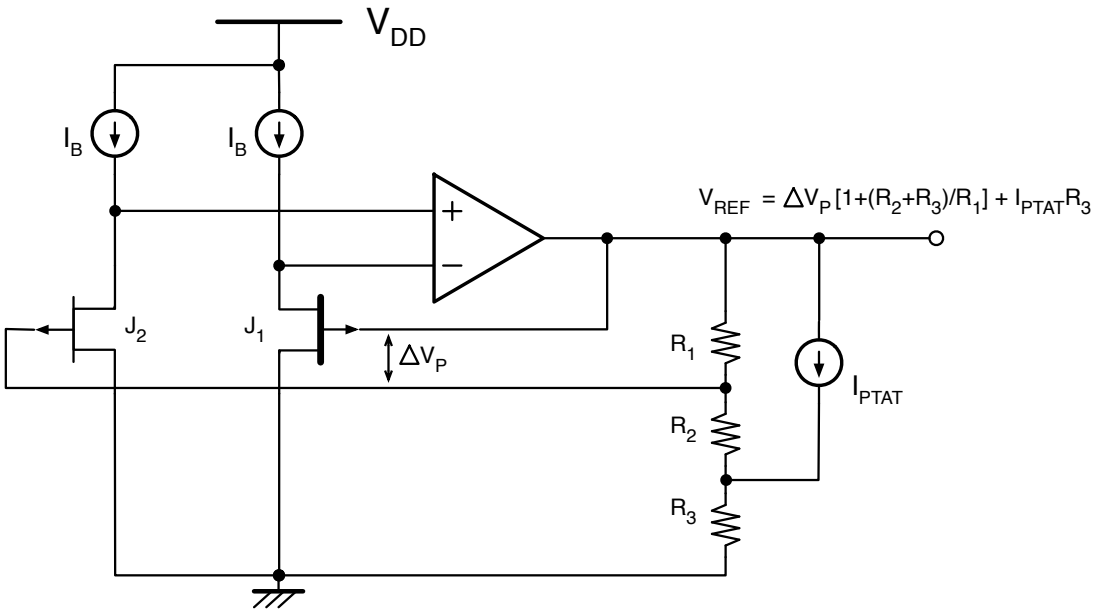

Figure 1.4: Basic XFET reference.

In Figure 1.4, J_1 and J_2 are driven with the same drain currents, I_B. J_1 is the JFET with the extra implantation and the difference between the pinch-off voltages, ΔV_P, will appear between the gates of J_1 and J_2 for identical current driving conditions and equal source voltages, which is ensured by the feedback loop with amplifier. As a result, reference voltage is obtained as:

$$V_{OUT} = \Delta V_P \left(1 + \frac{R_2 + R_3}{R_1}\right) + I_{PTAT} R_3 \qquad \textbf{(1.8)}$$

where I_{PTAT} is the positive temperature coefficient correction current to compensate for the negative temperature coefficient of XFET core. The overall temperature drift performance of the reference is in a range of 3-8 ppm/°C [6].

The XFET architecture provides a performance level in between bandgap and buried zener references since its noise level and temperature drift are lower than bipolar transistor based bandgap references for the equivalent current levels [3, 6].

1.3.4 Floating-gate voltage reference

Another relatively new high performance voltage reference topology is based upon EEPROM floating-gate technology, which allows storing a precise voltage on a floating gate.

A conceptual ideal voltage reference that is composed by an ideal switch and ideal capacitor is shown in Figure 1.5. The charge stored on the capacitor will be kept if there is no switching element present. In this case, the main issue for the realization of the ideal voltage reference becomes obtaining an ideal switch. In the work reported in [9] the switch is realized by using the so-called tunnel diodes, available in a given EEPROM technology. These diodes show very low leakage current and operate under the Fowler-Nordheim tunneling mechanism. The current-voltage expression is given by:

$$I_{TD} = C \times V_{TD}^2 \times \exp\left(-\frac{\alpha}{V_{TD}}\right) \tag{1.9}$$

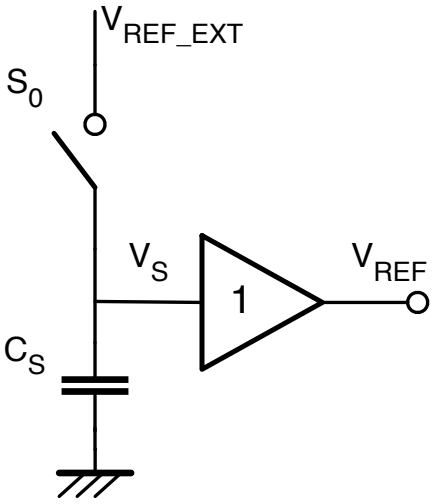

Figure 1.5: Conceptual ideal voltage reference.

The simplified schematic and cross-section of the floating-gate device, which is a conventional EEPROM memory cell, shown in Figure 1.6. The device consists of an NMOS transistor, an equivalent capacitance C_S, and two tunnel diodes, T1 and T2. As seen in the cross-section, the tunnel diode is fabricated as an oxide insulation between two conducting electrodes and the interior conducting node is isolated by oxide in all

the directions. Since this node is also the NMOS gate terminal, it is referred to as the "floating-gate".

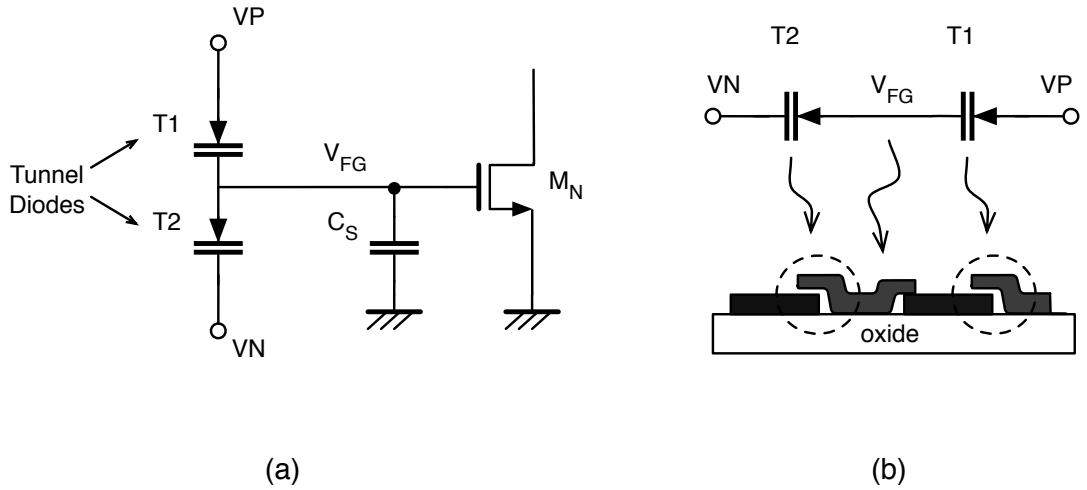

Figure 1.6: Simplified schematic and physical cross-section of FGMOS device/cell.

Since tunnel diodes are two-terminal devices, two tunnel diodes, one (T1) for charging and the other for discharging (T2), are required to obtain the desired voltage level at the floating gate. By raising VP FG node is charged through T1 and by lowering VN FG node is discharged through T2 until the desired voltage is set to FG node. Finally, by making VP and VN zero, tunnel diodes are turned off.

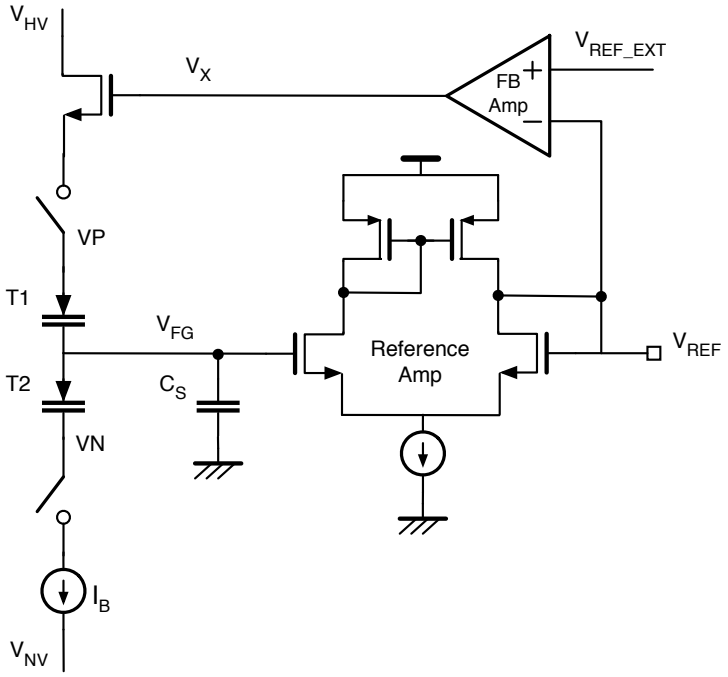

Figure 1.7: Simplified schematic floating-gate voltage reference.

The simplified schematic of the entire floating gate voltage reference is shown in Figure 1.7. To be able to continuously adjust the floating gate voltage, VN is connected to a current source I_B that pulls it down to a negative voltage thereby limiting the diode conduction current to an appropriate value. At the same time VP is connected to a large positive voltage source through a source follower. V_{HV} and V_{NV} are generated by on-chip charge pumps. As seen in Figure 1.7, an external voltage source is used during the calibration of the reference. Tunnel diodes are driven through the feedback loop that includes the additional feedback amplifier and sets the voltage on the floating gate. Finally, reference amplifier generates the reference voltage.

The voltage reference, fabricated in a 25 V 1.5 μm EEPROM CMOS process, achieves a temperature coefficient better than 1 ppm/°C with a total current consumption of 500 nA due to the sub-threshold region operation of the buffer amplifiers [9].

1.4 Scope of the Dissertation

The last century has witnessed an explosion in the market demand for battery-operated systems through the applications like cellular phones, personal digital assistants, and laptops. Therefore, circuits like DC-DC converters, linear regulators, and bandgap references, that form an integral component of their power management architecture, are critical to system performance. The primary market requirements for these portable systems are high functional integration, small size, and most importantly, low power and cost.

However, todays technology satisfy the need of functional integration and low cost by fabricating digital, RF and analog circuits on the same substrate (SoC), it poses number of design challenges for analog parts of the systems due to the required precision and low supply voltage limitation of sub-micron technologies. Indeed, it would be optimal to use a supply voltage on the order of 0.5-0.6 V since it is the voltage range a single solar cell can supply at its output and digital circuits can work with such low voltages. On the contrary, conventional analog blocks such as amplifiers and reference circuits need higher supply voltage due to the required overheads at the output stage and the necessary output swing.

In line with this motivation and these facts, this thesis concentrated on design of bandgap reference in standard CMOS technologies. At first, the need of high precision is tried to be solved through a curvature correction method in order to remove the nonlinear temperature dependency of output voltage. In this BGR circuits, a gain stage is utilized in stead of an operational amplifier to make the architecture compact and power efficient. During the design, base current compensation technique have been proposed and adopted with respect to the designed BGR circuit. Moreover, a block bulk isolation strategy proposed and adopted in order the suppress the substrate noise coupling which is especially important for mixed signal SoCs, since these systems have to incorporate both noise sensitive precision analog blocks as well as very large and noisy digital blocks. However, even if high temperature stability is achieved through these designed circuits, they are suffering from the need of relatively high supply voltage.

Therefore, in the second part of the thesis, the need of working with a sub-1V supply voltage and very low power is tried to be satisfied through the proposed new voltage reference architectures for standard CMOS technologies. The proposed architectures consist of a conventional current mode bandgap reference core and an LDO with its control circuitry formed by a sampled-data amplifier and its compensation circuit that provides the bias current of bandgap core. The minimum supply voltage depends on the required output level and a number of practical limits such as limitation coming from each sub-block utilized in the proposed architecture. For instance, in the preferred implementation, an output voltage of 200 mV, 300 mV across the PMOS diode, and a voltage drop as low as 100 mV across M_{LDO} lead to a supply voltage down to 0.6 V. This, however, it is not the only and also the dominant constraint in the circuit. The dominant one for determining the minimum supply voltage is due to the input stage of the proposed sampled data amplifier since in the used technology, the thresholds of the P-channel and the N-channel transistors are -0.45 V and 0.4 V, respectively. With an overdrive voltage of 50 mV, the minimum supply voltage is, hence, 0.65 V. However, this value increases for low temperatures as the transistors threshold voltage also increases. As a result, the performance of the designed and implemented circuits are obtained while using 0.8 V nominal supply voltage.

The main contributions of this thesis can be summarized as follows:

- Design and implementation of a higher-order compensation method in order to obtain high precision low noise BGR working with moderately high supply voltages.
- Development and implementation of block bulk isolation design strategy to reduce the noise coupling between blocks in the same die, which is especially important for mixed-signal SoCs that has to incorporate both noise sensitive analog blocks and noisy digital blocks.
- Design and implementation of new voltage reference generator architectures, which can work down to very low supply voltages with very low quiescent current through taking the advantage of sampled data operation while having moderate temperature stability (moderate precision).

1.5 Organization of the Dissertation

The objective of this research is to design and implement fully integrated CMOS voltage references. In particular, this thesis consists of two main bandgap reference designs; one of them focusing on a high precision, low noise BGR design that exhibits high immunity to substrate noise, the second one focusing on a low supply voltage and and low power BGR design in a standard CMOS technology. For this reason, firstly, primary specifications of voltage references and also types of voltage references are covered in chapter 1.

In order to understand and quantify those specifications, an overview of integrated devices utilized within the voltage reference circuits is given in chapter 2. For each device, their operation regions, temperature characteristics and matching performances/properties are summarized. Moreover, since the thesis concentrated on bandgap reference design, chapter conitunes with presenting the operational principles of BGR circuits and presents an extensive literature review on various kinds of BGR circuits with respect to different classification aspects such as temperature compensation order, topology or utilized devices.

In chapter 3, the design and implementation of high precision low noise BGR circuits are presented. The chapter starts with a curvature corrected current mode BGR circuit design and continues with improving the design by adopting the proposed block bulk isolation strategy in order to increase the immunity to substrate noise. Moreover, the switched biasing technique, which is mostly applied to the oscillators, is also implemented in the designed BGR in order to improve the low noise performance of the circuit. Chapter concludes with the measurement results obtained from the designed BGR circuits.

Chapter 4 concentrates on low voltage and low power bandgap reference design. With this motivation two different new voltage reference topologies are proposed utilizing sampled data operation. In this chapter, the design and implementation details of the two proposed voltage reference circuits are presented. Chapter concludes with the measurement results obtained from the designed low voltage low power BGR circuits.

Finally, in chapter 5, a conclusion of the thesis is given by summarizing all the information that has been presented. And possible future extensions to the current research is also discussed.

2. INTEGRATED DEVICES UTILIZED WITHIN THE VOLTAGE REFERENCE CIRCUITS AND LITERATURE REVIEW

In this chapter, an overview of integrated devices utilized within the voltage reference circuits in terms of their operation regions, temperature characteristics and matching performances/properties are summarized and an extensive literature review on various kinds of BGR circuits with respect to different classification aspects such as temperature compensation order, topology or utilized devices is presented.

2.1 Integrated Devices Utilized Within The Voltage Reference Circuits

2.1.1 Diode

Diodes are one of the simplest two-terminal semiconductor devices which have basically three different operating regions: forward-biased, reverse-bias and reversed-breakdown regions, as seen in Figure 2.1.

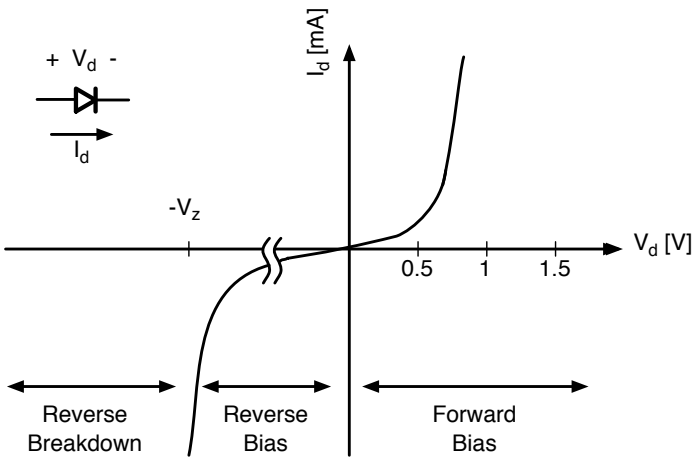

Figure 2.1: Typical $I-V$ curve of a junction diode.

When the voltage applied between two terminals (anode to cathode) is positive, the region of operation is called forward-biased and a significant amount of current flows once the applied voltage is higher than the value of the potential barrier. In this region, the diode current grows exponentially with the diode voltage:

$$I_D = I_S \left[\exp\left(\frac{V_D}{nV_T} \right) - 1 \right] \tag{2.1}$$

where I_D is the current flowing through the diode, I_S is the saturation current, V_D is the voltage across the diode, n is a process dependent constant and V_T is the thermal voltage that is directly proportional to the temperature:

$$V_T = \frac{kT}{q} \tag{2.2}$$

where k is Boltzmann's constant, T is the absolute temperature in Kelvins and q is the magnitude of the electron charge. At room temperature (27°C), the thermal voltage is approximately 25.8 mV.

Due to the exponential characteristic of the $I-V$ relationship in the forward-biased region, the diode voltage is approximately constant around 0.6 V for current levels ranging from a few to hundred micro-amps, which makes a forward-biased diode appropriate for generating a predictable and repeatable voltage.

When the diode anode-to-cathode voltage is between the breakdown voltage ($-V_z$) and "0", the operating region of the diode is called reverse-biased and, as seen in Figure 2.1, the current flowing through the diode in this region is significantly low. However, when the voltage across the junction exceeds the reverse-breakdown voltage, a significant amount of current starts flowing into the cathode terminal. This is due to the two mechanisms called "zener effect" and "avalanche effect".

The Zener effect is a type of electrical breakdown due to the increased electric field that enables tunneling of electrons from the valence to the conduction band of the semiconductor and leads to a large number of free minority carriers. This is generating a reverse current across the junction. Avalanche process occurs when the carriers in the transition region are accelerated by the electric field to energy levels sufficient to create more free electron-hole pairs through impact ionization, increasing the reverse current. The Zener effect is responsible for junction breakdown if breakdown occurs when the reverse-bias voltage is less then 5 V whereas avalanche breakdown occurs when the reverse-bias voltage is higher than 7 V. When the reverse-bias voltage is between 5 and 7 V, the breakdown mechanism can be ascribed to either one of the two

effects or both [10]. However, today diode reverse breakdown is referred as Zener and breakdown diodes are Zener diodes, even though it is usually avalanche breakdown [6].

Moreover, Zener tunnelling mechanism, in zener diodes, with a breakdown voltage less than 5 V has a negative TC, while avalanche breakdown mechanism in diodes with a breakdown voltage higher than 7 V has a positive TC. In the breakdown voltage range between 5 V and 7 V that corresponds to the transition from Zener tunneling to avalanche breakdown mechanism, TC values are relatively low (i.e. +1.5 to 5 mV/°C). Therefore, diodes with breakdown voltages in this range are appropriate for voltage reference designs [2].

2.1.1.1 Temperature characteristics

The temperature dependence of the forward-biased diode voltage is approximately -2.2 mV/°C which also includes a nonlinear temperature dependence. A detailed analysis of the temperature dependence of the diode voltage will be given in the temperature characteristics of BJT section.

2.1.1.2 Matching performance

Junction diodes in integrated circuit technologies are implemented via various connections of NPN and PNP transistors. Therefore their matching performance is directly related to the matching accuracy of bipolar transistors that is described in the following section.

2.1.2 BJT

The bipolar junction transistor (BJT) is a type of transistor that is formed by the connection of two series back to back *pn* junctions (the base-emitter junction and the base-collector junction). The transistor is named bipolar because current conduction is provided by two kinds of charge carriers (i.e. electrons and holes) [10].

Depending on the biasing condition of the *pn* junctions, bipolar transistors have three different modes of operation. With both junctions forward-biased, a BJT is in saturation mode and facilitates high current conduction from the collector to the emitter (or the other direction in the case of PNP). In cut-off, the biasing conditions are opposite with respect to the saturation case (both junctions reversed biased) and the

transistor is not letting current go through from collector to emitter. The typical current versus voltage ($I-V$) characteristics of a bipolar transistor are shown in Figure 2.2.

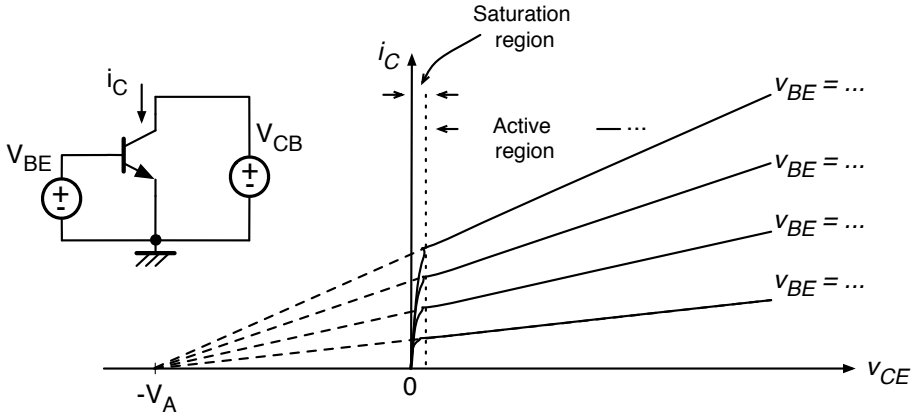

Figure 2.2: Typical I-V characteristics of a BJT.

In the region called forward-active (or active) region, the base-emitter junction is forward biased while the base-collector junction is reverse biased. Bipolar transistors are mostly used in this region of operation and the collector current in this region can be expressed as:

$$i_C = I_S \left[\exp\left(\frac{v_{BE}}{V_T} \right) \right] \tag{2.3}$$

where I_S is a saturation current which is on the order of 10^{-12} to 10^{-15} and is directly proportional to the junction area and V_T is thermal the voltage. The base current, i_B, is also proportional to $\exp\left(\frac{v_{BE}}{V_T}\right)$ and therefore it can be expressed as a fraction of collector current as:

$$i_B = \frac{I_S}{\beta} \left[\exp\left(\frac{v_{BE}}{V_T} \right) \right] = \frac{i_C}{\beta} \tag{2.4}$$

where β is called common-emitter current gain. This parameter is affected by the width of the base region and the relative dopings of the emitter and base regions, so it is constant for a given transistor. Finally, the emitter current, i_E, is equal to the sum of the base and collector current of the transistor:

$$i_E = i_C + i_B \tag{2.5}$$

Alternatively, it can be expressed as a multiplicand of the collector current:

$$i_E = \alpha i_C \tag{2.6}$$

where α is a constant related to β as given in (**2.7**) and close to unity since β is usually in the range from 100 to 200.

$$\alpha = \frac{\beta + 1}{\beta} \tag{2.7}$$

2.1.2.1 Temperature characteristics

The collector current of a bipolar transistor has an exponential relationship to the base-emitter voltage as expressed in **2.3**. The base-emittor voltage can be rewritten as:

$$V_{BE} = V_T \ln\left(\frac{i_C}{I_S}\right) \tag{2.8}$$

The saturation current I_S is related to the device structure, as described in [11]

$$I_S = \frac{qA{n_i}^2\overline{D_n}}{Q_B} \tag{2.9}$$

where q is the magnitude of the electrical charge on the electron, A is the emitter-base junction area (or emitter cross-sectional area), n_i is the intrinsic minority carrier concentration, $\overline{D_n}$ is the electron diffusion constant in the base, Q_B is total base doping per unit area. The quantities that are temperature dependent are

$${n_i}^2 = BT^3 \exp\left(\frac{-V_{g0}}{V_T}\right) \tag{2.10}$$

$$\overline{D_n} = V_T\overline{\mu_n} = CV_T T^{-n} \tag{2.11}$$

where V_{g0} is the band-gap voltage of the silicon extrapolated to 0 K, μ_n is the average mobility for minority carriers in the base, B, C and exponent n are temperature independent constants. Therefore, the saturation current I_S can be explicitly expressed by

$$I_S = DT^{4-n} \exp\left(\frac{-V_{g0}}{V_T}\right) \tag{2.12}$$

where D is a temperature independent constant, $D = kABC/Q_B$, defined by all the constants such as k, A, B, C, and Q_B in the previous equations. For the sake of temperature modeling, the collector current can be expressed as:

$$i_C = ET^x \tag{2.13}$$

where E is another temperature independent constant and x is a number defined by the temperature dependence of the collector current, for instance x is equal to 1 for PTAT. Consequently, the temperature dependence of the base-emitter voltage can be obtained by replacing the saturation and collector currents in **2.8**. However, for the purpose of design, expressing the temperature dependence of V_{BE} as a function of the reference temperature (T_r) is more appropriate. This expression can be derived by solving for the constant V_{BE} relationship at given reference temperature and substituting it back in the V_{BE} equation. The resulting expression for the V_{BE} temperature behaviour is given by [12]

$$V_{BE}(T) = V_{g0} - \left(V_{g0} - V_{BE}(T_r)\right)\frac{T}{T_r} - (\eta - x)\frac{kT}{q}\ln\left(\frac{T}{T_r}\right) \tag{2.14}$$

where V_{g0} is bandgap of silicon extrapolated to 0 K, T is the absolute temperature in K, $V_{BE}(T_r)$ is the voltage across the diode at temperature T_r, η is a process dependent but temperature independent constant and x relates to the order of the temperature dependence of the collector current $(I_C \propto T^x)$.

2.1.2.2 Matching performance

The most important causes of BJT mismatch are variations in the base and collector currents. The variations can be reduced with increasing device (emitter) area. In a matched bipolar transistor pair, the errors are bias point independent; moreover, the collector current mismatch is the dominant error source for collector current and base-emitter voltage matching [13].

For a conventional bandgap circuit, the error that BJT mismatch creates is the deviation in the desired ratio of the saturation current density J_S of transistors. The fractional error in the ratio δ_Q, can be expressed as

$$\delta_Q = \frac{\Delta I_S}{I_S} \tag{2.15}$$

Since bipolar transistors can be matched to a high degree of accuracy (e.g. 0.1-1 %), BJT mismatch has a small effect on the accuracy of the reference voltage. The error due to a mismatch of 1 % is only 3 mV or roughly 0.25 % for a 1.2 V reference [7]. From the layout point of view, careful layout techniques such as the use of dummy devices, avoiding metal coverage, and maintaining identical environments around devices have to be adopted to not to degrade the high intrinsic matching of bipolar devices [14].

2.1.3 MOSFET

A metal-oxide-semiconductor field-effect transistor (MOSFET) consists of two highly doped semiconductor regions (source and drain) , which are isolated from the substrate by reverse-biased *pn* junctions. A metal or polysilicon gate covers the region between source and drain. The gate is separated from the semiconductor by the gate oxide.

A MOSFET is a voltage controlled majority carrier device. The movement of majority carriers in a MOSFET is controlled by the voltage applied on the control electrode Gate (G) which is insulated by a thin oxide layer from the bulk semiconductor body. The electric field produced by the gate voltage modulates the conductivity of the semiconductor material in the region between the main current carrying terminals called Drain (D) and Source (S).

The MOS transistor has three different operation regions, depending on the voltages at its terminals: weak inversion where the gate-source voltage is lower than the threshold voltage $(V_{GS} < V_{TH})$, saturation where the drain current is almost totally controlled by the gate voltage and linear (or triode) region where the drain-source voltage is effective besides the gate voltage on the control of the drain current. The transition between the saturation and linear regions is determined by the condition $(V_{DS} = V_{GS} - V_{TH})$. The typical current versus voltage $(I-V)$ characteristics of a MOSFET are shown in Figure 2.3.

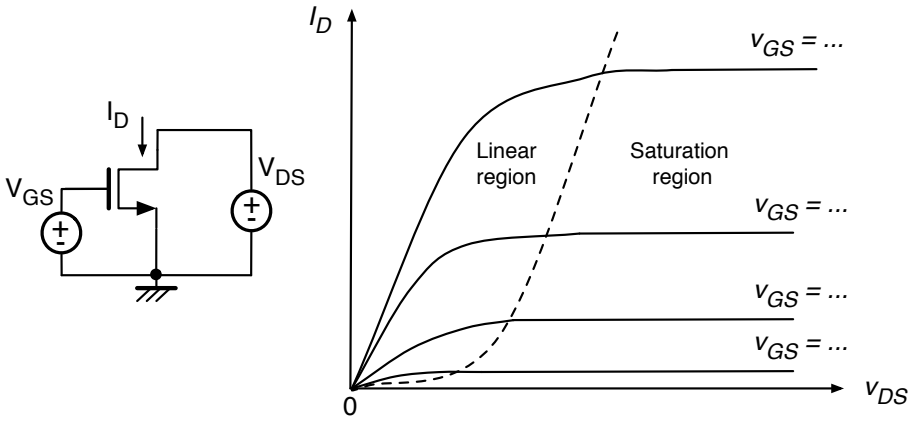

Figure 2.3: Typical I-V characteristics of a nMOS.

In the weak inversion (or sub-threshold) region, the effect of thermal energy on the Boltzmann distribution of electron energies allows some of the more energetic electrons at the source to enter the channel and flow to the drain which results in a sub-threshold current. This current depends exponentially from the gate-source voltage and can be approximated by [11]

$$I_C = I_{D0}\left[\exp\left(\frac{V_{GS}-V_{th}}{nV_T}\right)\right] \tag{2.16}$$

where I_{D0} is the current at $V_{GS} = V_{th}$, and n is the slope factor $(n = 1 + (C_D/C_{ox}))$ which takes values between 1.5 and 3 for typical CMOS technologies. A significant result is that the behaviour of a MOS transistor in weak inversion region is similar to behaviour of a bipolar transistor. While working in the weak inversion region, the MOS transistors deliver the highest possible transconductance-to-current ratio (see in **2.17**), which is almost equal to the one of a bipolar transistor [15].

$$\frac{g_m}{I_D} = \frac{1}{(nV_T)} \tag{2.17}$$

When $(V_{GS} > V_{TH})$, an inversion layer (the channel) is created, allowing current to flow between the drain and the source. This current can be expressed as

$$I_D = \mu C_{ox}\frac{W}{L}\left[(V_{GS}-V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{2.18}$$

where μ is the carrier effective mobility, C_{ox} is the gate oxide capacitance per unit area, W and L are the gate width and length of the transistor, respectively. In the triode

region, the drain current is linearly proportional to the overdrive voltage $(V_{GS} - V_{th})$, which is the dominant control voltage if $V_{DS} \ll (V_{GS} - V_{th})$. In these conditions, the MOS transistor can be used as a voltage controlled resistor. Moreover, **2.18** represents a parabola on the $I_D - V_{DS}$ plane whose maximum is achieved in the condition $V_{GS} - V_{th} = V_{DS}$, in which the charge in the inverted layer at the drain end goes to zero and any larger V_{DS} results in unrealistic situations. Therefore, this condition defines the range in which **2.18** is valid and establishes the limits of the triode region.

When the gate voltage is still higher than the threshold voltage and the V_{DS} voltage exceeds the aforementioned condition, $V_{GS} - V_{th}$, transistor leaves the linear region and enters the saturation region. The drain current in this region varies with the square of the overdrive voltage and is given by

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2\left[1 + \lambda V_{DS}\right] \tag{2.19}$$

where λ is the channel length modulation parameter which defines the V_{DS} dependency of the drain current due to channel length modulation in this region. The slope of the $I_D - V_{DS}$ curves in Figure 2.3 is λ.

2.1.3.1 Temperature characteristics

The carrier mobility μ and the threshold voltage are the two main factors that determine the MOS transistor temperature behaviour. The temperature dependence of the mobility can be expressed as [16]

$$\mu\left(T\right) = \mu\left(T\right)\left(T/T_0\right)^{\alpha_\mu} \tag{2.20}$$

where T_0 is the reference temperature and the parameter α_μ can be considered independent from the temperature and its values is normally assumed equal to -1.5, which is valid when the scattering mechanism is dominant [17]. Therefore the temperature coefficient of the carrier mobility can be approximated as

$$TC_\mu = \frac{1}{\mu}\frac{\delta\mu}{\delta T} = \alpha_\mu\frac{1}{T} \cong \frac{-1.5}{T} \tag{2.21}$$

The threshold voltage of a MOS transistor is given by

$$V_{th} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \tag{2.22}$$

where V_{FB} is the flat band voltage, ϕ_F is the Fermi potential of the substrate and γ is the body effect parameter. Even these parameters have different temperature dependencies [18], the threshold voltage of a MOS transistor is commonly modeled to decrease linearly with the temperature increase [19]

$$V_{TH}(T) = V_{TH}(T) + \alpha_{V_{TH}}(T - T_0) \tag{2.23}$$

where $\alpha_{V_{TH}}$ is assumed as temperature independent coefficient and takes values from -1 mV/°C to -4 mV/°C [16].

2.1.3.2 Matching performance

The dominant sources of drain current and gate-source voltage mismatch for MOS transistors are threshold voltage differences ΔV_{th} and current factor differences $\Delta\beta$ ($\beta = \mu C_{ox} W/L$) and their matching scales with the device area. However, in contrast to the BJT case, MOS transistor matching is bias dependent; for typical bias points (i.e. $(V_{GS} - V_{TH}) < 0.65\ V$) the relative effect of V_{TH} mismatch is dominant [13].

For a conventional bandgap circuit, the error that MOS mismatch creates is due to the deviation in the desired ratio of the current mirrors. The mismatch between the mirrored currents δ_M can be expressed as

$$\delta_M = \frac{\Delta\beta}{\beta} - \frac{2\Delta V_{TH}}{(V_{GS} - V_{TH})} \tag{2.24}$$

A 3-σ mismatch of MOS transistors is on the order of 2% and generates an approximate error of 24 mV or 2% in a 1.2 V reference at room temperature which is relatively high with respect to error caused by BJT mismatch. Matching performance can be improved by increasing the active area and the overdrive voltage $(V_{GS} - V_{th})$ of the MOS transistors since $\Delta\beta$ and V_{th} are inversely proportional to the active area of the device [20]. However, increasing the transistor area results in higher parasitic capacitances at the mirror nodes thus causing a reduction in the bandwidth and degrading the capability of the reference to respond to line and load fluctuations. In other words, this worsens the AC performance [7]. On the other hand, using large

overdrives to achieve high matching performance requires to high voltage headroom which is difficult to obtain or is conflict with the shrinking supply voltages of modern CMOS processes. As a result, MOS mismatch is the most critical process-induced error source in bandgap reference circuits.

From the layout point of view, although device position and orientation have not significant effect on random mismatch errors, it can cause systematic differences. Therefore, utilizing dummy devices, using common-centroid and inter-digitation techniques and maintaining symmetry (also in the sense of metal connections) is important to prevent possible systematic errors [21].

2.1.4 Resistor

Integrated resistors are made of thin strips of resistive layer, and they are connected to metal terminals by two ohmic contacts, as shown in Figure 2.4 [22]. The total resistance can be calculated by

$$R = 2R_{cont} + \frac{L}{W}R_{\square} \tag{2.25}$$

where R_{cont} is the resistance of metal connection contacts, $R_{\square}$ is the sheet resistance of the layer used to form the resistance and L/W is the number of squares. Most commonly used integrated resistors are formed by polysilicon (first or second poly) or diffusion (p+, n+ or well) layers. Moreover, polysilicon resistors exhibit higher sheet resistance due to the grain-boundary regions [23].

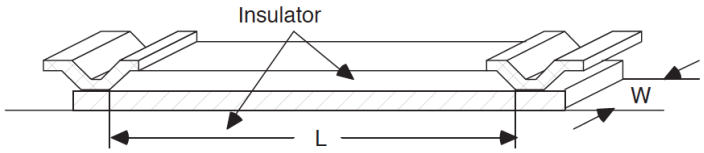

Figure 2.4: Typical integrated resistor.

The body of the resistance is insulated from its surroundings by an oxide layer or by a reverse biased junction. For diffusion resistors, this insulation is ensured by reverse biased junctions which cause a capacitive coupling between the resistor itself and the substrate (or well). Therefore, it is important to deal with these parasitic capacitances by appropriate shielding strategies to prevent noise coupling from the substrate, even if it has not significant effect on the frequency behaviour. On the other hand, for

polysilicon resistors insulation is ensured mostly by an oxide layer and these resistors are not in the immediate proximity with the substrate. For these kind of resistors, the coupling is far weaker with respect to the diffusion ones and more effective shielding can be employed. As a result, diffusion resistors are mostly used in electrostatic discharge protection circuits while doped polysilicon resistors are commonly used as a precise analog resistor element for a wide range of applications [23]. The stability of resistors directly affects the accuracy of the reference voltage; therefore, they have an important role on performance of particularly high speed mixed-signal IC applications that require high precision and temperature stability.

2.1.4.1 Temperature characteristics

The temperature coefficient of a resistor (TC_R) is the parameter that is used to define the temperature dependent characteristic of a resistor and can be expressed as

$$TC_R = \frac{1}{R}\frac{\delta R}{\delta T} \tag{2.26}$$

Even though, (TC_R) values of integrated diffusion and polysilicon resistors are highly dependent on technology and given as a process parameter, in general diffused resistors have positive (TC_R) values while polysilicon resistors exhibit negative ones. Moreover, diffusion resistors (TC_R) are far bigger when compared to polysilicon ones [22].

2.1.4.2 Matching performance

Integrated resistors can be matched to a high degree of accuracy through appropriate layout techniques such as using dummy devices at the edges of resistor arrays that can reduce mismatch due to etching errors, using common-centroid layout and inter-digitation that spatially average geometry and dopant fluctuations over resistor arrays [21]. Moreover, again increasing device (resistor) area also increases the matching performance through averaging fluctuations in geometry. After careful layout, resistor mismatch is typically in the range of 1% to 0.1% and 0.5% of resistor mismatch generates an error of about 3 mV or 0.25% for a conventional 1.2 V reference.

Process variations lead to a large deviation in resistor values often as large as 20%. These deviations can be reduced by choosing appropriate kind of resistor (i.e.

polysilicon resistors typically exhibit a smaller variation of resistance with voltage and temperature, than n-well resistors). However, resistor variations due to deviations in sheet resistance from one die to another cannot be controlled. Only a proper trimming procedure after fabrication can reduce the effect of those variations.

2.2 Literature Review on Bandgap Reference Circuits

In the previous chapter, different types of voltage references have been mentioned with respect to their design origin. The bandgap voltage reference (BGR), which was firstly proposed by Widlar [24] and was further developed by Kuijk [25] and Brokaw [26], is the most popular circuit topology utilized to implement voltage references.

The basic operation of BGR circuits relies on the summation of a PTAT voltage with a CTAT voltage.This results in the cancelation of linear temperature dependent terms so that a first-order temperature compensation is achieved. The CTAT voltage is obtained through the temperature dependence of a forward biased diode voltage that corresponds, in general, to a base-emitter voltage (V_{BE}) of a bipolar transistor and the PTAT voltage is obtained through the thermal voltage V_T that is extracted from the difference of two forward-biased diode voltages.

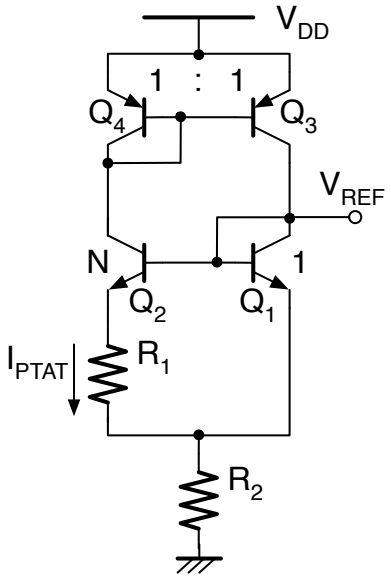

Figure 2.5: Classic Brokaw bandgap reference circuit.

The commonly known Brokaw cell is shown in Figure 2.5. The current mirror (basic current mirror used for the sake of simplicity) forces the same current to both bipolar transistors Q_1 and Q_2, which have different emitter areas and hence different

base-emitter voltages. The difference of the base-emitter voltages of transistors Q_1 and Q_2, when applied to resistor R_1, produces a PTAT current, I_{PTAT}, and, consequently, a PTAT voltage, V_{PTAT}, across resistor R_2:

$$I_{PTAT} = I_{C1} = I_{C2} = \frac{V_T}{R_1} \ln\left(N\frac{I_{C1}}{I_{C2}}\right) = \frac{V_T}{R_1} \ln(N) \tag{2.27}$$

$$V_{PTAT} = 2I_{PTAT}R_2 = 2V_T \ln(N) \frac{R_2}{R_1} \tag{2.28}$$

This voltage, having a positive temperature coefficient, is then added to the base-emitter voltage of Q_1, which has a negative temperature coefficient, to generate the temperature stable reference voltage, V_{REF}:

$$V_{REF} = V_{BE1} + 2\frac{R_2}{R_1} V_T \ln(N) \tag{2.29}$$

As seen from Figure 2.5, bipolar transistors are used in the classic Brokaw cell, in which all device terminals are floating. For this reason, the schematic, as it is, cannot be implemented directly in a standard CMOS technology. Figure 2.6 shows the simple implementation of bandgap reference concept in CMOS technology with parasitic substrate PNP transistors [11]. Current mirrors formed by M_1, M_2 and M_5 enforce branch currents equal to a PTAT current which is generated by Q_1, Q_2 and R_1 when the voltages on node A and B are imposed to be equal by a voltage-clamping circuit composed of M_3 and M_4. Thus, V_{REF} is given by

$$V_{REF} = V_{EB3} + \left(\frac{R_2}{R_1}\right) V_T \ln(N) \tag{2.30}$$

As a result, the achieved V_{REF} is in the form of

$$V_{REF} = V_{BE} + MV_T \tag{2.31}$$

where M is determined by the circuit parameters such as (R_2/R_1) and N. For first-order approximation, the temperature dependence of the base-emitter voltage **2.14** can be rewritten using the linearization for values of T near T_r, $\ln(T_r/T) \simeq (T_r - T)/T$ to neglect higher-order nonlinear components.

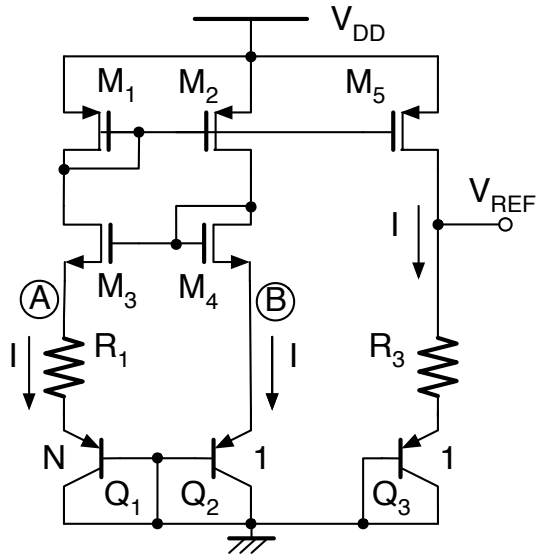

Figure 2.6: Simple CMOS implementation of bandgap reference.

$$V_{BE} \approx \left[V_{g0} + (\eta - x)V_{T_r}\right] - \left[V_{g0} - V_{BE}(T_r) + (\eta - x)V_{T_r}\right]\frac{T}{T_r} \tag{2.32}$$

where the value of the constant x can be replaced by "1" since the collector current is PTAT. In order to have a zero-TC for the reference voltage at a reference temperature, its first derivative must be equal to zero,

$$\frac{\delta V_{REF}}{\delta T} = -\left[\frac{V_{g0} - V_{BE}(T_r) + (\eta - 1)V_{T_r}}{T_r}\right] + \left[\frac{MV_T(T_r)}{T_r}\right] \tag{2.33}$$

Consequently, the value of M to have zero-TC at a given reference temperature is obtained as

$$M = \frac{V_{g0} - V_{BE}(T_r)}{V_{T_r}} + (\eta - 1) \tag{2.34}$$

Therefore, a V_{REF} with low temperature coefficient can be easily obtained by optimizing temperature-independent circuit parameters (R_2/R_1) and N. As a result, a reference voltage for zero temperature coefficient has a value around 1.205 V and is intrinsically-defined: it is the value of the energy bandgap of the silicon.

2.2.1 Higher-order bandgap references

The accuracy level that typical first-order compensated bandgap references can achieve is limited with the nonlinear (logarithmic) component of the base-emitter

(diode) voltage temperature behaviour (**2.14**) and it is not adequate for many high performance systems [2]. Therefore, several high-order compensation techniques such as quadratic temperature compensation [27], exponential temperature compensation [28], piecewise-linear curvature correction [29], temperature-dependent resistor ratio compensation [30, 31], and matched or exact nonlinear compensation [32–35] have been reported to further reduce the reference voltage output temperature coefficient (TC) to the range 1-10 ppm/°C by compensating for higher-order temperature dependency.

In the temperature-dependent resistor ratio technique, temperature coefficients of different resistors in the process are used to compensate for nonlinear terms in a first-order bandgap scheme. Figure 2.7 shows one of the implementations of this method reported in [31].

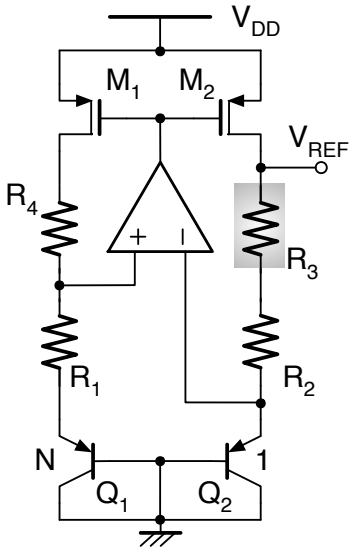

Figure 2.7: Curvature-corrected bandgap reference based on temperature-dependent resistor ratio proposed by Leung *et al* [31].

All the resistors except R_3 are realized using the same material, while R_3 is made of high-resistive polysilicon which has a negative TC. The reference voltage can be written as:

$$V_{REF} = V_{EB2} + \left(\frac{R_2}{R_1}\right) V_T \ln(N) + \left(\frac{R_3}{R_1}\right) V_T \ln(N) \qquad (\mathbf{2.35})$$

where R_3/R_1 is a temperature-dependent ratio. Therefore, the nonlinear temperature-dependent term in V_{EB} $(T \ln T)$ can be compensated for depending on

the relative temperature coefficients of R_1 and R_3. Moreover, R_4 is used to provide good matching between V_{DS} voltage of M_1 and M_2 by setting it equal to $(R_2 + R_3)$ at room temperature. Notice that, with this implementation the achieved TC is 5 times improved with respect to the first-order compensated one [31].

The method so called matched or exact curvature correction method, is based on generating a nonlinear difference current which is obtained through the V_{BE} difference of bipolar transistors with different temperature-dependent collector currents. Note that, in the temperature dependence equation of V_{BE} **2.14**, x is a variable related to the temperature dependence of the collector current, i.e. it takes the value "1" for PTAT collector current and "0" for first order compensated current. The implementation of the matched curvature correction method proposed in [32] is shown in Figure 2.8.

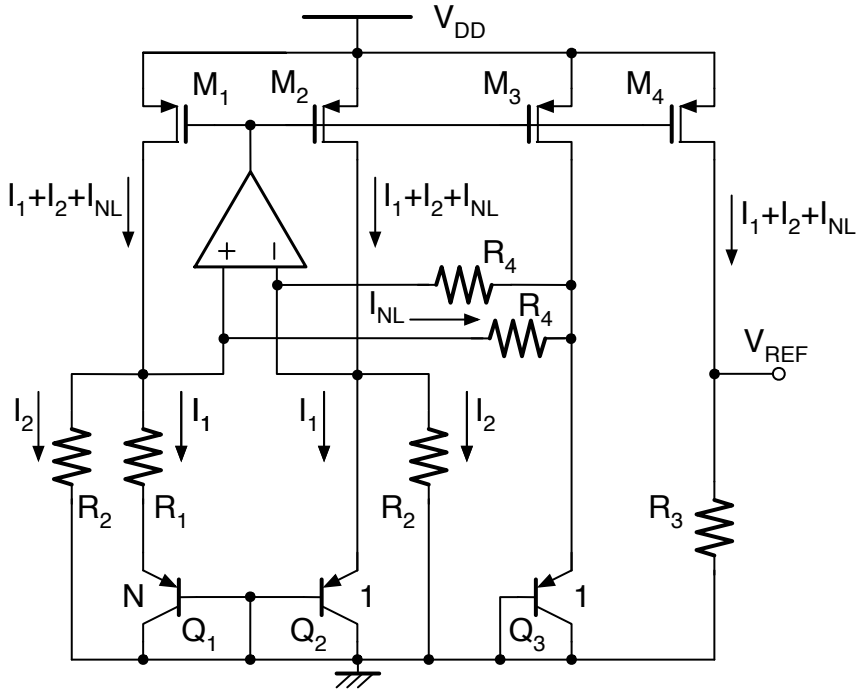

Figure 2.8: Curvature-corrected bandgap reference proposed by Malcovati *et al* [32].

In this circuit, Q_2 is biased by a PTAT current ($x = 1$ in (**2.14**)), while Q_3 is biased by a first-order temperature-independent current ($x = 0$ in (**2.14**)). The base-emitter voltage difference of Q_2 and Q_3 is dropped on R_4 to obtain the nonlinear current I_{NL}, is given by

$$I_{NL} = \frac{(V_{EB2} - V_{EB3})}{R_4} = -\frac{1}{R_4} V_T \ln\left(\frac{T}{T_r}\right) \qquad \textbf{(2.36)}$$

Therefore, since the reference voltage V_{REF} is obtained on the resistor R_3 driven with the output current $(I_1 + I_2 + I_{NL})$, V_{REF} is given by

$$V_{REF} = \left(\frac{R_3}{R_2}\right) + \left[V_{EB2} + \left(\frac{R_2}{R_1}\right) V_T \ln(N) - \left(\frac{R_2}{R_4}\right) V_T \ln\left(\frac{T}{T_r}\right)\right] \tag{2.37}$$

When the resistor ratio $R_2/R_4 = \eta - 1$, the nonlinear term in V_{EB2} is cancelled. However, resistors temperature dependence affects the PTAT and temperature-independent currents generation, thus introducing inaccuracies. In addition, another source of error in this architecture is due to the mismatch of current mirrors. Therefore, V_{REF} can be set to about one V_{EB} in order to match the V_{DS} of M_4 with the one of $M_1 - M_3$.

Another implementation of this technique proposed in [35] is shown in Figure **??**. In the circuit, Q_1 is driven by a PTAT current, while Q_2 is driven by a first-order temperature compensated current (summation of the PTAT current with the CTAT current generated on R_1). Finally V_{BE} voltages of these two BJTs are translated to currents by resistors in order to take the difference of these currents. In the figure, the PTAT current generation is not shown for simplicity. The output reference voltage of the circuit is given by

$$V_{REF} = \left(\frac{V_{BE1}}{R_1} + \frac{V_{BE2}}{R_2}\right)(R_3 + R_4) + I_{PTAT} R_4 \tag{2.38}$$

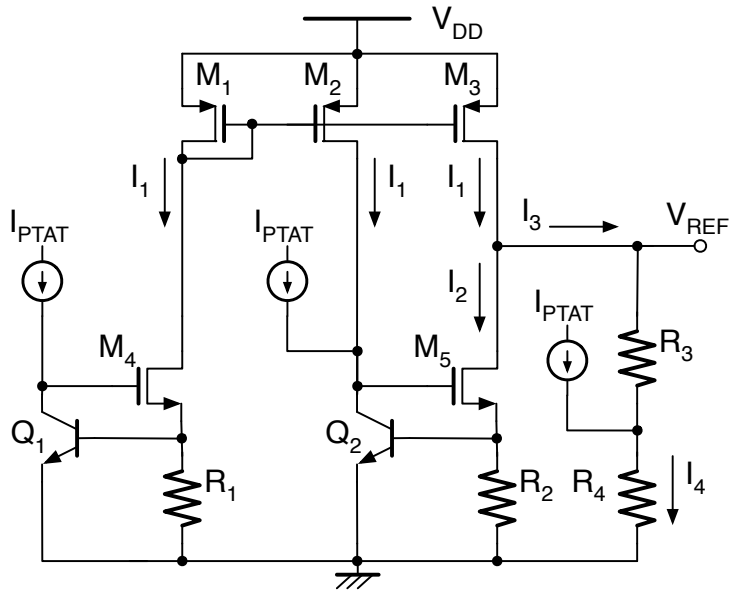

Figure 2.9: Exact curvature-corrected bandgap reference proposed by Mora *et al* [35].

By substituting for V_{BE} terms in this equation, proper design relationships to cancel the linear and nonlinear temperature dependent terms can be obtained. Therefore, applying these conditions result in

$$V_{REF} = V_{g0}\,(R_3 + R_4)\left(\frac{1}{R_1} - \frac{1}{R_2}\right) \tag{2.39}$$

2.2.2 Low-voltage / Sub-1V bandgap references

As pointed out earlier, technology scaling and demand for low power applications lead to lower supply voltage, which makes traditional BGRs no more suitable. Indeed, when the temperature effects have been canceled, as previously mentioned the value of the reference voltage for traditional BGRs is approximately equal to the extrapolated bandgap voltage of silicon at 0 K, 1.205 V. This problem can be solved by using resistive subdivision methods that allow scaling down the reference voltage and enabling sub-1V operation [32, 36, 37]. These implementations are also called current mode BGRs since they generate a temperature-independent current, which is then mirrored to an output resistor to create a sub-1V output voltage.

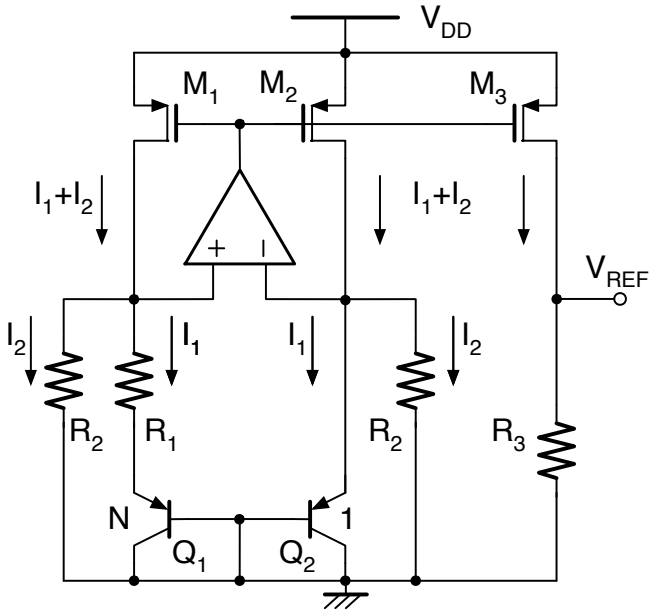

Figure 2.10: A CMOS bandgap reference with sub-1V operation proposed by Banba *et al* [36].

Figure 2.10 shows the circuit presented in [36]. The reference voltage is generated by the summation of the two currents I_1, which is a PTAT current formed by Q_1, Q_2 and R_1, and I_2, a current due to V_{EB2} and R_2. Hence, V_{REF} is given by

$$V_{REF} = \left(\frac{R_3}{R_2}\right)\left[V_{EB2} + \left(\frac{R_2}{R_1}\right) V_T \ln(N)\right] \tag{2.40}$$

The temperature compensation is achieved by selecting an appropriate R_2/R_1 ratio and N. Moreover, the reference voltage can be scaled down to be less then 1.205 V by setting the resistor ratio R_3/R_2, so that the value of V_{REF} can be adjusted for different applications.

The theoretical minimum supply voltage for this circuit architecture is $V_{DD(min)} = V_{EB} + V_{DSsat,P}$. However, the supply voltages of most bandgap references (that use an opamp) is, in fact, limited by the input common mode range of the opamp, which is required to produce a PTAT voltage or current. Several techniques have been proposed to overcome this limitation, such as using native (low-threshold) devices [36], using PMOS input stage with a potential divider [37] or implementing an opamp using a BiCMOS technology [32].

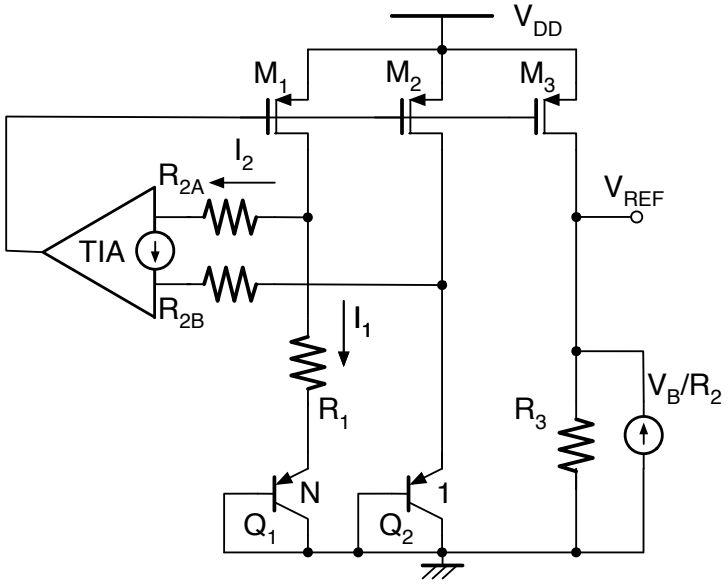

Figure 2.11: Bandgap voltage reference using transimpedance amplifier proposed by Jiang *et al* [38].

Another method to get rid of the input stage limitation of the opamp consists of using a transimpedance amplifier (TIA), as shown in Figure 2.11, [38]. The basic principle of this bandgap reference is to remove the input differential stage of the opamp and to replace it with a TIA using resistors. The TIA has a large impedance gain and a very low input impedance with a fixed potential V_B at both inputs which is lower then V_{EB}. Hence, the current I_2 is given by $(V_{EB} - V_B)/R_2$ where I_1 is a PTAT current given by

$V_T \ln(N)/R_1$. To eliminate the term with V_B, an additional current I_3 proportional to V_B and given by V_B/R_2 is introduced to the output node. As a result, a scalable reference voltage V_{REF} is achieved:

$$V_{REF} = \left(\frac{R_3}{R_2}\right)\left[V_{EB2} + \left(\frac{R_2}{R_1}\right) V_T \ln(N)\right] \tag{2.41}$$

In addition to the current-mode techniques, the reverse bandgap voltage principle (RBVP), which is based on adding a V_T to an attenuated V_{BE} instead of adding a V_{BE} to a scaled V_T, is used for sub-1V operation [39] as shown in Figure 2.12. The transistor Q_1 and resistors R_1, R_2 form a modified V_{BE} multiplier so that voltages V_1 and V_{REF} can be expressed as

$$V_1 = \left(\frac{R_2}{R_1} + 1\right) V_{BE1} + I_{B1} R_2 \tag{2.42}$$

$$V_{REF} = V_1 - V_{BE2} - (I_{B2} R_4) \tag{2.43}$$

By selecting the R_2 and R_4, such that $I_{B1}R_2 = I_{B2}R_4$, the reference voltage is obtained as

$$V_{REF} = \left(\frac{R_2}{R_1} + 1\right) V_{BE1} + V_T \ln(N) \tag{2.44}$$

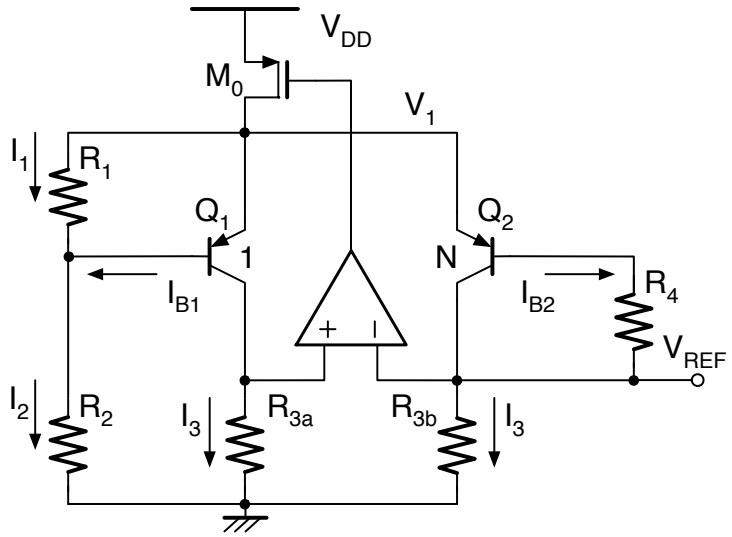

Figure 2.12: Reverse bandgap voltage reference circuit proposed by Sanborn *et al* [39].

The main advantage of this technique over the current-mode counterparts is the low output noise, which is dominated by high flat-band and flicker $(1/f)$ noise of MOS current mirrors in current-mode references.

The design techniques that have been mentioned are based on the generation of a fraction of material bandgap at the expense of extra area required for resistors. The third method for low-voltage BGR design uses dynamic threshold MOS (DTMOS) devices [40]. For the MOS diodes based on DTMOS transistors in which gate and back-gate (bulk) are interconnected, the applied gate voltage would result in an increased electrostatic filed across the junction, hence the effective bandgap voltage becomes

$$V_{gap,\,effective} = V_{gap,0} - \Phi_{b1} \tag{2.45}$$

where Φ_{b1} is the capacitive subdivided version of the built-in voltage over the gate oxide and over the silicon. This effective bandgap extrapolated to 0 K is about 0.6V and it is temperature dependent. Figure 2.13 shows the circuit described in [40], where M_1 and M_2 are DTMOS transistors used in the input stage of the opamp, M_{12} and M_{13} are DTMOS based diodes. As a result, the bandgap reference circuit generates an output voltage of 0.65 V under a minimum supply voltage of 0.85 V. The reported sub-1V voltage references can achieve a TC in the range of 7-15 ppm/°C.

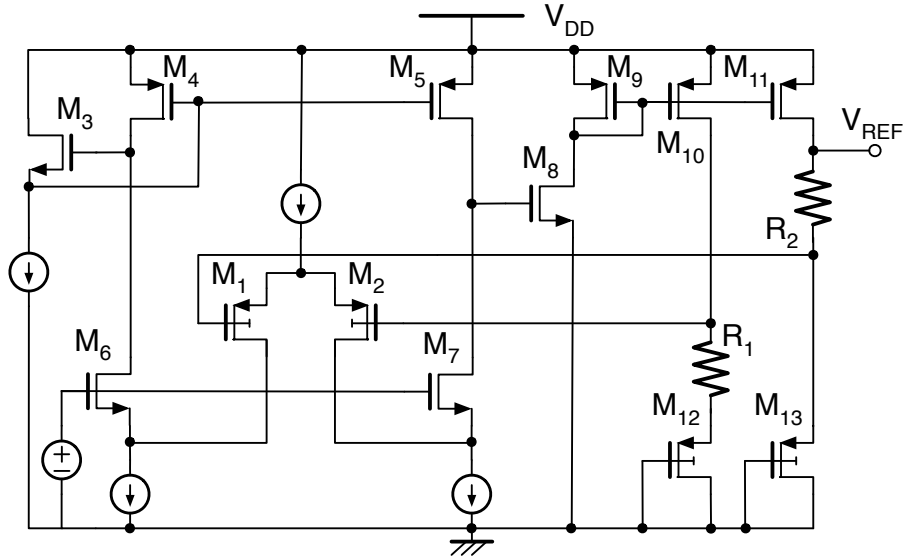

Figure 2.13: DTMOS based bandgap voltage reference circuit proposed by Annema [40].

2.2.3 CMOS-only bandgap references

If a standard CMOS technology is utilized, parasitic substrate BJTs formed in p-well (or n-well) are commonly used to implement BGRs [27, 37]. There are also CMOS-only voltage references. The most popular implementations use MOSFET transistors operating in the subthreshold region instead of BJTs [41, 42]. The basic operation principle of the circuit relies on the negative temperature dependance of the MOS threshold voltage (or gate-source voltage biased with a constant drain current) and gate-source voltage that can be used instead of the base-emitter voltage.

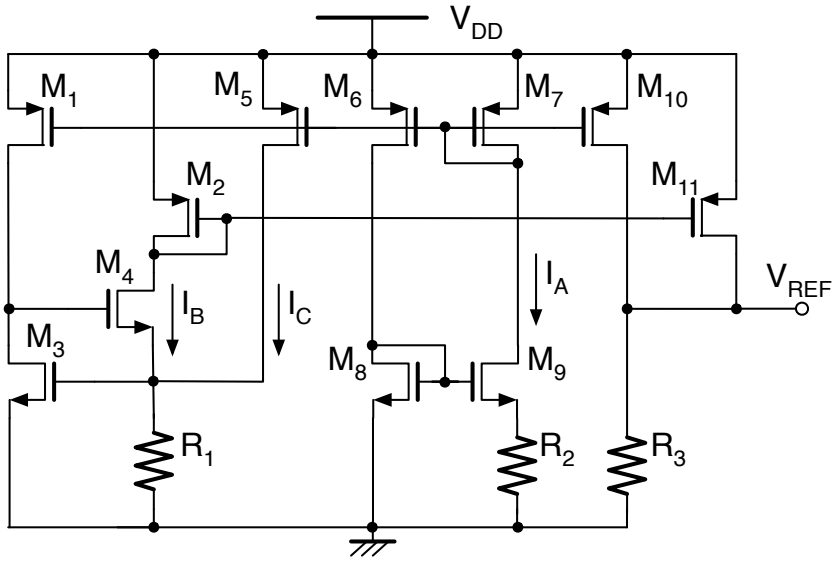

Figure 2.14: Subthreshold based CMOS-only bandgap voltage reference circuit proposed by Huang *et al* [42].

The circuit presented in [42] is shown in Figure 2.14. In this circuit, transistors M_8 and M_9 are operating in the subthreshold region in order to generate a PTAT current I_A on resistor R_2:

$$I_A = \frac{nV_T}{R_2} \ln\left(\frac{P_9}{P_8}\right) \tag{2.46}$$

where n is the slope factor (non-ideal) of a MOS in subthreshold region and P_8 and P_9 are the aspect ratios of the transistors M_8 and M_9, respectively. This current is used to bias M_3, to generate V_{GS3} and to produce the CTAT current I_B due to M_3 operating in the subthreshold region as well. The drain current of M_5 (I_C) is an N times mirrored version of I_A. Finally, through M_{10} and M_{11}, I_A and I_B are mirrored to the output resistance R_3 thus generating the reference voltage V_{REF} which can be expressed as

$$V_{REF} = \left[\frac{P_{10}}{P_7} I_A + \frac{P_{11}}{P_2}\left(\frac{V_{GS3}}{R_1} - N I_A\right)\right] R_3 \qquad (\mathbf{2.47})$$

where $P = \left(W_{eff}/L_{eff}\right)$ is the transistor aspect ratio. If the current values are replaced in **2.47**, the reference voltage can be expressed in the following form

$$V_{REF} = \alpha V_{GS3} + \beta V_T \qquad (\mathbf{2.48})$$

where $\alpha = (P_{11}R_3/P_2R_1)$ and $\beta = [(P_{10}/P_7) - N(P_{11}/P_2)](R_3/R_2)\, n \ln(P_9/P_8)$.

Another CMOS-only voltage reference implementation is based on the weighted gate-source voltage difference between an NMOS and a PMOS transistor. This implementation makes use of the different temperature dependencies of the threshold voltages of the two devices [43, 44]. Figure 2.15 shows the simple circuit, presented in [43], that uses this technique and obtains V_{REF} basically by subtracting from $|V_{THp}|$ a scaled version of V_{THn}.

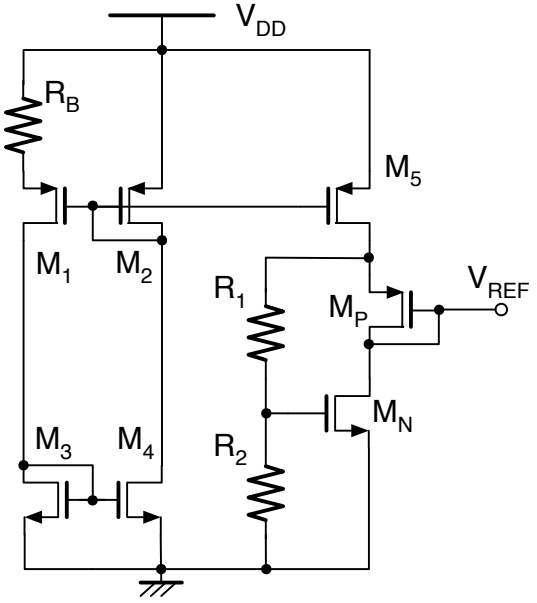

Figure 2.15: CMOS-only bandgap voltage reference based on weighted ΔV_{GS} proposed by Leung *et al* [43].

Transistors M_1-M_4 provide a current which is mirrored to the reference core through M_5. The core reference circuitry is formed by M_N, M_P, R_1, and R_2. Notice that the principle of the operation of the circuit is based on all transistors operating in the saturation region. From inspection of the circuit, the reference voltage is given by

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right) V_{GSn} - |V_{GSp}| \tag{2.49}$$

The circuit can be optimized by choosing an adequate resistance ratio R_1/R_2 in order to compensate for the temperature dependence of the threshold voltage. In addition, the aspect ratios of transistors M_N and M_P are key design parameters to compensate for the mobility temperature dependence at the reference temperature. Note that, the value of the obtained reference voltage V_{REF} may vary since it depends on the process parameters.

In conclusion, CMOS-only references that use subthreshold MOS operation exhibit very low power consumption. However, the major drawback of these topologies is the large output voltage spread at process corners. This is because at different process corners, the threshold voltage of a MOS transistor is not related to any specific physical constant unlike the V_{BE} of BJTs which is converging to a unique voltage, i.e. to the bandgap voltage of the silicon extrapolated to 0 K. In the literature, it is reported that the temperature coefficient of a CMOS-only voltage reference can be reduced down to the 10 ppm/°C range.

2.2.4 Switched-capacitor bandgap references

If a continuous reference output is not required, as in the case of data converter applications, switched-capacitor (SC) based BGRs provide a good solution. SC based techniques are popular because they eliminate the need of using large resistors and can reduce the effect of the amplifier offset [27, 45–47]. Moreover, these structures are suitable for fully differential operation that is beneficial for reducing the effects of the power supply noise and substrate coupling [48].

Figure 2.16 shows an implementation of a bandgap reference circuit with a SC network in conduction with a single bipolar transistor [45]. As seen in the figure, two current sources drive the transistor to bias it to a given level during a precharge phase and to a second, higher level during the reference voltage phase. During the precharge phase, switch S_1 is on and switch S_2 is off. Since the opamp is operating in a unity gain configuration, the voltage across the first capacitor is equal to $(-V_{BE1})$. Then, by turning switch S_1 off and S_2 on, the circuit works in the so called reference voltage phase. The transistor is driven by the sum of the two currents I_1 and I_2. Consequently,

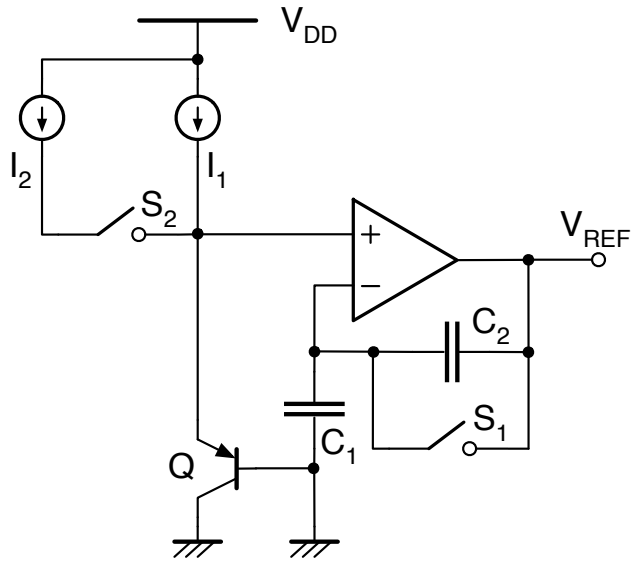

Figure 2.16: Switched-capacitor voltage reference with a single BJT proposed by Gilbert *et al* [45].

V_{BE2} is produced, thus forcing the voltage on C_1 to be equal to $-V_{BE2}$. Therefore, the resulting V_{REF} is given by

$$V_{REF} = V_{BE2} + \frac{C_2}{C_3}(V_{BE2} - V_{BE1}) \tag{2.50}$$

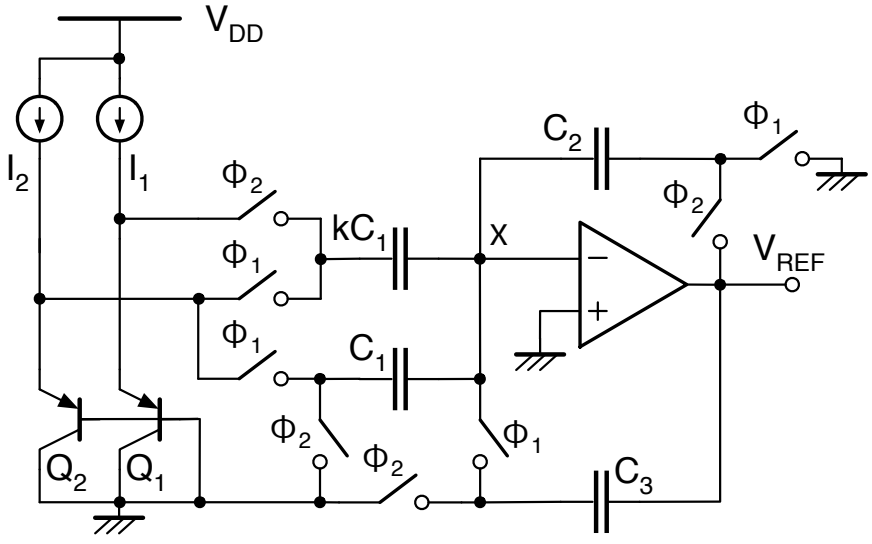

Figure 2.17: Switched-capacitor voltage reference [49].

Figure 2.17 shows another implementation of a reference voltage designed with SC-based technique [49], in which the bipolar transistors are used to generate both temperature coefficients at the expense of large silicon area. When the charge transfer

equations are written in both phases ($\phi_1 = 1, \phi_2 = 0$ and $\phi_1 = 1, \phi_2 = 0$) and combined V_{REF} is given by

$$V_{REF} = \frac{C_1}{C_2 - C_3}\left[V_{BE2} + kV_T \ln\left(\frac{I_2}{I_1}\right)\right] \tag{2.51}$$

A CMOS-only and sub-1V realization of a SC voltage reference is shown in Figure 2.18. The core circuit inputs V_{GS1} and V_{GS2} to the operational transconductance amplifier (OTA) during $\phi_1 = 1$ and $\phi_2 = 1$, respectively, where ϕ_1 and ϕ_2 are non overlapping control signals. In the first phase ($\phi_1 = 0$ and $\phi_2 = 1$), the current flowing through transistor M_{11} is MI_B and correspondingly the gate-source voltage V_{GS2} is stored on the capacitors C_1 and C_2. In the second phase ($\phi_1 = 0$ and $\phi_2 = 1$), the current flowing through that transistor is equal to I_B and the corresponding gate-source voltage V_{GS1} is connected to C_1 while C_2 is grounded and C_3 is put into the negative feedback loop. Since the reference voltage appears in the second phase, the circuit uses a sample and hold to store the reference voltage. Writing the charge conservation equations, V_{REF} can be derived as

$$V_{REF} = \frac{C_1}{C_3}\left[\left(1 + \frac{C_2}{C_1}\right)V_{GS2} - V_{GS1}\right] \tag{2.52}$$

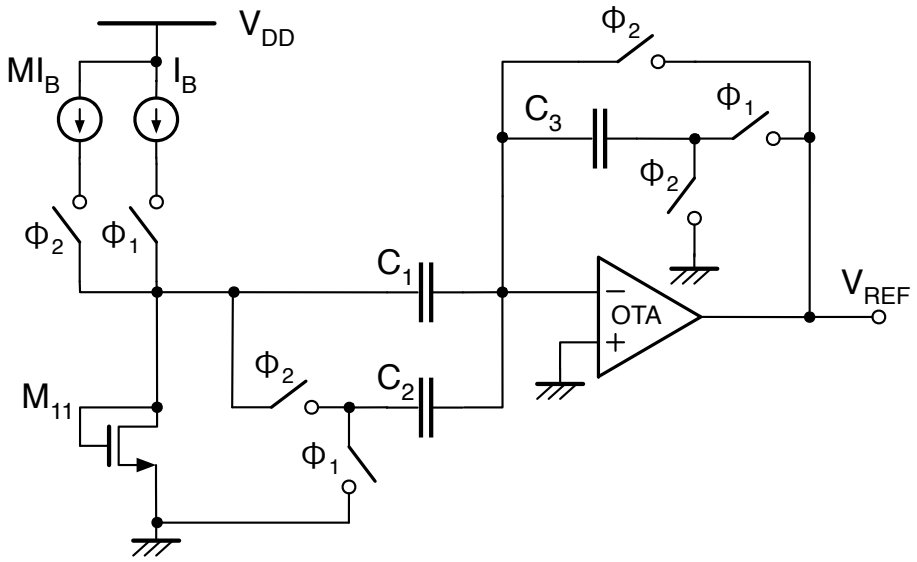

Figure 2.18: CMOS-only switched-capacitor based voltage reference proposed by Huang *et al* [46].

In general, the threshold voltage has negative temperature coefficient that implies that the biasing current I_B has to be proportional to the square of the absolute temperature to

compensate for the temperature coefficient. As a result, zero temperature coefficients can be achieved by adjusting the values of the capacitors $C_1 - C_3$. The reported SC BGRs achieve a temperature coefficient between 10 and 20 ppm/°C.

The aforementioned structures are all standard CMOS compatible and they do not require any special process steps or devices. The voltage references based on threshold-voltage difference which can be obtained through selective channel implant [50, 51], work-function difference due to different gate dopings [52], and flat-band voltage difference due to different gate materials [53] are not applicable in standard low-cost CMOS technologies since additional fabrication steps are needed.

2.2.5 Summary

In this subsection, an extensive literature review on various kinds of BGR circuits which are proposed to meet the required properties and aforementioned specifications dominated by high precision, low supply voltage and low power operation and low cost. Since the conventional BGRs are first-order temperature compensated, higher-order or non-linear temperature compensation required to obtain better temperature drift performance. The achieved temperature coefficient in the reported literature over higher-order compensated architectures is in the range of 1-10 ppm/°C.

As pointed out, another important limitation of traditional BGR circuits is supply voltage since the value of reference voltage for traditional BGRs is approximately equal to approximately 1.25 eV; hence, they require a supply voltage greater than 1.25 V. There different methods reported in the literature that are proposed to solve this problem and able to work sub-1V supply voltage. The reported sub-1V voltage references can achieve a TC in the range of 7-15 ppm/°C.

From the cost point view, it is important to be able to have a CMOS compatible BGR circuit that does not require any special process step mostly to reduce the threshold voltages of the transistors, hence the minimum required supply voltage. Parasitic substrate BJTs formed in p-well (or n-well) are available in standard CMOS technologies and they are commonly used to implement BGRs. However, there are also CMOS only voltage references in which MOSFET transistors operating in subthreshold region are utilized instead of the BJTs in BGRs. Thanks to the subthreshold operation, very low power consumption is achieved by these structures on

the order of 1-10 nW. However, CMOS-only voltage reference topologies suffer from the large output voltage spread at the process corner. In the literature, it is reported that the temperature coefficient of CMOS-only voltage reference can be reduced down to the 10 ppm/°C range.

Another kind of approach while designing BGRs is sampled-data operation called (SC) based BGRs, if continuous reference output is not required as in the case of data converter applications. If the application is appropriate, this kind of architecture can be preferred intend of other counterparts since they are eliminating the need for large resistors, can reduce the effect of the amplifier offset and optimise the power consumption of the circuit. Moreover, these structures are suitable for fully differential operation that is beneficial for reducing the effects of the power supply noise and substrate coupling [48]. The reported SC BGRs achieve a temperature coefficient between 10-20 ppm/°C.

3. HIGH PRECISION LOW NOISE BANDGAP DESIGN

The bandgap reference is the most popular method to implement voltage references. The principle of operation of the bandgap reference is based on the temperature dependence of forward biased diode voltage that corresponds to base-emitter voltage of a bipolar transistor (BJT) in CMOS technology. Summation of a proportional to absolute temperature (PTAT) voltage with a base-emitter voltage that is complementary to absolute temperature (CTAT) results in compensation of linear temperature dependent terms so that first order temperature compensation achieved. However, logarithmic temperature dependence of the diode voltage still exists after the first order compensation; therefore, curvature compensation is required to further reduce temperature coefficient (improve the precision) by compensating higher order temperature dependency.

In this chapter, two different implementation of curvature-corrected current mode bandgap voltage reference circuits are presented. In the designs, current mode BGRs are preferred since they are more advantageous in terms of power consumption and can operate with a lower supply voltage level. Moreover, a bulk isolation strategy is proposed to reduce the substrate noise coupling which is an important problem of low power voltage defence designs in noisy SoCs. Furthermore, switched biasing technique proposed in [54] is applied to the one of the designed BGR in order to improve the low frequency noise performance of the BGR circuit. The designed voltage reference circuits are realized and fabricated in 0.35 μm 3.3 V triple-well CMOS technology.

3.1 Current Mode Curvature Corrected BGR

The basic operation of the presented BGRs relies on compensating linear and nonlinear components of base-emitter voltage, V_{BE}, temperature dependence as expressed in [12]

$$V_{BE}(T) = V_{g0} - \left(V_{g0} - V_{BE\_Tr}\right)\frac{T}{Tr} - (\eta - x)\frac{kT}{q}\ln\left(\frac{T}{Tr}\right) \qquad \textbf{(3.1)}$$

where V_{g0} is the extrapolated bandgap voltage to 0 K, Tr is the reference temperature, V_{BE_Tr} is the base-emitter voltage at reference temperature, η is a process dependent but temperature independent variable and x relates to the order of the temperature dependence of the collector current ($I_C \propto T^x$).

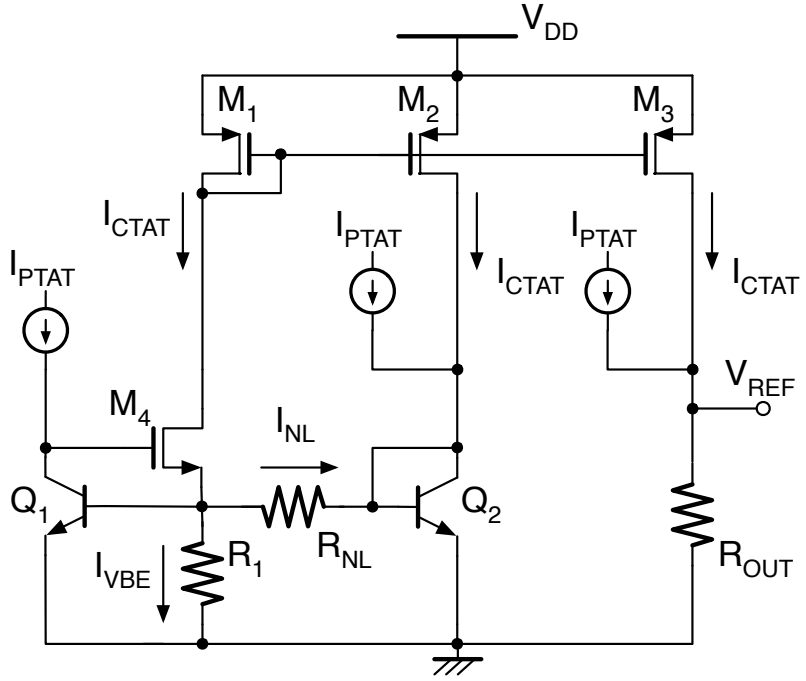

Figure 3.1: Simplified schematic diagram of the $Tln(T)$ curvature correction method.

Figure 3.1 shows the simplified schematic diagram of the $Tln(T)$ curvature correction method adopted for the presented circuits. For the simplicity, generation of PTAT current is not shown in the figure. The linear component, the second-term in **3.1**, is compensated by the PTAT voltage generated using the base emitter voltage differences of two bipolar transistors with different current densities. The nonlinear component, the third-term, is compensated using the base-emitter voltage differences of two bipolar transistors (Q_1 and Q_2) driven with collector currents having different temperature dependency. As seen in Figure 3.1, Q_1 is driven by I_{PTAT} while Q_2 is driven by $I_{PTAT} + I_{CTAT}$ which is temperature independent. Hence, the voltage difference between base-emitter voltages of Q_1 and Q_2 gives rise to the nonlinear compensation current, I_{NL}, on resistor R_{NL} and added to I_{VBE}. Current mode operation is based on generation of a temperature compensated current and then mirroring this current on an output resistor to obtain the reference voltage. Since the proposed circuits perform

curvature correction, a nonlinear compensation current exist at the output stage in the CTAT current. Therefore, in general terms current mode curvature corrected bandgap output voltage can be written as

$$V_{OUT} = (I_{PTAT} + I_{CTAT}) \times R_{OUT} \tag{3.2}$$

where $I_{CTAT} = (I_{VBE} + I_{NL})$.

3.1.1 Theory of operation

Figure 3.2 shows the schematic diagram of the proposed circuit. The negative feedback within the topology equalize the voltages at nodes 1 and 2. The BGR circuit generates three distinct currents. The first one is a linear PTAT current generated by driving two equally sized BJTs $(Q_0,\ Q_1)$ with different collector currents. This current is expressed as

$$I_{PTAT} = V_T \ln(N) / R_0 \tag{3.3}$$

where N is the ratio of the collector currents of Q_0 and Q_1 achieved by adjusting aspect ratios of PMOS current mirrors $(M_{P0},\ M_{P1})$. The second one is proportional to the base-emitter voltage of bipolar transistor Q_1

$$I_{VBE} = V_{BE1} / R_1 \tag{3.4}$$

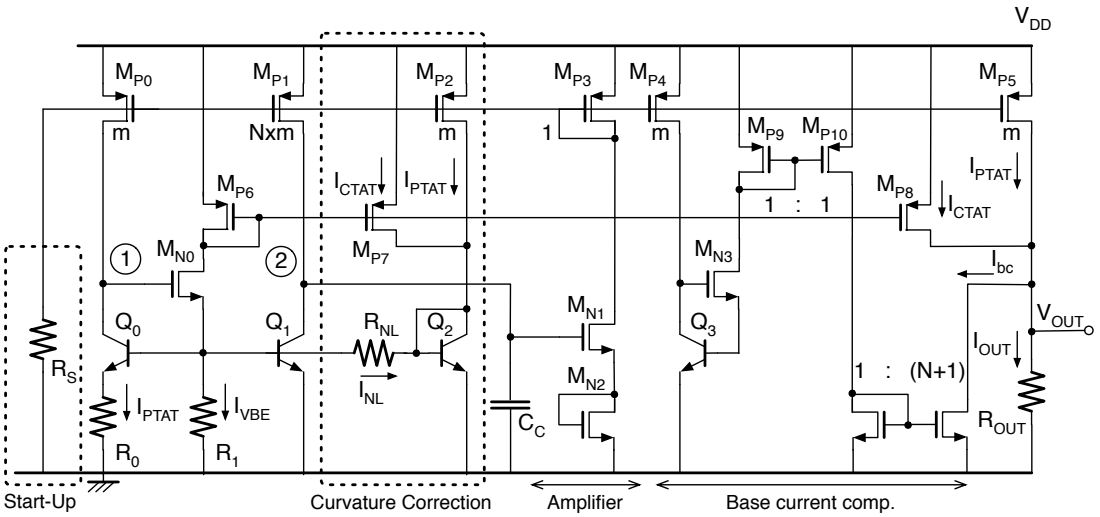

Figure 3.2: Schematic diagram of the proposed current mode bandgap reference circuit.

The third one is a nonlinear current that is temperature independent to the first order. It is generated by driving Q_1 and Q_2 with collector currents that have different temperature dependencies. The base-emitter voltage difference of these transistors is dropped on resistor R_{NL}. Base-emitter voltages of Q_1 and Q_2 can be written as in **3.5** and **3.6**, since Q_1 is driven by a PTAT current $(x = 1)$ and Q_2 is driven by a current that is temperature independent to the first order $(x = 0)$. Thus, the current flowing through R_{NL} is

$$V_{BE1} = V_{g0} - \left(V_{g0} - V_{BE1\_Tr}\right)\frac{T}{Tr} - (\eta - 1)\frac{kT}{q}\ln\left(\frac{T}{Tr}\right) \tag{3.5}$$

$$V_{BE2} = V_{g0} - \left(V_{g0} - V_{BE2\_Tr}\right)\frac{T}{Tr} - (\eta - 0)\frac{kT}{q}\ln\left(\frac{T}{Tr}\right) \tag{3.6}$$

$$I_{NL} = \frac{1}{R_{NL}}\left[(V_{BE1\_Tr} - V_{BE2\_Tr})\frac{T}{Tr} + \frac{kT}{q}\ln\left(\frac{T}{Tr}\right)\right] \tag{3.7}$$

As seen in Figure 3.2, the current flowing through the current mirror formed by $M_{P6} - M_{P8}$, is the sum of the current I_{VBE} and the nonlinear current (I_{NL}). This current, I_{CTAT}, is

$$I_{CTAT} = \frac{V_{g0}}{R_1} + \left[\frac{V_{BE1\_Tr} - V_{g0}}{R_1} + \frac{V_{BE1\_Tr} - V_{BE2\_Tr}}{R_{NL}}\right]\frac{T}{Tr} + \left[\frac{-(\eta - 1)}{R_1} + \frac{1}{R_{NL}}\right]\frac{kT}{q}\ln\left(\frac{T}{Tr}\right) \tag{3.8}$$

The value of R_{NL} is chosen to compensate the $Tln(T)$ temperature dependency of I_{VBE} so that the CTAT current has only linear temperature dependency. **3.9** expresses this choice for R_{NL} and **3.8** turns into **3.10**

$$R_{NL} = \frac{R_1}{(\eta - 1)} \tag{3.9}$$

$$I_{CTAT} = \frac{V_{g0}}{R_1} - \frac{V_{g0} - \eta V_{BE1\_Tr} + (\eta - 1)V_{BE2\_Tr}}{R_1}\frac{T}{Tr} \tag{3.10}$$

Hence, the output current I_{OUT}, which is the sum of CTAT and PTAT currents, can be expressed as:

$$I_{OUT} = \frac{V_{g0}}{R_1} - \frac{V_{g0} - \eta V_{BE1\_Tr} + (\eta - 1)V_{BE2\_Tr}}{R_1}\frac{T}{Tr}$$

$$+\frac{kT}{q}\frac{\ln(N)}{R_0} \tag{3.11}$$

The value of the resistor R_1 is chosen to cancel the linear temperature dependency of CTAT current. This choice of R_1 can be obtained by solving **3.11** for this condition.

$$R_1 = \frac{V_{g0} - \eta V_{BE1\_Tr} + (\eta - 1)V_{BE2\_Tr}}{\ln(N)\,Tr\left(k/q\right)}R_0 \equiv KR_0 \tag{3.12}$$

Finally the output current and the reference voltage are obtained as:

$$I_{OUT} = \frac{V_{g0}}{R_1} \Rightarrow V_{REF} = V_{g0}\frac{R_{OUT}}{R_1} \tag{3.13}$$

Base currents of the bipolar transistors are ignored during the analysis for the sake of simplicity. However, the output current I_{OUT} includes also the base currents of Q_0 and Q_1. While generating the output reference voltage, the base currents of bipolar transistors are subtracted from I_{OUT} using base current compensation circuitry.

3.1.2 Implementation

In the implementation of the proposed circuit, emitter areas of the BJTs are chosen to be minimum and equal in order to match and minimize the device parasitics and the area. Mirroring ratio of collector currents of the BJTs Q_0 and Q_1 are chosen as $N = 4$.

Since the operation of the circuit is based on a current mode technique, the output voltage can be adjusted to an arbitrary level by scaling the output resistor R_{OUT}. In the preferred implementation, the output resistor is chosen equal to 120 kΩ to obtain 0.5 V reference voltage. Table 3.1 gives the transistor sizes of the designed curvature corrected BGR.

Table 3.1: Transistor sizes of the designed curvature corrected BGR.

Transistor	Parameter
Q_0, Q_1, Q_2, Q_3	Normalized Area = 1
M_{P0}, M_{P2}, M_{P4}, M_{P5}	W / L = 10μm / 20μm
M_{P1}	W / L = 40μm / 20μm
M_{P3}	W / L = 5μm / 20μm
M_{P6}, M_{P7}, M_{P8}	W / L = 10μm / 20μm
M_{P9}, M_{P10}	W / L = 0.5μm / 50μm
M_{N0}	W / L = 5μm / 5μm
M_{N1}, M_{N2}	W / L = 10μm / 5μm
M_{N4}	W / L = 0.5μm / 50μm
M_{N5}	W / L = 2.5μm / 50μm

The feedback amplifier is formed by M_{N1}, M_{N2} and M_{P3}. Although M_{N2} reduces the amplifier open loop gain, it is necessary to provide similar operating conditions to Q_0 and Q_1. In the worst case, the loop has more than 40 dB gain which is adequate. Since the small signal gain of the implemented feedback amplifier is independent of the bias current, the circuit is designed to lower the amplifier bias current in order to reduce the power consumption. The feedback loop has only one high impedance node, i.e. node 2. Therefore, a compensation capacitor C_C is connected to this node.

The channel lengths of the transistors $M_{P0} - M_{P5}$ and $M_{P6} - M_{P8}$ that are forming current mirrors are chosen as L=20 μm to minimize the effect of the channel length modulation, thus to achieve more accurate mirroring ratio and high power supply rejection (PSR). The diode load of the feedback amplifier, i.e. M_{P3}, improves the PSR even further. The simplified expression for the PSR of the circuit is

$$\frac{V_{OUT}}{V_{VDD}} = \frac{R_{OUT} \times g_{o,P0}}{R_0 \times g_{m,Q0}} = \frac{R_{OUT}}{R_0} V_T \lambda_P \tag{3.14}$$

where V_T is the thermal voltage and λ_P is the channel-length modulation parameter of the PMOS current mirrors. For a given power consumption target, the value of R_0 is fixed. R_{OUT} is set by the desired output reference voltage level. Therefore, to improve the PSR performance of the circuit, the channel length modulation parameter λ_P should be lowered. This can be achieved either by topological modifications such

as using cascodes or adding degeneration resistors to the PMOS source terminals or by increasing the channel lengths of the PMOS current mirror transistors.

The minimum supply voltage for the circuit is $|V_{th,p}| + |V_{th,n}| + 3V_{DS,sat}$. $V_{th,p}$ and $V_{th,n}$ levels within 0.35 μm CMOS process is around -0.9 V and 0.6 V, respectively, over the temperature range -40 °C to 125 °C. With choosing the $V_{DS,sat}$ voltages of the transistors, the designed BGR circuit can operate with supply voltage down to 1.8V.

A start-up circuit is required since circuit has an additional stable operating point at which the output voltage is zero. The start-up is formed with resistor R_S and it operates by pulling down the gates of the current mirrors formed with transistors $M_{P0} - M_{P5}$ and $M_{P6} - M_{P8}$. At the steady-state, the feedback amplifier adjusts its input so that M_{P3} drain current reaches to the desired level. Therefore, start-up circuitry does not require extra power. Since some of the bias current of M_{N1} is stolen by R_S, the start-up resistor should be chosen large enough to guarantee required loop gain.

The design and implementation of the BGR circuit is finalized by compensating the base currents of the bipolar transistors at the output node. For this purpose, base current compensation circuitry shown in Figure 3.2 is utilized by mirroring a base current of auxiliary BJT with same collector current and subtracting it from output current.

3.1.3 Simulation and experimental results

The proposed BGR circuit is designed and implemented in 0.35 μm 3.3 V CMOS technology having vertical NPN BJT transistors. The layout of the circuit occupying a silicon area of of 350 x 250 μm^2 is given in Figure 3.3. The fabricated samples (also including the BGR circuits in the following section) are packaged in CQFP-64 package, top-level chip microphotograph and bonding diagram are given in APPENDIX A.1. In order to control the trimming bits of designed BGRs and to enable the clocks for the bias switches of the BGR presented in APPENDIX A.3, a digital I^2C block is integrated into the chip. Therefore, performance optimization and trimming of the designed BGR circuits are done via the I^2C interface. Top level pins and I^2C control signals are explained in Table A.1 - A.2, respectively.

During the measurements, ESPEC BTZ-175E thermal chamber has been used to control the temperature of the test chip, while power supply for the circuits are

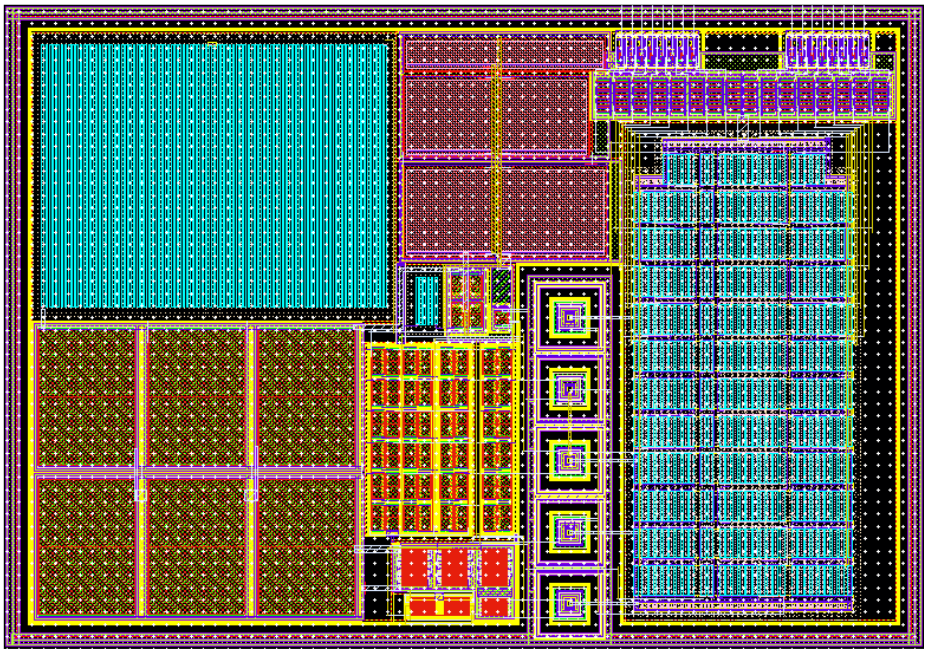

Figure 3.3: Layout of the proposed BGR.

provided from power analyzer Agilent 6705B and the data from output of the voltage references are collected by Agilent 3458A 8.5 digit multimeters. Low frequency noise measurements are done via Agilent B1500A semiconductor parameter analyzer, by using it in voltage sampling mode. The spectrum data for power supply rejection and block bulk isolation measurements are collected via the spectrum analyzer Rohde&Schwarz FSU-26. Measurements automatized by controlling the measurement equipments through NI Labview environment. The test setups and the configuration of the measurement equipments during the measurements are given APPENDIX A.2.

In this section, simulation (post-layout) and experimental results obtained from the designed current mode curvature corrected BGR circuit will be given together. In the supplied performance graphics simulation results are given with solid lines while measurement results given with dashed lines.

Figure 3.4 shows the measured output voltage as a function of temperature after 8-bit trimming of R_1 by using the test setup and procedure given in Figure A.5. The circuit achieves 511.7 mV of output voltage with 9.52 ppm/°C temperature coefficient over the temperature range of -40 °C to 130 °C. The result is consistent with the simulation, in which 10.1 ppm/°C of TC has been obtained in the same temperature range. Measured current consumption of the circuit is 9.8 μA at nominal temperature (25 °C) from a 3.3 V single supply.

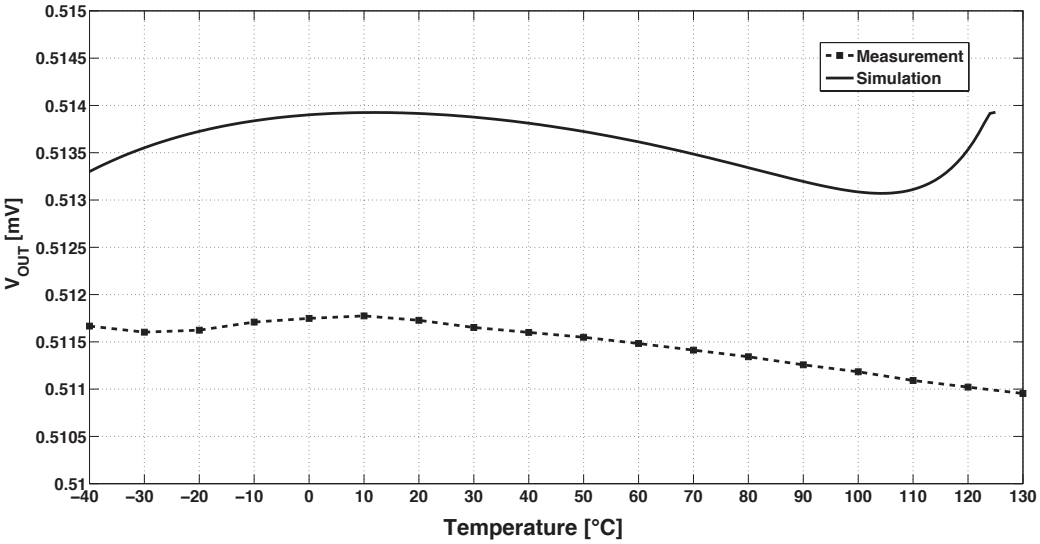

Figure 3.4: Measured and simulated output voltage as a function of the temperature.

Output voltage and TC distributions is given as simulation results since the number of packaged samples were only 3. Figure 3.5 shows the distribution of output voltage level. The proposed circuit generates a 513.5 mV reference with a standard deviation of 4 mV.

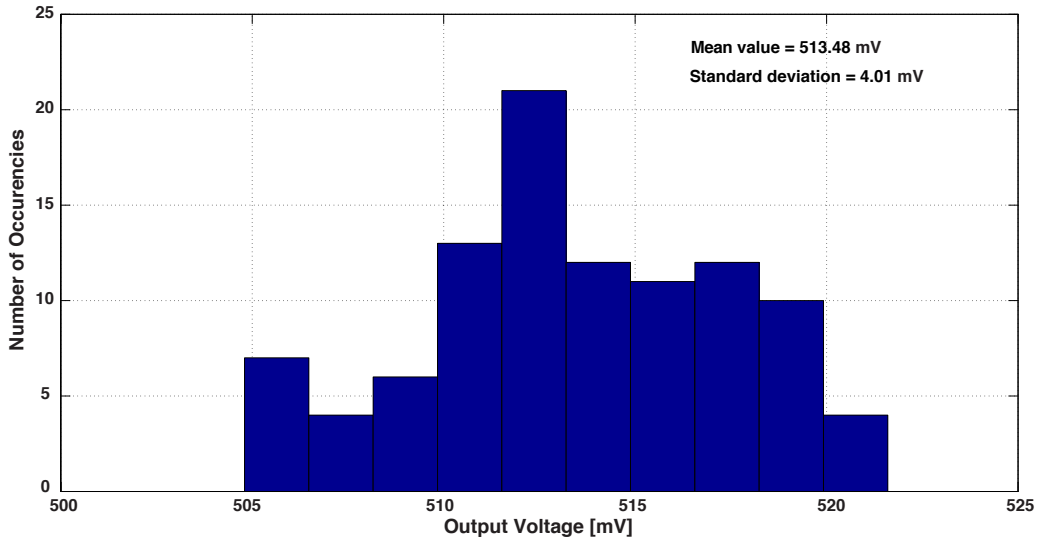

Figure 3.5: Distribution of the reference output voltage obtained through 100 Monte Carlo simulations.

Figure 3.6 shows the distribution of untrimmed temperature coefficient for the temperature range -40 °C to 130 °C, obtained from 100 mismatch-only Monte Carlo simulations. The proposed reference has a mean TC of 18.46 ppm/°C with a standard deviation of 6.04 ppm/°C. Furthermore, the Monte Carlo simulations with mismatch and process variations shows that the temperature coefficient can be lowered to less

then 10 ppm/°C with 99 percent confidence level by 8 bit trimming of R_1. This has been also verified through the 3 samples that we had.

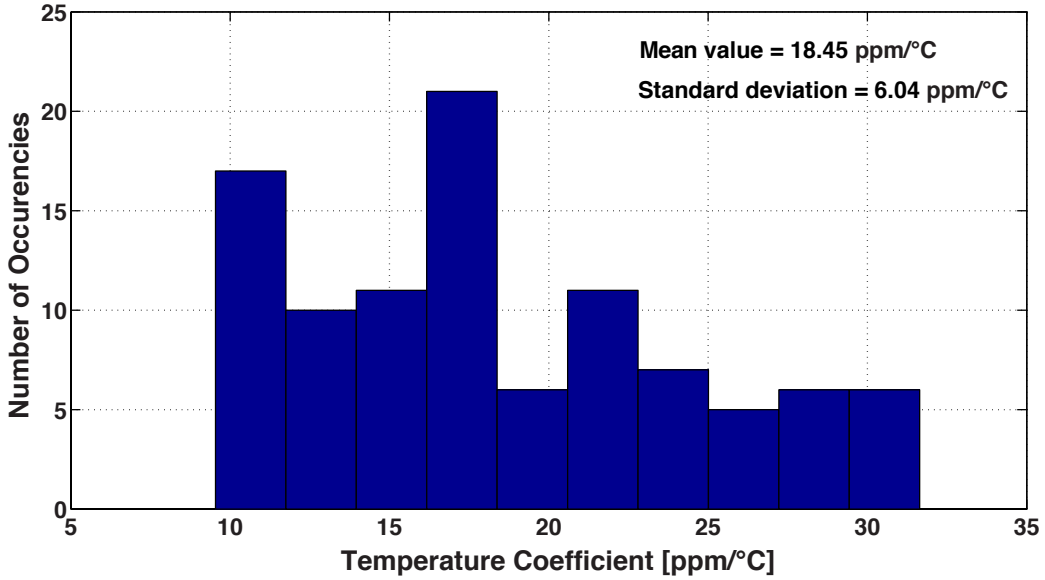

Figure 3.6: Distribution of untrimmed temperature coefficient obtained through 100 Monte Carlo simulations.

In Figure 3.7, output voltage variation with respect to supply voltage is given. The measurement results demonstrate that the circuit is working down to 1.9 V supply voltage with line regulation performance of 781.2 ppm/V for the input voltages between 1.9 V and 3.6 V. As shown in figure, in the post layout simulations, the designed BGR has been operating properly down to 1.8 V supply voltage with a line regulation performance of 715.8 ppm/V, the difference between measurements and simulations can be explained via the threshold voltage variation in the process. The

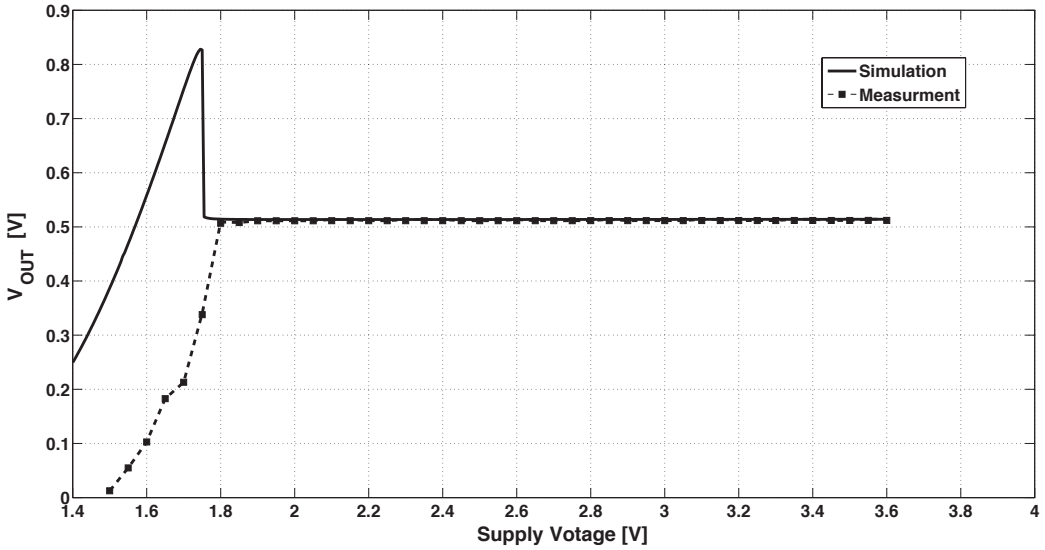

Figure 3.7: Measured and simulated output voltage as a function of supply voltage.

results shows that threshold voltages of the MOS transistors are slightly higher then the typical values in simulations.

Figure 3.8 shows the power supply rejection performance of the designed BGR. PSR of the circuit is -67.5 dB at 100 Hz. As seen from the figure measurements results are given in limited frequency range. Lower limit is determined by the minimum frequency of the spectrum analyser utilized during the measurements, while upper limit due to the bandwidth of the op-amp used in unity gain configuration (see in Figure A.6) to drive the 50 Ω input of the spectrum analyzer. The measurement results are more consistent with simulation results at lower frequencies (-67.3 dB at 100 Hz); while at higher frequencies there is an anomaly between simulation and measurement results that is most probably due to the measurement setup or PCB originated poles.

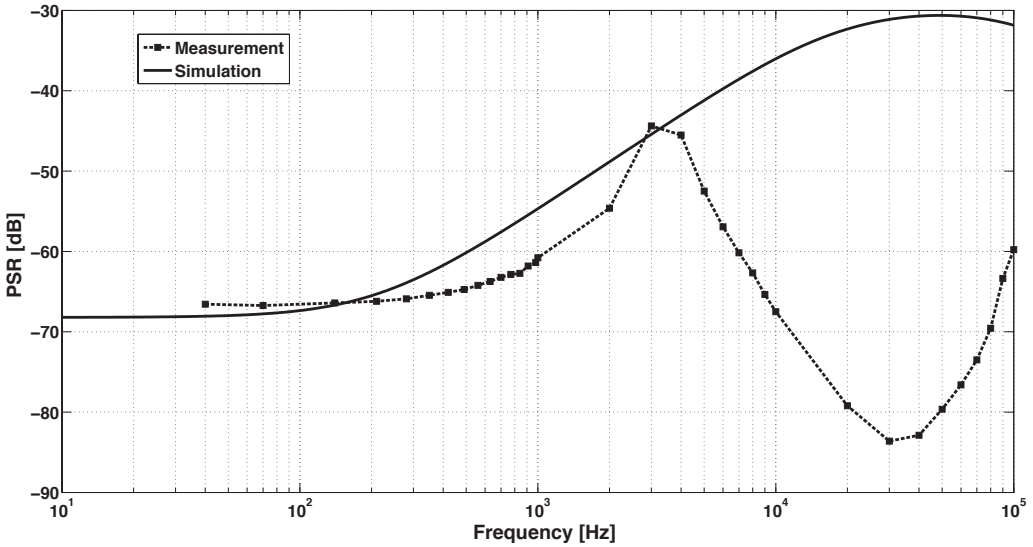

Figure 3.8: Measured and simulated PSR of the output voltage.

Figure 3.9 shows the measured and simulated output noise spectral density of output voltage. For the frequency range 0.1 Hz to 50 Hz, the measurements for this frequency range taken through parameter analyzer by using it in voltage sampling mode with high resolution unit as explained in Figure A.7. The peak-to-peak noise voltage of the BGR output is 22.45 μV (3.75 μVrms) integrated from 0.1 Hz to 10 Hz. To measure flat band noise performance spectrum analyzer utilized since parameter analyzer maximum sampling frequency is 10 KHz. The measured flat band noise is 366.5 nV/$\sqrt{Hz}$. The measured noise results are consistent with the simulated results results that are

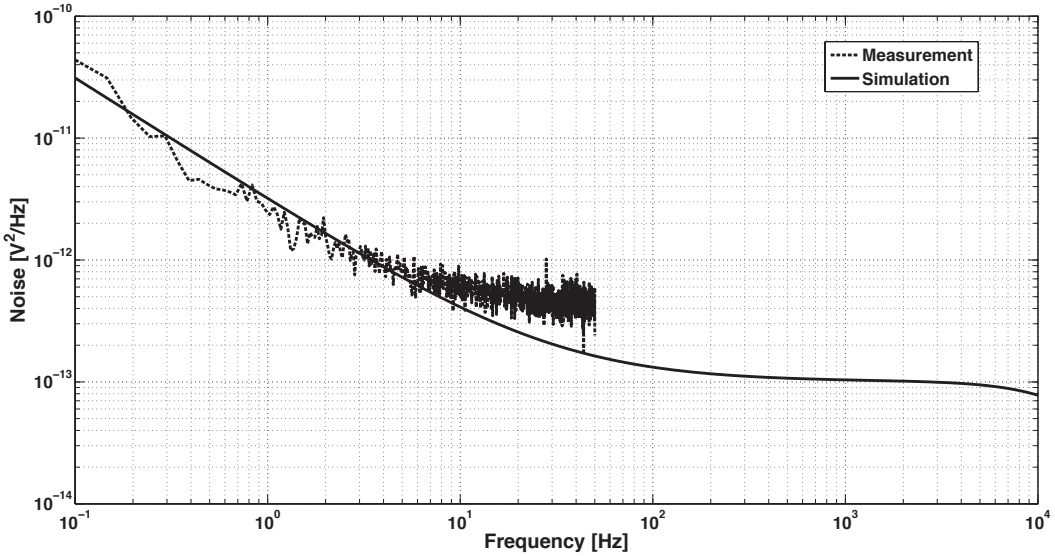

Figure 3.9: Measured and simulated noise power spectral density of the output voltage.

3.91 μVrms noise at the output integrated from 0.1 Hz to 10 Hz and flat band noise 320 nV/$\sqrt{Hz}$.

3.2 Block Bulk-Isolated BGR Design

In this section, the design of a low-drift, bulk-isolated bandgap voltage reference in a 0.35 μm 3.3 V triple-well CMOS technology is presented. The designed circuit operates in current mode and uses a non-linear current in the form of $Tln(T)$ to compensate temperature variation of the reference voltage. The voltage reference is designed so that the circuit can be bulk isolated by a reverse biased junction diode from the rest of the die to drastically reduce substrate noise coupling. This is especially important for voltage reference designs in a very noisy SoC.

3.2.1 Process overview and block bulk isolation strategy

A recent trend of the IC fabrication technologies is the triple-well option, especially for RF and mixed-signal modules [55–57], which enables the designer to fully isolate noisy digital blocks from the noise sensitive ones through reverse-biased junction diodes.

The proposed BGR circuit is implemented in a 0.35 μm triple-well CMOS process. The process has isolated nmos (NMOSI), isolated pmos (PMOSI) and vertical npn (VERT-NPN) transistors. Figure 3.10 shows the process cross-section. The intrinsic

substrate is p-type; hence, it has to be connected to the ground potential. The bulk terminal of each MOSFET has to be biased so that the associated parasitic body diodes are always reverse biased. Notice that, the collector terminal layer of the vertical npn is the same layer as the one utilized for pmos substrate.

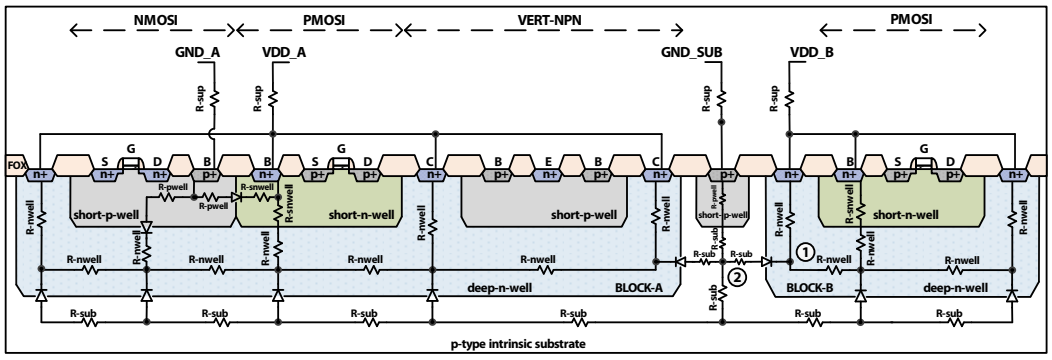

Figure 3.10: Device cross-section and substrate model of the 0.35 μm triple-well CMOS process and the block bulk isolation strategy block diagram.

Block bulk isolation strategy enables bulk isolation of different blocks within the same die. This technique is especially important for mixed signal SoCs, since these systems have to incorporate both noise sensitive precision analog blocks as well as very large and noisy digital blocks. The block bulk isolation technique together with proper separation of the power domain of different functional blocks can significantly reduce the noise coupling between functional blocks.

The technique requires that the layout of each functional block is within one single separate deep n-well layer. This is possible if the utilized process has triple well. The technique allows each block to be isolated from the die substrate by a reverse biased pn-junction and to be isolated from each other by two reverse biased pn-junctions. This can be achieved by following the procedure described below during the schematic design:

- All PMOS transistors have to share the same n-well. Hence, their bulk terminals have to be connected to V_{DD}.
- The collectors of all vertical NPN BJTs should be connected to V_{DD}. They have to be placed within the PMOS n-well layer of the respective block.
- Bulk layers of the NMOS transistors, i.e. p-well, should be within PMOS n-well of the respective block.

A possible implementation cross-section of two blocks, block A and B, designed using the above defined recipe are shown in Figure 3.10. Block-A and Block-B are realized within two separate deep n-wells and they are in separate power domains. The substrate noise sensitivity improvement of BGR output voltage obtained through the block bulk isolation strategy is simulated and results will be given in Section 4.2.4.

In this simulation, the substrate structures of the standard CMOS and triple-well CMOS processes are modeled exactly as described in [58]. This model, shown in Figure 3.10, contains all different reverse-biased junction diodes and the sheet resistances of the respective layers. In order to include the parasitic diodes and the sheet resistances to the simulation, the models of the components provided by the process design kit are modified. Furthermore, the parasitic connection resistances are also included to the model.

In digital circuits, the substrate noise stems from the minority carriers injected from the temporarily forward-biased drain-bulk parasitic junction diode to the substrate due to the digital signal transitions. The majority of the minority carriers are collected by the substrate bias terminal. The remaining part travels through the substrate to reach other circuits and creates substrate noise [21].

To simulate the effectiveness of the proposed isolation strategy, the transfer function gains from the substrate noise sources to the BGR output are compared. Since the noise stems from the minority carriers within the substrate, the noise sources are modeled as current sources connected to the respective substrate nodes for each case, i.e. to the node 1 for the triple-well case and to the node 2 for standard CMOS case within the simulation. Note that NMOS transistors of the BGR schematic modified for the standard CMOS simulation are all in the intrinsic p-type die substrate. As it will be shown later in the Section 3.3.2., the isolation strategy improves the BGR output noise sensitivity more than 40 dB up to 1 MHz.

3.2.2 Designed BGR: theory of operation

Figure 3.11 shows the schematic diagram of the proposed bandgap reference circuit. This circuit is a current mode bandgap reference utilizing the same curvature correction method, so called $Tln(T)$, like the designed BGR in previous section (Section 4.1) as well. However, in the proposed implementation the described block bulk isolation

design procedure is followed leading to the circuit given in Figure 3.11 which is less sensitive to the substrate noise.

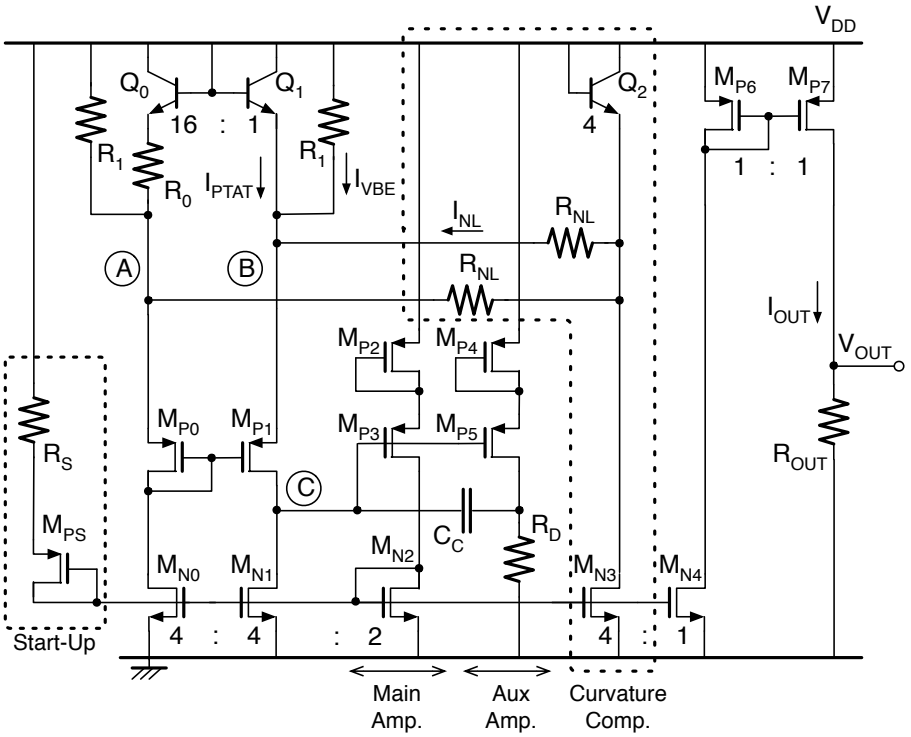

Figure 3.11: Schematic of the proposed bandgap reference circuit.

In this implementation, the common nodes of the BJTs forming the core of the bandgap cell (forming the loop to generate PTAT current) are base and collectors. Therefore, to generate CTAT currents through base-emitter current two separate resistors are required, contrary to the design in previous section. This type of connection of base and collector of the BJTs is advantageous, since base currents are drawn from V_{DD} and they are not affecting directly the PTAT or CTAT currents so the output current. Moreover, the curvature correction method requires two extra resistors, a BJT and a current mirror in addition to the well-known current-mode bandgap core reported in [36]. The design of this branch is optimized to generate the required nonlinear current for curvature correction. For the bandgap core, a simpler gain structure instead of operational amplifier is used, making the circuit much more compact and lower power than the implementations reported in [32, 34].

The negative feedback within the topology forces the nodes A and B to be at equal voltages. The BGR circuit generates three distinct currents. The first one is a PTAT current generated by driving the BJTs (Q_0, Q_1) with different current densities. This current is expressed as

$$I_{PTAT} = V_T \ln(N)/R_0 \tag{3.15}$$

where N is the ratio of the emitter areas of Q_0 and $Q1$. The second one is proportional to the base-emitter voltage of Q_1 and expressed in (**3.16**).

$$I_{VBE} = V_{BE1}/R_1 \tag{3.16}$$

The third one, I_{NL}, is a nonlinear current needed to compensate $Tln(T)$ dependency of (**3.1**). It is generated by driving $Q_{0,1}$ and Q_2 with collector currents that have different temperature dependencies. Q_1 is driven by a PTAT current ($x = 1$ in (**3.1**)) and Q_2 is driven by a current that is temperature independent to the first order ($x = 0$ in (**3.1**)). The base-emitter voltage difference of Q_1 and Q_2 is dropped on R_{NL} to obtain the nonlinear current I_{NL}, given in (**3.17**).

$$I_{NL} = \frac{1}{R_{NL}} \left[(V_{BE1\_Tr} - V_{BE2\_Tr}) \frac{T}{Tr} + \frac{kT}{q} \ln\left(\frac{T}{Tr}\right) \right] \tag{3.17}$$

As it is clear from Figure 3.11, these three current terms are summed separately on nodes A and B. By defining I_{CTAT} as the sum of I_{VBE} and I_{NL}, it can be expressed as:

$$I_{CTAT} = \frac{V_{g0}}{R_1} + \left[\frac{V_{BE1\_Tr} - V_{g0}}{R_1} + \frac{V_{BE1\_Tr} - V_{BE2\_Tr}}{R_{NL}} \right] \frac{T}{Tr}$$
$$+ \left[\frac{-(\eta - 1)}{R_1} + \frac{1}{R_{NL}} \right] \frac{kT}{q} \ln\left(\frac{T}{Tr}\right) \tag{3.18}$$

The value of R_{NL} has to be chosen so that the third term in (**3.18**) is removed and the CTAT current has only linear temperature dependency. Solving (**3.18**) for this condition yields:

$$R_{NL} = \frac{R_1}{(\eta - 1)} \tag{3.19}$$

Substituting (**3.19**) in (**3.18**) results in

$$I_{CTAT} = \frac{V_{g0}}{R_1} - \frac{V_{g0} - \eta V_{BE1\_Tr} + (\eta - 1) V_{BE2\_Tr}}{R_1} \frac{T}{Tr} \tag{3.20}$$

Hence, the output current I_{OUT}, which is the sum of CTAT and PTAT currents, can be expressed as:

$$I_{OUT} = \frac{V_{g0}}{R_1} - \frac{V_{g0} - \eta V_{BE1\_Tr} + (\eta - 1)V_{BE2\_Tr}}{R_1}\frac{T}{Tr}$$

$$+\frac{kT}{q}\frac{\ln(N)}{R_0} \tag{3.21}$$

The value of the resistor R_1 is chosen to cancel the linear temperature dependency of I_{OUT}. The value of R_1 can be obtained by solving (**3.21**) for this condition.

$$R_1 = \frac{V_{g0} - \eta V_{BE1\_Tr} + (\eta - 1)V_{BE2\_Tr}}{\ln(N)\,Tr\left({}^{k}/_{q}\right)}R_0 \equiv KR_0 \tag{3.22}$$

Finally the output current and the reference voltage are obtained as:

$$I_{OUT} = \frac{V_{g0}}{R_1} \Rightarrow V_{REF} = V_{g0}\frac{R_{OUT}}{R_1} \tag{3.23}$$

3.2.3 Implementation

The emitter area ratio N and R_0 have to be determined with matching, area and power consumption in mind. Choosing smaller N results in a larger R_0 over R_1 ratio. Due to the fact that the matching of the BJTs are better than the resistors for the utilized CMOS process, the ratio N is chosen to be rather large, i.e. 16.

Since the operation of the circuit is based on a current mode technique, the output voltage can be adjusted to an arbitrary level by scaling the output resistor R_{OUT}. For the current design, the output reference voltage is set to 220 mV by choosing R_{OUT} equal to 110 kΩ.

During the design of the curvature correction circuit, the size of Q_2 has to be chosen to guarantee the proper direction of I_{NL} for all operation conditions. The bias current has to be chosen so that when compared to I_{NL}, it dominates Q_2's collector current. Table 3.2 gives the transistor sizes of this 0.35 μm CMOS design.

Table 3.2: Transistor sizes of the designed block bulk isolated BGR.

Transistor	Parameter
Q_0	Normalized Area = 16
Q_1	Normalized Area = 1
Q_2	Normalized Area = 4
M_{N0}, M_{N1}, M_{N3}	W / L = 40 μm / 40 μm
M_{N2}	W / L = 20 μm / 40 μm
M_{N4}	W / L = 10 μm / 40 μm
M_{P0}, M_{P1}	W / L = 160 μm / 5 μm
M_{P2}, M_{P3}	W / L = 60 μm / 5 μm
M_{P4}, M_{P5}	W / L = 30 μm / 5 μm
M_{P6}, M_{P7}	W / L = 5 μm / 40 μm
M_{PS}	W / L = 40 μm / 5 μm

The minimum supply voltage of the circuit is $V_{th,n} + \left|V_{th,p}\right| + 3V_{DS,sat}$. Since the maximum threshold voltages of NMOS and PMOS transistors are around 0.6 V and -0.9 V, respectively, over the temperature range -40 °C to 125 °C, the designed BGR circuit can be designed to operate with a supply voltage down to 1.8 V assuming better than 100mV gate overdrive voltage. However, for this implementation, the gate overdrive voltages are chosen bigger than 150 mV to achieve better matching. Therefore, the minimum supply voltage of the this implementation is 2 V.

The supply current of the topology is solely determined by the resistor R_0. The equation (**3.24**) gives the total supply current of the presented BGR. Note that although increasing R_0 reduces the total supply current, resistors occupy larger estate and the performance of the reference degrades due to worsened device matching. For this design, R_0 is chosen as 25 kΩ.

$$I_{total} = 4\left(\frac{V_{g0}}{KR_0}\right) \tag{3.24}$$

The feedback amplifier forces the voltages at nodes A and B to be equal using the current flowing through M_{N0} and M_{N1}. As with every bandgap core, the circuit has positive $(M_{P3} - M_{N2} - M_{N1})$ and negative $(M_{P3} - M_{N2} - M_{N0} - M_{P0} - M_{P1})$ feedback loops [59]. The simplified gains of the positive and negative feedback loops can be expressed as:

$$A_{v\_p} = m\left(\frac{g_{m\_P3}}{g_{m\_P3}\frac{1}{g_{m\_P2}}+1}\right)R_C \tag{3.25}$$

$$A_{v\_n} = -m\left(\frac{g_{m\_P3}}{g_{m\_P3}\frac{1}{g_{m\_P2}}+1}\right)\left(1+\frac{g_{m\_P0}R_0}{1+g_{m\_P0}r_e}\right)R_C \tag{3.26}$$

where m is the ratio of the aspect ratios of M_{N0} and M_{N2}, R_C is the equivalent resistance of the node C, r_e is the small-signal emitter resistance of Q_1 and g_{m_P0}, g_{m_P1}, g_{m_P2} and g_{m_P3} are transconductances of the transistors M_{P0}, M_{P1}, M_{P2} and M_{P3}, respectively. The feedback loop gain that is the sum of negative and positive gains, is given in (**3.27**).

$$A_{v\_total} = -m\left(\frac{g_{m\_p3}}{1+g_{m\_p3}\frac{1}{g_{m\_p2}}}\right)\left(\frac{g_{m\_p0}R_0}{1+g_{m\_p0}r_e}\right)R_C \tag{3.27}$$

Although M_{P2} reduces the gain of the amplifier, it is necessary to provide similar biasing conditions to M_{P0} and M_{P1}. It reduces the gain by almost 6 dB since M_{P2} and M_{P3} are equally sized. The ratio m determines the current level of the feedback amplifier formed by M_{P2}, M_{P3}, M_{N2}.In order to optimize the amplifier current level and the loop gain, m is chosen to be 2 for the current design.

In order to prevent right half plane zero of the Miller compensation, an auxiliary amplifier formed by M_{P4}, M_{P5} and R_D is utilized in order to load the node C with C_C multiplied by the auxiliary amplifier gain. To reduce power consumption, M_{P5} and M_{P4} are sized half of M_{P3} and M_{P2} so that auxiliary amplifier bias current is half that of the main amplifier. Corner simulations show that, in the worst case, the loop has more than 50 dB gain and 60° an adequate phase margin.

The simplified transfer function from power supply to output node derived without curvature $TlnT$ compensation scheme and start-up circuit, is

$$\frac{V_{OUT}}{V_{VDD}} = \frac{V_{OUT\_DC}\lambda_n}{R_0}\left(\frac{1}{g_{m\_Q0}}+\frac{1}{g_{m\_P0}}\right) \tag{3.28}$$

where V_{OUT_DC} is the DC level of the output voltage, λ_n is the channel-length modulation parameter of the NMOS transistors, g_{m_Q0} and g_{m_P0} are transconductances of transistors Q_0 and $M_{P0,1}$, respectively. Note that V_{OUT_DC} is not a design parameter and is fixed by the system level requirement. The value of R_0 is set by the desired power

consumption level. Transconductance g_{m_Q0} is determined by its collector current, i.e. PTAT current. In other words, for a given power consumption target, the value of R_0 and g_{m_Q0} are also fixed. Therefore, to improve the PSR performance of the circuit, the channel-length modulation parameter λ_n is the only parameter that the designer can play with. To increase the output resistance of the NMOS transistors, it is possible to make topological modifications such as using a cascode topology or adding degeneration resistors to the NMOS source terminals.

To analyze and optimize the noise performance of the proposed circuit, dominant noise sources of the circuit for different frequency ranges are identified and their transfer functions to the output are derived. In addition to the common design practices to reduce the device noises, the design recipes to reduce the transfer function magnitude will be analyzed next.

For the frequency range 0.1 Hz-100 Hz, flicker noises of transistors M_{N0}, M_{N1} and M_{N4} are dominant noise sources. The drain noise current transfer function of M_{N0}, M_{N1} and M_{N4} are given in (**3.29**), (**3.30**) and (**3.31**) respectively. Notice that R_{OUT} has to be reduced to improve low frequency noise performance whereas it has to be increased to improve PSR.

$$\frac{V_{OUT}}{I_{n-M_{N0}}} = -\frac{R_{OUT}}{4R_0}\left(\frac{1}{g_{m\_P0}} + \frac{1}{g_{m\_Q0}} + R_0\right) \tag{3.29}$$

$$\frac{V_{OUT}}{I_{n-M_{N1}}} = \frac{R_{OUT}}{4R_0}\left(\frac{1}{g_{m\_P0}} + \frac{1}{g_{m\_Q0}}\right) \tag{3.30}$$

$$\frac{V_{OUT}}{I_{n-M_{N4}}} = \frac{R_{OUT}}{1 + g_{o\_P7}R_{OUT}} \approx R_{OUT} \tag{3.31}$$

where g_{o_P7} is the output conductance of the transistor M_{P7}. For a chosen output voltage level the ratio of R_{OUT}/R_0 is fixed. Moreover, transconductance g_{m_Q0} is also fixed since it is set by the desired power consumption level. Therefore, for a desired output voltage and power consumption level, the dominant flicker noise transfer functions can only be slightly improved by increasing g_{m_P0}.

For the frequency range 100 Hz-1 MHz, channel thermal noises of transistors M_{N0}, M_{N4}, M_{P6} and M_{P7}, thermal noises of resistors R_{OUT} and R_0 are the dominant noise

sources. The noise transfer functions for M_{N0} and M_{N4} have already been given in (**3.29**) and (**3.31**). It is equal to unity for R_{OUT} and approximately equal to R_{OUT} for M_{P6} and M_{P7}. The simplified thermal noise transfer function of R_0 can be expressed as:

$$\frac{V_{OUT}}{I_{n-R_0}} = \frac{KR_{OUT}\ln(N)}{4} \tag{3.32}$$

The value of K is set together with N to optimize the temperature coefficient. R_{OUT} is determined by the chosen output voltage level and desired power consumption.

The noise analysis of the proposed BGR shows that the best method of reducing the output noise spectral density is to reduce the R_{OUT} which will result in an increase in power dissipation for a given output voltage level.

Presented BGR requires a start-up circuit since the circuit has an additional stable operating point at which the output voltage is zero. The start-up is formed with resistor R_S and diode connected transistor M_{PS}. It operates by pulling up the gates of the current mirrors formed with transistors $M_{N0} - M_{N4}$. A diode connected transistor M_{PS} is used to decrease voltage drop across R_S. At the steady-state, the feedback amplifier adjusts its input so that drain current of the transistor M_{N2} reaches to the desired level. Therefore, the start-up part does not require extra power. Since some of the bias current of M_{P3} is stolen by R_S, the start-up resistor should be large enough to guarantee the required loop gain. Note that since R_S is connected to the supply, the start-up circuit also degrades the PSR of the BGR. Start-up effects are included in PSR simulation results.

3.2.4 Simulation and experimental results

The BGR circuit is designed and implemented in a 0.35 μm 3.3 V triple-well CMOS technology having vertical NPN BJT transistors. The layout of the circuit occupying a silicon area of of 325 x 300 μm^2 is given in Figure 3.12. The designed circuit is fabricated in the same die with the BGR designed in Section 3.1, the package, test PCB and test setups are the same with previous one. In this subsection, the simulation (post-layout) and measurement results of block bulk isolated BGRs which are designed and fabricated in 0.35 μm triple-well CMOS technology is presented.

Moreover, a comparison between the same BGR circuits implemented with isolated and non-isolated devices and surrounded with a noisy diffusion that emulates the noise of digital circuits is presented in order to show the effectiveness of the proposed strategy.

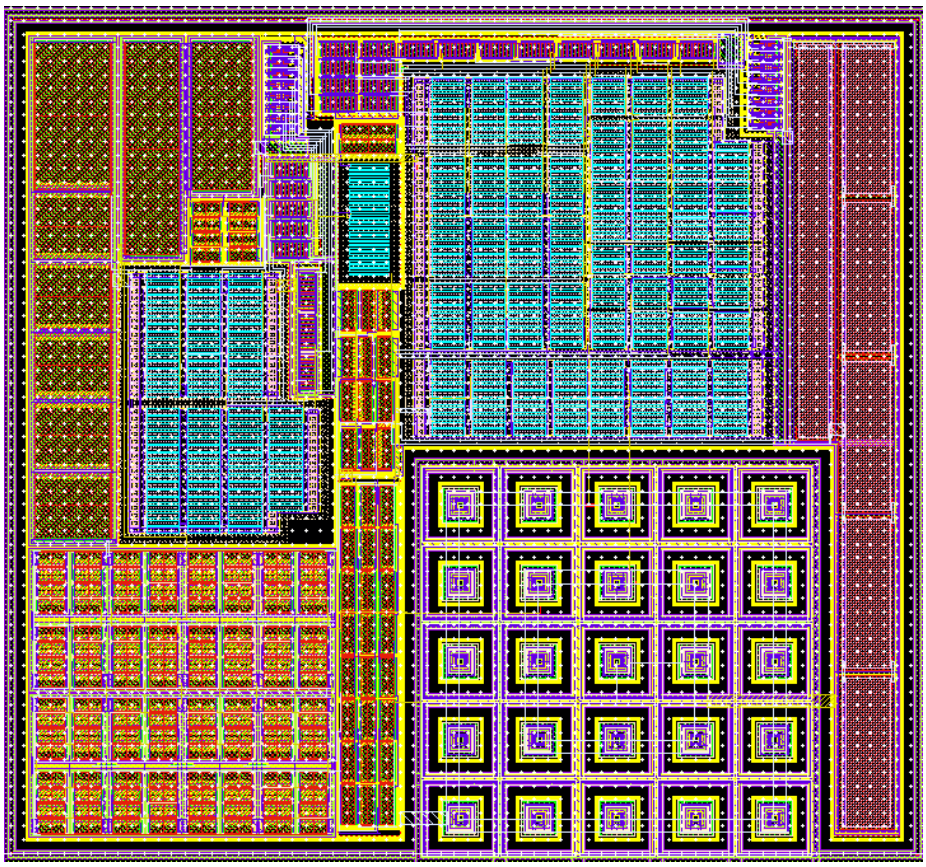

Figure 3.12: Layout of the proposed BGR.

Figure 3.13 shows the measured output voltages of the BGRs as a function of temperature after 8-bit trimming of R_1. The BGR circuit achieves 220.38 mV of output voltage with a TC of 3.56 ppm/°C over the temperature range of -40 °C to 130 °C. The minimum TC achieved in the simulations (the best trimmed one in nominal process corner) for the both circuits have been on the order of 1.5 ppm/°C while the the output voltage levels have been almost the same. The measured total current consumption of the circuits are 33.15 μA.

Also in this circuit output voltage and TC distributions is given as simulation results since the number of packaged samples were only 3. Figure 3.14 shows the distribution of output voltage level. The proposed circuit generates a 220.4 mV reference with a standard deviation of 1.78 mV.

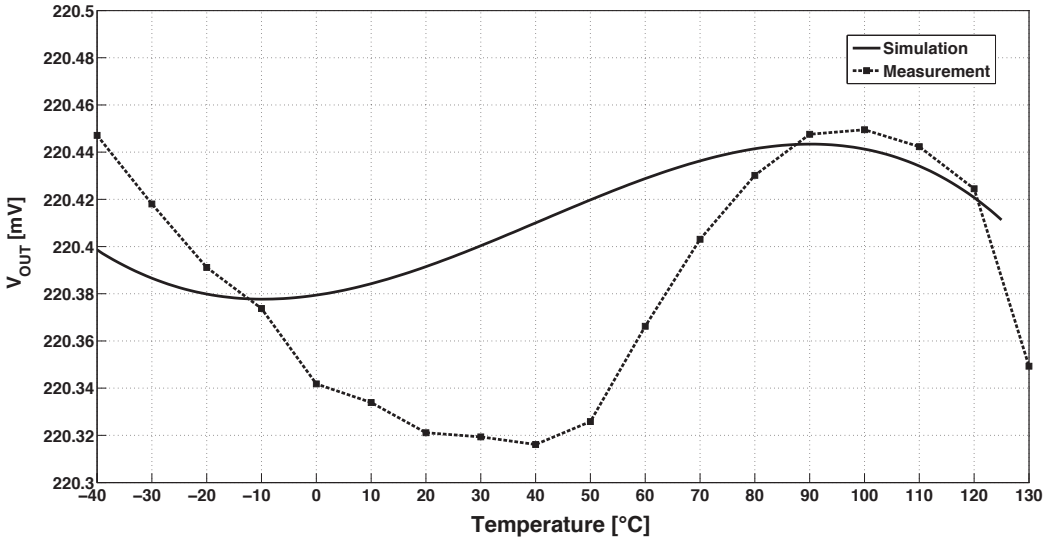

Figure 3.13: Measured and simulated temperature variation of best-compensated reference voltage.

Figure 3.15 shows the distribution of untrimmed temperature coefficient for the temperature range -40 °C to 130 °C, obtained from 100 mismatch-only Monte Carlo simulations. The proposed reference has a mean TC of 11.45 ppm/°C with a standard deviation of 6.34 ppm/°C. Furthermore, the Monte Carlo simulations with mismatch and process variations shows that the temperature coefficient can be lowered to less then 2 ppm/°C with 99 percent confidence level by 8 bit trimming of R_1. However, in the measurements, TCs of the BGRs have been lowered to the level of 3.5 ppm/°C for the available 3 samples.

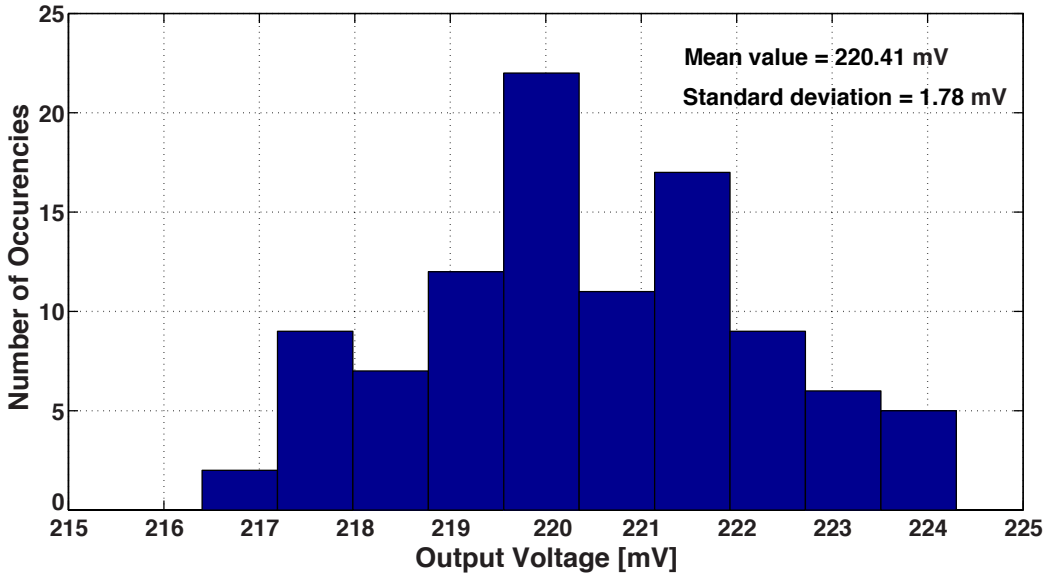

Figure 3.14: Distribution of the reference output voltage obtained through 100 Monte Carlo simulations.

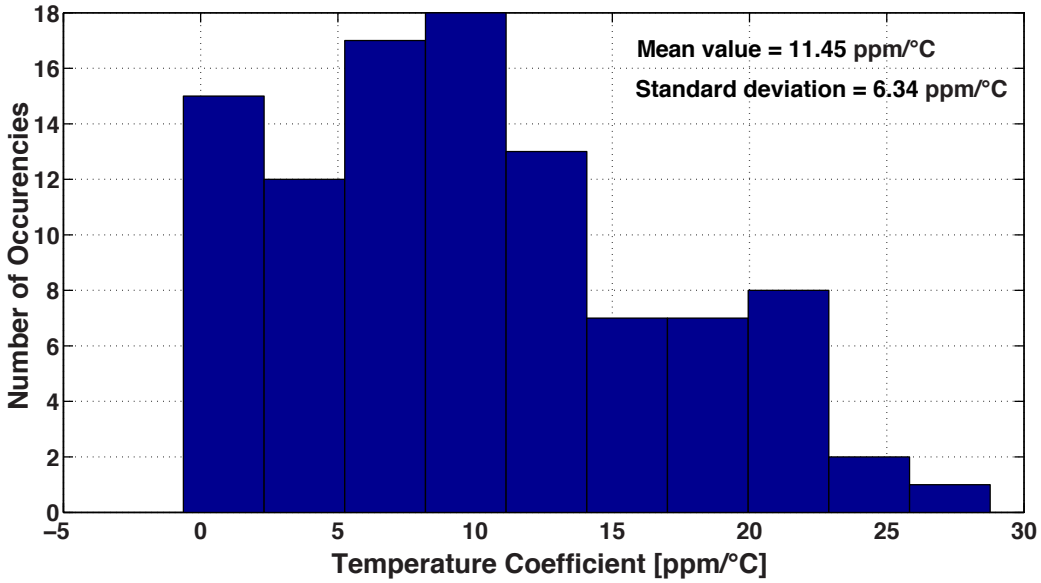

Figure 3.15: Distribution of untrimmed temperature coefficient obtained through 100 Monte Carlo simulations.

In Figure 3.16, variation of output voltages with respect to supply voltage is given. The measurement results demonstrate that the circuit is working down to 2.1 V supply voltage with line regulation performance of 0.16 %/V for the input voltages between 2.1 V and 3.6 V. In the simulations, the BGR has been operating properly down to 2 V supply level, this 100 mV difference between the simulations and measurements should be the result of threshold voltage variation in the process.

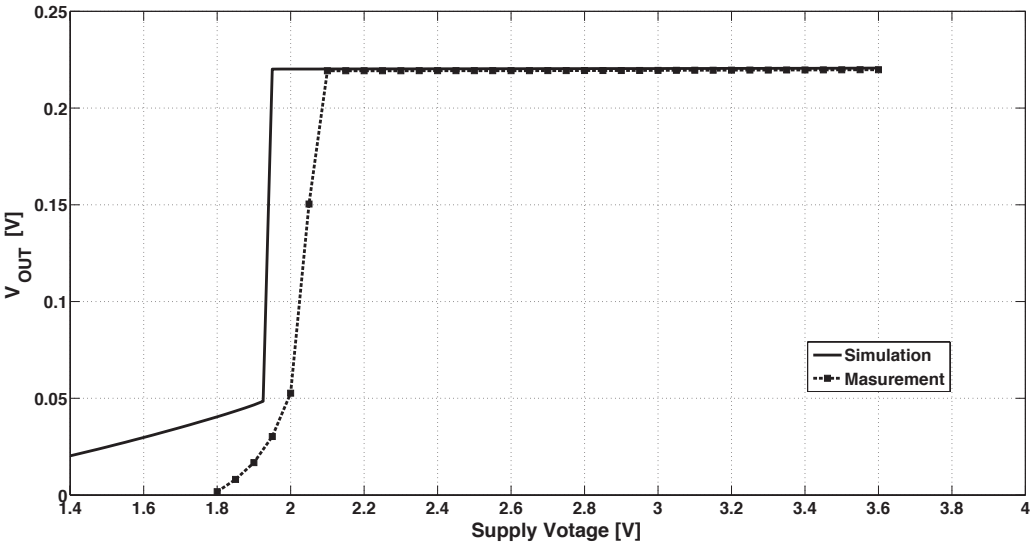

Figure 3.16: Measured and simulated output voltage as a function of supply voltage.

Figure 3.17 shows the power supply rejection performances of the BGR. PSR of the circuit is -69.51 dB at 100 Hz. The measurement results are more consistent with simulation results at lower frequencies (-70.35 dB at 100 Hz). However, as mentioned

before, since the test PCB and setups are the same with the previous designed BGR, the anomaly of PSR between simulation and measurement results for the high frequency range is also seen in Figure 3.17 due to the same reasons.

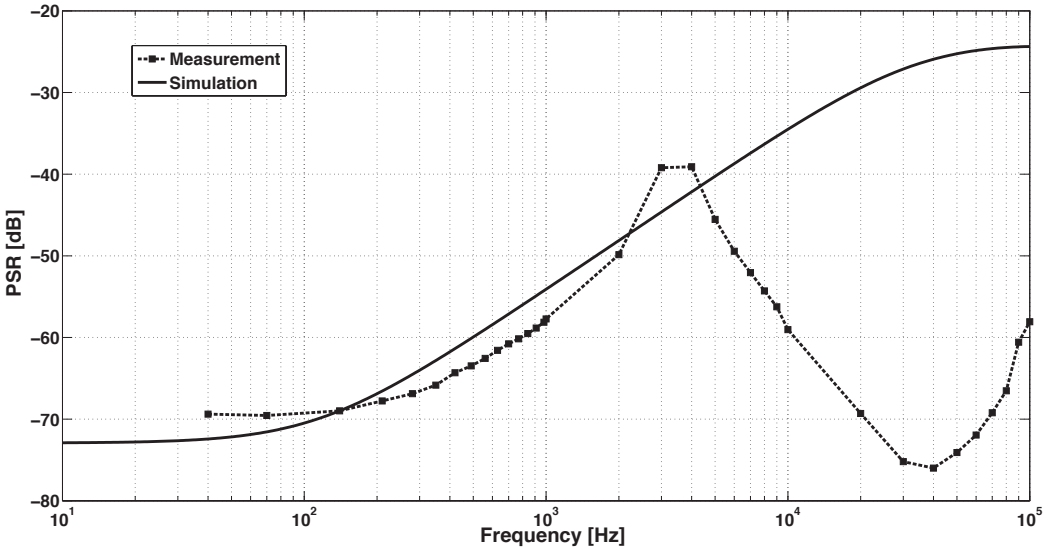

Figure 3.17: Measured and simulated PSR of the output voltage.

Figure 3.18 shows the measured and simulated output noise spectral density. The measurements results are obtained for the frequency range 0.1 Hz to 10 Hz via the same setup given in Figure A.7. The peak-to-peak noise voltage at the outputs are 15.26 μV (2.54 μVrms) while the measured flat band noise is around 170 nV/$\sqrt{Hz}$ for both of the circuits. The measured noise results are slightly higher but consistent with the simulated ones that are 1.96 μVrms noise at the output integrated from 0.1 Hz to 10 Hz and 100 nV/$\sqrt{Hz}$ flat band noise.

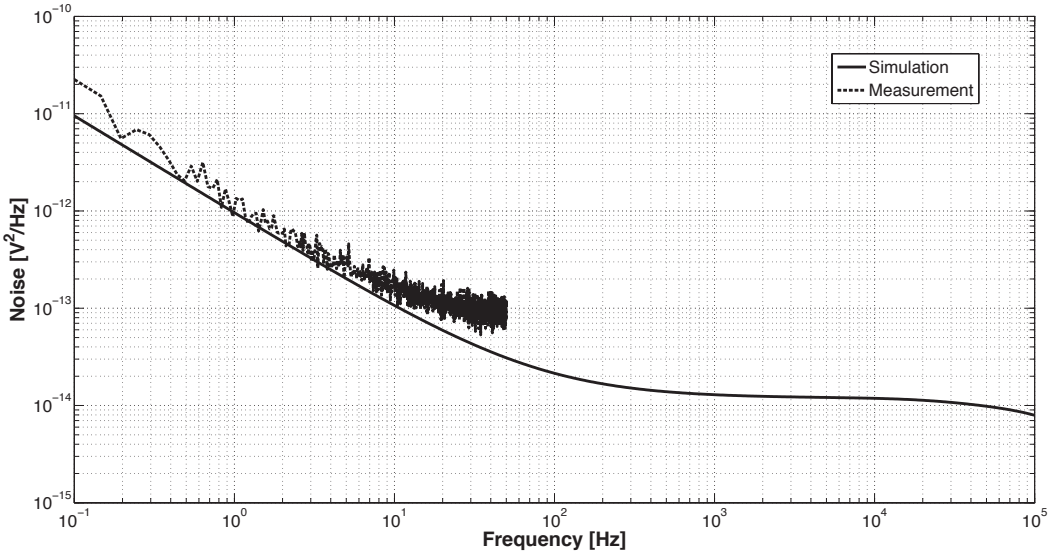

Figure 3.18: Measured and simulated output noise spectral density.

In order to show the effectiveness of the proposed block bulk isolation strategy, the same BGR are implemented with isolated and non-isolated devices and surrounded by a diffusion layer. The adopted strategy is exciting the surrounding diffusion externally in order to emulate the noise injected to the bulk from the digital circuits and measuring the gains from the diffusion to the BGR outputs implemented with isolated and non-isolated devices. Figure 3.19 shows the measured gains from diffusion to the BGR outputs when the diffusion is biased to -200 mV and excited with 100 mV sinusoidal signal. Measurement results show that with the proposed block bulk isolation strategy, the substrate noise immunity of the circuit is improved more then 40 dB frequencies up to 1 MHz.

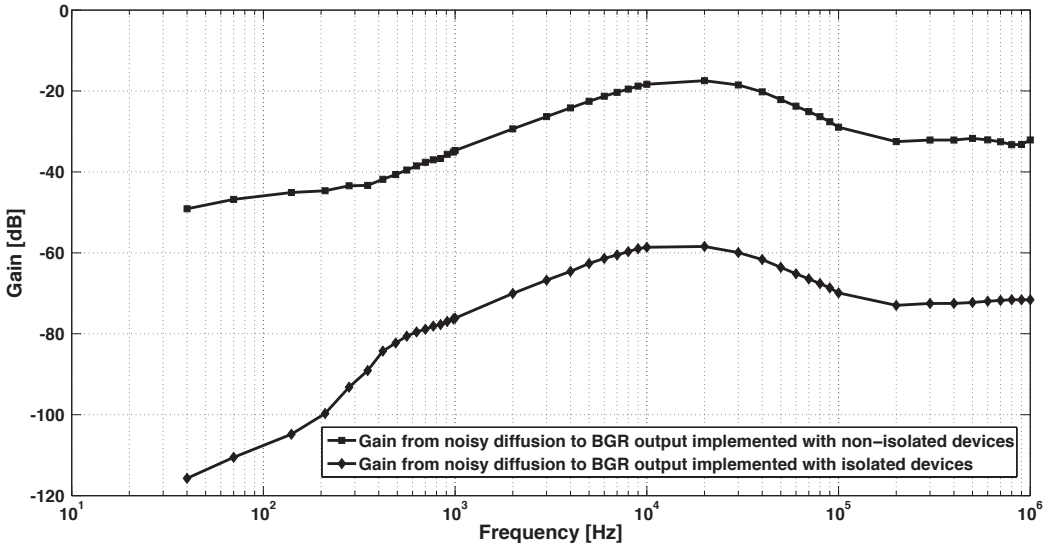

Figure 3.19: Measured gains from diffusion layer to bandgap reference outputs implemented with isolated and non-isolated devices (in a standard CMOS and in a triple-well CMOS proceses).

Moreover, in order to improve the low frequency noise performance of the BGR, transistor sizes of NMOS current mirrors, which are the dominant noise sources (especially M_{N0}, M_{N1} and M_{N4}) in the frequency range 0.1 Hz to 100 Hz, are increased while keeping the aspect ratio constant in order to have the same operating conditions. As a result, $W \times L$ values of the transistors will be increased leading to a low flicker noise. On the other hand, transistors sizes of PMOS current mirror at the output is also increased with the same ratio in order to increase output impedance of the current mirror and improve the PSR performance. Since with both of these two modifications $W \times L$ of the transistors are increasing, the matching performance is improved as well, leading to less mean value of the TC and standard deviation in Monte Carlo

simulations at the cost of area. Table 3.3 gives the measured performance summary and comparison of these two designs utilizing exactly the same architecture.

Table 3.3: Performance summary of the designed BGRs.

	L = 40 μm	**L = 120μm**
Technology	0.35	0.35
Output voltage [mV]	220.38	217.95
Minimum supply voltage [V]	2.1	2
Supply current [μA]	33.15	32.65
Mean temperature coefficient [ppm/°C]	11.45	6.22
Standard deviation [ppm/°C]	6.34	4.10
Minimum temperature coefficient [ppm/°C] 8-bit trimmed	3.56	3.75
Temperature range [°C]	-40-130	-40-130
PSR @ 100 Hz [dB]	-69.51	-75.68
Line regulation [%/V]	0.16	0.0713
Noise peak-to peak, 0.1 Hz-10 Hz [μV]	15.26	5.51
Area [mm^2]	0.0975	0.165

3.3 Summary

In this chapter, the design, implementation and measurement results of two different curvature-corrected current mode BGR circuits in 0.35 μm triple-well 3.3 V CMOS technology having vertical npn (VERT-NPN) transistors are presented. Both of the circuits utilizing so called $Tln(T)$ type curvature correction, via generation of a nonlinear compensation current.

The first designed BGR circuit (Section 3.1) generates an output voltage of 511.7 mV and can operate with a supply voltage down to 1.9 volts. The temperature coefficient of the output voltage is 9.52 ppm/°C over the temperature range -40 to 130 °C after 8-bit trimming. It consumes 9.8 μA current from 3.3 V supply voltage with a line regulation of 781.2 ppm/V while supply voltage changes within the range 1.9 V to 3.6 V. PSR of the circuit is -67.5 dB at 100 Hz. Its peak-to-peak output noise voltage is 22.45 μV (3.91 μVrms) integrated over the frequency range of 0.1 Hz to 10 Hz while flat band noise is 366.5 nV/$\sqrt{Hz}$. The designed BGR circuit occupies an area of 250 x 350 μm^2.

The circuit designed in Section 3.1 was suffering from base currents of NPN BJTs that are effecting directly the output current. Thus, it is compensated via an extra circuitry for the base current compensation as shown in Figure 3.2. This is a solution without changing the core or the topology of the designed circuit. However, in order to get rid of the problem itself (base current incorrection), the circuit topology has to be modified such that design expressions are not be modified by base currents.

In Section 3.2, a bulk isolation strategy is presented in order to reduce the substrate noise coupling and the design of the BGR circuit employing proposed block bulk isolation strategy is demonstrated. Note that in this topology the base currents are not a problem anymore, since they do not directly affect the generated currents. Moreover, in order to improve the low frequency noise performance of the BGR, transistor sizes ($W \times L$) of NMOS current mirrors, which are the dominant noise sources in the frequency range 0.1 Hz to 100 Hz, are increased while keeping the aspect ratio (W/L) constant. On the other hand, transistors sizes of PMOS current mirror at the output stage is also increased with the same ratio in order to improve the PSR performance. Both of these two modifications lead to improve the matching performance that can be observed from the decrease in the mean value of the TC and standard deviation in Monte Carlo simulation results given in Table 3.3.

Measurement results show that the designed BGR circuit (with L= 120 μm) generates an output voltage of 217.95 mV with a TC of 3.75 ppm/°C in the temperature range -40 °C to 130 °C. The circuit can operate with supply voltage down to 2 V. It consumes 32.65 μA current from 3.3V supply voltage with a line regulation of 713 ppm/V while supply voltage changes within the range of 2 V to 3.6 V. PSR of the circuit is -75.68 dB at 100 Hz. Its peak-to-peak output noise integrated from 0.1 Hz to 10 Hz is 5.51 μV (0.918 μVrms). The designed BGR circuit occupies an area of 550 x 300 μm^2. Due to the employed block bulk isolation strategy, the substrate noise sensitivity at the BGR output improved more than 40 dB up to 1 MHz.

Performance summary of the designed circuits and their comparison with other high precision voltage reference circuits reported in the open literature is given in Table 3.4. The table shows that the designed BGR achieves the best temperature coefficient (after 8-bit trimming) with minimum area and supply current. Its noise performance is equivalent to the best reported [39] while occupying 1/2.5 the area. Moreover, due to

the employed block bulk isolation strategy, the substrate noise sensitivity at the BGR output improved more than 40 dB up to 1 MHz.

Table 3.4: Performance comparison of curvature corrected bandgap reference circuits in literature.

	BGR-1	**BGR-2**	**[60]**	**[61]**	**[39]**	**[62]**
Technology [μm] CMOS	0.35	0.35	0.35	0.5	0.5	0.35
Output Voltage [V]	0.512	0.218	0.617	0.489	0.191	0.858
Min. Voltage [V]	1.9	2	1.8	1.2	1	1.4
Supply Current [μA]	9.8	32.65	38	48	20	116
Temp. Coef. [ppm/°C]	9.52	3.75	3.9	8.9	11	12.4
Temp. Range [°C]	-40-130	-40-130	-15-150	-40-110	-40-125	-20-100
PSR @100Hz [dB]	-67.5	-75.68	N/A	-58	N/A	-68
Line Regulation [ppm/V]	781	713	390	2400	252	N/A
Noise pp, 0.1-10Hz [μV]	22.45	5.5	N/A	N/A	4	54.6
Area [mm^2]	0.081	0.165	0.102	0.1	0.4	1.2
Trim bits	8	8	7	NT	NT	15

4. LOW VOLTAGE AND LOW POWER BANDGAP DESIGN

Circuits for mobile electronics require ultra-low power consumption and need to work with a very-low supply voltage. It would be optimal to use a supply voltage on the order of 0.5-0.6 V because this is the voltage range at the output of a single solar cell [63]. Digital circuits can work with such low voltages, since their required supply voltage is just a bit more than the threshold of an n-channel or a p-channel transistor. On the contrary, conventional analog blocks such as amplifiers and reference circuits need higher supply voltage due to the required overheads at the output stage and the necessary output swing.

The band of signals handled in many sensor applications is narrow and the speed is not of much importance. Instead, low-power consumption is the more relevant and important design requirement. Indeed, the power harvested indoors by a solar cell battery is around tens of μW/cm^2 [64]. Therefore, the power consumed by a single analog cell can be in the hundreds of nW range.

Low supply voltage implies low signal-to-noise ratio (SNR): the voltage swing of the signal is low, but the noise remains the same. This is a problematic issue. However, at the same time, it allows moderating the analog performance requirements. For instance, a large DC gain in op-amps is not as important, since the errors due to the value and non-linearity become negligible compared to the expected SNR.

Increasing requirements for analog blocks working with a sub 1-V supply voltage and very low power should be satisfied by new circuit solutions using standard technologies. In this chapter, studies are focused on new voltage reference topologies that are appropriate for sub-micron technologies and can work with very low supply voltages. For the implementation of proposed voltage reference circuits, a 0.18 μm CMOS technology is chosen. Detailed information about the design implementations and obtained results about the proposed low voltage and low power voltage reference topologies are presented in the following sub-sections.

4.1 Proposed Voltage ReferenceTopologies

The basic operation of traditional bandgap reference circuits relies on the summation of a proportional to absolute temperature (PTAT) voltage with a complementary to absolute temperature (CTAT) voltage. This results in the cancellation of the linear temperature dependent terms so that first-order temperature compensation is achieved. The CTAT voltage is obtained through the temperature dependence of a forward biased diode voltage that corresponds, in general, to the base-emitter voltage V_{BE} of a BJT while PTAT voltage is achieved by taking advantage of the thermal voltage V_T that is extracted from the difference of two forward biased diode voltages. These circuits generally consist of two diodes and one operational amplifier in which the required minimum supply voltage and power consumption are set by the selected operational amplifier topology.

In this chapter, two different bandgap voltage reference topologies that use a sampled data amplifier to optimize power consumption are presented. These two topologies use the same bandgap core cell. Its bias current is provided through an LDO and its control circuitry, consisting of a sampled-data amplifier and a compensation circuit (or loop to determine its quiescent output voltage and to reduce the input error voltage due to the temperature). The main difference between these two proposed topologies is that the adopted method determines the quiescent output voltage of the sampled-data amplifier controlling the LDO.

In other words, the quiescent output voltage of the sampled-data amplifier has to be nominally set to the V_{GS} of M_{LDO} (in Figures 4.1 and 4.15) to reduce the input error voltage due to the temperature dependence of the threshold of M_{LDO}. For this purpose, the temperature dependency of quiescent output voltage of the proposed amplifier and the required control voltage for LDO are analysed. In the first proposed bandgap voltage reference topology this temperature dependence problem is solved by biasing the sampled-data amplifier with a CTAT current generator. As a second method, a feedback loop that includes a variable duty-cycle generator circuit controlling the amplification phase (duration time) of the sampled-data amplifier is used. This second feedback loop works to reduce the input error voltage by setting the quiescent output

voltage of the amplifier to the desired value. The details of the methods and proposed sub-blocks circuit implementations are explained in the following sections.

4.1.1 Voltage reference circuit with current regulated loop (CRL)

Figure 4.1 shows the schematic diagram of the circuit. The conventional current mode bandgap [36] is reversed so that the reference voltage is generated across the output resistors R_{OUT}. PMOS transistors M_{P1} and M_{P2} operate in the sub-threshold region to provide the diode-like voltage-current response, as required to give rise to PTAT and CTAT currents. An LDO, consisting of the transistor M_{LDO} and its control circuitry, generates the voltage V_x. The loop equates the two output voltages, V_{O1} and V_{O2}, on output resistors (R_{OUT}) of the bandgap cell. The operation of the LDO incorporates the start-up function, which is always required in bandgap circuits.

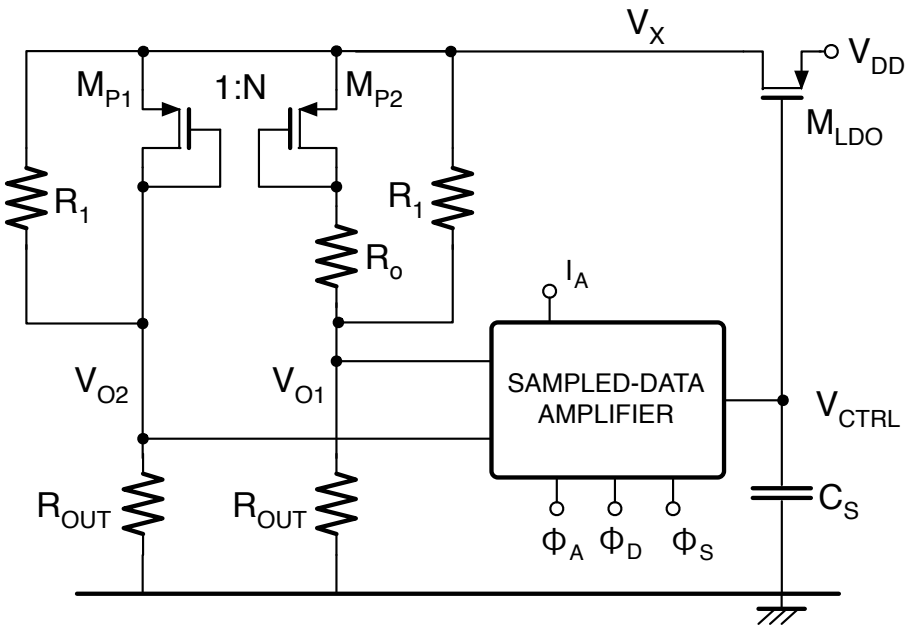

Figure 4.1: Conceptual scheme of proposed circuit topology – Voltage reference circuit with current regulated loop.

The circuit in Figure 4.1 can operate with very low supply voltages. The minimum supply voltage depends on the required output level and a number of practical limits such as limitation coming from each sub-block utilized in the proposed topology. By inspection of Fig. 4.1, it results that:

$$V_{DD} = V_{O2} + |V_{GS,MP1}| + V_{DS,MLDO} \tag{4.1}$$

In the preferred implementation, an output voltage of 200 mV, 300 mV across the PMOS diode, and a voltage drop as low as 100 mV across M_{LDO} lead to a supply voltage down to 0.6 V. This, however, it is not the only and the dominant constraint in the circuit. The dominant one for determining the minimum supply voltage is due to the input stage of the proposed sampled data amplifier since in the used technology, the thresholds of the P-channel and the N-channel transistors are -0.45 V and 0.4 V, respectively. With an overdrive voltage of 50 mV, the minimum supply voltage is, hence, 0.65 V. However, this value increases for low temperatures as the transistors threshold voltage also increases. As a result, the performance of the designed and implemented bandgap reference circuits are obtained while using 0.8 V nominal supply voltage. The design and implementation details of the sub-blocks will be given in following sub-sections.

4.1.1.1 Bandgap Voltage Reference Cell

The reversed version of traditional current-mode bandgap reference architecture in which reference voltage can be scaled [36] is utilized as the bandgap core cell since this design focuses on proposing voltage reference topologies that can work with low supply voltages. The basic principle of operation consists of generating a first order temperature-independent current that, through a resistor, directly provides the output

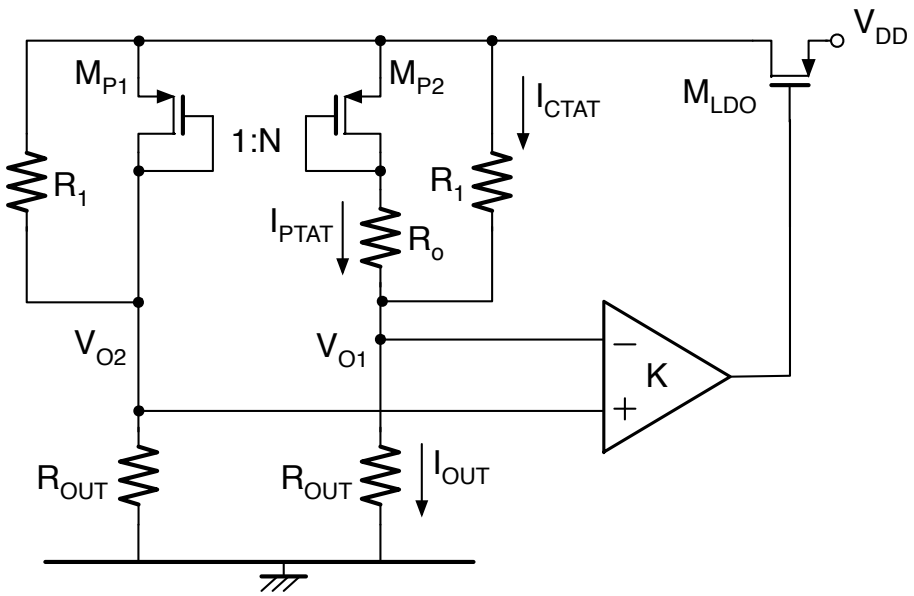

Figure 4.2: Current-mode bandgap voltage reference cell.

reference voltage. As a result, the output reference voltage can be determined by choosing an adequate output resistor value.

The schematic of the designed current-mode bandgap cell with an ideal operational amplifier is shown in Figure 4.2. PMOS transistors (M_{P1} and M_{P2}) are biased to operate in sub-threshold region. The loop established by the operational amplifier makes V_{O1} and V_{O2} equal. As a result, the voltage drop on resistor R_0 is the voltage difference between two diode voltages, which is proportional to the absolute temperature (PTAT), so that a PTAT current is generated through resistor R_0. However, the voltage drop on resistor R_1 is a diode voltage that is complementary to absolute temperature (CTAT) so that a CTAT current is generated through resistor R_1. Finally, the output voltage is obtained by direct transformation of these PTAT and CTAT currents into voltage on output resistors (R_{OUT}). The adopted reversed architecture avoids the use of current mirrors, which are often the source of inaccuracy [65]. The output voltage of the current mode bandgap is given by

$$V_{O1} = \frac{R_{OUT}}{R_1}\left[V_{GS1} + \frac{R_1}{R_0} nV_T \ln(N)\right] \tag{4.2}$$

The bandgap core cell shown in Figure 4.2 has been designed and simulated using a 0.18 μm standard CMOS process. In the implementation of the bandgap core, the

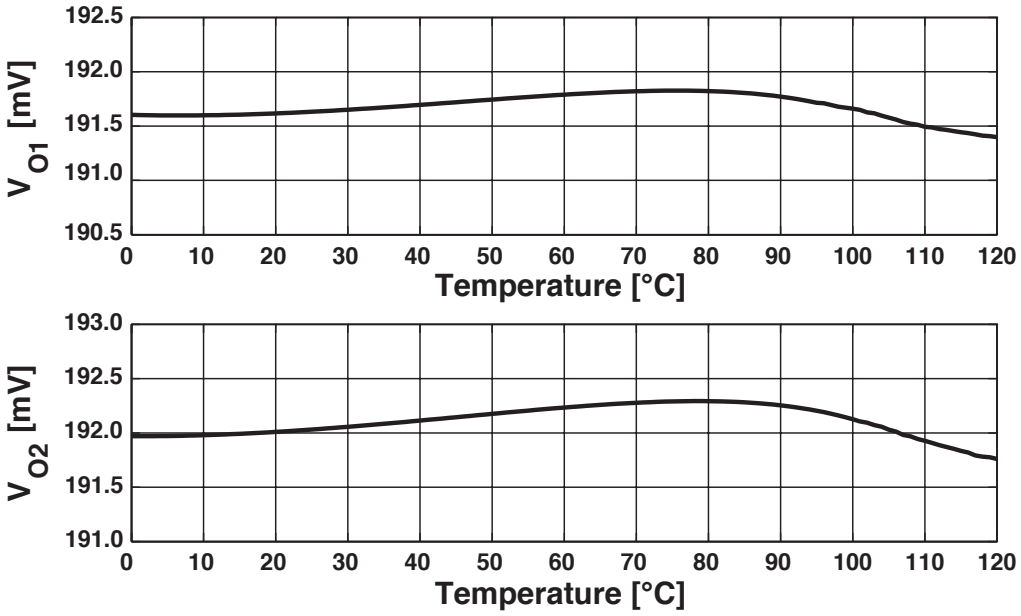

Figure 4.3: Simulated output voltages of bandgap reference core cell as a function of temperature.

ratio between the aspect ratios of M_{P1} and M_{P2} is chosen as $N = 16$. The currents flowing through the diodes are 100 nA from 0.6 V nominal supply voltage. An ideal operational amplifier with DC gain (K in Figure 4.2) of 40 dB is used while designing and optimizing the bandgap core cell and output resistors are R_{OUT} = 1.1 MΩ to have an output reference voltage of 200 mV.

Figure 4.3 shows the simulated output voltages as a function of the temperature in the range from 0 to 120 °C. The obtained output reference voltages are 191.6 mV and 192.1 mV with temperature coefficients of 18 ppm/°C and 23 ppm/°C, respectively, where $R_1/R_0 = 3.6$. The total current consumption of the bandgap core cell is 350 nA.

Figure 4.4 shows the layout of the designed bandgap core cell in which most of the area is occupied by resistors. Indeed, their values are on the order of mega Ohms to have the current in the order of hundreds of nano Amperes. The active area is 450 x 430 μm^2.

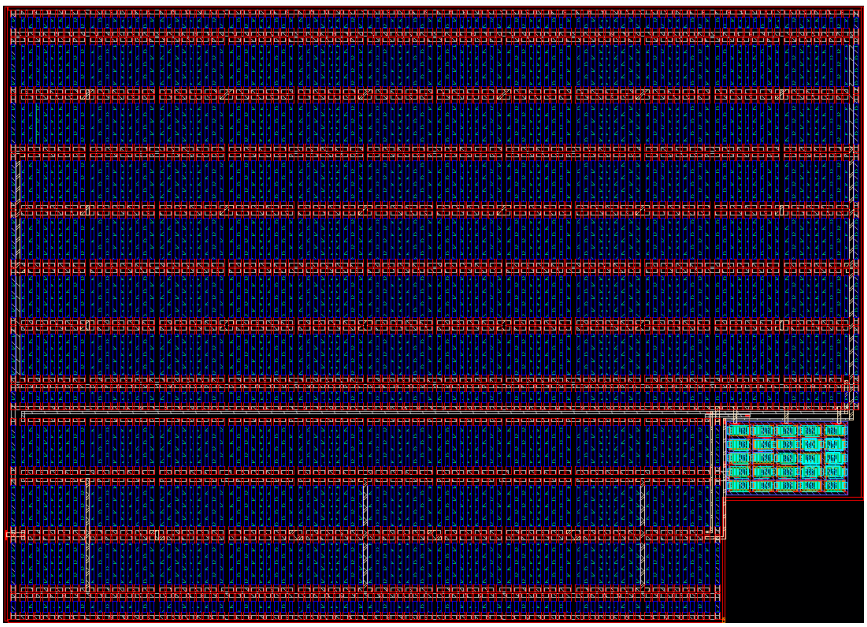

Figure 4.4: Layout of the bandgap reference core cell.

4.1.1.2 Sampled-data amplifier

When the signal band is small, like in the case of a bandgap circuit, it can be convenient to use sampled-data operation. There are many examples of sampled-data systems for realizing filtering functions or for data conversion [66–68]. In this case, the sampled data technique is utilized even at the op-amp level. It results in the output voltage of the op-amp changing in a discrete manner under the control of a clock with a frequency higher than the frequency of the system. However, since the proposed voltage reference

circuit is a continuous system, it is not setting an operation frequency limitation for the op-amp.

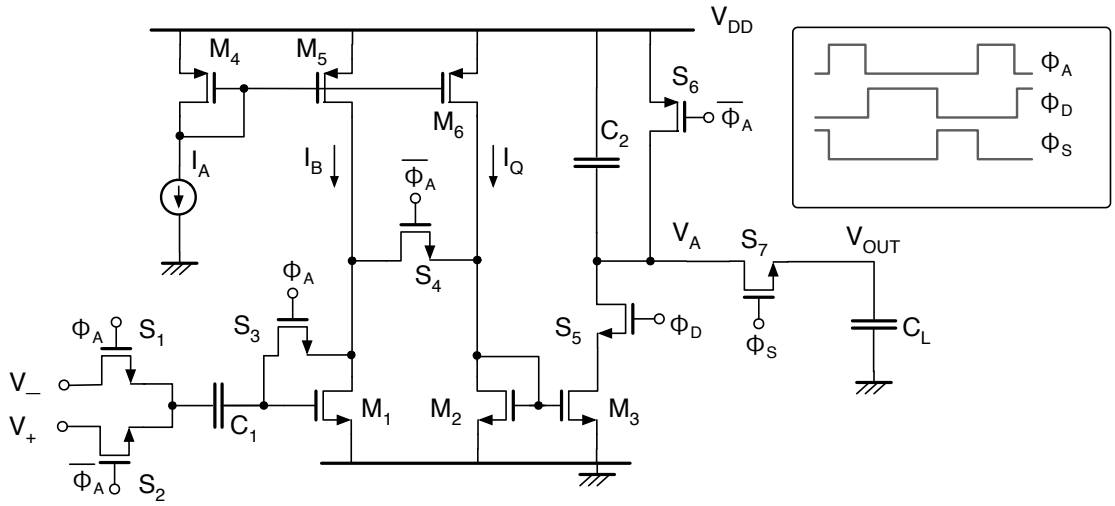

Figure 4.5: Schematic diagram of the sampled-data amplifier.

Figure 4.5 shows the used sampled-data amplifier. It operates under the control of three phases. The first phase, Φ_A, connects the input transistor M_1 in the diode configuration to charge the auto-zero capacitor C_1 to V_- minus the V_{GS} of the input transistor M_1. The second phase, Φ_D, is the amplification phase. The signal current, i_d, flows through the switch S_4 into M_2 and mirrored to charge the capacitor C_2 for the fixed time set by Φ_D. The bias current I_Q determines the quiescent discharge voltage. The switched capacitor output structure, controlled by Φ_S, provides the output. The differential inputs and the transconductance of the input transistor M_1, which operates in sub-threshold region, give rise to the charging signal current:

$$i_d = g_{m_1}(V_+ - V_-) = \frac{I_B}{nV_T}(V_+ - V_-) \tag{4.3}$$

where I_B is the current in M_1, n the sub-threshold region slope and V_T the thermal voltage.

It is easy to verify that the DC gain of the sampled-data amplifier of Figure 4.5 is

$$A_0 = \frac{i_d T_D}{C_2} = \frac{I_B}{nV_T}\frac{T_D}{C_2} \tag{4.4}$$

which depends on three parameters: the bias current in M_1, the charge time, T_D, and the value of C_2. For $I_B = 100$ nA, $T_D = 10$ μs and $C_2 = 0.15$ pF, the calculated gain is around 40 dB.

The quiescent output voltage, V_Q, depends on the quiescent current I_Q, the charge time and the value of C_2. If the signal current is zero, V_Q is

$$V_Q = V_{DD} - \frac{I_Q T_D}{C_2} \tag{4.5}$$

that, for $V_{DD} = 0.6$ V and the above used parameters, leads to $I_Q = 5$ nA to obtain $V_Q = V_{DD}/2$.

The circuit of Figure 4.5 has been designed and simulated at the transistor level using a 0.18-μm CMOS technology ($V_{th,n} = 0.4$ V, $V_{th,p} = -0.45$ V). The current in the bias generator M_4 is 10 nA with $W/L = 4$. The aspect ratios of transistors M_5 and M_6 are 40 and 2, respectively, to have nominal currents $I_B = 100$ nA and $I_Q = 5$ nA. The capacitor C_1 used for storing the input offset during the auto-zero period is 2 pF. The clock frequency is 50 kHz ($T = 20$ μs) with auto-zero phase, Φ_A, 25% and amplification phase, Φ_D, 50% of the clock period.

The switches are realized by single NMOS or PMOS transistors. In order to ensure a low on resistance, the amplitude of the phase controlling the NMOS switches is 1 V. Therefore, switches S_1 and S_2 operate properly while the common mode input voltage is 0.3 V. Any other input common mode value can be admitted, provided that the two switches are working as required. Table 4.1 gives the transistors sizes of this 0.18-μm CMOS design.

Table 4.1: Transistor sizes of the sampled-data amplifier.

Transistor	**W/L**
M_1	100 μm / 1 μm
M_2, M_3	5 μm / 1 μm
M_4	20 μm / 5 μm
M_5	200 μm / 5 μm
M_6	10 μm / 5 μm
S_1, S_2, S_7	0.22 μm / 0.18 μm
S_4, S_5, S_6	5 μm / 0.18 μm

The accuracy of the DC gain depends on the accuracy of the Φ_D period. A possible jitter in T_D, δT_D, changes the gain by δA_0. The sensitivity is

$$\frac{\delta A_0}{A_0} = \frac{\delta T_D}{T_D} \tag{4.6}$$

which is very low for the designed value of T_D (=10 μs) and the jitter of a normal phase generator.

It is possible to increase the DC gain by changing the design parameters of **4.4** or by increasing the mirror factor between M_2 and M_3. Since even the bias current I_Q augments, it is necessary to compensate for its effect on the output stage with an additional branch. The transistor M_7 supplies a current $(N-1)I_Q$ as shown in Figure 4.6 to set the quiescent current used to charge C_2 to the expected value I_Q.

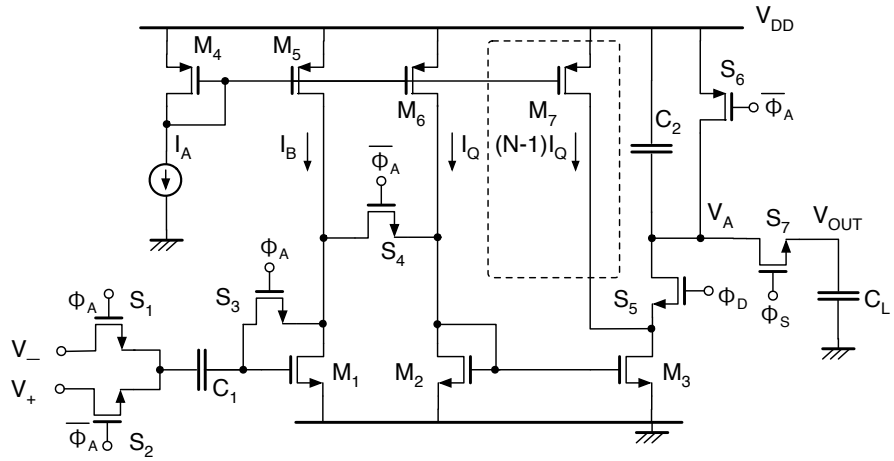

Figure 4.6: Schematic diagram of the sampled-data amplifier with the modification to increase the gain.

The transient level simulations confirm the expected circuit operation. The supply voltage is 0.6 V and, with zero differential input signal, the output voltage becomes 301 mV. Figure 4.7 shows the discharge transients of C_2 for various differential inputs.

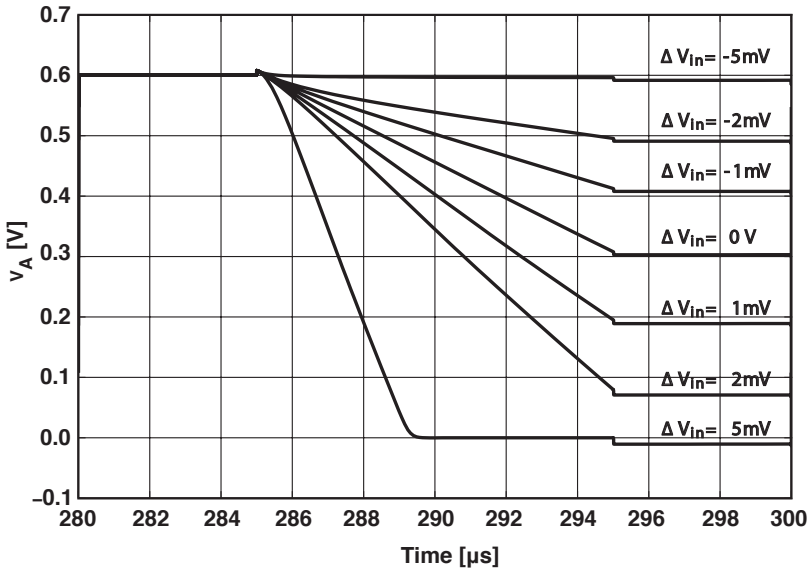

Figure 4.7: Simulated discharge transients for various differential inputs.

When the differential input voltage is more than $\pm$ 3.5 mV, the output almost saturates to the supply levels. The behaviour is slightly asymmetrical. The switching off of S_6 and the switching on of S_7 cause limited clock feedthrough, as shown in Figure 4.7. This corresponds to a small input referred offset, which is negligible for this design. When the switches do not work properly, for instance when the amplitude of the clock phase is reduced to 0.6 V, the circuit performance worsens significantly. Having a good overdrive for the transistors that realize the switches is essential. For this reason, the phases must have a relatively large amplitude.

The input-output characteristic of the sampled-data amplifier is given in Figure 4.8 (a). With a negative signal current, the charge drained from C_2 diminishes and the output voltage ($V_A = V_{DD} - V_{C2}$) increases. A positive signal current speeds up charging and the output voltage becomes smaller. The asymmetry of the response is evident from Figure 4.8 (b), which shows the small signal gain. The maximum gain is more than 42 dB. The use of the pseudo-differential version shown in Figure 4.9 (a) leads to the

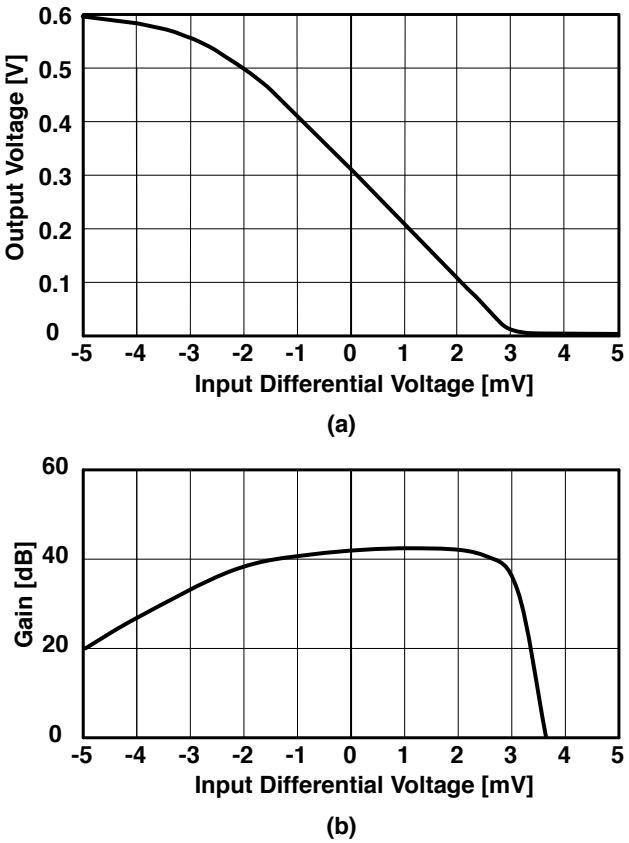

Figure 4.8: (a) Simulated amplifier input-output characteristic. (b) Differential gain as a function of the input differential voltage.

symmetrical gain curve of Figure 4.9 (b). The peak gain is 48.2 dB at the cost of doubling the power consumption.

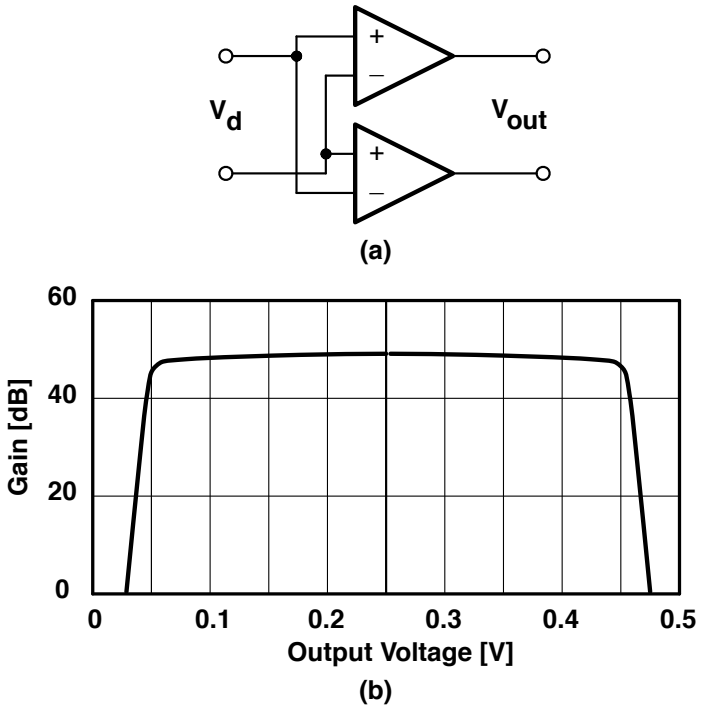

Figure 4.9: (a) Pseudo-differential configuration. (b) Small signal differential gain as a function of the output voltage.

Periodic steady state and periodic AC analysis estimate the frequency response of the sampled-data amplifier. The gain and the phase plots of the single ended version are shown in Figure 4.10. The DC gain is 42.45 dB and the bandwidth is 2.5 kHz. Since the clock frequency is 50 kHz, there are zeros at that frequency and its multiples.

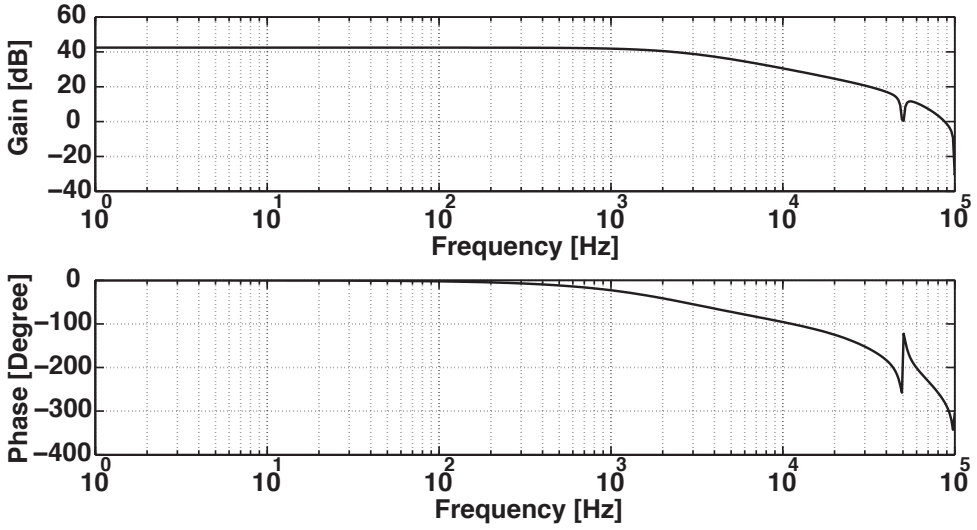

Figure 4.10: Simulated frequency response of the sampled-data amplifier.

The power supply rejection ratio performance is around -40 dB, as shown in Figure 4.11, which is poor since any variation of the supply voltage becomes an equal variation at output. The obvious recommendation is using the pseudo-differential configuration that increases the DC gain by 6 dB, but, more importantly, this modification rejects spurs coming from the power supply.

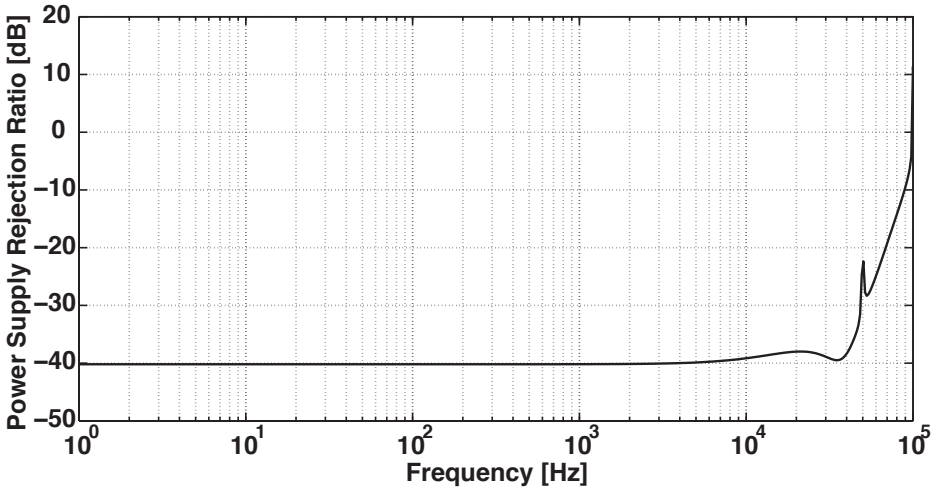

Figure 4.11: Simulated power supply rejection ratio of the sampled-data amplifier.

Temperature variation of the quiescent output voltage, V_Q, of the sampled-data amplifier is given in Figure 4.12. Temperature coefficient of the quiescent output voltage is -0.33 %/°C. The negative sign of TC means that quiescent discharging current, I_Q, is increasing with temperature. This is an expected result due to threshold voltage variation of PMOS transistors used in the current mirror that provides the

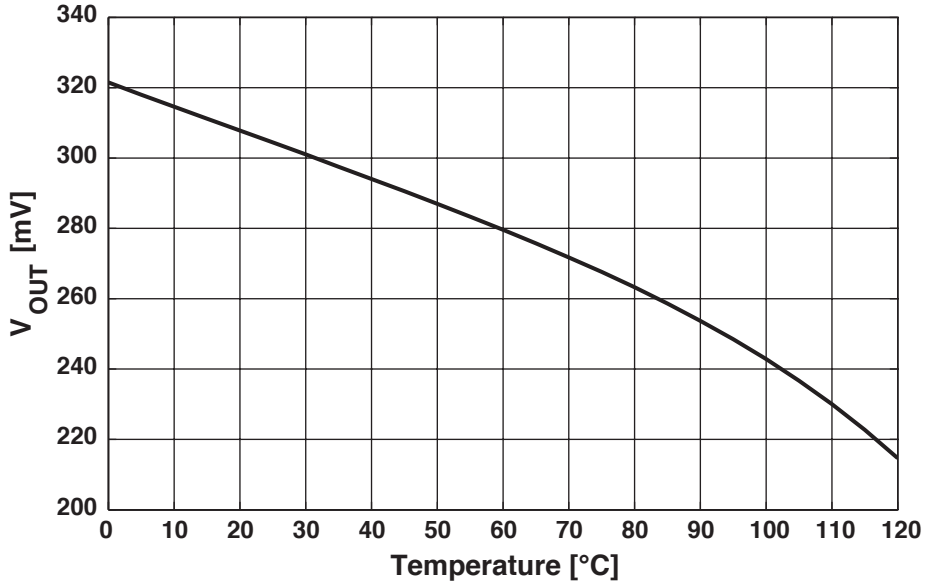

Figure 4.12: Simulated quiescent output voltage of sampled-data amplifier as a function of temperature.

circuit bias current. It is, indeed, well known that the transistor threshold voltage decreases with a temperature increase. As seen from **4.5**, there are three design variables, I_Q, T_D, C_2, that determine the value of V_Q. For the temperature dependence of V_Q, one of these three parameters can be modified.

In this study two different methods are proposed and implemented in two different voltage reference topologies. The first method consists in biasing the sampled-data amplifier biased with a CTAT current. This compensates for the charging quiescent current I_Q temperature dependence. The second method is based on modifying the charge time, T_D, using a variable duty-cycle generator for the amplification phase.

4.1.1.3 CTAT current generator

In the proposed voltage reference topology, the approach consists in biasing the sampled-data amplifier with a CTAT current in order to compensate for the temperature dependency of the quiescent output voltage of the sampled-data amplifier, which controls the M_{LDO}. For this purpose, a CTAT current generator is designed whose schematic diagram is shown in Figure 4.13.

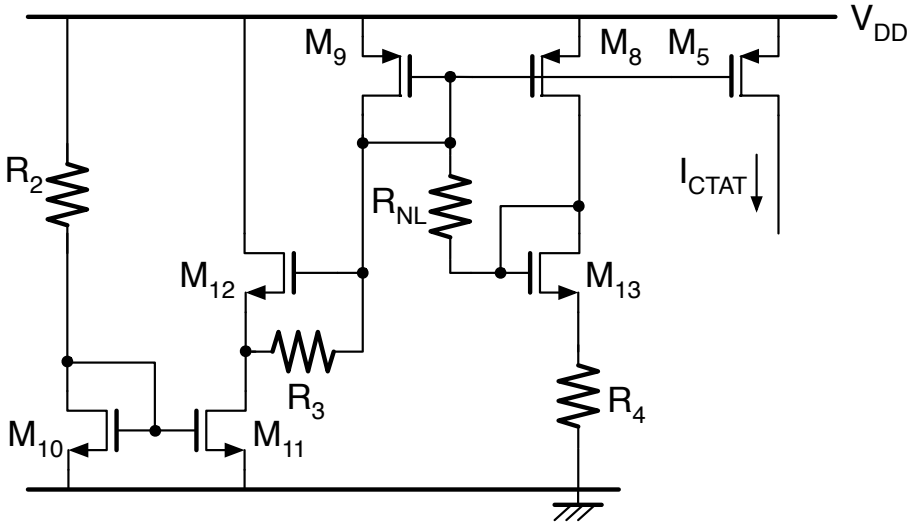

Figure 4.13: Schematic of CTAT current generator.

In the circuit, a CTAT current is generated on R_3 through the V_{GS} voltage of transistor M_{12}. M_8, M_{13} and R_{NL} compensate for the high temperature nonlinearity of generated CTAT current. Resistor R_4 is added to have the same biasing conditions for M_{12} and M_{13}. The absolute value of the CTAT current can be adjusted through the resistor R_3,

as follows:

$$I_{CTAT} = V_{GS,12} / R_3 \tag{4.7}$$

Table 4.2 shows the transistor sizes and resistor values in the designed CTAT generator. The simulated temperature variation of the designed CTAT current generator is given in Figure 4.14. The nominal output current is 100 nA with temperature coefficient equal to -0.37 %/°C.

Table 4.2: Transistor sizes and resistor values of CTAT generator.

Component	Size/Value
M_8, M_9	20 μm / 5 μm
M_{10},M_{11}	2 μm / 5 μm
M_{12}, M_{13}	100 μm / 0.35 μm
R_2	5 M Ω
R_3	15 M Ω
R_4	7.5 M Ω
R_{NL}	150 M Ω

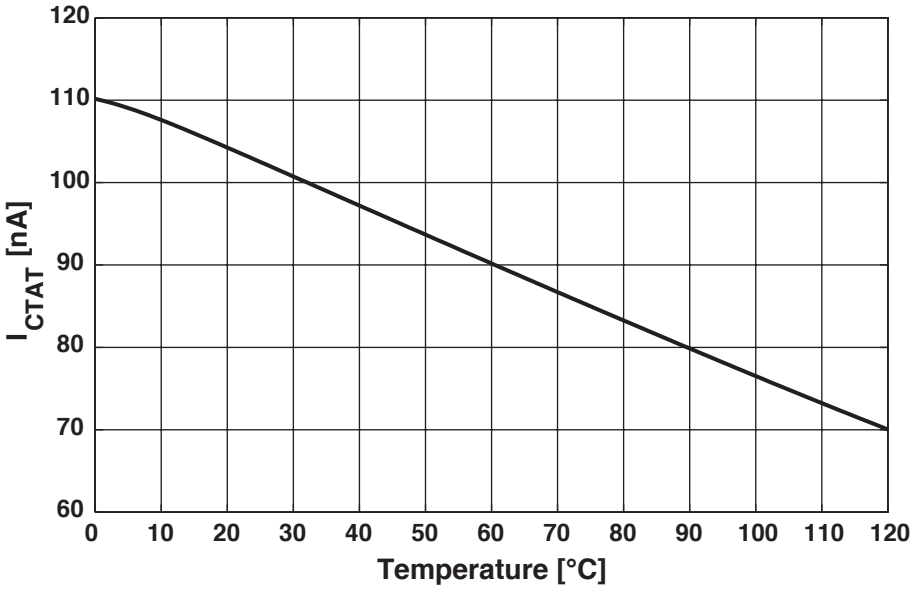

Figure 4.14: Simulated temperature variation of designed CTAT current.

4.1.2 Voltage reference circuit with duty-cycle regulated loop (DCRL)

Figure 4.15 shows the schematic diagram of the proposed voltage reference topology. As seen from the figure, this circuit uses the same bandgap reference cell and sampled-data amplifier included in the architecture described in Section 4.1.1.

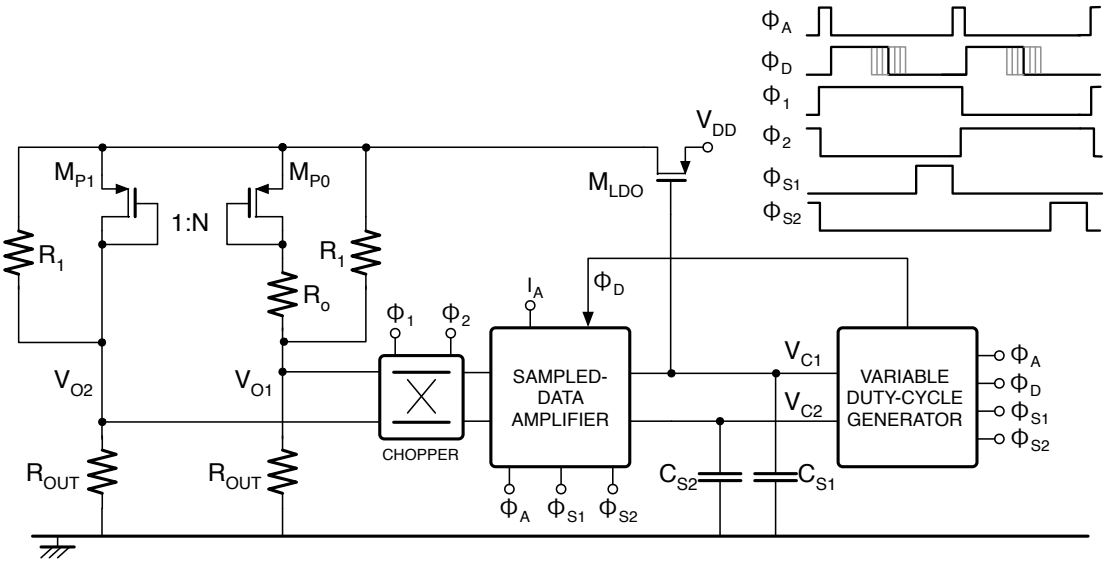

Figure 4.15: Conceptual scheme of the proposed circuit topology – Voltage reference circuit with duty cycle regulated loop.

However, in this topology, by using a chopper method at the input of the sampled-data amplifier, two different output voltages are generated with respect to the differential input in each phase, Φ_1 and Φ_2. The scheme includes two feedback loops. The first is established by the sampled-data amplifier which controls the gate terminal of transistor M_{LDO}. The second uses a variable duty-cycle generator to determine the amplification phase duration of the sampled-data amplifier in order to properly control its output voltage level. The two loops act together to bring the control voltage of M_{LDO} to the optimum value in order to minimize the input error voltage. This happens when the two bandgap output voltages V_{O1} and V_{O2} are equal.

The circuit in Figure 4.15 can operate with very low supply voltages as well. An output voltage of 200 mV, about 300 mV across the M_P transistors, and a voltage drop as low as 100 mV across M_{LDO} lead to a supply voltage down to 0.6 V. However, same practical limitations are valid again due to the output swing and input stage of the sampled-data amplifier.

As mentioned before, the scheme includes the same bandgap reference core cell and sampled data amplifier are utilized in the reference topology described in Section 4.1.1; therefore, their design and implementation details will not be described in this section again to prevent repetitions. The design and implementation details of the variable duty-cycle generator and of the circuit phase generator will be given in following sections.

4.1.2.1 Variable duty-cycle generator

Figure 4.16 shows the schematic diagram of the proposed sampled-data based variable duty-cycle generator. The operation principle of the variable duty-cycle generator is quite similiar to the one of the sampled-data amplifier without sampling phase. There are two phases of operation. The first phase, $\overline{\Phi_A}$, connects the input transistor M_7 in the diode configuration to charge the auto-zero capacitor C_3 to V_- minus the V_{GS} of the input transistor M_7. In the second phase, Φ_A, the signal current, i_d, flows through the switch S_{12} into M_8 and is mirrored to charge the capacitor C_4. The voltage on this node, V_{CAP}, is not sampled as in the sampled-data amplifier case, but is compared with the threshold voltage of M_{13}. The result at the node V_{PHI} square wave properly amplified with inverters to generate Φ_D at the output. The total duration time of the generated phase signal, Φ_D, includes also the auto-zero duration time, however effective duration time (charge time of C_4), T_D, will be the difference between Φ_D and Φ_A. The bias current I_Q determines the quiescent duration time, T_D, of the generated square wave.

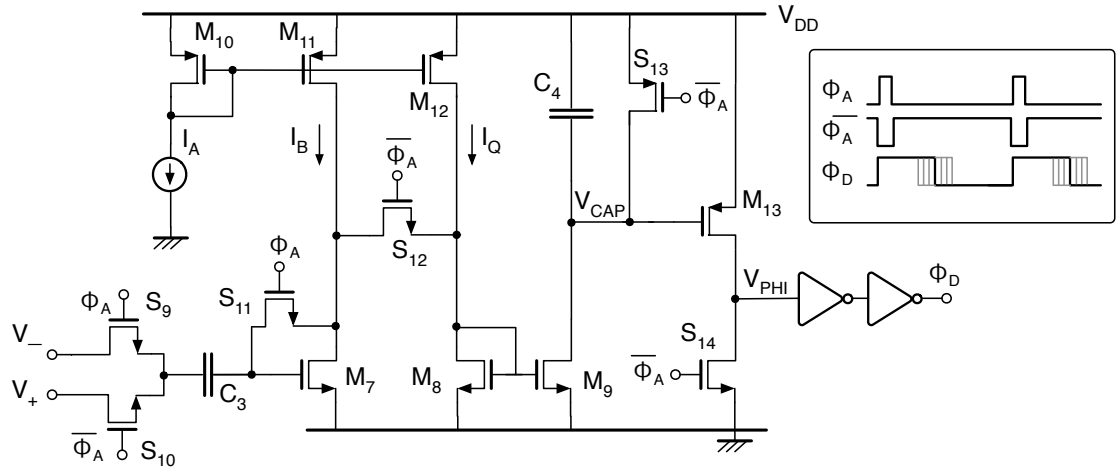

Figure 4.16: Schematic diagram of the variable duty-cycle generator.

The input differential voltage and the transconductance of the input transistor M_7, which operates in sub-threshold region, gives rise to the charging signal current:

$$i_d = g_{m_7}(V_+ - V_-) = \frac{I_B}{nV_T}(V_+ - V_-) \tag{4.8}$$

where I_B is the current in M_7, n the sub-threshold region slope and V_T the thermal voltage.

The change in the duration time of the proposed duty-cycle generator with respect to the input differential voltage can be expressed as

$$\frac{\delta T_D}{\delta (V_+ - V_-)} = \frac{C_4}{i_d} = \frac{nV_T}{I_B} C_4 \tag{4.9}$$

which depends on two parameters: the bias current of M_7 and the value of C_4. For $I_B = 100$ nA and $C_4 = 0.15$ pF, the calculated gain is about 50 ns/V.

The quiescent duration time $T_{D,Q}$, depends on the quiescent current I_Q, the threshold voltage $V_{th,p}$ and the value of C_4. If the signal current is zero, $T_{D,Q}$ is

$$T_{D,Q} = \frac{C_4 |V_{th,p}|}{I_Q} \tag{4.10}$$

In order to achieve $T_{D,Q} = T/2$, considering $T = 20$ μs, $|V_{th,p}| = 0.45$ V and C4 = 0.15 pF, the quiescent current, I_Q, turns out to be equal to 5 nA.

The current in the bias generator M_{10} is 10 nA with $W/L = 4$. The aspect ratios of transistors M_{11} and M_{12} are 40 and 2, respectively, to have nominal currents $I_B = 100$ nA and $I_Q = 5$ nA. The capacitor C_3 used for storing the input offset during the auto-zero period is 2 pF. The clock frequency is 50 kHz ($T = 20$ μs) with auto-zero phase, Φ_A, 25% of the clock period ($T_A = 5\mu$s).

The switches are realized by single NMOS or PMOS transistors. In order to ensure a low on resistance, the amplitude of the phase controlling the NMOS switches is 1 V which requiers a simple clock boost on chip. Therefore, switches S_9 and S_{10} operate properly while the common mode input voltage is 0.3 V. Any other input common mode value can be admitted, provided that the two switches are working as required. Table 4.3 gives the transistors sizes of this 0.18-μm CMOS design.

Table 4.3: Transistor sizes of variable duty-cycle generator.

Transistor	**W/L**
M_7	100 μm / 1 μm
M_8, M_9	5 μm / 1 μm
M_{10}	20 μm / 5 μm
M_{11}	200 μm / 5 μm
M_{12}	10 μm / 5 μm
M_{13}	50 μm / 5 μm
S_9, S_{10}	0.22 μm / 0.18 μm
S_{11}, S_{12}, S_{13}, S_{14}	5 μm / 0.18 μm

Transient simulations confirm the expected circuit operation. The supply voltage is 0.6 V and, with zero differential input signal, the output phase duration becomes 10 μs. Figure 4.17 shows the discharge transient of C_4 and generated phase signal, Φ_D for various input differential voltage values. When the differential input voltage is higher than 3 mV, the output almost saturates to the clock period. The behaviour is asymmetrical. When the switches do not work properly, for instance when the amplitude of the clock phase is reduced to 0.6 V, the circuit performance worsens significantly. Having a good overdrive for the transistors that realize the switches is essential. For this reason, the phases must have a relatively large amplitude.

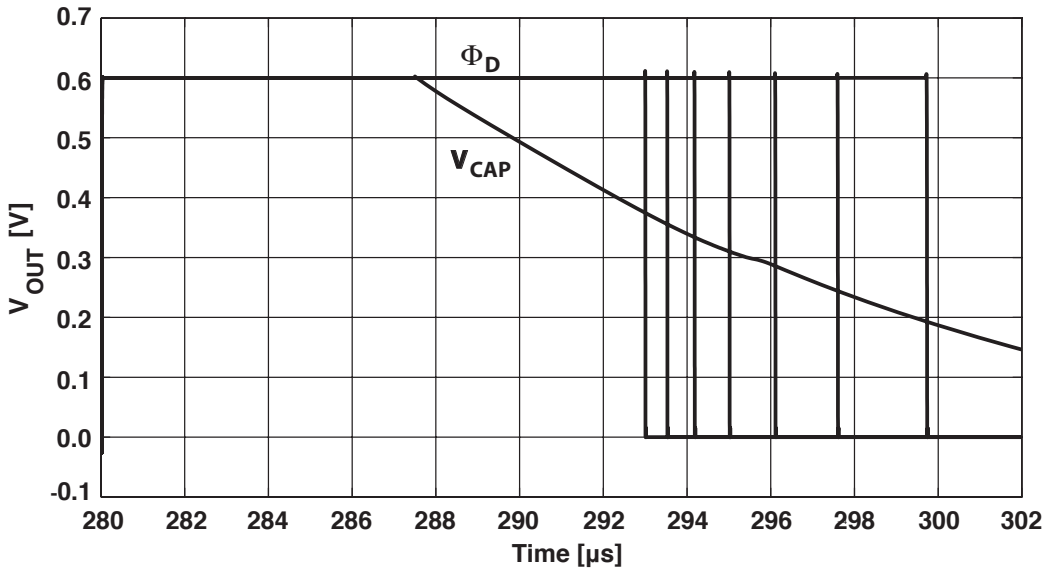

Figure 4.17: Simulated output phase duration for various differential inputs.

The simulated circuit input-output characteristic is given in Figure 4.18. Note that, with a negative signal current, the current charging capacitor C_4 diminishes, thus increasing the time required to the voltage V_{CAP} for crossing the value $V_{DD} - |V_{th,p}|_{M_{13}}$. This results in an increase of the duration time (duty-cycle) of the generated phase. A positive signal current, on the contrary, speeds up charging C_4 and the duration time of the output phase becomes smaller.

Figure 4.19 shows the simulated quiescent duration time, $T_{D,Q}$, as a function of the temperature in the range from 0 to 120 °C. The negative slope of the curve is due to two effects, both ascribed to the transistors threshold temperature dependence. A variation in the threshold of transistors composing the current mirror which provides the quiescent bias current causes an increase of the latter with a temperature increase.

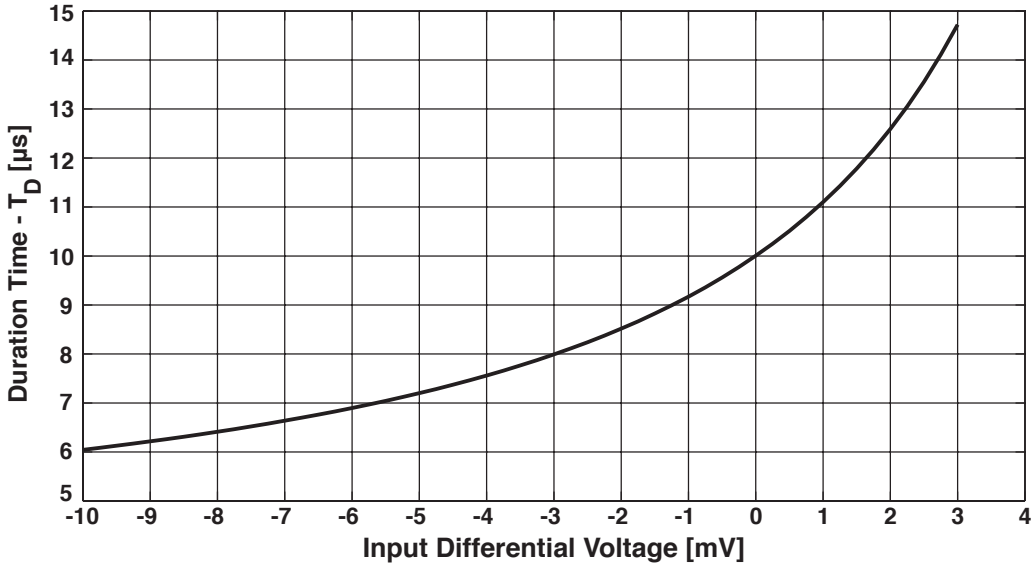

Figure 4.18: Simulated variable duty-cycle generator input-output characteristic.

Threshold temperature dependence of transistor M_{13} directly modifies the output transition point which determines the output phase duration.

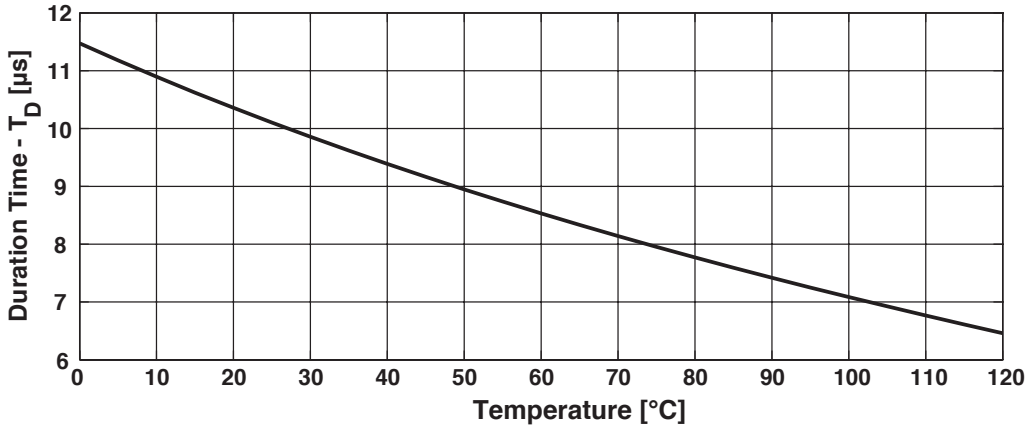

Figure 4.19: Simulated duration time of the generated output phase as a function of the temperature.

4.1.2.2 Generation of the phases of operation

Figure 4.20 shows the schematic diagram of the digital logic utilized in order to generate the phases of operation of the proposed circuit given in Figure 4.15. As seen from the figure, in the proposed phase generator circuit, three input signals required. The first one of them is so called auto zero phase Φ_A for the sampled data amplifier. The second one is *ENB* which is a square wave with a frequency of half of the clock frequency. In the preferred implementation, Φ_A and *ENB* signals are externally provided to the circuit. The last one is the Φ_D which is determining the duration time of the amplification phase and provided by the designed variable duty-cycle

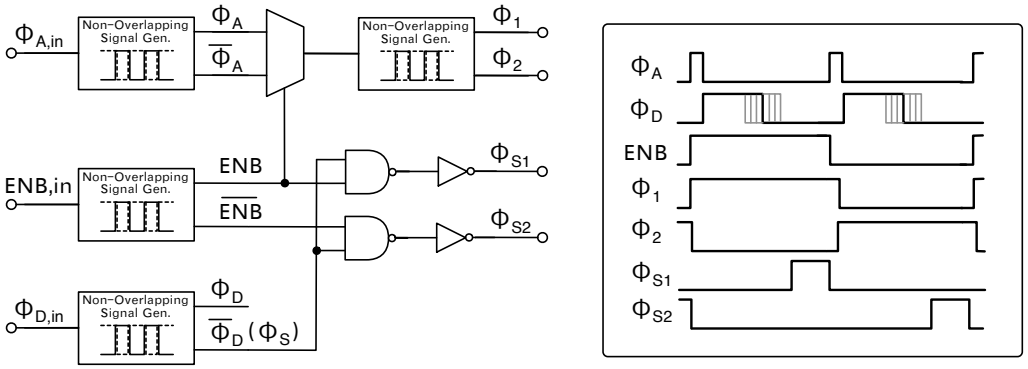

Figure 4.20: Schematic diagram of the digital logic used for generating phases of operation.

generator circuit given in the previous section. Note that the non-overlapping signal generator block is conventional one which is formed by standard digital gates (NAND and inverter).

4.2 Top-Level Simulation and Experimental Results

The presented voltage reference topologies are designed, simulated and fabricated in a standard 0.18 μm CMOS technology with 6 metal and 2 poly layers. This section describes and discusses the top level schematics, chip micrographs and the simulation and experimental results of the designed two voltage reference circuits. During the measurements, a Thermo-Stream T-2800 has been used to control the temperature of the device under test. In order to generate phase signals Φ_A and Φ_D for the circuit described in Section 4.1.1 and Φ_A and ENB for the the circuit described in Section 4.1.2, an arbitrary pulse generator has been used. The output voltages of the BGRs are sampled by means of 6.5 digit multimeter.

4.2.1 Voltage reference circuit with current regulated loop (CRL)

In Figure 4.21 and Figure 4.22, the top-level schematic and chip micrograph of the voltage reference circuit with current regulated loop are shown, respectively. The circuit occupies the area of 450 x 430 μm^2 in which the active area, dominated by the resistors used in the CTAT current generator. The adopted approach consists of compensating for the temperature dependency of sampled-data amplifier output voltage biasing the sampled-data amplifier with a CTAT current.

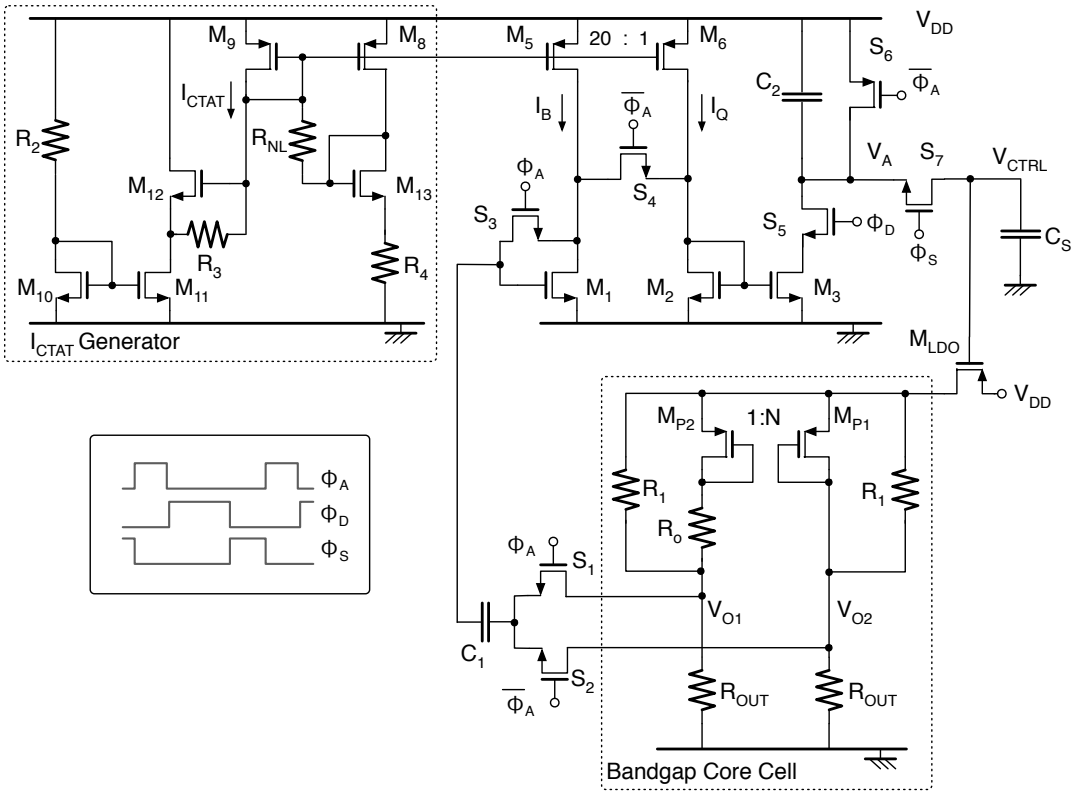

Figure 4.21: Top-level schematic diagram of the voltage reference with current regulated loop.

The circuit in Figure 4.21 has been simulated and measured with a clock frequency of 50 kHz where the auto-zero phase, Φ_A, and the amplification phase, Φ_D, are 25 % and

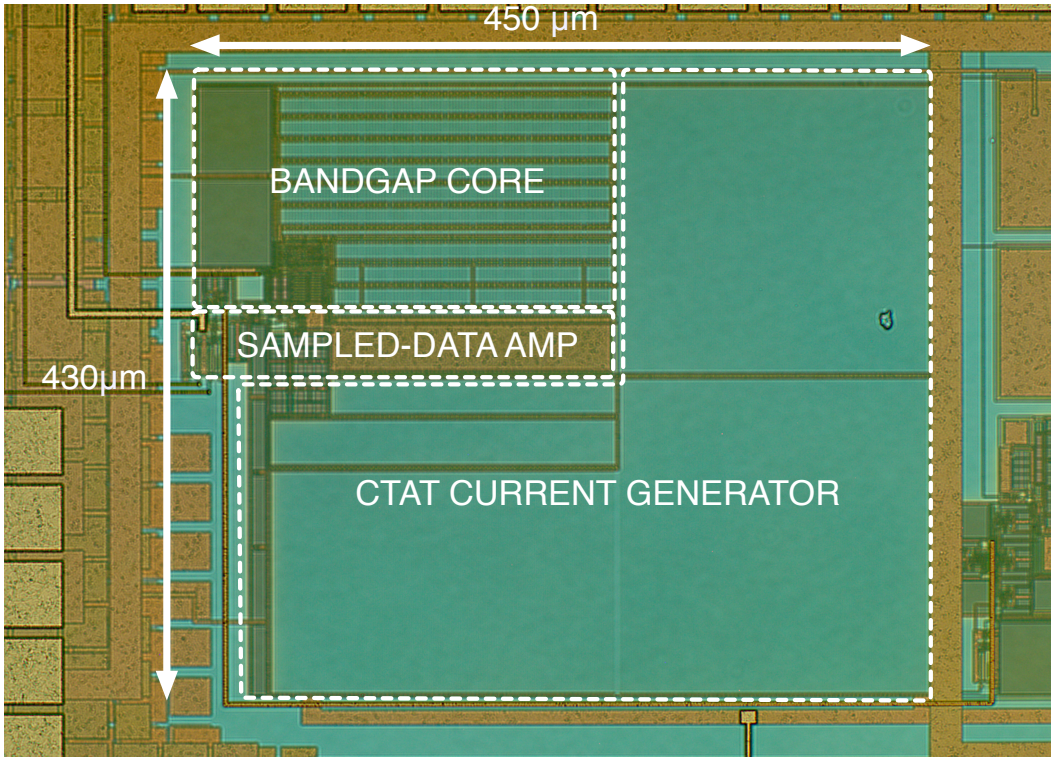

Figure 4.22: Chip micrograph of the voltage reference with current regulated loop.

50 % of clock period, respectively. Figure 4.23 shows the measured output voltage as a function of temperature for different supply voltages. For the higher values of threshold voltages of the input switches of the sampled data amplifier and of M_{LDO}, the circuit is not working at 0.6 V. It starts working at a supply level of 0.65 V and fully working at 0.8 V for the temperature range 0 °C to 120 °C. The circuit achieves 193.1 mV output voltage with a TC of 43 ppm/°C for this temperature range.

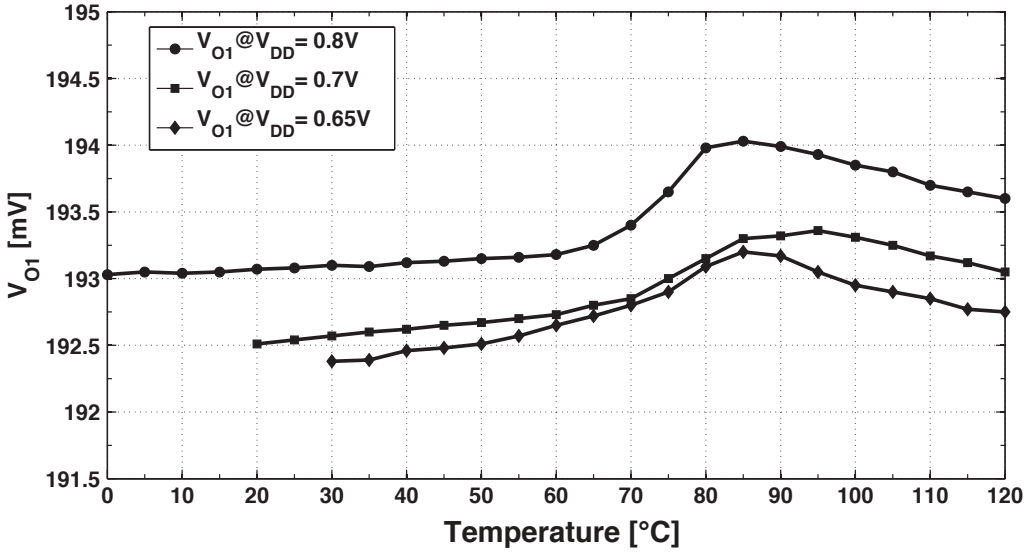

Figure 4.23: Measured output voltage of CRL as a function of the temperature for different supply voltages.

However, the same performance holds for lower supply voltages 0.7 V and 0.65 V with limited temperature ranges where the difference between output voltages V_{O1} and V_{O2} is less then 1 mV. Since for low supply and low temperature, the loop control does not work properly, the experimental data is not provided for the entire temperature range. The reason is that the threshold voltage of the transistors is higher than the value predicted by the simulations at low temperatures.

Figure 4.24 shows the top-level simulated output voltage of the sampled-data amplifier, V_{CTRL}, controlling the gate of M_{LDO} as a function of the temperature. The negative slope of the quiescent output voltage of the amplifier with respect to temperature given in Figure 4.12 becomes positive after current regulation. A positive slope is, indeed, required to compensate for the threshold voltage temperature dependence of transistor M_{LDO} that controls the current in the bandgap core cell.

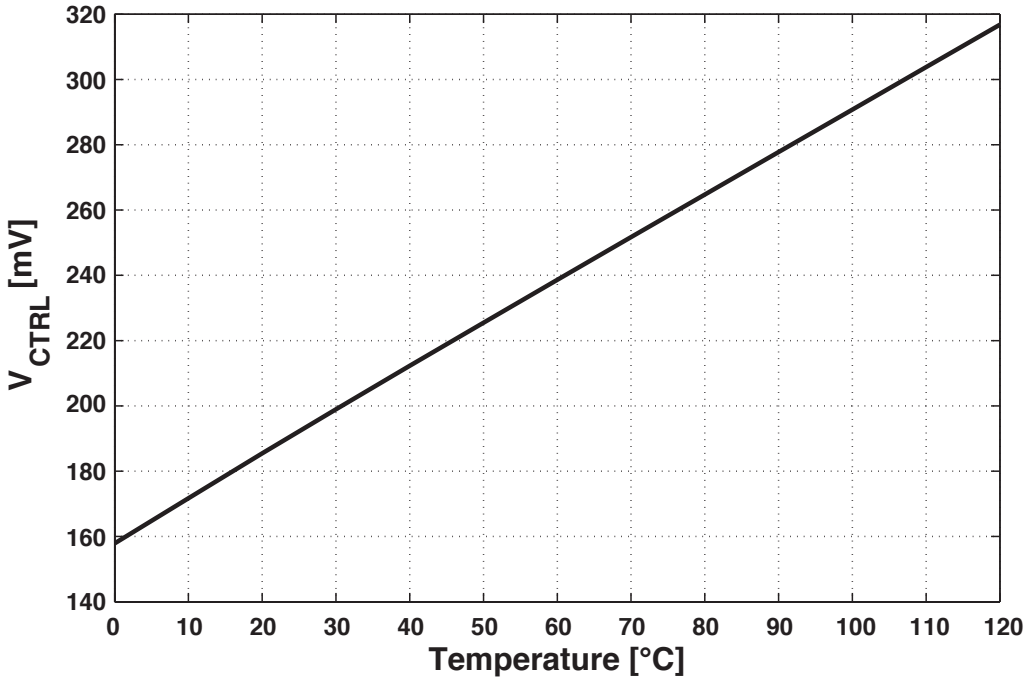

Figure 4.24: Simulated temperature variation of sampled data amplifier output in current regulated loop.

Figure 4.25 shows the measured power supply rejection (PSR) with a 0.8 V supply voltage. The output is filtered with a 6 pF capacitor. The PSR is -50 dB at 100 Hz and -36 dB at 10 MHz.

Figure 4.26 plots the supply current as a function of the temperature when the supply voltage is 0.8 V. Thanks to the CTAT biasing of the control circuit, it changes only by 2 % over the entire temperature range. The average value of the supply current is

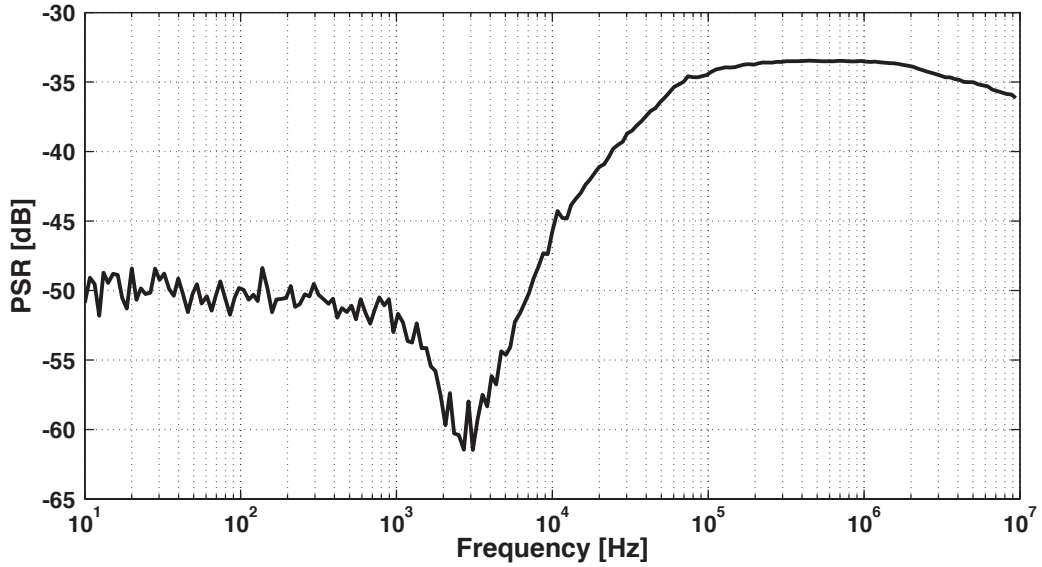

Figure 4.25: Measured power supply rejection (PSR) of CRL.

491.8 nA. At room temperature, the supply current is about 490 nA leads to the power consumption of 390 nW.

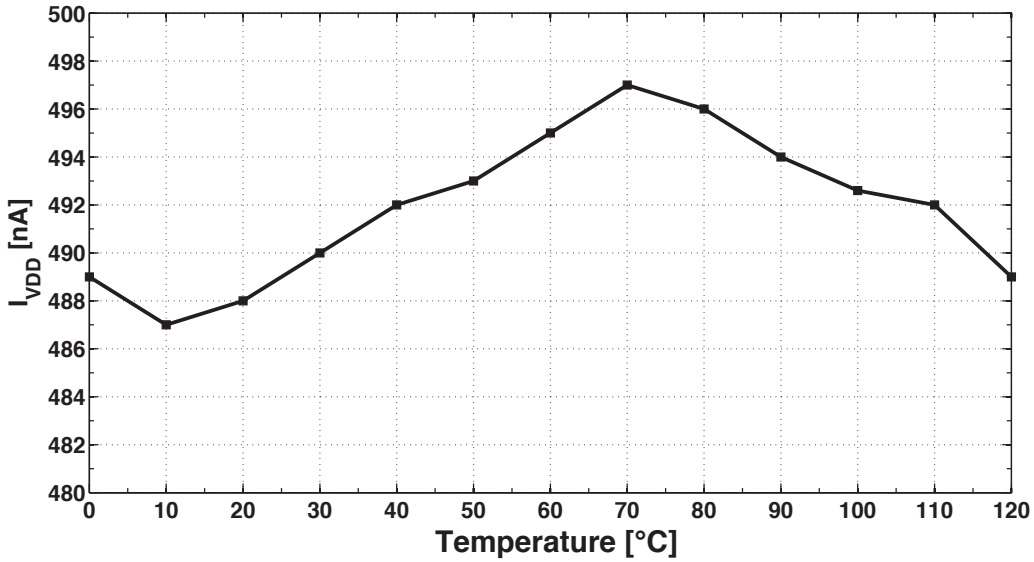

Figure 4.26: Measured supply current as a function of the temperature of CRL.

Figure 4.27 shows the distribution of the output voltage level for the 20 available samples without any device trimming or phase duty-cycle calibration. Measurements have been collected at room temperature, with a supply voltage equal to 0.8 V and a duty cycle of Φ_D equal to 50 %. The mean value is 192.96 mV while the standard deviation is 0.53 mV. The 3 σ inaccuracy is 0.8 %. This is due to chip-to-chip mismatches; calibration of the duty cycle of Φ_D can reduce the inaccuracy to less than 0.1 %.

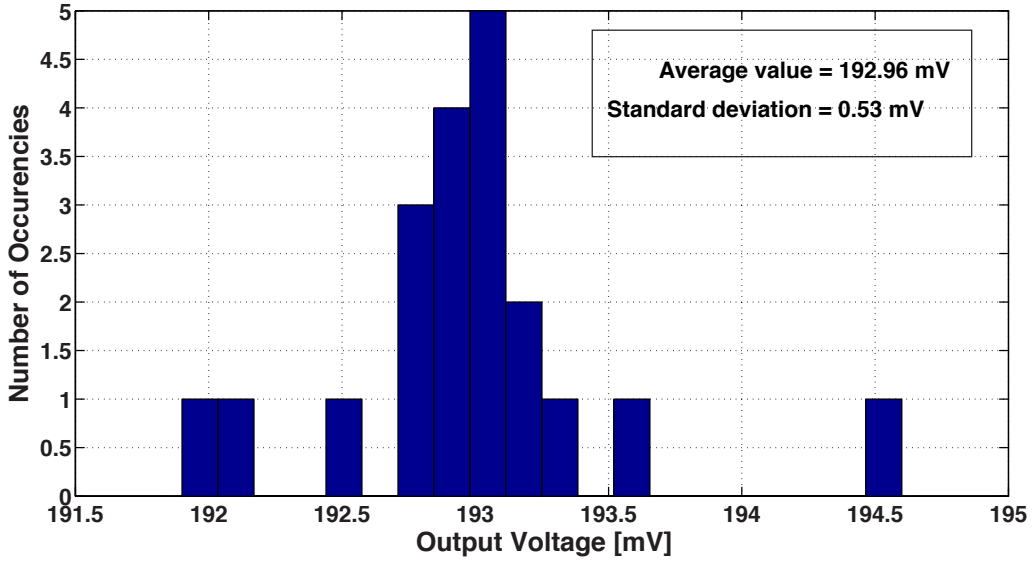

Figure 4.27: Measured output voltage level distribution of CRL.

4.2.2 Voltage reference circuit with duty-cycle regulated loop (DCRL)

In Figure 4.28 and Figure 4.29, the top-level schematic diagram and chip micrograph of the voltage reference circuit with duty-cycle regulated loop are shown. The circuit occupies the area of 400 x 200 μm^2 in which the active area, dominated by the resistors used in the bandgap core cell and it is quite smaller then the circuit with current regulated loop. The adopted approach consists of compensating for the temperature dependence of the sampled-data amplifier output voltage by utilizing an additional feedback loop which includes a variable duty-cycle generator which determines the duration of amplification phase, Φ_D, of the sampled-data.

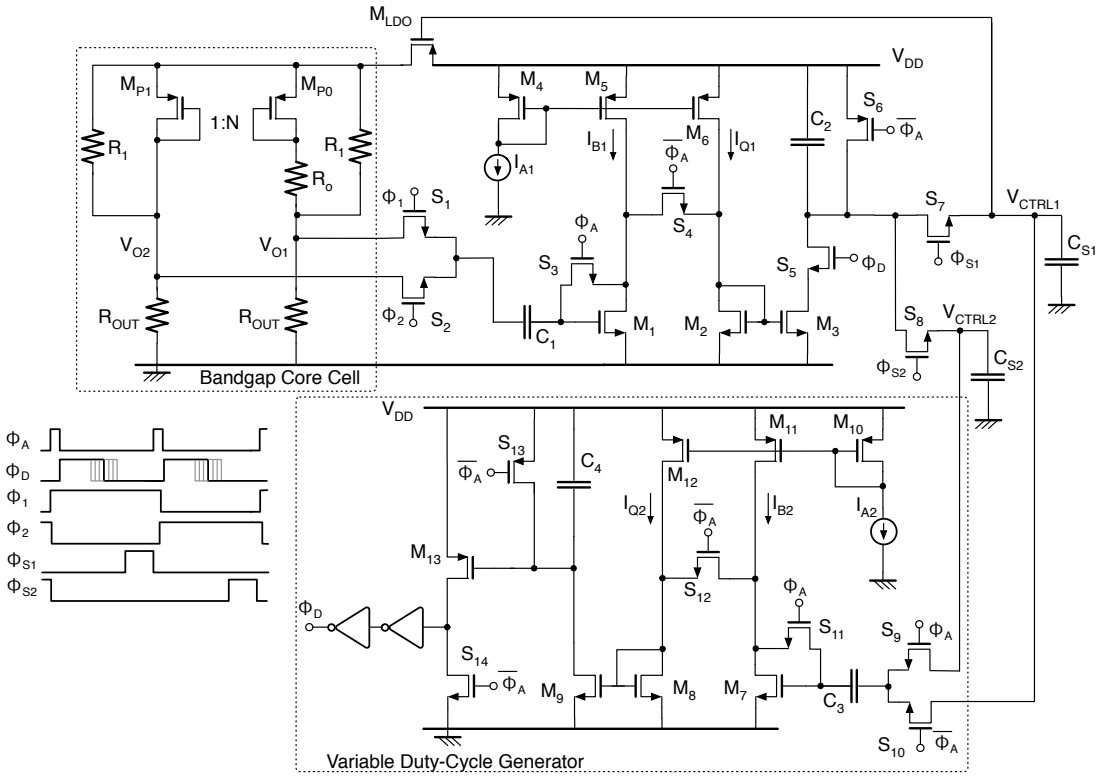

Figure 4.28: Top-level schematic of voltage reference with duty-cycle regulated loop.

The circuit in Figure 4.28 has been simulated and measured with a clock frequency of 50 kHz. The auto-zero phase, Φ_A, 25 % of clock periods, while Φ_1 and Φ_2 have a frequency of 25 kHz. Figure 4.30 shows the measured output voltage as a function of the temperature for different supply voltages. The circuit starts working at 0.65 V with limited temperature range due to the higher values of threshold voltages of input switches of smiled data amplifier and of M_{LDO}. The circuit achieves 191.5 mV output voltage with a TC of 52.5 ppm/°C in the range from 0 °C to 100 °C at 0.8 V supply voltage. The same performance holds for lower supply voltages (0.7 V and 0.65 V),

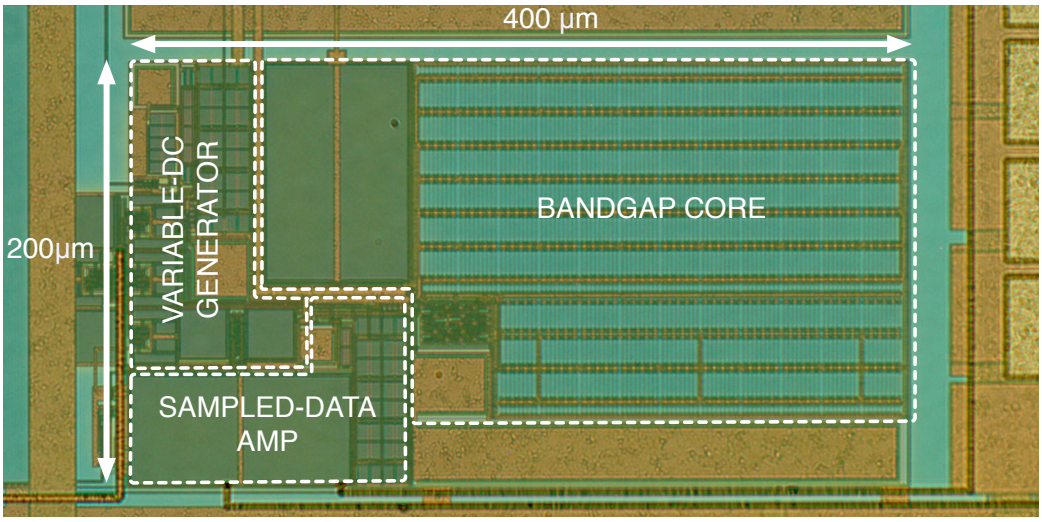

Figure 4.29: Chip micrograph of the voltage reference circuit with duty-cycle regulated loop.

since as also verified for the circuit presented in Section 6.2.1, for low supply and low temperature, the loop control does not work properly and the experimental data are not provided for the entire temperature range. The reason is again in this case that the threshold voltages that are higher than the value predicted by the simulations at low temperatures. On the other hand, as seen from Figure 4.30, for temperatures higher then 100°C, the generated output voltages are lower then expected values to have better temperature variation performance (i.e., less TC). the reason is that, the temperature compensation scheme of the second feedback loop which includes the duty-cycle generator is not effectively working for temperatures higher then 100 °C. On the

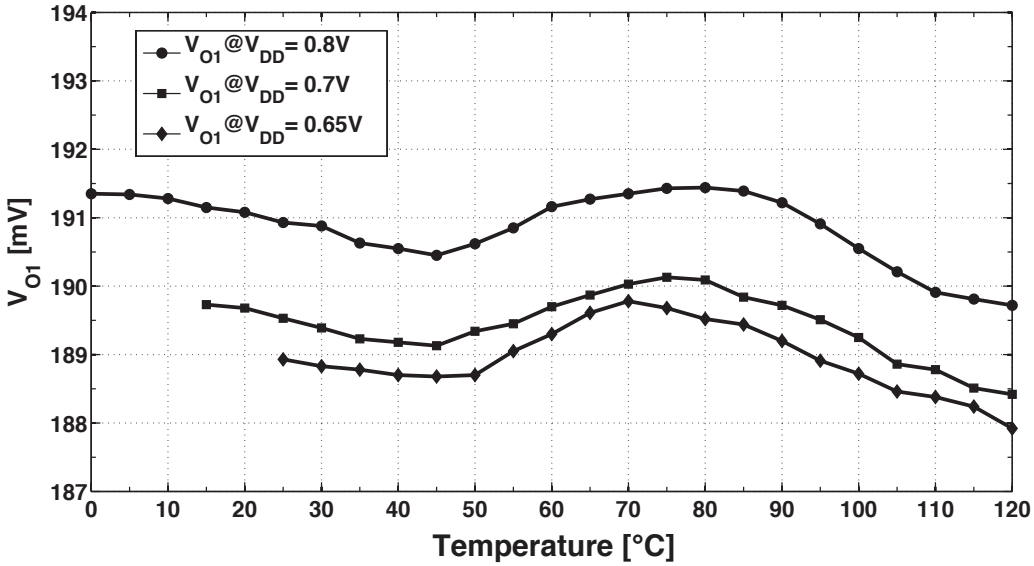

Figure 4.30: Measured output voltage of DCRL as a function of the temperature for different supply voltages.

contrary, the main feedback loop is working properly and the difference between two output voltages V_{O1} and V_{O2} is less 1 mV.

The top-level simulated output voltages of sampled-data amplifier, V_{CTRL1} and V_{CTRL2}, as a function of temperature are shown in Figure 4.31. As seen from the figure, these two control voltages are really close to each other when the loop is locked. Notice that, the slopes of the quiescent output voltages of the amplifier with respect to the temperature is positive. This shows that second feedback loop is working in the direction to compensate for the threshold voltage temperature dependence of M_{LDO} that controls the current of the bandgap cell.

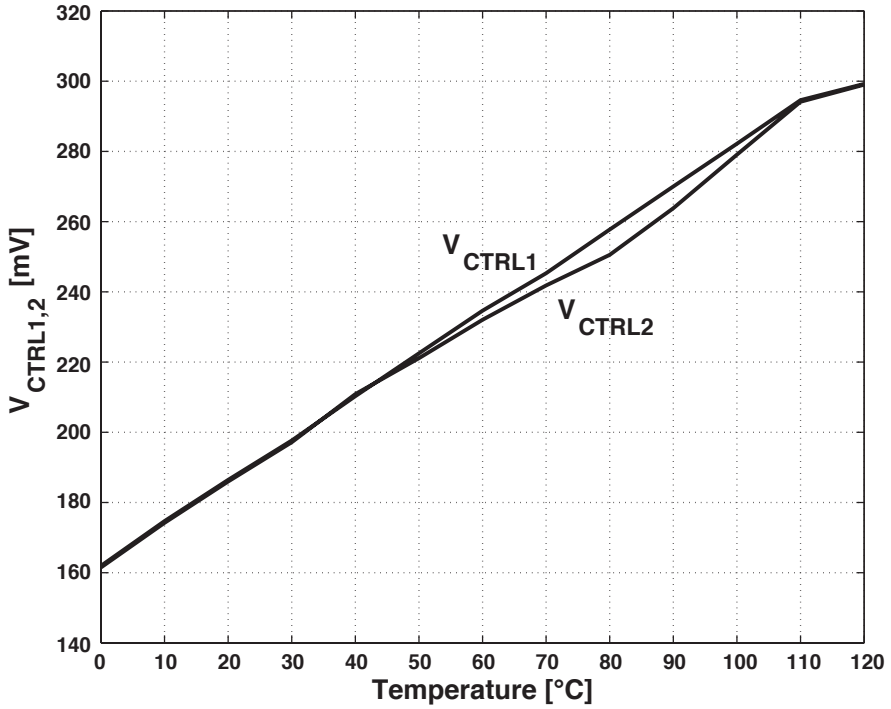

Figure 4.31: Simulated temperature variation of control voltages in the duty-cycle regulated loop scheme.

In order to understand the problem at high temperatures, the variable duty-cycle generator has been characterised stand-alone at 0.8 V supply voltage. The bias current of the circuit is tuned to have a 50 % phase duration time (T_D=10 μs) with 0 V input voltage difference at room temperature. Figures 4.32 - 4.33 show the measured output phase duration time of variable duty-cycle generator with respect to the input differential voltage and temperature, respectively.

As seen from Figure 4.33, the slope of the curve is decreasing with a temperature increase. As a result, at high temperatures, the value of the generated phase duration

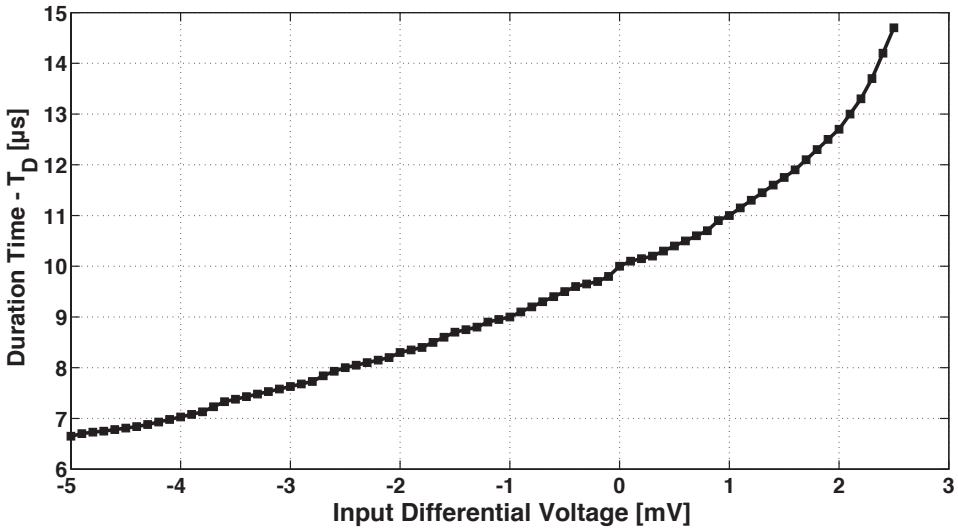

Figure 4.32: Measured duration time of variable duty-cycle generator with respect to input differential voltage.

time, T_D, is almost saturating to its minimum. This leads to a T_D which is lower then what required in order to properly generate the control voltage for M_{LDO}.

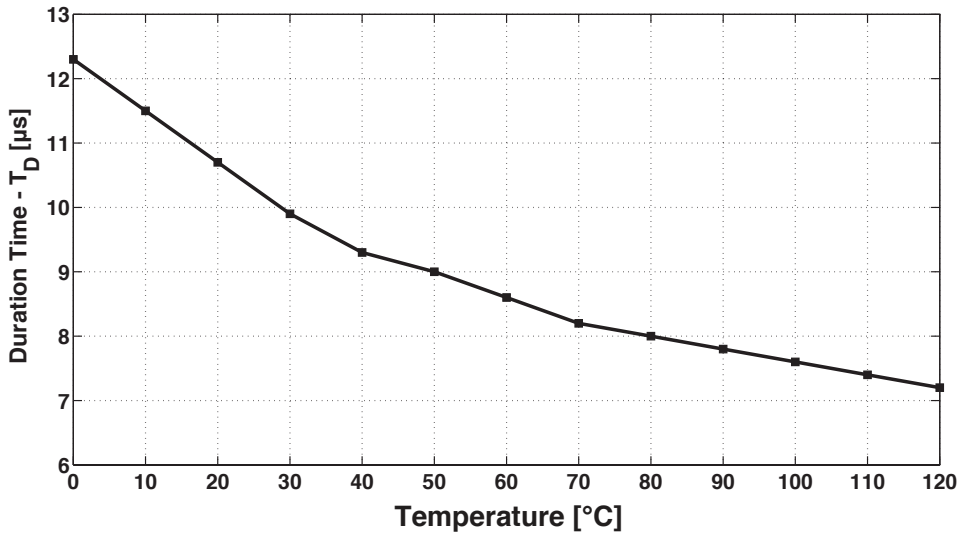

Figure 4.33: Measured duration time of variable duty-cycle generator as a function of the temperature.

Figure 4.34, shows the measured power supply rejection (PSR) at the nominal supply voltage. The output is filtered with a 6 pF capacitor. The PSR is -52.5 dB at 100 Hz and -35 dB at 10 MHz.

Figure 4.35 plots the measured supply current as a function of the temperature when the supply voltage is 0.8 V. Since, in this topology, the temperature compensation of the circuit is based on duty-cycle instead of current regulation, the total current drawn from the supply is changing more with respect to the scheme described in Section

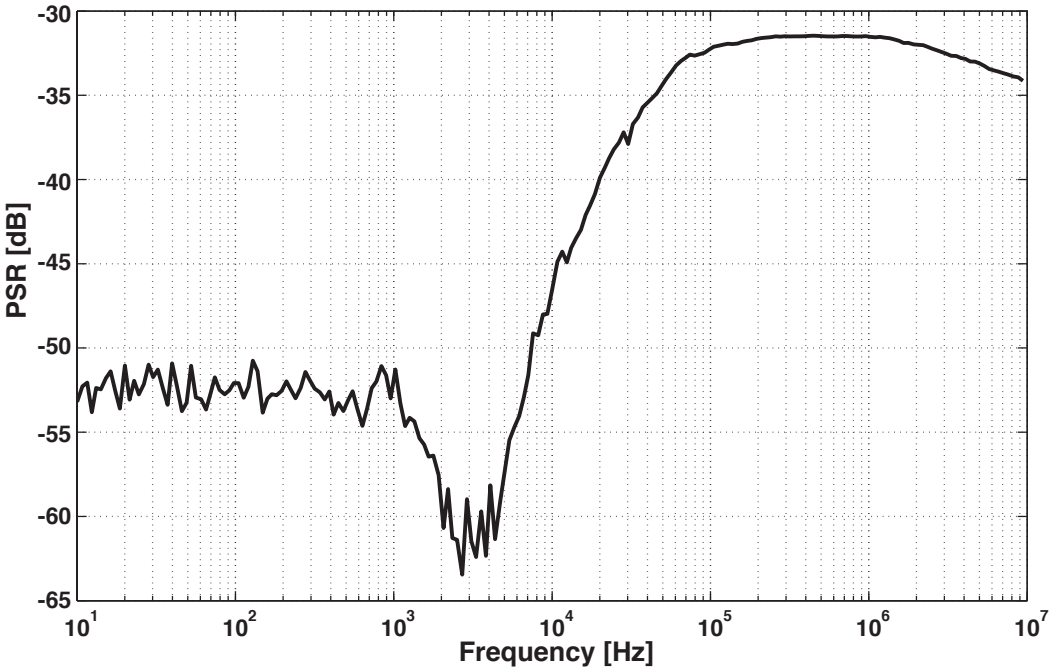

Figure 4.34: Measured power supply rejection (PSR) of DCRL.

4.1.1. The variation of the measured current is about 11.8 % in the entire temperature range. The nominal current value is 650 nA at room temperature from a 0.8 V supply voltage, leading to a power consumption of 0.52 μW.

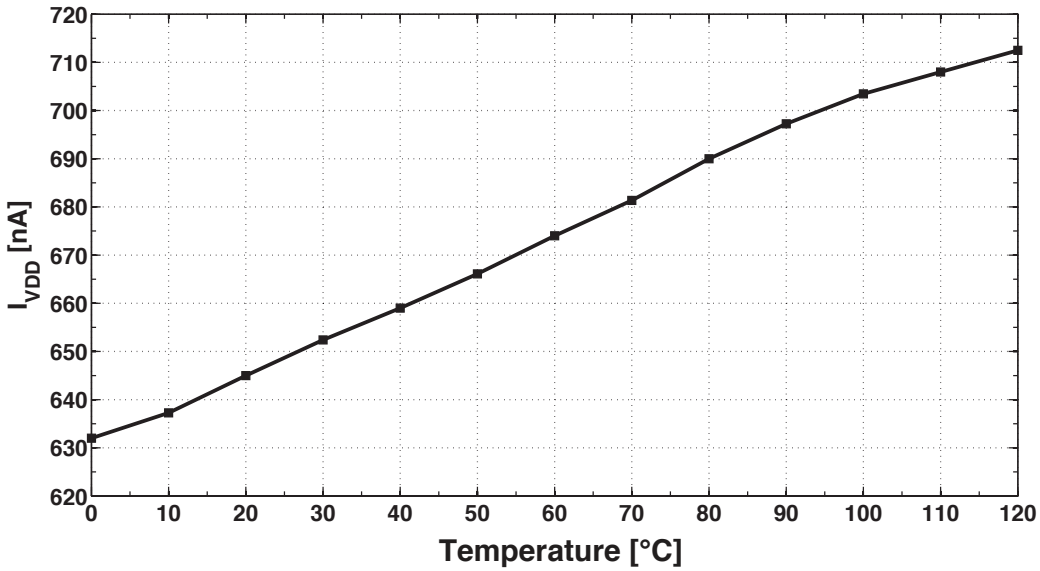

Figure 4.35: Measured supply current as a function of the temperature of DCRL.

Figure 4.36 shows the distribution of the output voltage level for the 20 available samples without any device trimming or bias current calibration. Measurements have been collected at room temperature, with a supply voltage equal to 0.8 V. The mean value is 191.67 mV while the standard deviation is 0.62 mV. The 3 σ inaccuracy is 1 %.

This is due to chip-to-chip mismatches; calibration of the bias current of sampled-data amplifier or variable duty-cycle generator can reduce the inaccuracy to less than 0.1 %.

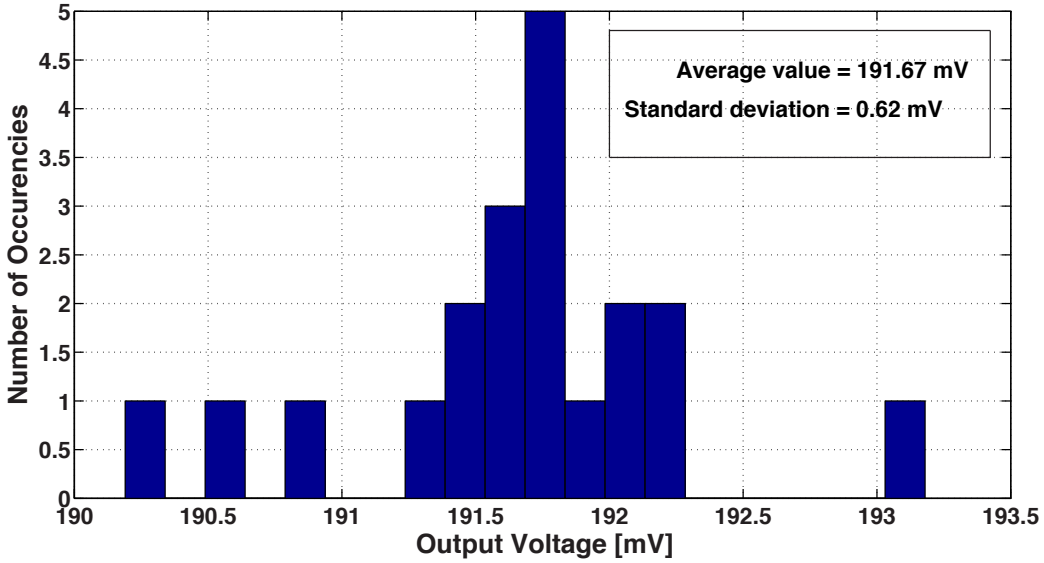

Figure 4.36: Measured output voltage level distribution of DCRL.

4.3 Summary

This section presents the measurement results collected from the two very low power bandgap voltage references designed and implemented in a standard 0.18 μm CMOS technology with 6 metal and 2 poly layers. The measurement results show that the proposed topologies are capable of operating down to a 0.65 V supply voltage. This is the lowest published supply level achieved without any special process steps and thanks to the use of a reversed current-mode bandgap scheme and of a sampled-data amplifier. The circuits achieve 191 mV output reference voltages with temperature coefficient on the order of 40 ppm/°C in the temperature range of 0 - 120 °C. The total consumed powers are 0.3 μW and 0.4 μW at 27 °C while occupying the area of 0.2 mm^2 and 0.08 mm^2, respectively.

Performance summary of the designed circuits and their comparison with other sub-1V voltage reference circuits reported in the open literature is given in Table 4.4. The table shows that the proposed voltage reference topologies achieve reference voltage with comparable level of temperature coefficient and quite low power consumption with respect to the other proposed sub-1V voltage reference circuits.

Performance summary of the designed circuits and their comparison with other sub-1V voltage reference circuits reported in the open literature is given in Table 4.4. The table shows that the proposed voltage reference topologies achieve reference voltage with comparable level of temperature coefficient and quite low power consumption with respect to the other proposed sub-1V voltage reference circuits.

Table 4.4: Performance comparison of sub-1V voltage reference circuits in literature.

	CRL	**DCRL**	**[65]**	**[42]**	**[37]**	**[46]**
Technology [μm] CMOS	0.18	0.18	0.13	0.18	0.6	0.35
Output Voltage [mV]	193	191.6	256	221	603	190.1
Minimum Supply Voltage [V]	0.65	0.65	0.75	0.85	0.98	1
Supply Current [μA]	0.49	0.6	0.2	3.9	18	0.25
Temperature Coefficient [ppm/$^\circ$C]	43	52.5	40	194	15	16.9
Temperature Range [$^\circ$C]	0-120	0-100	-25-85	-20-120	0-100	-40-80
PSR @ 100Hz [dB]	-50	-50	N/A	N/A	-44	-41
PSR @ 10MHz [dB]	-36	-36	N/A	N/A	-17	-17
Area [mm^2]	0.2	0.08	0.07	0.0228	0.24	0.049

5. CONCLUSION

In this thesis, design and implementation of different kinds of voltage reference circuits in standard CMOS technologies were presented. In this respect, this thesis consisted of two main parts. First part concentrated on high precision, low noise bandgap reference design while second part concentrated on low voltage and low power voltage reference design.

Firstly, in order to obtain a high precision and low noise BGR, two different curvature corrected current mode bandgap reference were designed and implemented in 0.35 μm triple-well CMOS technology. In these designs a simple gain stage was utilized instead of a conventional op-amp which dominated the total power consumption of the circuit. The first design had been suffering from base current incorrections due to the topology chosen, even if it had been compensated through an additional base current compensation circuitry. Measurement results showed that with this designed BGR provided 511.7 mV reference output voltage with a 9.52 ppm/°C temperature coefficient after 8-bit trimming over the temperature range of -40 °C to 130 °C while consuming 9.8 μA from a single 3.3 V supply voltage. Moreover, the design was improved by modifying the topology, as base current incorrections were discarded and the proposed block bulk isolation strategy was adopted in order to increase the immunity to substrate noise. Two versions of this design were implemented and measured. The only difference between these two implementations was the channel length of the current mirrors that were utilized, in the second version channel lengths were chosen to be quite larger with respect to the first implementation in order to improve the low frequency noise performance of the circuit. The measurement results show that both of the two implemented BGRs generated an output voltage of 220 mV while achieving a TC around 3.5 ppm/°C after 8-bit trimming over the temperature range of -40 °C to 130 °C. The RMS value of the noise at the outputs of the designed BGRs were 2.54 μV and 0.918 μV integrated from 0.1 Hz to 10 Hz, respectively; while the measured flat band noise is around 170 nV/$\sqrt{Hz}$ for both of the circuits. The

circuits were consuming a supply current around 32 μA from a 3.3 V single supply. The designed BGR achieved the best temperature coefficient with minimum area and supply current. Its noise performance is equivalent to the best reported [39] while occupying 1/2.5 the area. However, the most important drawback of the designed BGRs is that they can operate properly down to a 2 V supply voltage which is, firstly, due to the utilized topology and, secondly, the high threshold voltages of the chosen technology (0.35 μm) for implementation. Furthermore, the effectiveness of the proposed block bulk isolation strategy is shown in the measurement results, the improvement is more than 40 dB for frequencies up to 1 MHz.

The second part of the thesis concentrated on low voltage and low power voltage reference design. For this purpose, two new voltage reference topologies that utilize sampled data operation were proposed. The proposed voltage reference topologies were implemented and fabricated in 0.18 μm CMOS technology. In these two different topologies the same current mode bandgap cell and sampled-date amplifier were utilized. The main difference between two topologies is the adopted method that determines the quiescent output voltage of the amplifier, or in other words, the temperature compensation method. Measurement results showed that the proposed voltage reference circuits are working properly down to 0.65 V while achieving an output voltage around 193 mV with a temperature coefficient on the order of 50 ppm/°C in the temperature range of 0-120 °C. This is the lowest published supply level achieved without any special process steps. The total power consumption of the two designed voltage references are 0.3 μW and 0.4 μW at 27 °C, while occupying the area of 0.2 mm^2 and 0.08 mm^2, respectively. As a result, the proposed voltage reference topologies generate a reference voltage with comparable level of temperature coefficient and quite low power consumption with respect to the other sub-1V voltage reference circuits reported in open literature.

As future work, the supply voltage limitation of the designed curvature corrected bandgap reference circuits will tried to be lowered down via using different kind of gain or amplifier stage, since the supply voltage constrict of the architecture is dominated by its gain stage. Moreover, the architecture will be tried to convert to a CMOS-only one in order to flex the supply voltage constraint for bandgap core and able to work with lower quiescent currents. Moreover, complementary switched biasing technique

(has been implemented on the second designed BGR circuit (see APPENDIX A.3.)) that should improve the low noise performance of the circuit without increasing the device area will tried to be verified. The proposed and designed very low voltage low power bandgap reference circuits have moderate temperature stability due to the lack of higher-order (nonlinear) temperature compensation for the core circuit. Therefore, since it is proven that architecture is working, an appropriate method to compensate for higher-order temperature behaviour will be tried to be adopted to achieve higher precision without increasing the required supply voltage.

REFERENCES

[1] **AN-3998.** (2007). Calculating Temperature Coefficient and Initial Accuracy for Voltage References, *Maxim Integrated Application Note*.

[2] **Rincon-Mora, G.A.** (2001). *Voltage References: From Diodes to Precision Higher-Order BandGap Circuits*, Wiley-Interscience.

[3] **Miller, P. and Moore, D.** (1999). Precision Voltage Reference, *Texas Instruments Inc., Analog Applications Journal*.

[4] **Becker-Gomez, A.** (2010). *Analog and Mixed Signal Techniques for Low Voltage Bandgap References*, Dallas, Texas.

[5] **Lee, M.** (1999). Understanding and Applying Voltage References, *Linear Technology Application Note*.

[6] **MT-087** (2009). Voltage References, *Analog Devices Tutorials*.

[7] **Gupta, V.** (2007). *An Accurate, Trimless, High PSRR, Low-Voltage CMOS Bandgap Reference IC*, (Doctoral dissertation) Georgia Institute of Technology, Atlanta, Georgia.

[8] **Reay, R.**, **Klaassen, E. and Kovacs, G.** (1995). A micromachined low-power temperature-regulated bandgap voltage reference, *Solid-State Circuits, IEEE Journal of*, *30*(12), 1374–1381.

[9] **Ahuja, B.**, **Vu, H.**, **Laber, C. and Owen, W.** (2005). A very high precision 500-nA CMOS floating-gate analog voltage reference, *Solid-State Circuits, IEEE Journal of*, *40*(12), 2364 – 2372.

[10] **Adel S. Sedra, K.C.S.** (2007). *Microelectronic Circuits*, Oxford University Press, Inc., 5. edition.

[11] **Paul R. Gray, Paul J. Hurst, S.H.L. and Meyer, R.G.** (2001). *Analysis and Design of Analog Integrated Circuits*, John Wiley and Sons, 4. edition.

[12] **Tsividis, Y.** (1980). Accurate analysis of temperature effects in I_C-V_{BE} characteristics with application to bandgap reference sources, *Solid-State Circuits, IEEE Journal of*, *15*(6), 1076–1084.

[13] **Kinget, P.** (2005). Device mismatch and tradeoffs in the design of analog circuits, *Solid-State Circuits, IEEE Journal of*, *40*(6), 1212–1224.

[14] **Tuinhout, H.**, **Bretveld, A. and Peters, W.C.M.** (2003). Current mirror test structures for studying adjacent layout effects on systematic transistor mismatch, *Microelectronic Test Structures, 2003. International Conference on*, pp.221–226.

[15] **Vittoz, E.A.** (1996). The Fundamentals of Analog Micropower Design, *Circuit and Systems Tutorials*, 365 – 372.

[16] **Laker, K.R. and Sansen, W.M.C.** (1994). *Design of Analog Integrated Circuits and Systems*, McGraw-Hill.

[17] **Sze, S.M. and Ng, K.K.** (2006). *Physics of Semiconductor Devices*, John Wiley and Sons.

[18] **Chuang, H.M.**, **Thei, K.B.**, **Tsai, S.F. and Liu, W.C.** (2003). Temperature-dependent characteristics of polysilicon and diffused resistors, *Electron Devices, IEEE Transactions on*, *50*(5), 1413–1415.

[19] **Tsividis, Y.P.** (1987). *Operation and Modeling of MOS Transistor*, McGraw-Hill.

[20] **Pelgrom, M.J.M.**, **Duinmaijer, A.C.J. and Welbers, A.P.G.** (1989). Matching properties of MOS Transistors, *Solid State Circuits, IEEE Journal of*, *24*(5), 1433–1439.

[21] **Hastings, A.** (2000). *Art of Analog Layout*, Prentice Hall.

[22] **Maloberti, F.** (2001). *Analog Design for CMOS Integrated Systems*, Kluwer Academic Publishers.

[23] **Chuang, H.M.**, **Thei, K.B.**, **Tsai, S.F. and Liu, W.C.** (2003). Temperature-dependent characteristics of polysilicon and diffused resistors, *Electron Devices, IEEE Transactions on*, *50*(5), 1413–1415.

[24] **Widlar, R.** (1971). New developments in IC voltage regulators, *Solid-State Circuits, IEEE Journal of*, *6*(1), 2–7.

[25] **Kuijk, K.** (1973). A precision reference voltage source, *Solid-State Circuits, IEEE Journal of*, *8*(3), 222–226.

[26] **Brokaw, A.** (1974). A simple three-terminal IC bandgap reference, *Solid-State Circuits, IEEE Journal of*, *9*(6), 388–393.

[27] **Song, B. and Gray, P.** (1983). A precision curvature-compensated CMOS bandgap reference, *Solid-State Circuits, IEEE Journal of*, *18*(6), 634 – 643.

[28] **Lee, I.**, **Kim, G. and Kim, W.** (1994). Exponential curvature-compensated BiCMOS bandgap references, *Solid-State Circuits, IEEE Journal of*, *29*(11), 1396 –1403.

[29] **Rincon-Mora, G. and Allen, P.** (1998). A 1.1-V current-mode and piecewise-linear curvature-corrected bandgap reference, *Solid-State Circuits, IEEE Journal of*, *33*(10), 1551 –1554.

[30] **Gunawan, M.**, **Meijer, G.**, **Fonderie, J. and Huijsing, J.** (1993). A curvature-corrected low-voltage bandgap reference, *Solid-State Circuits, IEEE Journal of*, *28*(6), 667 –670.

[31] **Leung, K.N.**, **Mok, P. and Leung, C.Y.** (2003). A 2-V 23-μA 5.3-ppm/C curvature-compensated CMOS bandgap voltage reference, *Solid-State Circuits, IEEE Journal of*, *38*(3), 561 – 564.

[32] **Malcovati, P.**, **Maloberti, F.**, **Fiocchi, C. and Pruzzi, M.** (2001). Curvature-compensated BiCMOS bandgap with 1-V supply voltage, *Solid-State Circuits, IEEE Journal of*, *36*(7), 1076 –1081.

[33] **Holman, W.** (1996). A new temperature compensation technique for bandgap voltage references, *Circuits and Systems, 1996. ISCAS '96., Connecting the World., 1996 IEEE International Symposium on*, volume 1, pp.385 –388 vol.1.

[34] **Stefan, M. and O'Dwyer, T.** (2008). Curvature correction method for a bandgap voltage reference, *Signals and Systems Conference, 208. (ISSC 2008). IET Irish*, pp.134 –137.

[35] **Rincon-Mora, G.A.** (2000). *U.S. Patent No. 6,157,245*, Washington, DC: U.S. Patent and Trademark Office.

[36] **Banba, H.**, **Shiga, H.**, **Umezawa, A.**, **Miyaba, T.**, **Tanzawa, T.**, **Atsumi, S. and Sakui, K.** (1999). A CMOS bandgap reference circuit with sub-1-V operation, *Solid-State Circuits, IEEE Journal of*, *34*(5), 670 –674.

[37] **Leung, K.N. and Mok, P.** (2002). A sub-1-V 15-ppm/C CMOS bandgap voltage reference without requiring low threshold voltage device, *Solid-State Circuits, IEEE Journal of*, *37*(4), 526 –530.

[38] **Jiang, Y. and Lee, E.** (2000). Design of low-voltage bandgap reference using transimpedance amplifier, *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, *47*(6), 552–555.

[39] **Sanborn, K.**, **Ma, D. and Ivanov, V.** (2007). A Sub-1-V Low-Noise Bandgap Voltage Reference, *Solid-State Circuits, IEEE Journal of*, *42*(11), 2466 –2481.

[40] **Annema, A.J.** (1999). Low-power bandgap references featuring DTMOSTs, *Solid-State Circuits, IEEE Journal of*, *34*(7), 949–955.

[41] **Giustolisi, G.**, **Palumbo, G.**, **Criscione, M. and Cutri, F.** (2003). A low-voltage low-power voltage reference based on subthreshold MOSFETs, *Solid-State Circuits, IEEE Journal of*, *38*(1), 151 – 154.

[42] **Huang, P.H.**, **Lin, H. and Lin, Y.T.** (2006). A Simple Subthreshold CMOS Voltage Reference Circuit With Channel- Length Modulation Compensation, *Circuits and Systems II: Express Briefs, IEEE Transactions on*, *53*(9), 882 –885.

[43] **Leung, K.N. and Mok, P.** (2003). A CMOS voltage reference based on weighted ΔVGS for CMOS low-dropout linear regulators, *Solid-State Circuits, IEEE Journal of*, *38*(1), 146 – 150.

[44] **De Vita, G. and Iannaccone, G.** (2007). A Sub-1-V, 10 ppm/C, Nanopower Voltage Reference Generator, *Solid-State Circuits, IEEE Journal of*, *42*(7), 1536 –1542.

[45] **Gilbert, Barrie, S.S.F.** (1996). *U.S. Patent No. 5,563,404*, Washington, DC: U.S. Patent and Trademark Office.

[46] **Huang, H.W.**, **Hsieh, C.Y.**, **Chen, K.H. and Kuo, S.Y.** (2008). A 1V 16.9ppm/C 250nA Switched-Capacitor CMOS Voltage Reference, *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pp.438 –626.

[47] **Tiew, K.C.**, **Cusey, J. and Geiger, R.** (2002). A curvature compensation technique for bandgap voltage references using adaptive reference temperature, *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, volume 4, pp.IV–265 – IV–268 vol.4.

[48] **Nicollini, G. and Senderowicz, D.** (1991). A CMOS bandgap reference for differential signal processing, *Solid-State Circuits, IEEE Journal of*, *26*(1), 41 –50.

[49] **David Johns, K.W.M.** (1997). *Analog Integrated Circuit Design*, John Wiley and Sons.

[50] **Blauschild, R.**, **Tucci, P.**, **Muller, R. and Meyer, R.** (1978). A new NMOS temperature-stable voltage reference, *Solid-State Circuits, IEEE Journal of*, *13*(6), 767 – 774.

[51] **Tanaka, H.**, **Nakagome, Y.**, **Etoh, J.**, **Yamasaki, E.**, **Aoki, M. and Miyazawa, K.** (1994). Sub-1-uA dynamic reference voltage generator for battery-operated DRAMs, *Solid-State Circuits, IEEE Journal of*, *29*(4), 448 –453.

[52] **Oguey, H. and Gerber, B.** (1980). MOS voltage reference based on polysilicon gate work function difference, *Solid-State Circuits, IEEE Journal of*, *15*(3), 264 – 269.

[53] **Tobey, J.M.C.**, **Giuliani, D.J. and Ashkin, P.B.** (1976). *U.S. Patent No. 3,975,648*, Washington, DC: U.S. Patent and Trademark Office.

[54] **Klumperink, E.**, **Gierkink, S.L.J.**, **Van Der Wel, A. and Nauta, B.** (2000). Reducing MOSFET 1/f noise and power consumption by switched biasing, *Solid-State Circuits, IEEE Journal of*, *35*(7), 994–1001.

[55] **Service, E.I.** (2013). TSMC technology overview, Retrieved: June, 2013 from, *http://www.europractice-ic.com/technologies-TSMC.php*.

[56] **Service, E.I.** (2013). UMC technology overview, Retrieved: June, 2013 from, *http://www.europractice-ic.com/technologies-UMC.php*.

[57] **Service, E.I.** (2013). AMS technology overview, Retrieved: June, 2013 from, *http://www.europractice-ic.com/technologies-AMS.php*.

[58] **Ogasahara, Y.**, **Hashimoto, M.**, **Kanamoto, T. and Onoye, T.** (2008). Measurement of supply noise suppression by substrate and deep N-well in 90nm process, *Solid-State Circuits Conference, 2008. A-SSCC '08. IEEE Asian*, pp.397 –400.

[59] **Ivanov, V.V. and Filanovsky, I.M.** (2004). *Operational Amplifier Speed and Accuracy Improvement: Analog Circuit Design with Structural Methodology*, Kluwer Academic Publishers.

[60] **Andreou, C.**, **Koudounas, S. and Georgiou, J.** (2012). A Novel Wide-Temperature-Range, 3.9 ppm/C CMOS Bandgap Reference Circuit, *Solid-State Circuits, IEEE Journal of*, *47*(2), 574 –581.

[61] **Li, J.H.**, **bao Zhang, X. and yan Yu, M.** (2011). A 1.2-V Piecewise Curvature-Corrected Bandgap Reference in 0.5μm CMOS Process, *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, *19*(6), 1118 –1122.

[62] **Perry, R.**, **Lewis, S.**, **Brokaw, A. and Viswanathan, T.** (2007). A 1.4 V Supply CMOS Fractional Bandgap Reference, *Solid-State Circuits, IEEE Journal of*, *42*(10), 2180 –2186.

[63] **Bourgoine, N.** (2011). Harvest Energy from a single Photovoltaic Cell, *Journal of Analog Innovation*, *21*(1).

[64] **Raju, N. and Grazier, M.** (2010). ULP meets energy harvesting: a game-changing combination for design engineers, *Texas Instruments, White Paper, Energy Harvesting*, *26*.

[65] **Ivanov, V., B.R. and Gerber, J.** (2012). An Ultra Low Power Bandgap Operational at Supply From 0.75 V, *Solid-State Circuits, IEEE Journal of*, *47*(7), 1515–1523.

[66] **Laker, K. and W.M.C., S.** (1994). *Design Of Analog Integrated Circuits And Systems*, McGraw-Hill.

[67] **Schreier, R. and Temes, G.** (2005). *Understanding Delta-Sigma Data Converters*, New York: Wiley-IEEE.

[68] **Quiquempoix, V., D.P.B.A.B.G.M.J.S.J. and Temes, G.** (2005). A low-power 22-bit incremental ADC, *Solid-State Circuits, IEEE Journal of*, *41*(7), 1562–1571.

[69] **Analog Devices, I.** (2013). AD-8628: Zero-Drift, Single-Supply Rail-to-Rail Input-Output Opamp Data Sheet, Retrieved: June, 2013 from, *http://www.analog.com/en/all-operational-amplifiers-op-amps/operational-amplifiers-op-amps/ad8628/products/product.html*.

[70] **Kirton, M.J., U.M.** (1989). Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/f) noise, *Advances In Physics*, *38*(4), 367–468.

[71] **McWhorter, A.** (1957). *1/f noise and germanium surface properties. In Semiconductor Surface Physics*, Philadelphia: University of Pennsylvania Press.

[72] **Berz, F.** (1970). Theory of low frequency noise in Si MOST's, *Solid-State Electron*, *13*, 631.

[73] **Hung, K.**, **Ko, P.K.**, **Hu, C. and Cheng, Y.** (1990). A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors, *Electron Devices, IEEE Transactions on*, *37*(3), 654–665.

[74] **Abowitz, G.**, **Arnold, E. and Leventhal, E.** (1967). Surface states and 1/f noise in MOS transistors, *Electron Devices, IEEE Transactions on*, *14*(11), 775–777.

[75] **Klaassen, F.** (1971). Characterization of low 1/f noise in MOS transistors, *Electron Devices, IEEE Transactions on*, *18*(10), 887–891.

[76] **Mikoshiba, H.** (1982). 1/f noise in n-channel silicon-gate MOS transistors, *Electron Devices, IEEE Transactions on*, *29*(6), 965–970.

[77] **Hooge, F.N.** (1994). 1/f noise sources, *Electron Devices, IEEE Transactions on*, *41*(11), 1926–1935.

[78] **Kleinpenning, T. and Vandamme, K.** (1981). Model for 1/f noise in metal-oxide-semiconductor transistors, *Journal of Applied Physics*, *52*, 1595–1596.

[79] **Bult, K. and Geelen, G.** (1992). An inherently linear and compact MOST-only current division technique, *Solid-State Circuits, IEEE Journal of*, *27*(12), 1730–1735.

[80] **Mensink, C.H.J.**, **Nauta, B. and Wallinga, H.** (1997). A CMOS soft-switched transconductor and its application in gain control and filters, *Solid-State Circuits, IEEE Journal of*, *32*(7), 989–998.

[81] **Bloom, I. and Nemirovsky, Y.** (1991). 1/f noise reduction of metal-oxide-semiconductor field-effect transistors when cycled from inversion to accumulation, *Applied Physics Letters*, *58*(15), 1664 –1666.

[82] **Van Der Wel, A.**, **Klumperink, E.**, **Gierkink, S.L.J.**, **Wassenaar, R. and Wallinga, H.** (2000). MOSFET 1/f noise measurement under switched bias conditions, *Electron Device Letters, IEEE*, *21*(1), 43–46.

[83] **Shockley, W. and Read, W.** (1952). Statistics of the recombinations of holes and electrons, *Physics Review*, *87*(5), 835–842.

[84] **Van Der Wel, A.**, **Klumperink, E.**, **Vandamme, L. and Nauta, B.** (2003). Modeling random telegraph noise under switched bias conditions using cyclostationary RTS noise, *Electron Devices, IEEE Transactions on*, *50*(5), 1378–1384.

[85] **Shi, Z., M.J. and Dutoit, M.** (1994). Random telegraph signals in deep submicron n-MOSFETs, *Electron Devices, IEEE Transactions on*, *41*(7), 1161–1168.

[86] **Van Der Wel, A.P., K.E.H.E. and B., N.** (2005). Relating random telegraph signal noise in meta-oxide-semiconductor transistors to interface trap energy distribution, *Applied Physics Letter*, *87*.

[87] **Xu, X.L., K.R.W.J. and Ozturk, M.C.** (1992). Rapid thermal chemical vapor deposition of thin silicon oxide films using silane and nitrous oxide, *Applied Physics Letters*, *60*(24), 6063 – 6065.

[88] **Soltanian, B. and Kinget, P.** (2006). Tail Current-Shaping to Improve Phase Noise in LC Voltage-Controlled Oscillators, *Solid-State Circuits, IEEE Journal of*, *41*(8), 1792–1802.

APPENDICES

APPENDIX A.1 : Chip Microphotograph and Bonding Diagram of the BGRs in Chapter 3
APPENDIX A.2 : Test Setups for the Measurement of the Designed BGRs
APPENDIX A.3 : Switched Biasing Technique BGR Design

APPENDIX A.1: Chip Microphotograph and Bonding Diagram of the BGRs in Chapter 3

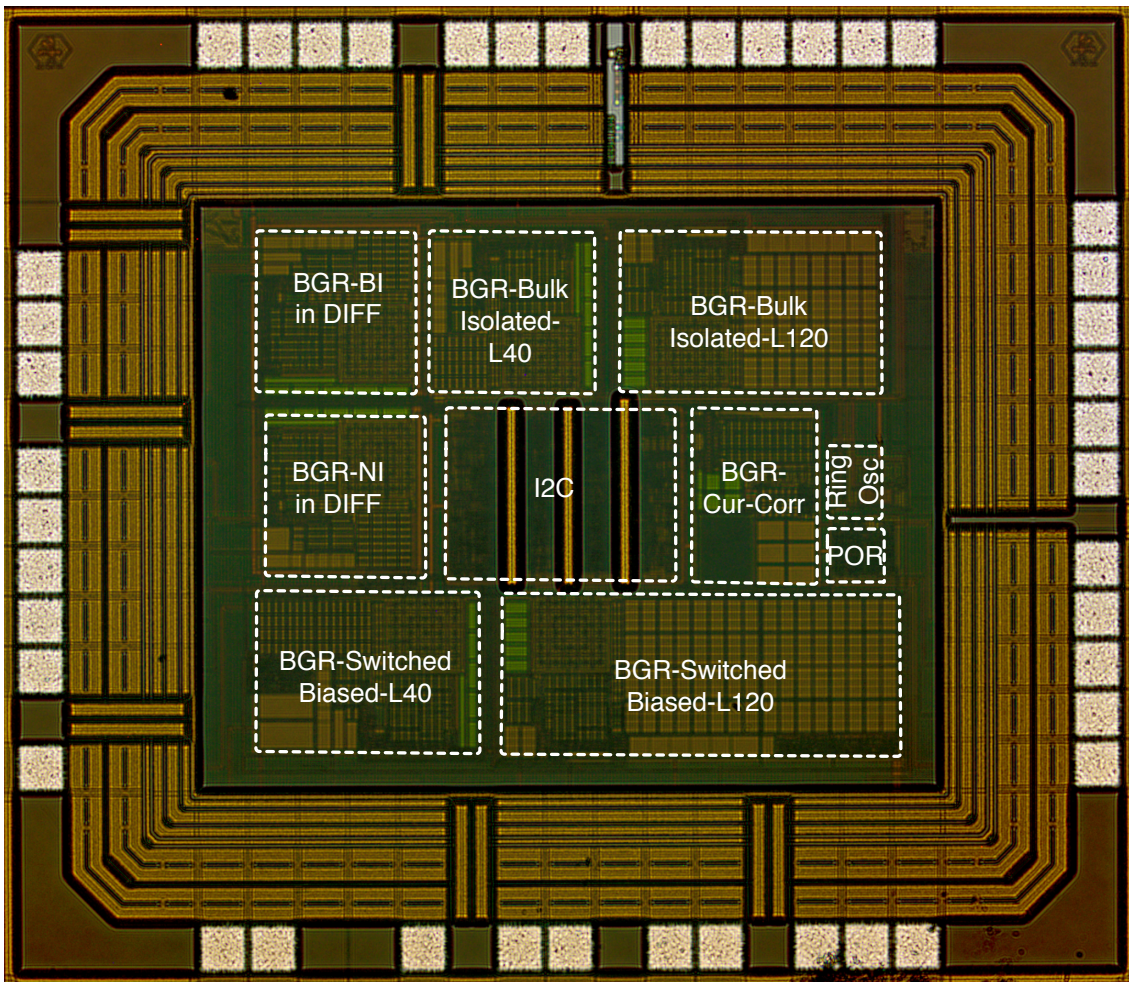

Figure A.1: Microphotgraph of the chip including the designed BGRs in Chapter 4.

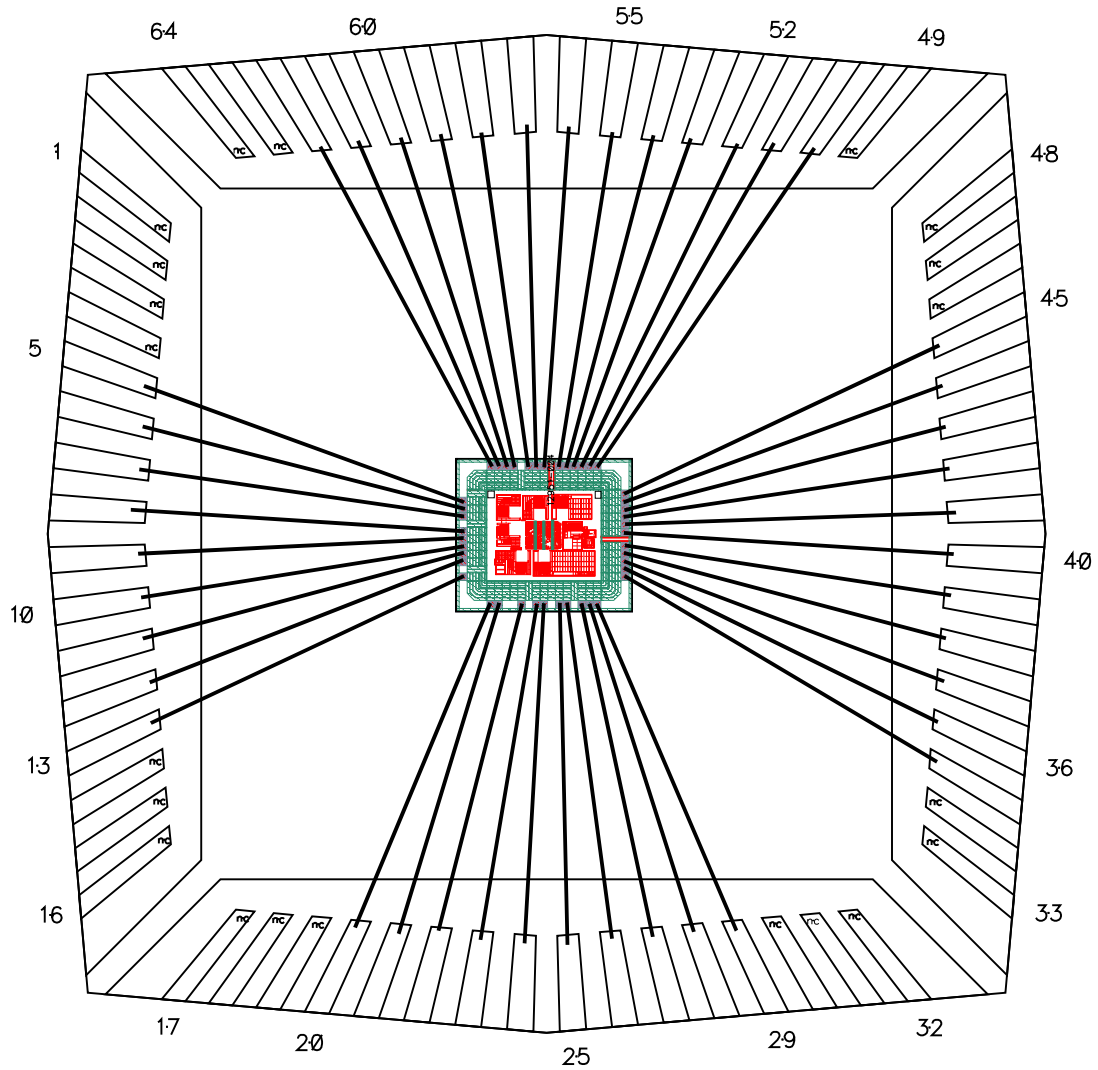

Figure A.2: Bonding diagram of the chip including the designed BGRs in Chapter 4.

Table A.1: Pin explanations of test chip.

Pin Name	Explanation	Pin No
PSUB	Substrate terminal for entire chip	29
AVDD	Analog supply for BGR in Sec. 4.1	38
AGND	Analog ground for BGR in Sec.4.1	35
BGR-OUT-0	Analog output of the BGR in Sec. 4.1	28
AVDD1	Analog supply for BGR in Sec. 4.2 in floating diffusion	5
AGND1	Analog ground for BGR in Sec. 4.2 in floating diffusion	7
BGR-OUT-BI-inDIFF	Analog output of the BGR (with isolated devices) in floating diff.	6
AVDD2	Analog supply for BGR in Sec. 4.2 in floating diffusion	8
AGND2	Analog ground for BGR in Sec. 4.2 in floating diffusion	10
BGR-OUT-NI-inDIFF	Analog output of the BGR (with normal devices) in floating diff.	9
DIFF-IN	Analog input for to bias the floating diffusion	62
AVDD3	Analog supply for BGR in Sec. 4.2 (L = 40μm)	61
AGND3	Analog ground for BGR in Sec. 4.2 (L = 40μm)	59
BGR-OUT-L40	Analog output of the BGR in Sec. 4.2 (L = 40μm)	60
AVDD4	Analog supply for BGR in Sec.4.2 (L = 120μm)	58
AGND4	Analog ground for BGR in Sec. 4.2 (L = 120μm)	56
BGR-OUT-L120	Analog output of the BGR in Sec. 4.2 (L = 120μm)	57
AVDD5	Analog supply for BGR in Sec. 4.3 (L = 40μm)	20
AGND5	Analog ground for BGR in Sec. 4.3 (L = 40μm)	21
BLK-CM-0	Bulk terminal of NMOS current mirrors in Sec. 4.3 (L = 40μm)	13
BGR-OUT-SW-L40	Analog output of the BGR in Sec. 4.3 (L = 40μm)	22
AVDD6	Analog supply for BGR in Sec.4.3 (L = 120μm)	23
AGND6	Analog ground for BGR in Sec. 4.3 (L = 120μm)	25
BLK-CM-1	Bulk terminal of NMOS curent mirrors in Sec. 4.3 (L = 120μm)	26
BGR-OUT-SW-L120	Analog output of the BGR in Sec. 4.3 (L = 120μm)	24
VMAX-SW	Analog input for current switches used in Sec. 4.3	53
DVDD	Digital supply for I^2C and ring oscillator	45
DGND	Digital ground for I^2C and ring oscillator	50
SDAIO	Data input-output of I^2C	55
SCL	Clock input of I^2C	54
POR-SEL	Digital input to control the source of POR	52
POR-EXT	External power on reset input for digital circuits	51
CLK-EXT	External clock input for current switches used in Sec. 4.3	53
CLK-TST	Digital output to test clock signal	44

Table A.2: I^2C control signals.

Signal Name	Default Val.	Explanation
BG-TRIM-0	10001100	R_1 trim of BGR in Sec. 4.1
ROUT-TRIM-0	01110011	R_{OUT} trim of BGR in Sec. 4.1
BG-TRIM-inDIFF	10001100	R_1 trim of BGRs in Sec. 4.2 in floating diff.
ROUT-TRIM-inDIFF	01111100	R_{OUT} trim of BGRs in Sec. 4.2 in floating diff.
BG-TRIM-L40	10000011	R_1 trim of BGR in Sec. 4.2 (L = 40μm)
ROUT-TRIM-L40	10000011	R_{OUT} trim of BGR in Sec. 4.2 (L = 40μm)
BG-TRIM-L120	01111101	R_1 trim of BGR in Sec. 4.2 (L = 120μm)
ROUT-TRIM-L120	10000010	R_{OUT} trim of BGR in Sec.4.2 (L = 120μm)
BG-TRIM-SW-L40	01111100	R_1 trim of BGR in Sec. 4.3 (L = 40μm)
ROUT-TRIM-SW-L40	10000011	R_{OUT} trim of BGR in Sec. 4.3 (L = 40μm)
BG-TRIM-SW-L120	01111101	R_1 trim of BGR in Sec. 4.3 (L = 120μm)
ROUT-TRIM-SW-L120	10000010	R_{OUT} trim of BGR in Sec. 4.3 (L = 120μm)
CLK-SEL	1	Selects the source of CLK input for current switches
ENB-RINGO	0	Enables ring oscillator as an internal CLK
SEL-RINGO	11	Selects the frequency of ring oscillator
ENB-SW-L40	1	Enables input sig. for inv. of BGR in Sec. 4.3 (L = 40μm)
ENB-SW-L120	1	Enables input sig. for inv. of BGR in Sec. 4.3 (L = 120μm)

APPENDIX A.2: Test Setups for the Measurement of the Designed BGRs

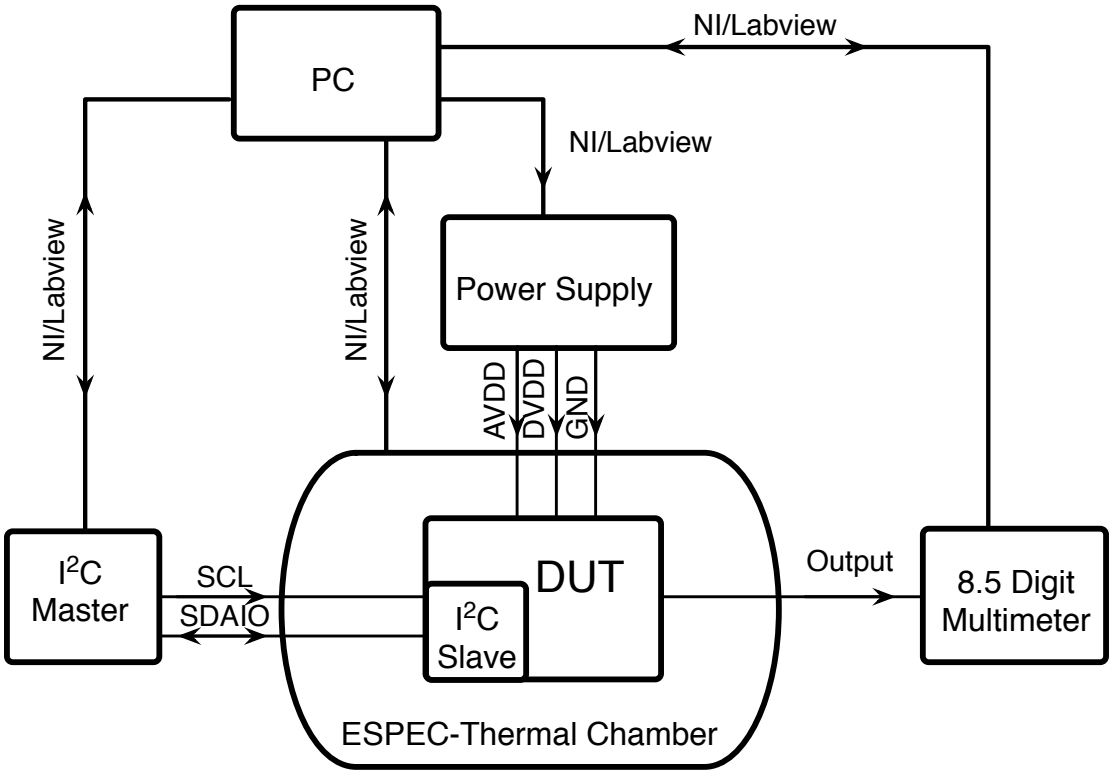

Figure A.3: The test setup utilized for the temperature characterization of the BGR circuits.

Figure A.3 shows the test setup utilized for the temperature characterization of the BGR circuits. Each measurement instrument is controlled by NI/Labview environment. For the TC measurements, firstly the value of R_{OUT} is set in order to have its desired output voltage level at nominal temperature by changing R-OUT-TRIM bits via I^2C interface. Then, with the control loop formed in the Labview environment, the output voltage data is sampled/collected by 8.5 digit multimeter after thermal chamber is settled to the required temperature. For each temperature, desired number of BG-TRIM bits are changed via I^2C interface while the thermal chamber keeps the temperature constant until the end of the data sampling process of multimeters and then the process continues with the next temperature level. The temperature range and number of trim data is controlled by the model established in Labview.

Figure A.4 shows the test setup utilized for the power supply rejection characterization. As seen in the figure, since outputs of the designed BGRs are high impedance, first a low noise amplifier in unity gain configuration with ($R_1 = R_f = 10$ kΩ) is utilized in order to drive 50 Ω input impedance of the spectrum analyzer. Moreover, an AC coupled op-amp circuit with an external capacitor $C_1 = 20$ mF is used to have the lower cut-off frequency of the system is less then 0.1 mHz which will not interfere with the measurements, since the minimum frequency of the spectrum analyzer (R&S FSU-26) is 10 Hz. The amplifier used in this setup is a commercial product of Analog Devices (AD-8628) which has a unity gain bandwidth of 1 MHz for a 20 pF of load capacitance [69].

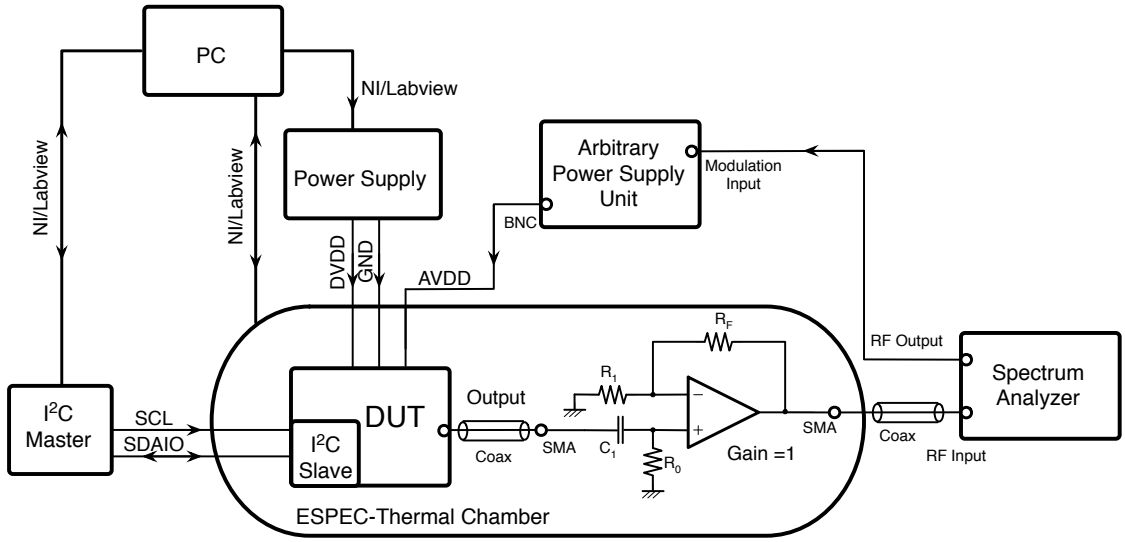

Figure A.4: The test setup utilized for the PSR characterization of the BGR circuits.

An arbitrary power supply unit (Hameg-8143) is used to modulate the power supply signal by generating an FM signal, with its modulation source is the frequency signal from the spectrum analyzer output. which is provided from spectrum analyzer, to its modulation input. Then, the modulated power supply signal is used as the power supplies of the BGR circuits (AVDD), while the digital power supply (DVDD) for the I^2C is driven from an other power source without modulation. These measurement setup makes possible to obtain PSR values as a function of frequency in which the power of the modulation signal, the frequency range and the resolution bandwidth of the PSR sweeps are determined through the spectrum analyzer.

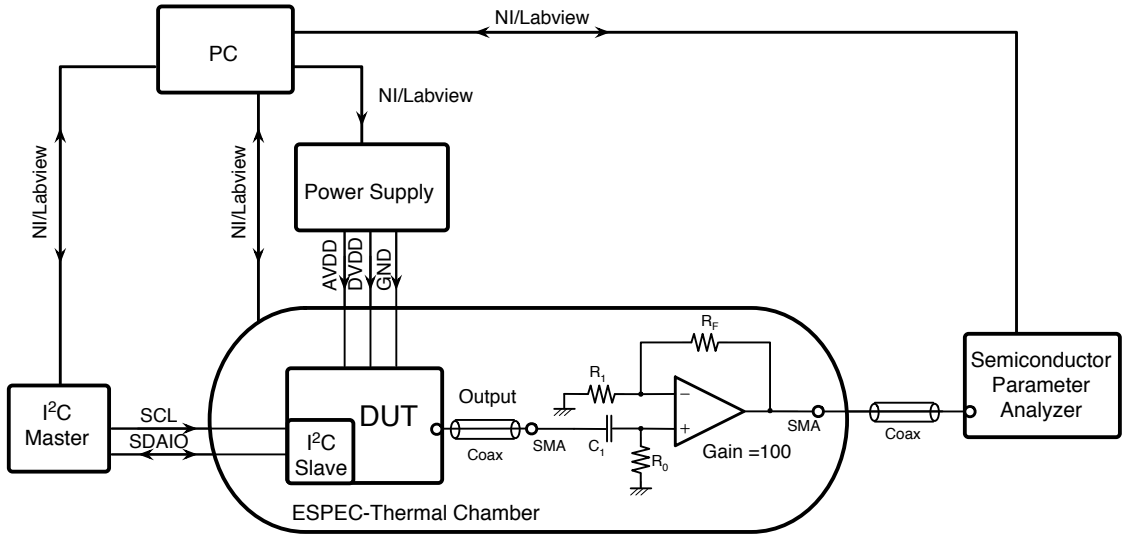

Figure A.5: The test setup utilized for the low frequency noise characterization of the BGR circuits.

As in all noise measurements, first it has to be verified that the noise floor of the instrument should be lower than the DUT. Figure A.5 shows the test setup utilized for the low frequency noise characterization of the BGR circuits. Since it has been observed that the noise floor of the measurement instrument (semiconductor analyzer) is higher than the estimated/simulated noise level of some of the BGR circuits, output

noise is increased above the noise floor of the instrument by configuring a low noise amplifier with a gain of 100. The amplifier used in this setup is the same with the one in PSR measurement setup. However, it should be noted that this configuration will limit the high frequency bandwidth to about 10 kHz. Bandwidth limitation caused by using op-amp in high gain configuration will not affect the measurements since this setup is intended for low frequency noise measurements in the range of 0.1 Hz to 10 Hz.

The frequency range of interest (0.1 Hz to 10 Hz) is also the one of the reasons for using the semiconductor parameter analyzer to collect the data for power spectral noise density instead of the spectrum analyzer, which has minimum frequency of 10 Hz. While collecting the data, the semiconductor parameter analyzer is used in Sampling I/V using with its high resolution ADC. During the measurements, 100001 (limit of the instrument) data point taken with a sampling frequency of $f_s = 100$ Hz, therefore the resolution bandwidth of the power spectral density is 1 mHz.

Moreover, in order to extract/calculate the noise of the DUT (BGR circuit), first noise floor/contribution of the system is measured by connecting the input of the amplifier to the ground. Then, the same measurement is repeated by connecting DUT to the input of the amplifier. Hence, the noise of the DUT (v^2_{n-DUT}) can be calculated/obtained from

$$v^2_{n-total} = v^2_{n-noDUT} + (A_v v_{n-DUT})^2 \tag{A.1}$$

where $v^2_{n-total}$ is the measured output noise power of the configuration seen in Figure A.5 including DUT, $v^2_{n-noDUT}$ is the measured output noise contributed from just the amplifier and the system itself, and A_v is the gain of the amplifier configuration which is 100 in the proposed setup.

APPENDIX A.3: Switched Biasing Technique BGR Design

The low frequency (flicker) noise in MOSFETs increases with shrinking device dimensions, so new generations of sub-micron CMOS technologies tend to have higher 1/f noise corner frequencies where flicker noise dominates white thermal noise. Therefore, low frequency noise has larger effect in limiting noise performance of the circuits. In this section, the BGR circuit designed in Section 4.2 is modified to incorporate switched biasing technique proposed in [54] in order to reduce the low frequency noise of the designed BGR.

Flicker (1/f) Noise in MOSFETs

The flicker noise or simply $1/f$ noise in MOSFETs is such that it has a power spectral density which is inversely proportional to frequency f and the MOS gate area $(W \times L)$. Although exact mechanism behind flicker noise is still under investigation (lacking), it has been cleared out in [70] that the random telegraphic signal (RTS) noise plays significant role in the low frequency noise performance of MOSFETs. There are two main theories that have been proposed to explain physical origins of the flicker noise in MOSFETs: carrier number fluctuation and mobility fluctuation. Both of these theories are based on fluctuation of the conductivity of MOS transistors $(\sigma = \mu\ n\ q)$ where μ and n are the mobility and the concentration of the carriers, respectively. Therefore, a fluctuation of the conductivity is due to either a fluctuation of the number of carriers or a fluctuation in the channel mobility.

Carrier number fluctuation theory, originally proposed by McWhorter [71], considers flicker noise as a result of the surface potential fluctuation and modulation of the charge carrier density due to trapping and detrapping random process of charges in the traps at the $Si - SiO_2$ interface [72]. Trapping and detrapping process from a single trap leads to an RTS. Each trap is characterized by a relaxation time τ that depends on the mean time needed for the trapping process and the mean time needed for detrapping. For a uniform oxide trap distribution in the energy gap, by superposing the RTS signals due to each traps, theory predicts an input referred noise power, given by **A.2**, independent from gate bias but inversely proportional to the square of gate capacitance C_{ox} (or square of oxide thickness t_{ox}) [73].

$$S(f) \approx \frac{K}{f}(\Delta N)^2 \quad for \quad 1/2\pi\tau_2 \ll f \ll 1/2\pi\tau_1 \tag{A.2}$$

where (ΔN) is fluctuation of number of carriers, K is a constant associated with the device. Even if there are many experiment results reported in literature [74–76] that are supporting number of carrier fluctuation theory, the two main lacking point of this theory are the assumptions that traps are isolated and do not interact with each other and each of the traps are coupled to the output current in the same way.

However, mobility fluctuation theory considers flicker noise as a result of the fluctuation in bulk mobility based on Hooge's empirical relation for the noise spectral density of homogenous layers:

$$\frac{S_I}{I^2} = \frac{\alpha_H}{fN} \tag{A.3}$$

where I is the mean current flowing through the sample, S_I is the spectral density of the noise affecting the current, N is the total number of free carriers, and α_H is the Hooge's RTS parameter which is an empirical constant taking values in the range 10^{-6} - 10^{-4} [77]. By applying this relation to MOSFETs, theory predicts an input referred noise power proportional to the gate bias and inversely proportional to the gate capacitance $((V_{GS} - V_{th})C_{ox}^{-1})$ [78].

Since the extensive analysis of flicker noise in MOSFETs has a more complicated dependence on gate bias and on the oxide thickness, a uniformed model that assumes correlated mobility and carrier number fluctuations has been proposed by Hung et al [73]. In this uniformed model, carrier number fluctuations theory dominates at low gate bias while mobility fluctuation theory dominates at high gate bias levels.

Reduction of Flicker Noise and Switched Biasing Technique

Since the flicker noise in MOSFETs in sub-micron technologies are tend to increase, it is important to reduce $1/f$ noise in order to improve the noise performance of the circuit. From the design aspect, the main controllable parameters are W and L of the transistors and its biasing. However, changing biasing is not a practical solution, since many important performance parameters of the circuits such as gain, signal swing, transfer function and linearity are strongly bias dependent. Increasing gate area ($W \times L$) while keeping W/L ratio constant has less effect on many of the performance parameters, but causing speed reduction due to the increase in gate capacitance together with the obvious area penalty.

On the other hand, there are known circuit techniques reported in the literature to reduce the effect of $1/f$ noise. One of these techniques is keeping MOS transistor in triode region with $V_{DS} = 0$, so that noise current becomes zero. However, the utilization of this technique is limited with resistive circuits such as current dividers [79] or transconductors [80], since in triode region MOSFET can have a maximum intrinsic voltage gain of 1. Therefore, it cannot be a solution for circuits requiring voltage gain in which MOS transistor should operate in saturation region. Moreover, there are also techniques such as chopper stabilization, auto-zeroing and dynamic element matching to reduce the DC offset and drift. Since at low frequencies $1/f$ noise is not distinguishable from drift, reduction of $1/f$ noise is also achieved by utilizing these techniques. However, the reduction is limited mostly by device mismatches and charge injection.

These stated techniques reduce the effect of $1/f$ noise in circuits, while in [54] the switched biasing has been proposed as a technique for reducing the $1/f$ noise itself not its effect. The technique is based on intriguing physical effect: cycling a MOS transistor between strong inversion and accumulation reduces its intrinsic $1/f$ noise [81].

In Figure A.6, the idea of cycling an NMOS transistor between strong inversion and accumulation is illustrated. The gate-source voltage applied to the transistor is switched between two levels: the high level $V_{GS,on}$ which is higher than the threshold voltage in order to bias the transistor in strong inversion and the low level $V_{GS,off}$ which equal to or less than threshold voltage so that depending on its value, $V_{GS,off}$ state corresponds to biasing the transistor in moderate inversion, weak inversion or accumulation. If the duty cycle of switched biasing is 50 % and $V_{GS,off}$ equal to V_{th}, the resulting noise power in baseband is $(1/2)^2$ (or -6 dB) when compared to the $1/f$

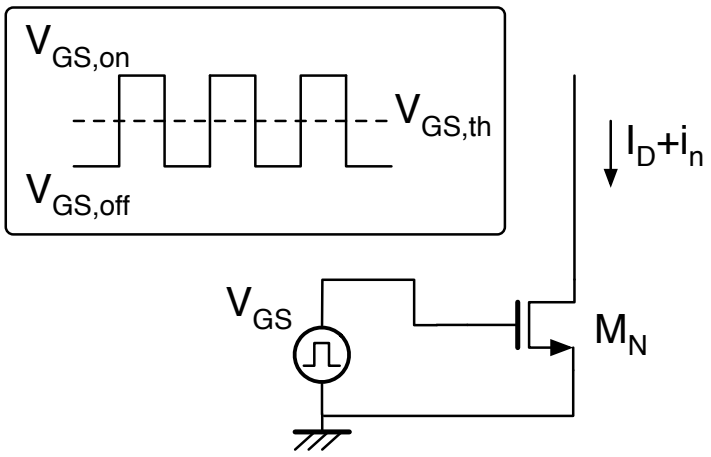

Figure A.6: Concept of switched biasing by an NMOS transistor cycling between operation state and rest-state.

noise power of constant bias scheme that can be explained by modulation theory [54]. Moreover, when $V_{GS,off}$ is decreased below V_{th} down to a value that corresponds to accumulation, measurement results show that further noise reduction up to 8 dB achieved [82].

Modeling low frequency noise under switched bias conditions

As already stated, it has been cleared out in [70] that random telegraphic signal (RTS) noise plays significant role in the low frequency noise performance of MOSFETs. RTS noise in a MOSFET is caused by a so-called "trap" which is a localized energy state in the bandgap that has an energy level between the conduction band energy level (E_c) and the valance band energy level (E_v). Trapping behaviour in a MOSFET is governed by Fermi-Dirac statistics, as described in the classical Shockley-Read-Hall (SRH) model for trapping and detrapping [83]. The traps that are close to the conductance band edge interact with the conductance band, and traps that are close to the valence band edge will interact with the valence band. Therefore, traps that dominate the low frequency noise of NMOS transistors are the ones close to the conductance band while the same behaviour/contribution is valid for the traps near valance band for PMOS transistors.

For an NMOS transistor, a trap near the conductance band can interact with the conductance band by capturing or releasing an electron thus cause RTS noise in two ways: Firstly, it is changing the number of charge carriers, known as ΔN effect, since the electron captured will no more take part in the conduction process. Secondly, a trap will be negatively charged after capturing an electron which has an effect of modulating the position of the channel that is known as " Coulomb scattering" or $\Delta\mu$ effect.

The RTS noise has two discrete states, low and high, and it is observed in a MOS device as a fluctuation in the drain current via aforementioned reasons. Considering an NMOS transistor, it is possible to associate the mean time spent in the high current state with capture time (τ_c) and the mean time spent in the low current state with emission time (τ_e). When τ_c and τ_e are constant, RTS noise is stationary with a Lorentzian power spectrum (S_{RTS}), as shown in Figure A.7 [84]. Ignoring DC term, S_{RTS} can be expressed as

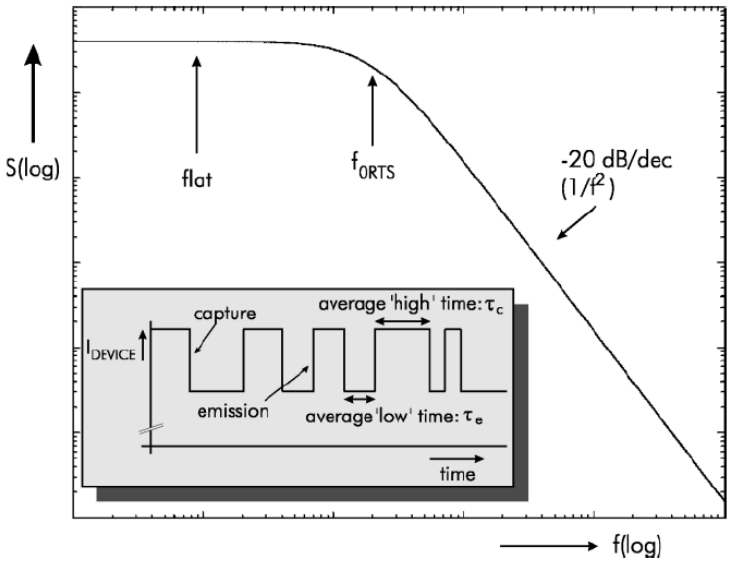

Figure A.7: Time and frequency representation of a stationary RTS.

$$S_{RTS}(f) = 2(\Delta I)^2 \frac{\beta}{(1+\beta)^2} \frac{1}{f_{0,RTS}} \frac{1}{1+\left(f/f_{0,RTS}\right)^2} \tag{A.4}$$

where ΔI is the current steps observed in the drain current, β is a parameter defined as a ratio between the capture and emission time constants ($\beta = \tau_c/\tau_e$), and $f_{0,RTS}$ is the RTS corner frequency:

$$f_{0,RTS}(f) = \frac{1}{2\pi}\left(\frac{1}{\tau_c} + \frac{1}{\tau_e}\right) \tag{A.5}$$

The last term of **A.4** defines the frequency dependence of the power spectrum which is flat at low frequencies and decaying with -20dB/decade above the RTS corner frequency. The corner frequency only depends on τ_c and τ_e while low frequency PSD depends on asymmetry factor β. When $\beta = 1$, an RTS has maximum contribution to the low frequency noise while for strongly asymmetric RTS noise (β far from 1), the low frequency PSD will be small. Even though the PSD of an RTS decays with $1/f^2$ instead of $1/f$, as for $1/f$ noise, the addition of many Lorentzians with different corner frequencies lead to a $1/f$-like spectrum.

The parameters of RTS noise in a MOS transistor are its amplitude, and mean time before capture (τ_c) and emission (τ_e) of an electron. According to the Shockley-Read-Hall theory, these time constant can be expressed as follows on the basis of Fermi-Dirac statistics [83]:

$$\begin{aligned} \tau_c &= \left[n\sigma(E,x)\, v_{th}\right]^{-1} \\ \tau_e &= \left[N_c\sigma(E,x)\, v_{th} exp\left(-E/kT\right)\right]^{-1} \end{aligned} \tag{A.6}$$

where $\sigma(E,x)$ is the capture cross section, effective area within which an electron is captured by a trap, of the trap that depends on the energy level of the trap ($E = E_c - E_T$)

and its depth in the oxide (x), v_{th} is the thermal velocity of the electrons, n is the electron density in the conduction band and N_c is the effective density of states in the conduction band. Moreover, under constant bias conditions capture and emission rates of traps should be equal with respect to the balance principle. According to the **A.6**, τ_c can be varied by changing V_{GS}, since it is bias dependent via the bias dependency of the carrier density, while τ_e seems to be independent of applied V_{GS} because energy level of the trap, E, is independent of V_{GS}. However, that holds for traps located exactly at $Si-SiO_2$ interface, E can be bias dependent if the trap is located some distance in the oxide thus E depends on V_{GS}. Measurements of bias dependency of τ_c and τ_e in NMOS transistors presented in [70, 85] revealed that as V_{GS} is decreased, the probability of a trap being full decreases (τ_c increases) and the probability of a trap being empty increases (τ_e decreases). The change in τ is commonly up to two orders of magnitude. Therefore, to explain/model the RTS noise under switched biasing conditions, effective RTS time constants have been derived in [86] with the assumption of τ_c and τ_e are instantaneous functions of the V_{GS}.

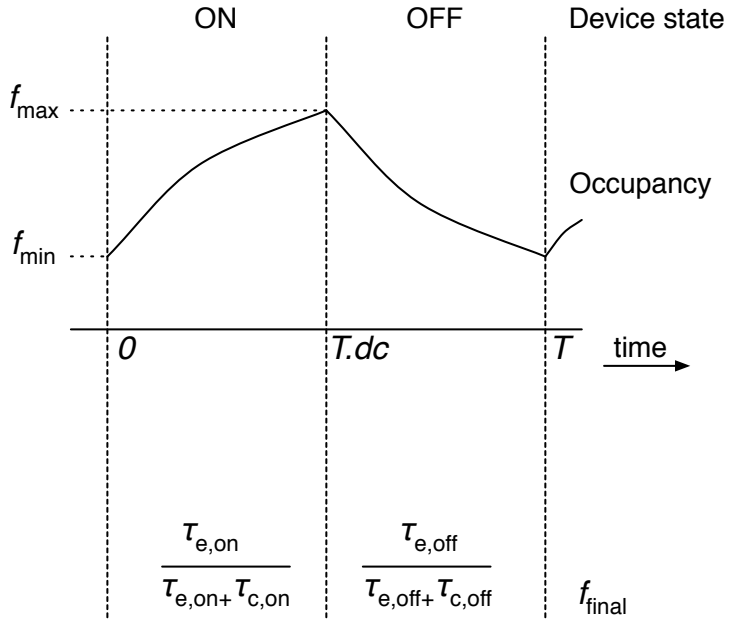

Figure A.8: Occcupancy of trap when device is cycled on and off.

Figure A.8 shows the model for the expected trap occupancy for an NMOS transistor under switched bias conditions. An exponential increase and decrease of occupancy is predicted according to SRH theory. In this model, it has been shown that a cyclo-stationary RTS can be described with a constant occupancy which is function of the effective/equivalent cyclo-stationary capture and emission times ($\tau_{c,eff}$, $\tau_{e,ff}$) if the switching frequency is sufficiently higher than the RTS corner frequency. The expressions for effective time constants are

$$\tau_{c,eff} = \left[\frac{dc}{\tau_{c,on}} + \frac{1-dc}{\tau_{c,off}}\right]^{-1}$$
$$\tau_{e,eff} = \left[\frac{dc}{\tau_{e,on}} + \frac{1-dc}{\tau_{e,off}}\right]^{-1} \qquad \textbf{(A.7)}$$

where dc is the duty cycle of the switched bias waveform with the period T, $\tau_{c,on}$ and $\tau_{e,on}$ are the capture and emission time constants, respectively, when the device is on ($t = 0...T.dc$) and $\tau_{c,off}$ and $\tau_{e,off}$ are the capture and emission time constants, respectively, when the device is off ($t = T.dc...T$).

The properties of PSD of the stationary RTS given in (**A.4**, **A.5**) are also holds for the switched bias case with the derived effective time constants. Therefore, the behaviour of a single RTS under switched bias conditions can be predicted. However, practically in devices there are multitudes of traps and it has to be explain total behaviour. For this reason, a physical model that relates the RTS noise in MOSFETs to the interface trap energy distribution has been proposed in [86]. In this model, behaviour explained in terms of number of traps, the location of traps in the oxide and the energy level of traps.

As stated before, for stationary RTSs (or traps) the dominant noise contributors are the ones with $\beta = \tau_c/\tau_e$ close to 1. When the transistor subjected to switched biasing, the effective RTS time constants are changing due to their bias dependence. If τ_c and τ_e is modelled in a simple way as $\tau_{e,off} = \tau_{e,on}/m_e$ and $\tau_{c,off} = \tau_{c,on}.m_e$, respectively, in order to take consideration the bias dependence, by substituting them in **A.7** with 50 % the effective capture and emission time constants can be written as follows

$$\begin{aligned} \tau_{c,eff} &= \left(2m_c/\left(m_c+1\right)\right)\tau_{c,on} \\ \tau_{e,eff} &= \left(2m_e/\left(m_e+1\right)\right)\tau_{e,on} \end{aligned} \qquad \textbf{(A.8)}$$

where m_c and m_e are bias dependence coefficients of capture and emission time constants. As a result, the effective RTS time constants and their asymmetry factor β with respect to steady state is changed which means that the main contributors of the PSD is not the same traps any more. Note that the shape of the noise contribution curve does not change, it has been shifted. In other words, for constant biasing in strong inversion, traps close to the conduction band dominate the contribution to the low frequency noise while for switched biased case, traps located closer to the middle of the bandgap become dominant. Therefore, there shouldn't be any change in noise spectrum, if the distribution of traps in energy is uniform in all over the bandgap. However, distribution of traps commonly U-shaped with a lower trap density near the centre of the bandgap according to the reported literature [87]. This result is consistent with the measurements reported in the literature showing that low frequency noise of MOSFETs reducing under the switched bias conditions.

Implementation of switched biasing technique

With the knowledge of the $1/f$ noise reduction effect, the switched biasing technique has been proposed in [54]. In the technique, a MOS transistor is periodically switched between two states, "operation-state" and "rest-state", instead of applying a constant gate-source voltage. In the operation-state, transistor is in strong inversion thus active in the circuit operation (i.e. delivers biasing current), while in the rest-state, transistor is in or close to accumulation thus not active in the circuit operation. The intentional switching-off of the MOS transistor (rest-state) is introduced in order to reduce the $1/f$ noise of the MOS transistor during its operational state. In addition, it reduces the power consumption. Even if periodically switching transistors between these

two states is not appropriate for all kind of circuits without affecting correct circuit operation, there are some circuits, in which a bias current is needed only certain time intervals or signal processing is not taking placing continuously, giving this freedom. For instance, in many types of oscillators the transistor contribute actively to the circuit operation during only a part of oscillation and application/implementation examples of the switched biasing technique in a sawtooth and LC oscillators have been reported in [82, 88].

In order to implement switched biasing technique to the structures/circuits in which the bias current required continuously, complementary switched biasing scheme is needed. Figure A.9 shows the complementary switched biasing scheme to draw the current continuously. Complementary ON-OFF operations between two transistors are possible by applying differential signals.

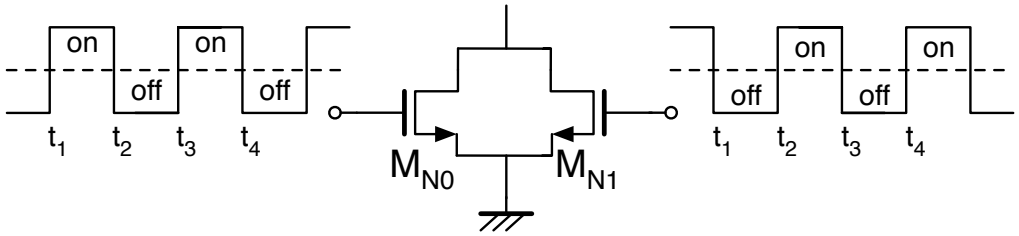

Figure A.9: Complementary switched biasing scheme with differential signals.

Implementation

From the noise analysis of the BGR circuit given in Section 4.2, the dominant noise sources of the circuit at low frequency are the transistors M_{N0}, M_{N1} and M_{N4}. Therefore, in order to improve the low frequency noise performance of the circuit, it is required to reduce the flicker noises of these transistors. The straightforward method to do it in terms of the design parameters is increasing the gate areas ($W \times L$) of the transistors while keeping the aspect ratios (W/L) constant at the cost of area and bandwidth of the circuit.

However, with the knowledge of the switched biasing technique which has been mostly applied to different kinds of oscillator circuits till now in the reported literature, the designed/proposed BGR circuit in previous section is modified in order to apply the switched biasing technique. Figure A.10 shows the schematic diagram in which complementary switched biasing scheme is utilized at NMOS current mirrors to improve the low frequency noise performance. The current switching is achieved/implemented using the inverters which are forcing the sources of the NMOS transistors that are forming the current mirrors. Since the effect of the operating point cycling on MOS flicker noise is not modeled and cannot be simulated, the strategy is to make sure the simulated noise performance of the circuit remains unchanged when switching is enabled. Therefore, a simple digital circuit, which is pulling up the inputs of the inverters in order to disable the bias switching and giving the phase signals Φ_{SB} and $\overline{\Phi_{SB}}$ in order to enable switching, is added to the system to assess the noise improvement during measurement.

Once the bias switching is enabled, M_{Ni} and $M_{Ni,c}$ where $i = 0-4$ are turned on and off in a complementary fashion. Hence, one of the two biasing transistors is ON at all times. Therefore, the achieved noise performance improvement will be related to the

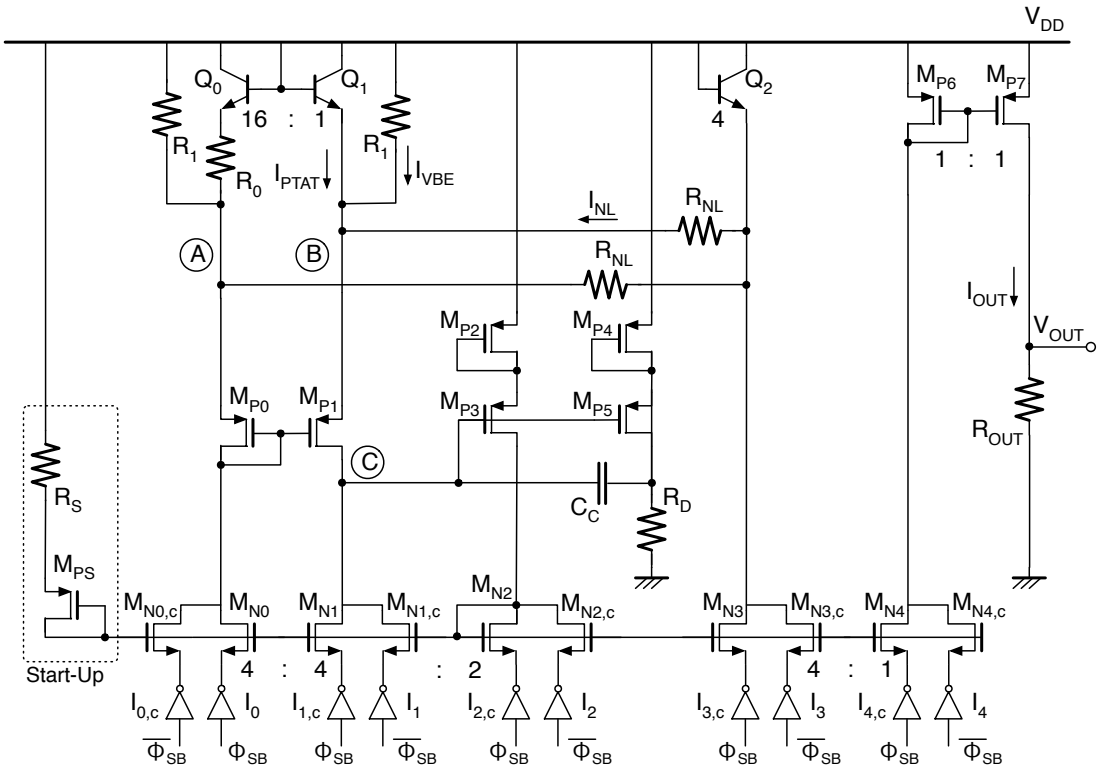

Figure A.10: Schematic diagram of the BGR with complementary switched biasing technique.

flicker noise reduction of the device itself during its operation state due to the switched biasing.

Figure A.11 shows the schematic diagram of the inverters utilized to implement bias switching scheme. It is more advantageous to turn on and off the current source transistors by disconnecting their source terminal with an inverter rather than turning them on and off through their gate terminal voltage. Upon disconnecting, their source voltage rises to the value V_{MAX} to turn off the device. This way, the bias voltage is not disturbed and the inverter can be driven with digital signals. Note that V_{MAX} is a voltage provided from an external voltage source, hence the value of V_{MAX} can be determined independently to cycle the current source transistors between inversion and accumulation regions. Moreover, this scheme makes possible to observe the effect of $V_{GS,off}$ value in the switched biasing technique by setting different values for V_{MAX}.

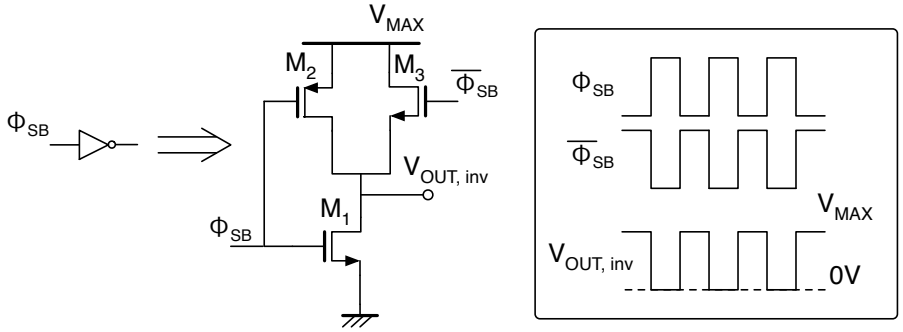

Figure A.11: Schematic diagram of the inverters utilized in the proposed switched biased BGR circuit.

The additional NMOS transistor, M_3 in the inverter schematic is required in order to be able to set the value of the V_{MAX} below the threshold of the PMOS transistor $V_{th,p}$. The transistor sizes of the inverters determined such that the threshold voltages of the inverters equal to $V_{MAX}/2$ In the design of inverters. Thus, W/L ratios of the PMOS transistors are 3 times larger than the one of NMOS transistors, since $\mu_n/\mu_p \approx 3$ for the technology. Furthermore, note that the loads of the inverters are not equal. Hence, the transistor sizes of the inverters determined with respect to its load in order to equalize the propagation delays and rising and falling times of the signals at the sources of bias transistors eventhough all the inverters are seeming identical in Figure A.10. As a result, the driving capabilities of the inverters I_0, $I_{0,c}$, I_1, $I_{1,c}$, I_3 and $I_{3,c}$ are 2 times larger than the one of I_2 and $I_{2,c}$ and 4 times larger than the one of I_4 and $I_{4,c}$.

Figure A.12 shows the schematic diagram of the ring oscillator by using standard digital gates to provide the digital input signal in order to have a fully integrated BGR scheme. And via a digital logic consists of XOR gates, Φ_{SB} and $\overline{\Phi_{SB}}$ are generated symmetrically. The output frequency of the ring oscillator is 32 MHz divided by four different values (2, 4, 8, 16), therefore the output frequency of the designed ring oscillator can be set to different values via a simple MUX in order to be able to observe the effect of switching frequency on noise performance of the circuit. Figure A.13 shows the layout of the designed digital ring oscillator occupying an area of 30 x 140 μm^2

Note that the circuit designed such that the digital clock signal required for inverters can also be provided from external source that can be controlled via the digital I^{2}C block which is also controlling ENB signal of the the designed ring oscillator.

Simulation Results

The switched bias BGR circuit is designed and implemented in a 0.35 μm 3.3 V triple-well CMOS technology having vertical NPN BJT transistors. The layout of the circuit without the ring oscillator occupying a silicon area of of 450 x 300 μm^2 is given in Figure A.14.

Figure A.15 shows the transient response of the designed/modified BGR circuit, where switched frequency is 5 MHz. Moreover, the results obtained through post-layout

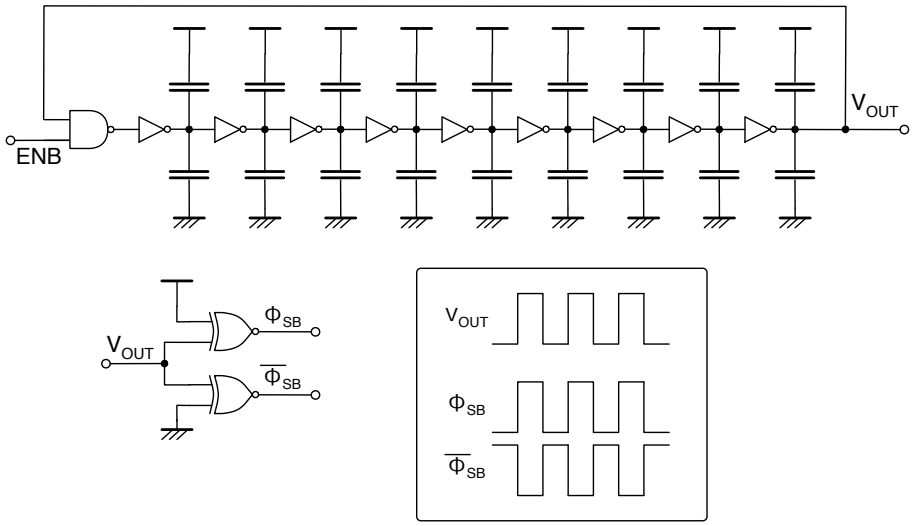

Figure A.12: Schematic diagram of the ring oscillator.

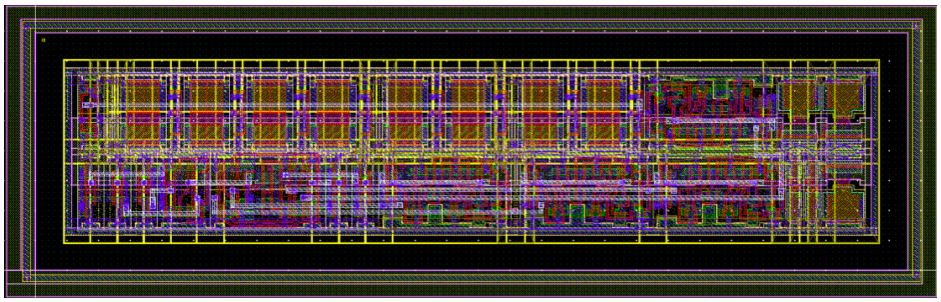

Figure A.13: Layout of the ring oscillator.

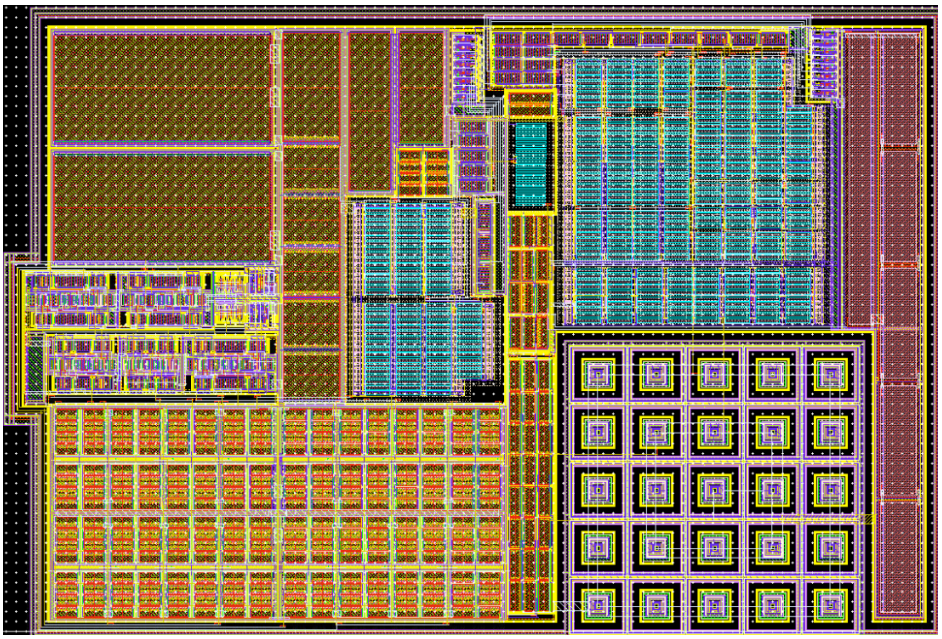

Figure A.14: Layout of the BGR with complementary switched biasing technique.

periodic steady sate simulations (pas, pac, pnoise) shows that performance parameters of the circuit even the noise performance are not affected from the modifications to implement switched biasing technique. Since the flicker noise models of the MOS transistors are not including the operating point cycling effect, it is not possible to simulate it in our design environment. Therefore, while implementing the switched biasing technique the strategy has been to make sure the simulated noise performance of the circuit remains the same when switching is enabled.

Figure A.16 shows the the simulated noise power spectral densities of BGR circuits with constant and switched biasing cases. As seen from the figure, noise performance of the circuit remaining same. Hence, to avoid from repetition of same figures/graphics, simulation results summarized. The designed BGR circuit generates a reference voltage of 220.1 V while consuming 32.1 μA current from 3.3 V supply voltage. The temperature coefficient of the reference voltage is 1.65 ppm/°C for nominal process corner over a temperature range of -40 °C to 125 °C. The PSR performance of the circuit is -71.68 dB at 100 Hz. Its peak-to-peak output noise integrated from 0.1 Hz to 10 Hz is 12.35 μV (rms 2.058 μV). The designed BGR circuit occupies an area of 450 x 300 mm^2.

Summary

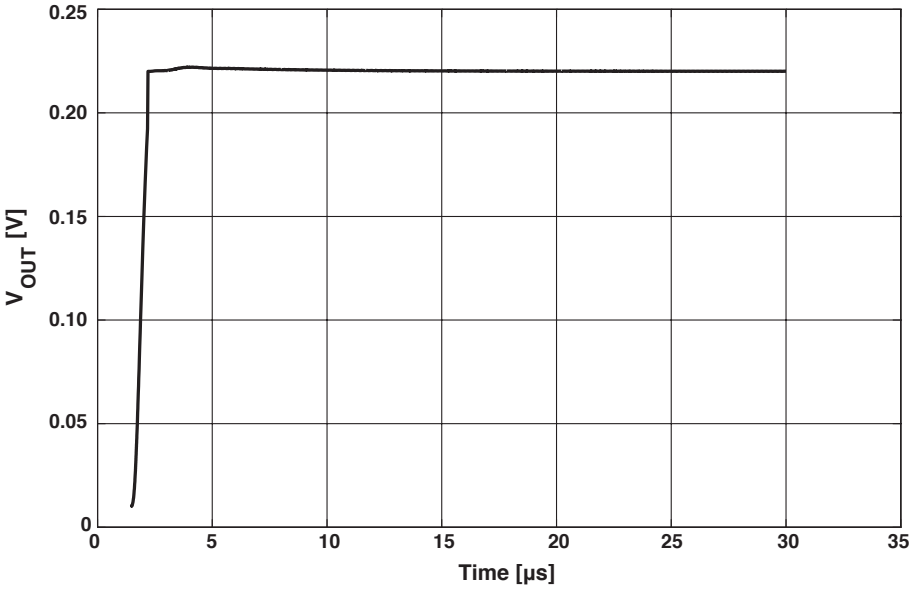

Figure A.15: Transient response of the BGR with complementary switched biasing technique.

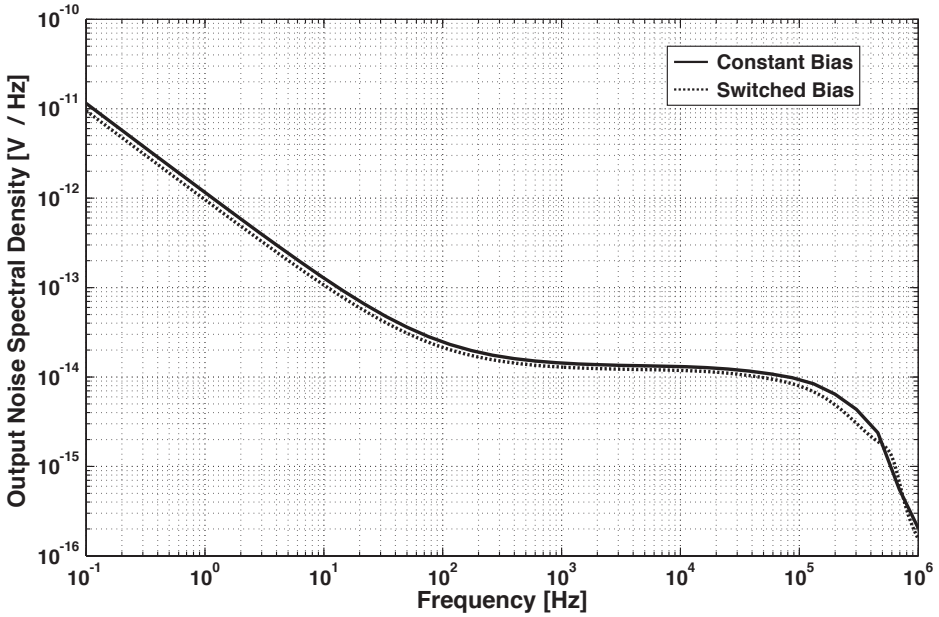

Figure A.16: Output noise spectral density of constant bias and switched bias schemes.

Conventional/straight-forward solution (increasing device area) for reducing flicker noise of the MOSFETs has well-known drawbacks such as limiting the bandwidth, increasing the area. Therefore, in Section 4.3, in order to improve the low noise performance of the designed BGR in Section 4.2, the circuit modified to incorporate an alternative and relatively new circuit technique called switched biasing which is proposed in [54]. The effect of operating point cycling on flicker noise of MOSFETs is not modelled, thus this effect cannot be observed in the simulation results as shown Figure A.16. Therefore, during the design and implementation of the technique, the strategy has been to make sure the simulated noise performance of the circuit remains the same when switching is enabled. The remaining circuit performance are also

not affected from the modification in order to implement switched biasing, they are almost same with the one given Section 4.2. The measurements of the designed circuit utilizing the switched biased technique is on going.

CURRICULUM VITAE

Name Surname: Pınar Başak Başyurt

Place and Date of Birth: Kırıkkale, 1983

E-Mail: basyurt@itu.edu.tr

B.Sc.: Istanbul Technical University, Electronics and Communication Engineering

M.Sc.: Istanbul Technical University, Electronics Engineering

Professional Experience and Rewards: Istanbul Technical University, Research Assistant

List of Publications and Patents:

▪ Aksin D. Y., **Basyurt P. B.**, Uyanik H. U., 2009. Frequency Synthesis Using Pulse Width Locked Loop. *Proceedings of IEEE International Symposium on Radio-Frequency Integration Technology*, 9-11 December 2009, Singapore.

▪ Aksin D. Y., **Basyurt P. B.**, Uyanik H. U., 2009. Single-Ended Input Four-Quadrant Multiplier for Analog Neural Networks. *Proceedings of ECCTD 2009: European Conference on Circuit Theory and Design*, 23-27 August 2009, Antalya, Turkey.

▪ Ates E. O., Aksin D. Y., **Basyurt P. B.**, 2009. CMOS Colpitts LC Reference Oscillator with 70 ppm Absolute Frequency Accuracy within 0 – 80 C. *Proceedings of MWSCAS 2009: The 52nd IEEE International Midwest Symposium on Circuits and Systems*, 2-5 August 2009, Cancun, Mexico.

▪ **Basyurt P. B.**, Tarim N., 2008. An X-Band Low Noise Amplifier with High Gain and Low Noise Figure. *Proceedings of ISCCSP 2008: The 3rd International Symposium on Communications, Control and Signal Processing*, 12-14 March 2008, St. Julians, Malta.

▪ **Basyurt P. B.**, Tarim N., Kuntman H., 2006. Realization of a CMOS Differential Voltage Current Conveyor and Its Applications. *Proceedings of ISEECE 2006: The 3rd International Symposium on Electrical, Electronic and Computer Engineering*, 3-25 November 2006, Nicosia, North Cyprus.

PUBLICATIONS/PRESENTATIONS ON THE THESIS

▪ **Basyurt P. B.**, Aksin D. Y., 2014. Untrimmed 6.2 ppm/C Bulk-Isolated Curvature-Corrected Bandgap Voltage Reference. *Integration, the VLSI Journal*, *(47)*1, 31–37.

▪ **Basyurt P. B.**, Bonizzoni, E., Aksin D. Y., Maloberti, F. , 2014. Sampled-Data Operational-Amplifier with Ultra-Low Supply Voltage and Sub μW Power Consump-

tion. *Proceedings of IEEE International Symposium on Circuits and Systems*, 1-5 June 2014, Melbourne, Australia.

▪ **Basyurt P. B.**, Aksin D. Y., 2012. Design of a Curvature-Corrected Bandgap Reference with 7.5 ppm/C Temperature Coefficient in 0.35 μm CMOS Process. *Proceedings of IEEE International Symposium on Circuits and Systems*, 21-23 May 2012, Seoul, Korea.

▪ **Basyurt P. B.,** , Aksin D. Y., 2012. Reference with 8.4 ppm/C Temperature Coefficient in 0.35 μm CMOS Process. *Proceedings of IEEE CDNLive 2012*, 14-16 May 2012, Munich, Germany.