Novel Methods for Efficient Realization of Logic Functions Using Switching Lattices

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Abstract—Two-dimensional switching lattices including four-terminal switches are introduced as alternative structures to realize logic functions, aiming to outperform the designs consisting of one-dimensional two-terminal switches. Exact and approximate algorithms have been proposed for the problem of finding a switching lattice which implements a given logic function and has the minimum size, \textit{i.e.}, a minimum number of switches. In this article, we present an approximate algorithm, called \textsc{Janus}, that explores the search space in a dichotomic search manner. It iteratively checks if the target function can be realized using a given lattice candidate, which is formalized as a satisfiability (SAT) problem. As the lattice size and the number of literals and products in the given target function increase, the size of a SAT problem grows dramatically, increasing the run-time of a SAT solver. To handle the instances that \textsc{Janus} cannot cope with, we introduce a divide and conquer method called \textsc{Medea}. It partitions the target function into smaller sub-functions, finds the realizations of these sub-functions on switching lattices using \textsc{Janus}, and explores alternative realizations of these sub-functions which may reduce the size of the final lattice. Moreover, we describe the realization of multiple functions in a single lattice. Experimental results show that \textsc{Janus} can find better solutions than the existing approximate algorithms, even than the exact algorithm which cannot determine a minimum solution in a given time limit. On the other hand, \textsc{Medea} can find better solutions on relatively large size instances using a little computational effort when compared to the previously proposed algorithms. Moreover, on instances that the existing methods cannot handle, \textsc{Medea} can easily find a solution which is significantly better than the available solutions.

Index Terms—emerging technologies, four-terminal switch, switching lattice, logic synthesis, satisfiability, binary search.

1 INTRODUCTION

As the Moore's law [1], \textit{i.e.}, the number of transistors doubles in the given chip every two years, has been reaching its limit [2], researchers have been exploring new technologies and structures. Nanotechnology, which aims to build materials and devices on the scale of atoms and molecules, has been an emerging technology to tackle the limitations of the conventional CMOS technology [3]. Recent years have seen successful design of memory cores and programmable logic arrays and interconnects using nanotechnologies [4], [5]. Moreover, architectures and structures for the nano-electronic computation, realizing simple logic gates, such as NAND and NOR, and implementing complex logic circuits, such as adders and microprocessors, have been introduced [6], [7], [8], [9], [10].

As shown in [11], a four-terminal switch, developed especially for the cross-points of nanoarrays, can be used to realize logic functions. As illustrated in Fig. 1a, if its control input \(x\) has the value 0, all its terminals are disconnected (OFF). Otherwise, they are connected (ON). In a switching lattice, that is formed as a network of four-terminal switches, each switch is connected to its horizontal and vertical neighbors. A \(3 \times 3\) switching network is shown in Fig. 1b where \(x_1, \ldots, x_9\) denote the control inputs of switches. The lattice function, whose inputs are the control inputs of switches, evaluates to 1 if there is a path between the top and bottom plates of the lattice and is written as the sum of products of control inputs of switches in each path. In a lattice with four-terminal switches, a path is a sequence of switches connected by taking horizontal and vertical moves. Fig. 1c shows the \(3 \times 3\) lattice function \(f_{3\times3}\). A lattice function is unique and does not include any redundant products, \textit{e.g.}, a possible path \(x_1x_3x_2x_1x_1x_7\) in the \(3 \times 3\) switching network is eliminated by the path \(x_1x_4x_7\).

One of the main advantages of using switching lattices is its reconfigurability. As shown in this article, there exists a switching lattice that can be used to realize all logic functions with a certain number of variables. Its another advantage is to reduce the number of switches when compared to the conventional two-terminal switches, such as field-effect transistors, in a given design. As an example, consider \(f(a, b, c, d) = \sum(2, 3, 4, 8, 9, 12, 14, 15)\) which can be written as \(f = \overline{abc} + abc + a\overline{bd} + b\overline{c}d\). Taking into account the most commonly used CMOS technology, its straightforward two-level realization using AND and OR gates, as shown in Fig. 2a, requires 42 CMOS transistors without counting the ones for the inverters of primary inputs. The number of CMOS transistors can be reduced further as follows: i) apply a state-of-art logic synthesis tool to the given logic function using a synthesis script; ii) map the

\[f_{3\times3} = x_3x_6x_7 + x_3x_4x_6 + x_3x_4x_5x_6 + x_3x_5x_4x_6 + x_3x_5x_6x_7 + x_3x_6x_5x_7 + x_3x_6x_5x_6x_7 + x_3x_6x_5x_6x_7 + x_{3x}x_4x_5x_6.\]
design into gates of a given library where the cost value of a gate is defined in terms of the number of CMOS transistors required to build the gate; iii) compute the design complexity in terms of the number of required transistors; and iv) repeat this process for a number of synthesis scripts and keep the design with the least complexity. In this work, we used ABC [12] as a logic synthesis tool, its 17 synthesis scripts, and a gate-library which is the extended version of the mcnc.genlib library. Fig. 2b presents the solution found for our example which requires 26 CMOS transistors without counting the ones for the inverter of a primary input. On the other hand, the realization of \( f \) using the 3 \( \times \) 3 lattice\(^1\), shown in Fig. 2c, needs 9 four-terminal switches.

It is shown in [13] that a four-terminal switch can be developed using the conventional CMOS technology and can be used to form a switching lattice. Fig. 3a and b present two CMOS-compatible devices introduced for the development of the four-terminal switch whose gate structure is square and cross, respectively. In this figure, T1, T2, T3, and T4 stand for the four terminals. Further details on the technology development can be found in [13]. It is confirmed through technology simulations that these devices behave as a four-terminal switch. During the fabrication process in implementation of a four-terminal switch, it is observed that the compact structure of a lattice, shown in Fig. 3c, has a potential to yield significant savings in area. This is mainly because the excessive area due to the placement and routing of transistors and gates [14] does not occur in the design of a switching lattice and the realization of a logic function using a lattice generally needs less number of switches than that in the conventional CMOS realization as shown in Fig. 2.

In recent years, many algorithms have been introduced to realize a logic function on a switching lattice using the fewest number of switches [15], [16], [17], [18], [19], [20]. However, while the exact algorithm [15] can only handle relatively small instances, the approximate algorithms [16], [17], [18], [19] can find solutions that are far away from the minimum. Hence, in this article, we present the approximate algorithm of [20], called JANUS, that can find better solutions using less computational effort when compared to the existing approximate algorithms. It improves the initial boundaries of the search space significantly and uses an efficient SAT formulation for the problem of finding if a given target function can be realized using a given switching lattice. However, as the number of literals and products in a logic function increases, the SAT problem complexity goes beyond the reach of state-of-art SAT algorithms. In order to handle such complex instances that JANUS finds hard to cope with, we introduce a divide and conquer algorithm called MEDEA. It is observed that MEDEA can find solutions using significantly less time than JANUS and its solutions are better than those of the previously proposed approximate algorithms and close to those of JANUS on logic functions with a small number of products. It is shown on the logic functions, which the existing algorithms cannot handle, that the solutions of MEDEA have significantly less number of switches than the best solutions found so far. Finally, in this article, we present an efficient way of realizing multiple functions in a single lattice using the proposed methods.

The rest of this article is organized as follows: Section 2 presents the background concepts, problem definitions, and related work. The proposed algorithms are introduced and the realization of multiple functions in a single lattice is described in Section 3. Experimental results are shown in Section 4 and finally, Section 5 concludes the article.

### 2 BACKGROUND

#### 2.1 Preliminaries

A Boolean function, \( f : B^r \rightarrow B \), over \( r \) variables \( x_1, \ldots, x_r \) maps each truth assignment in \( B^r \) to 0 or 1. The logic function \( f \) in sum of products (SOP) form on \( r \) variables is a disjunction of \( s \) products \( p_1, \ldots, p_s \), where a product \( p_i = l_1 \cdot l_2 \cdot \ldots \cdot l_j, i \leq s \) and \( j \leq r \), is a conjunction of literals. A literal \( l_j, j \leq r \), is either a variable \( x_j \) or its complement \( \bar{x}_j \). A product is an \textit{implicant} if and only if it evaluates to 1 and it is a \textit{prime implicant} if it is an implicant and there exist no other implicants whose literals are subset of its literals. In an \textit{irredundant} SOP (ISOP) form of \( f \), every product is a prime implicant and no product can be deleted without changing \( f \). The \textit{degree} of \( f \) is the maximum number of literals in the products of \( f \). The dual of \( f \) can be computed as \( f^D(x_1, \ldots, x_r) = \overline{f(x_1, \ldots, x_r)} \) and can be found by interchanging the AND and OR operations and the constants 0 and 1 as well. The Shannon expansion of \( f \) is given as \( f = \overline{x_i}f_{\overline{x_i}} + x_i f_{x_i}, 1 \leq i \leq r \), where \( f_{\overline{x_i}} \) and \( f_{x_i} \) stand for the negative and positive co-factors of \( f \) which are computed by replacing \( x_i \) with \( 0 \) and \( 1 \), respectively and include maximum \( r - 1 \) variables.

A Boolean function \( \varphi \) in product of sums (POS) form on \( r \) variables is a conjunction of \( t \) clauses \( c_1, \ldots, c_t \), where a clause \( c_i = l_1 + l_2 + \ldots + l_j, i \leq t \) and \( j \leq r \), is a disjunction of literals. If a literal of a clause is set to 1, the clause is satisfied. If all literals of a clause are set to 0, the clause is unsatisfied. The \textit{satisfiability} (SAT) problem is to find an assignment to
the variables of a function \( \varphi \) in POS form that makes \( \varphi \) to be equal to 1 or to prove that \( \varphi \) is equal to 0. The SAT problem is NP-complete [21].

A combinational circuit is a directed acyclic graph with nodes and directed edges corresponding to logic gates and wires connecting the gates, respectively. The POS formula of a combinational circuit is the conjunction of POS formula of each gate which denotes the valid input-output assignments to the gate. The derivation of POS formulas of basic logic gates can be found in [22]. Fig. 4 shows a combinational circuit and its formula in the POS form.

The 0-1 integer linear programming (ILP) problem is the minimization or the maximization of a linear objective function subject to a set of linear constraints and is generally defined as follows:

\[
\begin{align*}
\text{minimize} & \quad w^T \cdot y \\
\text{subject to} & \quad A \cdot y \geq b, \quad y \in \{0, 1\}^k
\end{align*}
\]

In the objective function given in Eqn. 1, each weight \( w_i \) associated with each variable \( y_i \) is an integer value, where \( 1 \leq i \leq k \). In Eqn. 2, \( A \cdot y \geq b \) denotes the set of \( j \) linear constraints, where \( b \in \mathbb{Z}^j \) and \( A \in \mathbb{Z}^{j \times k} \).

### 2.2 Switching Lattices

#### 2.2.1 Computing the Lattice Function

In a switching lattice, a four-connected path is a sequence of switches connected by taking horizontal and vertical moves and a lattice function includes all irredundant four-connected paths between the top and bottom plates. An eight-connected path is generated by taking diagonal moves in addition and the dual of a lattice function consists of all irredundant eight-connected paths between the left and right plates [11]. For example, the dual of the lattice function \( f_{3 \times 3} \) given in Fig. 1c has 17 products all with three variables. Thus, finding a realization of a target function on an \( m \times n \) switching lattice considering the four-connected paths between the top and bottom plates can also be done by finding a realization of the dual of target function on the same \( m \times n \) lattice considering the eight-connected paths between the left and right plates. This is because taking the dual of a logic function twice leads to the function itself.

Table 1 presents the number of products in the \( m \times n \) lattice function and its dual at the top and bottom of each entry, respectively, where \( 2 \leq m, n \leq 8 \). Similarly, Table 2 shows the degree of the \( m \times n \) lattice function and its dual at the top and bottom of each entry, respectively.

### 2.2.2 Reconfigurable Switching Lattices

Similar to the look-up tables in field programmable gate arrays [23], a switching lattice can be used as a reconfigurable block which can realize all logic functions with \( r \) variables. An upper-bound on the size of such a switching lattice can be determined based on the Shannon expansion in a recursive manner. Fig. 5a presents the realization of the Shannon expansion of a logic function, \( f = x_1 f_{r,x_1} + x_i f_{r,x_i} \), using a switching lattice when \( i \) is \( r \). Since any logic function including 1 variable requires a 1 x 1 lattice, any logic function with 2 variables can be realized using the 2 x 3 lattice as shown in Fig 5b. Note that the co-factors \( f_{\overline{r},x_1} \) and \( f_{2,x_2} \) include maximum one variable, i.e., \( x_1 \). Thus, any logic function with 3 variables can be realized using a 3 x 7 lattice as shown in Fig 5c where the co-factors \( f_{3,x_1} \) and \( f_{3,x_2} \), which
shown to be NP-complete. The lattice mapping function $f$ and an $(LM)$ problem, is defined as: given a target function $f$, find the appropriate lattice function $f_{m,n}$, and maximum two variables, are realized as given in Fig 5b. Hence, to realize any logic function with $r$ variables, an $r \times 2^r - 1$ lattice can be used. Observe that the size of such a lattice grows exponentially as $r$ increases.

On the other hand, by trying all possible logic functions, the switching lattice with the minimum size that can be used to realize any logic function with 2, 3, and 4 variables is found to be the $2 \times 2$, $3 \times 3$, and $3 \times 6$ lattice, respectively. Hence, using the Shannon expansion in a recursive manner, the size of the lattice, which can be used to realize any logic function with $r$ variables when $r \geq 5$, can be formulated as $(r-1) \times (6 \cdot 2^{-r-5} + 2^{r-2} - 1)$. For example, any logic function with 5 and 6 variables can be realized using the $4 \times 13$ and $5 \times 27$ lattice using the new formula rather than the $5 \times 31$ and $6 \times 63$ lattice, respectively.

### 2.3 Problem Definitions

Realization of a logic function using a switching lattice can be obtained by simply mapping the appropriate literals of this target function and/or constant values (0 and 1) to the control inputs of switches. The *lattice mapping* (LM) problem, is defined as: given a target function $f$ and an $m \times n$ lattice function $f_{m,n}$, find the appropriate assignments to the lattice variables such that the target function $f$ can be realized on the $m \times n$ lattice or prove that there exists no such assignment. The LM problem was shown to be NP-complete in [15]. As an example, consider $f(a,b,c,d,e) = \sum_1(1, 6, 7, 14, 17, 21, 24, 25, 30)$ which can be written as $f = abcde + abced + bcde + boede + abde$. It can be realized using the $4 \times 4$ lattice as shown in Fig. 6a and the $5 \times 3$ lattice, but cannot be realized using the $3 \times 3$ lattice.

In the realization of a logic function using a switching lattice, the design complexity is determined as the number of switches, i.e., the lattice size. Thus, the *lattice synthesis* (LS) problem, is defined as: given the target function $f$, find an $m \times n$ lattice such that there exists an appropriate assignment to the lattice variables, realizing $f$, and $m$ times $n$ is minimum. Returning to our example, Fig. 6b presents the realization of the target function on a lattice with the minimum size of $4 \times 3$.

### 2.4 Related Work

Over the years, logic structures and arrays, that provide regularity, reconfigurability, and ease of design, have been introduced to realize logic functions [24], [25], [26]. A structure similar to the switching lattices can be found in [26] where a rectangular logic array is composed of cells, each connecting to its neighbors. Each cell, which is a three-input and two-output circuit, connects the up and right cell to the down and left one based on the input values.

In order to realize logic functions using switching lattices, the recursive method of [27] maps logic functions onto nanowire based crossbar architectures with different topologies rather than using a regular switching lattice structure. In [11], an upper bound on the lattice size is computed by considering common literals in the products of the target function and its dual and the lower bound on the lattice size is obtained based on the minimum degrees of the target function and its dual. The exact algorithm of [15] explores the search space using a binary search technique in between the lower and upper bounds computed in [11]. During this search, for each possible lattice, an LM problem is generated. The LM problem is encoded as a quantified Boolean formula (QBF) problem, the QBF constraints are converted to SAT clauses, and a solution is found using a SAT solver. The approximate method of [15] restricts this exact QBF formulation by allowing the paths to include only the literals in the given products, reducing the size of SAT problems. However, since the approximate method may yield a non-optimal solution, it may solve more LM problems than the exact method. The technique of [17] synthesizes the D-reducible form of a target function, which is composed of two small sub-functions, on a switching lattice. In [17], these sub-functions are synthesized using the algorithm of [15] and then, their solutions are merged into a single lattice. Note that not every logic function can be represented in the D-reducible form. Similarly, the methods of [16], [18] exploit the p-circuits and autosymmetric form of a target function, respectively and use the algorithms of [11], [15] to find a solution on the decomposed sub-functions. In [18], the target function is synthesized with multiple lattices sharing the common ones, but adding extra logic gates which may not be desirable due to the wires between these gates and lattice control inputs. The method of [19] determines a number of promising lattice candidates and uses a method of [15] to find if one of these lattices leads to a solution.

### 3 Proposed Algorithms

In this section, we initially describe the approximate algorithm and then, the divide and conquer method, both developed for the realization of a single logic function using a switching lattice. Finally, we present the method developed for the realization of multiple functions on a single lattice.

#### 3.1 JANUS: An Approximate Algorithm

**JANUS** takes the target function $f$ as an input and finds its implementation on a switching lattice as described below:

1. Determine the lower bound ($lb$) and upper bound ($ub$) of the LS problem in terms of the number of switches.
2. If $lb = ub$, return the solution found while computing $ub$. 

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**Fig. 5.** (a) Realization of $f = \Sigma_1(0, 1, 2, 6, 12, 13, 14, 20, 25, 29, 30)$ using a switching lattice; lattices which can be used to realize any logic function including $r$ variables: (b) $2 \times 3$ lattice when $r$ is 2; (c) $3 \times 7$ lattice when $r$ is 3.

**Fig. 6.** Realizations of $f = abcd + abced + bcde + bde + abde$ using switching lattices: (a) $4 \times 4$; (b) $4 \times 3$. 

3) Determine the middle point as \(mp = \lfloor (lb + ub)/2 \rfloor\) and generate a set of lattice candidates \(C\).
4) For each lattice candidate in \(C\), generate the related LM problem and check if \(f\) can be realized using the lattice candidate. If there exists a solution to the LM problem, set \(ub\) to \(mp\) and go to Step 6. 
5) If there are no solutions for all lattice candidates in \(C\), set \(lb\) to \(mp + 1\).
6) If \(lb < ub\), go to Step 3. Otherwise, return the solution.

In following, we introduce the methods that compute the initial lower and upper bounds of the LS problem (Step 1), describe how the lattice candidates are generated (Step 3), present the encoding of the LM problem as a SAT problem (Step 4), and analyze the SAT problem complexity.

### 3.1.1 Computing the Initial Lower and Upper Bounds

The computation of the initial lower bound of the LS problem takes into account the products of the lattice and target functions and their duals and is described as follows:

1) Find the ISOP forms of the target function and its dual, both including a minimum number of products obtained using a logic minimization tool.
2) Set the lattice size \(ls\) equal to 1.
3) Obtain all possible lattice candidates with the size \(ls\) and apply the structural check procedure to each lattice candidate. If the structural check is passed, return the lower bound computed as \(ls\). Otherwise, try another lattice candidate.
4) If there exist no lattices with the lattice size \(ls\) that pass the structural check, increase \(ls\) by 1 and go to Step 3.

In the structural check procedure, we check for each product of the target function with \(j\) literals if the lattice candidate function has a different product with a number of literals greater than or equal to \(j\). If it is so, similarly, we check if each product of the dual of target function is covered by a different product of the dual of lattice candidate function. In this work, we use espresso [28] as a logic minimization tool. Consider our example in Fig. 2 and assume that \(ls\) is equal to 8. Note that the dual of the target function \(f = \overline{ab}c + abc + \overline{a}bc + b\overline{c}\) is \(f^D = \overline{a}c + \overline{a}d + ab\overline{c} + \overline{a}bd + b\overline{c}d + bde + \overline{b}\overline{c}d\). For the lattice size \(ls\) equal to 8, there exist four possible lattices, \(ie., 1\times8, 2\times4, 4\times2\), and \(8\times1\). There are eight products with only one variable in \(f_{1\times8} = x_1 + x_2 + x_3 + x_4 + x_5 + x_6 + x_7 + x_8\), \(f_{2\times4} = x_1x_5 + x_2x_6 + x_3x_7 + x_4x_8\) has four products each including only two variables, and similarly, \(f_{4\times2} = x_1x_2 + x_1x_4 + x_2x_3 + x_3x_4 + x_5 + x_6 + x_7 + x_8\). Each of these products has only one product in \(f_{8\times1} = x_1x_2x_3x_4x_5x_6x_7x_8\). Hence, the structural check confirms that all these lattices cannot be used to realize the target function. Thus, \(ls\) is increased to 9 and it is found that all products of the target function and its dual are covered by the products of the \(3\times3\) lattice function and its dual, respectively. Hence, the initial lower bound is determined as 9. Similarly, for our example in Fig. 6, where the dual of the target function \(f = \overline{a}b + \overline{a}c + \overline{a}bc + \overline{a}bd + b\overline{c}d\) is \(f^D = \overline{a}c + \overline{a}d + ab\overline{c} + \overline{a}bd + b\overline{c}d + bde + \overline{b}\overline{c}d\), the initial lower bound is computed as 9.

There exist three efficient methods used to find an initial upper bound. The dual production (DP) [11] method realizes a target function using an \(u\times v\) lattice, where \(v\) and \(u\) are the number of products in the target function and its dual, respectively. In the product separation (PS) method [15], the \(v\) products of a target function are placed on the columns of a lattice each separated by a column full of zeros, filling the unspecified entries of the lattice with constant 1. Thus, a solution with a \(\delta \times (2v - 1)\) lattice is found where \(\delta\) is the degree of the target function. In the dual product separation (DPS) method [19], the \(u\) products of the dual function are placed on the rows of a lattice separated by a row full of ones, filling the unspecified entries of the lattice with constant 0. Thus, a solution with a \((2u - 1) \times \gamma\) lattice is found where \(\gamma\) is the degree of the dual of target function.

For our example in Fig. 2, as shown in Fig. 7a-c, the DP, PS, and DPS methods find a solution with the \(4\times4, 3\times7\), and \(7\times3\) lattice, respectively. For our example in Fig. 6, we note that the solution of the PS, DP, and DPS methods includes the \(7\times5, 4\times9\), and \(13\times3\) lattice, respectively.

However, the PS and DPS methods can be modified to decrease the required number of switches by reducing the number of isolation columns and rows between the products, \(ie., the ones full of constant 0 and 1\), respectively. We developed the improved version of the PS method, called IPS, as follows:

1) Find the products with at least two literals, put each of them side by side by placing one literal on the \(\delta\)th row and the other on the other rows of that column, and finally, add an isolation column if there are products with more than 2 literals.
2) For each product, \(p_i\), find another product, \(p_j\), both including more than 2 literals, so that the pair function \(f_p = p_i + p_j\) can be realized using a \(\delta \times 2\) lattice, \(ie., without using an isolation column\). Such a product is found if the number of products in the dual of the pair function, \(f^D_p\), is less than or equal to \(\delta\). If such a product, \(p_j\), exists, add the realization of the pair...
function into the lattice. Otherwise, add $p_i$ into the lattice. If there exists other product(s) with more than 2 literals to consider, add an isolation column.

3) Find the products with a single literal and if there exist isolation columns, for each product, place its literal on every row of an isolation column full of constant 0. If the number of isolation columns is less than the number of such products, put each remaining product side by side by placing its literal on every row of that column.

The improved version of the DPS method, called IDPS, can be developed similarly. It consists of the second step of the IPS method, where the products including more than 1 literal are considered, and its third step.

For our example in Fig. 2, as shown in Fig. 7d and e, the IPS and IDPS methods find a solution with the $3 \times 5$ lattice and the $5 \times 3$ lattice, respectively. For our example in Fig. 6, we note that the solution of the IPS and IDPS methods includes the $4 \times 7$ and $10 \times 3$ lattice, respectively.

The run-time complexity of these methods is bounded by the complexity of finding the dual of a logic function which can be obtained using a little computational effort on functions even with a large number of products by the state-of-art logic minimization tools. For example, the dual of a logic function with 14 variables, 90 products (the largest in our experiments), and a degree value of 9, is found less than a second using espresso. However, we observed in our experiments that the solutions of these methods can be far away from the minimum on the logic functions including more than 10 products. Hence, a divide and synthesize (DS) method, which is based on our divide and conquer method described in Section 3.2, is developed. The DS method consists of three main steps described as follows:

1) Partition the products in the target function $f$ into two sub-functions $f_1$ and $f_2$ such that $f = f_1 + f_2$, where $f_1$ and $f_2$ have a number of products close to each other and a minimum number of literals.

2) Apply JANUS to these sub-functions and add its solution into a lattice using a single isolation column.

3) For each sub-function, explore alternative realizations with a small number of rows and columns.

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The partitioning of products into two sub-functions in the first step is formulated as a 0-1 ILP problem and solved using a 0-1 ILP solver. To explore alternative realizations of sub-functions in the third step, we initially compute the size and number of rows of the lattice found at the second step, denoted as the best cost $bc$ and best row $br$, respectively. Then, we apply the following procedure when $br \geq 3$.

1) For each solution of a sub-function with an $m \times n$ lattice, where $m \geq br > 3$, check if a $(br-1) \times k$ lattice, where $k > n$, can be used to synthesize this sub-function. Note that $k$ initially set to $n$ is incremented by 1 till the $bc$ value is exceeded or a solution is found.

2) For each solution of a sub-function with an $m \times n$ lattice, where $m < br - 1$, check if this sub-function can be realized using an $(br-1) \times k$ lattice, where $k < n$. Note that $k$ initially set to $n$ is decremented by 1 till there exists no solution.

3) If a solution with a size less than $bc$ is found, update the lattice and its cost.

As an illustrative example, assume that after the target function is partitioned into two sub-functions $f_1$ and $f_2$, the solutions of JANUS on these sub-functions include the $5 \times 2$ and $3 \times 4$ lattices, respectively. As shown in Fig. 8a, the lattice, that realizes the target function $f = f_1 + f_2$, is $5 \times 7$, where $bc$ and $br$ are 35 and 5, respectively. If both $f_1$ and $f_2$ are realized using the $4 \times 3$ lattice, $f$ can be realized using the $4 \times 7$ lattice as shown in Fig. 8b. Furthermore, if $f_1$ is realized using the $3 \times 4$ lattice, then $f$ can be realized using the $3 \times 9$ lattice as shown in Fig. 8c.

For our example in Fig. 2, the DS method finds a solution using the $3 \times 5$ lattice as shown in Fig. 7e. For our example in Fig. 6, we note that the DS method finds a solution using the $4 \times 5$ lattice.

In JANUS, the initial upper bound is computed as the minimum of solutions of all these methods. Thus, the upper bounds on our examples in Fig. 2 and 6 are computed as 15 and 20, respectively.

Observe that the methods used to compute the initial lower and upper bounds of the search space consider a single ISOP form of a logic function. However, a logic function may have a number of ISOP forms with different products. Thus, better initial lower and upper bounds can be found when all ISOP forms are considered, but increasing the computational effort.

### 3.1.2 Generation of Lattice Candidates

While exploring the search space of the LS problem in a binary search manner, the middle point $mp$ is computed as $[(lb + ub)/2]$ where $lb$ and $ub$ stand for the lower and upper bound of the LS problem, respectively. As done in [15], the set of lattice candidates $C$ in this case is found as follows:

$$
C = \begin{cases}
(m,n) & m \times n \leq mp \\
(m+1) \times n > mp \\
m \times (n+1) > mp \\
\forall (m',n') \notin F, m' \geq m \text{ and } n' \geq n
\end{cases}
$$

where $F$ is a failed set which includes the row and column of lattices on which the given target function cannot be realized as described in the next subsection. This is based on the fact that if it is proved that a given target function cannot be realized using an $m' \times n'$ lattice, then any $m \times n$ lattice with $1 \leq m \leq m'$ and $1 \leq n \leq n'$ cannot be used to realize the target function [15].

For our example in Fig. 2, with the initial lower and upper bounds computed as 9 and 15 in Section 3.1.1, $mp$ is determined as 12 and thus, the set $C$ includes the $1 \times 12$, $2 \times 6$, $3 \times 4$, $4 \times 3$, $6 \times 2$, $12 \times 1$, $2 \times 5$, and $5 \times 2$ lattices.
3.1.3 Finding a Solution to the LM Problem

Given the function of a lattice candidate and the target function with a minimum number of products obtained using a logic minimization tool, both in ISOP form, initially, the structural check, described in Section 3.1.1, is performed. If the structural check is not passed, the row and column of the lattice are added into the failed set. Otherwise, we check if there exists an assignment to the lattice function variables included in the lattice variable LV set from the target literal TL set, consisting of the target function literals and constants 0 and 1, such that every entry in the truth table of the target function is satisfied. The LM problem is encoded as a SAT problem in three steps as follows:

1) Generate variables of the LM problem and the necessary constraints related to these variables.
2) Generate constraints which ensure that the lattice function can be used to realize the target function.
3) Generate constraints which enable to reduce the computational effort on the SAT solver.

In the first step of the LM problem encoding, we generate the sets LV and TL and the mapping variables lv_i*tl_j, where lv_i ∈ LV, 1 ≤ i ≤ |LV|, tl_j ∈ TL, 1 ≤ j ≤ |TL|, and |A| denotes the cardinality of set A. The mapping variable lv_i*tl_j indicates that the lattice variable lv_i is assigned to an element of TL_j, when this mapping variable is set to high. As an example, consider our target function f = πc + abc + abc + bcd in Fig. 2 when the 3 × 3 lattice is used. Thus, LV = {x_1, x_2, . . . , x_9}, TL = {a, π, b, c, c, d, 0, 1}, and for example, the mapping variable x_1*tl_4 indicates that the lattice variable x_1 is assigned to tl_4, when x_1 is set to high. Then, we generate clauses, which confirm that each lattice variable is assigned to only one element in TL, as follows:

|LV| |TL| |LV| |TL-1| |TL| lv_i*tl_j + lv_i*tl_j = 1, where

where \( \prod \) and \( \sum \) denote AND and OR operators, respectively. The former clauses guarantee that for each lattice variable, at least one of the mapping variables should be high. The latter ones ensure that for each lattice variable, when one mapping variable is high, the other ones should be low. Note that \( \pi + \bar{b} \) is equal to both \( a \Rightarrow \bar{b} \) and \( b \Rightarrow \pi \), where \( \Rightarrow \) stands for the imply operator, indicating that if one of these variables is high, the other one should be low.

In the second step of the LM problem encoding, to satisfy the target function, for each truth table entry, we generate the combinational circuit corresponding to the lattice function and assign the target function value at this entry to the circuit output. The circuit inputs, i.e., the lattice function variables, are associated with the truth table entry and denoted as lv_i*tte, where 1 ≤ i ≤ |LV| and tte is the truth table entry. We obtain the POS formula of the circuit as shown in Fig. 4 and simplify it based on the logic value at the circuit output. For our example, Fig. 9 presents the circuits generated for abed = 0000 and abed = 1000, where the target function is 0 and 1, respectively. For the sake of clarity, only three products of \( f_{3x3} \) are shown in this figure.

Observe from Fig. 9a that when the target function is low for a truth table entry, the logic 0 at the OR gate output can be propagated to the outputs of AND gates and thus, the POS formula of the circuit can be reduced to the only ones that indicate the possible ways of setting each AND gate output to 0. For our example in Fig. 9a, the clause generated for the AND gate at the top is \( x_1, x_0, x_3, x_0 \), where \( x_3, x_0 \) is set to a low value in a lattice. Observe that the control inputs having a low value actually block all paths that can carry a high value from the top plate to the bottom plate.

Observe from Fig. 9b that when the target function is high for a truth table entry, the clauses, which ensure that if an input of the OR gate is high, then the OR gate output should be high, can be removed from the POS formula. Note that, for this case, there should be at least one four-connected path between the top and bottom plates, where the control inputs of associated switches are set to high. Such paths are illustrated in Fig. 11. Based on these paths, for the truth table entry where the target function is high, there are two facts described as follows: i) in each row of the switching lattice, there should be at least one switch whose control input has a high value; ii) in each two consecutive rows, there should be at least one situation that the control inputs of switches on the same column have a high value. We generate clauses for these facts to hold. These constraints add a problem-specific knowledge into the SAT problem, leading to a decrease in the run-time of the SAT solver.

To link the mapping variables to the circuit inputs, for each mapping variable, we generate clauses which ensure that when a mapping variable is set to high, the associated circuit input, i.e., a lattice variable, is set to a value determined by the truth table entry. For our example, when abed = 0000, the constraints, such as \( x_1, a \Rightarrow x_1, 0000 \) and \( x_3, b \Rightarrow x_3, 0000 \), ensure that the circuit input has the corresponding value when a lattice variable is assigned to a target literal. When a lattice variable is assigned to a constant value 0 or 1, the related circuit input is set to that value.
In the third step of the LM problem encoding, if the degree of the target function, denoted as $\delta$, is equal to that of the lattice function, for each product with $\delta$ literals in the target function, we generate clauses indicating that at least one of the products with $\delta$ variables in the lattice function should be used to realize this product. Consider the realization of $f = \overline{abcde} + abde$ on the $3 \times 3$ lattice, where $\delta$ is 5. It is obvious that the product $x_1x_4x_5x_6x_9$ or $x_3x_6x_5x_4x_7$ of $f_{3 \times 3}$ should realize $abde$. Among many possibilities, this can be achieved by setting the mapping variables $x_{1-6}, x_{8-9}, c, d, e$ to high. Moreover, it was noticed that realizing products with a large number of literals in the lattice is a hard task. Hence, if a product of a target function has more than 5 literals (determined empirically), we also generate clauses which ensure that this product is realized by at least one product with more than 5 variables in the lattice function.

Thus, a SAT problem, that formalizes the LM problem, is generated based on the target and lattice functions. We also consider the realization of the dual of target function using the dual of given lattice function and generate another SAT problem using a formulation similar to the one given above. This is due to the fact that the dual of lattice function may have a smaller number of products than that of the lattice function as shown in Table 1 and the dual of target function may have a smaller number of truth table entries where the target function is high, yielding a SAT problem with a small number of variables and clauses. After generating the alternative SAT problem, we choose the one that has the least complexity computed as the number of variables times the number of clauses and then, solve it using a SAT solver. Since it is easier for the SAT solver to find a solution if it exists than to prove that there is no solution, we set a time limit as 1200 seconds, determined empirically. Thus, if the SAT solver finds a solution in the given time limit, the assignment to the lattice variables is obtained by the mapping variables set to high. Otherwise, it is accepted that the target function cannot be realized using the given lattice. If it is proven that the given lattice cannot be used to realize the target function in the given time limit, the row and column of the lattice are added into the failed set $F$.

### 3.1.4 SAT Problem Complexity

In order to show the increase in the complexity of the SAT problem generated by JANUS as the number of literals and products in a target function and the lattice size increase, we consider the logic function of an $r$-input XOR gate, denoted as $r$-XOR. Note that $r$-XOR includes all possible $2^r$ literals and consists of $2(r-1)$ products, each having $r$ literals. Fig. 12 presents the number of variables and clauses (in the logarithmic scale) of the SAT problems generated for $r$-XOR on $m \times n$ lattices where $r$ varies in between 4 and 7 and $m$ and $n$ range in between 3 and 7.

Observe from Fig. 12 that the complexity of the SAT problem increases dramatically as the number of inputs in the XOR logic function, and consequently, the number of products, increase. For example, the SAT problem, which is generated to check if 6-XOR (7-XOR) can be realized using the $7 \times 7$ lattice, includes 1,532,826 (3,355,090) variables and 30,031,338 (65,576,998) clauses. It is important to note that the SAT problem complexity may reach to a point that is beyond the capabilities of state-of-art SAT solvers. Moreover, the SAT problem complexity increases as the lattice size increases because the number of products and degree of the lattice function increase as shown in Tables 1 and 2. For example, for 7-XOR to be realized using the $6 \times 6$ ($7 \times 7$) lattice, the SAT problem has 220,866 (844,372) variables and 3,016,945 (13,808,368) clauses. This analysis clearly indicates that the performance of JANUS depends heavily on the number of literals and products of the target function and lattice size. This also points out the importance of improving the initial upper bound because JANUS may need to solve large size SAT problems otherwise.

Although there are logic functions with a small number of products and literals that JANUS can handle easily, there are still complex instances that it may find them hard to solve as shown in Fig. 12. Hence, an algorithm, that can easily cope with such logic functions, is needed.

### 3.2 MEDEA: A Divide and Conquer Algorithm

The divide and conquer method, called MEDEA, aims to realize complex logic functions using a little computational effort. Its main steps are given as follows:

1) Recursively partition a large number of products in a single function into sub-functions with a small number of products such that they can be handled by JANUS.
2) Find the realizations of these sub-functions using JANUS and merge these lattices into a single lattice.
3) Explore alternative realizations of these sub-functions such that the final lattice requires a small number of switches.
In the first step, the logic function and also, the sub-functions to be generated are recursively partitioned into two sub-functions if the difference between the upper and lower bounds of the function, denoted as \( dulb \), is greater than or equal to 31. We note that the lower and upper bounds of a function are computed as described in Section 3.1.1, except the D5 method is not used while computing the upper bound. As an example, assume that a target function \( f \) is initially partitioned into sub-functions as \( f = f_1 + f_2 \). Then, the sub-function \( f_2 \), denoted as \( g \), which has a \( dulb \) value greater than or equal to 31, is decomposed as \( g = g_1 + g_2 \). Finally, the sub-function \( g_2 \), denoted as \( h \), which has a \( dulb \) value greater than or equal to 31, is divided into sub-functions as \( h = h_1 + h_2 \). Thus, the target function is written as \( f = f_1 + g_1 + h_1 \), where the sub-functions \( f_1, g_1, h_1, \) and \( h_2 \) have a \( dulb \) value less than 31. While determining the \( dulb \) value, we considered two main criteria. First, the sub-functions having the determined \( dulb \) value should lead to SAT problems which can be solved easily using the state-of-art SAT solvers, and thus, they can be easily handled by JANUS. Second, these sub-functions should yield a final lattice with a small size. However, these criteria conflict with each other as also shown in our experiments. It is observed that a large (small) \( dulb \) value leads to a small (large) number of sub-functions with a large (small) number of products whose realizations can be found using a great (little) computational effort and which are merged into a small (large) size single lattice. Thus, the \( dulb \) value is determined to be 31 based on experiments, meeting these two criteria adequately.

In its second step, as done in the D5 method, JANUS is used to find the realizations of these sub-functions on lattices. These lattices are added into a single lattice, separating each one of them by an isolation column and filling the unspecified entries by constant 1 as shown in Fig. 8a.

In its third step, as done in the D5 method, the possible realizations of each lattice with a small number of rows and columns are explored and the one that can reduce the final lattice size is chosen to replace the current one.

We note that the run-time limit for the SAT solver used in the second and third steps of MEDEA is set to 300 seconds to reduce the computational effort.

3.3 Realization of Multiple Functions

The proposed algorithms, which realize a single logic function using a switching lattice, can be used to realize multiple functions on a single lattice as follows:

1) Find the realization of each logic function using one of the proposed algorithms.
2) Merge these realizations into a single lattice.
3) Find alternative realizations of these functions that can reduce the final lattice size.

Based on the algorithm used to find the realization of each function on a switching lattice, i.e., JANUS or MEDEA, the developed algorithms are called as JANUS-MF and MEDEA-MF, respectively.

As an example, consider the functions of a full adder, where \( c_{out}(a, b, c_{in}) = \sum(3, 5, 6, 7) \) which can be written as \( c_{out} = ab + ac_{in} + bc_{in} \) and \( s(a, b, c_{in}) = \sum(1, 2, 4, 7) \) which can be written as \( s = \overline{a}bc_{in} + abc_{in} + abc_{in} + abc_{in} \).
the SAT problems generated for the \(3 \times 10\), \(5 \times 6\), \(6 \times 5\), and \(10 \times 3\) lattices on the mp2d_02 instance. This is mainly due to different number of products and degree of the lattice function as shown in Tables 1 and 2. Moreover, having a SAT problem with a small complexity does not always mean that it will be solved using a little computational effort, e.g., the SAT problems generated for the \(4 \times 5\) and \(7 \times 3\) lattices on the b12_06 instance. This is related to the number of products and the number of literals in products of both target and lattice functions. Furthermore, observe that the complexity of SAT problems generated for the mp2d_02 instance is larger than that of SAT problems generated for the b12_06 instance. This is mainly because the number of inputs of the mp2d_02 instance and the sizes of lattices checked for this function are larger than those in the b12_02 instance.

In order to compare the performance of algorithms, we used 48 instances presented in [20]. Table 5 shows the results of algorithms where \(lb\) stands for the lower bound found as described in Section 3.1.1, \(oub\) is the old upper bound computed based on the DP, PS, and DPS methods [19], \(nub\) is the new upper bound found considering also the solutions of the IPS, IDPS, and DS methods, and \(iubt\) denotes the time required for the computation of the initial lower and upper bounds in seconds. Finally, \(sol\) and \(CPU\) denote the solution and run-time of algorithms in seconds, respectively.

Observe from Table 5 that the use of new methods introduced for finding an upper bound improves the existing upper bound of [19] by 42.8\% on average using a little computational effort, reducing the search space of the LS problem significantly. Note that while the DP, PS, and DPS methods find a smaller upper bound on only one instance than other methods, the proposed IPS, IDPS, and DS methods lead to better upper bounds on 39 instances than other methods. Observe also that the new upper bound can be better than the solutions of existing methods proposed for the LS problem, e.g., 5xp1_3.

Observe from Table 5 that JANUS can find better solutions in terms of lattice size than the exact algorithm of [15], e.g., ex5_15, ex5_17, and ex5_24. This is simply because it explores a small search space due to the improved upper bounds and it encodes the LM problem as a SAT problem efficiently. Also, JANUS can find solutions with the same size as the exact algorithm, but using less computational effort, e.g., ex5_23, mp2d_02, and mp2d_04. Although JANUS does not consider all ISOP forms of a logic function while finding the initial lower and upper bounds of the LS problem as described in Section 3.1.1, its solutions are never worse than the exact ones. Furthermore, the solutions of JANUS are better or equal to those found by the existing algorithms, having the smallest lattice size on average. Moreover, MEDEA can find solutions using a little computational effort with respect to other algorithms except the method of [16], e.g., 5xp1_3, ex5_23, and mp2d_01, and its solutions are better than those of the existing approximate algorithms and close to those of the exact algorithm and JANUS on average. On the other hand, the strict rules on the realization of a product in the approximate method of [15] yield the worst solutions on instances ex5_15, ex5_17, and ex5_23. The solutions of the method [19] may be far away from the optimal, e.g., 5xp1_3, ex5_24, and mp2d_01, since it does not consider all possible lattice candidates. The method of [16] finds solutions using the least computational effort on average, but its solutions are worse than those of other algorithms on average.

Tables 6 and 7 respectively present the ratio of CPU times required by the methods used in JANUS and MEDEA over their total run-time given in percentage on instances in Table 5. Observe from these tables that while the run-time of JANUS is dominated by solving LM problems formulated as SAT problems, the run-time of MEDEA is dominated by finding lattice realizations using JANUS.

In order to explore the limitations of algorithms [15], [19] and JANUS, we used 12 logic functions taken from the LGS91 benchmark [32]. Table 8 presents the results of algorithms where \#in, \#pi, and \(\delta\) denote the number of inputs, prime implicants, and degree of the target functions in ISOP form, respectively. Since the methods of [15], [19] cannot find a solution on these instances in the given time limit, i.e., 6 hours, their CPU time is not listed to avoid repeated values.

We note that the initial upper bound of the LS problem for each instance given in Table 8 is found by the DS method, leading to a 73.6\% reduction on average when compared to the old upper bound computed by the DP, PS, and DPS methods. Observe that the found upper bound is better than the solutions of the algorithms [15], [16], [19] on average. However, the DS method cannot find the upper bound in the given time limit on two instances, i.e., sao2_01 and sao2_03.

Observe from Table 8 that the algorithms [15], [19] and JANUS find these instances hard to solve. While all solutions of the method [19] are equal to the initial upper bound, the methods of [15] can only improve the initial upper bound value on the inc_03 and rd53_01 instances. There is only one function, i.e., inc_03, that JANUS can find a solution in a given time limit. Observe that JANUS cannot improve the initial upper bound of any instance. However, it can find significantly better solutions than the algorithms [15], [19] which is due to the DS method used to find an initial upper bound. On the other hand, the method of [16] can find better solutions than the algorithms [15], [19], i.e., all instances except apex4_18 and sao2_01. This is because while the decomposed sub-functions can be solved by the exact method of [15], the whole functions are hard to solved by the exact method. However, the solutions of [16] are worse than those of JANUS and MEDEA on average. Moreover, the solutions of MEDEA are obtained using the least computational effort on
average and they are better than those of all algorithms on average, except those of JANUS.

Observe from Table 9 that as the \(dulb\) value, which is used while partitioning a logic function into two sub-functions, is changed from 11 to 51, in step of 10. These results are shown in Table 9 where \#sf denotes the number of generated sub-functions.

Observe from Table 9 that as the \(dulb\) value increases, the number of sub-functions is decreased, increasing the solution quality and the run-time of MEDEA. Note that while there is a 36.3% reduction in the average lattice size, there exists a 23.8% increase in the average run-time when the results obtained with the \(dulb\) value 11 and 51 are compared.

Observe from Table 8 that the solutions of MEDEA obtained for all \(dulb\) values are better than the old initial upper bounds and those of the methods [15], [16], [19] on average. In order to show the limitations of JANUS and to demonstrate the importance of MEDEA, we used 15 logic functions taken from the LGS91 benchmark [32]. Table 10 presents the details of logic functions, the initial lower bound of the search space and its upper bounds found by different methods, and the results of algorithms. Note that the lower and upper bounds were computed in less than a second. However, the algorithms of [15], [16], [19] and JANUS cannot handle these instances in the given time limit, i.e., 6 hours, and can only return a solution obtained by the techniques used to find the initial upper bounds of the LS problem. The DS method of JANUS could not find a solution on any of these instances in the given time limit. All solutions of the method [16] were found using the DP method [11] on the decomposed sub-functions since the exact algorithm of [15] could not handle these sub-functions. In this table, size stands for the number of switches in the lattice.

Observe from Table 10 that on each logic function, the proposed IPS and IDPS methods give an upper bound which is significantly better than that found by the pre-

### TABLE 5
Summary of initial lower and upper bounds and results of algorithms on moderate single functions.

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### TABLE 6
Summary of percentage of CPU times of tools in run-time of JANUS.

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<th>SAT Problem Solving glucose [29]</th>
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<td>Instance</td>
<td>Summary of percentage of CPU times of tools in run-time of JANUS.</td>
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<td>Instance</td>
<td>Summary of percentage of CPU times of tools in run-time of MEDEA.</td>
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<th>Logic Minimization espresso [26]</th>
<th>Lattice Realization JANUS</th>
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pviously proposed methods. Although the method of [16] improves the solution of the DP method [11] on the whole logic function on average by finding the realizations of the decomposed sub-functions using the DP method [11], its solutions are still worse than those of the IPS and IDPS methods. On the other hand, MEDEA finds significantly better solutions using a little computational effort than the available methods, yielding a 43.4% decrease in the lattice size on average when compared to JANUS. This experiment clearly indicates that MEDEA is crucial especially on logic functions that the existing algorithms cannot handle.

Observe from Table 10 that since the methods of [15], [16], [19] and JANUS include QBF-and SAT-based techniques to solve the LM problem, i.e., to determine if a logic function can be realized using a given switching lattice, and the LM problem is an NP-complete problem, there exist instances that these methods find hard to solve and even cannot handle. However, MEDEA can be applied to a logic function with a large number of inputs and products since it partitions this function into sub-functions with a small number of inputs and products which can be easily handled by JANUS.

Finally, Table 11 presents the results on instances including multiple functions. In this table, \#out denotes the number of outputs of given instances and the straight-forward method applies JANUS on each target function and merges its solutions into a single lattice, i.e., first two steps of the algorithm developed for the realization of multiple functions described in Section 3.3.

Observe from Table 11 that JANUS-MF outperforms the straight-forward method where the maximum gain is achieved as 32% on the bw instance. This is simply due to the impact of Step 3 of the algorithm as mentioned in Section 3.3, i.e., finding alternative realizations of logic functions. Note that JANUS finds a realization of a logic function without considering that all the realizations of logic functions that the existing algorithms cannot handle.
functions will be merged in a single lattice. However, it aims to find a small size lattice realizing a logic function. Hence, taking the complexity of these realizations into account, in the Step 3 of the algorithm, JANUS-MF explores different realizations of logic functions systematically and tries to reduce the size of the final lattice as shown in Fig. 8. We also note that MEDEA-MF finds the same results of JANUS-MF, except the square5 instance, where its solution, found in 7 seconds, includes a $3 \times 40$ lattice.

5 Conclusions and Future Work

This article addresses the problem of realizing a logic function on a switching lattice using a minimum number of four-terminal switches and introduces two algorithms called JANUS and MEDEA. While JANUS is developed for finding a solution close to the minimum, MEDEA is proposed to handle the instances, that JANUS finds them hard to solve, using a little computational effort. This article also introduces methods that can reduce the initial lower and upper bounds of search space, leading to significant reductions in run-time. Moreover, it presents an efficient SAT formulation of the problem of checking if a given target function can be realized using the given switching lattice. Furthermore, this article describes how multiple functions can be realized on a single lattice efficiently. Experimental results show that while JANUS can find significantly better solutions than existing exact and approximate algorithms, MEDEA can easily obtain solutions on relatively large size instances that JANUS and other exact and approximate algorithms cannot handle and its solutions can be better than those of the previously proposed algorithms.

In the realization of multiple functions, the lattice size can be further reduced by sharing the common products, which can be achieved using multiple lattices. As an illustrative example, consider the target functions $f$ and $g$, where $h$ denotes the function including the common products of these functions, $f_h$ and $g_h$, stand for the functions generated after the products of $h$ are extracted from $f$ and $g$, respectively such that $f = h + f_h$ and $g = h + g_h$. Fig. 14 shows the realizations of multiple functions $f$ and $g$. Rather than the common products, the common logic expressions, which can be found using a state-of-art logic synthesis tool, can also be utilized as done for the realization of a single function in [18]. However, although this technique may reduce the number of switches due to the sharing, it may increase the total area due to the connecting wires between the lattices. Hence, rather than the optimization of the number of four-terminal switches, the optimization of area of the whole design can be considered in this case.

Moreover, since there exist alternative realizations of a logic function using different switching lattices, each having a different area, delay, and power dissipation values, algorithms, that take into account the area, delay, and power dissipation of the design, can also be developed.

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References

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