İSTANBUL TECHNICAL UNIVERSITY « INSTITUTE OF SCIENCE AND TECHNOLOGY

HIGH ORDER PROGRAMMBLE LOG-DOMAIN FILTER DESIGN

M.Sc. Thesis by

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Department : **Electronics and Communication Engineering**

Program: **Electronics Engineering**

JUNE 2008

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YÜKSEK DERECEDEN PROGRAMLANABİLİR LOGARİTMİK FİLTRE TASARIMI

YÜKSEK LİSANS TEZİ

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May, 2008 **Burak Dündar**

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ÖZET

Bu çalışmada hard disk okuma kanalları için iki tane akım modlu logaritmik domende çalışan devre tasarlanmıştır. Öncelikle logaritmik domen filtreleme konsepti ile ilgili temel bilgi verilmiştir. Farklı logaritmik domen filtre tasarlama teknikleri tartışılmıştır. Sonrasında bir LC basamak türünden devreyi simule eden logaritmik domen filtre tasarımı yapılmıştır. Sözkonusu filtre için düşük distorsiyonlu bir çıkış katı önerilmiştir. Filtre THD değeri önemli ölçüde iyileştirilmiştir. Ayrıca yükseltme değerinin programlanabilir olmasına olanak veren bir kutuplama stratejisi kullanılmıştır. Sonrasında Gm-C kaskadlama metodu kullanılarak başka bir logaritmik domen filtre tasarlanmış ve mevcut tasarım ile karşılaştırılmıştır. Simülasyonlar AMS 0.35 BiCMOS prosesi kullanılarak yapılmıştır. Tasarlanan filtreler AC genlik ve fazları, lineerlik ve eleman toleranslarına duyarlılılık özellikleri bakımından karşılaştırılmıştır. Yapılan iyileştirmelerin bu spesifikasyonlar üzerindeki etkileri karakterize edilmiştir.

HIGH ORDER PROGRAMMABLE LOG-DOMAIN FILTER DESIGN

SUMMARY

In this work two different current mode log domain filters for hard disk drive applications are designed. First some theoretical background information is given about log domain filtering concept. Different log domain filter design techniques discussed. Then an LC ladder simulating log domain filter is designed. A new low distortion expanding stage is proposed. THD performance of the overall filter is improved. Also a new biasing strategy that allows boost programming is presented. After that another log domain filter is designed using Gm-C cascading method. Two different filters designed using two different methods are compared. Simulations carried out using AMS 0.35 BiCMOS process. Filters are compared for their AC magnitude and phase performances, linearity, and sensitivity to element values. The effects of the improvements made are also characterized.

1. INTRODUCTION

Log domain signal processing is a valuable method when low voltage, high dynamic range needed from the circuits. Combined with the high frequency operating capability of the current mode operation, these methods become good solutions to overcome the bottlenecks in design. Since signal processing is done in a nonlinear domain, in log domain design the general linearization techniques aren't needed. Specifications like high dynamic range, low voltage and high frequency are important for the filters used in hard disk drive read channels. So log domain filters are widely used in this type of circuits.

Several design methods have been developed for log domain filter design in literature. Kırcay and Cam (2006) gave some basic information is given on the state-space design methods for log domain filters. Perry and Roberts (1996), Psychalinos and Vlasis (2002), El-Gamal and Roberts (1997), Kontogiannopoulos and Psychalinos (2005) proposed different methods based on LC ladder simulation. El-Gamal and Roberts (2002), Rola and El-Gamal (2003) presented examples for log domain filters designed using Gm-C cascading method.

Sensitivity to element tolerances is a problem in filter design. Since some filter specifications strongly depend on the element values, if the filter sensitivity to element tolerances is high, some unpredicted results may occur. The filters designed using LC ladder simulation methods is claimed to have less sensitivity to element values. On the other hand they have a complicated design methodology compared to Gm-C cascading methods. Also in LC ladder simulating filters, the programmability of the filter specifications (cut off frequency, boost etc…) is not as flexible as in Gm-C cascaded filters. Total harmonic distortion (THD) is generally higher in LC ladder simulating filters than Gm-C cascaded filters.

The main motivation of this work is to combine benefits of log domain filtering and current mode operation with advantage of LC ladder simulation methods. While doing this, improvements for a satisfactory THD and a flexible programming method are proposed. Organization of the thesis is as follows; chapter 2 gives an idea about

log domain filtering concept and translinear principle. In chapter 3 some log domain filter design techniques found in literature are discussed and compared. Chapter 4 presents quick information about hard disk drive read channel architectures and filter specifications used in those architectures. In chapter 5 two filters are designed using two different common methods, they are compared and modified to improve some aspects of the circuits. Chapter 6 is the conclusion of the thesis.

2. LOG DOMAIN FILTERING CONCEPT

2.1 Log Domain Filtering

Log domain signal processing is done by compressing the input signal before processing, processing the compressed signal and expanding it in a similar way to preserve the linearity of the whole system. When the compression is logarithmic and decompression is exponential, the resulting filter is known as a "log-domain filter".

The main advantages of log domain filters can be summarized as;

1. High Dynamic Range.
2. Low Voltage Operation Compatibility.
3. High Frequency Operation.
4. Electronic Tuneability.

Since the log domain filters process the signal after compression, they can operate under lower supply voltage compared to conventional filters. The maximal dynamic range achievable using conventional filter implementation techniques, such as Opamp-MOSFET-C, transconductance-C, and switched-capacitor, becomes severely restricted by the supply voltage. In log domain filters however this dynamic range limitation is relaxed significantly. Also log domain filters have very high frequency capabilities because of their current mode architecture.

Unlike linear filters, in which linear circuits are implemented using nonlinear devices, log-domain techniques directly exploit the nonlinear characteristic of the transistors to linearize the whole filter. So linearization techniques that make the linear filter design process challenging won't be needed for log domain filters. Without the need for conventional circuit linearization techniques, log-domain filter circuits have a simple and elegant structure, and have the potential to run at high frequencies and operate with low power supplies.

The log domain filtering uses exponential I-V relations of the bipolar junction transistors or the MOSFETs operating in subtreshold region. The input signal, in voltage format, is first converted to a current signal by a voltage-to-current converter.

This current signal is then logarithmically compressed using a LOG block. This can be practically achieved by pushing the current into the collector of a bipolar transistor with a grounded emitter terminal. After compression the signal is filtered with proper circuit blocks implemented using translinear principle. The decompression of the signal is performed by an EXP (or ANTILOG) circuit block. Practically, it can be achieved by applying to the base of a bipolar transistor with a grounded emitter terminal. The whole concept is illustrated in Figure 2.1.

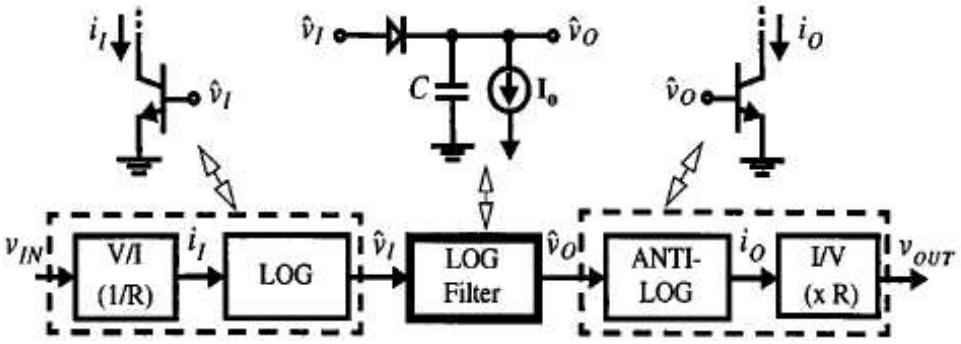


Figure 2.1 : Log Domain Filtering Concept

Sometimes it will be necessary to convert the output current to a voltage signal, for example for measurement purposes, using a current-to-voltage converter. [1]

2.2 Translinear Principle and Translinear Circuits

The first idea of "translinear" was suggested by Gilbert in 1975. The word translinear consists of first parts of the words transconductance and linear meaning transconductance linear with current [2]. Bipolar transistor is the main electronic device possessing the translinear principle. It has an exponential relation of current to voltage. The circuit based on the translinear principle is called a translinear circuit. When translinear elements connected together, clockwise or counterclockwise, form a loop that structure is called a translinear loop. A translinear loop concept is shown in Figure 2.2.

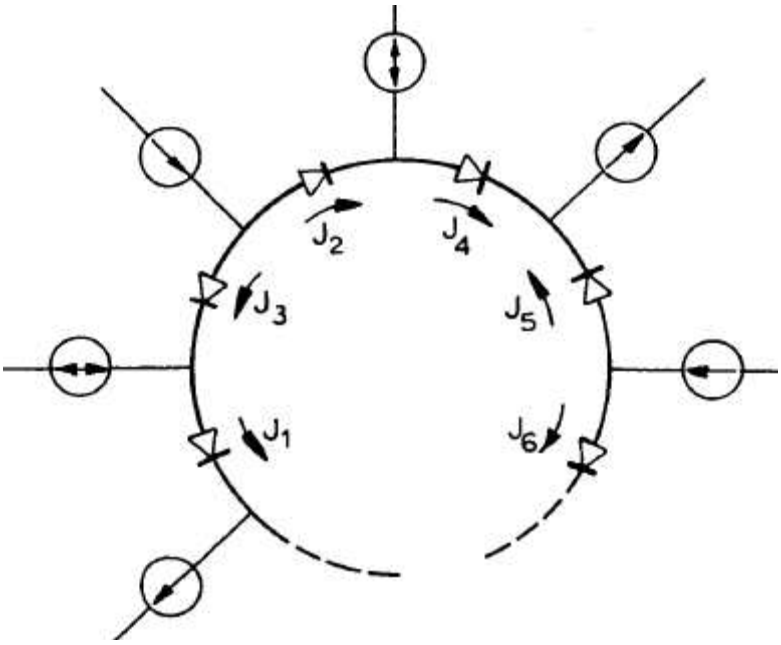


Figure 2.2 : Conceptual Translinear Loop

The translinear loop elements are bipolar transistors, MOS transistors operating in subtreshold and junction diodes. These elements can be represented by the graphical representations in the figures 2.3, 2.4 and 2.5.

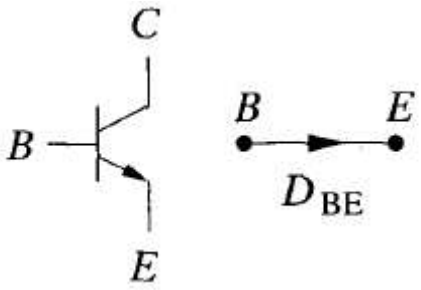


Figure 2.3 : BJT as Translinear Element

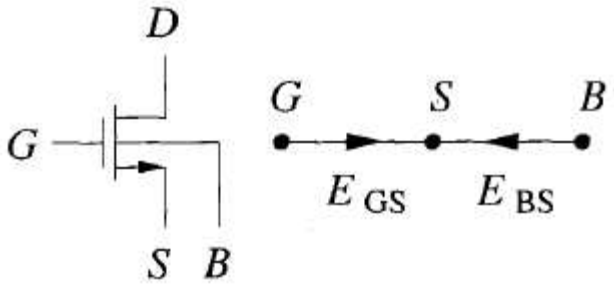


Figure 2.4 : MOS in Subtreshold as Translinear Element

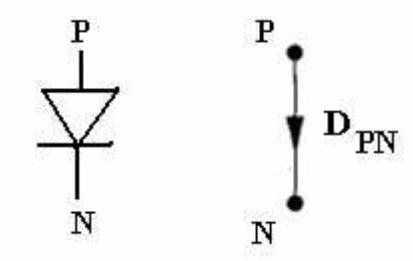


Figure 2.5 : Diode as Translinear Element

A translinear loop can be represented by a translinear circle. A translinear circle is a connected diagram with finite alternating sequence of vertices and directed edges. Each directed edge represents a translinear element. A translinear circle has an equal number of edges in the clockwise (CW) direction and edges in the counterclockwise (CCW) direction.

Tranlinear Principle is expressed as the following: The product of currents directed in clockwise (CW) direction is equal to the products of currents directed in opposite direction(CCW).

In a translinear loop sum of voltage drops on the translinear elements is zero.

$$\sum_{n \in \mathrm{CCW}} V_n = \sum_{n \in \mathrm{CW}} V_n \tag{2.1}$$

After a set of analytical manipulations equation leads to

$$\prod_{n \in \mathrm{CCW}} I_n = \prod_{n \in \mathrm{CW}} I_n \tag{2.2}$$

where I_n is the current flowing through a translinear element.

Translinear loops can be identified in circuits using a systematic way proposed in [3]. In a circuit containing translinear elements, to identify the translinear loop a dead graph of the circuit is obtained. To obtain a dead graph from the circuit;

1. Independent voltage sources are replaced by short circuits.
2. Independent current sources are replaced by open circuits.
3. All translinear elements are represented by the drawings mentioned before.

In the dead graph any circle (closed loop) identifies a translinear loop. And for every translinear loop the equation above holds. For example the circuit in Figure 2.6 contains bipolar transistors which can be considered as a translinear element. From the dead graph given in Figure 2.7, translinear loops are easily identified.

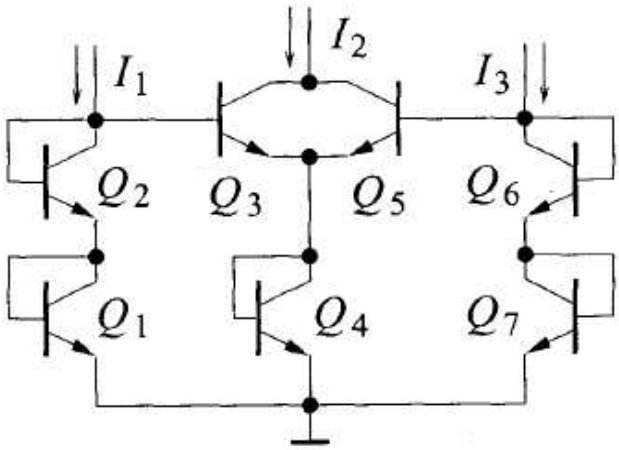


Figure 2.6 : Example of a Translinear Circuit

For this example the transistors Q1-Q2-Q3-Q4 and transistors Q4-Q5-Q6-Q7 form translinear loops.

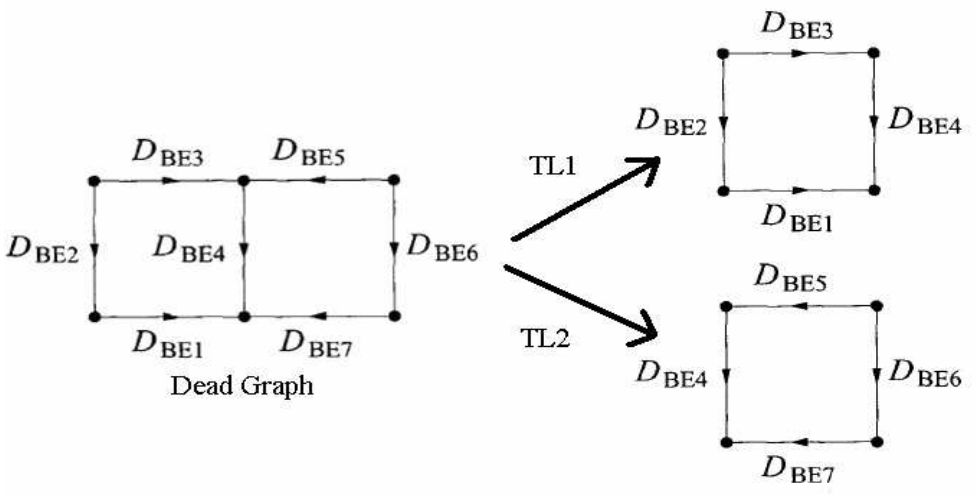


Figure 2.7 : Identified Translinear Loops

2.3 Synthesis of Translinear Loop Circuits

Synthesis of translinear circuits is a straightforward procedure. Translinear-loop circuits can be synthesized as follows.

1. Obtain the translinear loop equations. These can be the functions to implement.
2. Build a translinear loop for each of the equations.
3. Bias the translinear loops.
4. If possible simplify the overall circuit buy merging loops.

The class of translinear circuits is capable of realizing a wide range of linear and nonlinear relationships. However, not all functions are directly implementable by translinear circuits; we can directly realize products, quotients, power-law relationships, polynomials, rational functions, and various combinations of such relationships.

Once a set of translinear-loop equations is obtained, designer must construct a closed loop of translinear elements for each one. In general, there will be more than one translinear loop that implements any given translinear-loop equation. The choices of loop topology and current ordering must be guided by experience and other system-level design considerations. When synthesizing translinear circuits, stacked or alternating loop topologies can be used [4]. The main properties of these topologies are summarized in the Table 2.1.

Table 2.1 : Comparison of Translinear Loop Types

	Alternating Loop Topology	Stacked Loop Topology
Power Supply Requirement	Low	High
Biasing	Multiple matched bias sources are required	Same bias current can be used through multiple translinear elements
Input Current	Multiple copies may be needed.	Single copy of input current is enough

2.4 Biasing Of Translinear Circuits

Biasing of a translinear loop is important to maintain the operation of a translinear circuit. Generally translinear loops are biased by forcing a current into the emitter or collector of each input translinear element in the loop and arranging some type of

local negative feedback around it. This feedback adjusts translinear element's gate-emitter voltage.

There are three main biasing schemes for translinear elements. These are;

1. Diode Connection Biasing.
2. Emitter Follower Connection Biasing.
3. Enz-Punzenberger Biasing.

Figure 2.8 below shows the common diode connection biasing. A current is forced into the collector of the translinear element. This increases its collector voltage. This increased voltage is fed back to the base of the translinear element by diode connection. If any mismatch occurs between the collector current and the input gate voltage of the translinear element adjusted in order to reduce the mismatch. If the collector current is bigger than the input current, the gate will discharge, reducing the gate-to-emitter voltage.

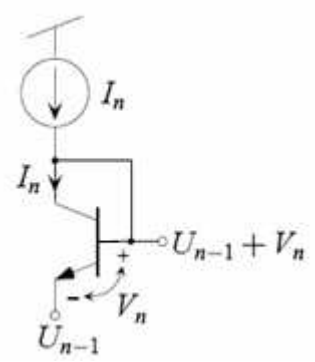


Figure 2.8 : Diode Connection Biasing

Figure 2.9 shows an emitter-follower connection. In this type of biasing a current is sinked from the emitter of the translinear element. In this configuration the emitter voltage will adjust itself up or down so that the emitter current balances the input current. If the emitter current is larger than the input current, the emitter voltage will charge up, reducing the gate-to-emitter voltage. This will reduce the emitter current of the translinear element, this will continue until the currents are matched. If the input current is larger than the emitter current, the emitter will be discharged, increasing the gate-to-emitter voltage, thereby increasing the emitter current until the currents balance.

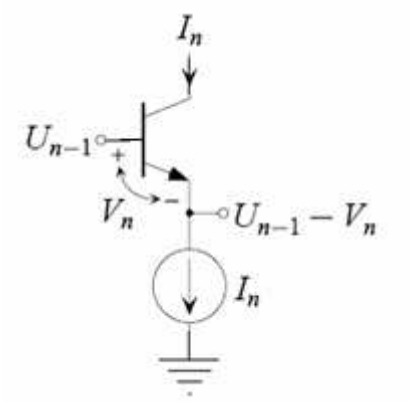


Figure 2.9 : Emitter Follower Connection Biasing

Figure 2.10 shows a simple alternative to the emitter-follower connection for biasing clockwise translinear elements. This biasing scheme is also called Enz-Punzenberger since it's first proposed by Enz and Punzenberger. Again here a current is forced into the collector of the translinear element. The collector voltage is sensed by another transistor to adjust the emitter current of the translinear element. This feedback element could be a MOS or bipolar transistor. When a large input current is inserted the collector voltage of the translinear element will increase. Since the collector voltage is tied to the gate (or base) of the feedback transistor, its current will also increase. Pulling more current from the translinear element will increase the emitter current of it. So the currents will tend to equalize. A similar mechanism occurs for small input currents.

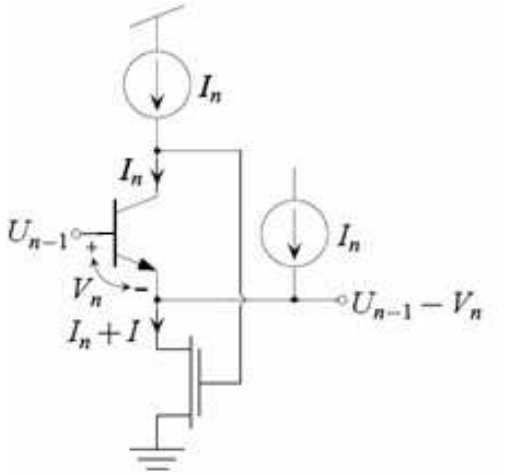


Figure 2.10 : Enz-Punzenberger Biasing

Table 2.2 is comparing the important properties of biasing schemes discussed above.

Table 2.2 : A Comparison of Translinear Element Biasing Schemes

Property	Diode Connection Biasing	Emitter Follower Connection Biasing	Enz-Punzenberger Biasing
Bias Current Requirement	Sourcing	Sinking	Sourcing
Direction of Translinear Element	Counterclockwise TE	Clockwise TE	Clockwise TE
Lateral Bipolar Compatibility	Yes	No	Yes
Number of Nodes (Complexity)	1	1	2

3. LOG DOMAIN FILTER DESIGN TECHNIQUES

In literature there are 3 main design methods for log domain filter design. All other methods consist of improvements and additions to these methods. These two main methods are;

1. State-Space (SS) Design methods
2. Gm-C Cascading Design Methods
3. LC Ladder Simulation Design Methods

These three methods have advantages or disadvantages over each other. Now these three techniques will be discussed briefly.

3.1 State-Space Design Methods

There is a set of first-order differential equations in a state-space formulation. The state variables are equal to simple functions of exponentials of node voltages. There is a one-to-one correspondence between the mathematical formulation and the circuit realization. So a systematic circuit implementation can be developed.

The state space synthesis method for log domain filters can be summarized as follows;

1. Find a suitable state-space description for the filter.
2. Write an exponential mapping function to the input and state variables.
3. Manipulate the equations to obtain a set of nodal equations.
4. Design the circuit elements like transistors, grounded capacitors, and current sources.

The first step used to synthesize a mapped state-space filter is to obtain appropriate system equations [5].

$$\frac{\partial}{\partial t}\overline{x} = A\overline{x} + \overline{b}u \tag{3.1}$$

$$y = \overline{p}^T \overline{x} + du \tag{3.2}$$

Here u, y and x denote global input, output, and state vector respectively.

The second step is the mapping. A mapping must be applied to the input and each state,

$$u = f(v_o) \tag{3.3}$$

$$x_i = f(v_i) \tag{3.4}$$

where i= 1,2,…,N.

Substitute these functions into of Eq. 3.1 and Eq. 3.2, and divide scale each line with

$$\frac{c_i}{\frac{\partial}{\partial v_i} f(v_i)} \tag{3.5}$$

where the C_i 's are arbitrary constants. We obtain the following equation 3.6:

$$C_i \dot{v}_i = [\sum_{j=1}^{N} \frac{C_i A_{ij}}{\frac{d}{dv_i} f(v_i)} f(v_i)] + \frac{C_i b_i}{\frac{d}{dv_i} f(v_i)} f(v_0) \tag{3.6}$$

These equations are a set of nodal equations. In fact, if we let v_i symbolize the I-th node voltage in a circuit, then the left-hand side of Eq. 3.6 represents the current flowing into a grounded capacitor. In the same manner, the right-hand side of Eq. 3.6 is the sum of some currents flowing into this capacitor. These currents are a form of voltage-controlled current sources, or transconductance. [5]

3.2 Gm-C Cascading Design Methods

In Gm-C continuous time filters, the transconductor often has to be linearized in order to achieve the desired dynamic range. Log-domain circuits exploit the exponential characteristic of a single device, they do not require any linearization and hence preserve the maximum gm/I ratio even for large signal operation.

The log domain integrators are the basic building blocks for Gm-C cascaded log domain filters.

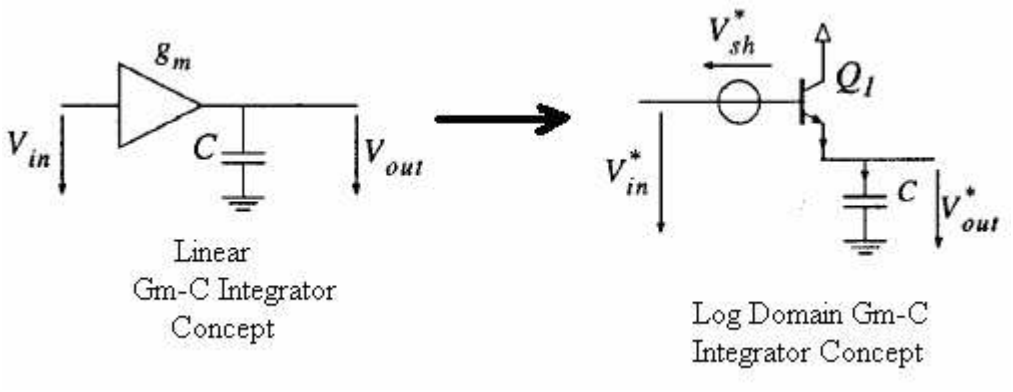


Figure 3.1 : Linear Gm-C and Log Domain Gm-C Integrator Concepts

The linear Gm-C integrator shown in the Figure 3.1 realizes the following equation;

$$g_m \cdot V_{in} = c \cdot \frac{\partial V_{out}}{\partial t} \tag{3.7}$$

The log domain Gm-C integrator realizes;

$$g_m \cdot U_T \cdot e^{V^*_{in}/U_T} = c \frac{\partial (U_T \cdot e^{V^*_{out}/U_T})}{\partial t} \tag{3.8}$$

Rearranging the equation

$$I_S \cdot e^{(V^*_{in} + V_{sh}{}^* - V^*_{out})/U_T} = c \cdot \frac{\partial V^*_{out}}{\partial t} \tag{3.9}$$

The log domain Gm-C integrator facilitates the same integration function. But instead of realizing this function with actual signals, it processes the compressed voltage signals.

In order to map a linear domain integrator to a log domain integrator the following transformation equations;

$$V^* = U_T \cdot \ln(V / U_T) \tag{3.10}$$

or

$$V = U_T \cdot e^{V^*/U_T} \tag{3.11}$$

can be used. Here $U_T = kT/q$ is the thermal voltage.

As it can be realized from the equations 3.10 and 3.11, the voltages within the log-filter are in the log-domain, while the currents are still in the linear domain.

The integration time constant of the log domain integrator can be derived [6]

$$\tau = (U_T / I_S) \cdot e^{-V_{sh}^*/U_T} \cdot c = (U_T / I_f) \cdot c = \frac{c}{g_m} \tag{3.12}$$

where

$$I_f = I_S \cdot e^{(V_{sh}^*/U_T)} \tag{3.13}$$

The time constant is determined by *C* and $g_m = I_f / U_T$ corresponding to a small-signal transconductance. Log-domain filters therefore use the maximum g_m/I while having a dynamic range much larger than the corresponding small signal circuit. In addition, a large g_m tuning range is obtained thanks to the validity of the exponential characteristic of bipolar transistors over several decades.

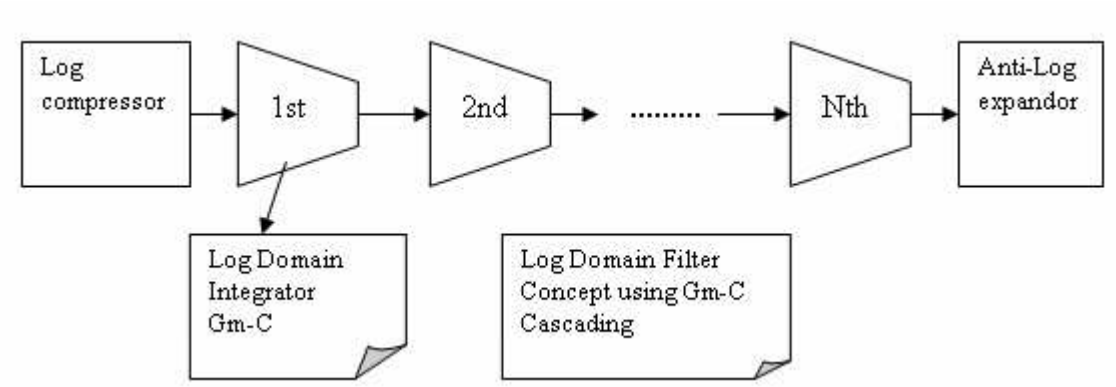


Figure 3.2 : Conceptual High Order Log Domain Gm-C Filter

As in linear domain synthesis of the Gm-C filters can be done by cascading integrators properly. Figure 3.2 shows the conceptual filter obtained by Gm-C cascading. Blocks for Log and Anti-Log conversion must be placed at the input and output of the filter.

3.3 LC Ladder Simulation Design Methods

Log domain filter design based on LC ladders is preferred for its tolerances on component drifts and parasitic effects. The filters designed with LC ladder simulation methods carry the characteristics advantages of LC ladders, they simulate. In addition to that advantages of log domain operation is also preserved.

In literature there are many works done on LC Ladders simulating filters and their design methodologies. For example in the case of elliptic filters. Some improvement techniques have been discussed literature. In [6] elliptic low pass filter was realized using a floating capacitor to approximately perform the required differentiations. In [7] an alternative SFG representation of elliptic LOG-domain filters is introduced. In this method the SFG of the LC ladder prototype is modified in such a way, that differentiation operation is not required. This is achieved through a manipulation of the voltage/current equations of the LC ladder, so that only lossless integrators and amplifiers are needed. Also improvements on LC simulation method have been reported for band pass filters. [8]

The main and generic procedure in design of a Log Domain filter based on LC ladders can be summarized as the following;

1. Choose an approximation method for the filter
2. Design the LC ladder prototype realizing the chosen approximation method and required specifications.
3. Optionally a Signal Flow Graph (SFG) of the prototype circuit can be extracted. (In some design methodologies this step could be unnecessary)
4. Obtain the log domain equivalents of the necessary elements such as inductor or capacitor and their different combinations.
5. Replace the LC ladder prototype elements with the obtained log domain equivalents.

The procedure above is a generic design process. So the methodologies developed in literature mainly follow the same procedure. They have slight differences at obtaining the log domain equivalents. Some of them use exponential transconductor cells [9], some of them use Bernoulli cells [10]. But all of these basic cells are designed using translinear principle. According method proposed in [9], the elements of the passive prototype filter is replaced its log domain equivalent in log

domain. The current that flows through the terminals of the passive element in the linear domain is the same with that flows through the terminals of the corresponding active block in the log domain. In this way, the linear operation of the whole filter is preserved. The voltages of the log domain filter are compressed to provide log domain filtering advantages.

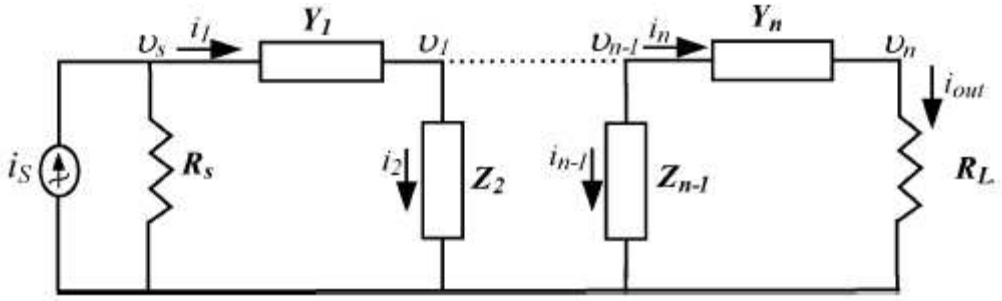


Figure 3.3 : Passive Filter in Ladder structure

Consider the current-mode LC ladder filter shown in Figure 3.3. When the passive elements in prototype are replaced by an appropriate active block, the current-voltage relationship of the passive element is implemented. But this replacement procedure should provide the following conditions;

1. The current that flows into the terminals of passive element would be equal to that flows into the corresponding terminals of its active equivalent,
2. The voltage at each terminal of passive element would be equal to the voltage at the corresponding terminal of its equivalent.

If log domain filtering is to be applied, the active blocks will be nonlinear and, thus, the above conditions must be changed as:

1. The current that flows into the terminals of passive element in the linear domain would be equal to that flows into the corresponding terminals of its active equivalent in the log domain,
2. The voltage at each terminal of passive element in the linear domain would be equal to the expanded voltage at the corresponding terminal of its equivalent in the log domain.

The details of the design method mentioned above [9] will be discussed in detail later.

3.4 Comparison of Gm-C and LC Ladder Filters

In this section a comparison of Gm-C cascaded and LC ladder simulating filters will be given based on [11].

The state space design method is a straight forward and mathematical method for designing log domain filters. But when the order of the filter is increased, the equations could become too complex to manipulate and solve. As a result for high order filter designs state space method is not preferable.

The Gm-C cascading method is an easy and quick way to design log domain filters. The high order filters can be designed by simply cascading the integrators. Also the tuning can be done easily. Different parameters such as gain, cutoff frequency or boost can be tuned independently. But the problem with Gm-C cascading design methods is the sensitivity of the circuit parameters to the element tolerances. So the circuit parameter drift due to the element tolerances can be a problem. The same problem exists not only in log domain but also in linear domain filters. By making the key aspects of the filters tunable these problems can be relaxed.

The LC ladder simulation design methods carry an important advantage arising from the LC ladder prototypes. LC ladder prototypes have very low sensitivities to element tolerances. So the active log domain filters simulating these LC ladder prototypes carry the same advantageous properties. This fact is illustrated in Figure 3.4 and Figure 3.5. LC ladder structures demonstrate a better sensitivity to transistor area mismatches than the cascade structures. This fact has been remarked in [11].

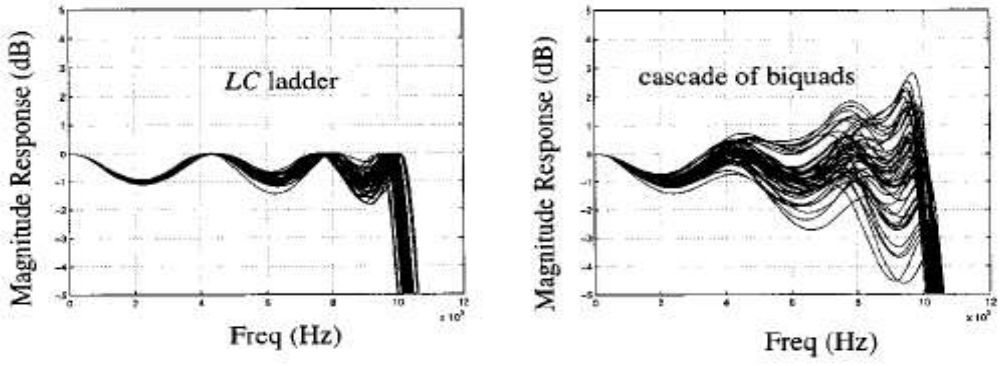


Figure 3.4 : LC Ladder simulation method Vs Gm-C Cascading (capacitor variations)

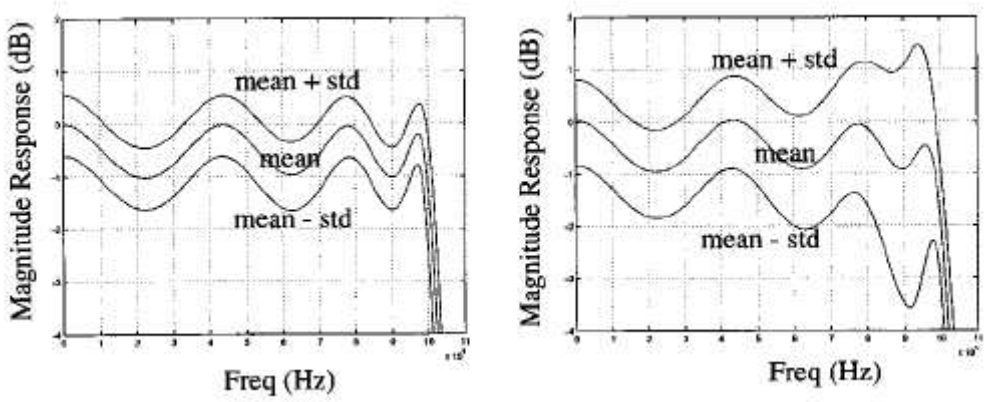


Figure 3.5 : LC Ladder simulation method Vs Gm-C Cascading (transistor mismatch)

The difficulty in design process varies for different methods. Some of them use quick and easy procedures for simulating LC ladders.

Table 3.1 compares some of the critical properties of design methods;

Table 3.1 : A comparison of Log Domain Filter Design Methods

Design Method	Design Complexity	Element Value Sensitivity	Tuning	SFG Construction
State Space Design Methods	High	Variable	Low	Needed
Gm-C Cascading Design Methods	Low	High	High	Not Needed
LC Ladder Simulation Design Methods	Variable	Low	Medium	Sometimes

4. HARD DISK DRIVE READ CHANNELS

The recording density of the hard disk drive (HDD) systems is increasing rapidly. But the sizes of the bit cells are becoming smaller and smaller. That fact results in hard constraints on the magnetic head: the size, positioning, and sensing of the head media require tighter control on precision and on tolerance. Noise and distortion also corrupt the analog signal obtained from the magnetic head. ISI (inter symbol interference) is the main source of distortion in HDD systems. Also some contribution is introduced from the electronics and the head media. The amplitude of the signal at the output of the head is typically in the microvolt range. So it needs preamplifying circuits to properly recover and use the detected signal. This task is performed by a low-noise amplifier followed by a variable gain amplifier (VGA). To avoid adding distortion to the phase response of the read signal from the amplifying circuits, the cutoff frequencies of the preamplifier and of the VGA are typically a factor of two higher than that of the following low-pass filter (LPF). [12]

In a HDD read channel AFE (Analog Front End), the LPF serves three main functions [13];

1. LPF limits the noise band on the read channel.
2. LPF helps equalize the signal delay within desired targets.
3. LPF enhances the pulses coming on the read channel (by pulse-slimming) and reduces the overlap of the pulses known as Inter-Symbol Interference (ISI).

In order to maintain these functions, LPFs, employed in the AFE of a HDD read channel, are generally high order Bessel or 0.05° phase equiripple type filters. These filters are also equipped with a programmable gain boost around cutoff frequency, and possibly a varying cutoff frequency to enable processing of different signals apart from the read channel signal.

The signal from the read head of the HDD comes with a distorted group delay. So it has to be equalized without losing any information from the content. For this reason Bessel and 0.05° phase equiripple type filters are prime implementations of the LPF

due to their excellent group delay characteristics. And also some signal conditioning and pulse shaping may be required to avoid overlap. For this reason LPF must be with the programmable boost feature around cutoff frequency. Since the spectral content of sharp pulses is mainly composed of high frequency components, a gain close to the filter cutoff would boost such components and suppress lower frequency components. The result is a slimmer pulse and a lesser likelihood of ISI. On the other hand this specifications and functions can change based on the chosen read channel architecture. Figure below shows the read channel architectures used in HDD applications. Specification and design complexity of LPF is relaxed or hardened according to HDD read channel architecture.

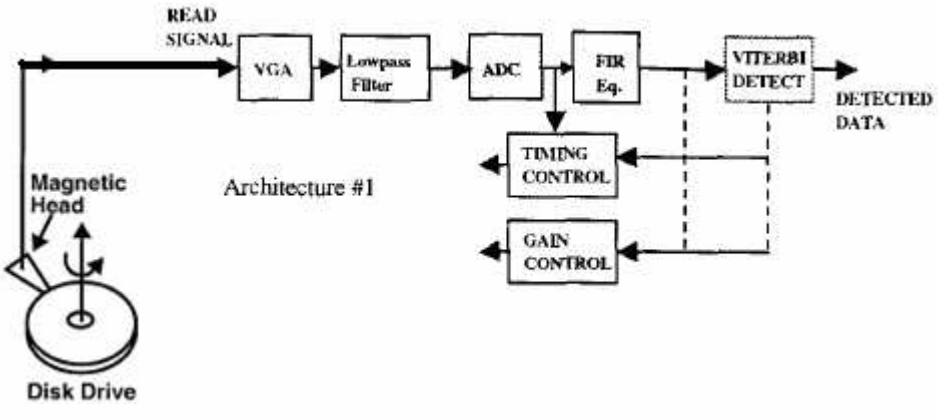


Figure 4.1 : Read Channel Architecture #1

Architecture #1 in Figure 4.1 was firstly developed by IBM. CMOS and BiCMOS implementations of this architecture can be found in literature. This architecture requires a full 6bit ADC and a digital FIR equalizer.

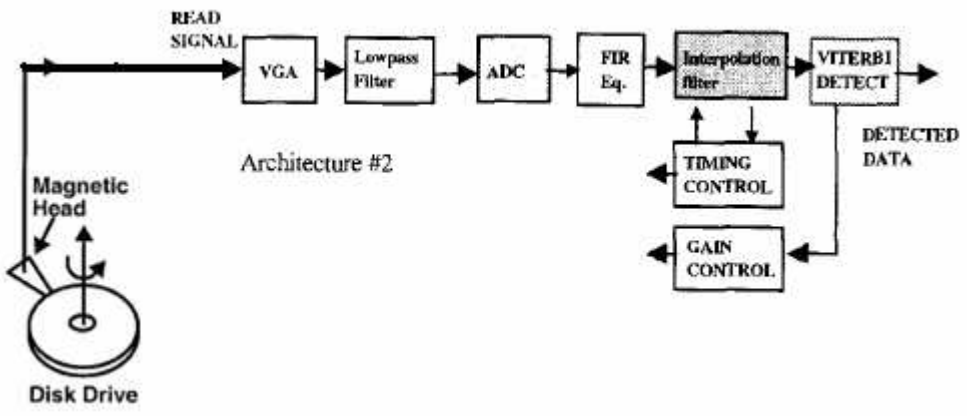


Figure 4.2 : Read Channel Architecture #2

Architecture #2 in Figure 4.2 is an extension of #1. Only difference is in #2 timing recovery is performed in digital domain. Of course this can relax the specifications on LPF.

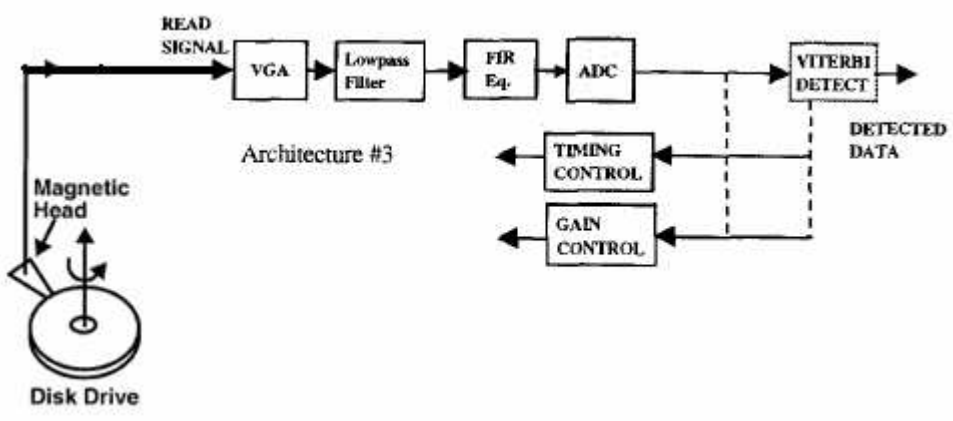


Figure 4.3 : Read Channel Architecture #3

Architecture #3 in Figure 4.3 trades the complexity of a continuous time filter to a simpler LPF and a FIR equalizer. The specifications on the filter are further relaxed.

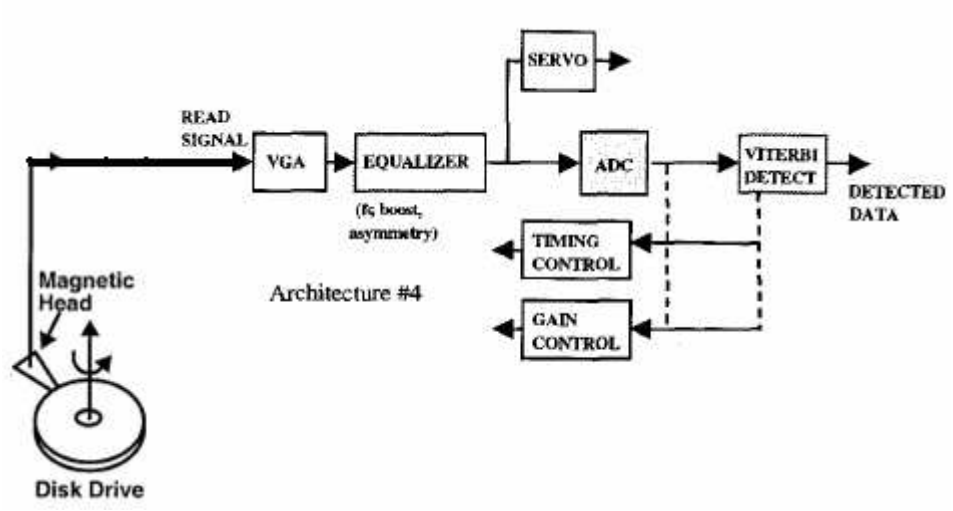


Figure 4.4 : Read Channel Architecture #4

Both architecture #3 and #4 (Figure 4.4) places equalization before ADC so that quantization noise enhancement is eliminated and less number of levels in quantizer is needed. [14]

5. DESIGN OF SEVENTH ORDER LOG-DOMAIN FILTERS

5.1 Filter Approximations

Gain and phase characteristic of a filter can be realized by using more than one transfer function. Time domain, frequency domain responses and the application determines the transfer function to be used. Sometimes there might be trade offs for performance against design complexity. Some important approximation methods for filter design are; Butterworth Filter, Butterworth Filter , Bessel Filter, Linear Phase Filter with Equiripple Phase Error.

The Butterworth filter gives a good attenuation and a good phase. There is no ripple in the pass band or the stop band; because of this, it is sometimes called a maximally flat filter. But the transition from stop band to passband is not very steep. It has average transient characteristics in the passband. Figure 5.1 shows the gain and group delay plots for Butterworth type filters.

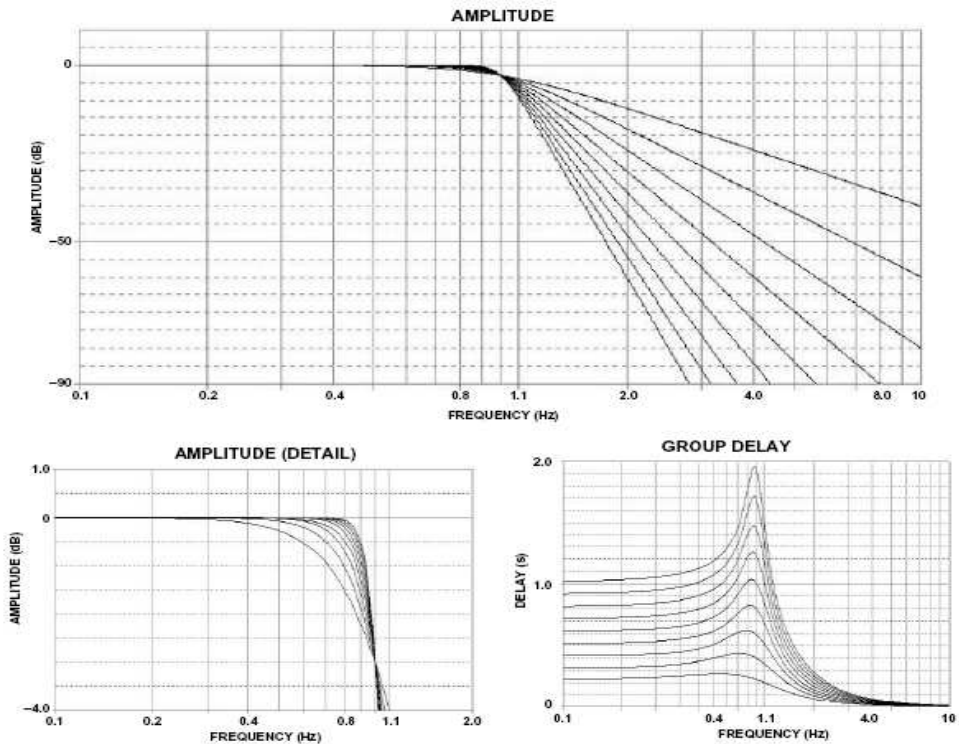


Figure 5.1 : Butterworth Type Filter Gain and Group Delay Plots

The Chebyshev filter's transition region is steeper than the same-order Butterworth filter, at the expense of ripples in its pass band. Chebyshev filter minimizes the height of the maximum ripple. The order of the filter also determines the characteristic in passband. For odd order Chebyshev filters begin with 0dB gain and go to ripple value. Even order filters begin from passband ripple value. The number of cycles of ripple in the passband is equal to the order of the filter. Figure 5.2 shows the gain and group delay plots for Chebyshev type filters.

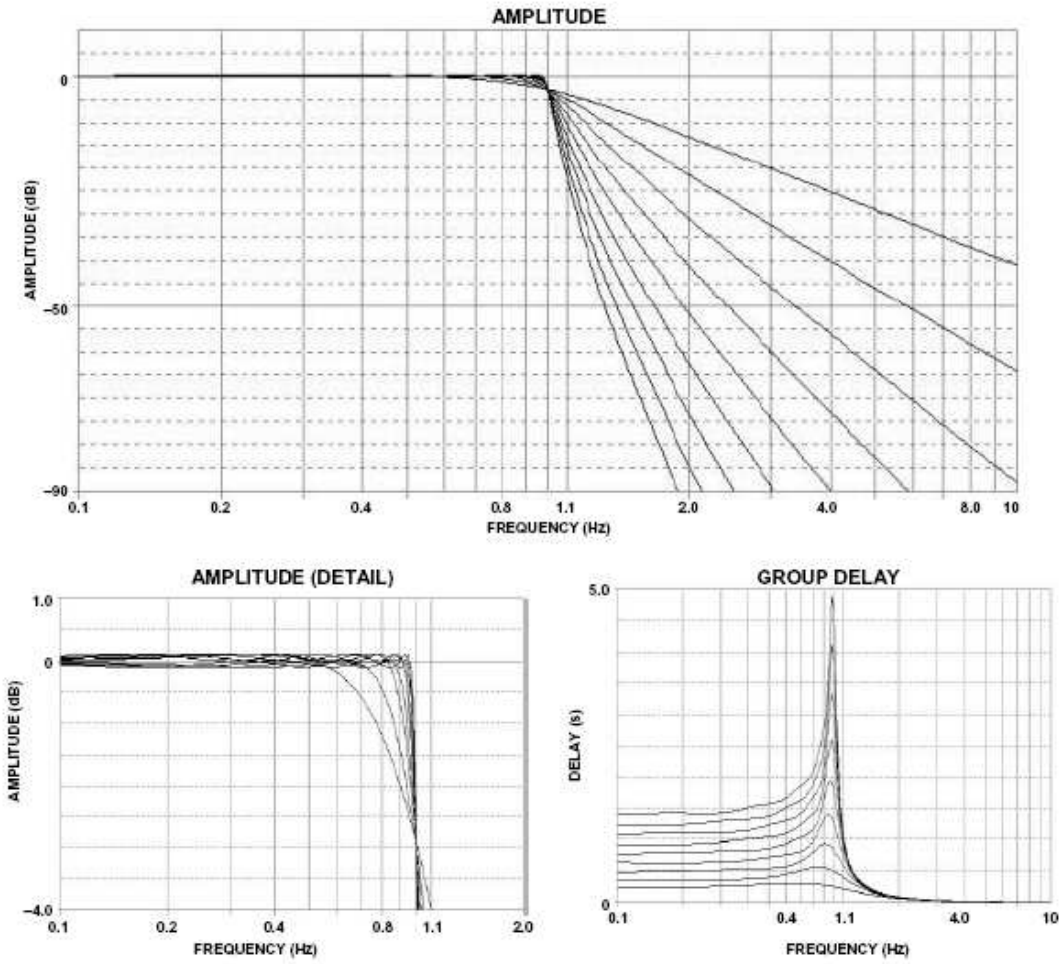


Figure 5.2 : Chebyshev Type Filter Gain and Group Delay Plots

The Bessel filter is optimized to obtain better transient response due to a linear phase in the pass band. This means that there will be relatively poor frequency response. Figure 5.3 shows the gain and group delay plots for Bessel type filters.

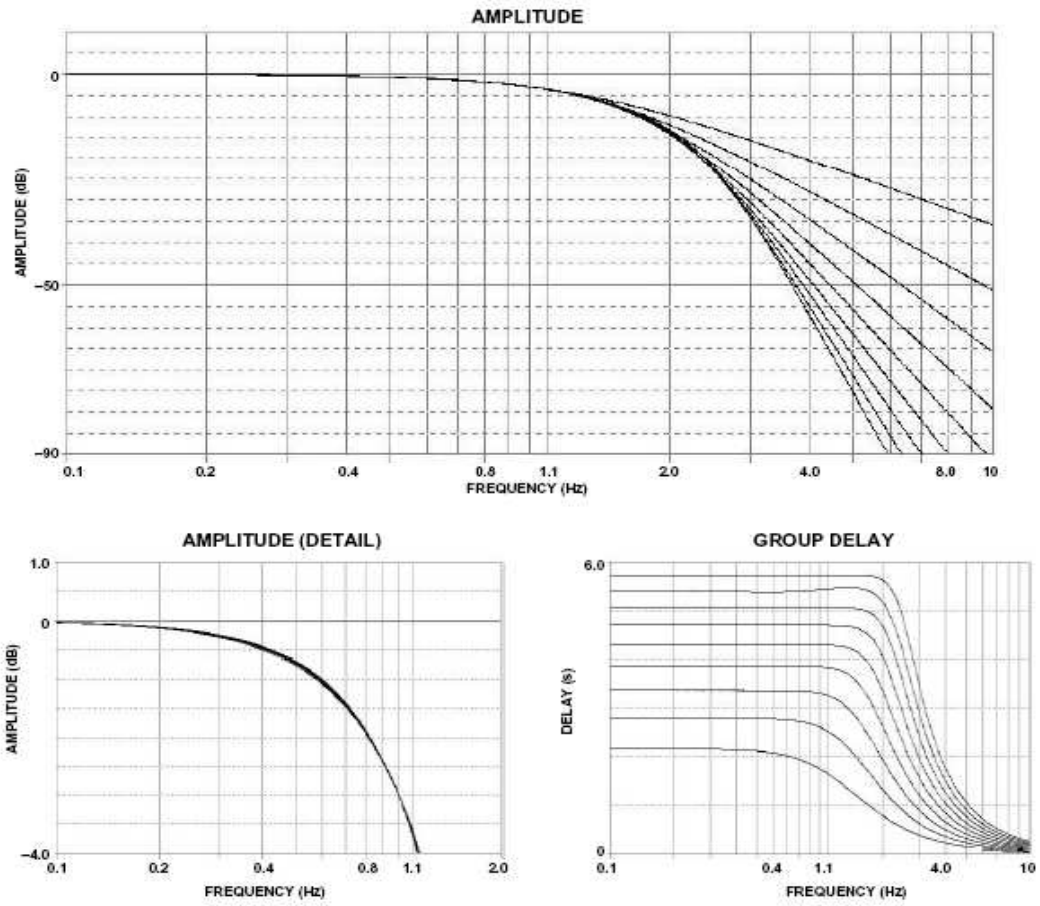


Figure 5.3 : Bessel Type Filter Gain and Group Delay Plots

The linear phase filter has a linear group delay characteristic in the passband. Compared with Bessel filter this linearity could extend far beyond the cutoff frequency of the filter. But this linearity is obtained by letting the phase response have ripples, similar to the amplitude ripples of the Chebyshev. The more ripple, the group delay of the filter has, the more linearity extends. The step response will show slightly more overshoot than the Bessel and the impulse response will show a bit more ringing. These filters are also called equiripple phase filters. Figure 5.4 shows the gain and group delay plots for linear phase type filters.

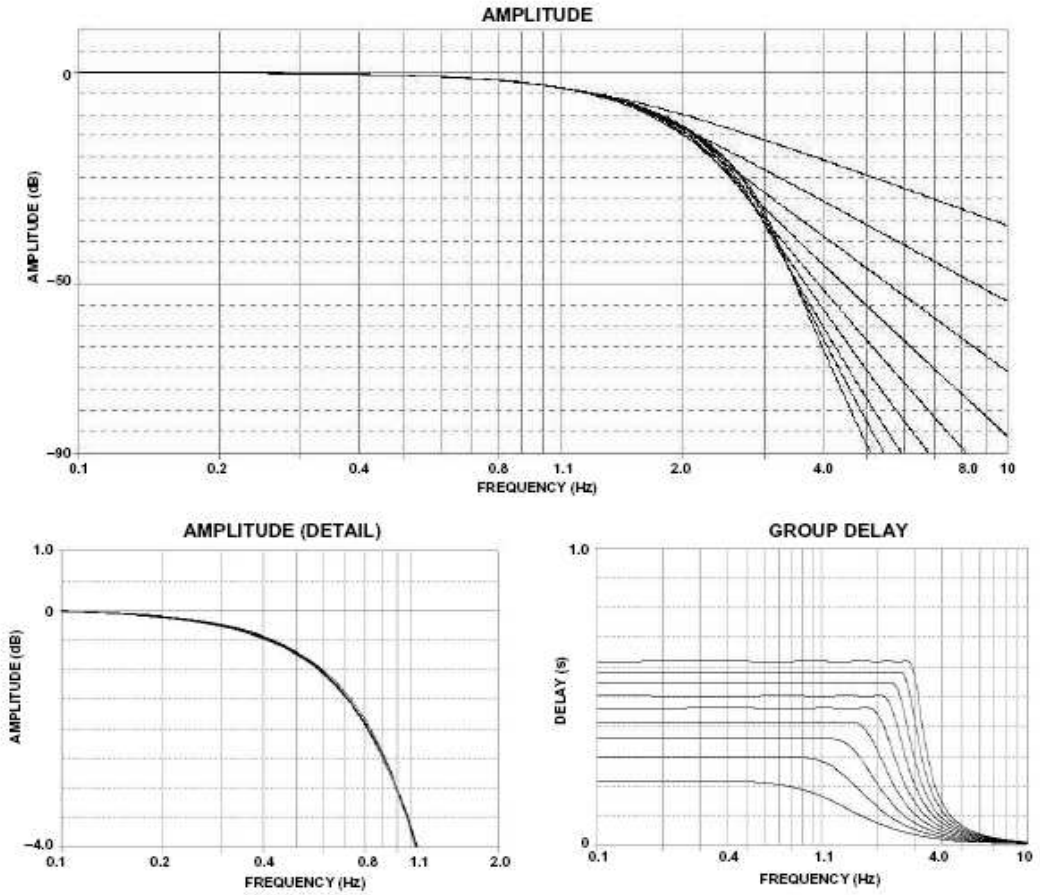


Figure 5.4 : Equiripple Type Filter Gain and Group Delay Plots

5.2 A Comparison of LC Ladder Prototypes

In section 5.1 some properties of filter approximations are given. For hard disk drive read channel filter two candidates exist; Bessel filter and 0.05 Equiripple type. Using Cadence Spectre simulator examples of these two filter prototypes have been designed. And properties of the filters are observed and verified.

Both filter prototypes are designed with the following common properties (Table 5.1):

Table 5.1 : Common Properties of Designed LC Ladder Prototypes

3dB Cut Off Frequency	100MHz
Order of the filter	7th
Input Impedance (Zin)	1 ohm
Output Impedance (Zout)	1 ohm

The calculated ideal element values for the LC ladder prototypes are shown in Table 5.2.

Table 5.2 : Calculated Element Values for LC Ladder Prototypes

Element Name	Bessel Type LC Prototype Element Values	0.05 Equiripple LC Prototype Element Values
C1	176.02537 pF	331.838 pF
L2	518.6859 pH	795.155 pH
C3	835.4 pF	1.059 nF
L4	1.117 nH	1.197 nH
C5	1.383 nF	1.392 nF
L6	1.1759 nH	1.696 nH
C7	3.606nF	3.636 nF

Using these element values the schematics of the prototypes (Figure 5.5) are formed and they are simulated using Cadence Analog Design Environment.

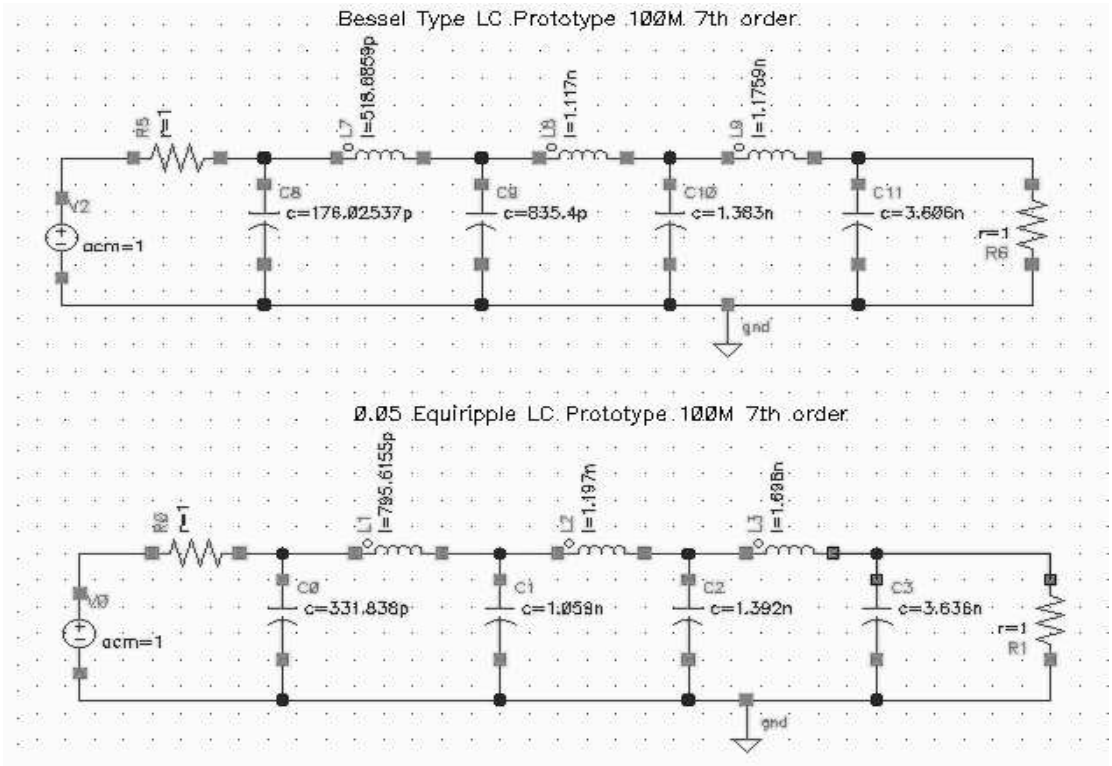


Figure 5.5 : Schematics of Designed LC Ladder Prototypes

Figure 5.6 shows the plots of AC magnitude and phase for ideal prototypes.

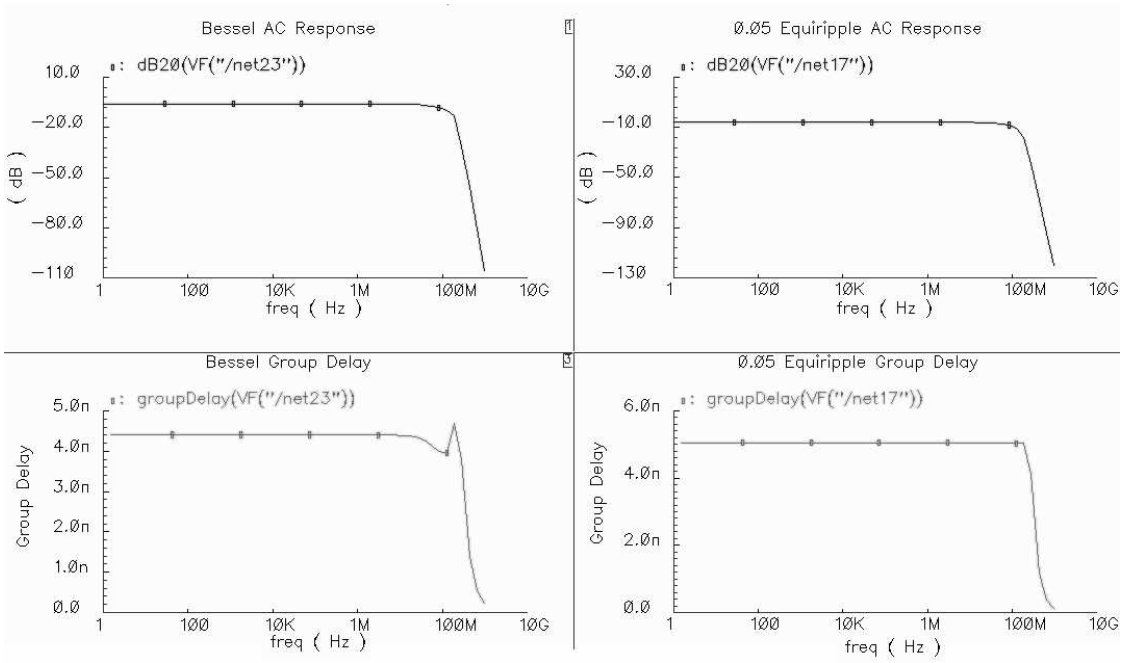


Figure 5.6 : AC Responses and Group Delays of Designed LC Ladder Prototypes

As expected the phase characteristics of these filters are suitable for HDD read channels. They both exhibit excellent phase characteristics in the passband. Since the in Bessel type filter the group delay flatness is limited to cutoff frequency, but in 0.05° Equiripple filter this flatness exceeds cutoff frequency. Since the degree of the filter is selected small enough, the ripples in phase characteristics are negligible. So the 0.05° Equiripple prototype is selected for the seven order log domain filter.

5.3 Design of 7th Order 0.05° Equiripple LC Ladder Prototype

Since 0.05° equiripple type LC ladders have better group delay performance than the Bessel types, the choice is equiripple. The designed LC ladder prototype specifications and element values are given below. The choice of R_L and R_S values will be dependent on the bias current value of the actual filter. The initial value of actual filter's bias current is chosen $I_o = 100\mu A$.

$$R = \frac{V_T}{I_o} \tag{5.1}$$

So the calculated value for source and load resistance of the prototype filter is

$$R = \frac{25mV}{100\mu A} = 250\Omega$$

The LC ladder prototype is shown in Figure 5.7.

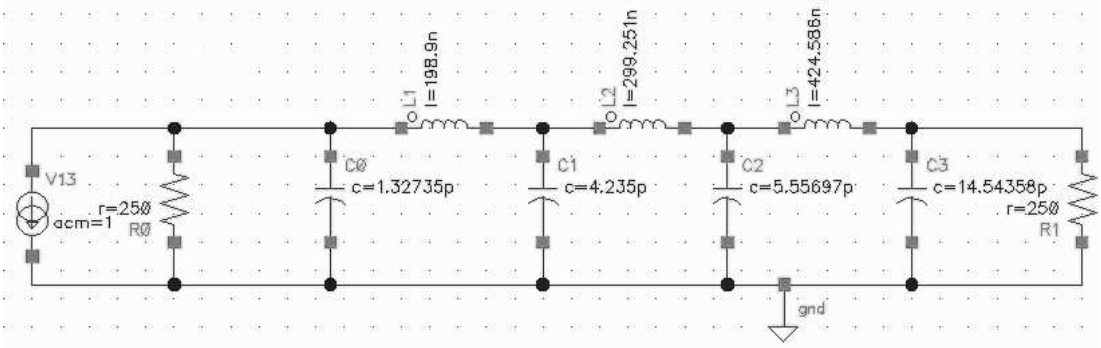


Figure 5.7 : 0.05° Equiripple LC Ladder Prototype

The designed cut off frequency is 100MHz. As expected group delay flatness extends to 200MHz range ($\geq 2f_C$)

Figure 5.8 shows the AC simulation results for 0.05° equiripple ideal LC ladder prototype.

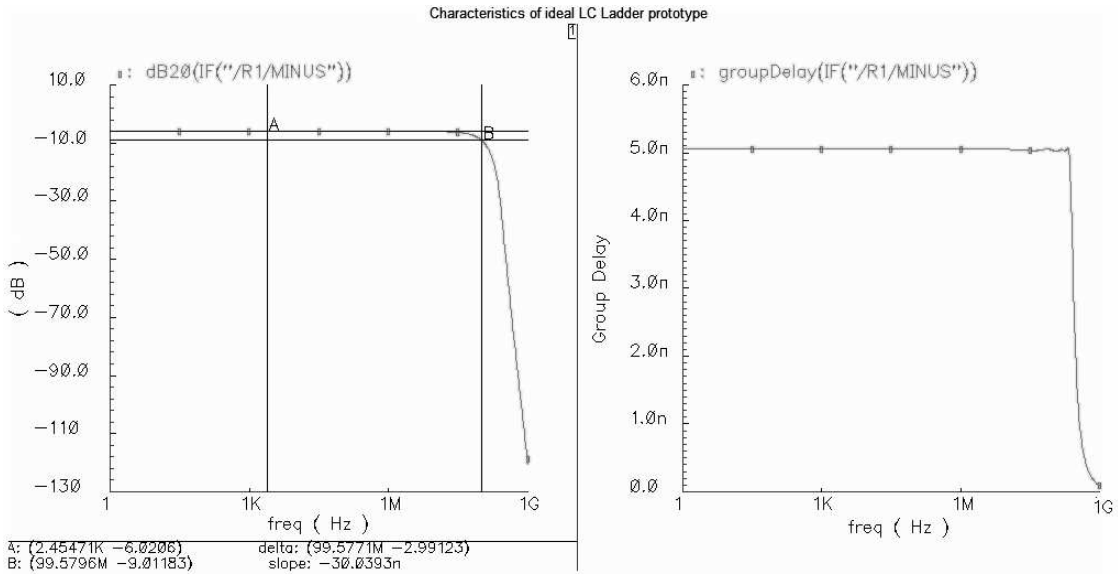


Figure 5.8 : AC characteristics of 0.05° Equiripple LC Ladder Prototype

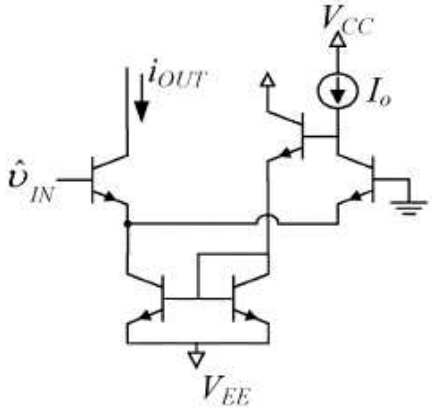
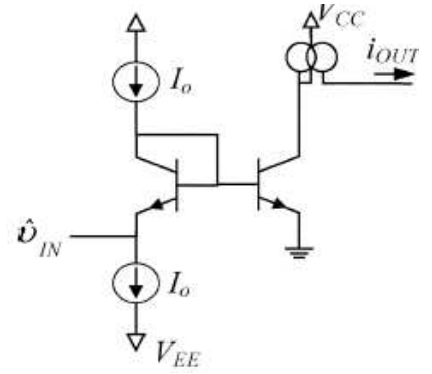
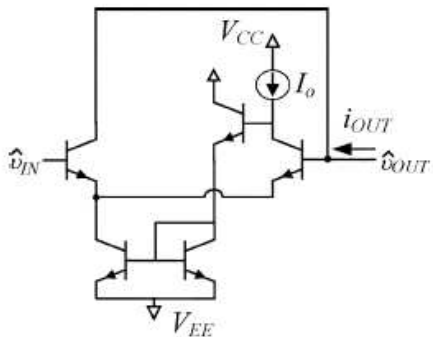
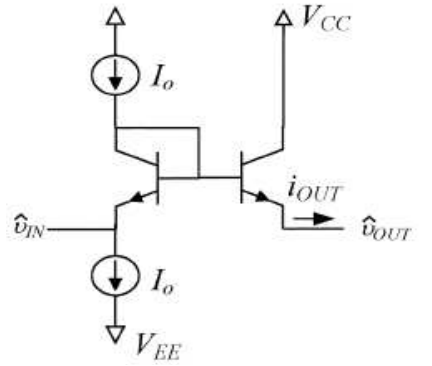
5.4 Design of 7th Order Filter Using LC Ladder Simulation Method

5.4.1 Log Domain Transconductors

In LC ladder simulation methods the elements of LC ladder prototypes are simulated using log domain equivalents of ideal elements in log domain. These log domain equivalents generally obtained using transconductors. When log domain operation is required, transconductors become log domain transconductors. In literature many transconductor topologies are proposed. All of them use translinear principle and the exponential characteristics of the bipolar transistors. In [9] a set of different transconductor cells are proposed. These transconductors are named positive or negative exponential transconductor cells. Negative exponential transconductor cells realize the same function as the positive ones. But the only difference is negative cells sink the output current, while positive ones are sourcing. This fact brings a minus sign in front of the defining equations of the positive cells.

Table 5.3 summarizes the transconductor cells described in [9].

Table 5.3 : Exponential Transconductor Cells [9]

Exponential Transconductor Cell Type	Transistor Level Schematic	Equation
Single-input negative exponential transconductor cell (E- cell).		$I_{OUT} = I_O \cdot e^{\hat{V}in/V_T}$
Single-input positive exponential transconductor cell (E+ cell).		$I_{OUT} = -I_O \cdot e^{\hat{V}in/V_T}$
Dual-input negative exponential transconductor cell (E+ cell).		$I_{OUT} = I_O \cdot e^{(\hat{V}in-\hat{V}out)/V_T}$
Dual-input positive exponential transconductor cell (E- cell).		$I_{OUT} = -I_O \cdot e^{(\hat{V}in-\hat{V}out)/V_T}$

5.4.2 Initial Design

After designing and verifying the LC ladder prototype, an initial form of actual log domain filter is designed. The elements in LC ladder prototype are simulated in log domain. In order to do that the ideal elements are replaced with log domain equivalents. These equivalents designed using the exponential transconductor cells mentioned before. The LC ladder prototype has 3 different types of elements which are; Grounded Resistor, Floating Inductor and Grounded Capacitor.

So for the actual filter design, the equivalents of these elements will be needed. These elements are chosen from the proposed topologies in [9]. In order to understand the operation of these proposed topologies two functions called EXP and LOG are defined.

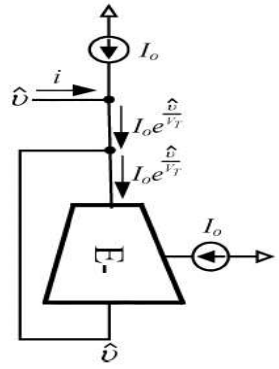
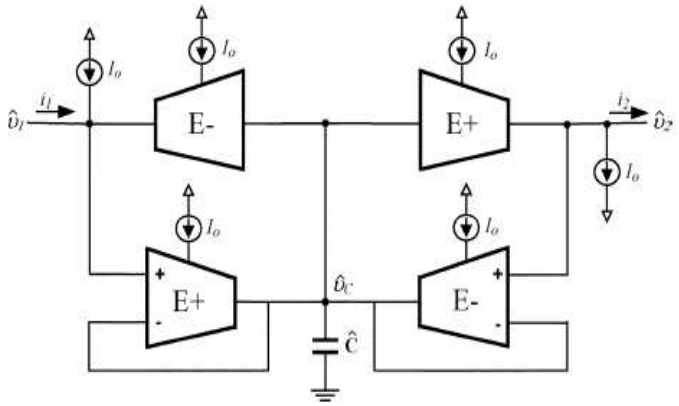
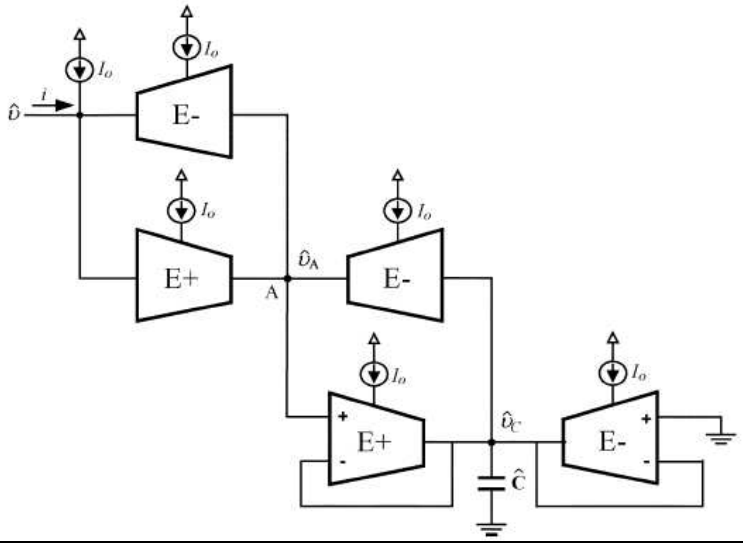
$$V = EXP(\hat{V}) = V_T \cdot e^{\hat{V}/V_T} - V_T \tag{5.2}$$

$$\hat{V} = LOG(V) = V_T \cdot \ln(\frac{V + V_T}{V_T}) \tag{5.3}$$

These functions are used to convert elements from log domain to linear domain and from linear domain to log domain respectively. While doing this conversion in order to preserve the linearity of the whole topology the currents of the elements replaced must be equal to the ideal prototype element currents.

The summary of the proposed topologies and their design equations are shown in Table 5.4. As seen from the table the resistor value is determined by the value of the bias current. The capacitor value in grounded capacitor equivalent circuit is same as the ideal LC ladder capacitor value. The capacitor value in floating inductor equivalent circuit is determined by both the inductor value of the ideal LC ladder and the bias current.

Table 5.4 : The Log Domain Equivalents of Elements in Ideal LC Ladder Prototype

LC Ladder Prototype Element	Element Schematic	Design Equation for Log Domain
Grounded Resistor (R)		$\hat{R} = \frac{V_T}{I_O}$
Floating Inductor (L)		$\hat{C} = \frac{L \cdot I_O^2}{V_T^2}$
Grounded Capacitor (C)		$\hat{C} = C$

In order to analyze the topologies mentioned above, the equations of elements in linear domain are a good start. The linear domain equation for a grounded resistor is

$$I = \frac{V}{R} \tag{5.4}$$

applying equation (5.2) to (5.4), equation (5.5) is obtained.

$$I = \frac{V_T \cdot e^{\hat{V}/V_T} - V_T}{R} \tag{5.5}$$

To preserve linearity of an element and to simulate it in log domain the currents in log domain and linear domain must be equal. Assuming the resistor equivalent in log domain will be realizing equation (5.6),

$$\hat{I} = I_O \cdot e^{\hat{V}/V_T} - I_O \tag{5.6}$$

$$I = \hat{I} = \frac{V_T \cdot e^{\hat{V}/V_T} - V_T}{\frac{V_T}{I_O}} \tag{5.7}$$

Equation (5.6) can be rewritten as (5.7) which can be realized using single input exponential transconductor cell as shown in Table 5.4. Next element needed to simulate in log domain is the floating inductor. The linear domain equation of a floating inductor is as in (5.8).

$$I = \frac{1}{L}\int (V_1 - V_2) \tag{5.8}$$

Again applying EXP function defined in (5.2), equation (5.9) is obtained.

$$I = \frac{1}{L}\int (EXP\ (\hat{V}_1) - EXP\ (\hat{V}_2)) \tag{5.9}$$

The dual input exponential transconductor cells in the log domain inductor topology perform the subtraction and the integration. The resulting current flowing through log domain equivalent is given in (5.10).

$$I = \hat{I} = \frac{I_O^2}{\hat{C} \cdot V_T^2}\int (EXP\ (\hat{V}_1) - EXP\ (\hat{V}_2)) \tag{5.10}$$

The capacitor equivalent the current and the voltage of the circuit are equal to the current and the voltage the ideal LC ladder element. This may be obtained from the KCL at node A (Table 5.4) and using the equations of transconductor elements.

$$I_O \cdot e^{(\hat{V}-\hat{V}A)/V_T} = I_O \cdot e^{(\hat{V}_C-\hat{V}_A)/V_T} \tag{5.11}$$

$$\hat{V}_C = \hat{V} \tag{5.12}$$

The current flowing through the equivalent circuit is given in (5.13).

$$I = \hat{I} = I_O \cdot e^{V_A/V_T} - I_O \tag{5.13}$$

The theoretical element values are calculated using the equations in Table 5.4. These results are summarized and compared with ideal LC ladder prototype element values in Table 5.5.

Table 5.5 : Theoretical Capacitor Values for 0.05° Equiripple Log Domain Filter

Element value @LC ladder prototype	Element value @Log domain filter	Name of the passive element @LC ladder prototype
1.32735 pF	1.32735 pF	C0
198.9 nH	3.1824 pF	L1
4.235 pF	4.235 pF	C1
299.251 nH	4.788 pF	L2
5.55697 pF	5.55697 pF	C2
424.586 nH	6.7933 pF	L3
14.5435 pF	14.5435 pF	C3

The whole design is made for AMS 0.35µ BiCMOS process. This process has a peak f_T of 30GHz at 80µA/µm. Process also have vertical pnp transistors. For log domain equivalents of the passive elements we used “npn121” transistor of the process which has 1 emitter, 1 collector and 2 bases. The emitter area of the transistor also can be modified by the designer.

Used npn transistor parameters and properties can be summarized as in Table 5.6;

Table 5.6 : BJT Transistor Parameters Used in Design

AMS 0.35µ npn transistor
npn121 : 1 collector, 1 emitter, 2 bases
Device area parameter = 12x
Bias Current = 100 µA

The transistor area is selected according to dc current flowing from the device such that, the operating point of the transistor stays on the left side of the fT –IC curve. But the possible tuning range of the bias current is also considered. So that high drops at f_T value because of current variations are avoided. This fact is illustrated in Figure 5.9.

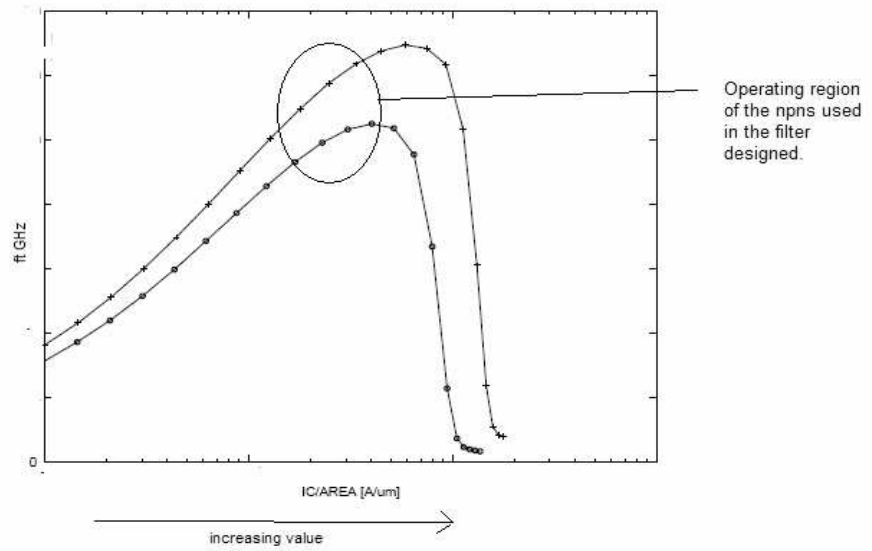


Figure 5.9 : Choosing BJT Transistor Size

The overall schematic of the 7th order 0.05° Equiripple Low pass filter is shown in the Figure 5.10.

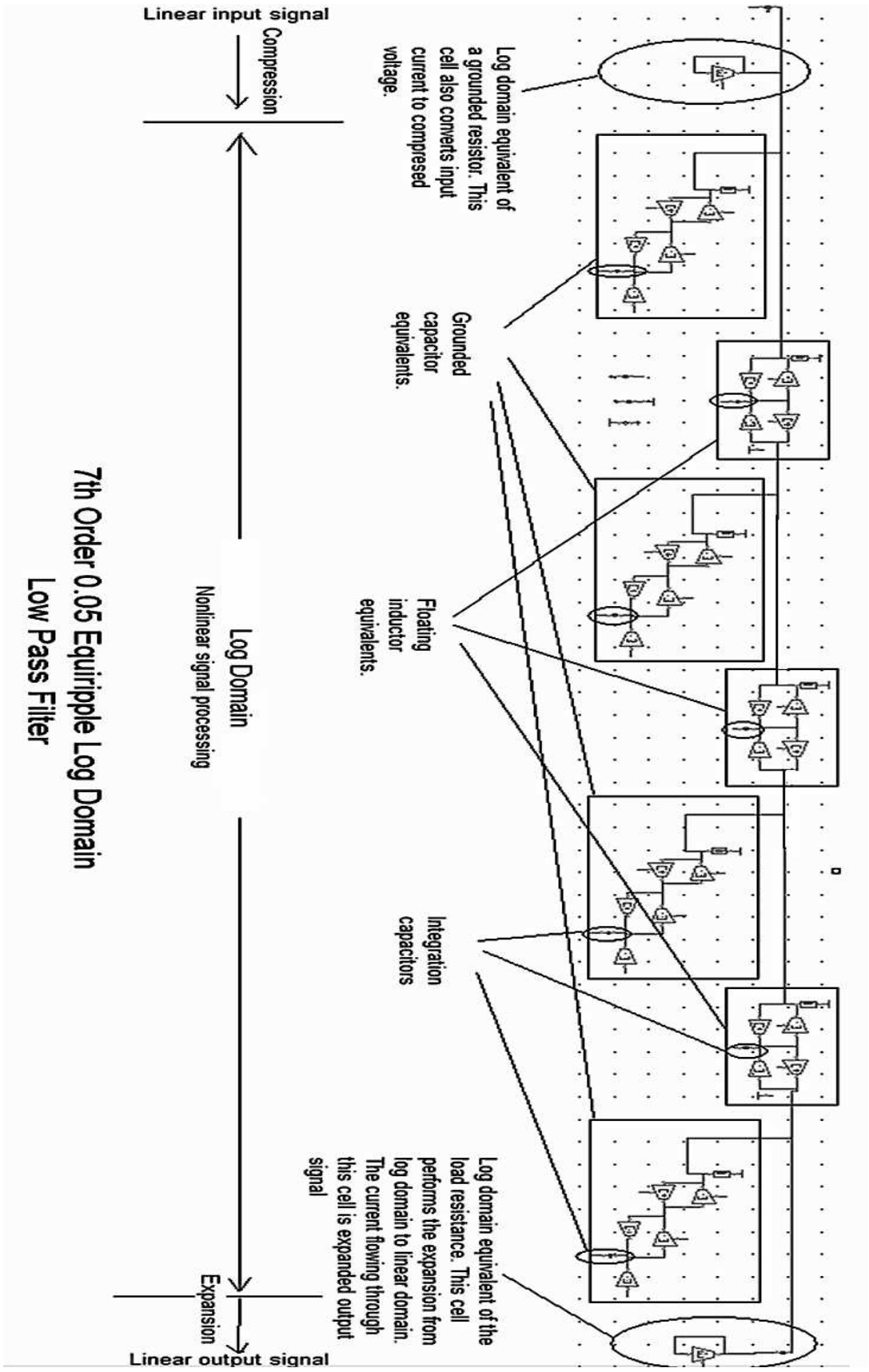


Figure 5.10 : Overall Schematic of 7th Order Log Domain Filter Simulating LC Ladder Prototype

After completing the initial design the performance of the ideal prototype circuit and the actual transistor level design has been compared. The AC analyses have been performed using Cadence Spectre Simulator. Since the filter is a current mode circuit, a current of AC 1A is injected from the input of the filter. Output current of the filter is observed. The AC magnitude and group delay performance of the filter is shown in Figure 5.11.

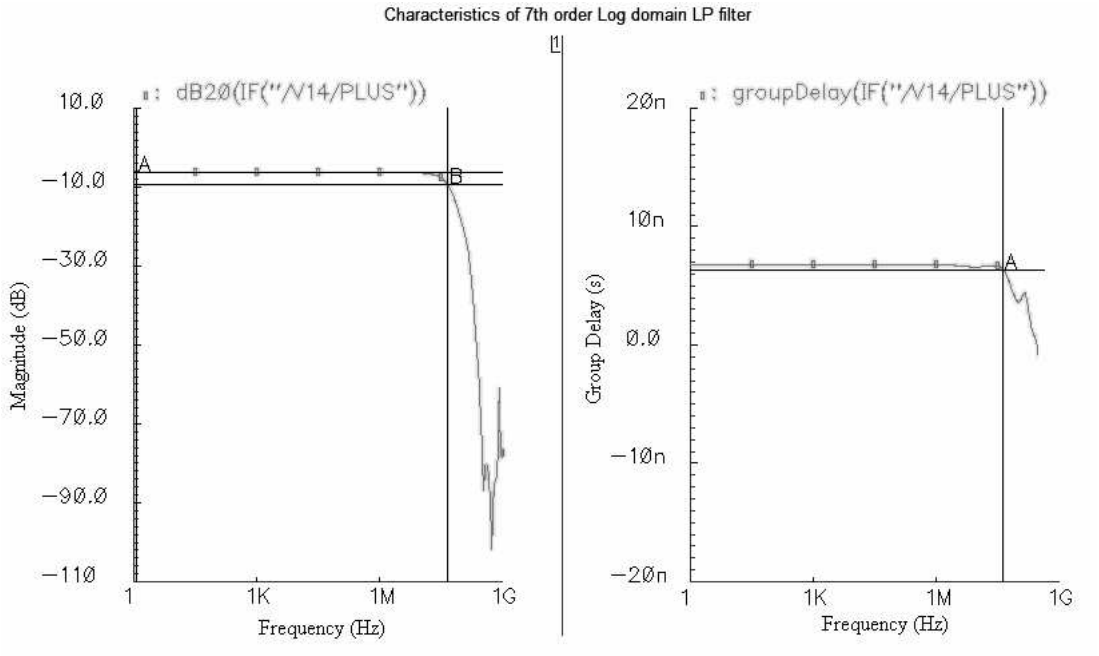


Figure 5.11 : Initial AC Simulation Results of the Filter

And the comparison of important specifications of the filter with LC ladder prototype is in Table 5.7.

Table 5.7 : Ideal LC Ladder Prototype Vs Initial Design

	Ideal LC Ladder Prototype	Log Domain Filter (Initial design)
Passband Gain (dB)	-6.02	-6.22
Cut Off Frequency (3dB- MHz)	100MHz	48 MHz
Group Delay Flatness (≤ 5 %)	Flatness Range ≥ 2 f_C	f_C ≤ Flatness Range ≤ 1.5fc

As seen from the results the filter has similar passband gain but a cut off frequency shift is observed. Also group delay flatness range is narrower than the prototype. There are several parasitic effects that impact the performance of the filter. From now on these effects are investigated and some improvements on this initial design is presented.

5.4.3 Modeling Nonideal Effects of Log Domain Filter

As it is mentioned before, in the initial deign filter response is different than the ideal LC prototype. In log domain filters the transistor nonidealities can be divided into two groups according to their effects on filter responses.

1. Effects that causes magnitude errors on filter responses
2. Effects that causes phase errors on filter responses.

These effects are the nonidealities coming from bipolar transistors. The parasitic emitter resistance and base resistance of the bipolar transistors are the main sources of magnitude errors. Finite beta of bipolar transistors and Early effect are the main sources of phase errors.

These errors affected group delay flatness, cut off frequency and passband gain of the log domain filter. In order to model these effects and verify this claim ideal LC prototype has been modified in order to obtain a non ideal prototype.

First of all to model parasitic dissipations resistors have been added to the ideal LC prototype. Used model for dissipative inductor and dissipative capacitor are shown in Figure 5.12. Here d_L and d_C are some coefficients.

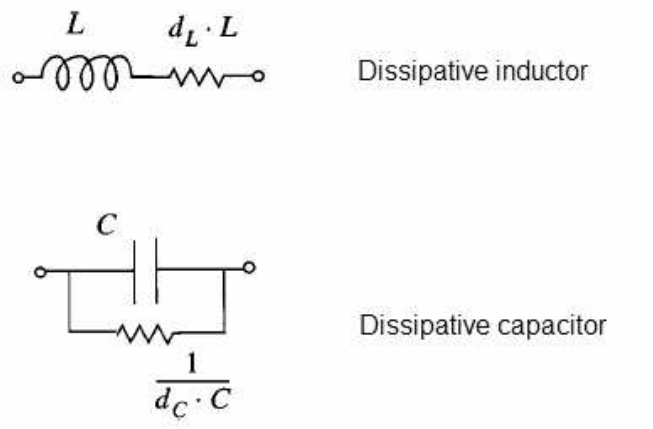


Figure 5.12 : Dissipative Capacitor and Dissipative Inductor

A second modification is applied to the ideal LC prototype. Element values of the LC ladder have been changed by a factor of k. This modification caused a frequency shift in ideal LC ladder response as in the actual case. The changes have been summarized in Table 5.8.

Table 5.8 : The Modifications on Ideal LC Ladder Prototype

	Element Type	New Value	Related Equation	Modeling Status
1st modification (change in element value)	Ideal Inductor (L) & Ideal Capacitor (C)	L' = L / k C' = C / k	$k = \frac{V_T}{V_T + R_E I_O}$	Models parasitic emitter resistance (R_E)
		L' = L / k C' = C / k	$k = \frac{V_T}{V_T + \frac{R_B I_O}{\beta}}$	Models parasitic base resistance (R_B)
2nd modification (add a dissipative element)	Ideal Inductor (L)	Add a series resistor to inductor $R_l = m / n$	$m = \frac{2}{(\beta + 7)^2}$ $n = \frac{\beta}{\beta + 2}$	Models Finite Beta Effect
	Ideal Capacitor (C)	Add a parallel resistor to capacitor $R_c = n / m$	$m = \frac{2}{(\beta + 7)^2}$ $n = \frac{\beta}{\beta + 2}$	Models Finite Beta Effect

Using these theoretical results [11] a new nonideal LC ladder is obtained. The final nonideal LC ladder schematic is shown in Figure 5.13. In order to determine the parasitic effects for designed filter a set of parametric simulations are made. Using Cadence Analog Environment tool the parameters modeling the nonidealities (k,m,n) have been swept over certain ranges. And various plots, showing the effect of nonidealities, have been obtained. These plots are in Figures 5.14, 5.15 and 5.16.

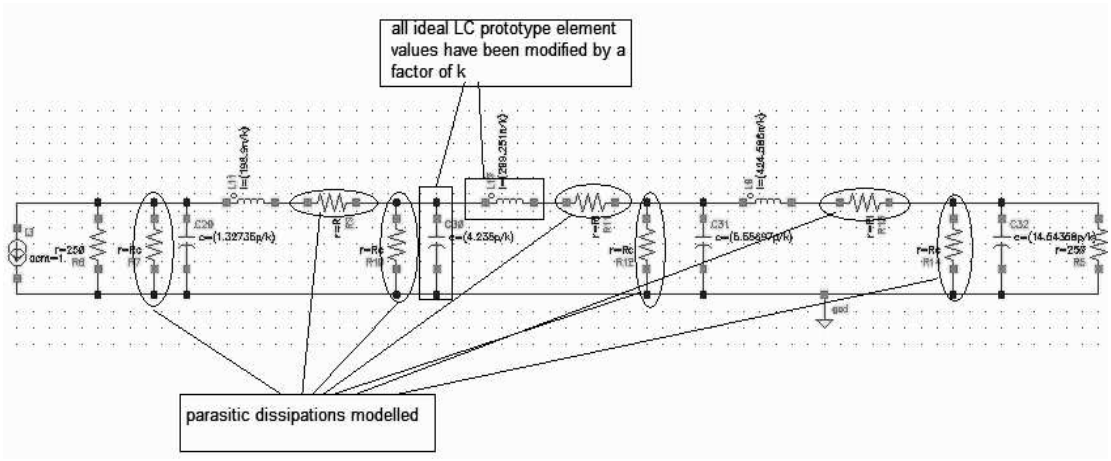


Figure 5.13 : Nonideal Effects Added to LC Ladder Prototype

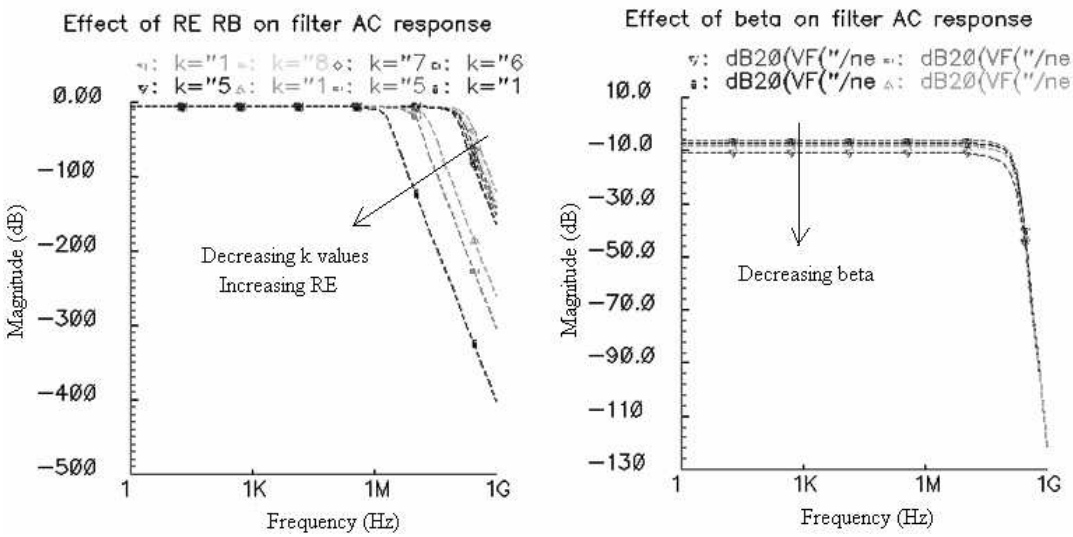


Figure 5.14 : Effect of Added Nonidealities on LC Ladder Prototype (AC magnitude)

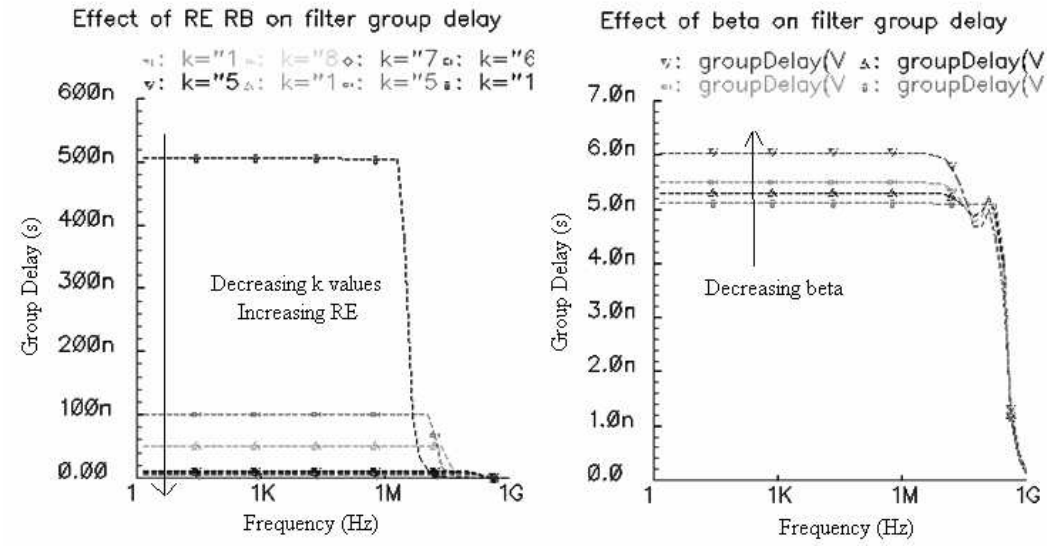


Figure 5.15 : Effect of Added Nonidealities on LC Ladder Prototype (group delay)

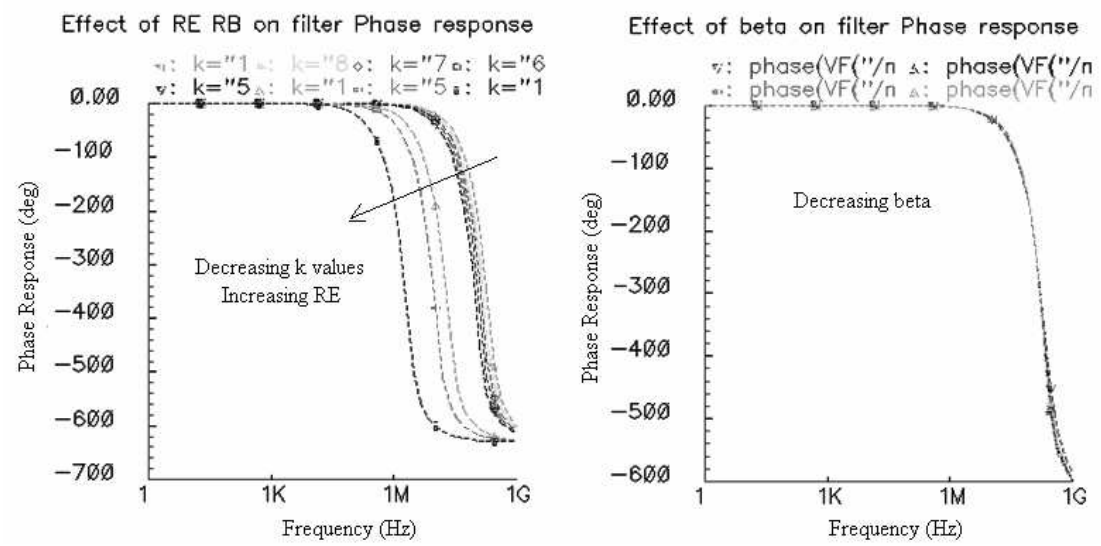


Figure 5.16 : Effect of Added Nonidealities on LC Ladder Prototype (phase)

The actual filter response and modified LC ladder prototype filter response are almost matched. The simulation results of the LC ladder matched to the actual filter results for k = 0.65, $R_l = 450*10^{-6}$ and $R_c = 2.22\ 10^3$. Here it will be wise to note that these parameters are purely process depended, and they are obtained with the help of simulator. For different processes these values can take different values.

Table 5.9 compares the important specifications of ideal LC ladder, parasitic added LC ladder and the actual filter.

Table 5.9 : Simulation Result Comparison

	Ideal LC Ladder Prototype	Parasitic Added LC Ladder Prototype	Log Domain Filter (Initial design)
Passband Gain (dB)	-6.02	-6.24	-6.22
Cut Off Frequency (3dB- MHz)	100MHz	50 MHz	48 MHz
Group Delay Flatness (≤ 5 %)	Flatness Range ≥ $2f_C$	Flatness Range $=2f_C$	$f_C \leq$ Flatness Range $\leq 1.5fc$

5.4.4 Improvements on Initial Design

After the results of the initial design and the modeling of nonidealities, some improvements are made. First of all to compensate for cut off frequency shift the nominal bias current has been increased. An increase of 100μA bias current shifted cut off frequency of the filter up to 70MHz. After that point a set of simulations are performed and some specifications of the initial design is obtained to see the main problems of the circuit. Problems of the initial design can be arranged as the following;

1. The finite beta causes cutoff frequency shift and AC magnitude errors.
2. Parasitic emitter resistance causes cutoff frequency shift.
3. The output stage of the filter causes extra distortion resulting higher THD (>1%).
4. Programming is not wide range.
5. Boost feature is not clearly programmable.

The first two effects are also modeled and verified in the previous sections. In order to compensate for cutoff frequency shift we can reasonably increase the bias current of the circuit. Since the filter is designed to be programmable. The cutoff frequency error will be compensated in expense of the increased nominal bias current. The AC magnitude losses can be compensated with a proper design of the output stage.

The THD is a measure of linearity. For initial design THD values of the filter seem unsatisfactory. For 10μA input current amplitude, at 1 MHz frequency the THD value is 2.8 %. Since the internal signals are already in nonlinear domain, the first cause of excessive nonlinearity is more likely the input and output stages. So after a bit digging the cause of excessive distortion seem to be the output stage topology. To obtain equivalent of a grounded resistor the collector and the base of the transistor is connected together, which corresponds to a connection from Vin terminal of the cell to the Iout terminal of the cell in Figure 5.17. The problematic connection is also shown. This diode connected BJT becomes the main source of nonlinearity added to system.

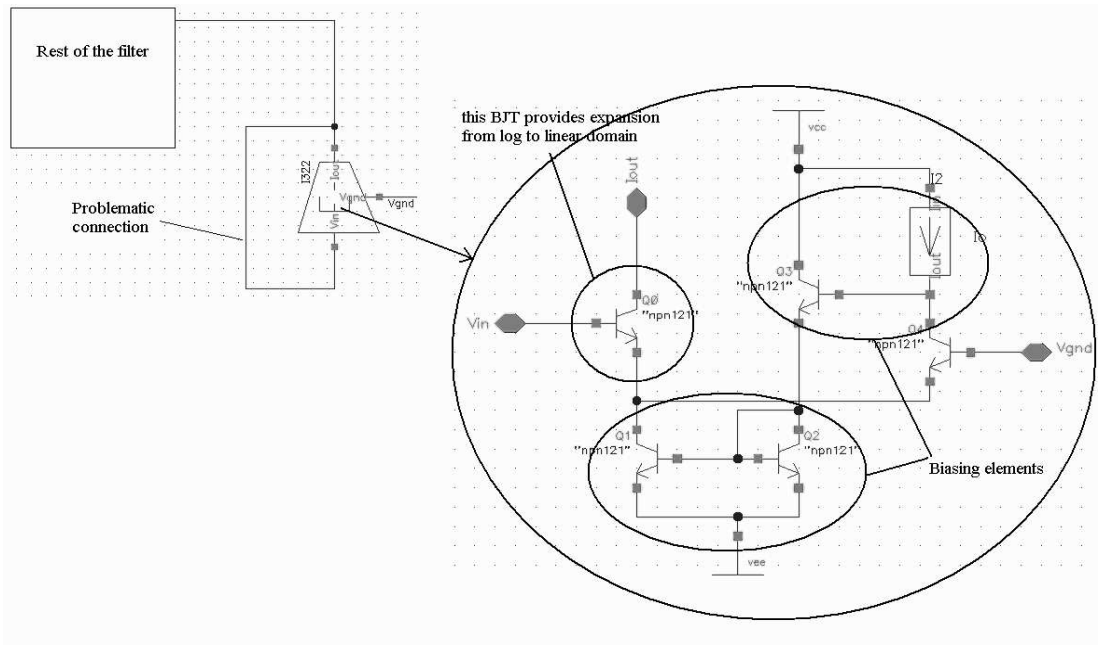


Figure 5.17 : The Reason of Excessive Distortion for Initial Design

So the output stage proposed in [15] used here to improve the linearity of the filter. This topology gets rid of the problematic connection in the previous topology, while maintaining the log to linear domain conversion. The new output stage is shown in Figure 5.18.

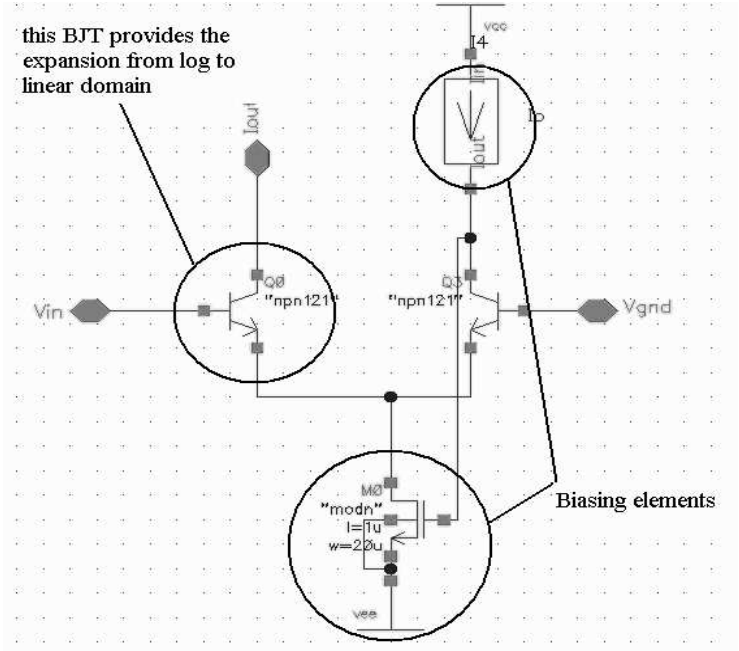


Figure 5.18 : Output Stage with EP bias

The circuit uses a different type of biasing. In this biasing scheme for a given gate voltage, any imbalance between the collector current and the input current will cause the feedback transistor to adjust the gate-to-emitter voltage in such a way as to reduce the imbalance. This is biasing type is called Enz–Punzenberger (EP) connection which was discussed in the previous sections.

It has the same transistor and current sinking configuration. But instead of sinking the output current from the rest of the filter, it directly sinks the current from the supply. Getting rid of the problematic connection of the previous architecture, THD of the overall filter can be improved. The usage of proposed output architecture is shown in Figure 5.19.

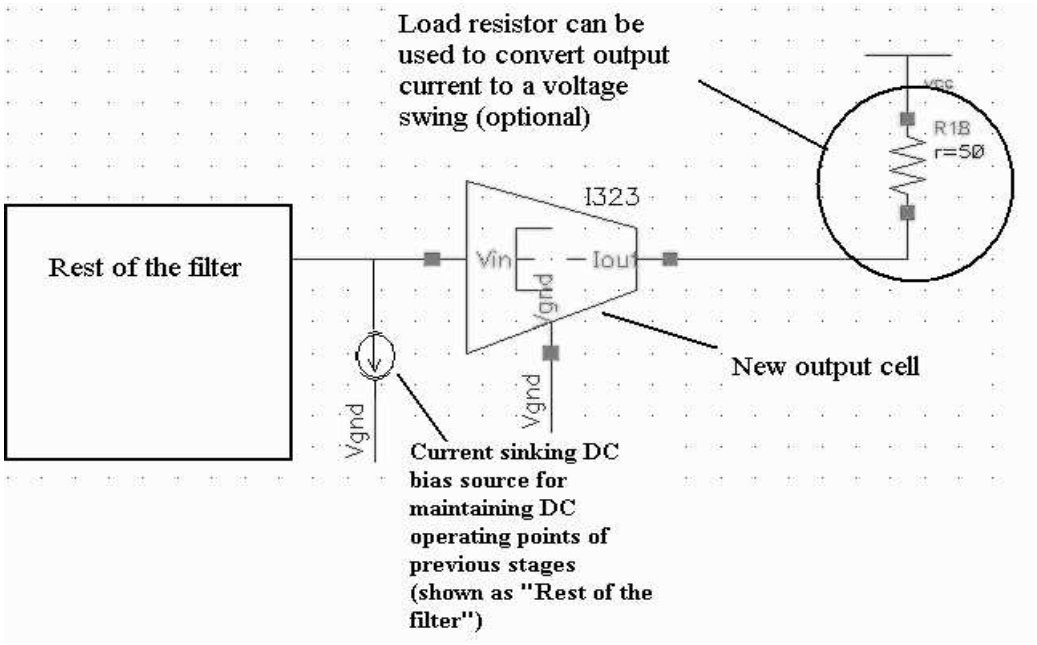


Figure 5.19 : Integration of the New Output Stage to the Rest of the Filter

The advantages of using this stage at the output can be written as the following;

1. Introduces less distortion to the system as a result THD is improved significantly
2. The output current can be turned into a voltage by adding a proper load resistor easily and without disturbing the filter operation.
3. The group delay performance of the circuit is comparable to the old output stage.
4. Overall pass band current gain of the filter is also increased for the same bias current.

To see and compare the improvements for the filter the old and the new architecture are simulated and their performances are compared. The comparison of both filters is given in Figure 5.20 and Figure 5.21. For the same bias current AC magnitude, phase characteristics and THD performances are compared. As seen from the results the THD of the filter is improved significantly. Also the gain and cutoff frequency errors are fixed.

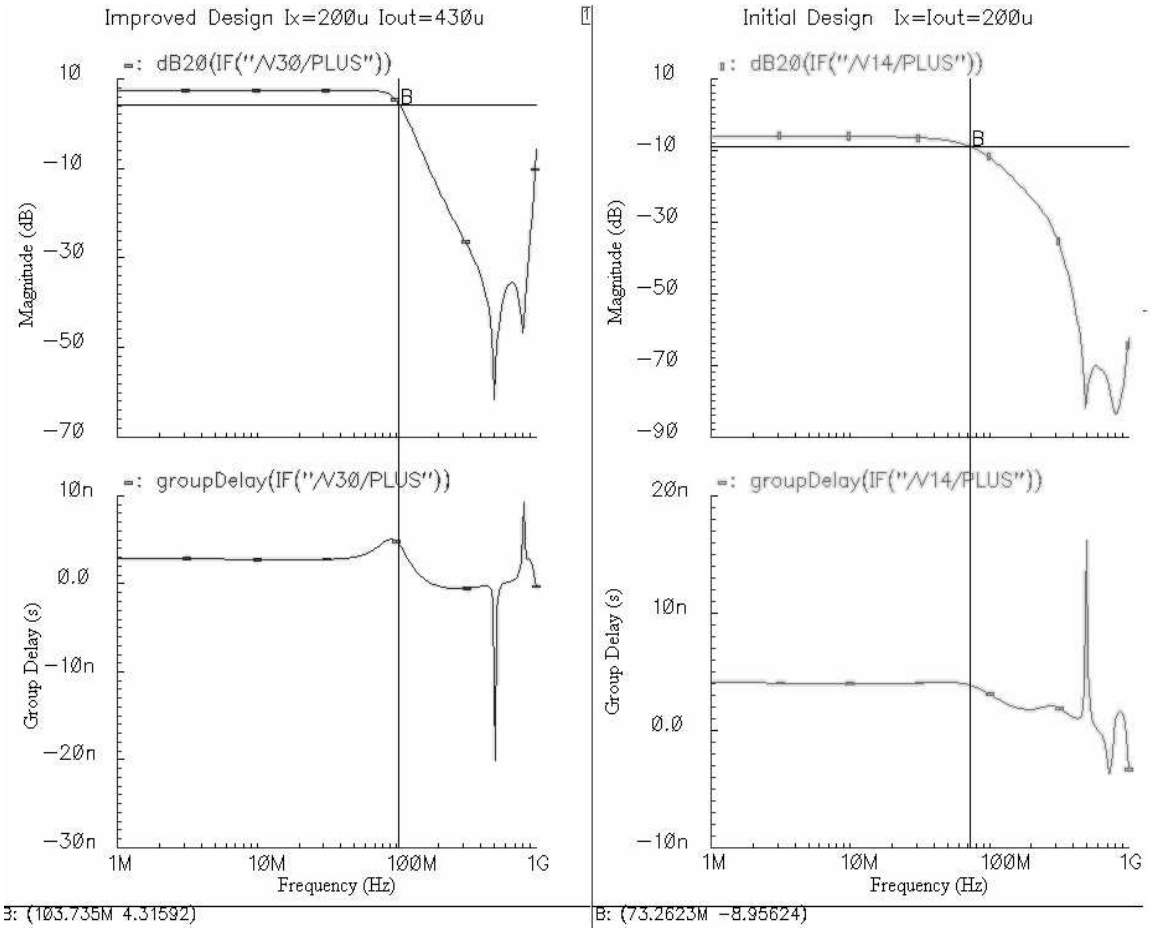


Figure 5.20 : Comparison of Old and New Designs for the Same Bias Currents

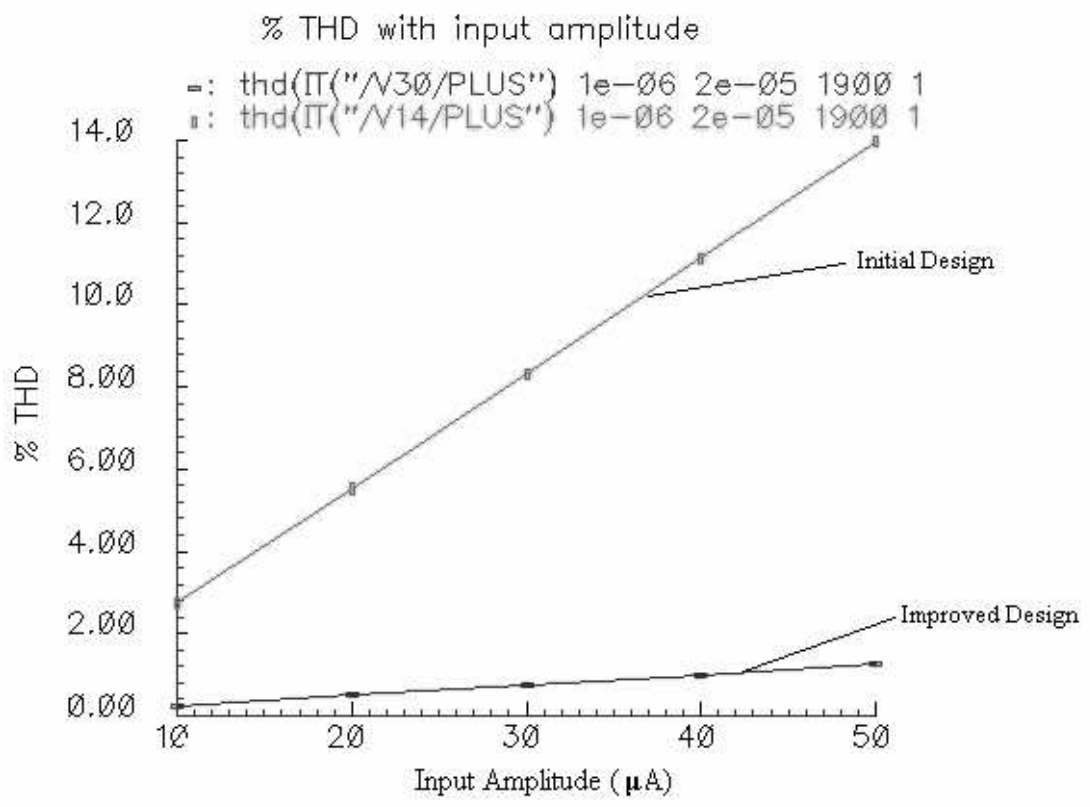


Figure 5.21 : THD Comparison for Different Input Amplitudes

Some of the important aspects of the circuits are also summarized in Table 5.10.

Table 5.10 : Comparison of Important Specifications for Improved and Initial Designs

Specification	Initial Design (with increased nominal bias current)	Improved Design (with proposed output stage)
Nominal Bias Currents	I_X =200 µA	I_X =200 µA I_{OUT} = 430 µA
Cut off Frequency @nominal bias current	70 MHz	100MHz
Passband Gain	-6 dB	7 dB
Group Delay Flatness (ripple < 10 %)	< 1.5 f_C	< 1.5 f_C
THD (%) @nominal bias, 10 µA input amplitude, 1MHz input frequency	2.7 %	0.25 %

5.4.5 Improved Programmability of the New Filter

The programming of the log domain filter is mainly done by changing the bias current of the whole filter. But unlike Gm-C cascaded filters, in LC ladder simulating filters some aspects of the circuit (gain, cutoff frequency, boost etc…) can not be tuned over a wide range independently. By changing the bias current of the designed filter over a wide range resulted unwanted boosts in the AC curves. Also that boost feature can not be programmed linearly by changing the bias current of the whole filter.

In order to add some independent flexibility to the programming feature of the filter, two bias current domains have been designed. The first bias current domain is internal bias current domain (I_X) and the second one is the input and output bias current domain (I_{OUT}). The proposed output stage combined with this flexibility improved the filters programming features. The improved programmability concept is shown in the block diagram (Figure 5.22).

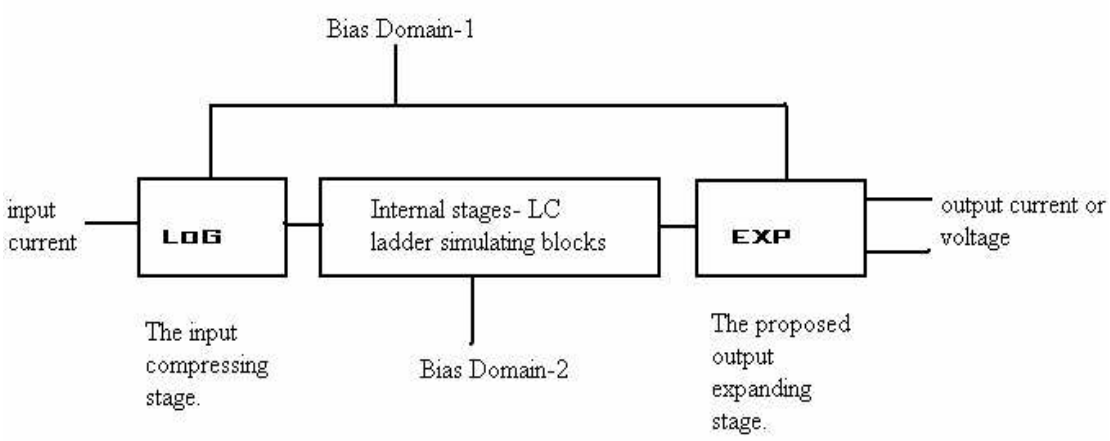


Figure 5.22 : New Programming Concept for the Filter

New programming method is summarized in Table 5.11;

Table 5.11 : New Programming Method for the Filter

Programming Type	Bias Domain-1 Current (I_{OUT})	Bias Domain-2 Current (I_X)	Effect
Cutoff Frequency Programming (Together with passband gain)	Increase I_{OUT} according to predefined value with respect to I_X	Increase I_X	Linear Increase in Cutoff Frequency
Boost Programming	Increase I_{OUT} further than the nominal value for chosen I_X	Chose a proper I_X	Added boost in AC characteristic and increases with increasing I_{OUT}

Using this programming technique the filter cutoff frequency and boost programming feature can be tuned with in proper tuning ranges independently. Table 5.12 shows the proper current values for some cutoff frequencies and THD values for corresponding bias conditions

Table 5.12 : Programming for Different Bias Currents

Bias Domain-2 Current (I_X)	Bias Domain-1 Current (I_{OUT}) Nominal	Cutoff Frequency (MHz) (No boost)	THD input amp = 10 µA input frequency=1MHz
100 µA	105 µA	60 MHz	0.46 %
150 µA	225 µA	81 MHz	0.31 %
200 µA	430 µA	103 MHz	0.25 %
250 µA	700 µA	121 MHz	0.23 %
300 µA	1100 µA	138 MHz	0.23 %

As seen from the table above bias domain-2 current is increased linearly but bias domain-1 current is increased in a quadratic characteristic. If the bias domain-1 current is increased any further a boost feature is added to the system. Figure 5.23 shows the relation between bias domain currents.

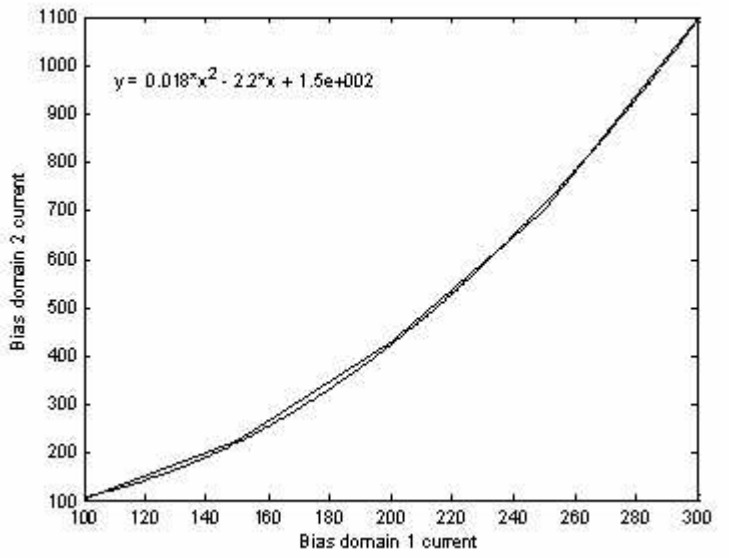


Figure 5.23 : Relation Between Current Domains

Empirically the relation between current values is obtained. (Eq. 5.14) It is wise to note that this relation depends on many parameters and is not true for all designs using this topology.

$$y = 0.018x^2 - 2.2x + 150 \tag{5.14}$$

In equation 5.14 y denotes bias domain-1 current x denotes bias domain-2 current.

The Figure 5.24 shows the AC characteristics of filter for different bias currents.

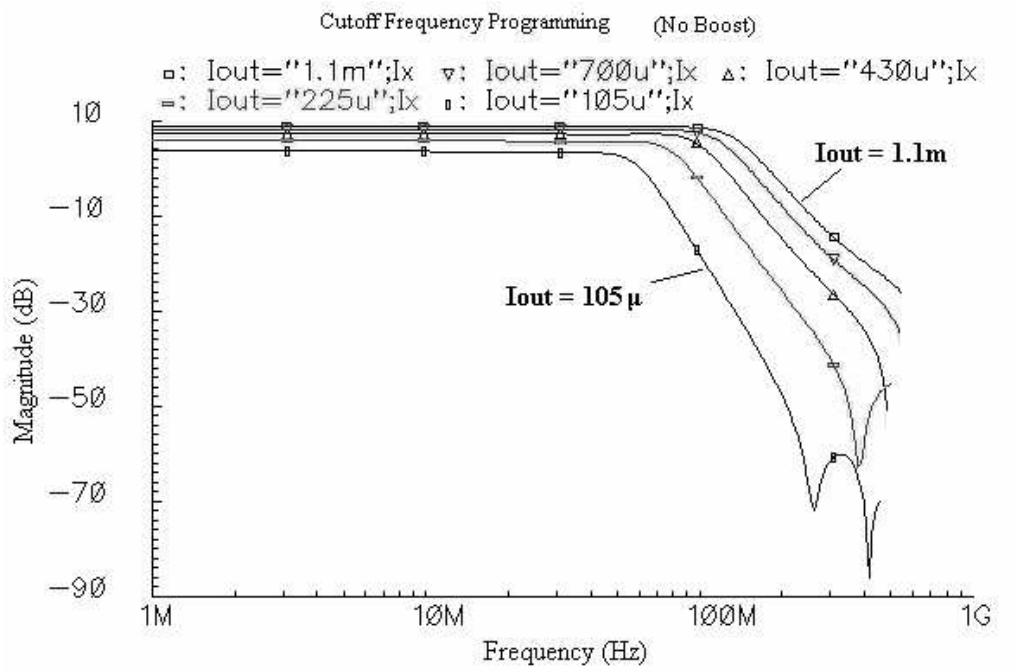


Figure 5.24 : Cutoff Frequency Programming

Figure 5.25 shows the filter tuning range.

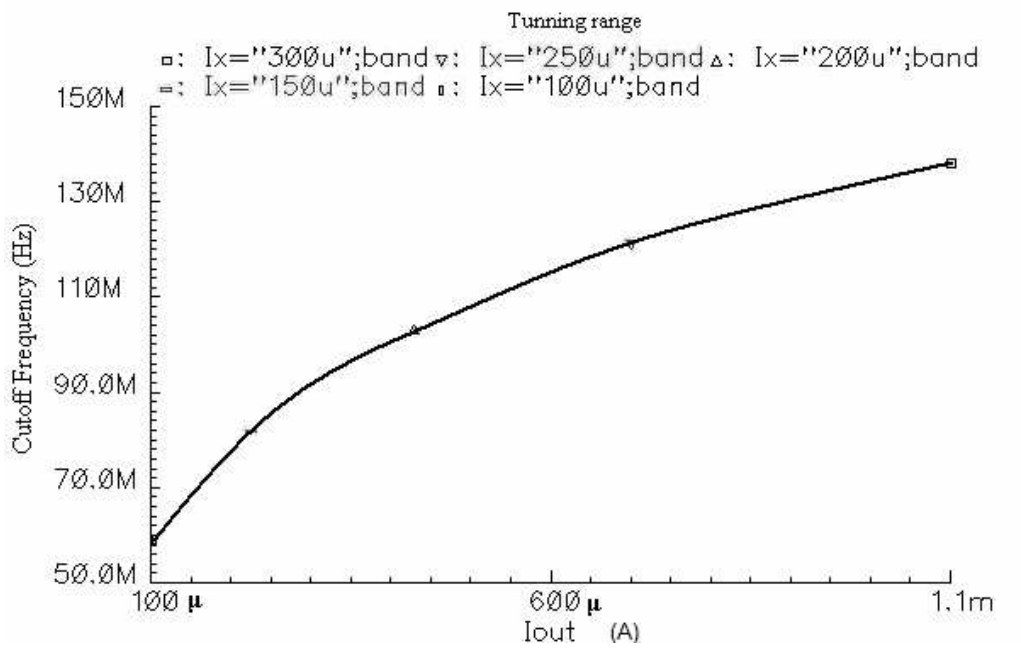


Figure 5.25 : Filter Tuning Range

Group delay flatness linearity is disturbed for the lower frequency edge of the tuning range. But for high bias currents group delay flatness is good. Group delay plots of the filter for changing bias currents are given in Figure 5.26.

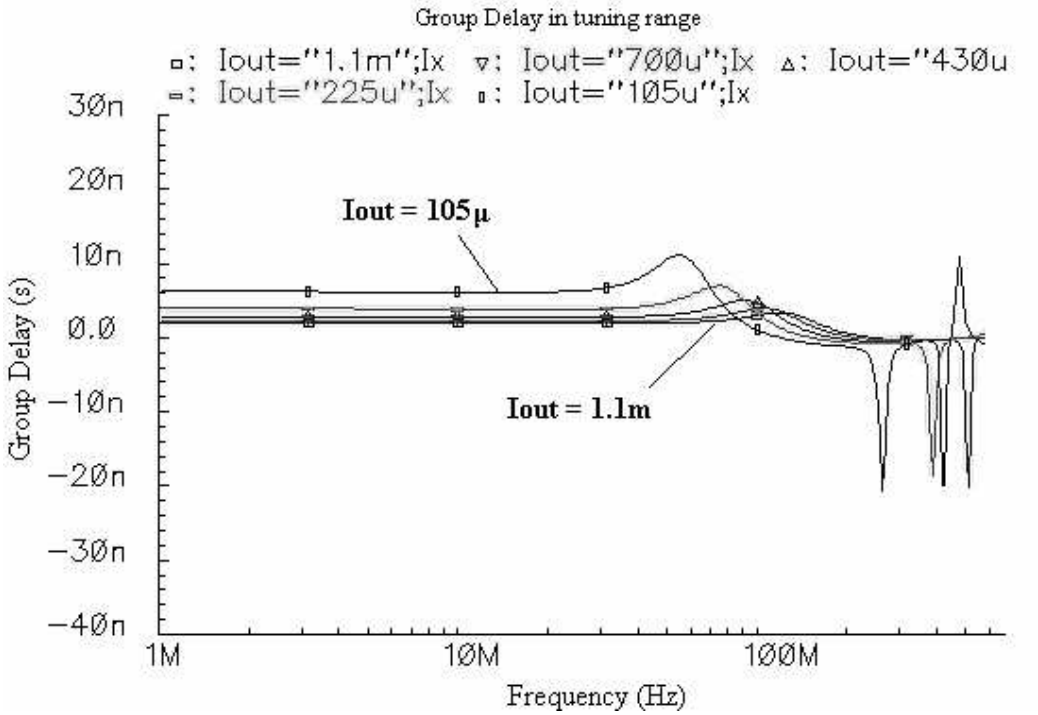


Figure 5.26 : Group Delay in Tuning Range

In tuning range THD stays below 1%. The THD of the filter for 10µA input amplitude is given for different bias current values Figure 5.27.

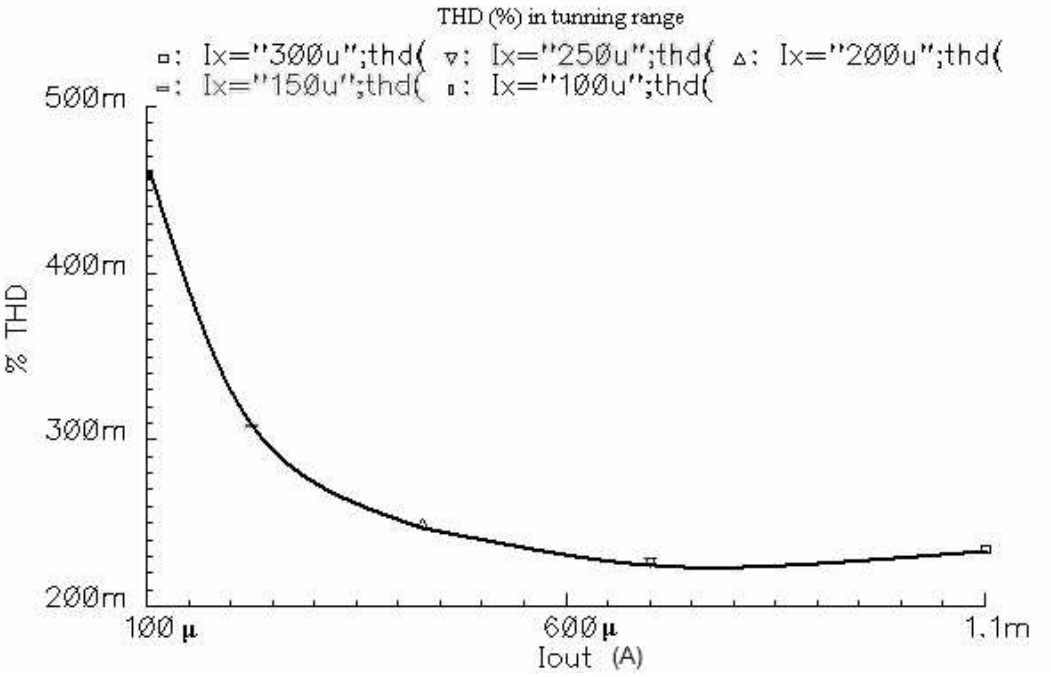


Figure 5.27 : THD in tuning range

Boost feature is not widely programmable. But separations of bias domains make the boost of the filter programmable within a small range. Increasing input and output circuit bias currents more than their nominal value, increases the amount of

boost added to system. Figure 5.28 shows the concept of programmable boost for the designed filter.

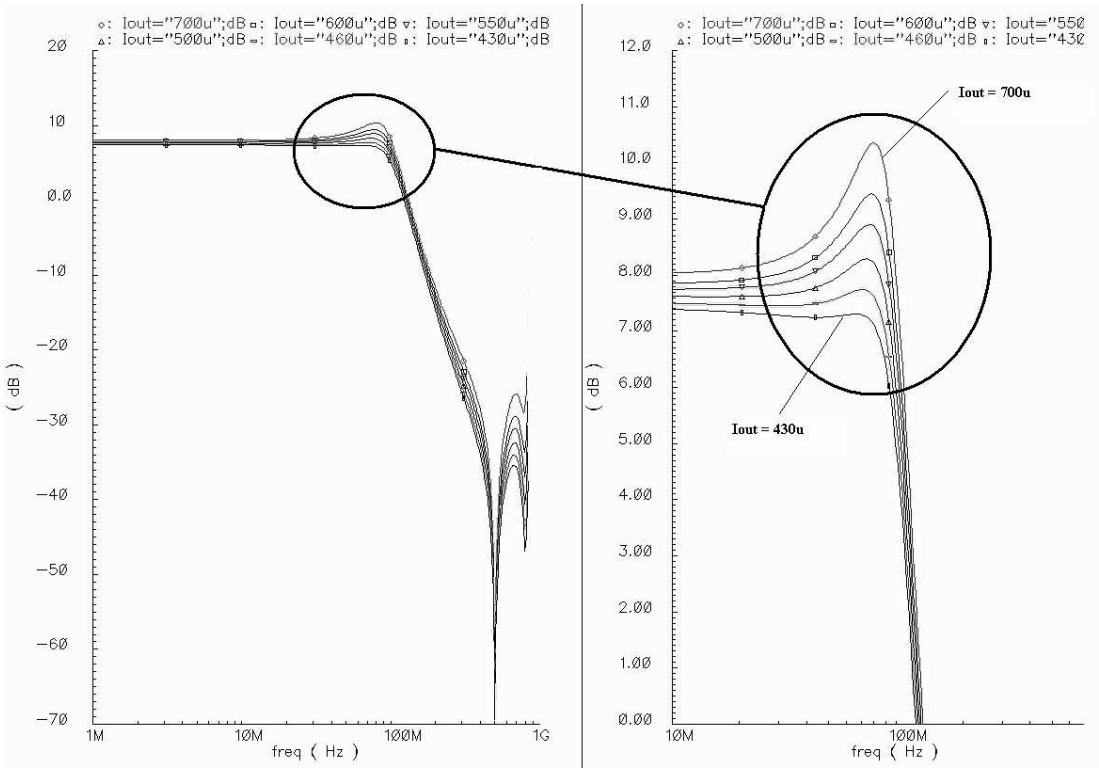


Figure 5.28 : Boost Programming Feature of the Filter

From the results presented above, it is obvious that the filter THD is improved significantly. With the proposed output stage for this filter, THD stays below % 1 in whole tuning range. The passband gain and the tuning range is also increased. With use of two different bias domains a boost programming feature is also added to the filter. All these improvements are made in expense of slightly increased bias current. The group delay flatness is disturbed only for low values of bias current. For higher currents group delay flatness stays comparable to the previous design.

5.5 Design of 7th Order Filter by Gm-C Cascading Method

After designing a 7th order log domain filter in order to compare the performance of the filters, another filter is designed by using Gm-C cascading method instead of LC ladder simulation method.

Using one of the exponential transconductor cells designed for LC ladder simulation method, the main building block for the new filter is obtained. The block diagram of the filter is shown in Figure 5.29.

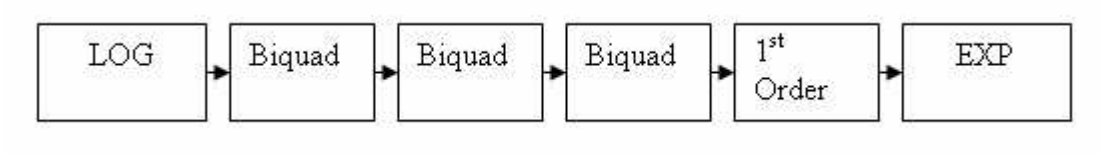


Figure 5.29 : The Block Diagram of 7th Order Log Domain Gm-C Filter

The filter designed before using LC ladder simulation method is using single ended operation. So in this design the single ended operation strategy is also used. In order to obtain a log domain integrator, the dual input positive exponential transconductor cell is used with the integration capacitor. The integrators used in the design will be replicas of this structure in a cascaded topology. The positive exponential transconductor is shown in Figure 5.30.

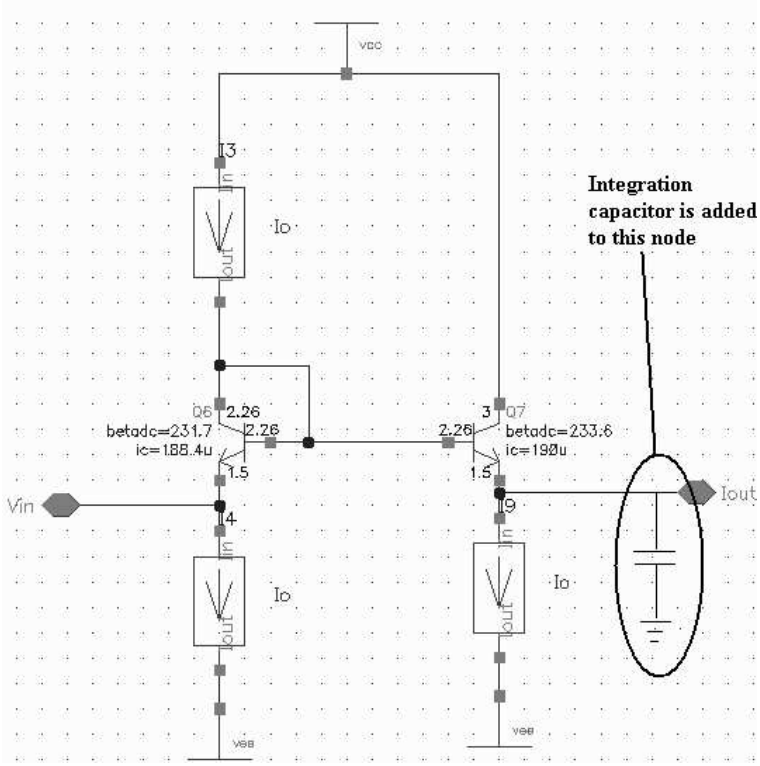


Figure 5.30 : Log Domain Gm-C Structure

By cascading the exponential Gm-C structures properly the 7th order filter is obtained. The schematic of the filter is shown in Figure 5.31.

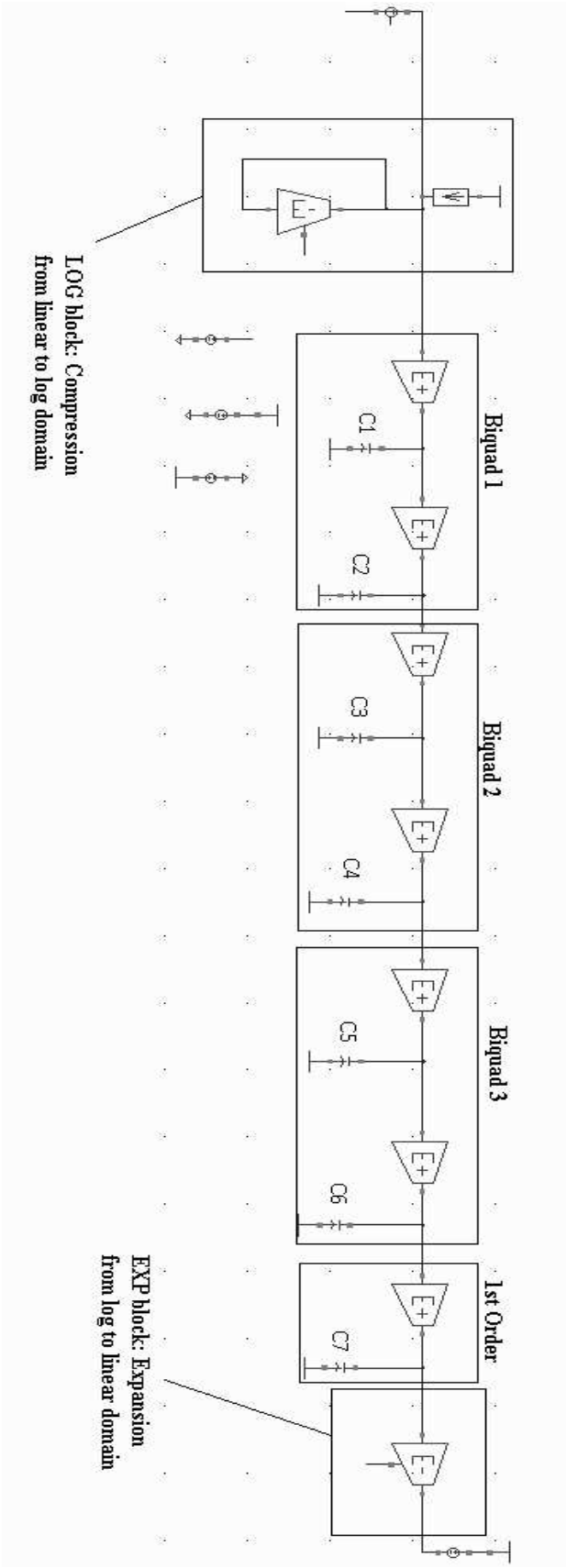


Figure 5.31 : Overall Schematic of 7th Order Log Domain Filter (Gm-C cascading)

The capacitor values for the 7th order filter by using Gm-C cascading method are shown in Table 5.13. Values are the same theoretical values calculated in [12].

Table 5.13 : Capacitor Values for Gm-C Cascaded Filter [12]

Name of the Capacitor	Capacitor Value
C1	4.9 pF
C2	5.4 pF
C3	2.5 pF
C4	2.2 pF
C5	2.7 pF
C6	0.9 pF
C7	3.7 pF

The same input stage and proposed output stage in design of LC ladder filter is also used here. This filter cutoff frequency is tuned by changing the bias current. The AC characteristic of the filter is shown for different bias currents (Figure 5.32).

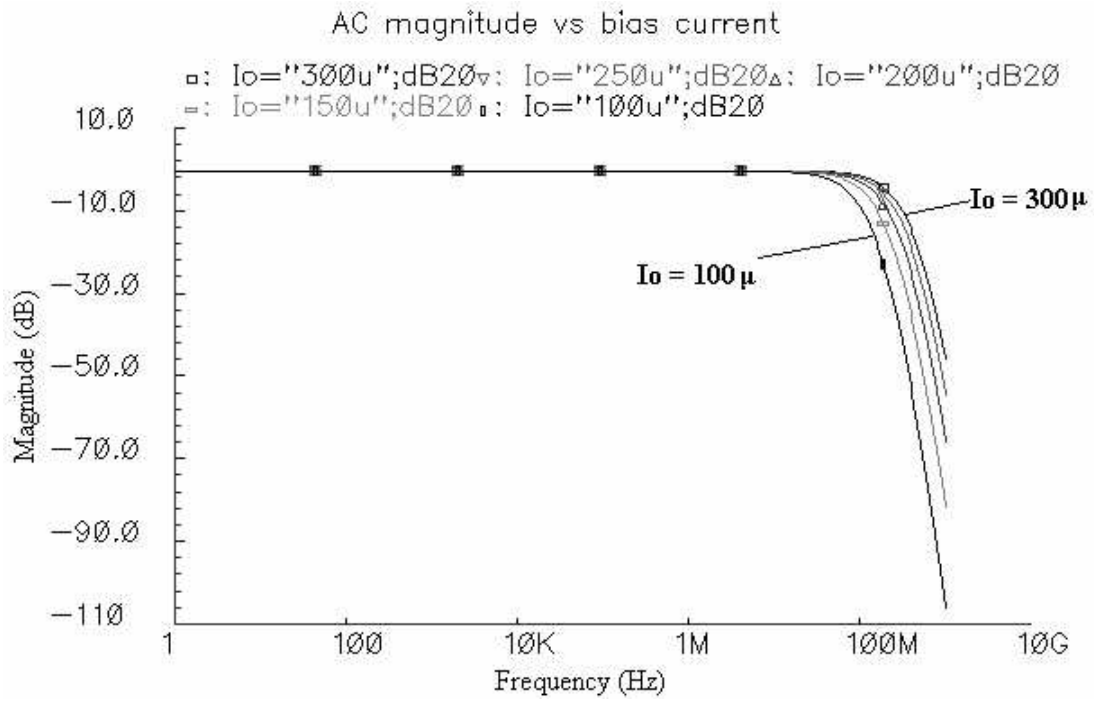


Figure 5.32 : AC Characteristic of Log Domain Gm-C Filter for Different Bias Currents

Capacitor values for the filter are calculated using equiripple approximation. As a result the group delay is flat in the passband. The group delay curves of the filter are shown in Figure 5.33.

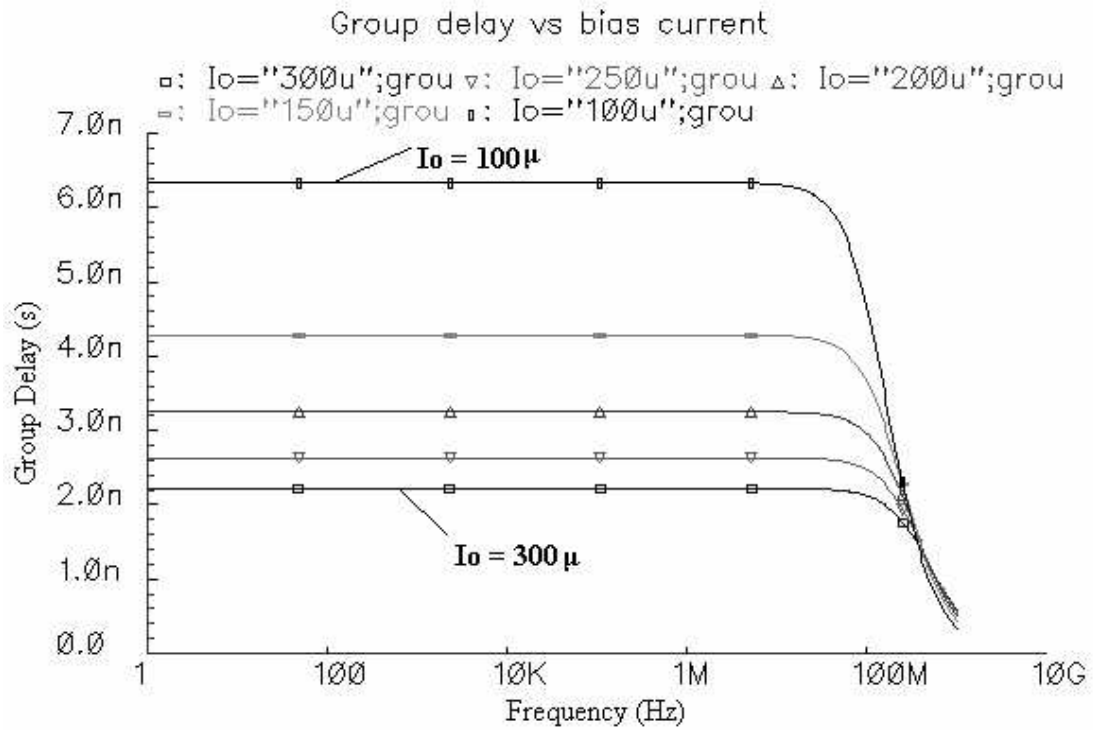


Figure 5.33 : Group Delay of Log Domain Gm-C Filter for Different Bias Currents

The bias current of the LC ladder filter is changed from 100µA to 300µA. So for Gm-C cascaded filter the same bias tuning range is used. The cutoff frequency change for different bias currents is shown in Figure 5.34.

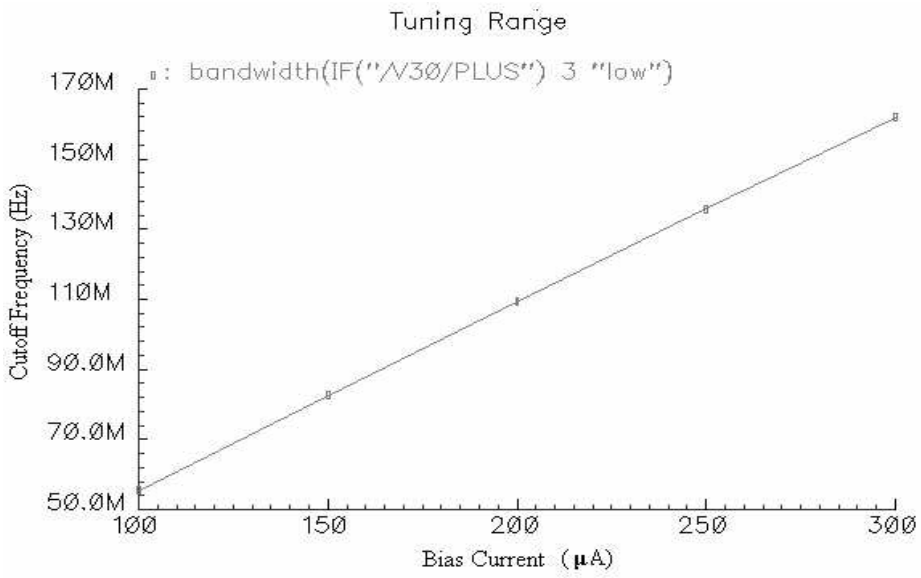


Figure 5.34 : Tuning Range of the Gm-C Filter

Thanks to the low distortion output stage, THD values for the filter are below % 1 for input amplitudes up to 100 μA and frequencies up to 20MHz. The THD results of the filter are summarized in Table 5.14 and Table 5.15.

Table 5.14 : THD values for Different Input Frequencies

Input Frequency	THD (%)
1 MHz	0.1
10MHz	0.15
20MHz	0.6
40MHz	2.5
80MHz	9

Table 5.15 : THD Values for Different Input Amplitudes

Input Amplitude	THD (%)
10μA	0.1
20μA	0.2
50μA	0.5
100μA	0.9

5.6 Comparison of Designed Filters: LC Ladder vs Gm-C

Two 7^{th} order programmable filters are designed with two different methods. In first design an LC ladder prototype is simulated topologically in log domain. 4 different log domain transconductor cells are used in the design. The overall filter performance specifications are observed. In second design Gm-C cascading method is used for a 7^{th} order log domain filter. A log domain transconductor cell is modified and an integration capacitor is added to form a transconductance-capacitor (Gm-C) structure. After that proper capacitor values chosen and Gm-C cells are cascaded to obtain high order filter behavior. Again various aspects of the filter are observed. In this section a comparison will be given. Since the main difference between LC ladder and Gm-C cascading methods is their sensitivity to element tolerances, that fact will be also checked. The two filters are compared extensively in Table 5.16

Table 5.16 : Comparison of Designed Filters

	7^{th} Order LC Ladder Filter	7^{th} Order Gm-C Cascaded Filter
Number of Log Domain Transconductor Cells	34	9
DC Current Consumption @Ibias =100μA	20 mA	3 mA
Supply Voltage	3.3 V	3.3 V
Tuning Range	55 MHz - 140MHz	55MHz - 165MHz
Passband gain	7 dB (variable)	0dB (constant)
Group Delay Flatness	$\leq 1.5\ f_C$	$\leq\ f_C$
Boost Programming Feature	Yes	No
% THD @10μ 1MHz input signal	0.25 %	0.1 %
Element Tolerance Sensitivity $\Delta C \leq 50$ %	Maximum Cutoff Frequency Drift $\Delta f_C = 20$MHz	Maximum Cutoff Frequency Drift $\Delta f_C = 29$MHz

The table summarizes most of the performance criterion. LC ladder filter has a disadvantage of having large number of transconductor elements, resulting in a higher DC power consumption. But as expected it has a better sensitivity to capacitor variations. For a 50 % variation of capacitor values (which is a very high value for AMS 0.35μ process), the filter cutoff frequency changes a maximum of 20 MHz, while this change for Gm-C filter is 29MHz (Figure 5.35). LC ladder has a novel boost programming mechanism which Gm-C filter hasn't. But it can be added to Gm-C filter as in [16]. Both filters have the advantages of log domain operation such as high dynamic range, high frequency and low power consumption. Also in both filters output stage is the proposed low distortion output stage. As a result THD values are below 1% for both. But Gm-C filter has slightly better THD. Design complexity is higher for LC ladder filter but the advantage of low sensitivity to element values worth it.

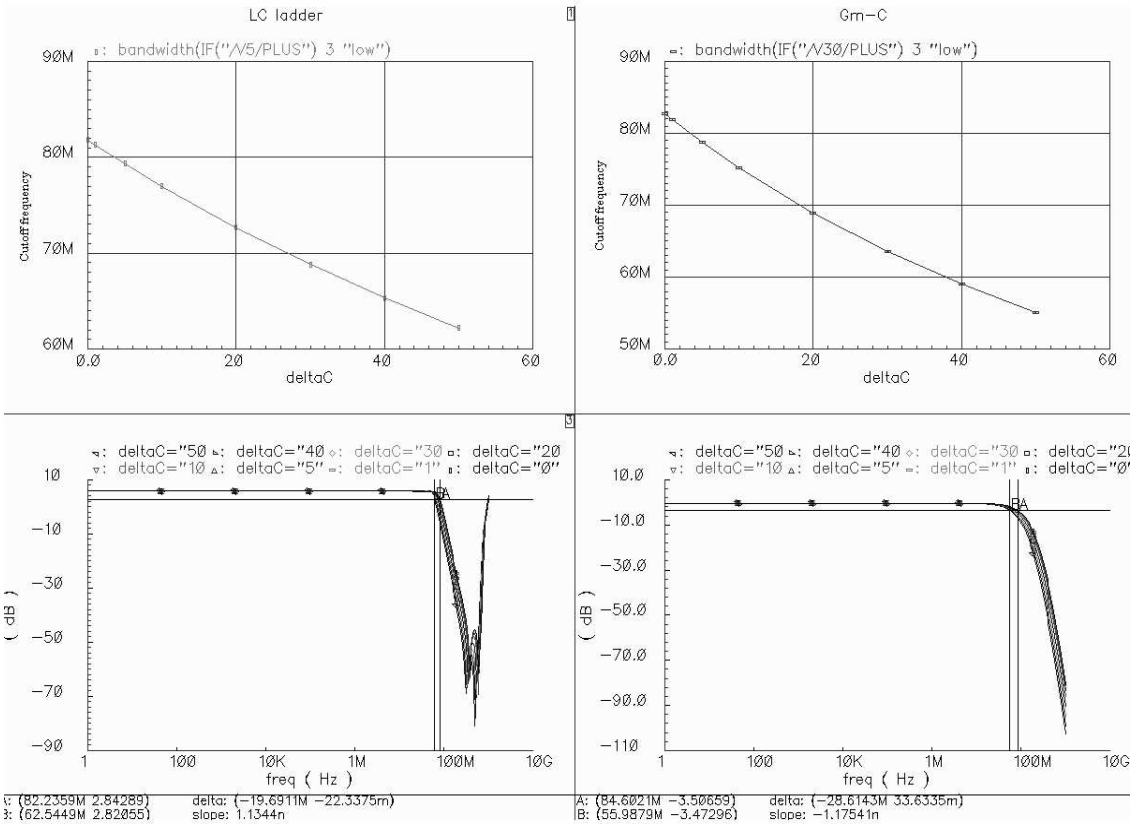


Figure 5.35 : Sensitivity of LC Ladder and Gm-C Filters to Capacitor Variations

5.7 Bias Circuit Design and Programmability

Biasing is a very important concept for filters, since many performance aspects depend on the value of bias current. Designed filters presented above need bias currents in both directions; sinking and sourcing. Both filters are tunable so the bias circuit current must be adjustable with a voltage value. To maintain all these requirements, the bias circuit seen in Figure 5.36 is designed. In that circuit the control voltage is sensed by an operational amplifier and applied to a reference current generating resistor. Then the current formed on this resistor is copied in both directions (sinking and sourcing). Finally the proper bias voltage is formed by properly placed diode connected MOSFETs. The biasing scheme uses the features of BiCMOS process. To get rid of the errors caused by nonzero base currents of bipolar transistors, MOSFETs are used as current sources.

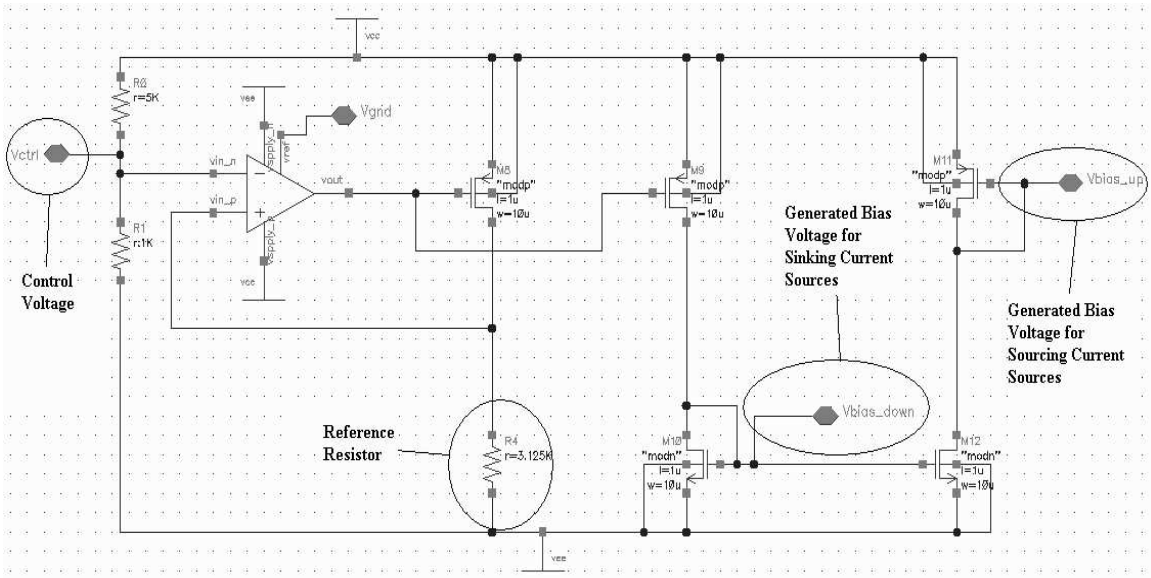


Figure 5.36 : Bias Circuit

A resistor divider is placed at the control voltage input of the circuit so that when no control voltage is applied to the circuit, the bias current remains at a constant default value.

A digital control interface can also be added to the filter. In order to provide digital control of bias current a DAC must be placed before the control voltage input of the circuit. A possible conceptual block diagram of the system with digital control interface is shown in Figure 5.37.

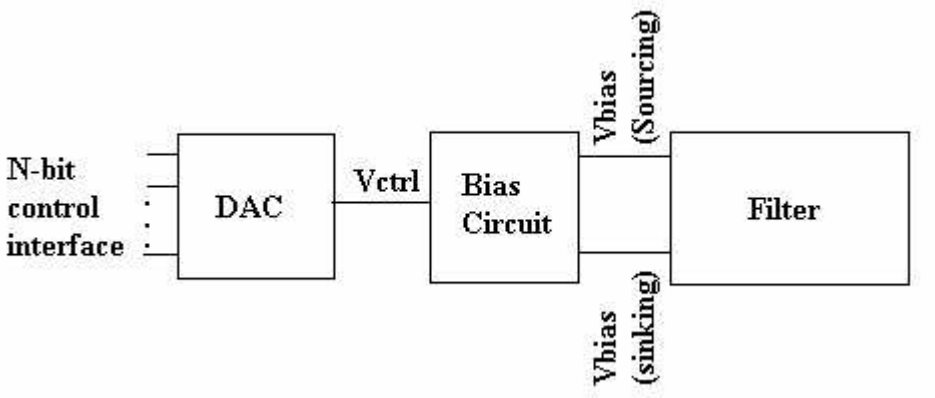


Figure 5.37 : A Possible Digital Control Interface for the Filters

6. CONCLUSION

The key concept of this thesis is to benefit from the various advantages of log domain filtering. For this reason different design methodologies for log domain filters are investigated. Advantages and disadvantages of these design methods are summarized. LC ladder simulating filters have the advantage of being less sensitive to element tolerances. On the other hand they are difficult to design and their programming is not as easy as in Gm-C cascaded filters. Also LC ladder simulating filters THD values are lower than Gm-C cascaded filters.

In this work LC ladder simulating log domain filter, suitable for hard disk drive applications, is designed. Its characteristic properties (AC gain, group delay, THD, programming range) are investigated. Nonideal effects on the filter performance are modeled. A low distortion expanding stage and new programming scheme is proposed. Designed filter has a wide tuning range (55MHz -140MHz), low THD value (< 1 %), satisfactory group delay ripple and a programmable boost feature. And still it has less sensitivity to element tolerances, thanks to the LC ladder simulating topology. In order to compare performances a Gm-C cascaded log domain filter is also designed and its characteristic properties are investigated. All designs are made using 0.35µ AMS SiGe BiCMOS process.

Still some extra work can be done, in order to decrease the power consumption of the LC ladder simulating filter. Since it has more exponential transconductor cells compared to Gm-C cascaded filter, its power consumption is higher.

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BIOGRAPHY

Burak Dündar was born in Bursa in 1983. He graduated from Istanbul Atatürk Science High School. In 2005 he received B.Sc. degree in Electronics Engineering from Istanbul Technical University. He is still pursuing his M.Sc. degree in Electronics Engineering at Istanbul Technical University. He has worked at TUBITAK UEKAE as Researcher. He is still working at Hittite Microwave Corporation Istanbul Design Center as a Design Engineer. His main interests are RF and mixed signal integrated circuit design.